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(54) **LIQUID CRYSTAL DISPLAY PANEL**

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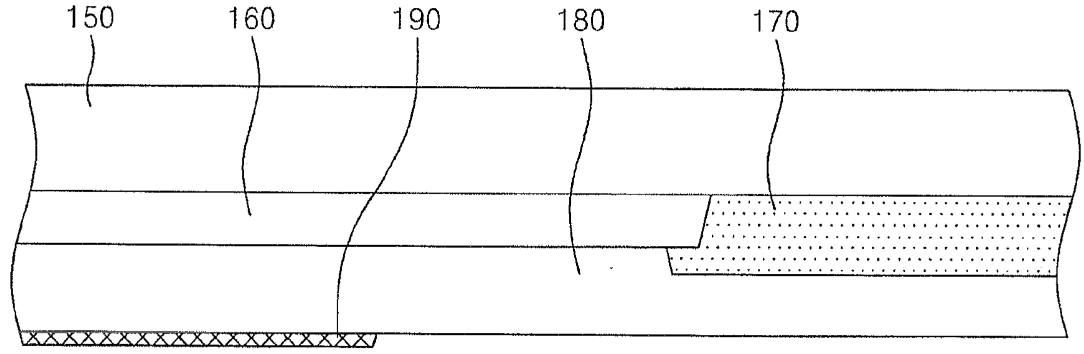
(52) **U.S. Cl.** **349/39**

(57) **ABSTRACT**

A liquid crystal display (LCD) panel includes: a first base substrate; a plurality of gate lines and a plurality of data lines disposed on the first base substrate and crossing each other; a pixel electrode pattern disposed on the first base substrate; a storage pattern disposed on the first base substrate, the storage pattern being positioned between consecutive gate lines and substantially in parallel with the gate lines; a second base substrate; a common electrode disposed on the second base substrate and alternately positioned with the pixel electrode; and a liquid crystal layer disposed between the first and second base substrates.



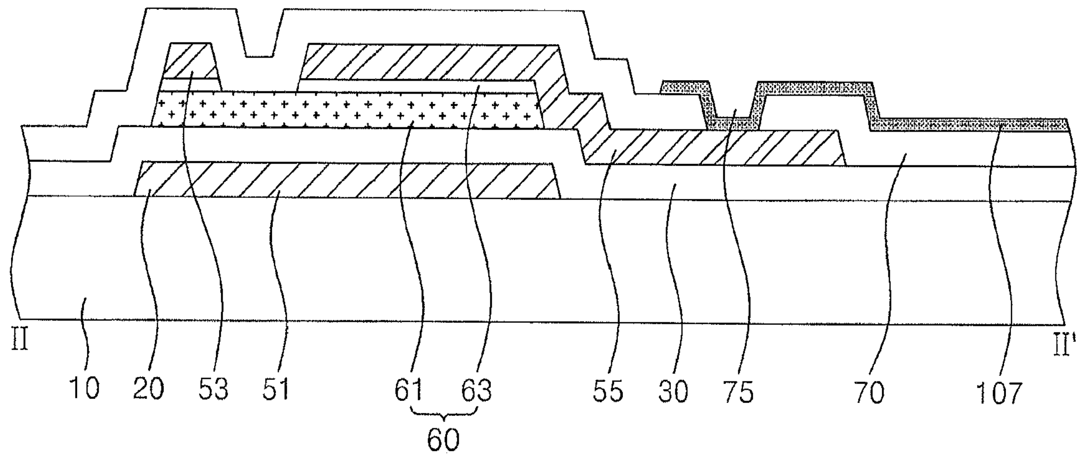


FIG. 1

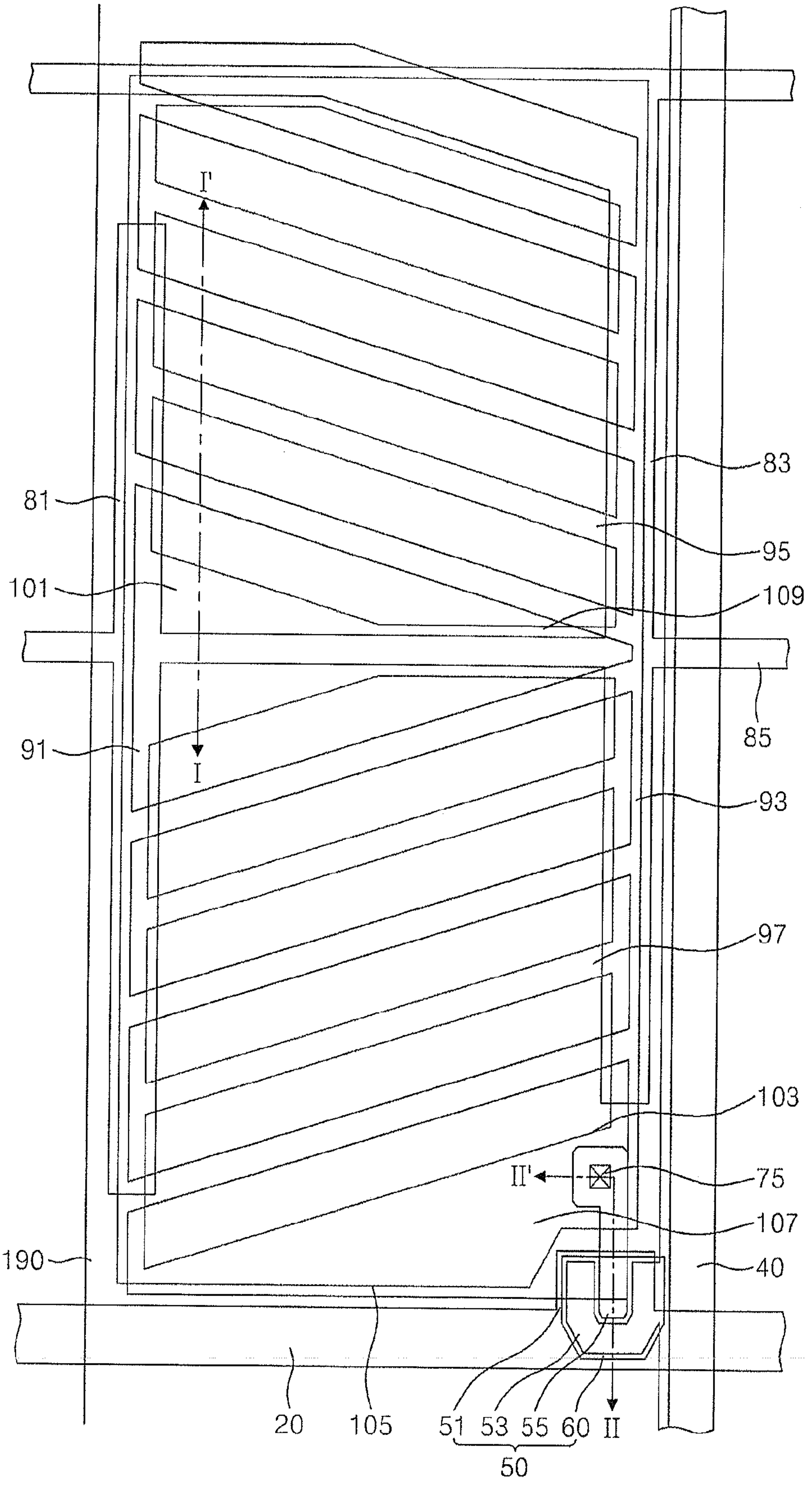

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FIG. 2A

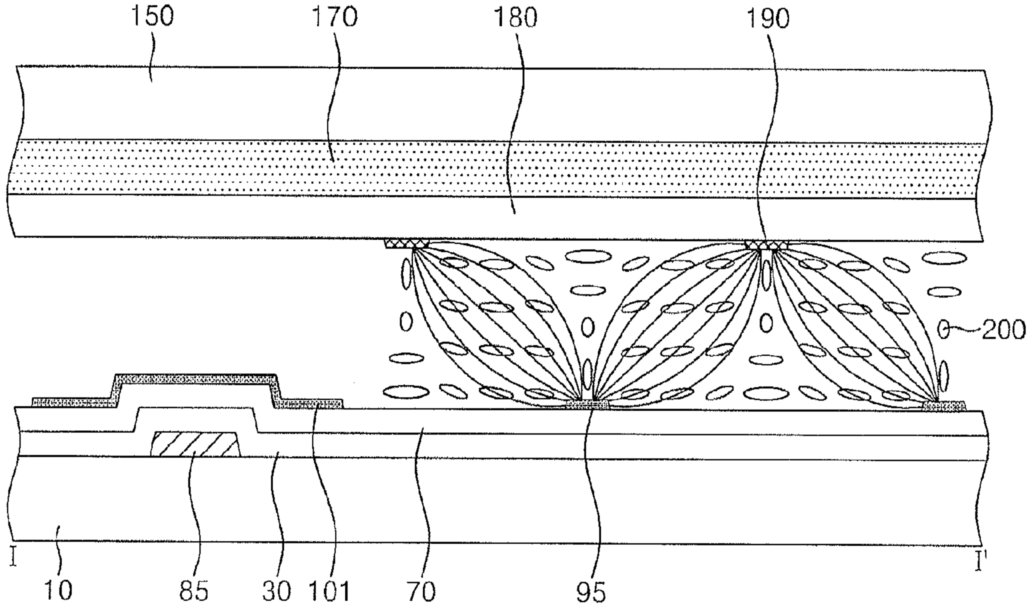

FIG. 2B

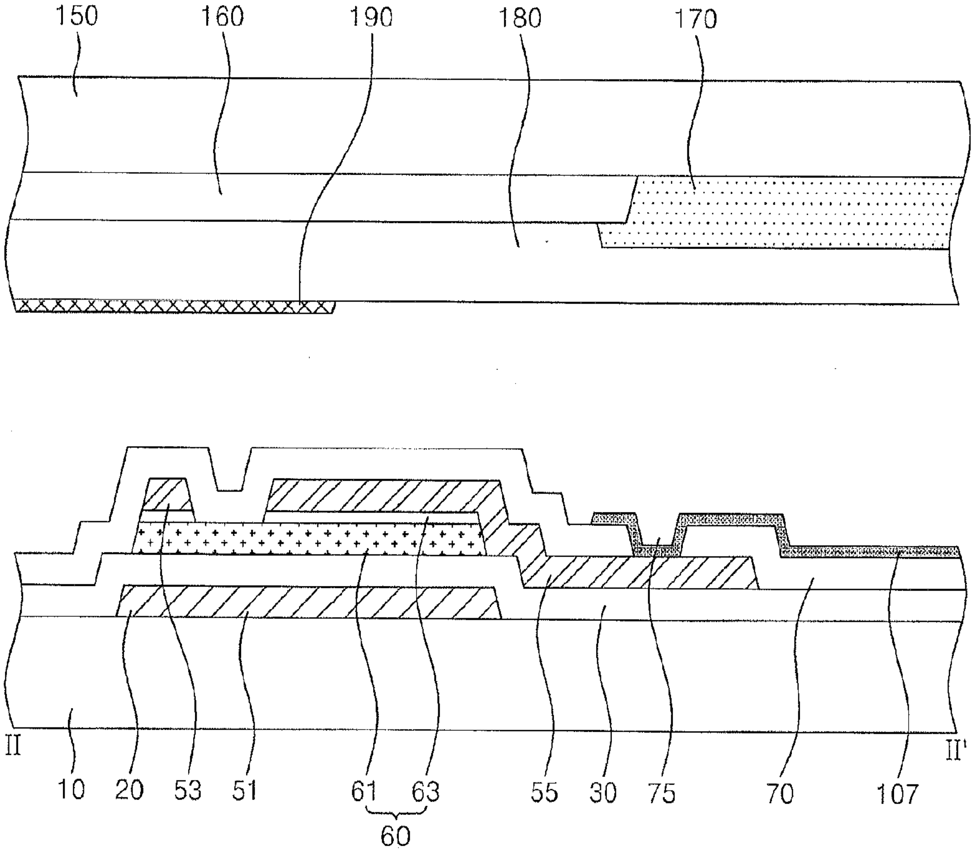

FIG. 3

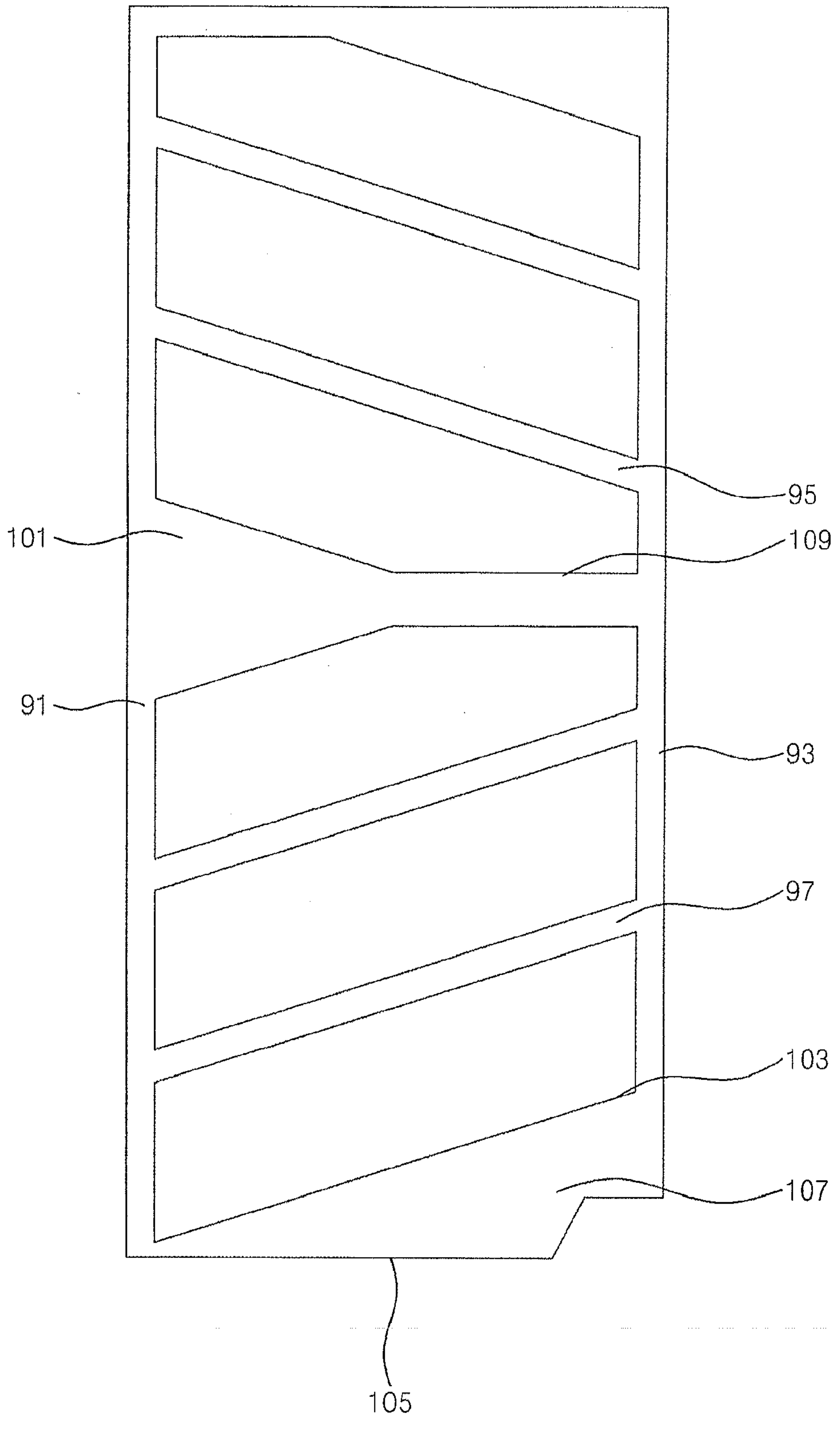

FIG. 4A

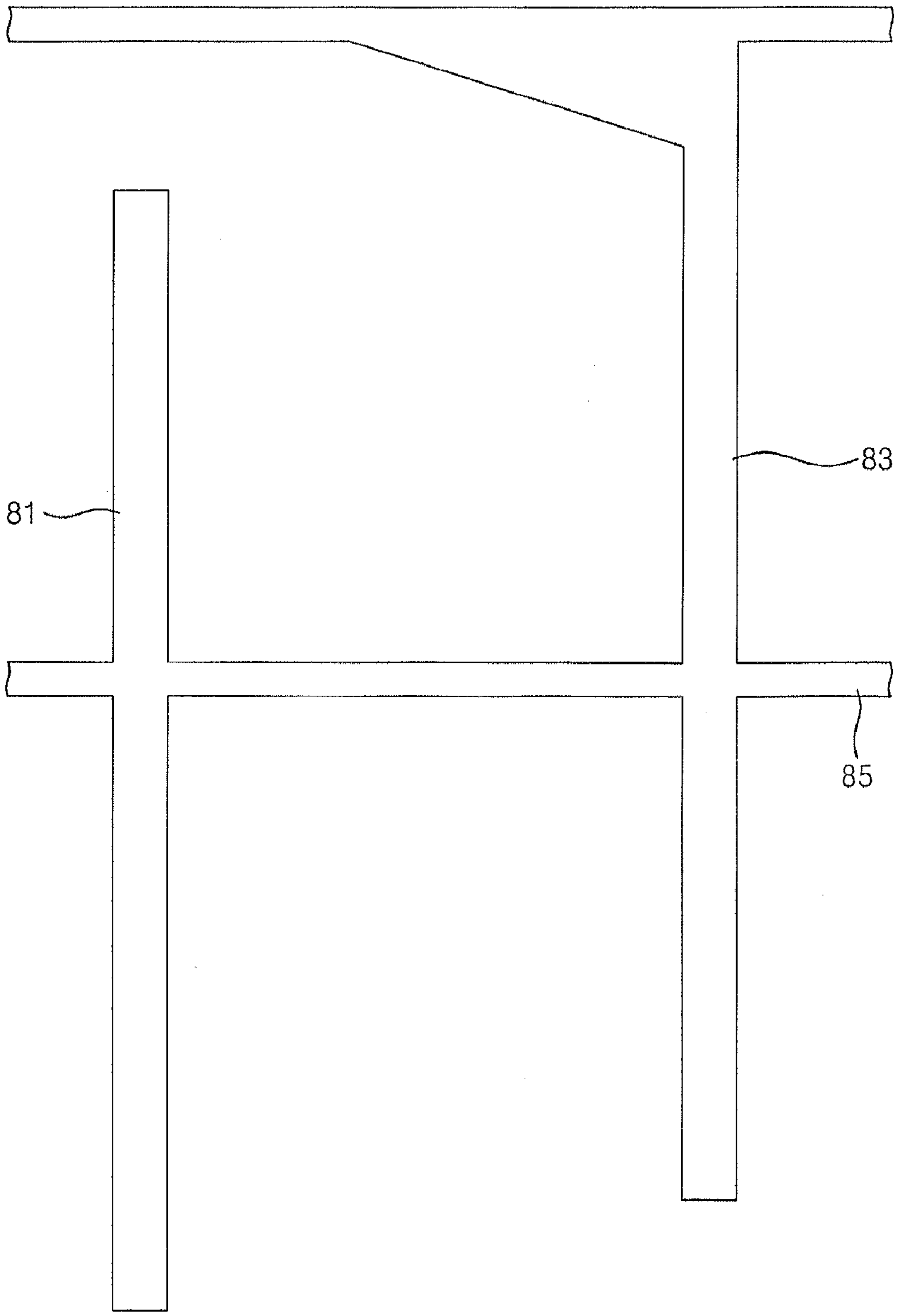

FIG. 4B

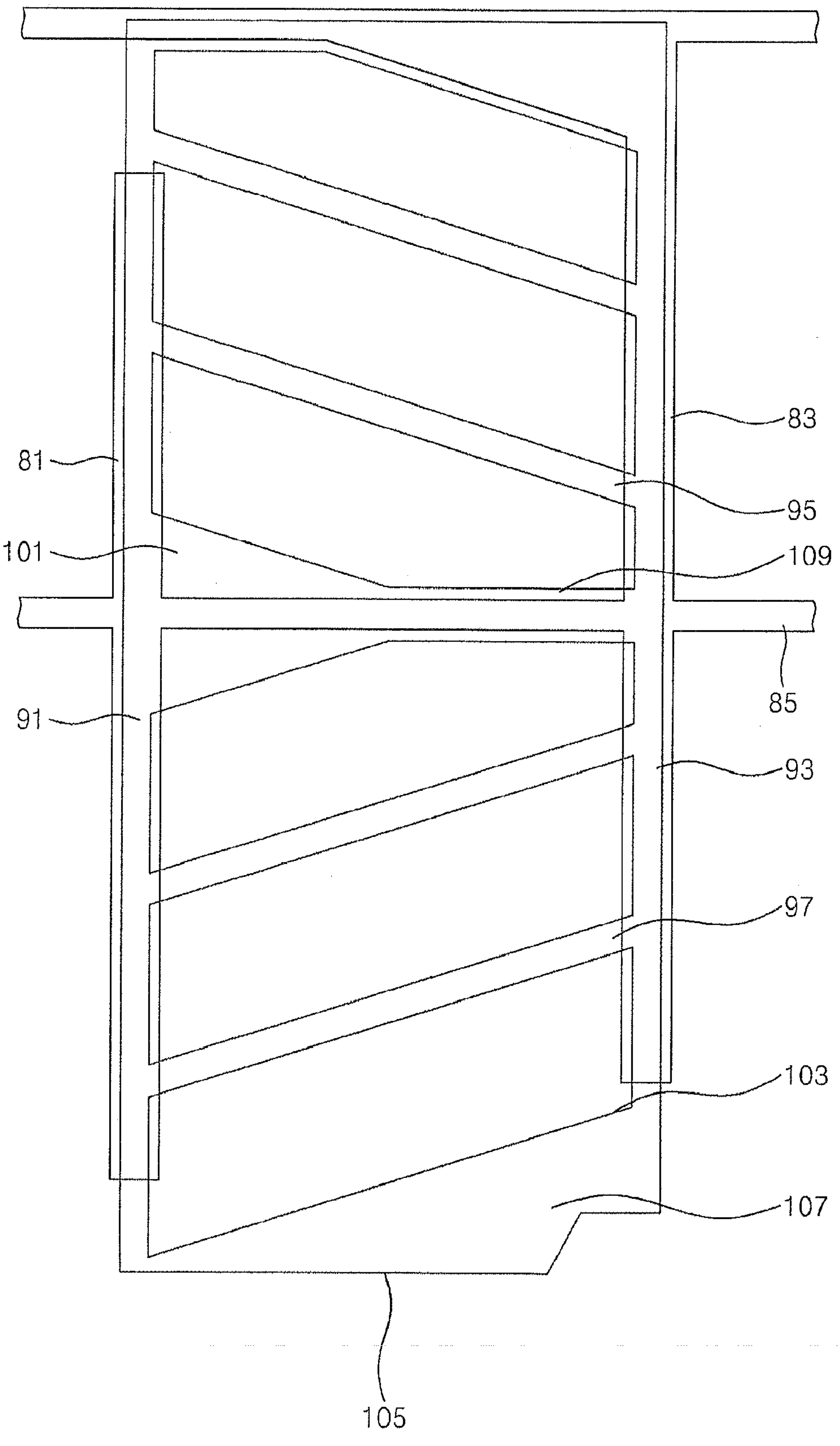

FIG. 5A

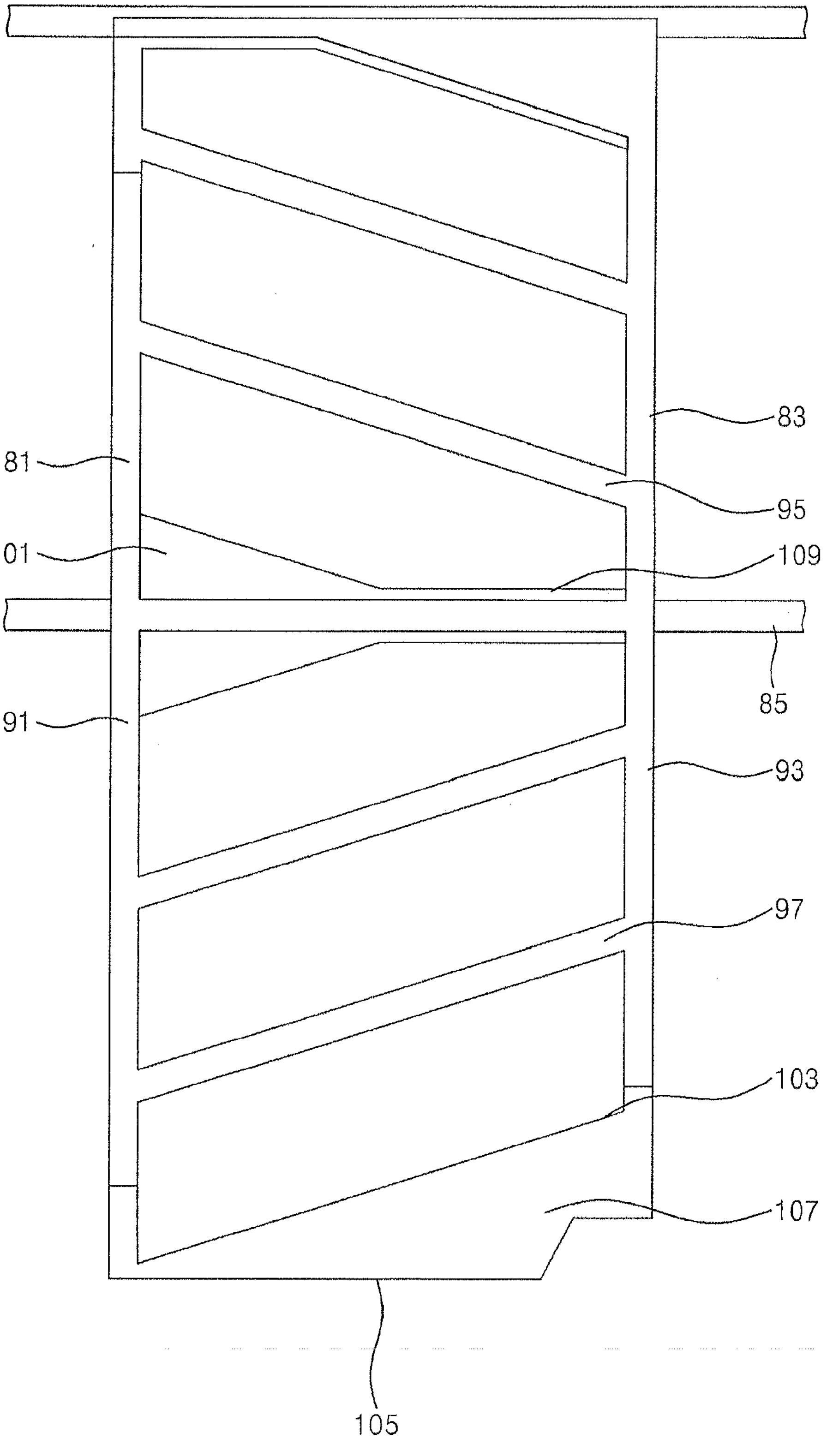

FIG. 5B

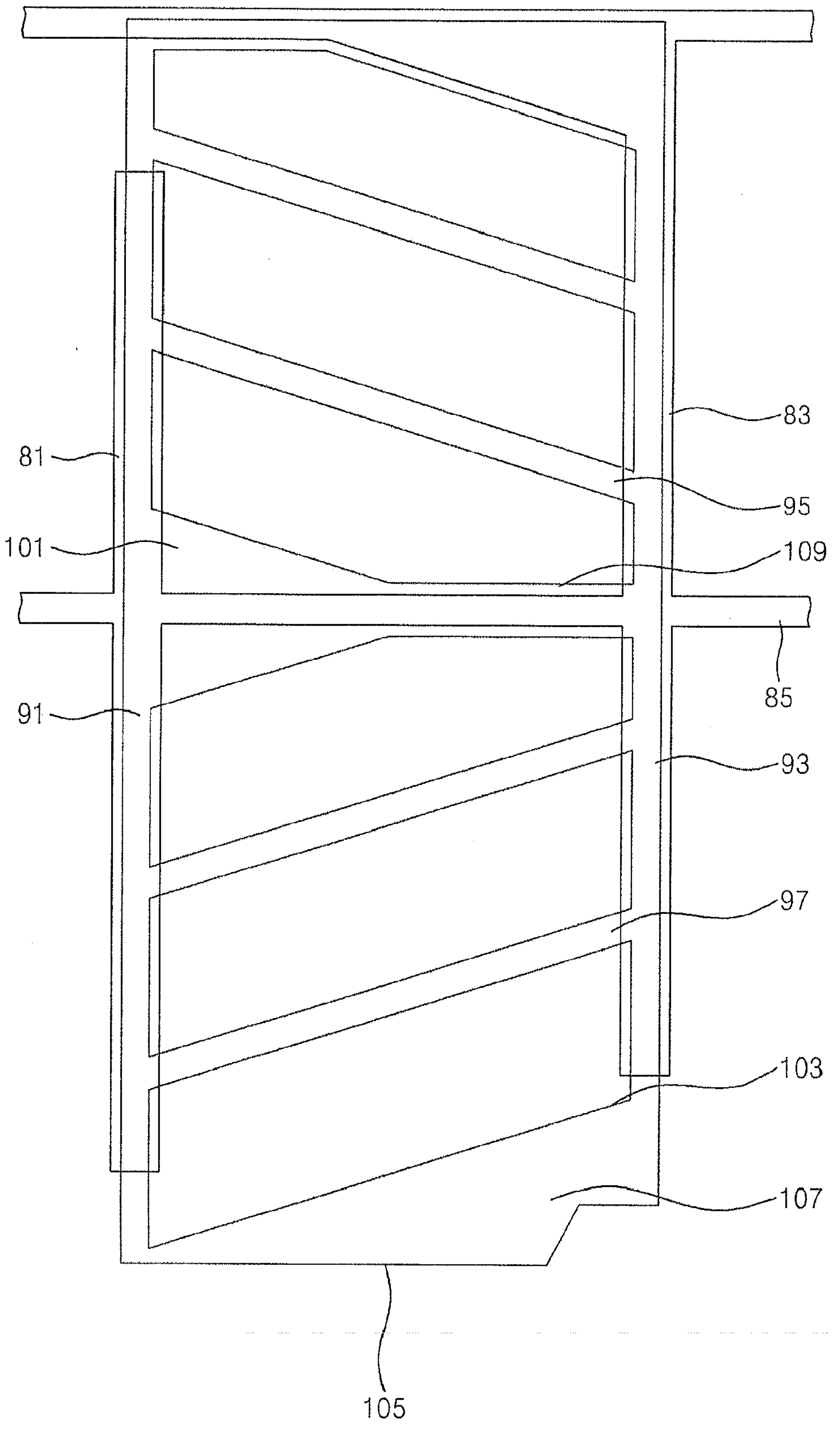

FIG. 6A

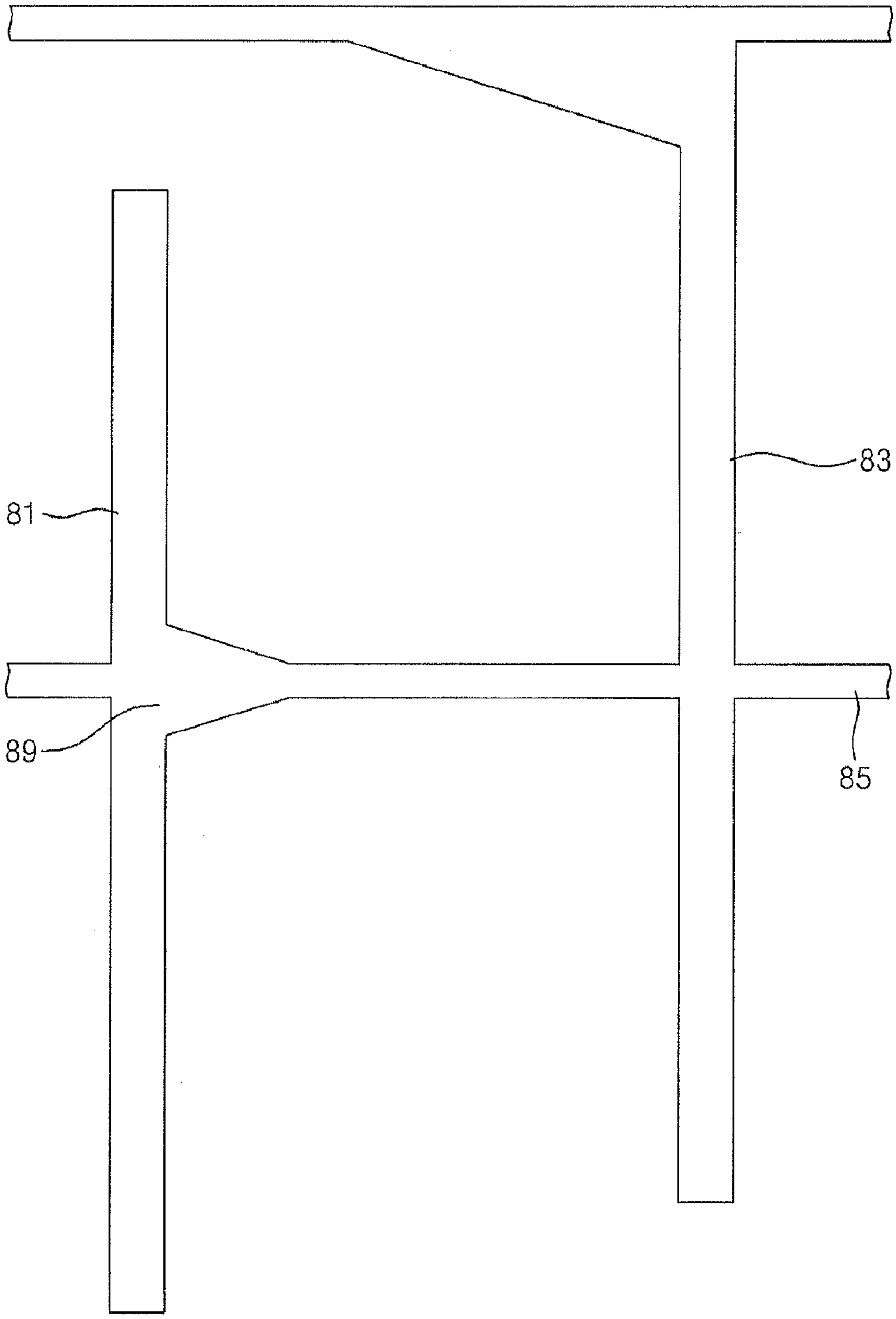

FIG. 6B

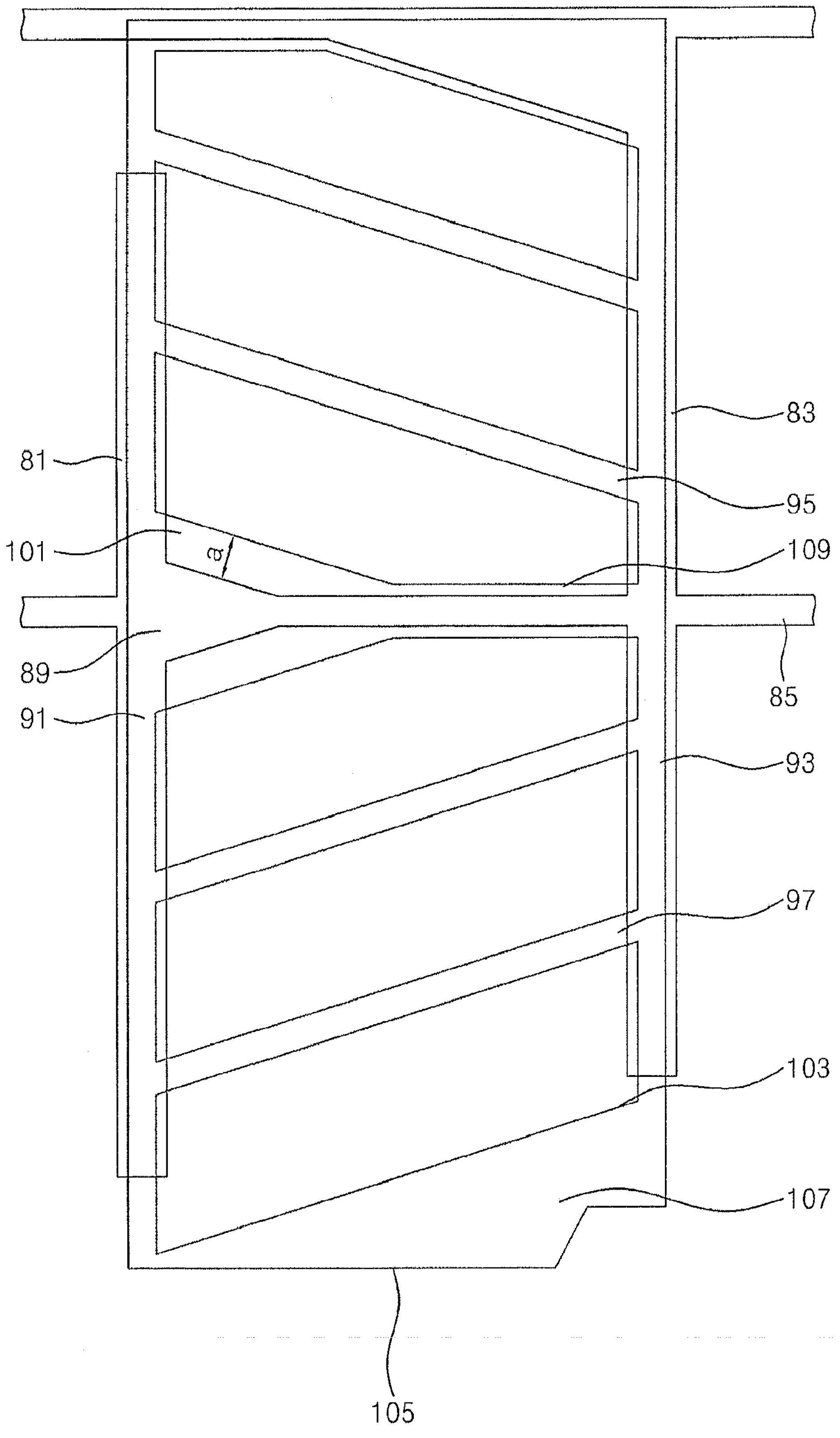

FIG. 7A

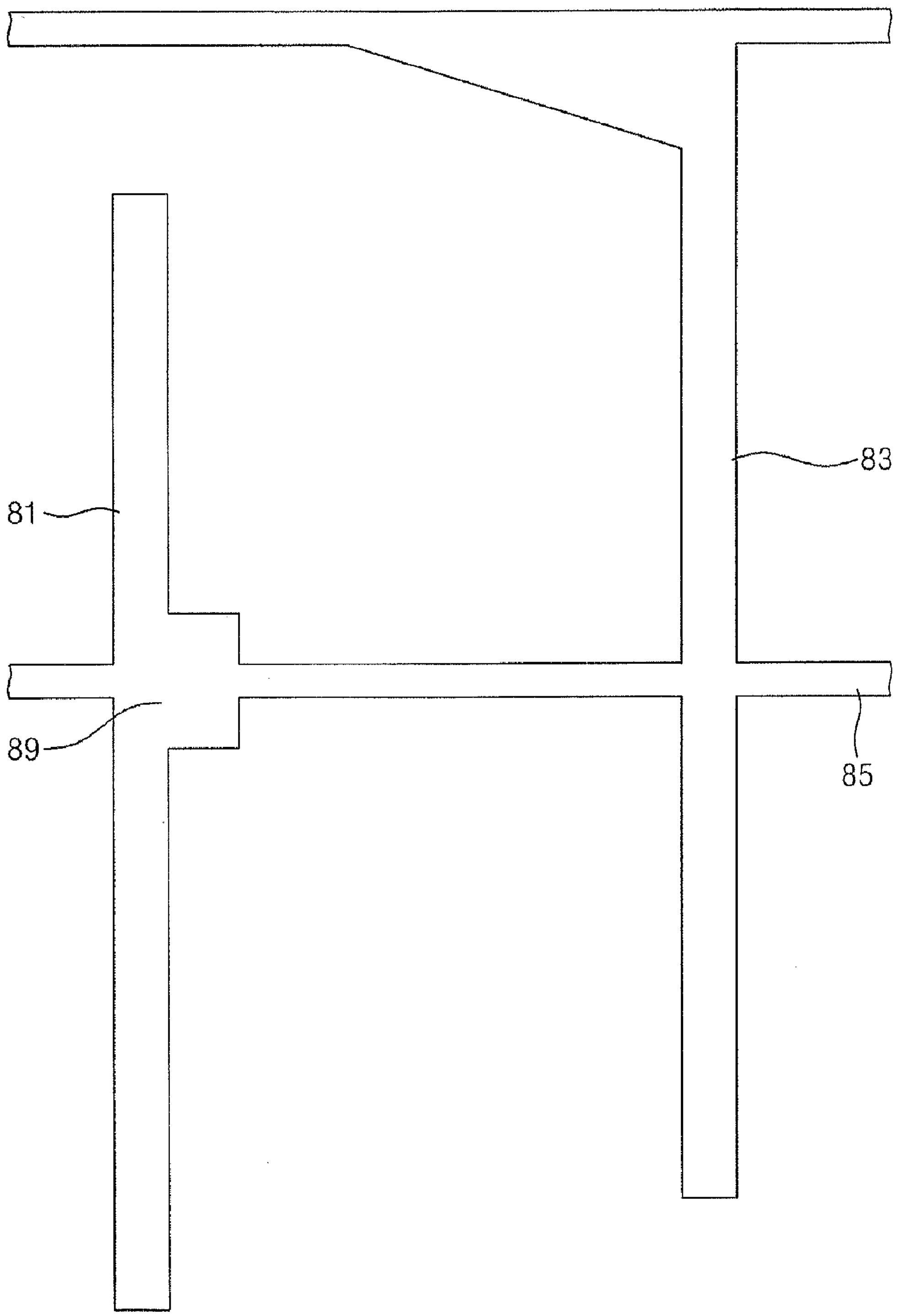

FIG. 7B

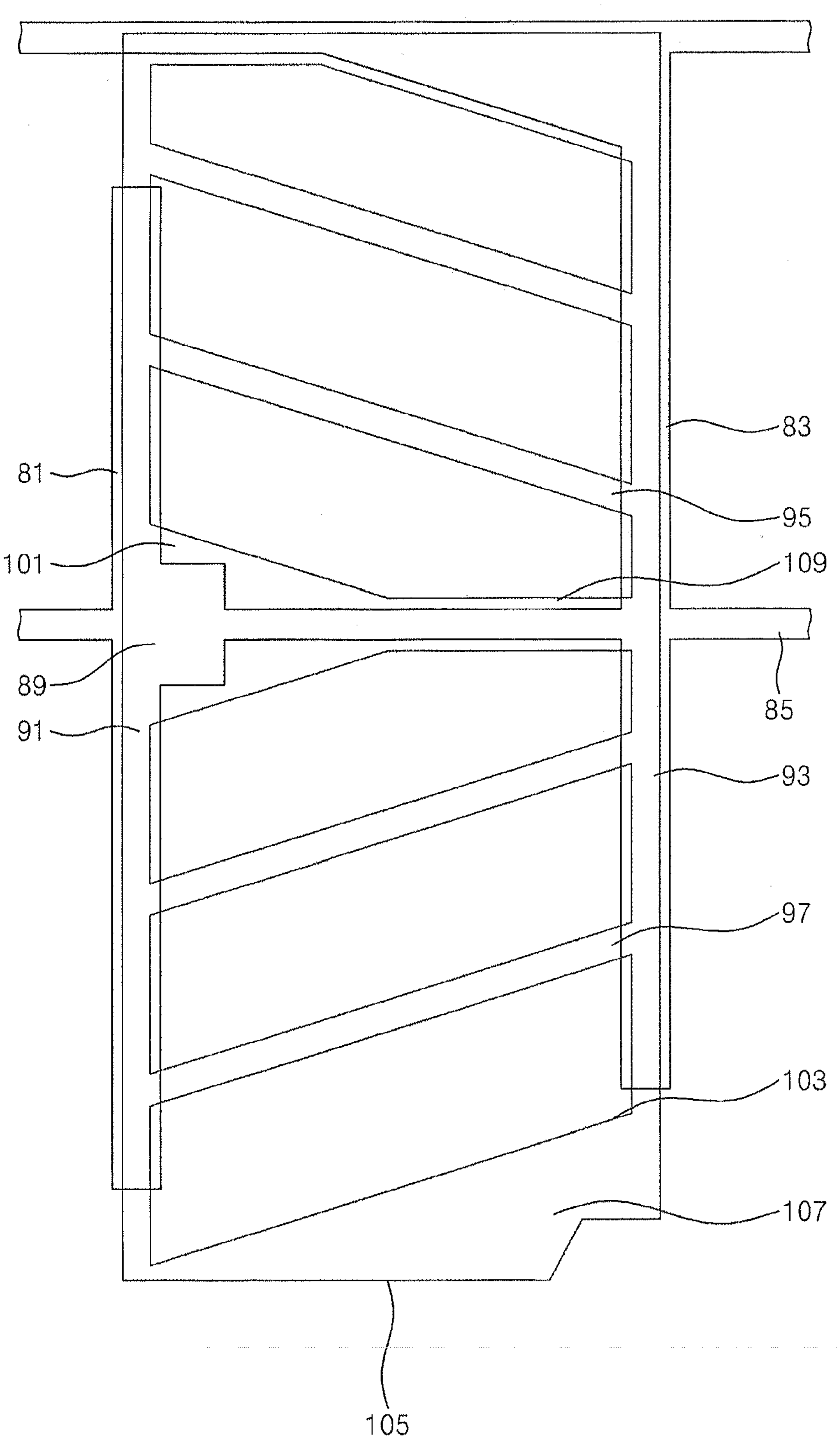

FIG. 8

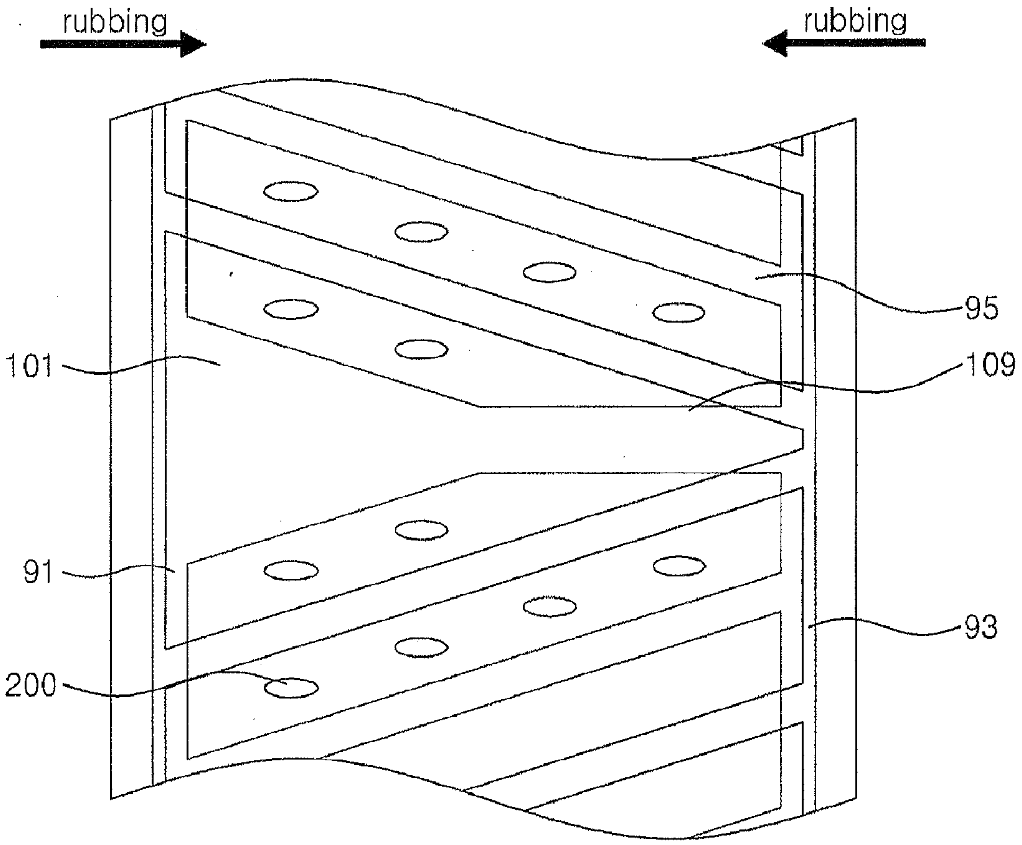

FIG. 9

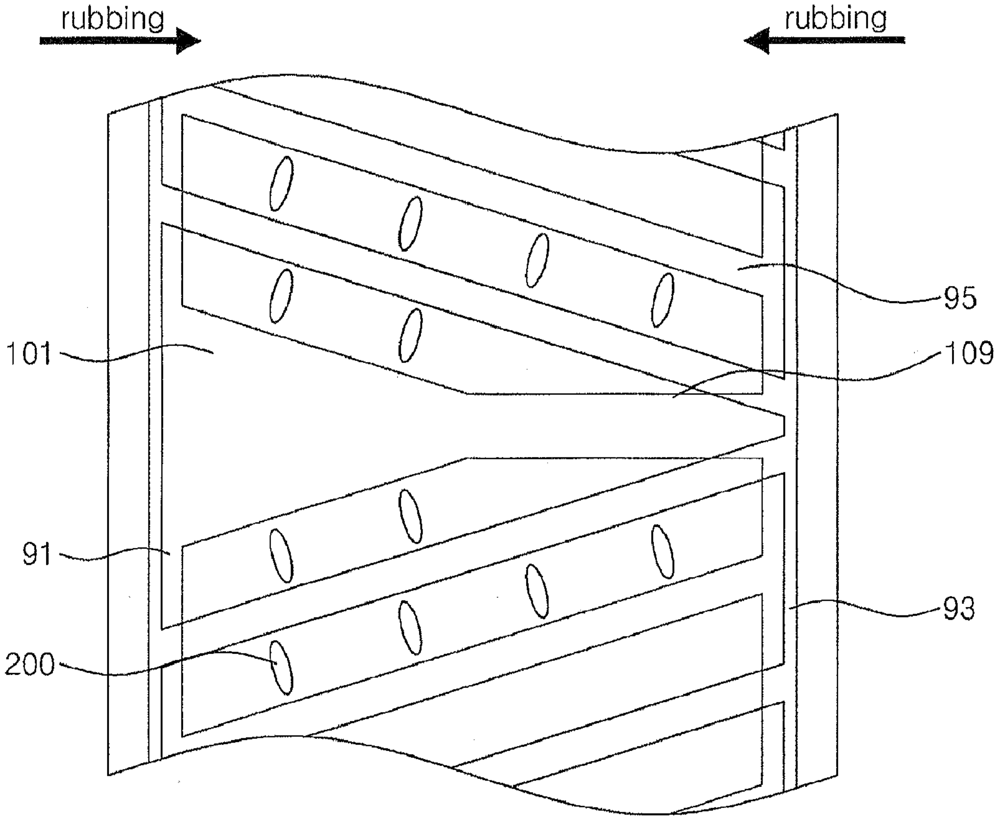

FIG. 10

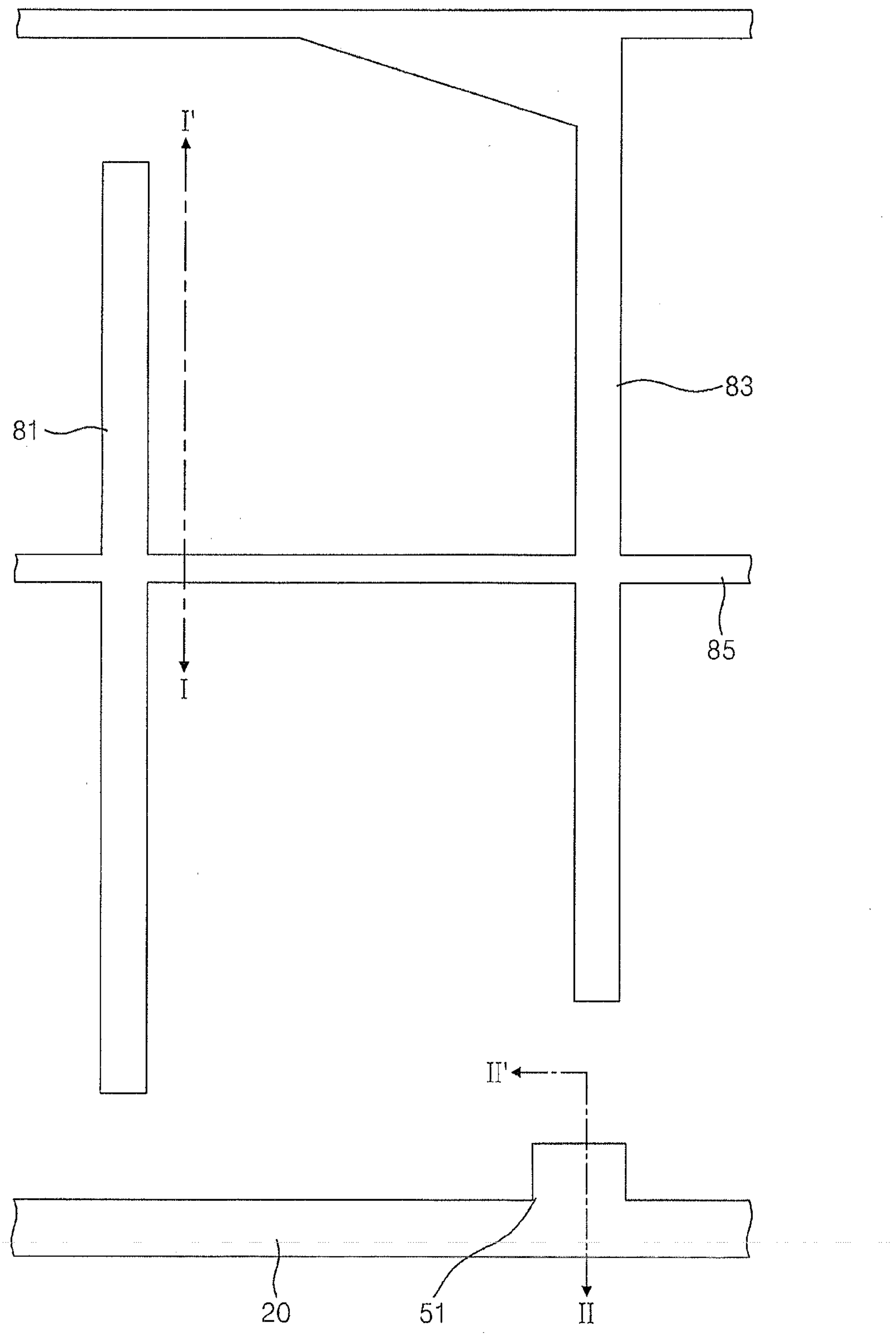

FIG. 11A

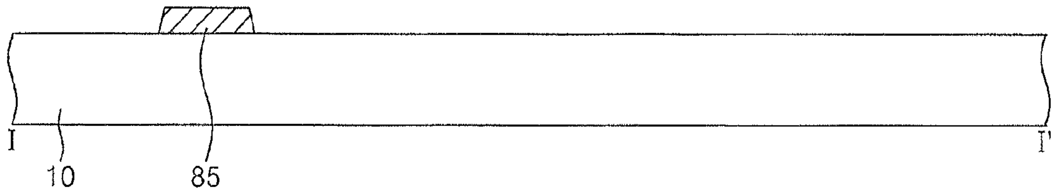

FIG. 11B

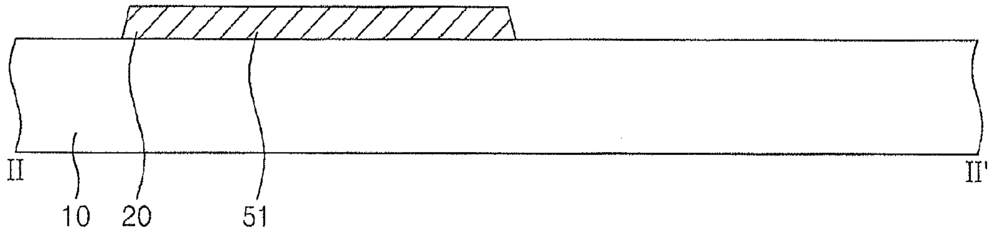

FIG. 12

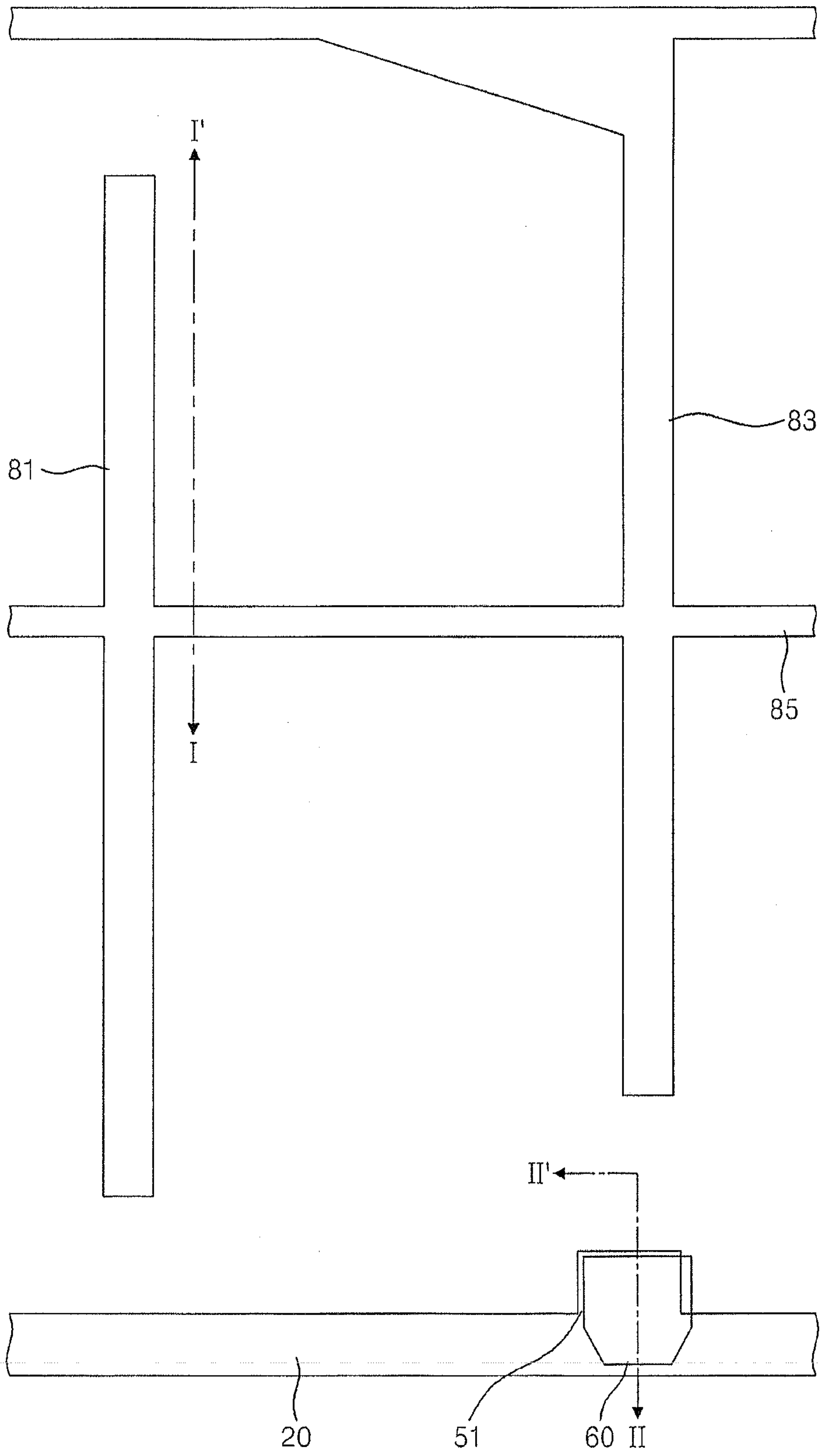

FIG. 13A

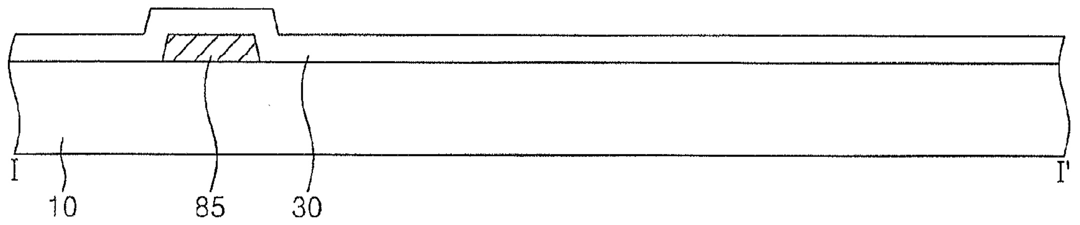

FIG. 13B

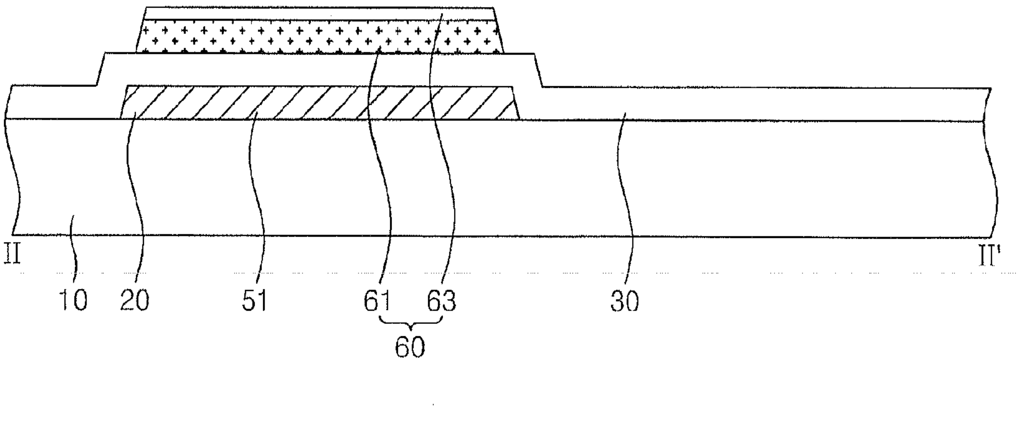

FIG. 14

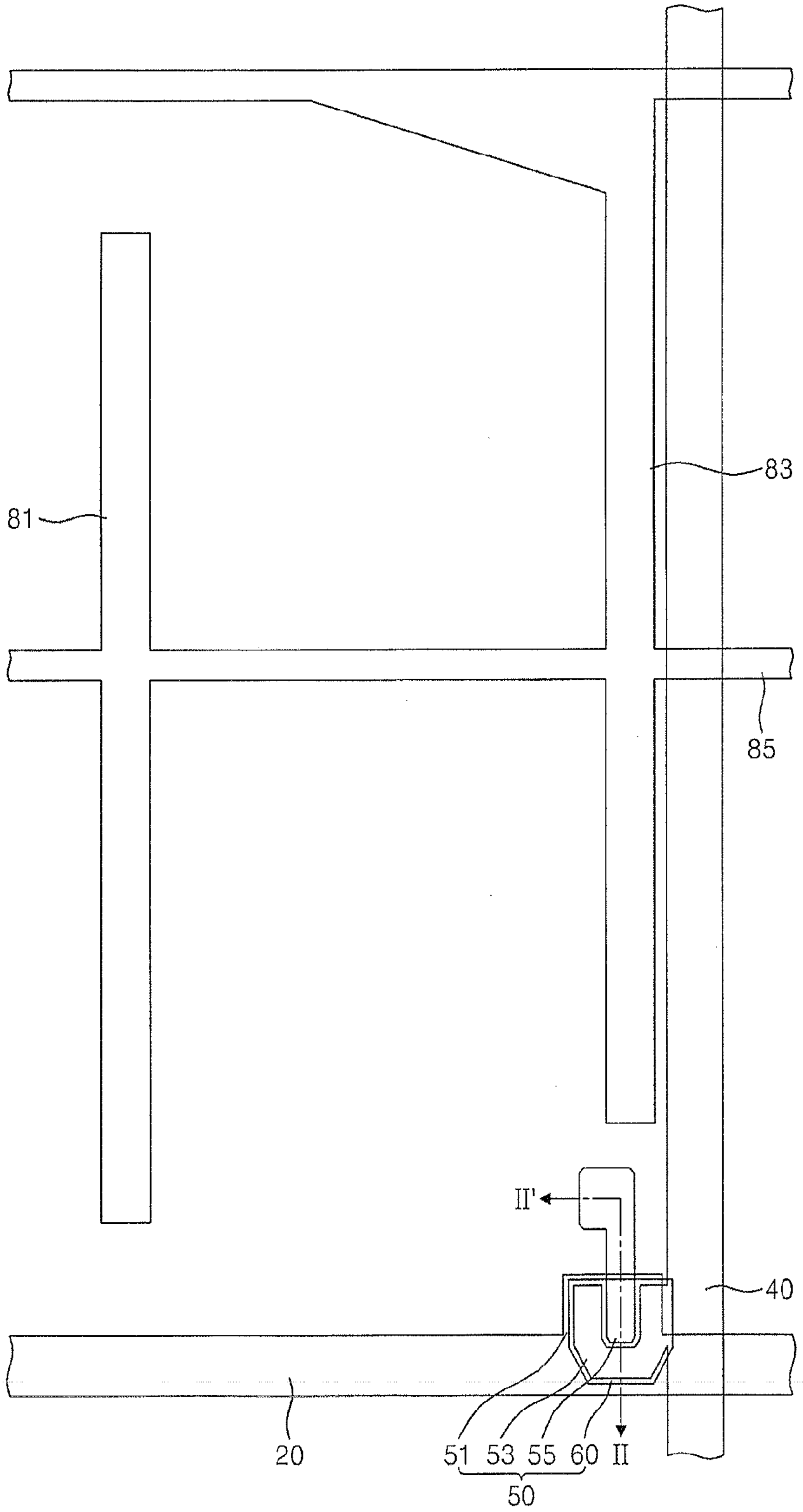

FIG. 15

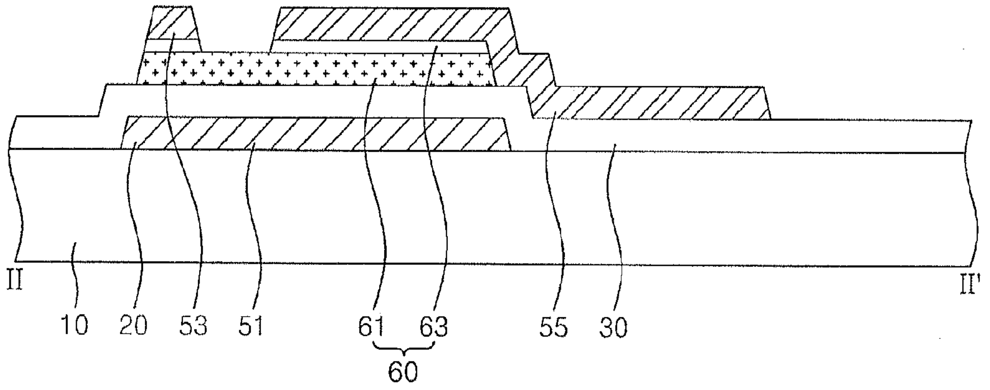

FIG. 16

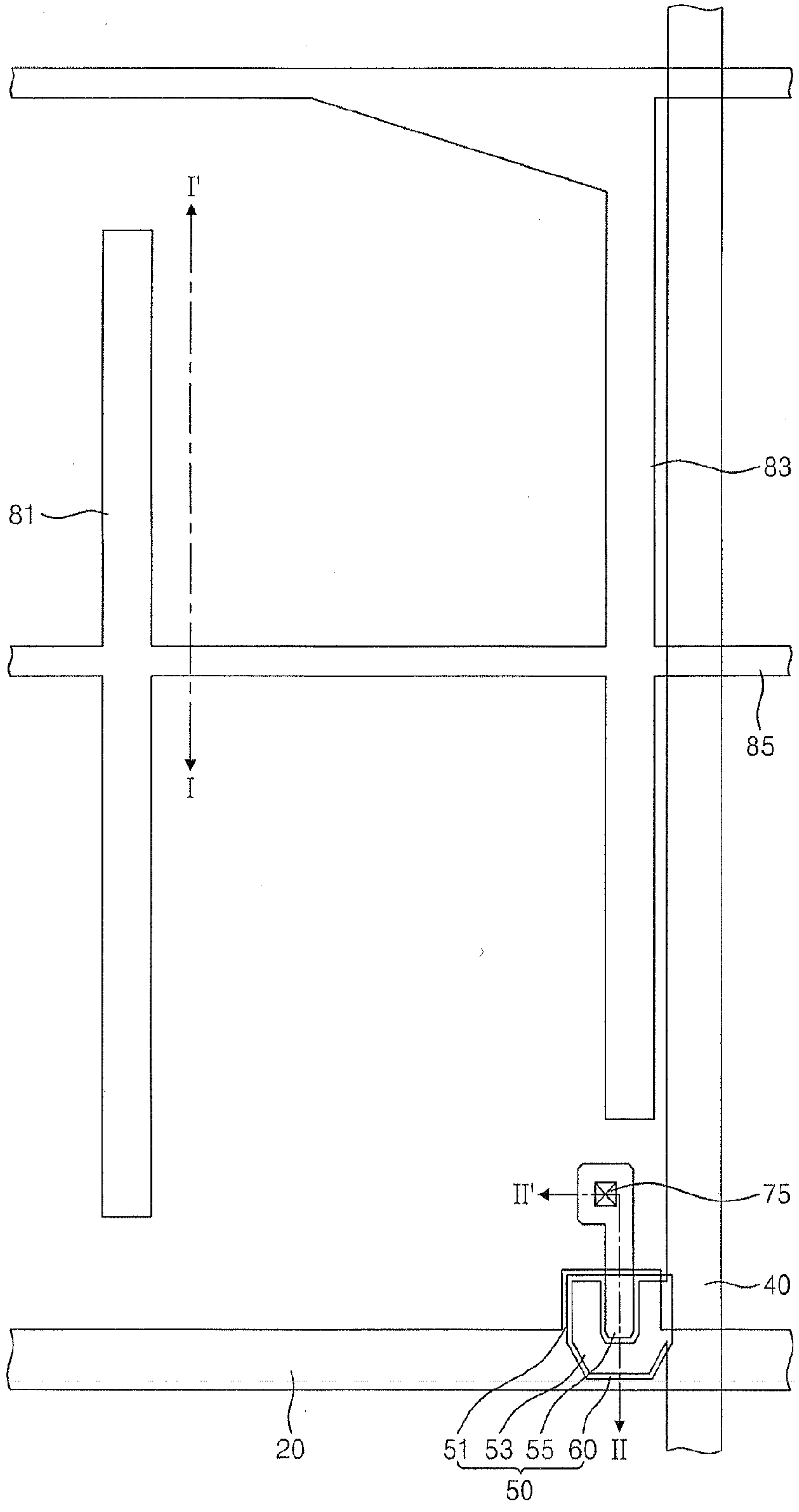

FIG. 17A

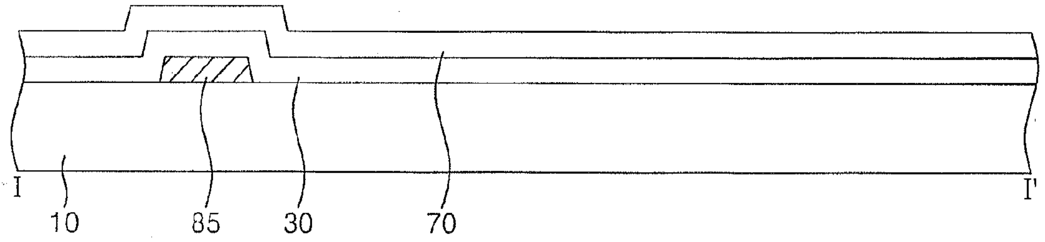

FIG. 17B

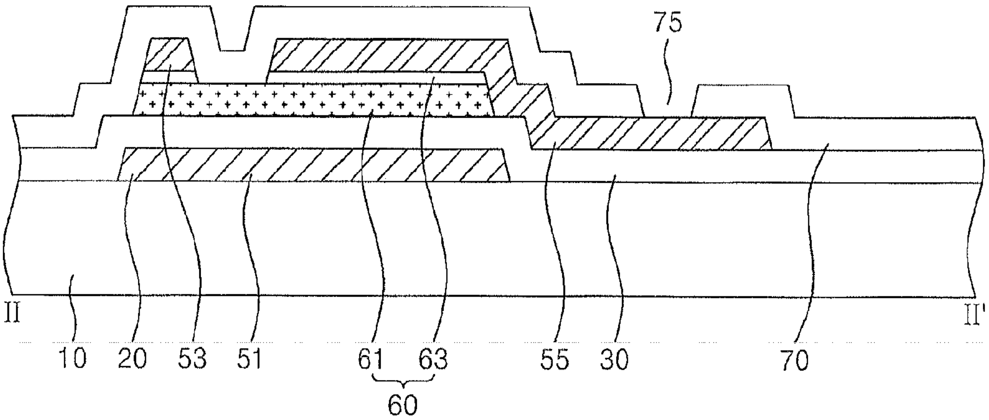

FIG. 18

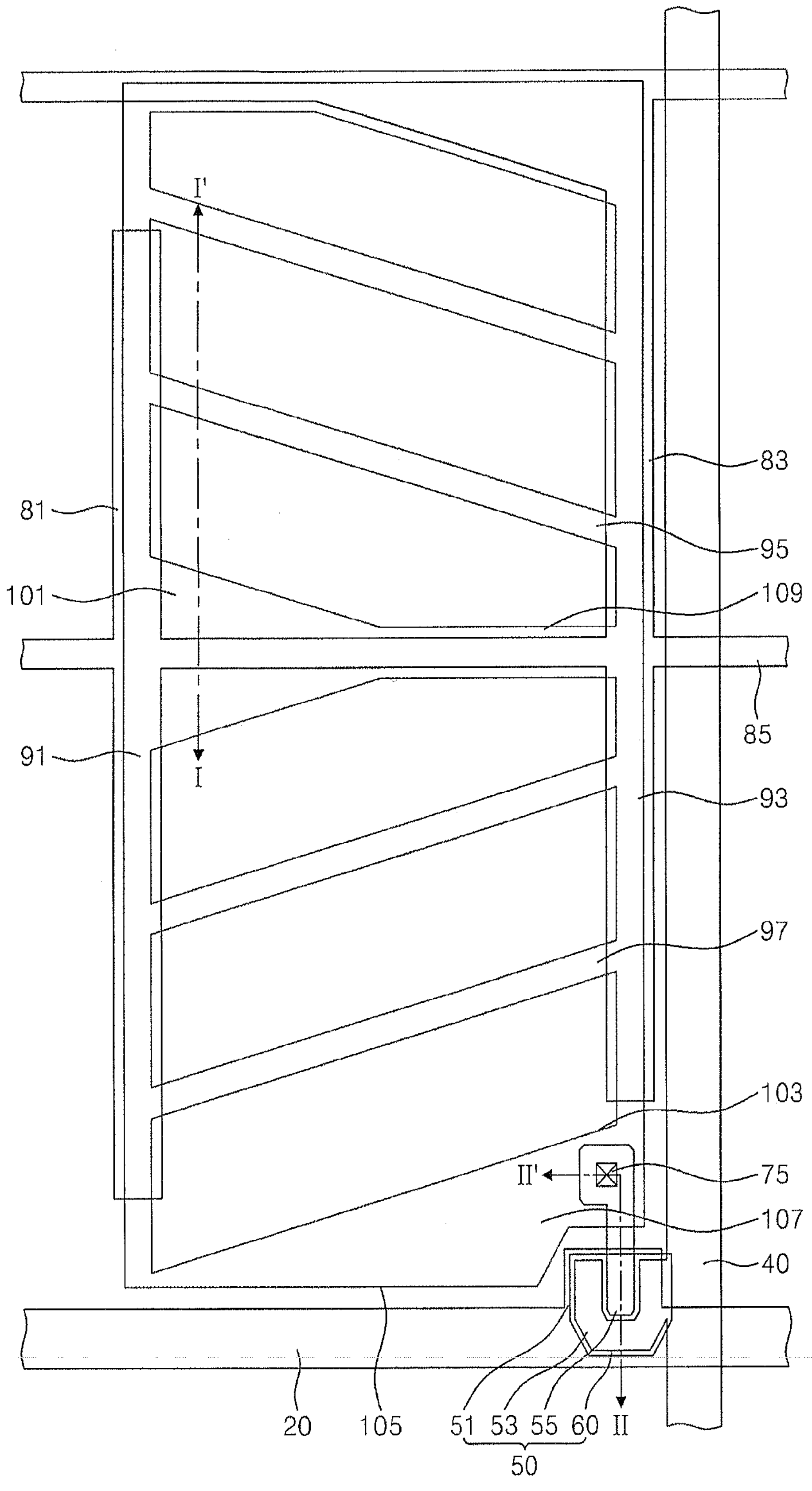
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FIG. 19A

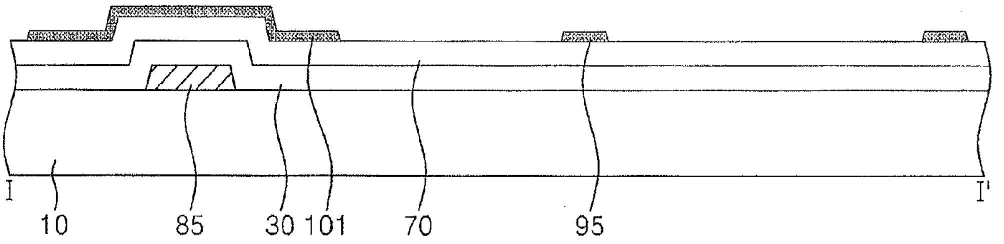
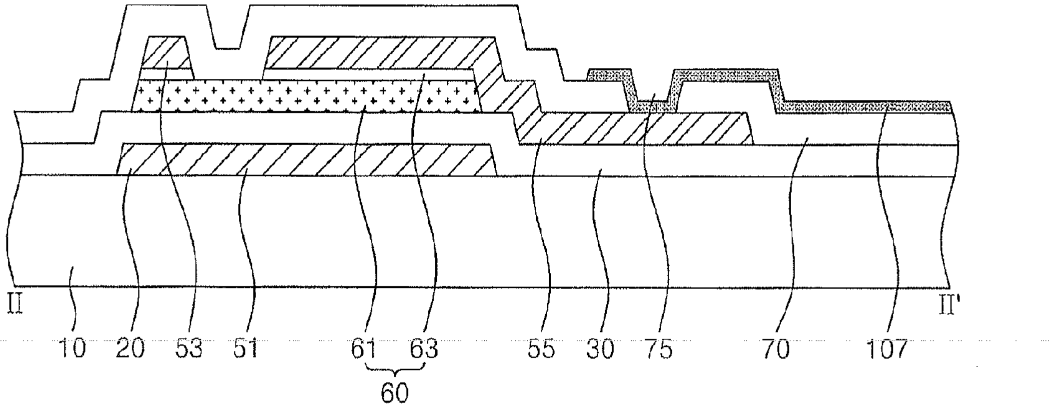


FIG. 19B



LIQUID CRYSTAL DISPLAY PANEL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. application Ser. No. 12/021,731 filed on Jan. 29, 2008, which claims priority to Korean Patent Application No. 10-2007-0009021, filed on Jan. 29, 2007, the disclosures of which are incorporated by reference herein in their entireties.

BACKGROUND OF THE INVENTION

[0002] 1. Technical Field

[0003] The present invention relates to a liquid crystal display (LCD) panel and, more particularly, to an LCD panel capable of preventing light leakage and texture generation.

[0004] 2. Discussion of the Related Art

[0005] A liquid crystal display (LCD) device displays an image by controlling light transmittance of respective liquid crystal cells arranged in a matrix form on an LCD panel according to video signals. To obtain a wide-viewing angle, the LCD device may employ, for example, a patterned vertical alignment (PVA) mode, an in-plane switching (IPS) mode, or a plane-to-line switching (PLS) mode.

[0006] In the PVA mode, a plurality of slits is formed on common electrodes and pixel electrodes of upper and lower substrates, and liquid crystal molecules located between the substrates are driven symmetrically with respect to the slits by fringe electric fields generated by the slits, thus forming a multi-domain structure.

[0007] In the IPS mode, a liquid crystal is driven by a horizontal electric field generated between a pixel electrode and a common electrode arranged in parallel on a lower substrate. In the IPS mode, the electrodes are formed on one substrate so that liquid crystal molecules are rotated in the plane of the same substrate and, as a result, an optical axis of a liquid crystal layer is rotated relative to the substrate.

[0008] In the PLS mode, a common electrode and a pixel electrode are provided in each pixel area with an insulating layer interposed therebetween to form a fringe electric field thereby causing all liquid crystal molecules filled between upper and lower substrates to be operated in the respective pixel areas.

[0009] However, in the IPS and PLS modes, residual images are generated and light transmittance is lowered since the electric fields are generated by the electrodes formed on one substrate. Moreover, in the PVA mode, the aperture ratio is low.

[0010] As an alternative to IPS, PLS and PVA, a dual field switching (DFS) mode has been proposed. In the DFS mode, a liquid crystal is aligned horizontally or vertically to an electric field generated between electric patterns of upper and lower substrates. The DFS mode improves side visibility and light transmittance by using fringe electric fields generated between pixel and common electrodes patterned on upper and lower substrates.

[0011] However, in an LCD device employing the DFS mode, a step height is formed by a pixel electrode and a storage electrode, which results in light leakage. In addition, a black brightness is increased by the light leakage thereby causing the capacity of a storage capacitor to be decreased. Moreover, since it is difficult to control the liquid crystal arranged in a position where the pixel electrode and a drain electrode are connected, an undesirable texture is generated.

[0012] Accordingly, there exists a need for an LCD panel that is capable of preventing light leakage and texture generation.

SUMMARY OF THE INVENTION

[0013] In an exemplary embodiment of the present invention, a liquid crystal display (LCD) panel, includes: a first base substrate; a plurality of gate lines and a plurality of data lines disposed on the first base substrate and crossing each other; a pixel electrode pattern disposed on the first base substrate, the pixel electrode pattern comprising, a first electrode connection portion and a second connection portion arranged in parallel with each other, a first linear pixel electrode and a second linear pixel electrode arranged between the first electrode connection portion and the second electrode connection portion, a central electrode arranged between the first linear pixel electrode and the second linear pixel electrode, and a central portion connected to the central electrode, wherein the first linear pixel electrode and the second linear pixel electrode are inclined in a different direction from each other with respect to the gate lines, and the central electrode is formed in a substantially triangular shape; a storage pattern disposed on the first base substrate, the storage pattern being positioned between consecutive gate lines and substantially in parallel with the gate lines, wherein the storage pattern is a lower electrode of a storage capacitor; a second base substrate; a common electrode disposed on the second base substrate and alternately positioned with the pixel electrode; and a liquid crystal layer disposed between the first and second substrates.

[0014] The storage pattern includes a first storage electrode and a second storage electrode formed at positions corresponding to the first and second electrode connection portions, respectively, and a storage line formed at a position corresponding to the central portion of the pixel electrode pattern and connected to the first storage electrode and the second storage electrode.

[0015] The storage pattern includes a first storage electrode and a second storage electrode formed at positions corresponding to the first and second electrode connection portions, respectively, and a central storage electrode formed at an intersection between the first storage electrode and the storage line, wherein the central storage electrode is formed in a linear shape.

[0016] The central storage electrode is formed in a substantially quadrangular shape.

[0017] The central storage electrode is formed in a substantially rectangular shape.

[0018] The central storage electrode is formed about 4 μm apart from the central electrode.

[0019] The central storage electrode is formed in a substantially triangular shape.

[0020] The first and second storage electrodes are formed to have substantially the same or wider widths as or than the first and second electrode connection portions, respectively.

[0021] The first and second linear pixel electrodes are formed obliquely with respect to the central portion of the pixel electrode pattern.

[0022] The pixel electrode pattern is formed to overlap the TFT and includes a texture prevention portion connected to the first and second electrode connection portions.

[0023] The texture prevention portion is formed in a substantially triangular shape, wherein one side of the texture prevention portion is formed parallel to the second linear pixel electrode and another side of the texture prevention portion is formed parallel to the gate line.

[0024] The texture prevention portion is connected to the TFT.

[0025] The storage line is formed of the same material as the gate line.

[0026] The storage line is formed on the same plane as the gate line.

[0027] The pixel electrode pattern is formed of a transparent conductive material.

[0028] The second substrate includes a transmissive region and a blocking region, a black matrix provided in the blocking region, and a color filter provided in the transmissive region.

[0029] The first linear pixel electrode is provided in plurality and the plurality of first linear pixel electrodes are spaced at regular intervals, and the second linear pixel electrode is provided in plurality and the plurality of second linear pixel electrodes are spaced at regular intervals.

[0030] In an exemplary embodiment of the present invention, a method of manufacturing a thin film transistor (TFT) substrate in a liquid crystal display (LCD) panel, includes: forming a gate metal pattern including a gate line, a gate electrode and a storage pattern on a substrate; forming a gate insulating layer on the gate metal pattern and a semiconductor pattern including an activation layer and an ohmic contact layer on the gate insulating layer; forming a data metal pattern including a data line, a source electrode and a drain electrode on the semiconductor pattern and the gate insulating layer, and removing the ohmic contact layer between the source electrode and drain electrode to expose the activation layer; forming a passivation layer on the data metal pattern and the gate insulating layer, and forming a contact hole in the passivation layer to expose the drain electrode; and forming a pixel electrode pattern on the passivation layer, the pixel electrode pattern including a texture prevention portion connected to the drain electrode via the contact hole.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] The above and other features of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

[0032] FIG. **1** is a plan view showing a liquid crystal display (LCD) panel in accordance with an exemplary embodiment of the present invention;

[0033] FIG. **2**A is a cross-sectional view of the LCD panel shown in FIG. **1** taken along line I-I';

[0034] FIG. **2**B is a cross-sectional view of the LCD panel shown in FIG. **1** taken along line II-II';

[0035] FIG. **3** is a plan view showing a pixel electrode pattern of the LCD panel shown in FIG. **1** in accordance with an exemplary embodiment of the present invention;

[0036] FIG. **4**A is a plan view showing a storage pattern of the LCD panel shown in FIG. **1** in accordance with an exemplary embodiment of the present invention;

[0037] FIG. **4**B is a plan view of the pixel electrode pattern shown in FIG. **3** and the storage pattern shown in FIG. **4**A;

[0038] FIG. **5**A is a plan view showing a storage pattern and a pixel electrode pattern of an LCD panel in accordance with an exemplary embodiment of the present invention;

[0039] FIG. **5**B is a plan view showing a storage pattern and a pixel electrode pattern of an LCD panel in accordance with an exemplary embodiment of the present invention;

[0040] FIG. **6**A is a plan view showing a storage pattern of an LCD panel in accordance with an exemplary embodiment of the present invention;

[0041] FIG. **6**B is a plan view showing the pixel electrode pattern shown in FIG. **3** and the storage pattern shown in FIG. **6**A;

[0042] FIG. **7**A is a plan view showing a storage pattern of an LCD panel in accordance with an exemplary embodiment of the present invention;

[0043] FIG. **7**B is a plan view showing the pixel electrode pattern shown in FIG. **3** and the storage pattern shown in FIG. **7**A;

[0044] FIG. **8** is a plan view illustrating an orientation of a liquid crystal when a voltage is not applied to the LCD panel shown in FIG. **1** in accordance with an exemplary embodiment of the present invention;

[0045] FIG. **9** is a plan view illustrating an orientation of a liquid crystal when a voltage is applied to the LCD panel shown in FIG. **1** in accordance with an exemplary embodiment of the present invention;

[0046] FIG. **10** is a plan view and FIGS. **11**A, and **11**B are cross-sectional views taken along lines I-I' and II-II' of FIG. **10**, respectively, illustrating a first mask process of a method of manufacturing a thin film transistor (TFT) substrate in an LCD panel in accordance with an exemplary embodiment of the present invention;

[0047] FIG. **12** is a plan view and FIGS. **13**A, and **13**B are cross-sectional views taken along lines I-I' and II-II' of FIG. **12**, respectively, illustrating a second mask process of the method of manufacturing the TFT substrate in the LCD panel in accordance with an exemplary embodiment of the present invention;

[0048] FIG. **14** is a plan view and FIG. **15** is a cross-sectional view taken along line II-II' of FIG. **14** illustrating a third mask process of the method of manufacturing the TFT substrate in the LCD panel in accordance with an exemplary embodiment of the present invention;

[0049] FIG. **16** is a plan view and FIGS. **17**A, and **17**B are cross-sectional views taken along lines I-I' and II-II' of FIG. **16**, respectively, illustrating a fourth mask process of the method of manufacturing the TFT substrate in the LCD panel in accordance with an exemplary embodiment of the present invention; and

[0050] FIG. **18** is a plan view and FIGS. **19**A, and **19**B are cross-sectional views taken along lines I-I' and II-II' of FIG. **18**, respectively, illustrating a fifth mask process of the method of manufacturing the TFT substrate in the LCD panel in accordance with an exemplary embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0051] The present invention is described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

[0052] FIG. **1** is a plan view showing a liquid crystal display (LCD) panel in accordance with an exemplary embodiment of the present invention, FIG. **2**A is a cross-sectional view of the LCD panel shown in FIG. **1** taken along line I-I', and FIG. **2**B is a cross-sectional view of the LCD panel shown in FIG. **1** taken along line II-II'.

[0053] Referring to FIGS. **1**, **2**A, and **2**B, an LCD panel includes a thin film transistor (TFT) substrate, an opposing substrate, and a liquid crystal **200** disposed between the TFT substrate and the opposing substrate.

[0054] The TFT substrate includes a first substrate **10**, a gate line **20**, a data line **40**, a gate insulating layer **30**, a TFT **50**, a passivation layer **70**, a pixel electrode pattern, and a storage pattern.

[0055] The first substrate **10** includes a plurality of pixels arranged in a matrix form and has a transmissive region for transmitting light emitted from a backlight assembly (not shown), and a blocking region for blocking the light. It is desirable that the first substrate **10** be formed of an insulating material such as glass or plastic.

[0056] The gate line **20** is formed on the blocking region of the first substrate **10**. The gate line **20** is connected to a gate electrode **51** of the TFT **50** and thereby supplies a gate signal to the gate electrode **51** of the TFT **50**. The gate line **20** may be formed of a metal material in a single layer or in a multilayer thereof. The metal material used in the formation of the gate line **20** may include molybdenum (Mo), niobium (Nb), copper (Cu), aluminum (Al), chromium (Cr), silver (Ag), tungsten (W), or an alloy thereof.

[0057] The gate insulating layer **30** is formed on the gate line **20**. The gate insulating layer **30** insulates a gate metal pattern including the gate line **20**, the gate electrode **51** and the storage pattern from a data metal pattern including the data line **40**, a source electrode **53** and a drain electrode **55**.

[0058] The data line **40** supplies a pixel voltage signal to the source electrode **53** of the TFT **50**. The data line **40** is formed to cross the gate line **20** with the gate insulating layer **30** interposed therebetween.

[0059] The TFT **50** allows the pixel voltage signal of the data line **40** to be charged to the pixel electrode pattern and maintained in response to a gate signal of the gate line **20**. The TFT **50** includes the gate electrode **51** connected to the gate line **20**, the source electrode **53** connected to the data line **40** and overlapping a portion of the drain electrode **55**, and the drain electrode **55** facing the source electrode **53** and connected to the pixel electrode pattern.

[0060] Moreover, the TFT **50** includes a semiconductor pattern **60** overlapping the gate electrode **51** with the gate insulating layer **30** interposed therebetween and forming a channel between the source electrode **53** and drain electrode **55**.

[0061] The semiconductor pattern **60** includes an activation layer **61** formed to overlap the gate electrode **51** with the gate insulating layer **30** interposed therebetween. The semiconductor pattern **60** further includes an ohmic contact layer **63** formed on the activation layer **61** and providing ohmic contact between the data line **40** and the source and drain electrodes **53** and **55**.

[0062] The passivation layer **70** is formed on the data line **40** and the TFT **50** to protect the same. The passivation layer **70** may be formed of an inorganic material.

[0063] FIG. **3** is a plan view showing the pixel electrode pattern of the LCD panel shown in FIG. **1** in accordance with an exemplary embodiment of the present invention.

[0064] As shown in FIG. **3**, the pixel electrode pattern includes a central portion **109**, linear pixel electrodes **95** and **97**, first and second electrode connection portions **91** and **93**, a central electrode **101**, and a texture prevention portion **107**. The pixel electrode pattern is formed on the passivation layer **70**. Moreover, the pixel electrode pattern is formed of a transparent conductive material such as indium tin oxide (ITO), tin oxide (TO), indium zinc oxide (IZO), and indium tin zinc oxide (ITZO).

[0065] The central portion **109** is formed in the center of the transmissive region parallel to the gate line **20**.

[0066] The linear pixel electrodes **95** and **97** include a plurality of first and second linear pixel electrodes **95** and **97** formed obliquely and symmetrically with respect to the central portion **109**.

[0067] The first and second electrode connection portions **91** and **93** are formed in the blocking region parallel to the data line **40**. The first and second electrode connection portions **91** and **93** are connected to the plurality of first and second linear pixel electrodes **95** and **97**. The first and second electrode connection portions **91** and **93** are connected to the central portion **109**. In other words, the first electrode connection portion **91** is connected to the left side of the central portion **109** and the second electrode connection portion **93** is connected to the right side of the central portion **109**. Upper and lower ends of the second electrode connection portion **93** are connected to upper and lower ends of the first electrode connection portion **91**. Moreover, the lower ends of the first and second electrode connection portions **91** and **93** are connected by the texture prevention portion **107**.

[0068] The central electrode **101** is formed at an intersection between the first electrode connection portion **91** and the central portion **109**. The central electrode **101** is formed in the shape of a triangle.

[0069] The texture prevention portion **107** is connected to the lower ends of the first and second electrode connection portions **91** and **93**. The texture prevention portion **107** is generally formed in the shape of a triangle. In particular, one side **103** of the texture prevention portion **107** is formed parallel to the second linear pixel electrode **97** and the other side **105** of the texture prevention portion **107** is formed parallel to the gate line **20**. With such a structure in that the one side **103** of the texture prevention portion **107** is formed parallel to the second linear pixel electrode **97**, a fringe electric field is generated constantly, thus enabling control of the liquid crystal **200**. Accordingly, the generation of texture on the LCD panel can be prevented. The texture prevention portion **107** is connected to the drain electrode **55** exposed by a contact hole **75** penetrating the passivation layer **70**.

[0070] FIG. **4**A is a plan view showing the storage pattern of the LCD panel shown in FIG. **1** in accordance with an exemplary embodiment of the present invention, and FIG. **4**B is a plan view of the pixel electrode pattern shown in FIG. **3** and the storage pattern shown in FIG. **4**A.

[0071] As shown in FIGS. **4**A and **4**B, the storage pattern includes first and second storage electrodes **81** and **83**, and a storage line **85**. The storage pattern is formed on the same plane as the gate line **20** and the gate electrode **51** with the same material. In particular, the storage pattern is formed of a metal material in a single layer or in a multi-layer thereof on the first substrate **10**. The metal material may include Mo, Nb, Cu, Al, Cr, Ag, W, or an alloy thereof.

[0072] The first and second storage electrodes **81** and **83** are formed parallel to the data line **40** in the blocking region. Moreover, the first and second storage electrodes **81** and **83** are formed in parallel with each other, with the storage line **85** interposed therebetween. In particular, the first storage electrode **81** is formed to extend from the storage line **85**. The second storage electrode **83** extending from the storage line **85** is formed from the drain electrode **55** to the upper end of the second electrode connection portion **93** and an end of the second storage electrode **83** protrudes therefrom. For example, the second storage electrode **83** may be generally formed in the shape of a reverse 'L'. The lower end of the first storage electrode **81** extends from the storage line **85** to the gate line **20** further than the lower end of the second storage electrode **83** extending to the gate line **20**. The first storage electrode **81** is formed parallel to the second storage electrode **83**. Meanwhile, as shown in FIG. **5**A, the first and second storage electrodes **81** and **83** are formed to have the same widths as the first and second electrode connection portions **91** and **93** of the pixel electrode pattern, respectively. Moreover, as shown in FIG. **5**B, the first and second storage electrodes **81** and **83** are formed to have widths larger than those of the first and second electrode connection portions **91** and **93**, respectively. The storage pattern and the pixel electrode pattern overlap each other to form a storage capacitor. In more detail, the storage pattern and the pixel electrode pattern overlap each other with the gate insulating layer **30** and the passivation layer **70** interposed therebetween, thus forming the storage capacitor. Accordingly, the capacity of the storage capacitor is increased as the storage pattern and the pixel electrode pattern overlap each other.

[0073] The storage line **85** is formed parallel to the gate line **20** in the center of the transmissive region. The storage line **85** is overlapped by the central portion **109** of the pixel electrode pattern. In particular, the storage line **85** is formed to be narrower than the central portion **109**. Accordingly, since the widths of the central portion **109** and the storage line **85** are not the same, a step height is not formed and therefore light leakage can be prevented. The storage line **85** is connected to the first storage electrode **81** and the second storage electrode **83**. In more detail, the left side of the storage line **85** is connected to the first storage electrode **81** and the right side of the storage line **85** is connected to the second storage electrode **83**. For example, the storage line **85** and the first and second storage electrodes **81** and **83** may be generally formed in the shape of an 'H'.

[0074] FIG. **6**A is a plan view showing a storage pattern of an LCD panel in accordance with an exemplary embodiment of the present invention, and FIG. **6**B is a plan view showing the pixel electrode pattern shown in FIG. **3** and the storage pattern shown in FIG. **6**A. Moreover, FIG. **7**A is a plan view showing a storage pattern of an LCD panel in accordance with an exemplary embodiment of the present invention, and FIG. **7**B is a plan view showing the pixel electrode pattern shown in FIG. **3** and the storage pattern shown in FIG. **7**A.

[0075] Referring the FIG. **6**A, the storage pattern includes a central storage electrode **89** formed at an intersection between the storage line **85** and the first storage electrode **81**. As shown in FIG. **6**B, the central storage electrode **89** is overlapped by the central electrode **101** of the pixel electrode pattern. The central storage electrode **89** may be formed about 4 μm apart from the central electrode **101**. If the interval 'a' between the central storage electrode **89** and the central electrode **101** is less than about 4 μm, a step height is formed, which results in light leakage. Accordingly, it is preferable that the interval 'a' between the central storage electrode **89** and the central electrode **101** be larger than about 4 μm. The central storage electrode **89** may be formed in the shape of a triangle. Moreover, as shown in FIGS. **7**A and **7**B, the central storage electrode **89** may be formed in the shape of a quadrangle. Accordingly, since a step height is not formed by the central storage electrode **89** and the central electrode **101**, light leakage can be prevented. Although the above description has been made for the case where the central storage electrode **89** has a triangular or quadrangular shape, the description is not limited thereto. For example, the central storage electrode **89** may be formed in any shape as long as the interval 'a' between the central storage electrode **89** and the central electrode **101** is larger than about 4 μm.

[0076] Referring back to FIGS. **1**, **2**A, and **2**B, the opposing substrate includes a second substrate **150**, a black matrix **160**, a color filter **170**, a planarization layer **180**, and a common electrode pattern **190**.

[0077] The second substrate **150** includes a transmissive region for transmitting light and a blocking region for blocking light. It is desirable that the second substrate **150** be formed of an insulating material such as glass or plastic.

[0078] The black matrix **160** is formed in a matrix shape in the blocking region of the second substrate **150** to define a plurality of pixels in which the color filter **170** is formed. Moreover, the black matrix **160** is formed to overlap the gate line **20**, the data line **40** and the TFT **50** on the TFT substrate. The black matrix **160** shields light generated by an undesirable orientation of the liquid crystal **200** to improve the contrast of the LCD panel. Moreover, the black matrix **160** intercepts direct light irradiation to the TFT **50** to prevent the generation of light leakage by the TFT **50**. For this, the black matrix **160** is formed of an opaque metal or opaque polymer resin.

[0079] The color filter **170** includes red (R), green (G) and blue (B) color filters **170** to reproduce colors. The respective R, G and B color filters **170** absorb or transmit light of a specific wavelength through R, G and B pigments included therein, thus displaying R, G and B colors. In this case, the R, G and B color filters **170** display various colors by an additive mixture of R, G and B lights passed through the R, G and B color filters **170**. The color filters **170** are arranged in a stripe shape where the R, G and B color filters **170** are arranged in a row.

[0080] The planarization layer **180** is formed on the color filters **170** and the black matrix **160** to planarize the surface of the color filters **170**.

[0081] The common electrode pattern **190** is formed on the planarization layer **180**. The common electrode pattern **190** is formed between the plurality of linear pixel electrodes **95** and **97** formed on the TFT substrate and thereby fringe electric fields are generated. The liquid crystal molecules **200** are driven symmetrically with respect to the linear pixel electrodes **95** and **97** using the fringe electric fields to form a multi-domain structure. The common electrode pattern **190** is formed of a transparent conductive material such as ITO, TO, IZO, and ITZO.

[0082] The liquid crystal molecules **200** are rotated by a difference between a pixel voltage from the pixel electrode pattern and a common voltage from the common electrode pattern **190** of the opposing substrate to control the transmittance of light emitted from the backlight assembly. To this end, the liquid crystal **200** is made of a material having dielectric anisotropy and refractive anisotropy.

[0083] In a dual field switching (DFS) mode, a liquid crystal **200** having a positive or negative dielectric anisotropy is aligned horizontally and driven horizontally or vertically to the electric field direction, thus controlling light transmittance. Moreover, a horizontal alignment layer is formed on the upper portion of the first and second substrates **10** and **150**. In the following, a description will be given with respect to the liquid crystal **200** having a positive dielectric anisotropy. As shown in FIG. **8**, when a voltage is not applied to the LCD panel, the liquid crystal molecules **200** are oriented at an angle of about 10° to about 30° with respect to the linear pixel electrodes **95** and **97** and the common electrode pattern **190**. As shown in FIG. **9**, when a voltage is applied to the LCD panel, the liquid crystal molecules **200** are aligned perpendicularly to the linear pixel electrodes **95** and **97** and the common electrode pattern **190**. In this case, only typical liquid crystal molecules **200** are depicted in FIG. **9** to illustrate that the state of the liquid crystal molecules **200** is varied when the voltage is applied to the LCD panel.

[0084] Next, a method of manufacturing a TFT substrate in an LCD panel in accordance with an exemplary embodiment of the present invention will be described in detail with reference to FIGS. **10** to **19**B.

[0085] FIG. **10** is a plan view and FIGS. **11**A and **11**B are cross-sectional views taken along lines I-I' and II-II' of FIG. **10**, respectively, illustrating a first mask process of a method of manufacturing a TFT substrate in an LCD panel in accordance with an exemplary embodiment of the present invention.

[0086] Referring to FIGS. **10**, **11**A, and **11**B, a gate metal pattern including a gate line **20**, a gate electrode **51** and a storage pattern is formed on an insulated first substrate **10** by a first mask process. In other words, a gate metal layer is formed on the insulated first substrate **10** by a deposition method such as sputtering. The gate metal layer is formed of a metal material in a single layer or in a multi-layer thereof. The metal material may include Mo, Nb, Cu, Al, Cr, Ag, W, or an alloy thereof. Subsequently, the gate metal layer is patterned by photolithography and etching processes using a first mask, thus forming the gate metal pattern including the gate line **20**, the gate electrode **51** and the storage pattern.

[0087] FIG. **12** is a plan view and FIGS. **13**A, and **13**B are cross-sectional views taken along lines I-I' and II-II' of FIG. **12**, respectively, illustrating a second mask process of the method of manufacturing the TFT substrate in the LCD panel in accordance with an exemplary embodiment of the present invention.

[0088] Referring to FIGS. **12**, **13**A, and **13**B, a gate insulating layer **30** is formed on the gate metal pattern including the gate line **20**, the gate electrode **51** and the storage pattern, and a semiconductor pattern **60** including an activation layer **61** and an ohmic contact layer **63** is formed on the gate insulating layer **30**.

[0089] The gate insulating layer **30**, an amorphous silicon layer, and an impurity-doped amorphous silicon layer are formed in sequence on the gate metal pattern by a deposition method such as plasma-enhanced chemical vapor deposition (PECVD). The gate insulating layer **30** is formed of an inorganic insulating material such as silicon oxide (SiOx) or silicon nitride (SiNx). Subsequently, the amorphous silicon layer and the impurity-doped amorphous silicon layer are patterned by photolithography and etching processes using a second mask, thus forming the semiconductor pattern **60** including the activation layer **61** and the ohmic contact layer **63**.

[0090] FIG. **14** is a plan view and FIG. **15** is a cross-sectional view taken along line II-II' of FIG. **14** illustrating a third mask process of the method of manufacturing the TFT substrate in the LCD panel in accordance with an exemplary embodiment of the present invention.

[0091] Referring to FIGS. **14** and **15**, a data metal pattern including a data line **40**, a source electrode **53** and a drain electrode **55** is formed on the semiconductor pattern **60** and the gate insulating layer **30**.

[0092] More specifically, a data metal layer is formed on the semiconductor pattern **60** and the gate insulating layer **30** by a deposition method such as sputtering. The data metal layer is formed of a metal material in a single layer or in a multi-layer thereof. The metal material may include Mo, Nb, Cu, Al, Cr, Ag, W, or an alloy thereof. Subsequently, the data metal layer is patterned by photolithography and etching processes using a third mask, thus forming the data metal pattern including the data line **40**, the source electrode **53** and the drain electrode **55**. Then, the ohmic contact layer **63** exposed between the source electrode **53** and the drain electrode **55** is removed using a third mask to expose the activation layer **61**. The semiconductor pattern **60** and the data metal pattern including the data line **40**, the source electrode **53** and the drain electrode **55** may be formed by one mask process using a diffractive exposure mask or a half-tone mask.

[0093] FIG. **16** is a plan view and FIGS. **17**A, and **17**B are cross-sectional views taken along lines I-I' and II-II' of FIG. **16**, respectively, illustrating a fourth mask process of the method of manufacturing the TFT substrate in the LCD panel in accordance with an exemplary embodiment of the present invention.

[0094] Referring to FIGS. **16**, **17**A, and **17**B, a passivation layer **70** including a contact hole **75** is formed on the data metal pattern and the gate insulating layer **30** by a deposition process such as PECVD. The passivation layer **70** is formed of the same inorganic insulating material as the gate insulating layer **30**. Subsequently, the passivation layer **70** is patterned by photolithography and etching processes using a fourth mask, thus forming the contact hole **75** exposing the drain electrode **55**.

[0095] FIG. **18** is a plan view and FIGS. **19**A, and **19**B are cross-sectional views taken along lines I-I' and II-II' of FIG. **18**, respectively, illustrating a fifth mask process of the method of manufacturing the TFT substrate in the LCD panel in accordance with an exemplary embodiment of the present invention.

[0096] Referring to FIGS. **18**, **19**A, and **19**B, a pixel electrode pattern is formed on the passivation layer **70**. In other words, a transparent conductive layer is formed on the passivation layer **70** by a deposition method such as sputtering. The transparent conductive layer is formed of a transparent and conductive material such as ITO, TO, IZO, and ITZO. Subsequently, the transparent conductive layer is patterned by photolithography and etching processes using a fifth mask, thus forming the pixel electrode pattern. A texture prevention portion **107** of the pixel electrode pattern is connected to the drain electrode **55** exposed by the contact hole **75** penetrating the passivation layer **70**.

[0097] As described above, in the LCD panel according to an exemplary embodiment of the present invention, the storage pattern is overlapped by the pixel electrode pattern in the transmissive region. In detail, since the storage line of the storage pattern and the central storage electrode of the storage pattern are overlapped by the central portion of the pixel electrode pattern and the central electrode of the pixel electrode pattern, respectively, a step height is not formed and therefore light leakage can be prevented. Moreover, with the texture prevention portion formed to control the liquid crystal, the generation of texture on the LCD panel can be prevented.

[0098] While the present invention has been described in detail with reference to the exemplary embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

What is claimed is:

1. A liquid crystal display (LCD) panel, comprising:
a first base substrate;
a plurality of gate lines and a plurality of data lines disposed on the first base substrate and crossing each other;
a gate insulating layer on the first base substrate;
a passivation layer on the gate insulating layer;
a pixel electrode pattern disposed on the first base substrate, the pixel electrode pattern comprising a first electrode connection portion, a second electrode connection portion parallel to the first electrode connection portion, and a central portion parallel to the gate lines to connect the first connection portion with the second connection portion;
a storage pattern disposed on the first base substrate, the storage pattern comprising a storage line being parallel to the gate lines and corresponding to the central portion;
a second base substrate;
a common electrode pattern disposed on the second base substrate; and
a liquid crystal layer disposed between the first and second base substrates,
wherein the pixel electrode overlaps with the storage pattern while interposing the gate insulating layer and the passivation layer therebetween to form a storage capacitor and a width of the central portion is wider than a width of the storage line.

2. The LCD panel of claim **1**, wherein the storage pattern further comprises a first storage electrode, a second storage electrode parallel to the first storage electrode, and a central storage electrode formed at an intersection between the storage line and the first storage electrode.

3. The LCD panel of claim **1**, wherein the storage pattern further comprises a central storage electrode formed at an intersection between the storage line and the first storage electrode and the central storage electrode has a substantially triangle or quadrangle shape.

4. The LCD panel of claim **2**, wherein the first storage electrode and the second storage electrode correspond respectively to the first electrode connection portion and the second electrode connection portion, a width of the first storage electrode is wider than a width of the first electrode connection portion, and a width of the second storage electrode is wider than a width of the second electrode connection portion.

5. The LCD panel of claim **1**, wherein the pixel electrode further comprises a first linear pixel electrode and a second linear pixel electrode arranged between the first electrode connection portion and the second electrode connection portion and the first linear pixel electrode and the second linear pixel electrode are inclined in a different direction from each other with respect to the gate lines.

6. The LCD panel of claim **5**, wherein the pixel electrode further comprises a central electrode formed at an intersection between the central portion and the first electrode connection portion and the first and second linear pixel electrodes are connected with the central electrode.

7. The LCD panel of claim **1**, wherein the liquid crystal layer has negative or positive dielectric anisotropy.

8. The LCD panel of claim **7**, wherein the liquid crystal layer comprises liquid crystal molecules which are aligned horizontally and driven horizontally or vertically to an electric field direction formed between the pixel electrode and the common electrode.

9. The LCD panel of claim **1**, wherein the common electrode pattern and the pixel electrode are alternately positioned with each other.

* * * * *

专利名称(译)	液晶显示面板		
公开(公告)号	US20100220253A1	公开(公告)日	2010-09-02
申请号	US12/777659	申请日	2010-05-11
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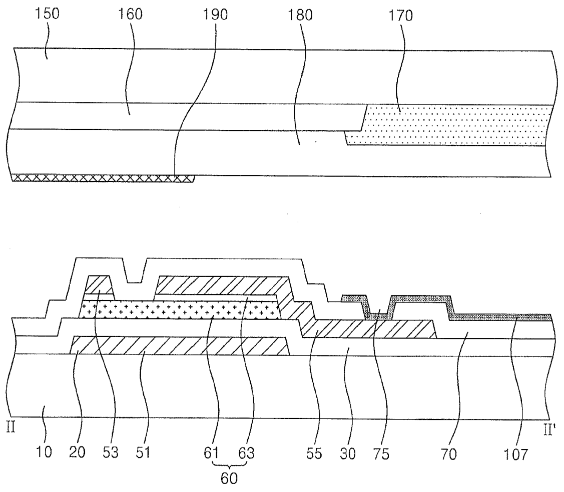
IPC分类号	G02F1/1343		
CPC分类号	G02F1/134336 G02F1/134363 G02F2001/134318 G02F1/136286 G02F1/136213		
优先权	1020070009021 2007-01-29 KR		
其他公开文献	US8077265		
外部链接	Espacenet USPTO		

摘要(译)

液晶显示（LCD）面板包括：第一基底基板;多条栅极线和多条数据线设置在第一基底基板上并相互交叉;像素电极图案设置在第一基底基板上;存储图案设置在第一基础基板上，存储图案位于连续的栅极线之间并且基本上与栅极线平行;第二基础基底;公共电极，设置在第二基板上并与像素电极交替定位;液晶层设置在第一和第二基底之间。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