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(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0279515 A1**
(43) **Pub. Date: Dec. 14, 2006**(54) **LIQUID CRYSTAL DISPLAY DEVICE,
DRIVING METHOD FOR LIQUID CRYSTAL
DISPLAY DEVICES, AND INSPECTION
METHOD FOR LIQUID CRYSTAL DISPLAY
DEVICES**(30) **Foreign Application Priority Data**

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G09G 3/36 (2006.01)(52) **U.S. Cl.** 345/100(57) **ABSTRACT**

Using technology which uses a single shift register and simultaneously generates multiple pulses, this invention is a liquid crystal display device which rapidly drives data lines. It is possible to increase the frequency of the shift register output signal without changing the frequency of the shift register operation clock. If the shift register output signals, by means of analog switches, are used to determine the video signal sampling timing, high speed data line driving can be realized. Additionally, if the output signals of the shift register mentioned above are used to determine the video signal latch timing in a digital driver, high speed latching of the video signal can be realized. Consequently, even if the driving circuits of the liquid crystal display matrix are composed of TFTs, high speed operation of the driving circuits is possible without increasing power consumption. The shift register can also be used to inspect the electrical characteristics of the data lines and analog switches.

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(60) Division of application No. 10/026,905, filed on Dec. 27, 2001, which is a division of application No. 09/218,497, filed on Dec. 22, 1998, now Pat. No. 6,337,677, which is a continuation of application No. 08/714,170, filed on Sep. 27, 1996, now Pat. No. 6,023,260, filed as 371 of international application No. PCT/JP96/00202, filed on Feb. 1, 1996.

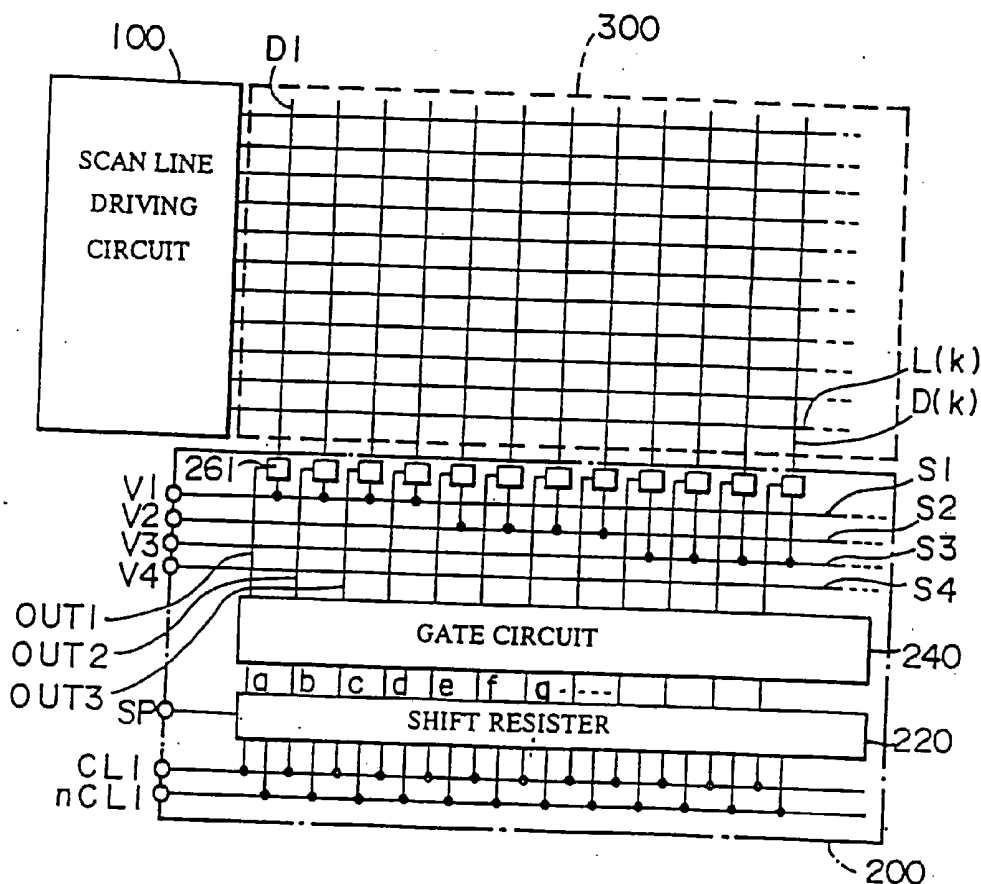


FIG. 1A

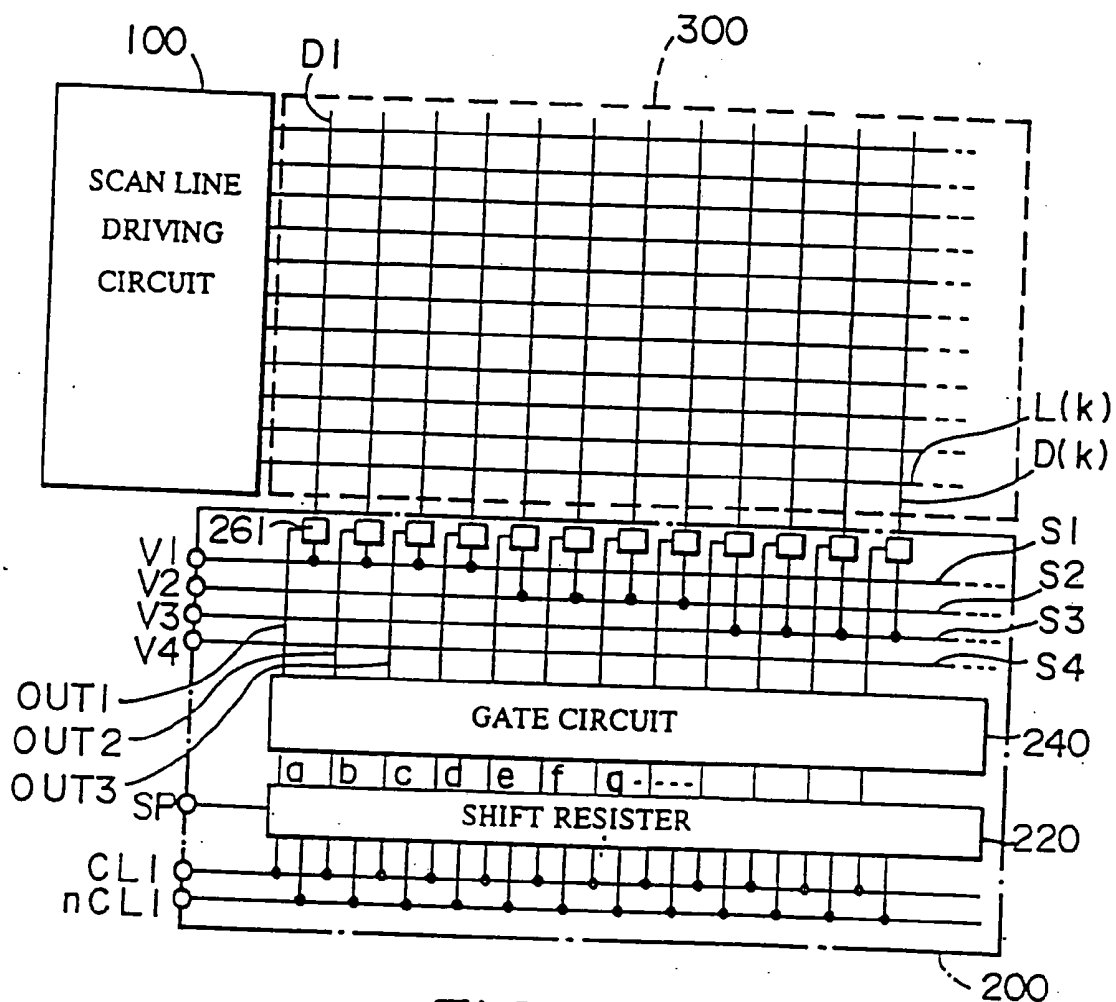


FIG. 1B

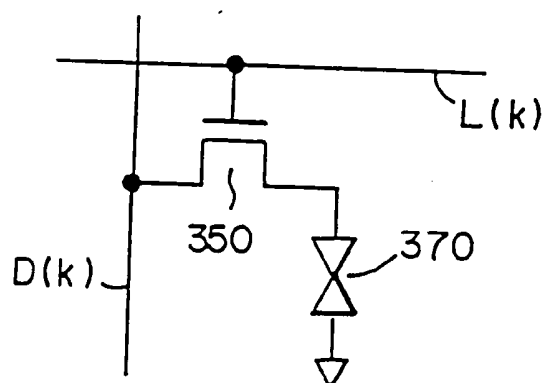


FIG. 2

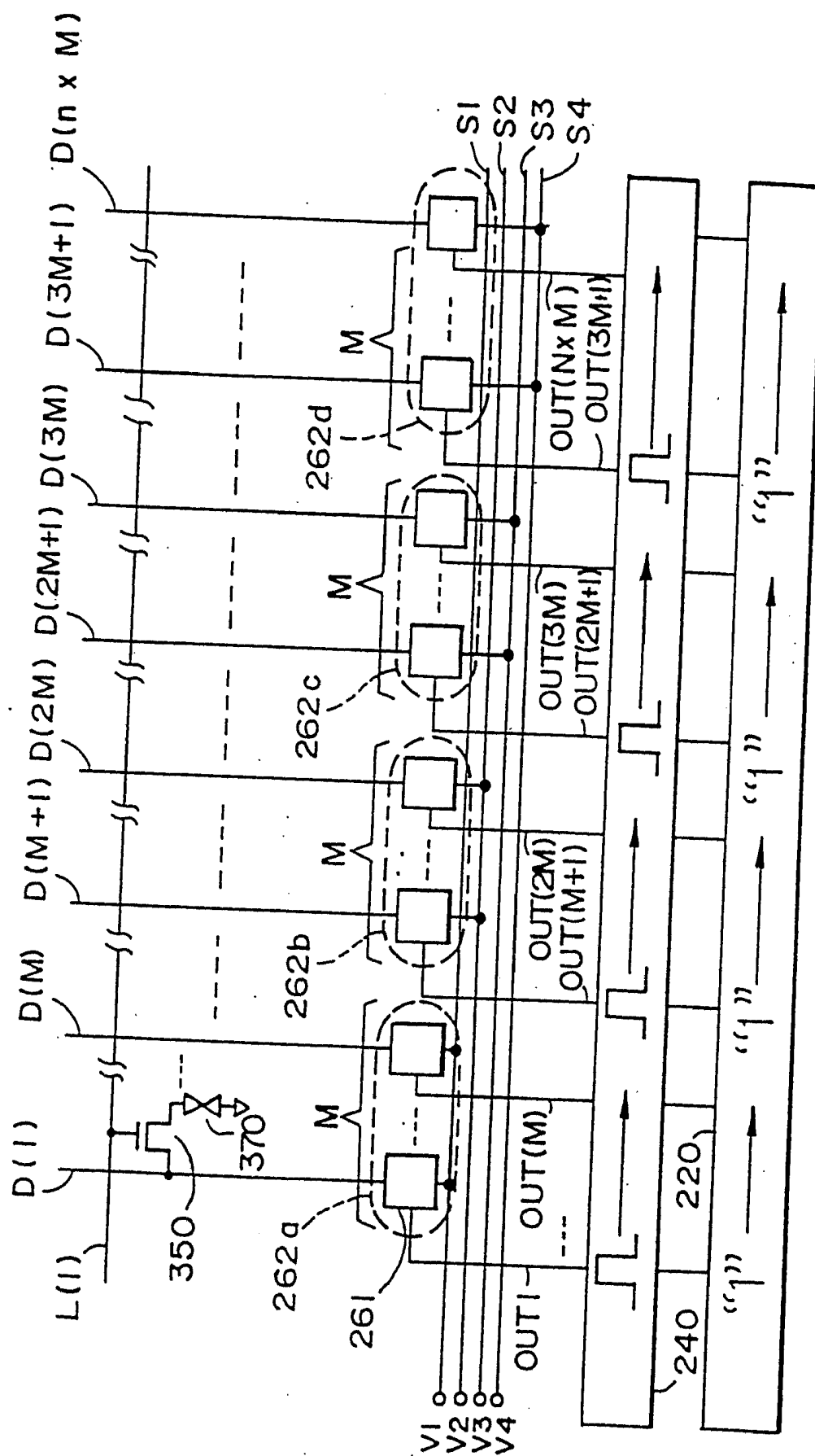


FIG. 3

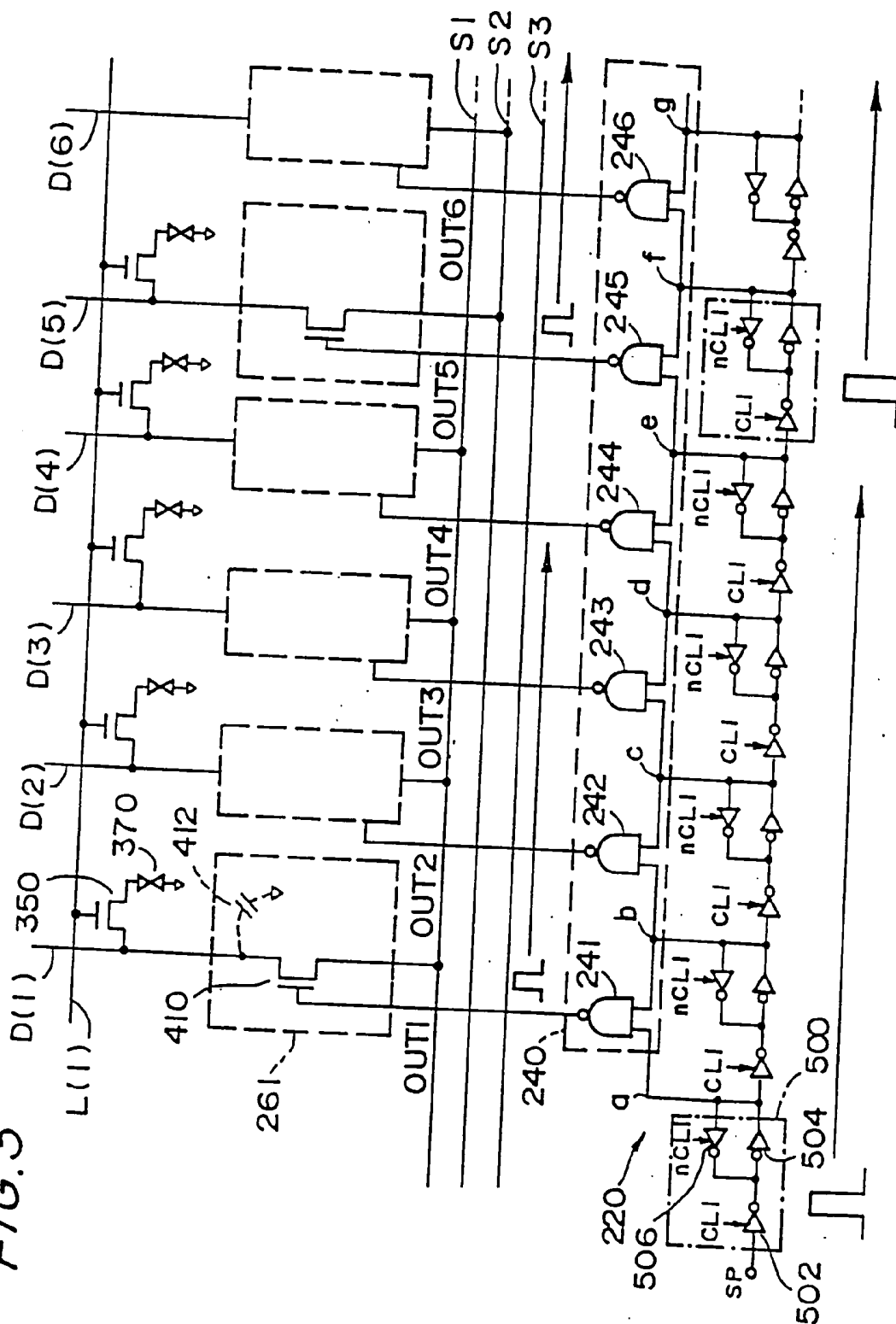


FIG. 4A

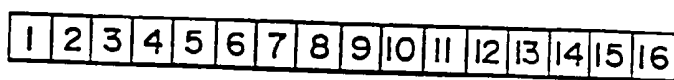


FIG. 4B

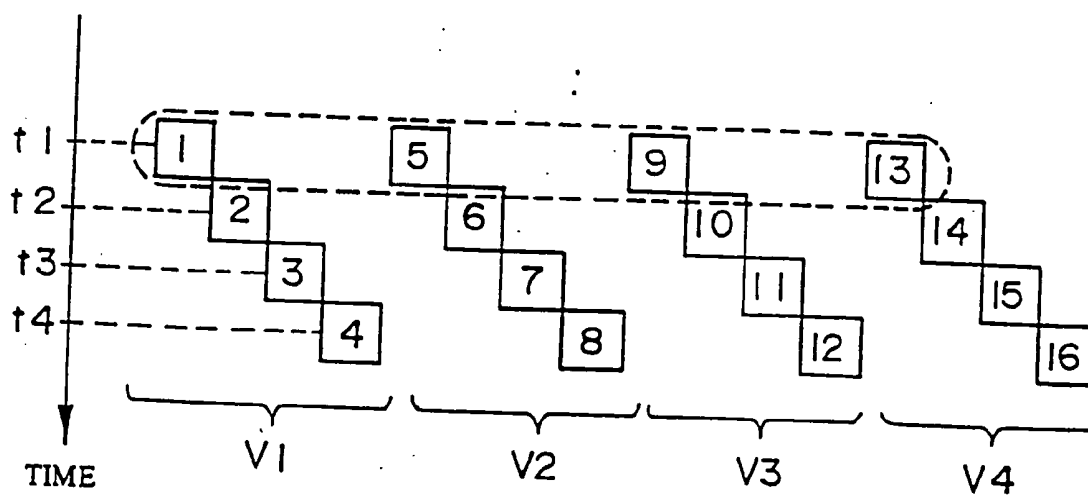


FIG. 5

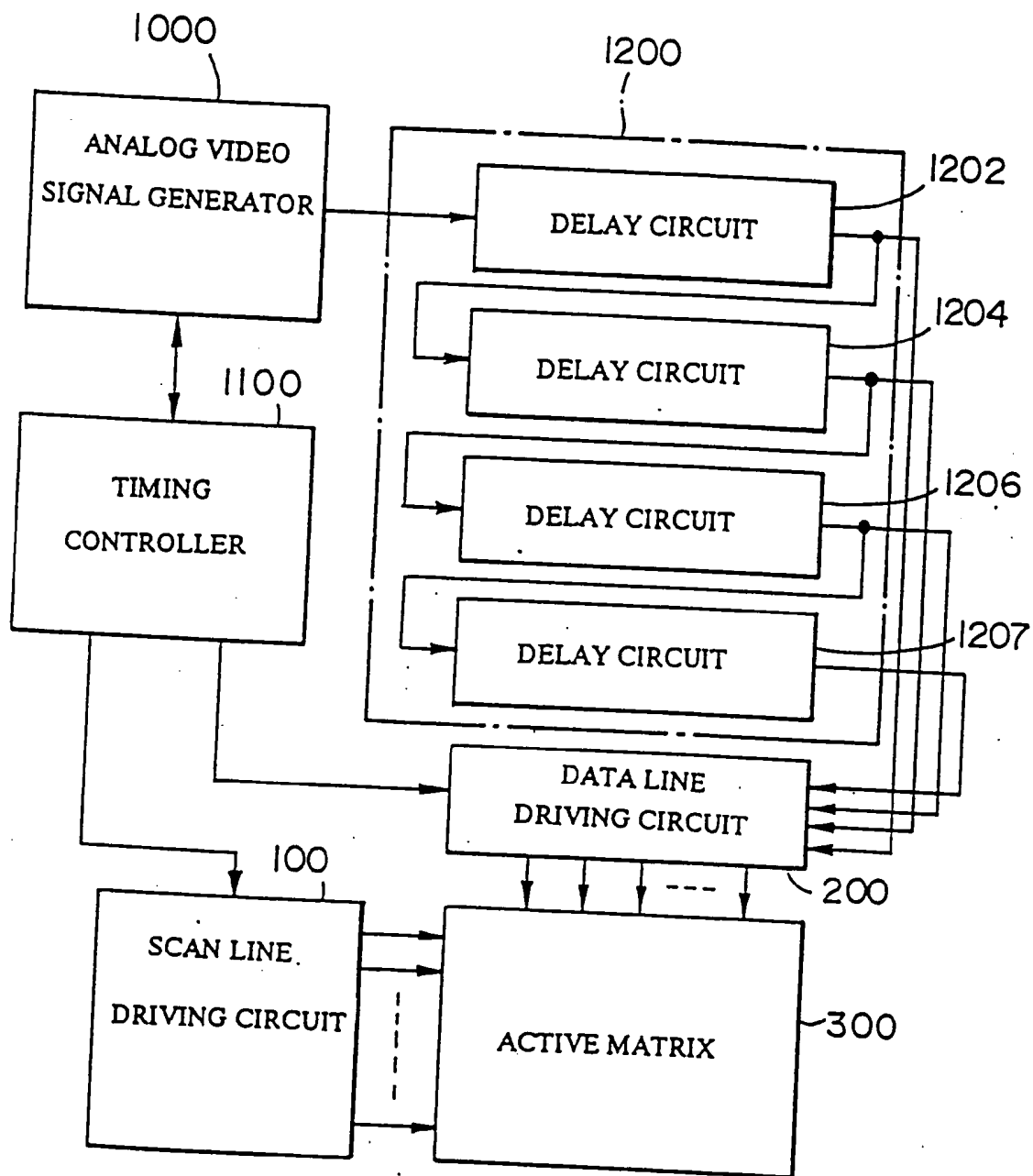


FIG. 6

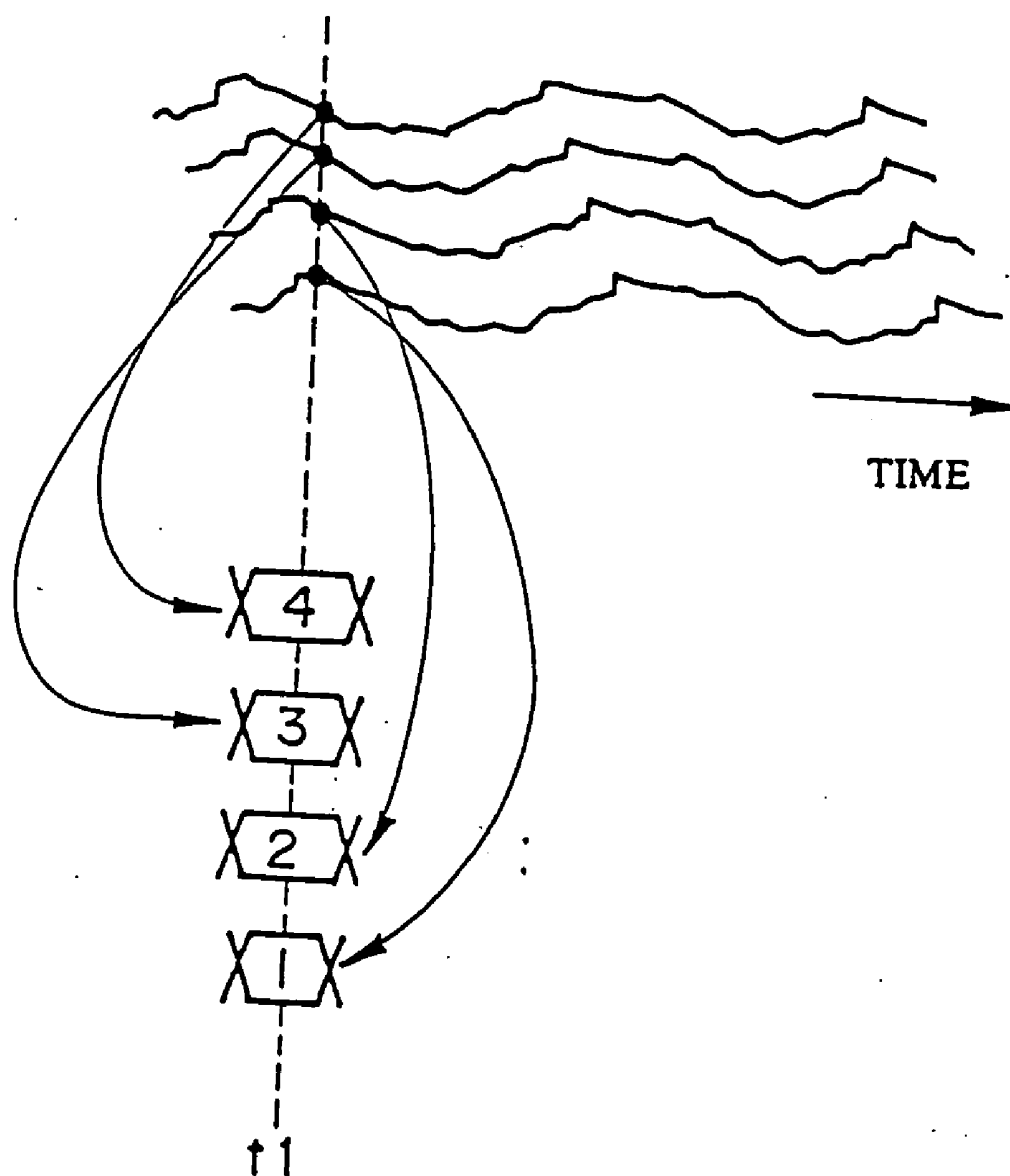


FIG. 7

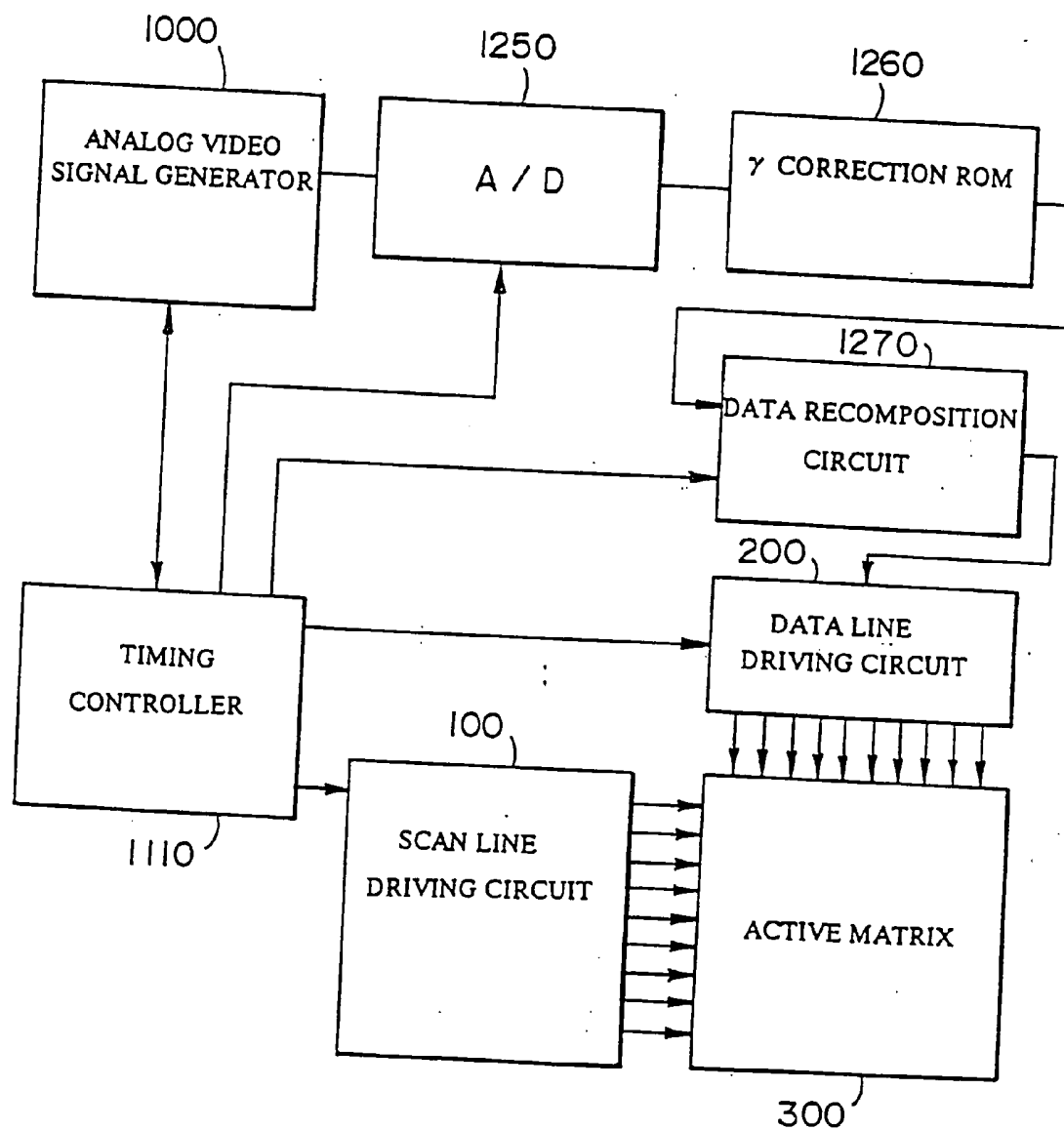


FIG. 8

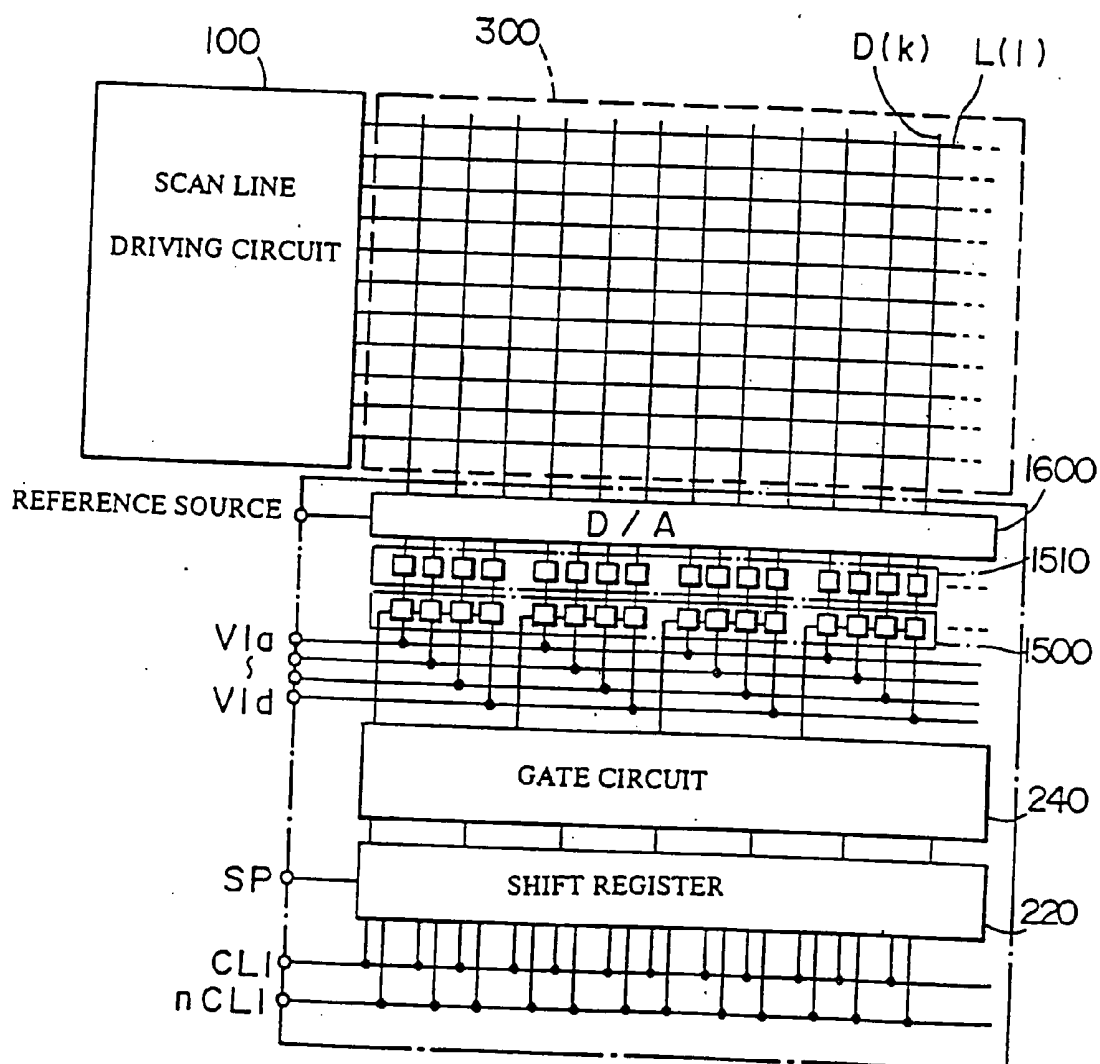


FIG. 9

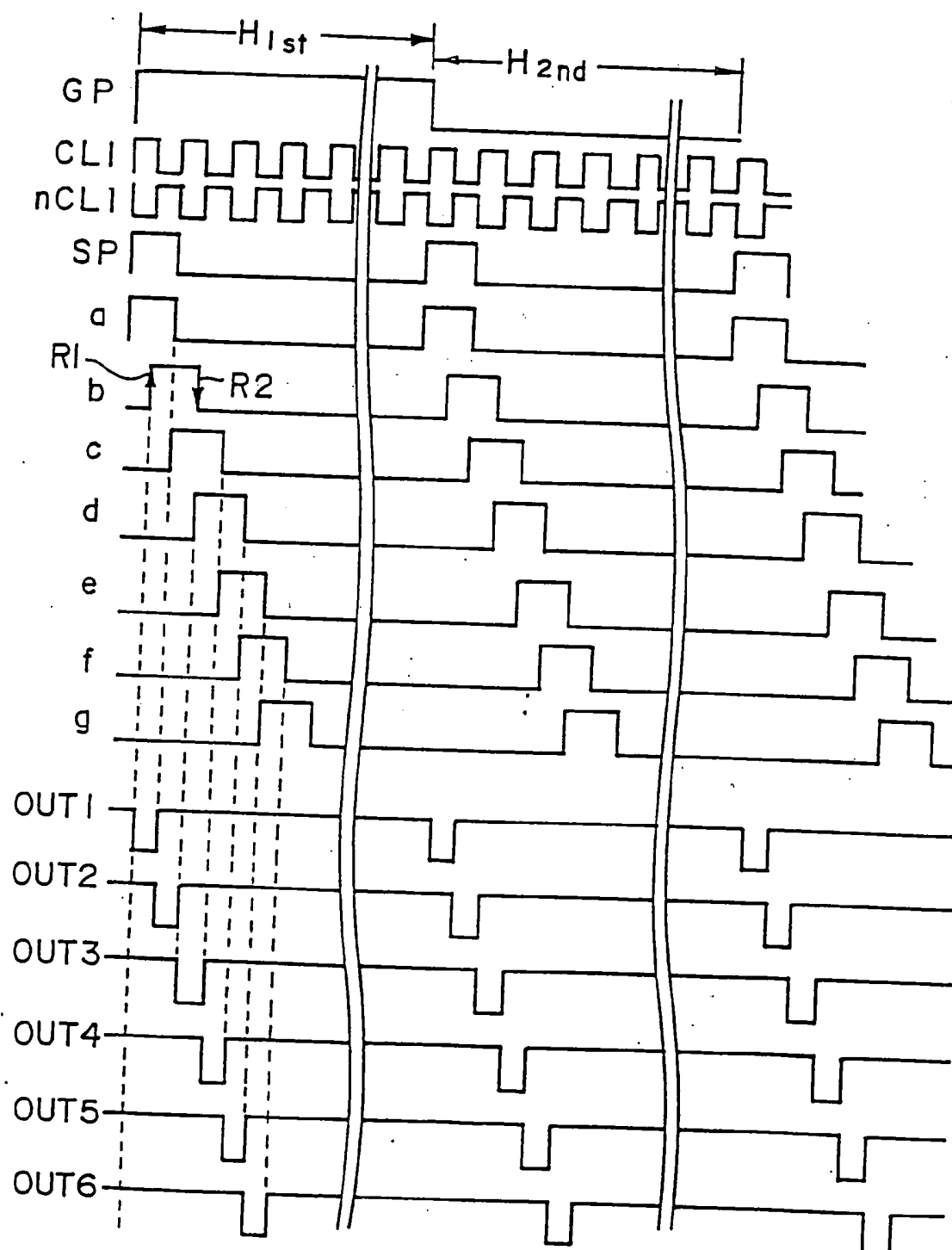


FIG. 10

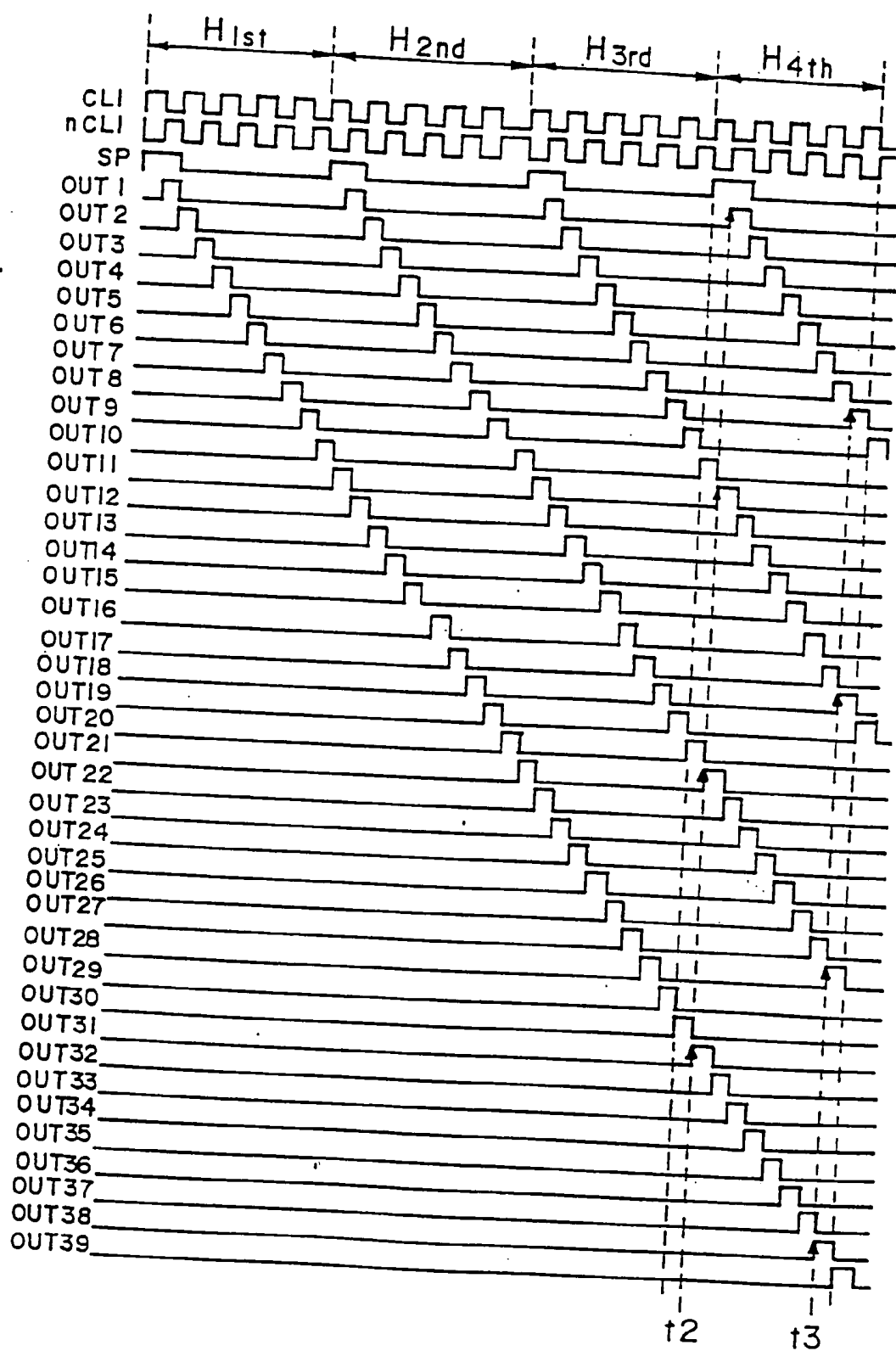


FIG. 11A

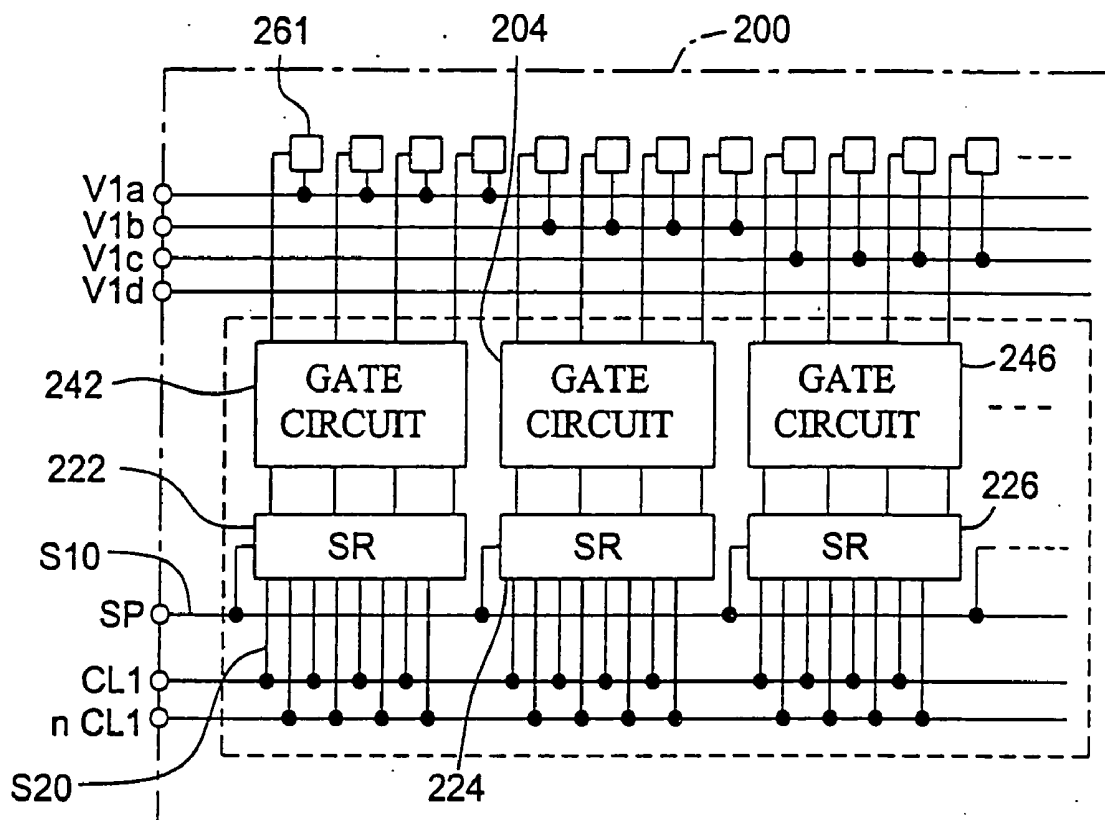


FIG. 11B

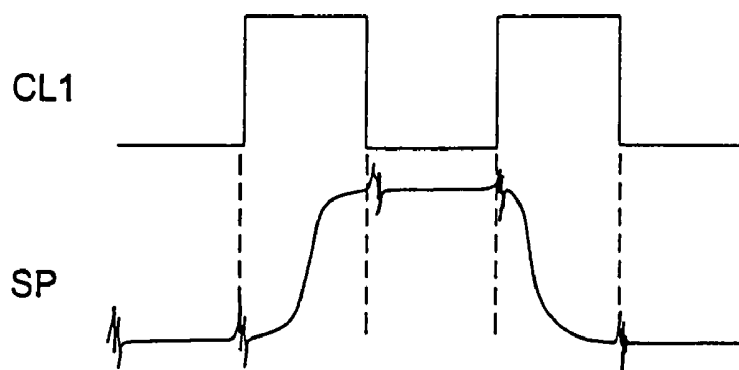


FIG. 12A

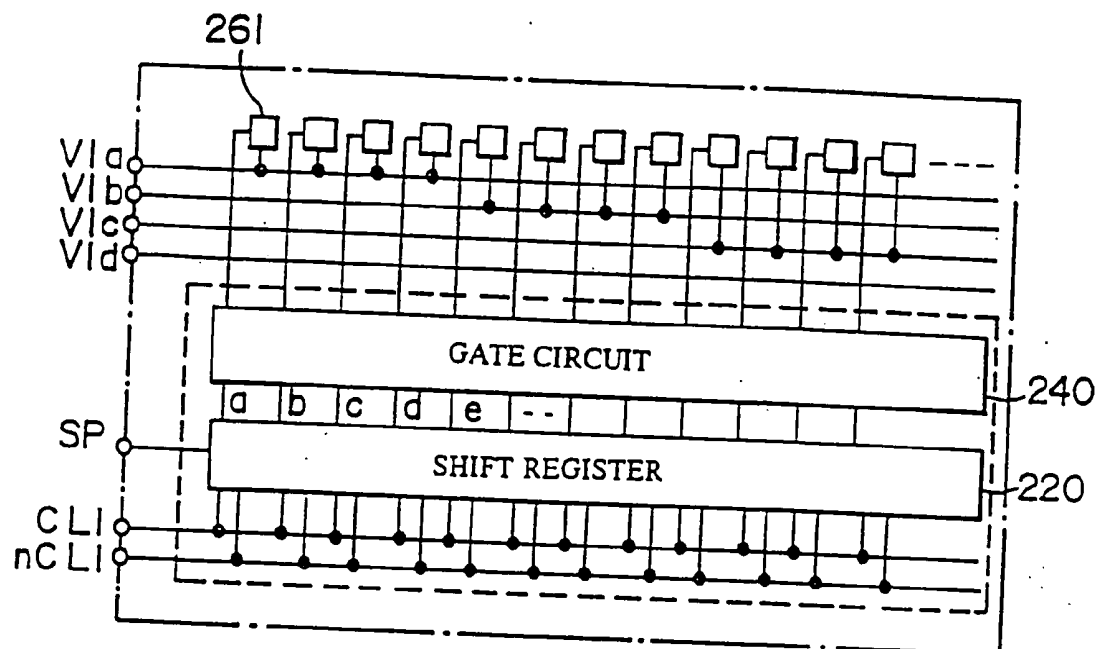


FIG. 12B

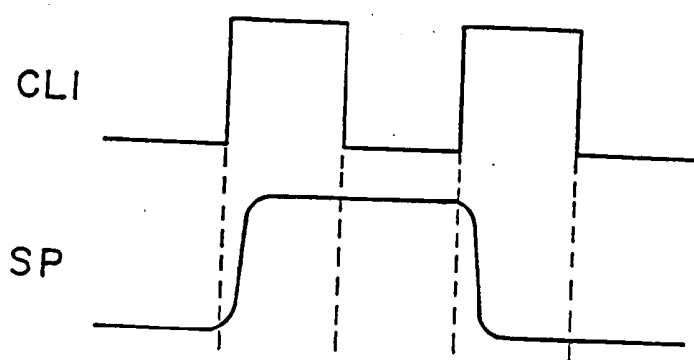


FIG. 13A

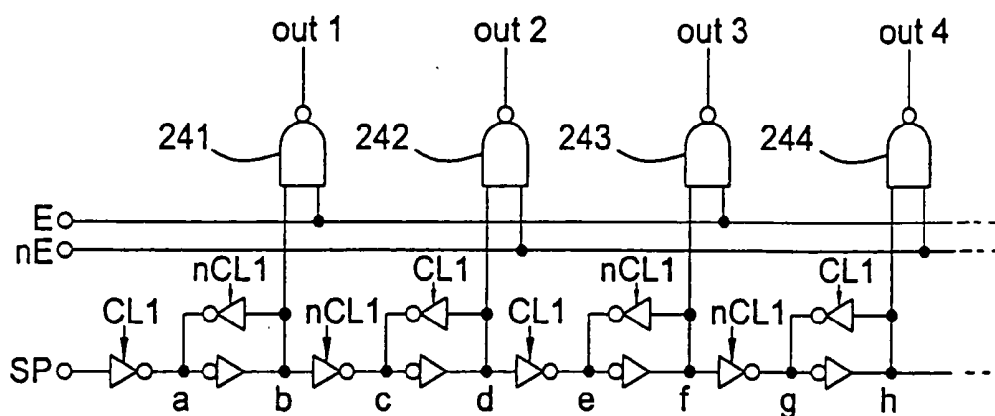


FIG. 13B

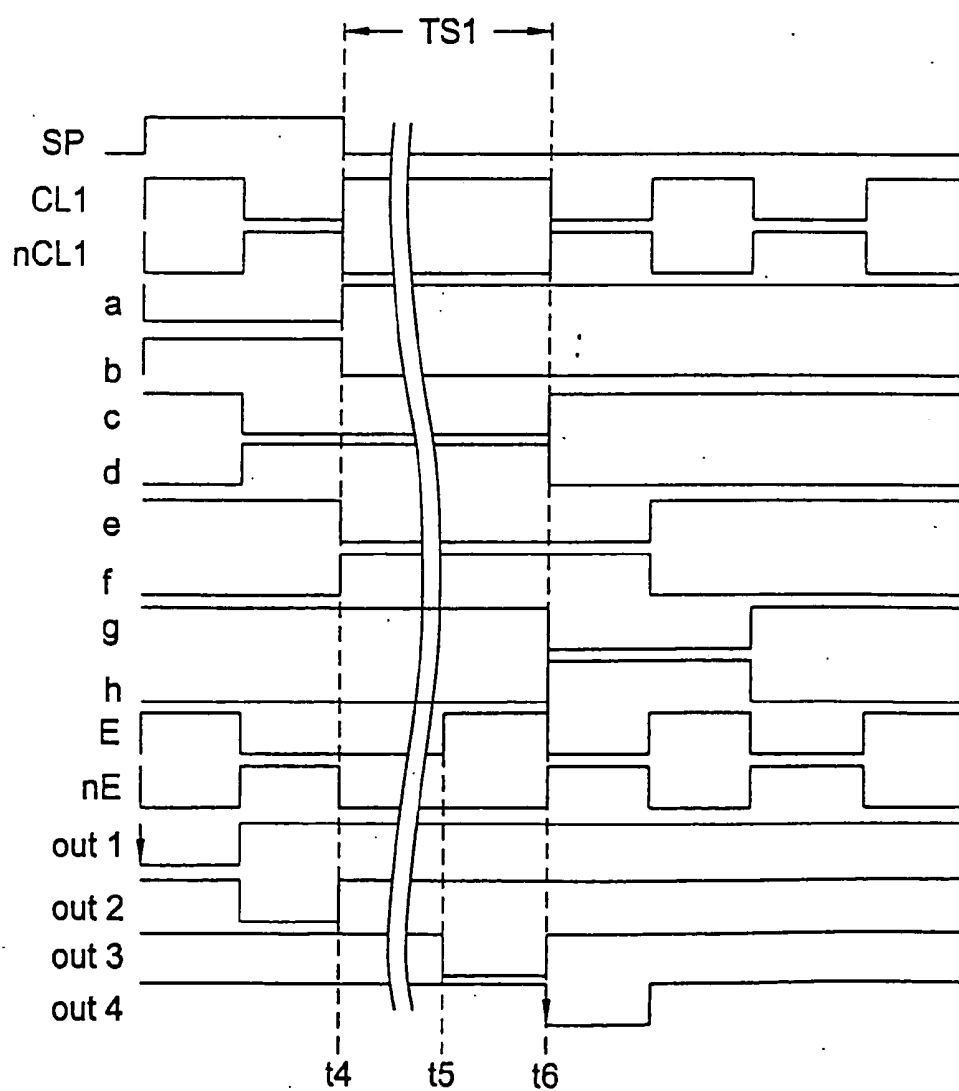


FIG. 14

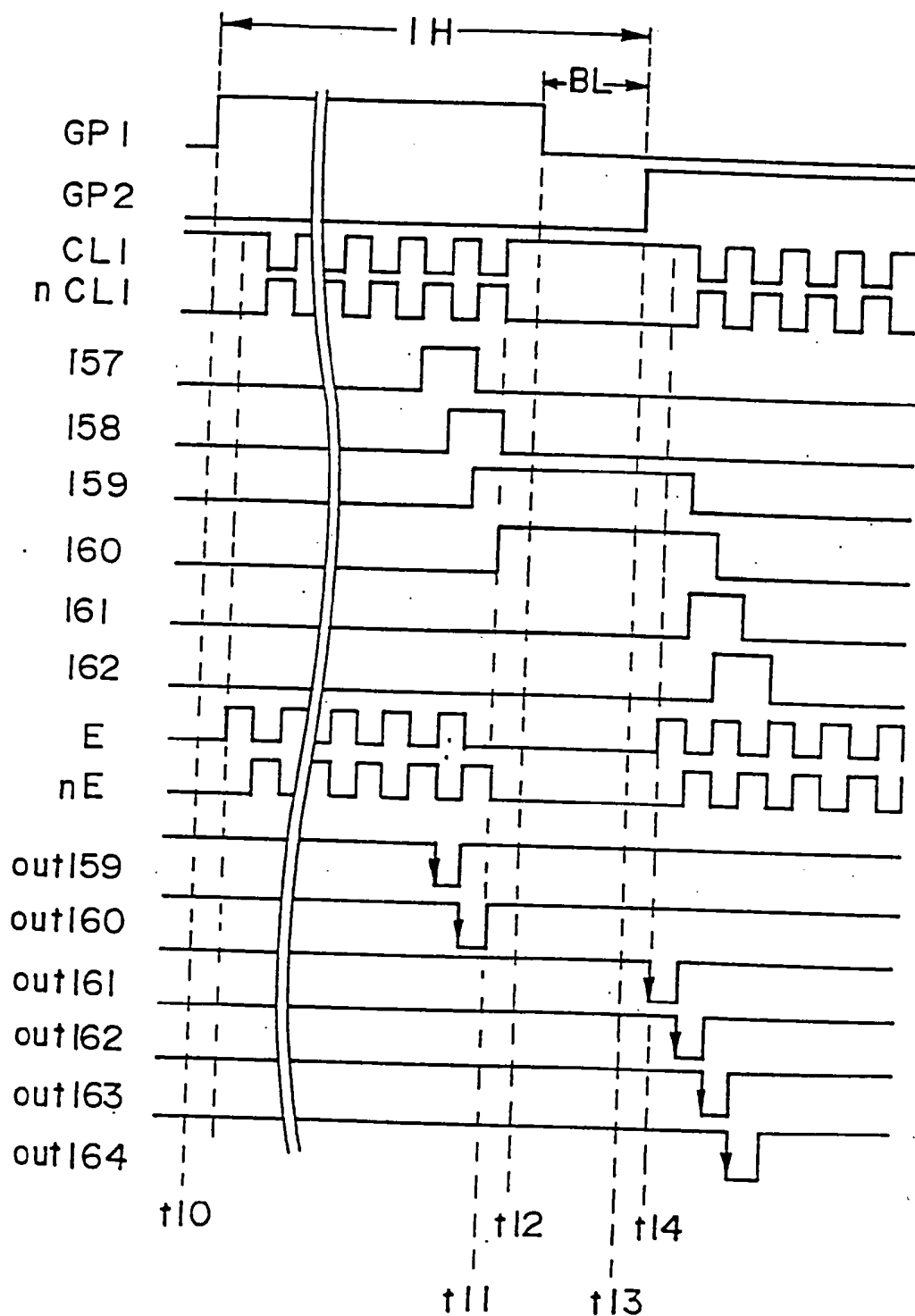


FIG. 15

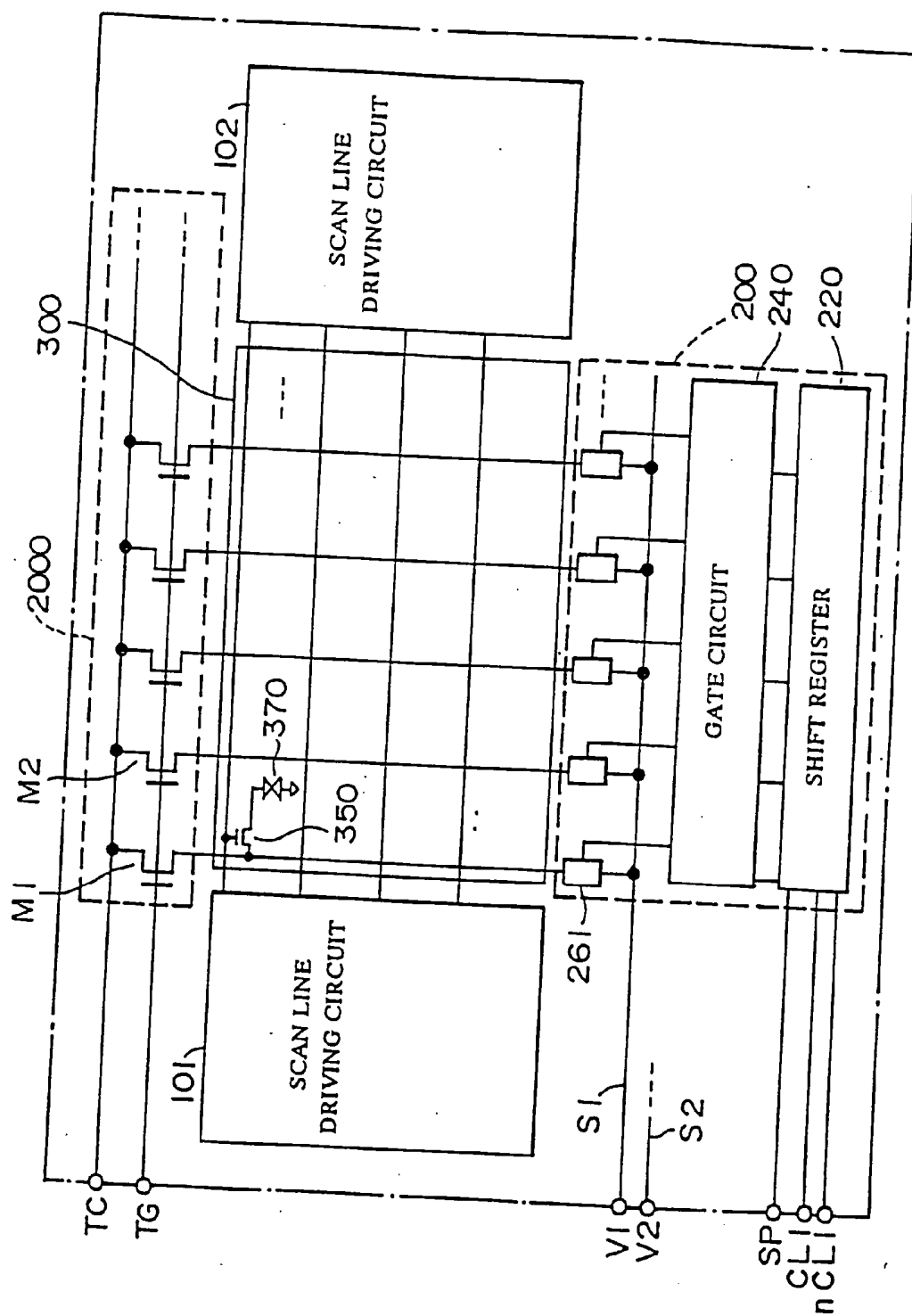


FIG. 16A

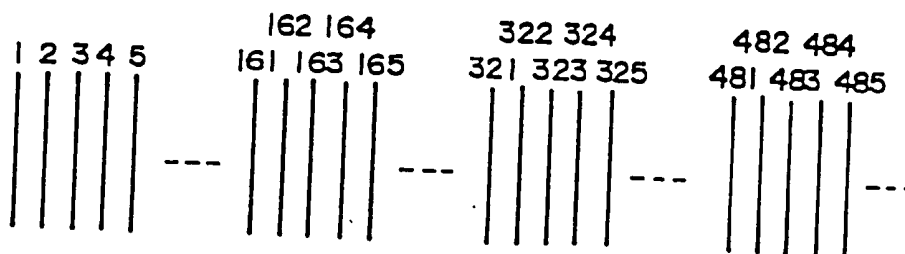


FIG. 16B

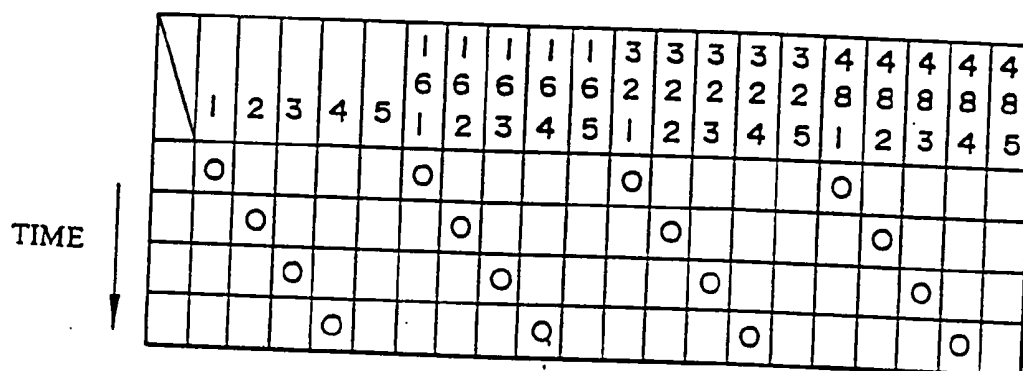


FIG. 16C

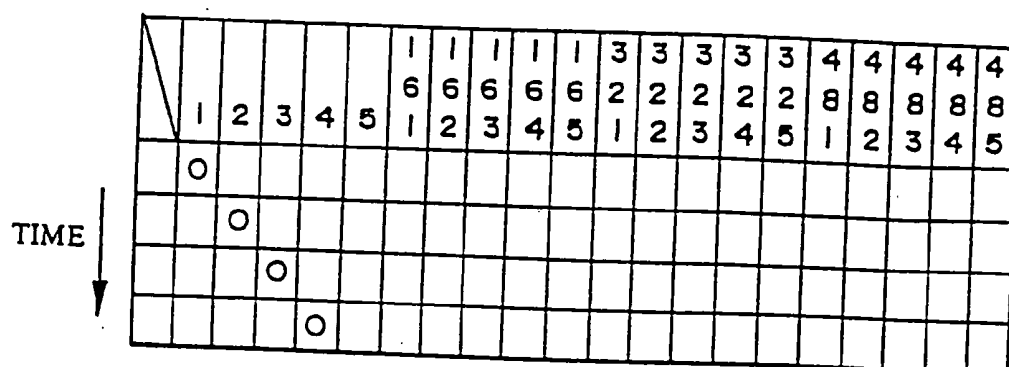


FIG. 17

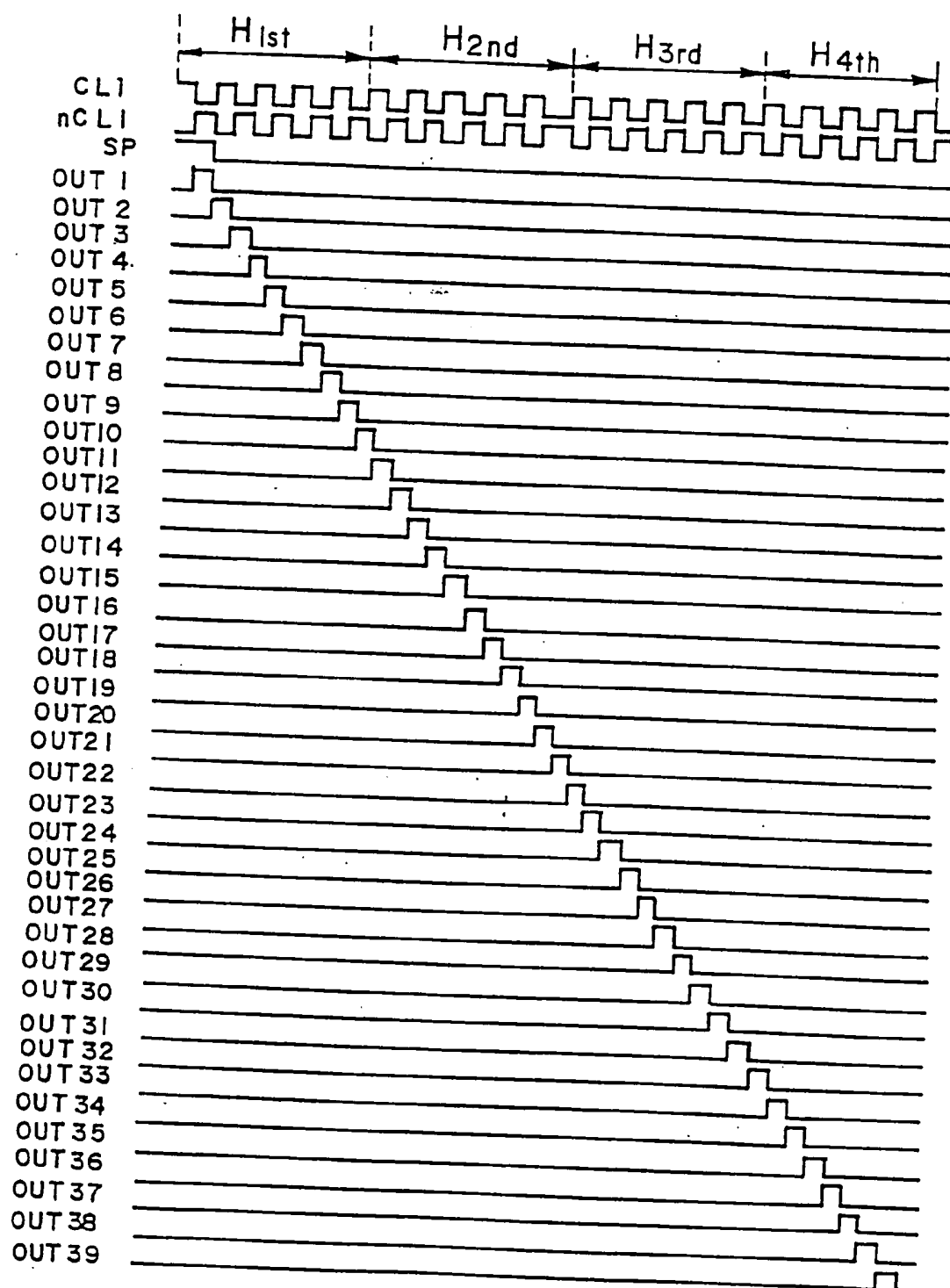


FIG. 18A

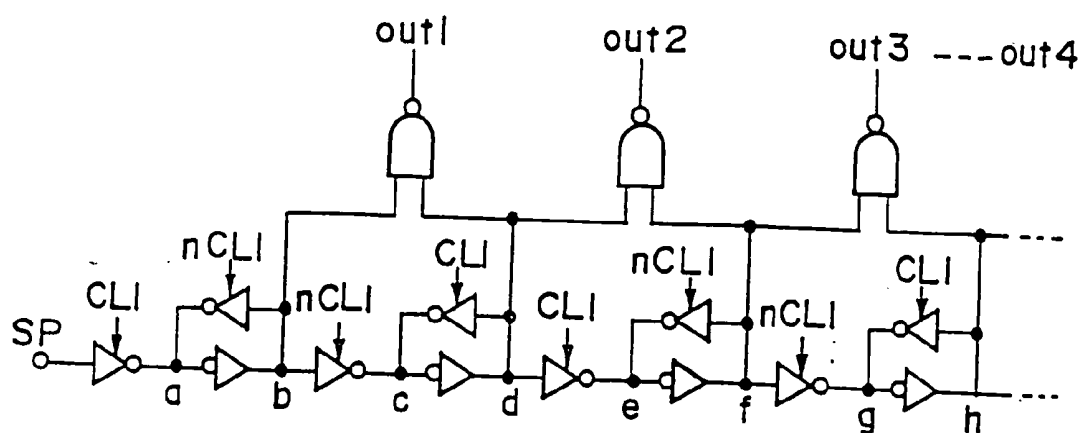


FIG. 18B

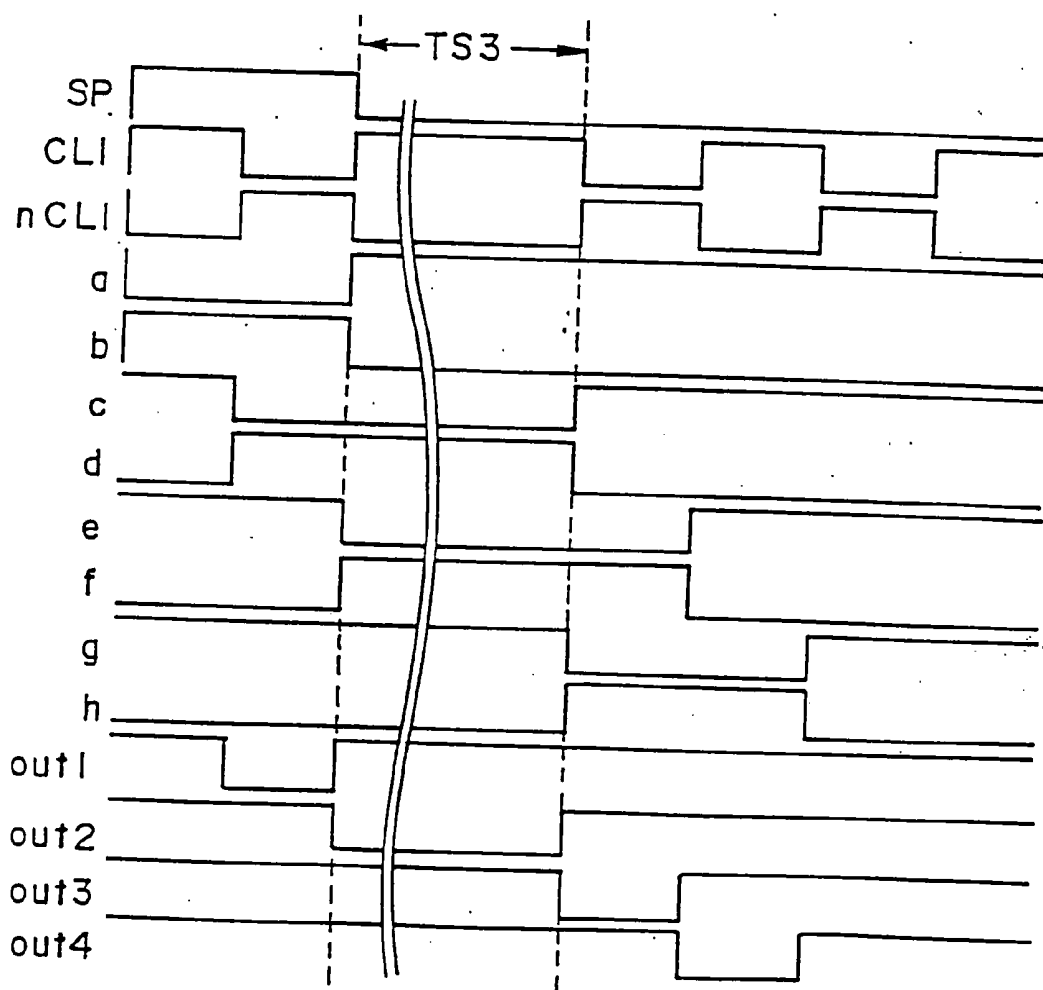


FIG. 20

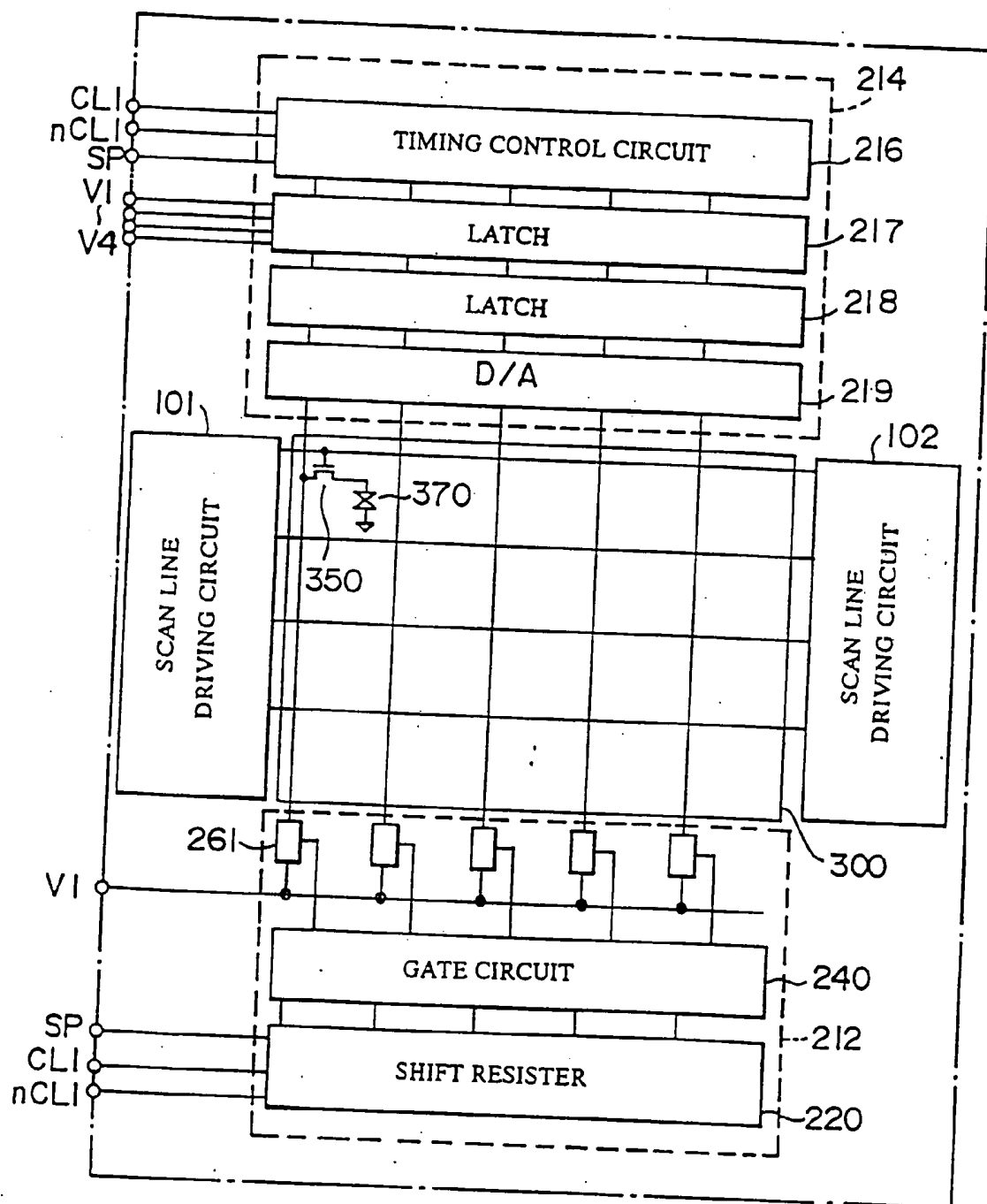


FIG. 21

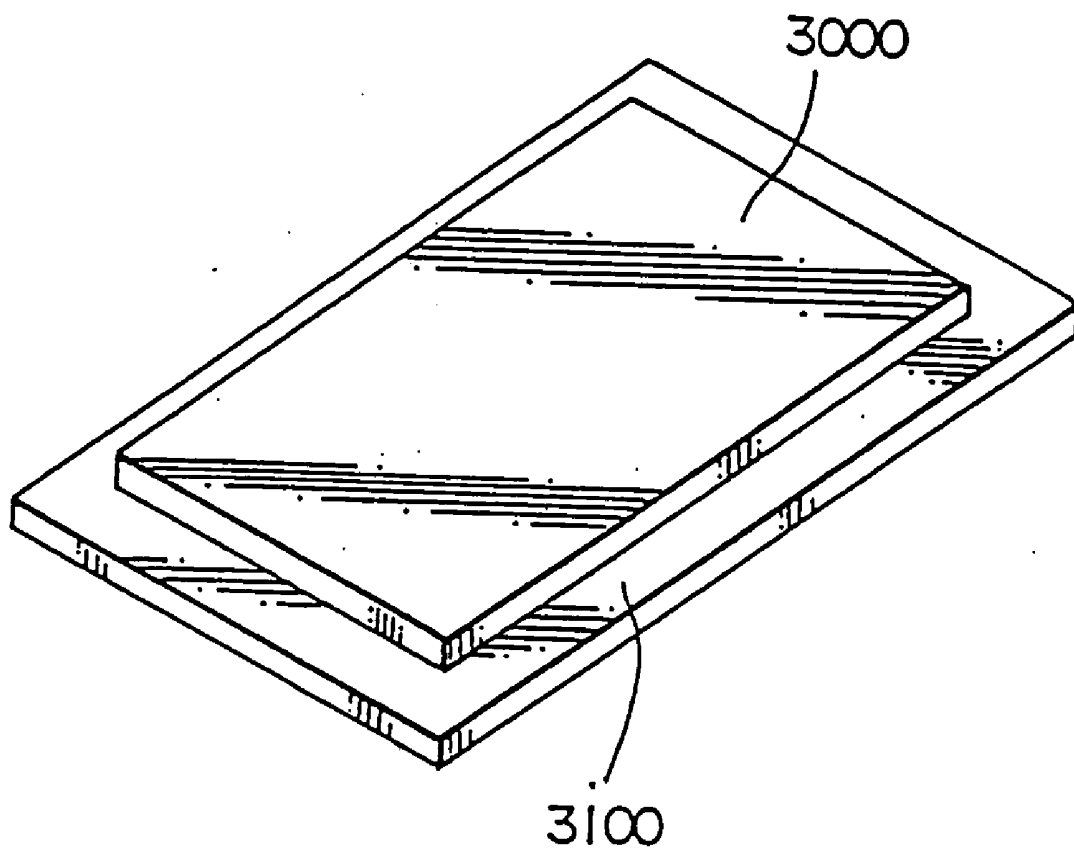


FIG. 22A

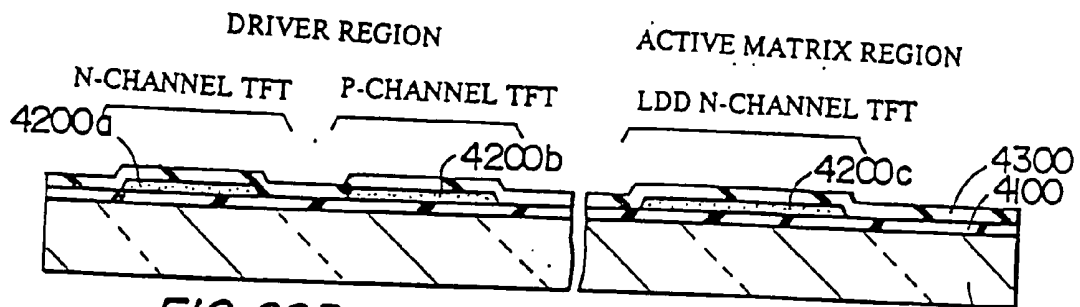


FIG. 22B

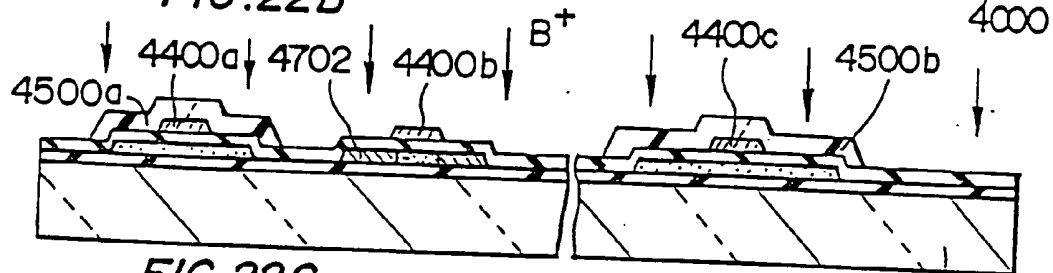


FIG. 22C

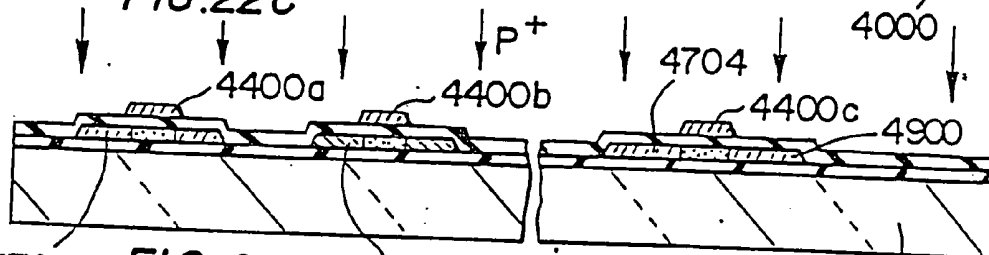


FIG. 22D

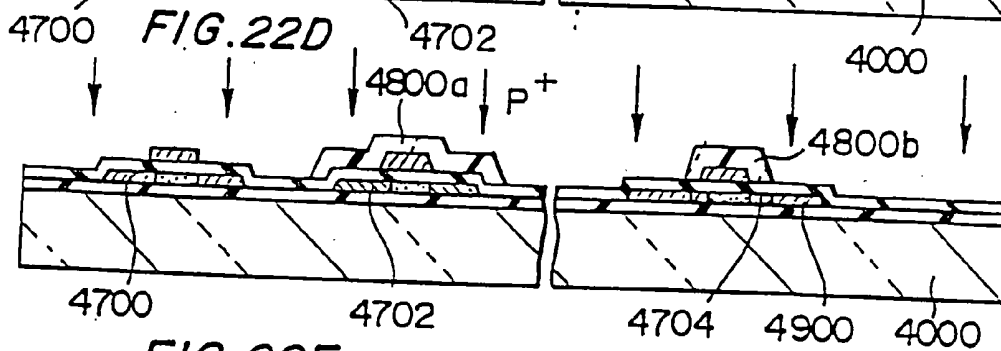


FIG. 22E

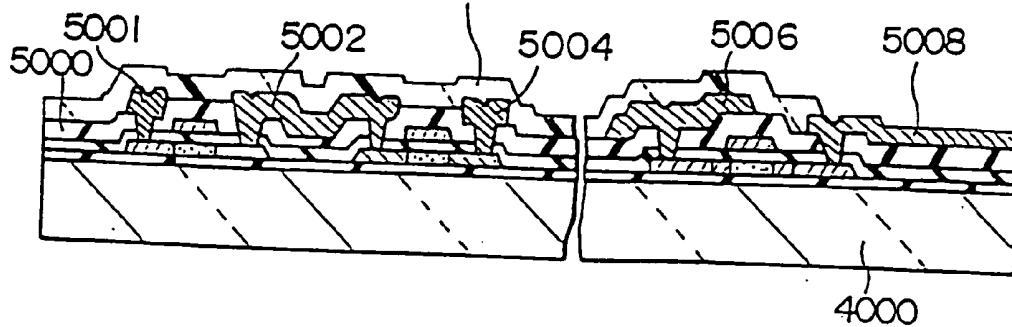


FIG. 23A

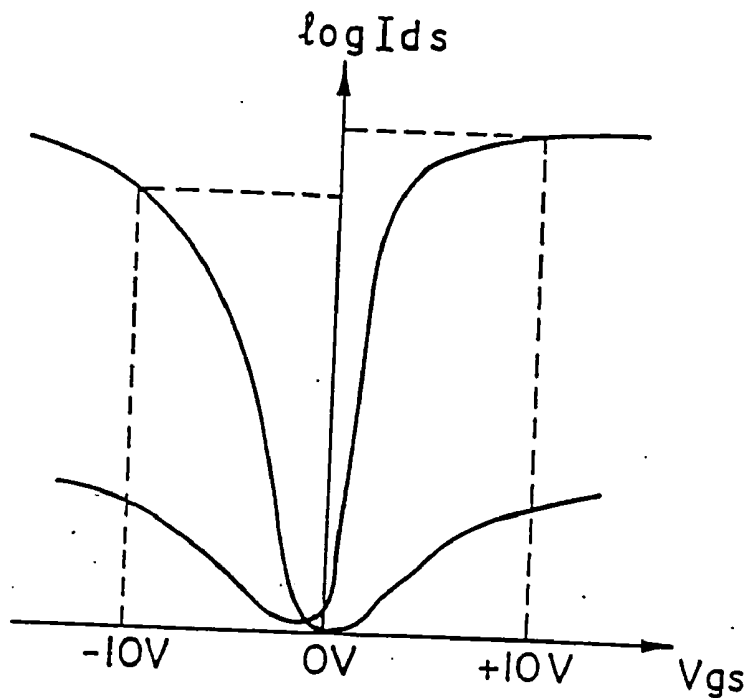


FIG. 23B

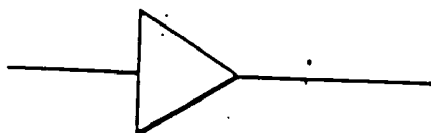


FIG. 23C

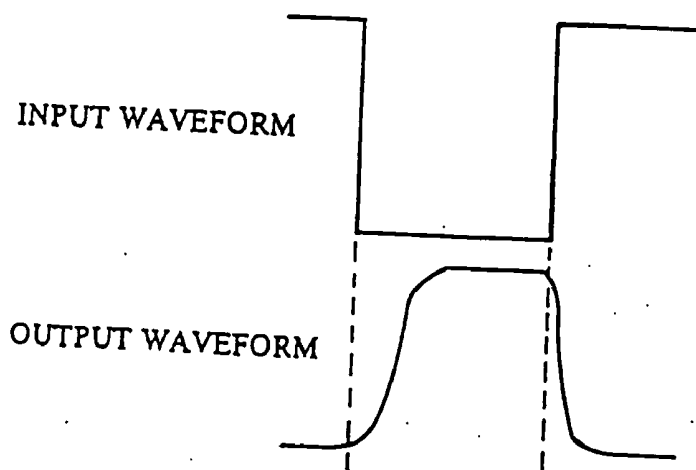


FIG. 24A

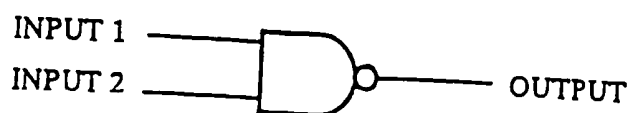


FIG. 24B

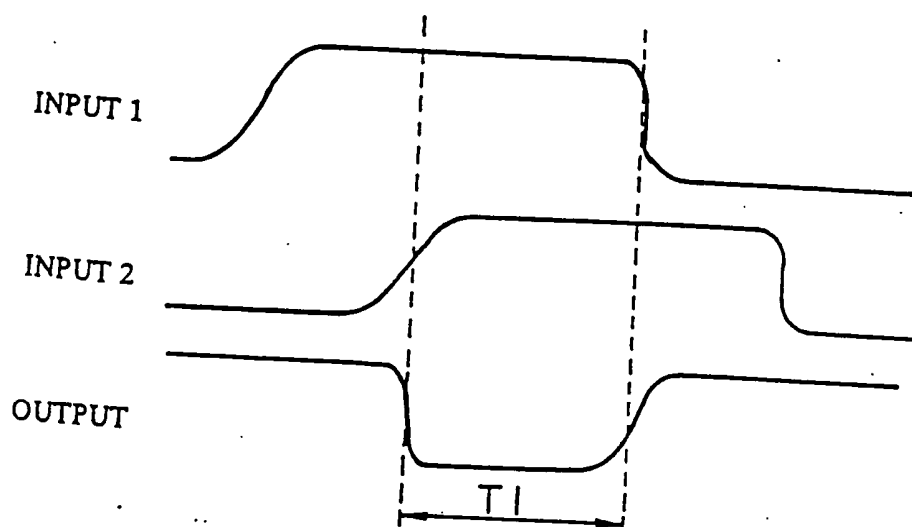


FIG. 24C



FIG. 24D

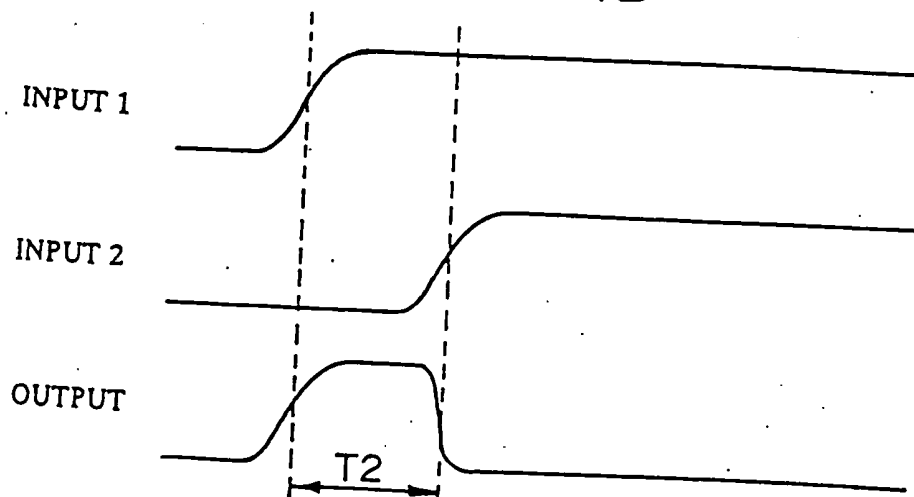


FIG. 25A

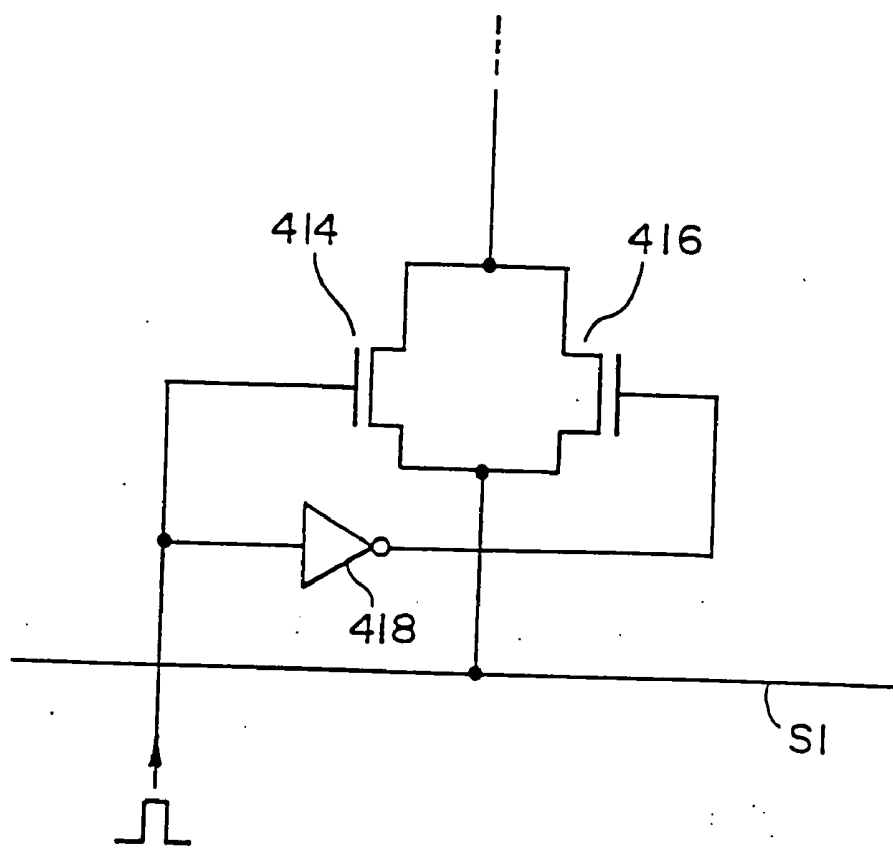
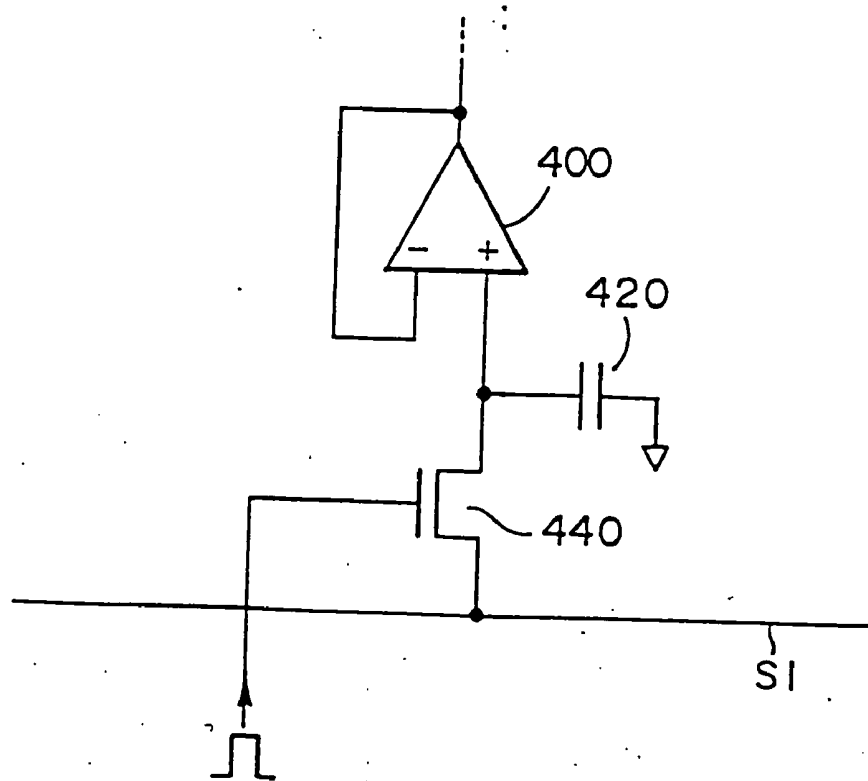


FIG. 25B



**LIQUID CRYSTAL DISPLAY DEVICE, DRIVING
METHOD FOR LIQUID CRYSTAL DISPLAY
DEVICES, AND INSPECTION METHOD FOR
LIQUID CRYSTAL DISPLAY DEVICES**

FIELD OF TECHNOLOGY

[0001] This invention pertains to a liquid crystal display device, driving methods for liquid crystal display devices, inspection methods for electrical properties of liquid crystal display devices; and, in particular, liquid crystal display devices such as those in which transistors are formed on a liquid crystal matrix substrate for the purpose of driving a liquid crystal matrix.

BACKGROUND TECHNOLOGY

[0002] In an active matrix liquid crystal display device using thin film transistors (abbreviated as TFTs in the remainder of this document) as the switching elements, if it is possible to form the active matrix driving circuits from TFTs and fabricate those TFTs at the same time as the picture element (pixel) TFTs on the active matrix substrate, the need to provide driver ICs is removed; and this is convenient.

[0003] Compared to transistors integrated on single crystal silicon, however, the operating speeds of TFTs are slow and there is a definite limit to the increase in driving circuit speed attainable. Additionally, if the driving circuits are made to operate at high speeds, the power consumption will increase by that much more.

[0004] As examples of technology for operating driving circuits of liquid crystal display devices at high speed, there is the technology in Japanese Unexamined Patent Application Showa 61-32093 and the technology in pages 609-612 of the SID Digest (1992).

[0005] In the technology described in Japanese Unexamined Patent Application Showa 61-32093, the driving circuits are composed of multiple shift registers and, by driving each shift register by clocks with slightly different phases, the effective operating frequency of the shift registers is increased.

[0006] In the SID Digest (1992), pages 609-612, technology in which multiple analog switches are driven collectively by a single output of a timing control circuit and the video signal is written in parallel is shown.

[0007] As examples of technology striving for reduced power consumption in driving circuits, there is the technology contained in Japanese Unexamined Patent Application Showa 61-32093. This technology achieves reduced power consumption by dividing the driving circuits into multiple blocks and operating only blocks which must be used while keeping all other blocks out of operation.

[0008] When actually implementing the technology described in Japanese Unexamined Patent Application 61-32093, however, it is necessary to provide multiple clocks with differing phases which leads to increased complexity of the circuit configurations and an increase in the number of terminals.

[0009] Further, in the technology described in the SID Digest (1992), pages 609-612, because multiple analog switches are driven collectively, the load is heavy and it is

necessary to provide a buffer which can drive a heavy load. Additionally, because of delays in the driving signals, it is easy for deviations to occur in the driving timing of each analog switch.

[0010] In the technology of Japanese Unexamined Patent Application 61-32093, a control circuit is necessary in order to selectively operate the divided blocks; and this leads to increased complexity of the circuitry. Additionally, this technology does not contribute at all to increasing the speed of the driving circuits.

[0011] Furthermore, when the driving circuits of the prior art described above are composed of TFTs, the circuits become complex in all cases; and the accurate, fast inspection of the circuits' electrical characteristics is difficult such that there are problems in the evaluation of reliability.

DESCRIPTION OF THE INVENTION

[0012] The present invention has taken the problems of the prior art described above into consideration. The purpose is to provide a novel liquid crystal display device and associated driving methods which allow high speed operation, a certain degree of reduction in power consumption, and ease of inspection.

[0013] In one mode of the liquid crystal display device of the present invention, multiple pulses are generated simultaneously using a single shift register.

[0014] Consequently, the frequency of the shift register output signal can be increased without changing the frequency of the shift register operation clock. When the number of simultaneously generated pulses is N (N is natural number of two or greater), the frequency of the output signal of the shift register becomes N-times.

[0015] If the shift register output signal mentioned above is used to determine the sampling timing of the video signal in an analog driver, high speed data line driving can be realized. Also, if the shift register output signal mentioned above is used to determine the latch timing of the video signal in a digital driver, high speed latching of the video signal can be realized. Consequently, high speed operation of the driving circuits is possible without increasing power consumption even when the driving circuits of the liquid crystal matrix are composed of TFTs.

[0016] In the simultaneous generation of multiple pulses using a single shift register, it is good if a stationary state such as that obtained when, for example, a single same polarity pulse is input to the shift register input terminal after one horizontal period of the video signal, waiting for the passage of at least (N-1) horizontal periods and N mutually spaced, parallel pulses are output from the output terminals of each stage of the shift register.

[0017] In another mode of the liquid crystal display device of the present invention, gate circuits are added to the single shift register with the output signals of the shift register input to the gate circuits, and the output signals of the gate circuits used as timing control signals of the circuits comprising the data line driving circuits. For example, the output signals of the gate circuits can be used as timing signals to determine the sampling timing of the video signal in an analog driver and can be used as timing signals to determine the latch timing of the video signal in a digital driver.

[0018] For example, if an EXCLUSIVE-OR gate is used as the gate circuit and the output of adjacent stages of the shift register are input into the EXCLUSIVE-OR gate, and a clock which makes two horizontal periods of the video signal one period is input to the shift register, the number of clock level changes in one horizontal period are reduced and further reduction in power consumption is possible.

[0019] In another mode of the liquid crystal display device of the present invention, by making the most use of a single shift register, a configuration which can perform electrical inspection of a liquid crystal matrix is achieved. For example, an input circuit for a testing signal is connected to one end of the data lines and video signal input lines are connected to the other ends of the data lines through analog switches.

[0020] Using the inspection signal input circuit, the inspection signals are input collectively to the data lines. Maintaining such an input, single pulses are output successively from the single shift register and these pulses are used to successively turn on multiple analog switches. The electrical characteristics of the data lines and analog switches can be inspected by receiving the inspection signals sent from one end of said data lines by way of the analog switches and the video signal input lines. For example, it is possible to accurately and quickly detect such things as frequency characteristics of data lines and analog switches as well as data line open circuits.

BRIEF EXAMINATION OF THE FIGURES

[0021] FIG. 1A shows the overall configuration of an example of a liquid crystal display device of the present invention, and FIG. 1B shows the configuration of the pixel region.

[0022] FIG. 2 is to explain the features of the example shown in FIG. 1.

[0023] FIG. 3 is a more specific circuit diagram of the circuit configuration shown in FIG. 2.

[0024] FIG. 4A shows the arrangement of the original image data, and FIG. 4B shows an example of the data arrangement when the original image data have been arranged in a time series according to the methods of the present invention.

[0025] FIG. 5 shows an example of the circuit configuration for processing an analog signal into a multiplexed signal as shown in FIG. 4B.

[0026] FIG. 6 is to explain the major operation of the circuits in FIG. 5.

[0027] FIG. 7 shows an example of the circuit configuration for processing a digital signal into a multiplexed signal as shown in FIG. 4B.

[0028] FIG. 8 shows an example of the configuration of liquid crystal matrix driving circuits for the digital line-sequential method.

[0029] FIG. 9 is a timing chart showing the operation timing of the circuits shown in FIG. 1A, FIG. 2, and FIG. 3.

[0030] FIG. 10 is a timing chart showing the output timing for the output signal of analog switch 261 shown in FIG. 1A, FIG. 2, and FIG. 3.

[0031] FIG. 11A shows the circuit configuration of a comparison example, and FIG. 11B is the signal waveform showing the problem points of the circuit in FIG. 11A.

[0032] FIG. 12A shows the essential part of the liquid crystal display device of the present invention shown in FIGS. 1 through 3, and FIG. 12B is a signal waveform showing the advantage of the circuit of FIG. 12A.

[0033] FIG. 13A shows the configuration of the essential part of another example of a liquid crystal display device of the present invention, and FIG. 13B is a timing chart to explain an example of the operation of the circuit in FIG. 13A.

[0034] FIG. 14 is timing chart for another example of the operation of the circuit shown in FIG. 13A.

[0035] FIG. 15 shows the overall configuration of another example of a liquid crystal display device of the present invention.

[0036] FIG. 16A shows the arrangement of the data lines in the circuit of FIG. 15; FIG. 16B shows the normal operation of the driving circuits of the present invention; and FIG. 16C shows an example of the operation during defect inspection of the driving circuit of FIG. 16B.

[0037] FIG. 17 is a timing chart to explain more specifically the operation of the driving circuits of the present invention shown in FIG. 16C during defect inspection.

[0038] FIG. 18A shows the configuration of the essential part of the driving circuits of the present invention, and FIG. 18B shows an example of the operation of the circuit of FIG. 18A during defect inspection.

[0039] FIG. 19A shows the configuration of the essential part of the driving circuits of the present invention, and FIG. 19B is a timing chart showing an example of the normal operation of the driving circuit of FIG. 19A.

[0040] FIG. 20 shows the configuration of another example of a liquid crystal display device of the present invention.

[0041] FIG. 21 shows an oblique projection of the structure of a liquid crystal display device.

[0042] FIG. 22A through FIG. 22E show an example of the fabrication process for simultaneously forming TFTs for the driver region and the active matrix region with the device cross-section shown for each process.

[0043] FIG. 23A shows the voltage-current characteristics for p-channel and n-channel TFTs; FIG. 23B shows the circuit diagram of a buffer circuit using p-channel TFTs and n-channel TFTs; and FIG. 23C shows input and output waveforms for the circuit of FIG. 23B.

[0044] FIG. 24A shows a NAND gate using p-channel and n-channel TFTs; FIG. 24B shows input and output waveforms for the circuit of FIG. 24A; FIG. 24C shows an EXCLUSIVE-OR gate using p-channel and n-channel TFTs; and FIG. 24D shows input and output waveforms for the circuit of FIG. 24C.

[0045] FIG. 25A shows an example of the configuration of an analog switch; and FIG. 25B shows the configuration of an analog driver.

THE BEST SYSTEMS FOR IMPLEMENTING
THE INVENTION

[0046] Using specific examples of the present invention, the contents of the present invention will be described in more detail below.

EXAMPLE 1

[0047] (Overall Configuration)

[0048] **FIG. 1A** shows the configuration of an example of a liquid crystal display device of the present invention, and **FIG. 1B** shows the configuration of the pixel region of an active matrix liquid crystal display device.

[0049] This is an example of a liquid crystal display device employing data line driving using analog switches (switch circuits).

[0050] Further, in this example, TFTs are used as the transistors comprising the data line driving circuit. These TFTs are fabricated on the substrate at the same time as the switching TFTs in the pixel region. The fabrication process will be described later.

[0051] A single pixel in pixel region (active matrix) **300** is composed of switching TFT **350** and liquid crystal element **370** as shown in **FIG. 1B**. The gate of TFT **350** is connected to scan line L(k) and the source (drain) is connected to data line D(k).

[0052] Scan lines L(k) are driven by scan line driving circuit **100** shown in **FIG. 1A**, and data lines D(k) are driven by data line driving circuit **200** shown in **FIG. 1A**.

[0053] Data line driving circuit **200** contains shift register **220** having at least as many stages as the number of data lines, gate circuit **240**, and multiple analog switches **261** which are connected to N (in this example, four) video image lines (S1 to S4).

[0054] The use of N video image lines (S1 to S4) means that the video signal is multiplexed with a degree of multiplexing of N.

[0055] Every M switches, where M is any number (M is 4 in this example), of the multiple analog switches are grouped; and the total number of groups is equal to the total number of video signal lines (that is, N). In other words, in this example four analog switches are in one group; and each analog switch in one group is connected in common to a single video image line.

[0056] In **FIG. 1A**, V1, V2, V3, and V4 indicate the multiplexed video signal; SP indicates the start pulse input into shift register **220**; and CL1 and nCL1 indicate operation clocks. CL1 and nCL1 are pulses with phases shifted by 180 degrees. In the explanations that follow, in other pulse signals, clocks which have been phase-shifted by 180 degrees are indicated by a prefix "n". Also, a digital signal of "1" corresponds to a positive pulse and a digital signal of "0" corresponds to a negative pulse.

[0057] The meaning of the multiplexing of the video image is shown in **FIG. 4B**. As shown in **FIG. 4A**, if a video signal ranging from 1 to 16 is taken as an example, normally each signal would be arranged in a time sequential order.

[0058] When the signal is multiplexed to a degree of four as in the present example, however, at time t1, individual

signals **1, 5, 9, and 13** appear simultaneously in video signals V1 to V4 as shown in **FIG. 4B**. Subsequently, at time t2, individual signals **2, 6, 10, and 14** appear simultaneously in the same way. At time t3, individual signals **3, 7, 11, and 15** appear simultaneously; and at time t4 individual signals **4, 8, 12, and 16** appear simultaneously.

[0059] The video signal multiplexing is possible, for example, by successively delaying the video signal by small amounts to make multiple video signals with slightly different phases as shown in **FIG. 6**. Such video signal delay can be achieved, for example, by using a delay circuit such as delay circuit **1200** shown in **FIG. 5**. Delay circuit **1200** is composed of four delay circuits **1202** to **1207** with identical amounts of delay connected in series. The outputs of each delay circuit supply data line driving circuit **200**. In **FIG. 5**, reference number **1000** is an analog video signal generator; and reference number **1100** is a timing controller.

[0060] In the present example, an increase in data line driving speed is achieved by multiplexing the video signal in the manner mentioned above, while simultaneously generating with a single shift register the number of pulses corresponding to the degree of multiplexing, simultaneously driving multiple analog switches, and simultaneously supplying the video signal to multiple data lines.

[0061] As shown in **FIG. 21**, the actual liquid crystal display device is formed by the combination of the active matrix substrate **3100** and the counter substrate **3000**. The liquid crystal is injected between the two substrates.

[0062] (Specific Configuration of the Data Line Driving Circuit)

[0063] In this example, there are special characteristics in the operation of the data line driving circuit **200** and these will be explained specifically below.

[0064] As shown in **FIG. 2**, in this example, in shift register **220**, multiple uniformly spaced positive pulses (a single pulse corresponds to data "1") are simultaneously shifted; and, corresponding to these, multiple mutually spaced pulses are output in parallel from each stage of the shift register. The number of parallel pulses is equivalent to the degree of multiplexing N of the video signal described above. In this example then, there are four.

[0065] These pulses are used to determine the operation timing of the analog switches **261**. Specifically, these pulses are input into gate circuit **240**; and mutually spaced, multiple parallel pulses are output from the output terminals (OUT1 to OUT (N×M)) of gate circuit **240**.

[0066] Then, in this example, these pulses output from gate circuit **240** are used to determine the sampling timing of the video signal from the analog switches.

[0067] Gate circuit **240** is used for waveform shaping. That is, there are differences in the voltage-current characteristics of p-channel and n-channel TFTs as shown in **FIG. 23A**. Therefore, if buffers such as those shown in **FIG. 23B** using these TFTs as output stage transistors are constructed, the output waveform will dull with respect to the input waveform as shown in **FIG. 23C**, thereby introducing signal delay. In order to control such delay, it is desirable to provide gate circuit **240**. It is not absolutely essential, however, and direct driving of analog switches **261** by the shift register output signal is also acceptable.

[0068] A more specific circuit configuration of data line driving circuit 200 is shown in FIG. 3.

[0069] As is shown clearly in FIG. 3, analog switch 261 is comprised of MOS transistor 410. Additionally, reference number 412 is the capacitance of the data line itself (called data line capacitance from hereon).

[0070] A single stage of shift register 220 (reference number 500) is comprised of inverter 504 and clocked inverters 502 and 506.

[0071] Gate circuit 240 has dual input NAND gates 241 to 246 which accept as inputs the outputs from two adjacent stages of the shift register.

[0072] (Explanation of Circuit Operation)

[0073] Next, the operation of the circuit shown in FIG. 3 will be explained in detail using FIG. 9 and FIG. 10. FIG. 9 shows the initial stages of operation prior to the time at which the four parallel pulses from shift register 220 are output steadily (that condition is shown in FIG. 10).

[0074] In FIG. 9, a through g, display the signal waveforms at the output terminals, shown in FIG. 3, of each stage of shift register 220; and OUT1 through OUT6 display the output signal waveforms of each of the NAND gates 241 to 246 also shown in FIG. 3. GP is the select pulse for a single scan line; and H1st indicates the first select period while H2nd indicates the second select period. Also, as explained above, CL1 and nCL1 are the operation clocks; and SP is the start pulse. The same definitions apply to FIG. 10.

[0075] As shown in FIG. 9, when a single start pulse (SP) is sequentially input to shift register 200 in the first select period (1H), a single pulse corresponding to this input pulse is output from each stage of shift register 220, and this pulse is sequentially shifted. In response, a single pulse is sequentially output from each of NAND gates 241 through 246.

[0076] This type of operation is repeated; and, as shown in FIG. 10, at the beginning of the fourth select period H4th (time t2), for the first time, four pulses are output simultaneously from the gate circuit 240 (OUT1, OUT11, OUT21, OUT31). Thereafter, each pulse runs parallel in the same direction while maintaining mutual spacing and a state in which four pulses are simultaneously output is steadily realized.

[0077] By means of four simultaneously output pulses obtained as described above, the MOS transistors comprising each analog switch 261 are turned on simultaneously, the multiplexed video signal is simultaneously sampled, and the video signal is simultaneously supplied to the corresponding four data lines.

[0078] In other words, when a pulse is input, MOS transistors 410 turn on, data lines (D(n)) and video signal lines (S1 to S4) are electrically connected, and the analog signal is written to the data line capacitance 412. Then, when MOS transistors 410 are turned off, the written signal is held in data line capacitances 412. Data line capacitance 412 functions as a holding capacitor. Because the data line drivers are composed only of analog switches, the circuit configuration is simple and it is possible to increase the degree of integration. Additionally, it is possible to accurately sample the video signal. In the case of relatively small liquid crystal

panels, it is possible to adequately drive the data lines using a driver having only analog switches as in this example.

[0079] In the manner described above, in this example, first, multiple pulses are generated simultaneously using a single shift register. Consequently, it is possible to increase the frequency of the shift register output signal without changing the frequency of the shift register's operation clock. When the number of simultaneously generated pulses is N (N is a natural number of two or greater), the frequency of the shift register output signal becomes N-times.

[0080] Then, by using each output signal of the shift register to determine the sampling timing of the video signal from the analog switches, high speed data line driving is realized. As a result, high speed data line driving is possible without increasing power consumption even when the liquid crystal matrix driving circuits are composed of TFTs.

[0081] It is also possible to use analog switches comprised of CMOS as shown in FIG. 25A as well as those comprised of single MOS transistors. CMOS switches are comprised of MOS transistors 414 and 416 and inverter 418.

[0082] It is also possible to use analog drivers such as shown in FIG. 25B as data line drivers. Analog drivers are composed of a sample and hold circuit containing MOS transistor 440 and holding capacitor 420 and a buffer circuit (voltage follower) 400.

[0083] This example has unique effects as described below. In the following, this example will be compared with a comparison example and the unique effects described.

COMPARISON EXAMPLE

[0084] FIG. 11A shows the configuration of the data line driving circuit of a comparison example, and FIG. 11B illustrates the problem points of the configuration in FIG. 11A.

[0085] In the comparison example of FIG. 1A, there are multiple shift registers (SR) and gate circuits (222 to 226, 242 to 246); and start pulses are supplied individually to each shift register. It is necessary for the input of the start pulses to the shift register to pass through special wiring S10.

[0086] In this case, start pulse input wire S10 intersects wire S20 used to input the operation clocks CL1 and nCL1 to each of the shift registers 222, 224, and 226. The result is the superposition of noise on the start pulse as shown in FIG. 11B.

[0087] The length of start pulse input wire S10 is at least on the order of 10 μm , and consequently is a major obstacle to miniaturization.

[0088] Additionally, the start pulse is delayed by the wiring resistance; and there is the danger that there will be differences in the input timing to each shift register.

[0089] In contrast, in the data line driving circuit of the present example, as shown in FIG. 12A, if the start pulse (SP) is input at the left side of the single shift register 220 with the desired timing, special start pulse wiring is not necessary.

[0090] As a result, in this example, there is no superposition of noise on the start pulse as shown in FIG. 11B, and a reduction in layout area can be achieved.

[0091] Also, because multiple pulses are generated by a single shift register, there is no delay in the start pulse.

[0092] In such a fashion, according to this invention, it is possible to achieve both miniaturization of the circuits and decrease in the frequency of the shift register operation clocks. Consequently, for example, both high speed and accurate operation can be insured even when TFTs made using a low temperature process are used as the TFTs comprising the data line driving circuit.

[0093] Therefore, if the present example is employed, it is possible to improve the performance of liquid crystal display devices having driving circuits composed of TFTs.

[0094] (TFT Manufacturing Process)

[0095] **FIGS. 22A through 22E** show one example of the manufacturing process (low temperature process) when the driver TFTs and the active matrix (pixel) TFTs are formed simultaneously on the substrate. The TFTs produced by this manufacturing process use polysilicon and have an LDD (lightly doped drain) structure.

[0096] First, insulating layer **4100** is formed on top of glass substrate **4000**. Following the formation of polysilicon islands (**4200a**, **4200b**, **4200c**) on top of insulating layer **4100**, the gate oxide layer **4300** is formed over the entire surface (**FIG. 22A**).

[0097] Next, after forming gate electrodes **4400a**, **4400b**, and **4400c**, mask material **4500a** and **4500b** are formed. Next, boron is ion implanted to a high concentration and p-type source and drain regions **4702** are formed (**FIG. 22b**).

[0098] Mask material **4500a** and **4500b** is then removed, phosphorous is ion implanted and n-type source and drain regions **4700** and **4900** are formed (**FIG. 22C**).

[0099] After mask material **4800a** and **4800b** is formed, phosphorous is ion implanted (**FIG. 22D**).

[0100] Interlayer dielectric layer **5000**; metal electrodes **5001**, **5002**, **5004**, **5006**, **5008**; and final passivation layer **6000** are formed to complete the device.

EXAMPLE 2

[0101] The present invention is applicable not only to data line driving circuits using analog drivers but also to data line driving circuits using digital drivers.

[0102] **FIG. 8** shows an example of the configuration of a line sequential driving data line driving circuit using digital drivers.

[0103] The special features of the configuration of this circuit include first latch **1500** which takes in the digital video signal (**V1a** to **V1d**) and stores it temporarily, second latch **1510** which collectively takes in each data bit from first latch **1500** and stores it temporarily, and D/A converter **1600** which simultaneously converts every digital data bit from second latch **1510** into an analog signal and simultaneously drives all the data lines.

[0104] The technology shown in the first example above is also applicable to the handling of the digital video signal (**V1a** to **V1d**) in first latch **1500** in circuits using digital drivers as described above. In other words, by multiplexing the digital video signal (**V1a** to **V1d**) and, further, simultaneously generating multiple pulses from a single shift reg-

ister and then using these pulses to latch in parallel multiple data of the digital video signal, it is possible to increase the latch speed of the digital video signal without increasing the frequency of the shift register operation clocks.

[0105] The multiplexing of the digital video signal can be realized, for example, by data recomposition circuit **1270** shown in **FIG. 7**. In **FIG. 7**, reference number **1000** indicates an analog video signal generator; reference number **1250** indicates an A/D converter circuit; reference number **1260** indicates a γ -correction ROM; and reference number **1110** indicates a timing controller.

[0106] The present invention is not limited to line sequential driving digital drivers, but is also can be applicable to point sequential driving digital drivers.

EXAMPLE 3

[0107] The special features of the third example of the present invention are shown in **FIGS. 19A and 19B**. In the first example, gate circuit **240** was composed of NAND gates (**FIG. 3**); but in this example, gate circuit **240** is composed of EXCLUSIVE-OR gates **251**. EXCLUSIVE-OR gates **251** take as inputs the outputs from two adjacent stages of the shift register (**a**, **b** . . .) and output pulses (**X**, **Y**, **Z** . . .) used to determine the sampling timing of the video signal.

[0108] The advantages of using EXCLUSIVE-OR gates **251** are that it is possible to reduce power consumption if one period of the start pulse (**SP**) is made equivalent to two select periods (twice the select period) and it is possible to avoid the spread of the pulse width since the trailing edge of the output pulse becomes sharp.

[0109] That is, as shown in **FIG. 3**, when one period of the start pulse (**SP**) is made equivalent to two select periods (twice the select period), along with the parallel output of pulses as a result of the circuit operation similar to that shown in **FIG. 9**, the number of level changes of the output (**a**, **b** . . . of each stage of the shift register in one select period is half when compared to the type of operation shown in **FIG. 9**.

[0110] In other words, as shown in **FIG. 19B**, there is one signal level change within one select period (**1H**) at point **b** in **FIG. 19A**. That is, in one select period (**1H**), there is only one positive edge **R3**.

[0111] In contrast, in the circuit operation shown in **FIG. 9**, the signal level at point **b** changes twice within one select period (**1H**). In one select period (**1H**), there are both positive edge **R1** and negative edge **R2**. Consequently, in comparison to the case of **FIG. 9**, the number of signal level changes for the case of **FIG. 19** is reduced by half; and, accompanying this, the power consumption is reduced to about half.

[0112] Also, as shown in **FIG. 24B**, in contrast to the case of a two input NAND gate (shown in **FIG. 24A**) in which the output pulse width (**T1**) is determined by the positive edge for one input and the negative edge for the other input, in the case of a two input EXCLUSIVE-OR gate (**FIG. 24C**), the output pulse width (**T2**) is determined by positive edges for both inputs. Because of this, the trailing edge of the output pulse becomes sharp; and spread of the pulse width can be prevented.

EXAMPLE 4

[0113] **FIG. 13** shows the configuration of the essential component of a fourth example of the present invention.

[0114] The special feature of this example is that the gate circuit **240** of **FIG. 1** is composed of NAND gates (**241, 242, 243, 244 . . .**) which take as inputs the output of each shift register and an output enable signal (E, nE).

[0115] By means of the control afforded by the output enable signals (E, nE), the shift register output level and the gate circuit output level are independent and possible to control. By making use of this special feature, while the circuit is in operation, it is possible to both temporarily interrupt the generation of pulses from the NAND gates (**241, 242, 243, 244 . . .**) and resume the pulse generation after terminating the interruption.

[0116] For example, in **FIG. 13B**, consider the cessation of NAND gate (**241, 242, 243, 244 . . .**) pulse generation from time **t4** to **t6** (period **TS1**) and the resumption of pulse generation at time **t6**.

[0117] This type of operation can be achieved by stopping operation clocks **CL1** and **nCL1** during period **TS1**; and, on the other hand, fixing the output enable signal (E) at low level from time **t4** to time **t5**, and then resuming the variation to that of the same period as the operation clock at time **t5**. It is sufficient if output enable signal (nE) resumes to that of the same period as the operation clocks at time **t6**.

[0118] This type of pulse generation interruption technology can be used, for example, to prevent video signal sampling during the horizontal blanking period (BL).

[0119] **FIG. 14** shows the interruption of gate circuit pulse generation during the horizontal blanking period (times **t12** to **t13**) in an actual circuit. In **FIG. 14**, for example, **157** indicates the output of stage **157** of the single shift register and **OUT159** indicates the output of the **159th** NAND gate.

[0120] As shown clearly in **FIG. 14**, in order to stop the generation of pulses from the gate circuit during the horizontal blanking period (time **t12** to **t13**), it is necessary to stop the operation clocks (**CL1, nCL1**) and the enable singles (n, nE) between times **t1** and **t4**.

EXAMPLE 5

[0121] The liquid crystal display device shown in **FIG. 1** is also suitable for inspecting the electrical characteristics of the data lines and other components. That is, as shown in the top of **FIG. 15**, by providing inspection signal input circuit **2000**, it is possible to accurately and quickly detect such things as data line and analog switch frequency characteristics and data line open circuits.

[0122] In **FIG. 15**, inspection signal input circuit **200** is connected to one end of the data lines; and video signal input line **S1** is connected to the other end of the data lines via analog switch **261**. In **FIG. 15**, **TG** represents the test enable signal; and **TC** represents the supply voltage.

[0123] Inspection is performed as described below.

[0124] First, the test enable signal **TG** is activated; and the supply voltage (inspection voltage) is collectively supplied to each data line.

[0125] Under such an applied voltage state, a single pulse is sequentially output from the single shift register. When this is done, single pulses are output from gate circuit **240**. By means of these pulses, the analog switches are turned on sequentially. As a result, the voltage supplied to one end of the data lines can be received through analog switches **261** and video signal input line **S1**. It is thus possible to inspect the electrical characteristics of the data lines and the analog switches.

[0126] In this example, the generation of single, sequential pulses from the single shift register is necessary. In other words, the data lines are arranged as shown in **FIG. 16A**. In the previous examples, simultaneous driving of multiple data lines was employed as shown in **FIG. 16B**; but in the present example, it is necessary to switch to a driving method in which each line is scanned sequentially as shown in **FIG. 16C**.

[0127] This type of switch can be easily accomplished by changing the input method for the start pulse as shown in **FIG. 17**. In other words, as shown in **FIG. 17**, a single start pulse (SP) is input at the beginning of the first select period (**H1st**). If that pulse is shifted across all of the output stages, single pulses are sequentially generated; and, if a single start pulse (SP) is input after each select period, it is possible to simultaneously generate multiple pulses as shown in **FIG. 10**.

[0128] By sequentially generating single pulses from a single shift register, it is possible to check the electrical characteristics of each line; and inspection becomes simple.

[0129] Further, when the configuration of **FIG. 18A** is used, if shift register operation clocks **CL1** and **nCL1** are stopped during a fixed period (**TS3**), only the NAND gate output (**OUT1**) is at high level during that period as shown in **FIG. 18B**. Consequently, only the corresponding analog switch will be on; and it is possible to thoroughly inspect just the first data line.

[0130] In **FIG. 20**, instead of the special inspection signal input circuit **2000**, it is acceptable to provide line sequential digital driver **214** (having the same configuration as that of **FIG. 8**). In this case, in addition to operation as a true data line driver, digital driver **214** also functions as an inspection signal input circuit.

[0131] In the configuration of **FIG. 20**, both data line driving based on an analog video signal and data line driving based on a digital video signal are possible.

[0132] If the liquid crystal display device described above is used as a display device in equipment such as personal computers, the product value increases.

1. A driving circuit, comprising:

N switch groups each of which includes a plurality of M switches two of which are adjacent to each other, the N being a natural number that is not less than 2, the M being a natural number that is not less than 2;

a plurality of video signal lines transmitting a plurality of video signals to a plurality of switches of all of the N switch groups, one of the plurality of video signal lines electrically connecting to the M switch circuits; and

a shift resistor outputting a plurality of timing signals that control the plurality of switch circuits of all of the N switch groups.

2. A driving circuit, comprising:

a plurality of switches including N of the plurality of switches outputting N output signals simultaneously, at least one switch of the plurality of switches except for the N of the plurality of switches being disposed between one of the N of the plurality of switches and another of the N of the plurality of switches, the N being a natural number that is not less than 2;

a plurality of video signal lines providing a plurality of video signals to the plurality of switches; and

a shift resistor outputting a plurality of timing signals that control the plurality of switches.

3. A driving circuit, comprising:

a plurality of switches that is divided into a first group and a second group, one switch of the first group and one switch of the second group transmitting output signals simultaneously, at least one of the plurality of switches except for the one switch of the first group and the one switch of the second group being disposed between the one switch of the first group and the one switch of the second group;

a plurality of video signal lines providing a plurality of video signals to the plurality of switches; and

a shift resistor outputting a plurality of timing signals that control the plurality of switches.

4. A driving circuit, comprising:

a D/A converter converting a plurality of digital video signals into a plurality of analog video signals;

N circuit groups each of which includes a plurality of M latch circuits two of which are adjacent to each other, a plurality of latch circuits of all of the N circuit groups transmitting the digital video signals to the D/A converter, the N being a natural number that is not less than 2, the M being a natural number that is not less than 2;

a plurality of video signal lines transmitting a plurality of video signals to the plurality of latch circuits of all of the N circuit groups, one of the plurality of video signal lines electrically connecting to the M latch circuits; and

a shift resistor outputting a plurality of timing signals that control the plurality of latch circuits of the N circuit groups.

5. A driving circuit, comprising:

a D/A converter that converting a plurality of digital video signals into a plurality of analog video signals;

a plurality of first latch circuits transmitting the digital video signals to the D/A converter;

N circuit groups each of which includes a plurality of M second latch circuits two of them are adjacent to each other, a plurality of second latch circuits of all of the N circuit groups transmitting the digital video signals to the D/A converter, the N being a natural number that is not less than 2, the M being a natural number that is not less than 2;

a plurality of video signal lines transmitting a plurality of video signals to the plurality of second latch circuits of all of the N circuit groups, one of the plurality of video signal lines electrically connecting to the M second latch circuits; and

a shift resistor outputting a plurality of timing signals that control the plurality of second latch circuits of the N circuit groups.

6. The driving circuit according to claim 1, N of the plurality of switches outputting N output signals simultaneously, at least one switch of the plurality of switch circuits except for the N of the plurality of switches being disposed between one of the N of the plurality of switches and another of the N of the plurality of switches.

7. The driving circuit according to claim 1, each the plurality of switches of the N switch groups being an analog switch.

8. The driving circuit according to claim 1, a number of the plurality of video signal lines being N, the plurality of switches of all of the N switch groups outputting N of the plurality of output signals simultaneously, each of the N of the plurality of output signals being outputted from different groups of the N switch groups.

9. The driving circuit according to claim 1, further comprising:

a gate circuits providing a plurality of gate signals to the plurality of switches of all of the N switch groups, the gate circuits inputting a plurality of timing signals that are outputted from the shift resistor.

10. The driving circuit according to claim 9, the gate circuit including a plurality of NAND gates, each of the NAND gates inputting two of the timing signals from the shift resistor, and each of the NAND gates outputting one of the gate signals to one of the switches.

11. The driving circuit according to claim 9, the gate circuit including a plurality of XOR gates, each of the XOR gates inputting two of the timing signals from the shift resistor, and each of the XOR gates outputting one of the gate signals to one of the switches.

12. The driving circuit according to claim 9, further comprising:

an output enable signal line that provides an output enable signal, the gate circuit including a plurality of NAND gates, each of the NAND gates inputting one of the timing signals from the shift resistor and the output enable signal, each of the NAND gates outputting one of the gate signals to one of the switches.

13. An active matrix substrate comprising: a plurality of scan lines;

a plurality of data lines crossing the scan lines; and

the driving circuit according to claim 1, the plurality of switch circuits of all of the N switch groups electrically connecting the plurality of the data lines.

14. A display device comprising:

a plurality of scan lines;

a plurality of data lines crossing the scan lines; and

the driving circuit according to claim 1, the plurality of switch circuits of all of the N switch groups electrically connecting the plurality of the data lines.

专利名称(译)	液晶显示装置，液晶显示装置的驱动方法和液晶显示装置的检查方法		
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摘要(译)

使用使用单个移位寄存器并同时产生多个脉冲的技术，本发明是一种快速驱动数据线的液晶显示器件。可以在不改变移位寄存器操作时钟的频率的情况下增加移位寄存器输出信号的频率。如果移位寄存器输出信号通过模拟开关用于确定视频信号采样定时，则可以实现高速数据线驱动。另外，如果上述移位寄存器的输出信号用于确定数字驱动器中的视频信号锁存定时，则可以实现视频信号的高速锁存。因此，即使液晶显示矩阵的驱动电路由TFT构成，也可以在不增加功耗的情况下高速操作驱动电路。移位寄存器还可用于检查数据线和模拟开关的电气特性。

