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(54) PIXEL STRUCTURE

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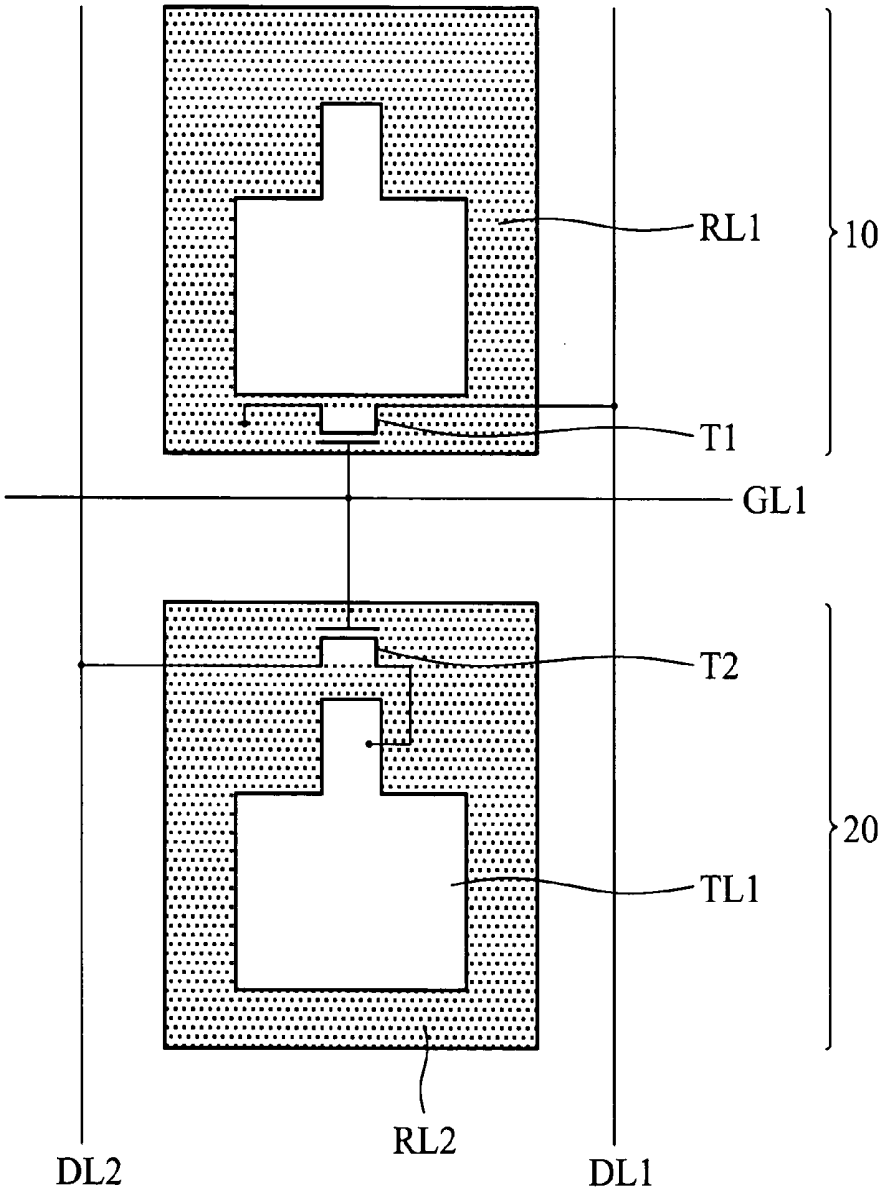
(52) **U.S. Cl.** **349/114**

(57) **ABSTRACT**

A pixel structure of a transflective LCD disposed between a first data line and a second data line. The pixel structure comprises a reflective cell and a transmission cell. The transistor comprises a gate coupled to a scan line, a source coupled to the first data line, and a drain coupled to the first reflective electrode. The first transistor is covered by the first reflective electrode. The transmission cell comprises a second transistor and a transparent electrode. The second transistor comprises a gate coupled to the scan line, a source coupled to the second data line, and a drain coupled to the transparent electrode. The second transistor is covered by a second reflective electrode.



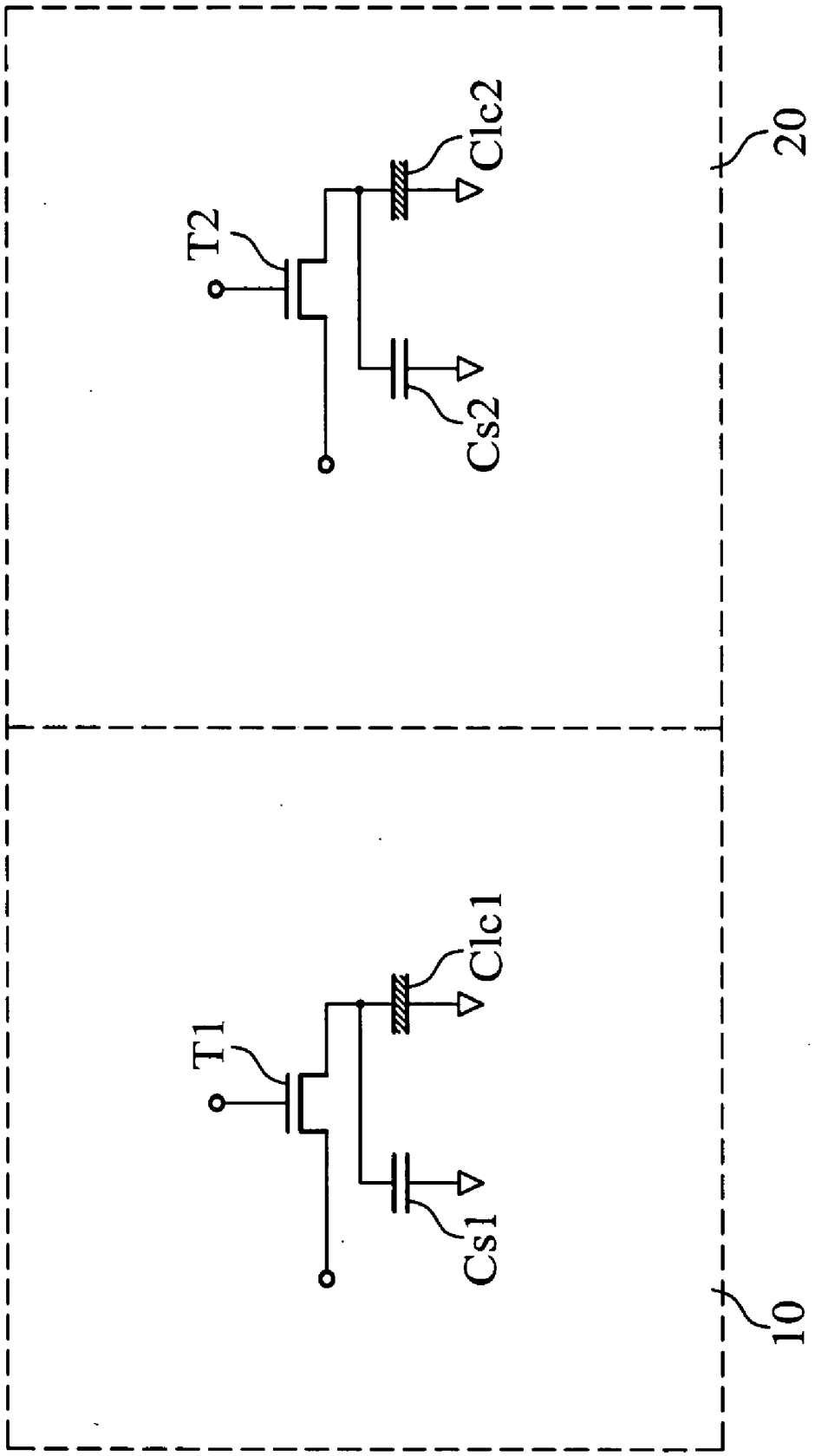


FIG. 1

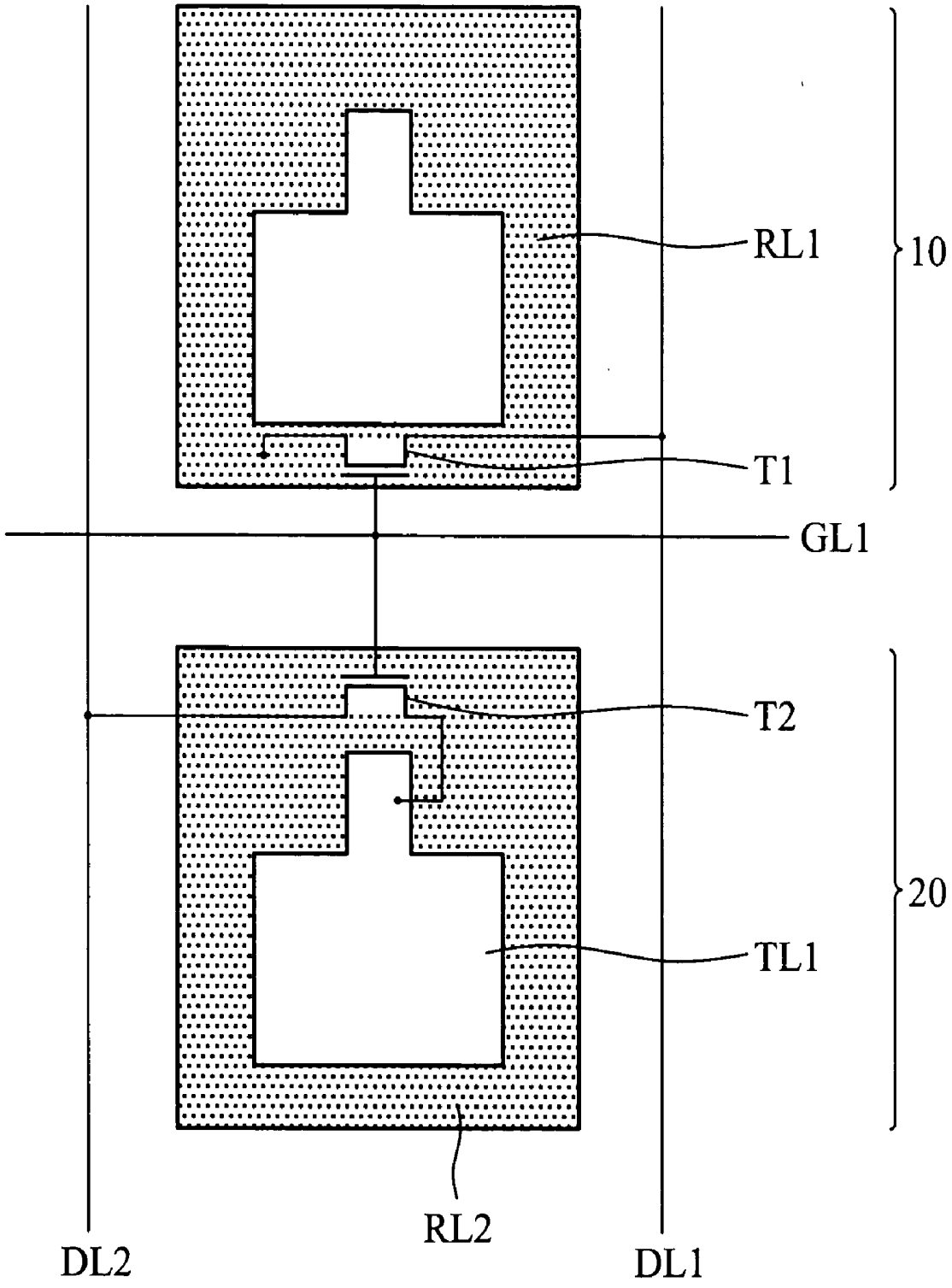


FIG. 2A

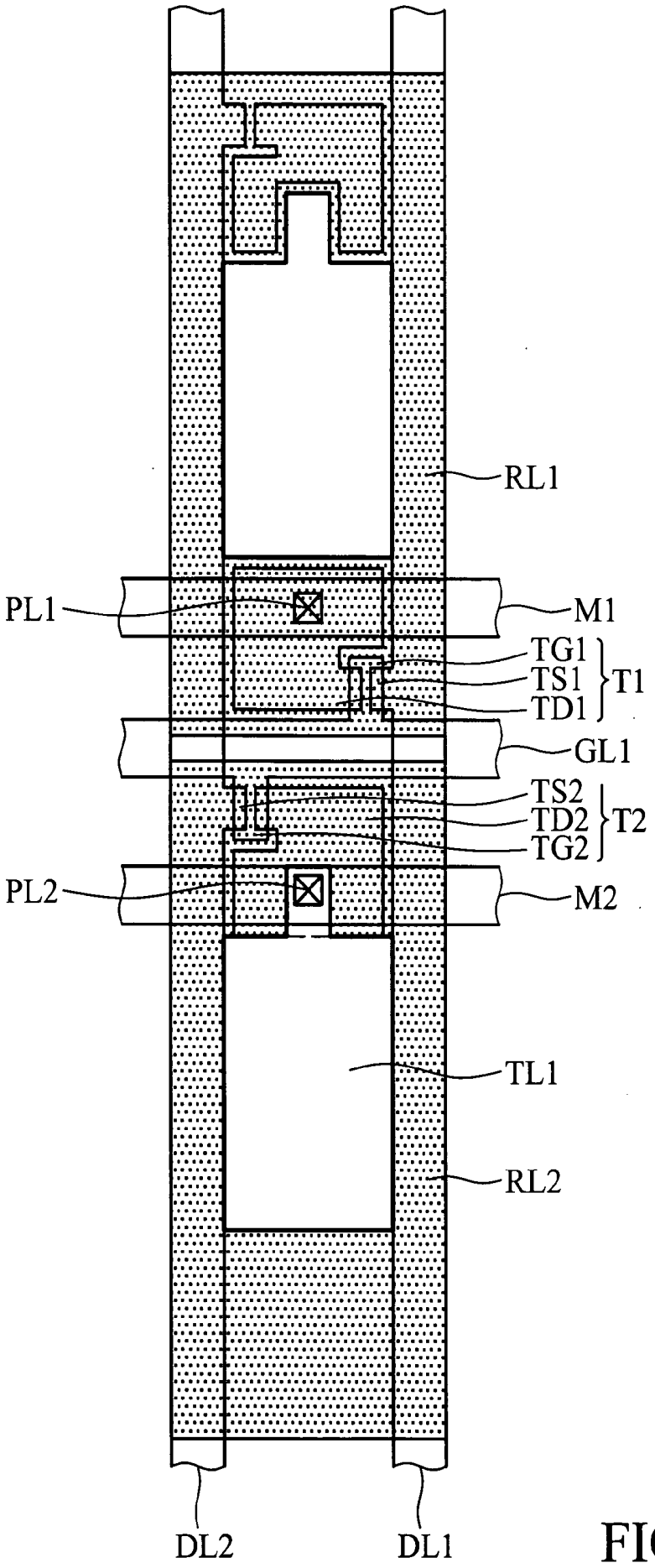

RL1
PL1
M1
TG1
TS1
T1
TD1
GL1
TS2
TD2
T2
TG2
PL2
M2
TL1
RL2
DL2
DL1

FIG. 2B

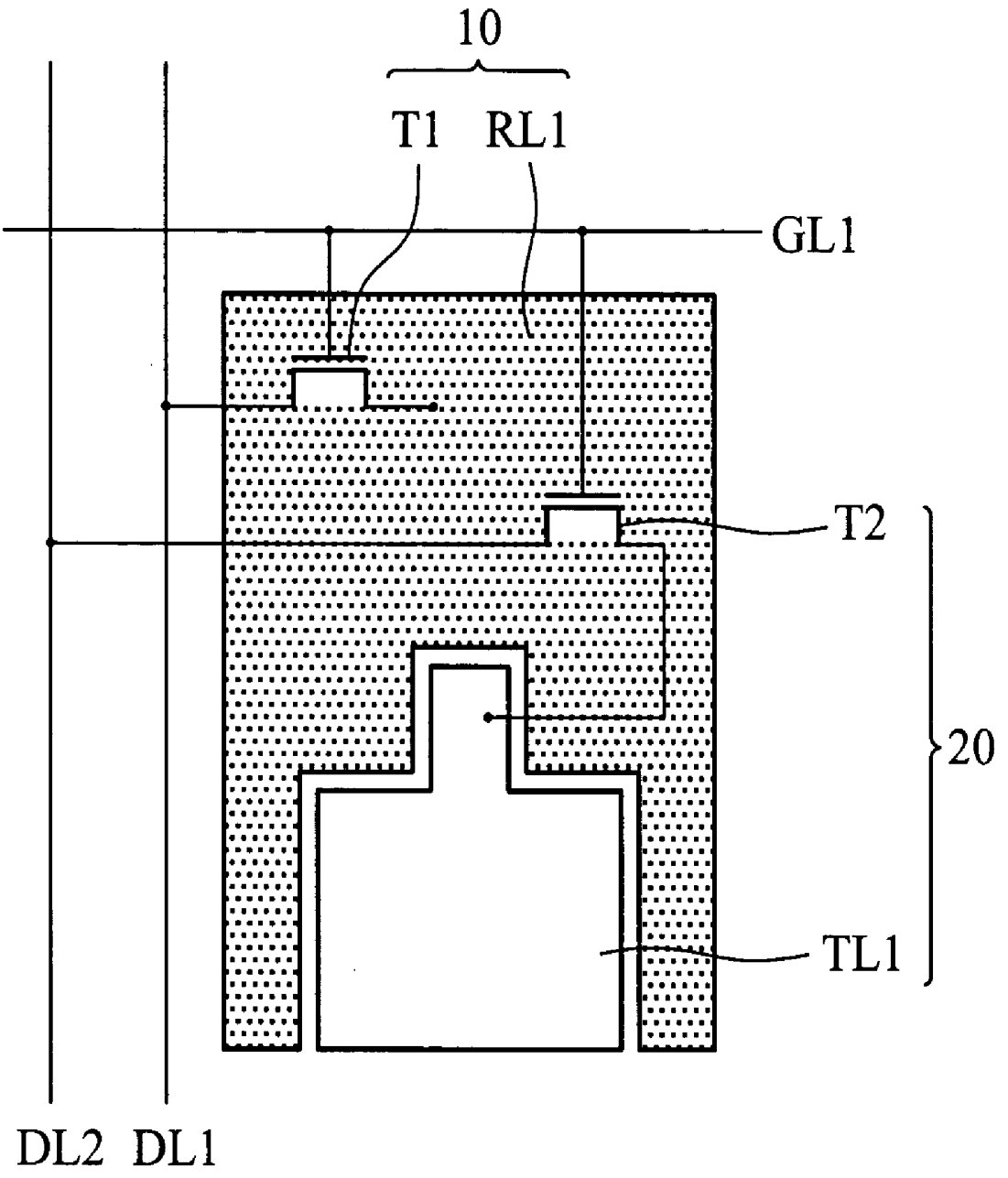


FIG. 3A

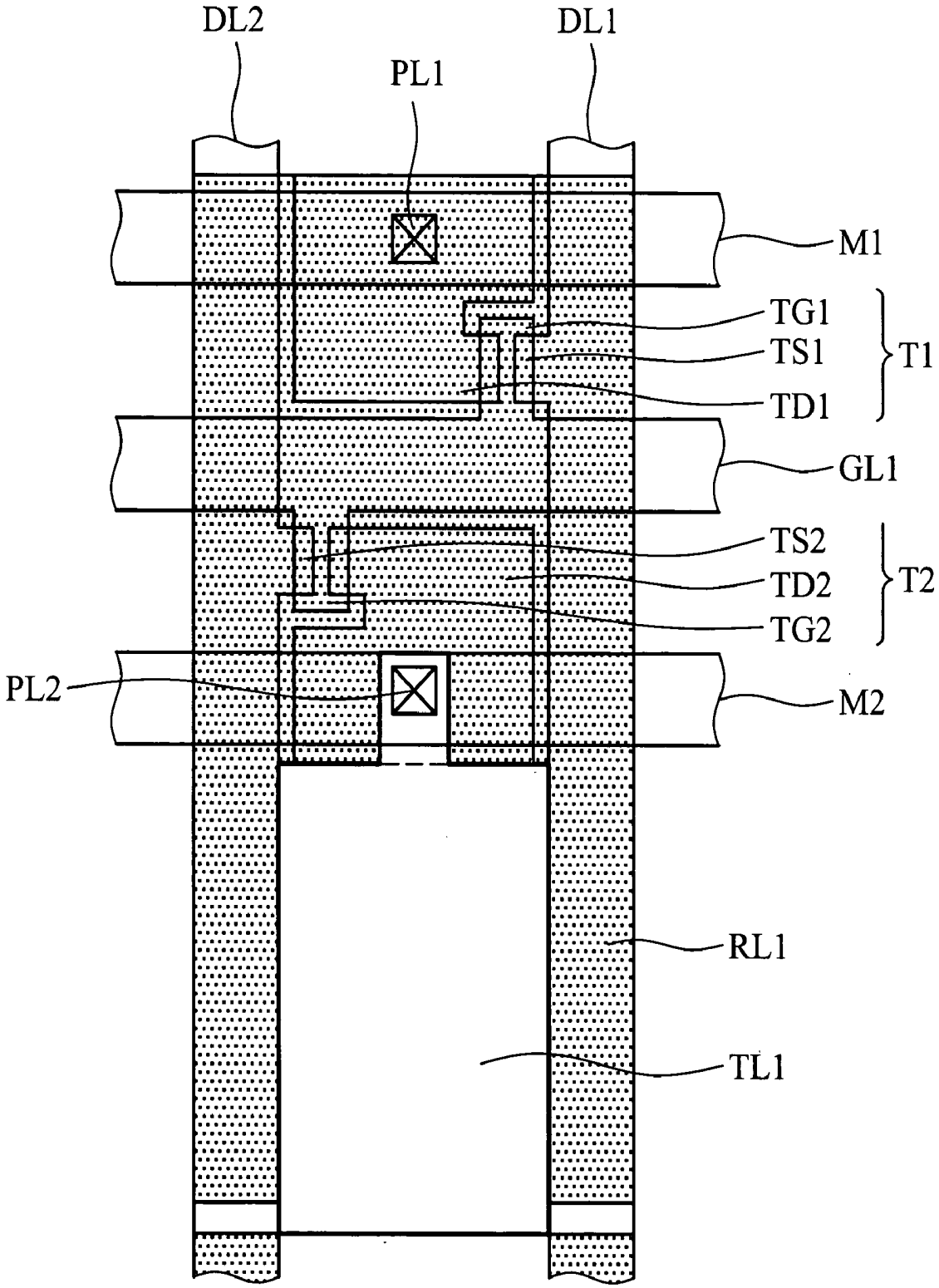


FIG. 3B

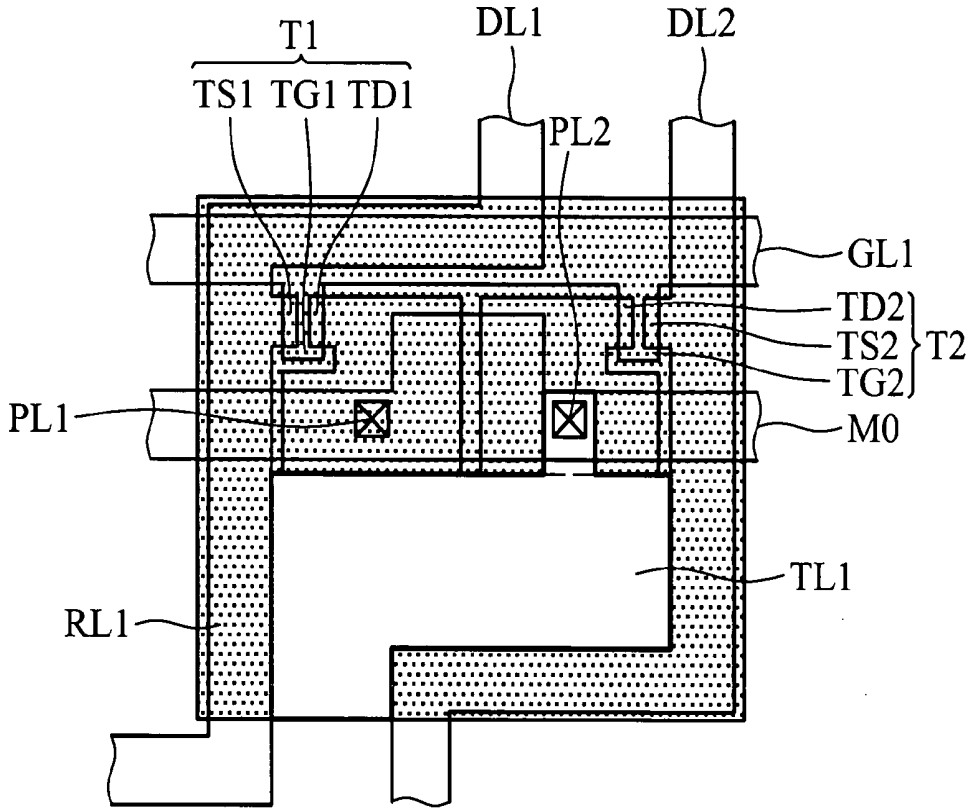

T1
TS1 TG1 TD1
DL1
DL2
PL2
GL1
TD2
TS2
T2
TG2
PL1
M0
TL1
RL1

FIG. 3C

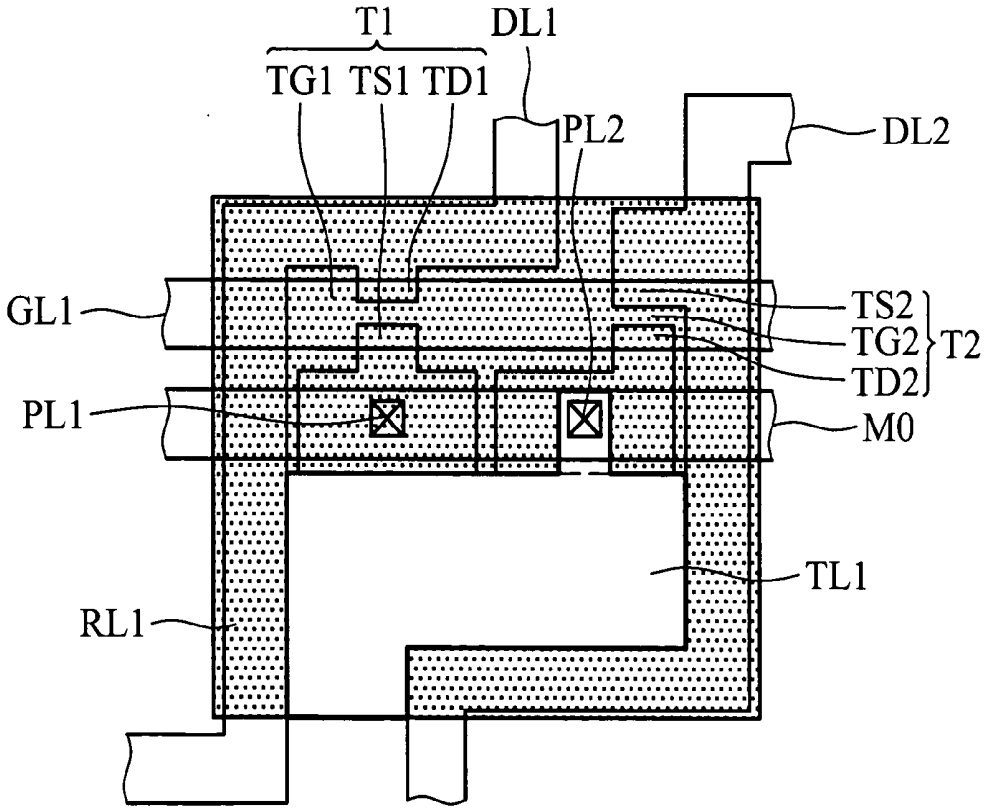

T1
TG1 TS1 TD1
DL1
PL2
DL2
GL1
TS2
TG2
T2
TD2
PL1
M0
TL1
RL1

FIG. 3D

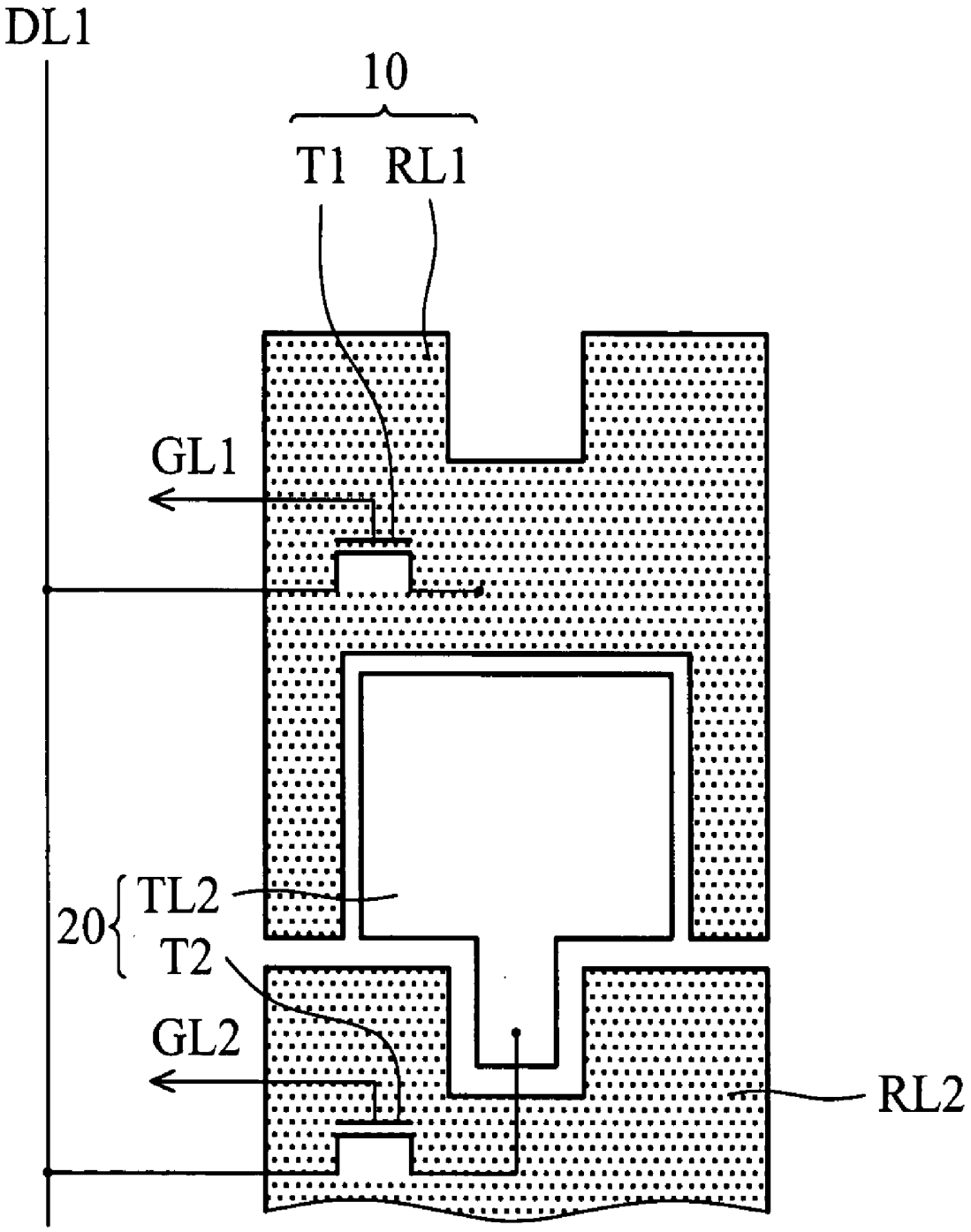


FIG. 4A

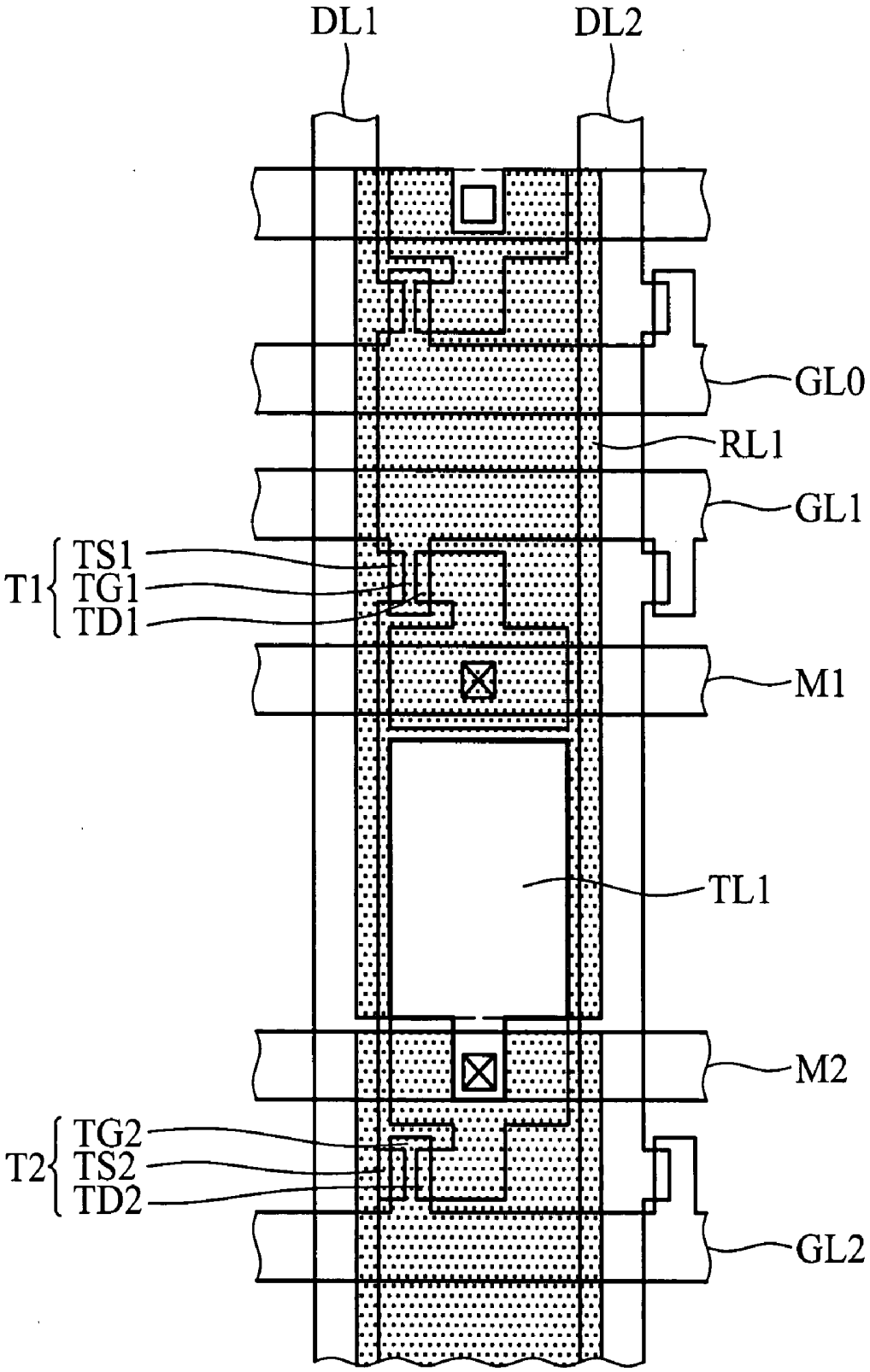


FIG. 4B

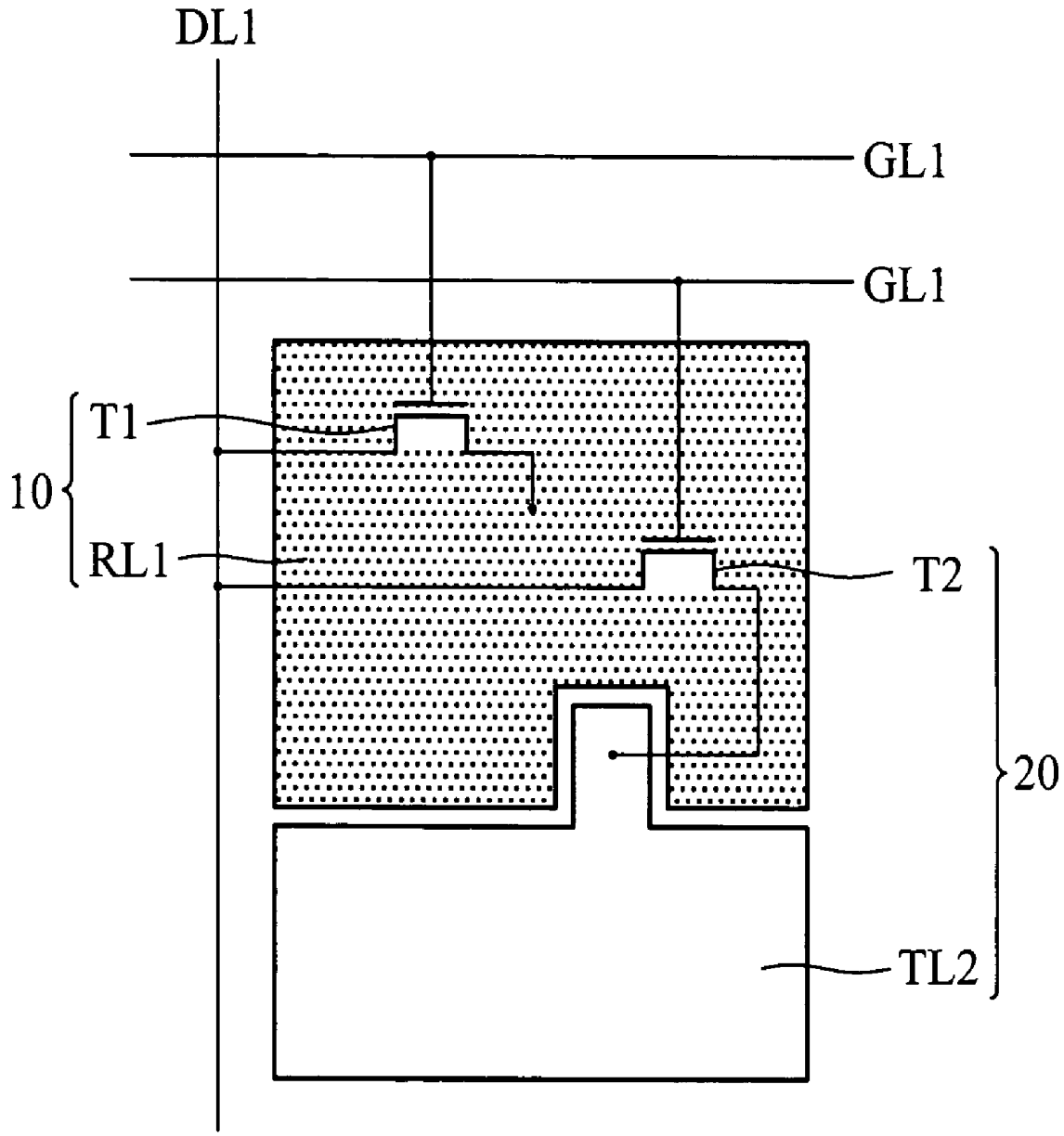


FIG. 5A

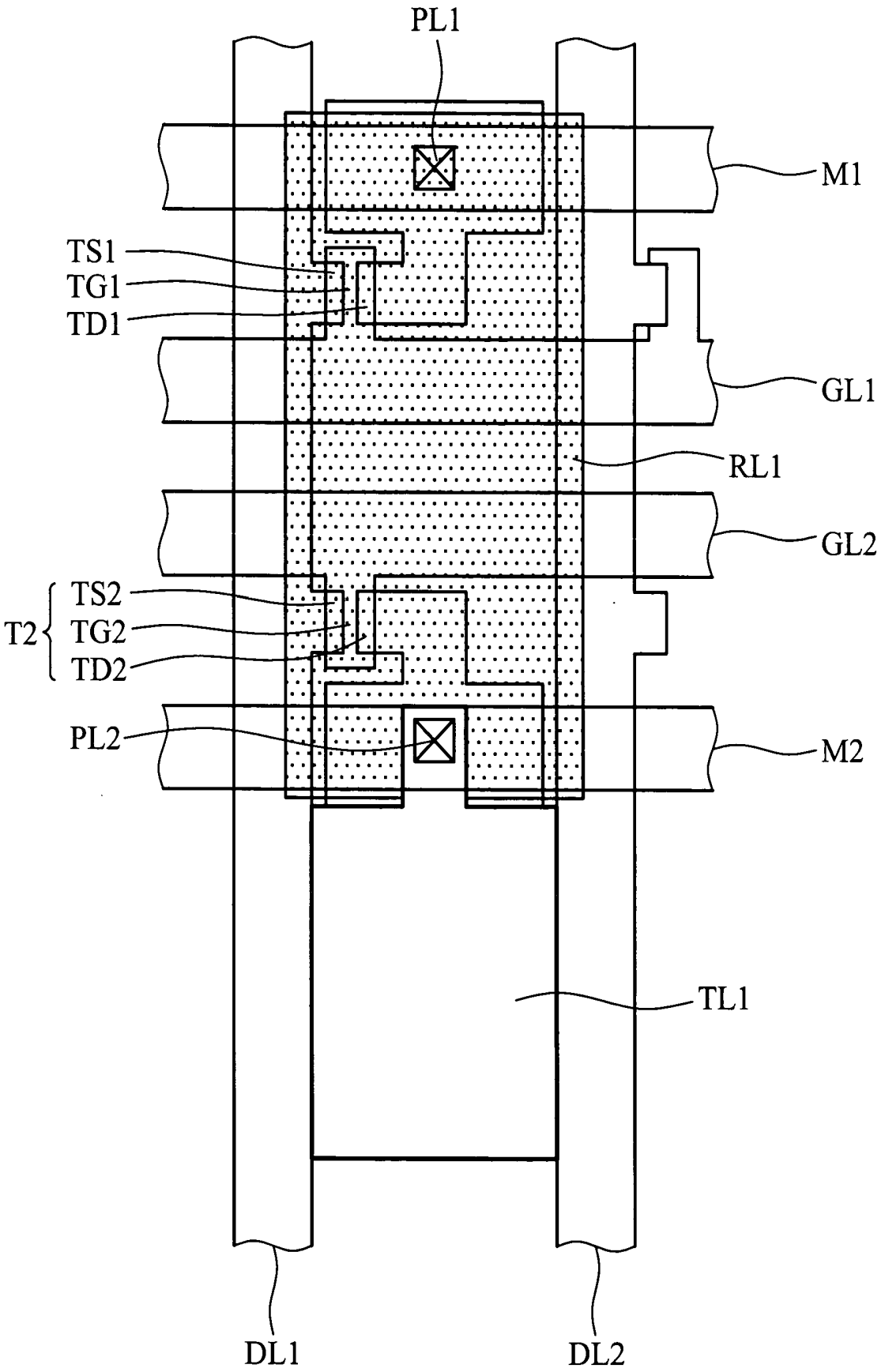


FIG. 5B

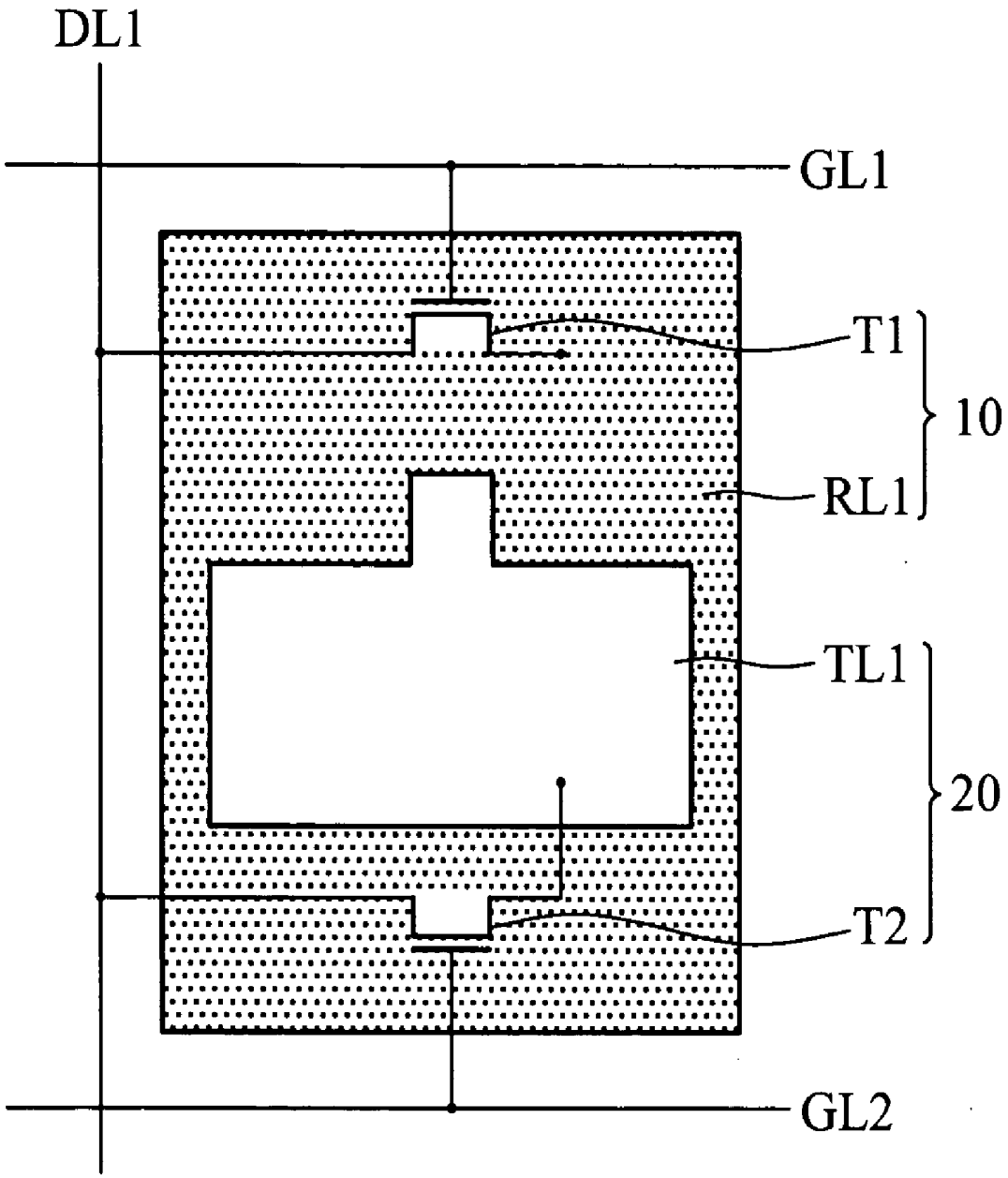


FIG. 6A

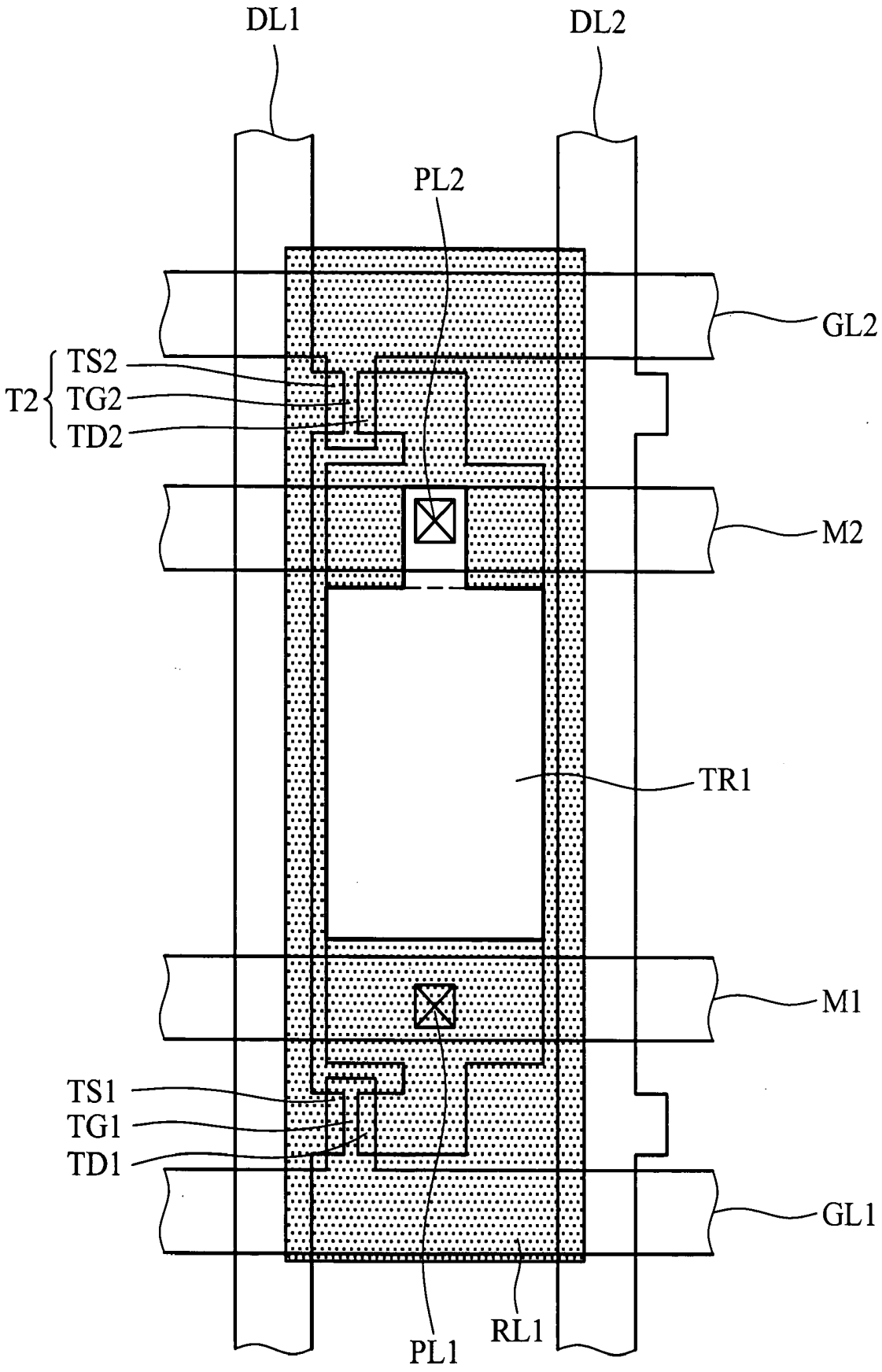


FIG. 6B

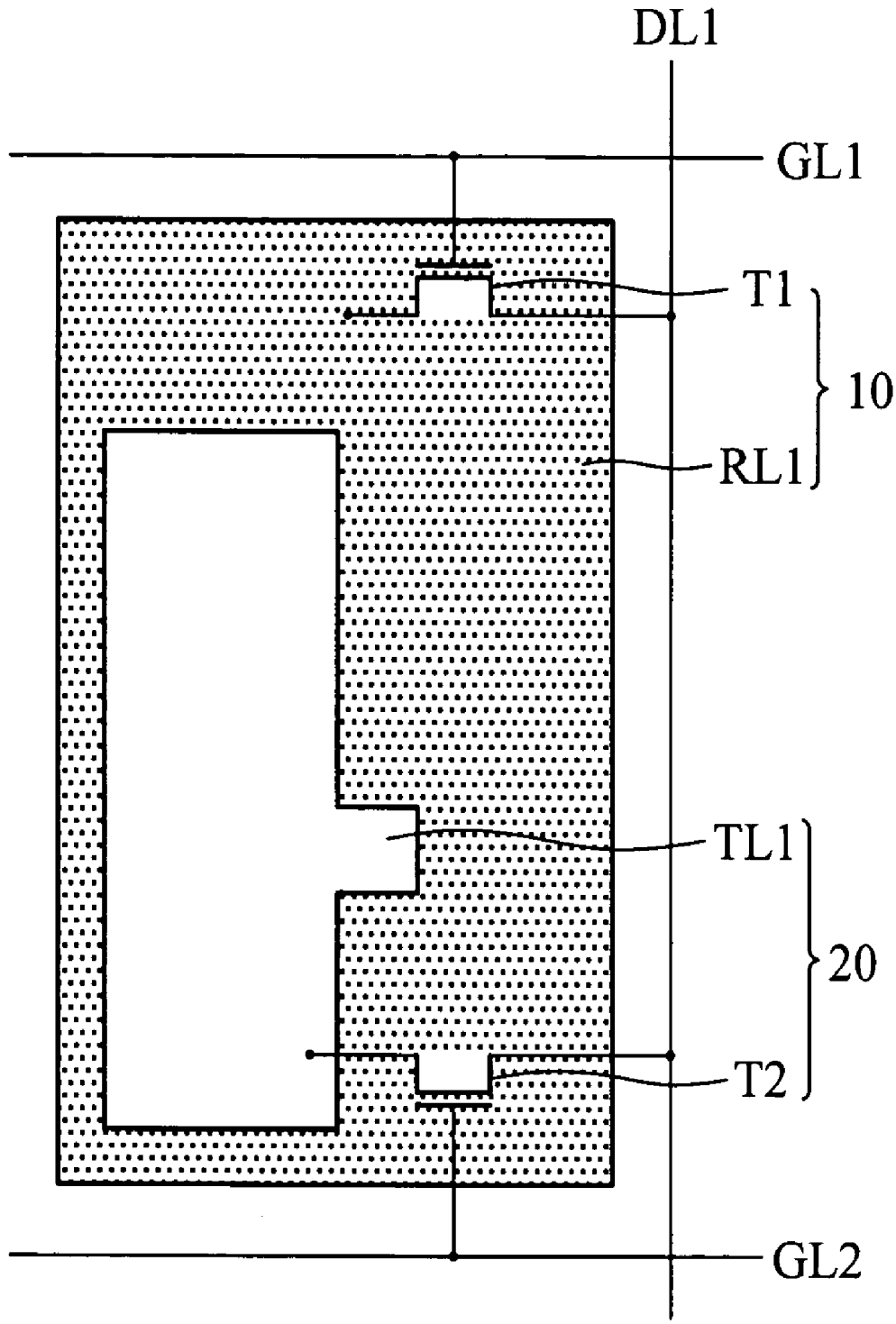


FIG. 7A

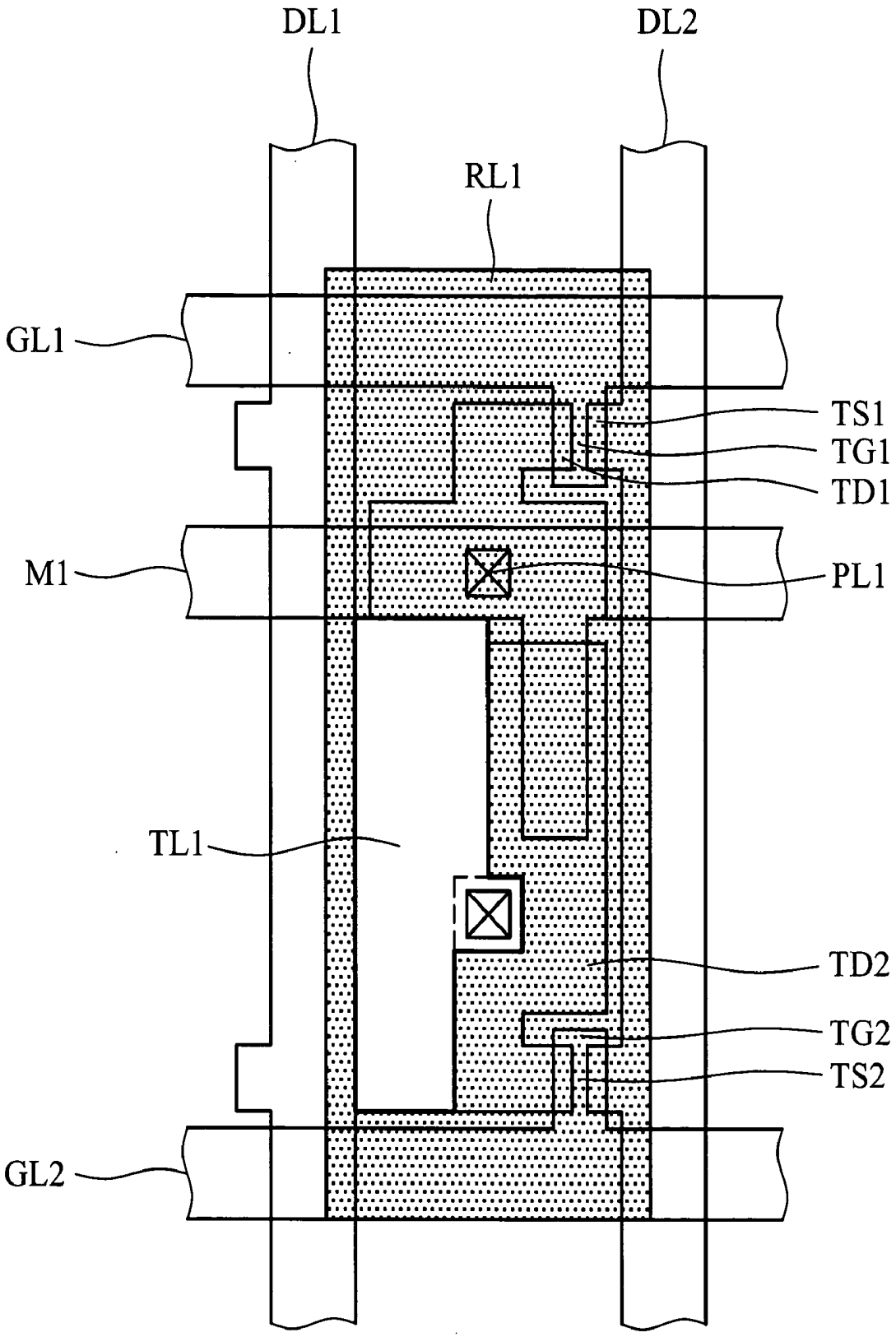


FIG. 7B

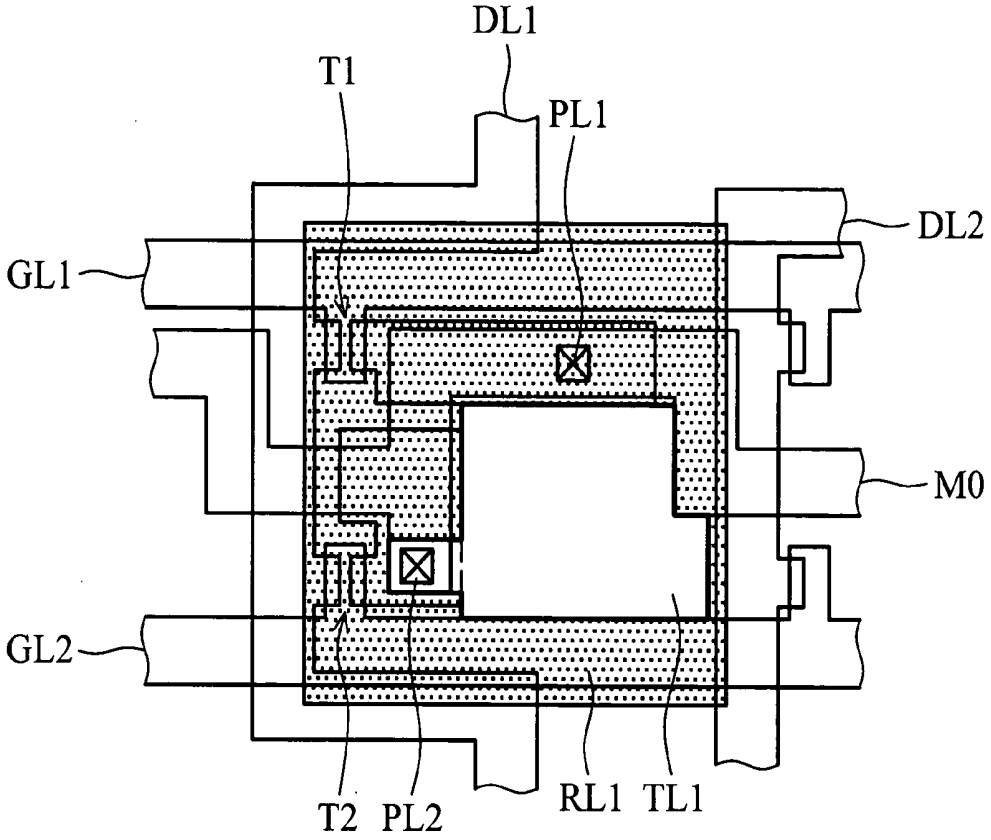

DL1
T1
PL1
DL2
GL1
M0
GL2
T2
PL2
RL1
TL1

FIG. 8A

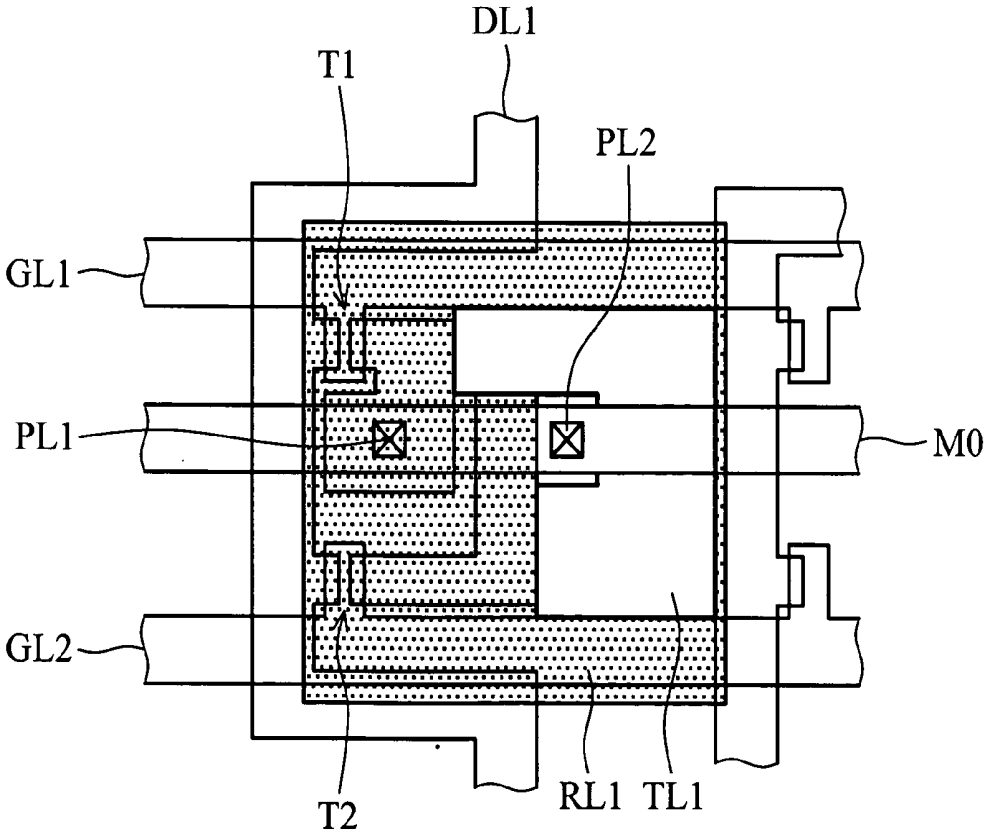

DL1
T1
PL2
GL1
PL1
M0
GL2
T2
RL1
TL1

FIG. 8B

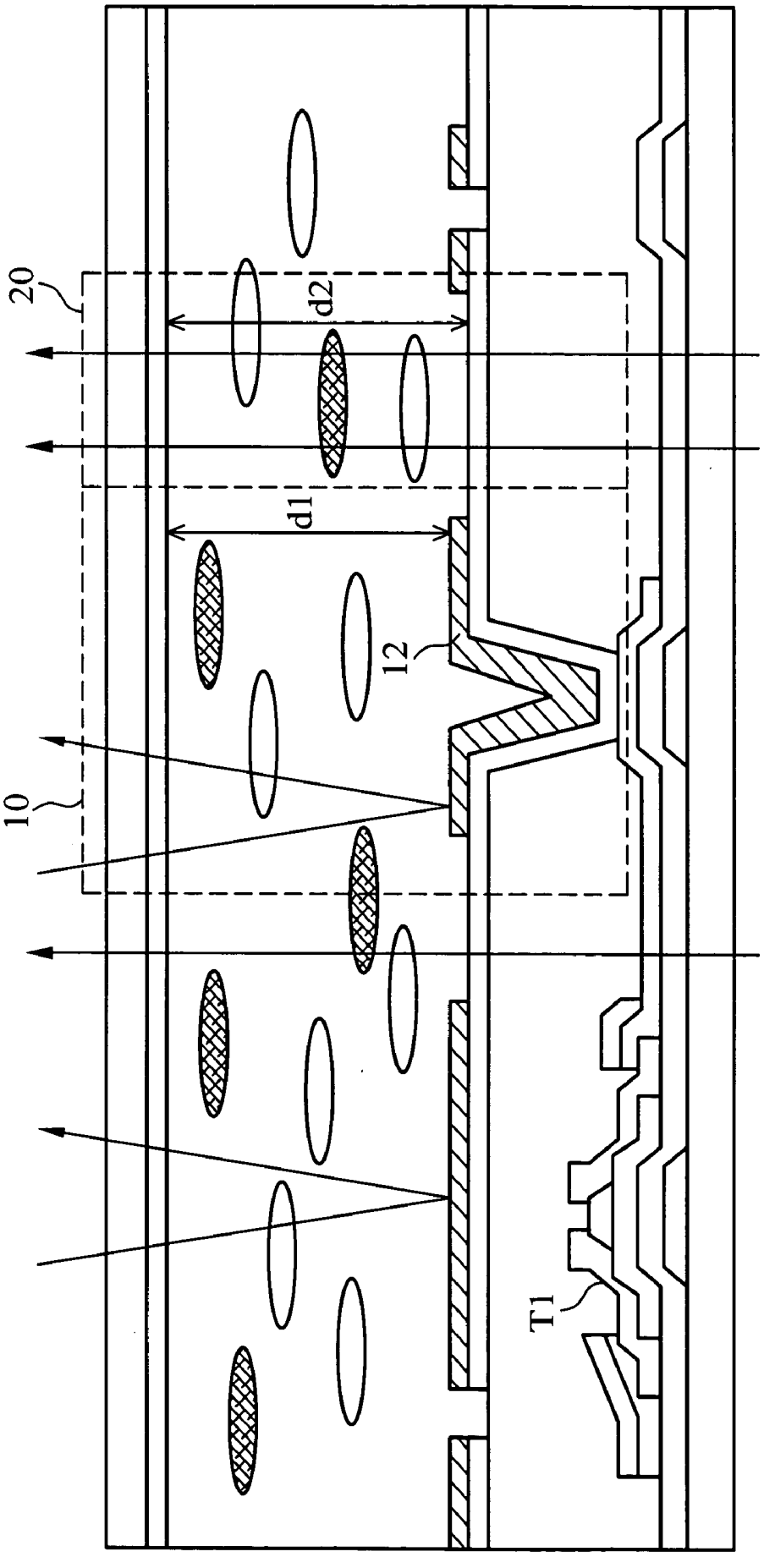


FIG. 9A

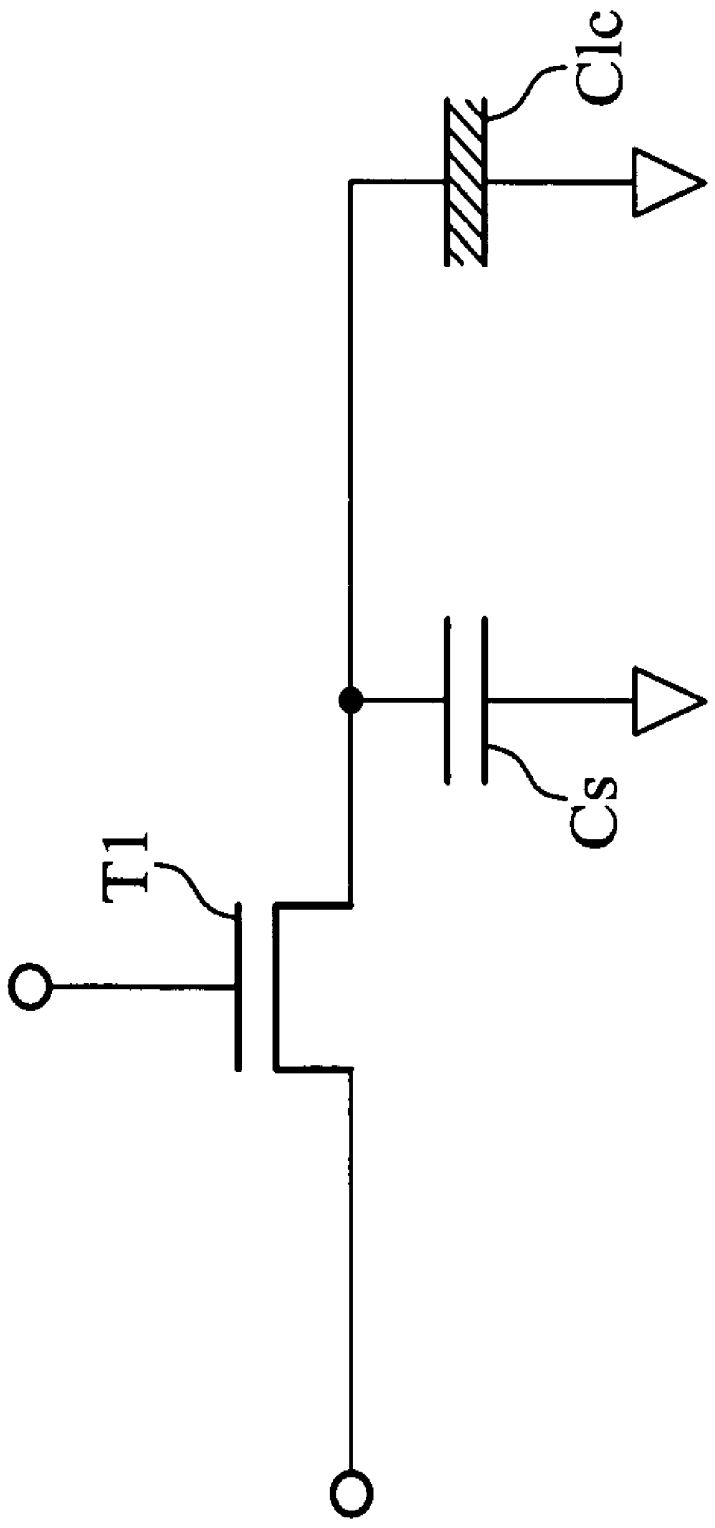


FIG. 9B

PIXEL STRUCTURE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a pixel structure, and more particularly to a pixel structure of a transflective liquid crystal display (LCD).

[0003] 2. Description of the Related Art

[0004] A pixel structure of a conventional transflective LCD has a reflective cell and a transmission cell. Unavoidably, the reflective cell has nearly double the phase difference of the transmission cell. Reduction of cell gap of the reflective cell to approach that of the transmission cell has been adopted in the past to address this issue. **FIG. 9A** shows a perspective diagram of a pixel structure of a conventional transflective LCD. The pixel structure includes a reflective cell **10** and a transmission cell **20**. The reflective cell **10** has a reflective film **12** and a cell gap d**1**. The transmission cell **20** has a cell gap d**2**.

[0005] An equivalent circuit is shown in **FIG. 9B**. The reflective cell **10** and transmission cell **20** are both coupled to a storage capacitor Cs and a TFT (thin-film-transistor) transistor T**1**. Thus, only one driving voltage can be supplied. The anti-inversion approach provides the cell gaps d**1** and d**2** with the same phase difference. The cell gaps d**1** and d**2** must be optimized to fit the LCD's operating mode, an approach that is difficult to adjust.

SUMMARY OF THE INVENTION

[0006] The present invention is directed to pixel structure with exact reflection and transmission of transflective LCD.

[0007] Accordingly, the present invention provides a pixel structure of transflective LCD disposed between a first data line and a second data line. The pixel structure comprises a reflective cell having a first transistor and a first reflective electrode, and a transmission cell having a second transistor and a transparent electrode. The first transistor comprises a gate coupled to a scan line, a source coupled to the first data line, and a drain coupled to the first reflective electrode, wherein the first transistor is covered by the first reflective electrode. The second transistor comprises a gate coupled to the scan line, a source coupled to the second data line, and a drain coupled to the transparent electrode, wherein the second transistor is covered by a second reflective electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a better understanding of the present invention, reference is made to a detailed description to be read in conjunction with the accompanying drawings, in which:

[0009] **FIG. 1** is an equivalent circuit diagram showing the pixel structure of the present invention;

[0010] **FIG. 2A** is a schematic diagram showing the pixel structure of the present invention;

[0011] **FIG. 2B** is a layout of **FIG. 2A**;

[0012] **FIG. 3A** is a schematic diagram showing another pixel structure of the present invention;

[0013] **FIG. 3B** is a layout of **FIG. 3A**;

[0014] **FIG. 3C** shows another configuration of **FIG. 3A**;

[0015] **FIG. 3D** shows another configuration of **FIG. 3A**;

[0016] **FIG. 4A** is a schematic diagram showing another pixel structure of the present invention;

[0017] **FIG. 4B** is a layout of **FIG. 4A**;

[0018] **FIG. 5A** is a schematic diagram showing another pixel structure of the present invention;

[0019] **FIG. 5B** is a layout of **FIG. 5A**;

[0020] **FIG. 6A** is a schematic diagram showing another pixel structure of the present invention;

[0021] **FIG. 6B** is a layout of **FIG. 6A**;

[0022] **FIG. 7A** is a schematic diagram showing another pixel structure of the present invention;

[0023] **FIG. 7B** is a layout of **FIG. 7A**;

[0024] **FIG. 8A** shows another configuration of **FIG. 6A**;

[0025] **FIG. 8B** shows another configuration of **FIG. 6A**;

[0026] **FIG. 9A** is a cross-section of a conventional pixel structure;

[0027] **FIG. 9B** is an equivalent circuit diagram showing the conventional pixel structure.

DETAILED DESCRIPTION OF THE INVENTION

[0028] **FIG. 1** is an equivalent circuit diagram showing the pixel structure of the present invention. The pixel structure comprises thin film transistors T**1** and T**2** and storage capacitors Cs**1** and Cs**2**. The thin film transistors T**1** and T**2** control drive voltages of a reflective cell **10** and a transmission cell **20** respectively. The phase differences of the reflective cell **10** and transmission cell **20** are normalized by adjusting the gamma correction curves but cell gaps, and reflection and transmission of the LCD are exact.

First Embodiment

[0029] **FIG. 2A** is a schematic diagram showing the pixel structure of the present invention, and **FIG. 2B** is a layout of **FIG. 2A**. The pixel structure having a reflective cell **10** and a transmission cell **20** is disposed between a first data line DL**1** and a second data line DL**2**, the reflective cell **10** comprises a transistor T**1** and a reflective electrode RL**1**, and the transmission cell **20** comprises a transistor T**2** and a transparent electrode TL**1**.

[0030] A projection of the first data line DL**1** acts as a source TS**1** of the transistor T**1**. A drain TD**1** of the transistor T**1** is coupled to the reflective electrode RL**1** by a plug PL**1**. A projection of the data line DL**2** acts as a source TS**2** of the transistor T**2**. A drain of the transistor T**2** is coupled to the transparent electrode TL**1** by a plug PL**2**. Two projections of a scan line act as gates TG**1** and TG**2** of the transistors T**1** and T**2** respectively.

[0031] The transistor T**1** is covered by the reflective electrode RL**1**, and the transistor T**2** is covered by a reflective electrode RL**2** of another pixel structure. The transparent electrode TL**1** is on the center of the reflective electrode RL**2**. Metal layers M**1** and M**2**, acting as storage capacitors,

are disposed under the plugs PL1 and PL2 respectively. In this invention, the transparent electrode TL1 can be formed by Indium Tin Oxide (ITO).

Second Embodiment

[0032] **FIG. 3A** is a schematic diagram showing another pixel structure of the present invention, and **FIG. 3B** is a layout of **FIG. 3A**. The pixel structure having a reflective cell **10** and a transmission cell **20** is disposed between a first data line DL1 and a second data line DL2, the reflective cell **10** having a transistor T1 and a reflective electrode RL1, and the transmission cell **20** comprises a transistor T2 and a transparent electrode TL1.

[0033] The first data line DL1 has a projection acting as a source TS1 of the transistor T1. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the data line DL2 acts as a source TS2 of the transistor T2. A drain of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2. Two projections of a scan line act as gates TG1 and TG2 of the transistors T1 and T2 respectively.

[0034] Transistors T1 and T2 are covered by the reflective electrode RL1, and disposed on the reverse side of the transparent electrode TL1. Metal layers M1 and M2, acting as storage capacitors, are disposed under the plug PL1 and PL2 respectively.

[0035] **FIGS. 3C and 3D** show other configurations of the embodiment. The pixel structure having a reflective cell **10** and a transmission cell **20** is disposed between a first data line DL1 and a second data line DL2.

[0036] The reflective cell **10** comprises a transistor T1 and a reflective electrode RL1, and the transmission cell **20** comprises a transistor T2 and a transparent electrode TL1.

[0037] A projection of the first data line DL1 acts as a source TS1 of the transistor T1. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the data line DL2 acts as a source TS2 of the transistor T2. A drain of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2. Two projections of a scan line act as gates TG1 and TG2 of the transistors T1 and T2 respectively.

[0038] The transistor T1 and T2 are covered by the reflective electrode RL1, and disposed on the reverse side of the transparent electrode TL1. A metal layer M0 acting as a storage capacitor is disposed under the drains TD1 and TD2 of the transistors T1 and T2 respectively.

Third Embodiment

[0039] **FIG. 4A** is a schematic diagram showing another pixel structure of the present invention, and **FIG. 4B** is a layout of **FIG. 4A**. The pixel structure having a reflective cell **10** and a transmission cell **20** is disposed between a first data line DL1 and a second data line DL2, the reflective cell **10** comprises a transistor T1 and a reflective electrode RL1, and the transmission cell **20** comprises a transistor T2 and a transparent electrode TL1.

[0040] A projection of the scan line GL1 acts as a gate TG1 of the transistor T1. Two projections of the data line DL1 act as sources TS1 and TS2 of the transistors T1 and T2 respectively. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the scan line GL2 acts as a gate TG2 of the transistor T2. A drain TD2 of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2.

[0041] The reflective electrode RL1 covers the transistor T1 and a transistor of another pixel structure, and a reflective electrode RL2 of another pixel structure covers the transistor T2. The transparent electrode TL1 is disposed between the transistor T1 and T2. Metal layers M1 and M2, acting as storage capacitors, are disposed under the plugs PL1 and PL2 respectively.

Fourth Embodiment

[0042] **FIG. 5A** is a schematic diagram showing another pixel structure of the present invention, and **FIG. 5B** is a layout of **FIG. 5A**. The pixel structure having a reflective cell **10** and a transmission cell **20** is disposed between a first data line DL1 and a second data line DL2, the reflective cell **10** comprises a transistor T1 and a reflective electrode RL1, and the transmission cell **20** comprises a transistor T2 and a transparent electrode TL1.

[0043] A projection of the scan line GL1 acts as a gate TG1 of the transistor T1. Two projections of the data line DL1 act as sources TS1 and TS2 of the transistors T1 and T2 respectively. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the scan line GL2 acts as a gate TG2 of the transistor T2. A drain TD2 of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2.

[0044] The transistors T1 and T2 are covered by the reflective electrode RL1, and disposed on the reverse side of the transparent electrode TL1. Metal layers M1 and M2, acting as storage capacitors, are disposed under the plugs PL1 and PL2 respectively.

[0045] **FIGS. 6A and 6B** show other configurations of the embodiment. A pixel structure having a reflective cell **10** and a transmission cell **20** is disposed between a first data line DL1 and a second data line DL2. The transistors T1 and T2 are covered by a reflective electrode RL1, and disposed on different sides under the transparent electrode.

[0046] **FIGS. 7A and 7B** show other configurations of the embodiment. A pixel structure having a reflective cell **10** and a transmission cell **20** is disposed between a first data line DL1 and a second data line DL2. The transistors T1 and T2 are covered by a reflective electrode RL1, disposed around a transparent electrode TL1. A metal layer M1 is disposed under a drain TD1 of the transistor T1, and extends to an underside of a drain TD2 of the transistor T2.

[0047] **FIG. 8A** shows another configuration of the embodiment. A pixel structure having a reflective cell and a transmission cell is disposed between data lines DL1 and DL2, wherein the data lines are bent. The transistors T1 and T2 are covered by a reflective electrode RL1. The reflective electrode RL1 is disposed around a transparent electrode TL1. A bent metal layer M0 is disposed under the drains TD1 and TD2 of the transistors T1 and T2.

[0048] **FIG. 8B** shows another configuration of the embodiment. A pixel structure having a reflective cell and a transmission cell is disposed between data lines DL1 and DL2, wherein the data lines are bent. The transistors T1 and

T2 are covered by a reflective electrode RL1. The reflective electrode RL1 is disposed around a transparent electrode TL1. A metal layer M0 is disposed under the drains TD1 and TD2 of the transistors T1 and T2.

[0049] In the present invention, the transistors T1 and T2 of the pixel structure control the drive voltages of the reflective cell and the transmission cell respectively, the reflection and transmission of the pixel structure are exact, such that the cell gaps do not have to adjust.

[0050] While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A pixel structure of transflective LCD disposed between a first data line and a second data line, comprising:

a reflective cell comprising a first transistor and a first reflective electrode, wherein the first transistor comprises a gate coupled to a scan line, a source coupled to the first data line, and a drain coupled to the first reflective electrode, and the first transistor is covered by the first reflective electrode; and

a transmission cell comprising a second transistor and a transparent electrode, wherein the second transistor comprises a gate coupled to the scan line, a source coupled to the second data line, and a drain coupled to the transparent electrode, and the second transistor is covered by a second reflective electrode.

2. The pixel structure of transflective LCD of claim 1, wherein the second reflective electrode is a first reflective electrode of another pixel structure.

3. The pixel structure of transflective LCD of claim 1, wherein the drain of the first transistor is coupled to the first reflective electrode by a first plug, and the drain of the second transistor is coupled to the transmission electrode by a second plug.

4. The pixel structure of transflective LCD of claim 3, further comprising a first metal layer and a second metal layer, acting as storage capacitors, disposed under the first plug and the second plug respectively.

5. A pixel structure of transflective LCD disposed between a first data line and a second data line, comprising:

a reflective cell comprising a first transistor and a first reflective electrode, wherein the first transistor comprises a gate coupled to a scan line, a source coupled to the first data line, and a drain coupled to the first electric electrode; and

a transmission cell comprising a second transistor and a transparent electrode, wherein the second transistor comprises a gate coupled to the second line, a source coupled to the second data line, and a drain coupled to the transparent electrode, and the first transistor and the second transistor are covered by the first reflective electrode.

6. The pixel structure of transflective LCD of claim 5, wherein the drain of the first transistor is coupled to the first reflective electrode by a first plug, and the drain of the second transistor is coupled to the transparent by a second plug.

7. The pixel structure of transflective LCD of claim 6, further comprising a first metal layer and a second metal layer, acting as storage capacitors, disposed under the first plug and the second plug respectively.

8. The pixel structure of transflective LCD of claim 5, wherein the first data line and the second data line are bent, the drain of the first transistor is coupled to the first reflective electrode by a first plug, and the drain of the second transistor is coupled to the transparent by a second plug.

9. The pixel structure of transflective LCD of claim 8, further comprising a metal line disposed under the drains of the first and second transistor, acting as a storage capacitor.

10. The pixel structure of transflective LCD of claim 8, wherein the metal line is bent, and the metal line acting as a storage capacitor is disposed under the drains of the first and second transistor.

11. A pixel structure of transflective LCD disposed between a first data line and a second data line, comprising:

a reflective cell comprising a first transistor and a first reflective electrode, wherein the first transistor comprises a gate coupled to a first scan line, a source coupled to the first data line, and a drain coupled to the first reflective electrode, and the first transistor is covered by the first reflective electrode; and

a transmission cell comprising a second transistor and a transparent electrode, wherein the second transistor comprises a gate coupled to a second scan line, a source coupled to the first data line, and a drain coupled to the transparent electrode, and the second transistor is covered by a second reflective electrode.

12. The pixel structure of transflective LCD of claim 11, wherein the second reflective electrode is a first reflective electrode of another pixel structure.

13. The pixel structure of transflective LCD of claim 11, wherein the drain of the first transistor is coupled to the first reflective electrode by a first plug, and the drain of the second transistor is coupled to the transparent electrode by a second plug.

14. The pixel structure of transflective LCD of claim 13, further comprising a first metal layer and a second metal layer, acting as storage capacitors, disposed under the first plug and the second plug respectively.

15. A pixel structure of transflective LCD disposed between a first data line and a second data line, comprising:

a reflective cell comprising a first transistor and a first reflective electrode, wherein the first transistor comprises a gate coupled to a scan line, a source coupled to the first data line, and a drain coupled to the first reflective electrode; and

a transmission cell comprising a second transistor and a transparent electrode, wherein the second transistor comprises agate coupled to a second scan line, a source coupled to the first data line, and a drain coupled to the transparent electrode, and the first and second transistor are covered by the first reflective electrode.

16. The pixel structure of transflective LCD of claim 15, wherein the drain of the first transistor is coupled to the first reflective electrode by a first plug, and the second transistor is coupled to the transparent electrode by a second plug.

17. The pixel structure of transflective LCD of claim 16, further comprising a first metal layer and a second metal layer, acting as storage capacitors, disposed under the first plug and the second plug respectively.

18. The pixel structure of transflective LCD of claim 15, wherein the first transistor and the second transistor are disposed on different sides under the transparent electrode.

19. The pixel structure of transflective LCD of claim 16, further comprising a first metal layer acting as a storage capacitor disposed under the first plug, and extending to an underside of the drain of the second transistor.

* * * * *

专利名称(译)	像素结构		
公开(公告)号	US20050018113A1	公开(公告)日	2005-01-27
申请号	US10/761154	申请日	2004-01-20
[标]申请(专利权)人(译)	沉YUH REN 陈清锴		
申请(专利权)人(译)	沈yuh-ren 陈清锴		
当前申请(专利权)人(译)	群创光电		
[标]发明人	SHEN YUH REN CHEN CHING YIH		
发明人	SHEN, YUH-REN CHEN, CHING-YIH		
IPC分类号	G02F1/1368 G02F1/1335 G02F1/1343 G02F1/1362		
CPC分类号	G02F1/133555 G02F2001/134345 G02F1/13624		
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摘要(译)

透射反射型LCD的像素结构设置在第一数据线和第二数据线之间。像素结构包括反射单元和透射单元。晶体管包括耦合到扫描线的栅极，耦合到第一数据线的源极，以及耦合到第一反射电极的漏极。第一晶体管被第一反射电极覆盖。传输单元包括第二晶体管和透明电极。第二晶体管包括耦合到扫描线的栅极，耦合到第二数据线的源极，以及耦合到透明电极的漏极。第二晶体管被第二反射电极覆盖。