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Komatsu(10) **Pub. No.: US 2002/0067455 A1**(43) **Pub. Date: Jun. 6, 2002**(54) **IN-PLANE SWITCHING MODE LIQUID
CRYSTAL DISPLAY DEVICE**

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Washington, DC 20004 (US)(21) Appl. No.: **10/015,765**(22) Filed: **Dec. 17, 2001****Related U.S. Application Data**(63) Continuation of application No. 09/116,707, filed on
Jul. 17, 1998, now patented.(30) **Foreign Application Priority Data**

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Publication Classification(51) **Int. Cl.⁷** **G02F 1/1343**(52) **U.S. Cl.** **349/141; 349/38**(57) **ABSTRACT**

An in-plane switching mode liquid crystal display device is disclosed which comprises first and second substrates, a plurality of gate and data bus lines formed on said first substrate to define a plurality of pixel regions, a common bus line aligned in each pixel regions of the first substrate, a thin film transistor(TFT) formed at each pixel regions of the first substrate, a data electrode which is formed on a gate insulator of the TFT and has a portion overlapping the common bus line for forming a first storage capacitor, a passivation layer formed over the data electrode and the TFT, a common electrode which is formed on the passivation layer so as to overlap the gate and data bus lines and has a portion overlapping said data electrode for forming a second storage capacitor, and a liquid crystal layer formed between the first and second substrates.

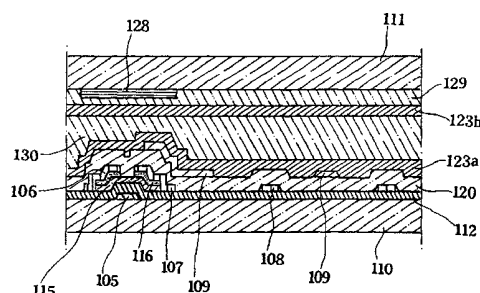
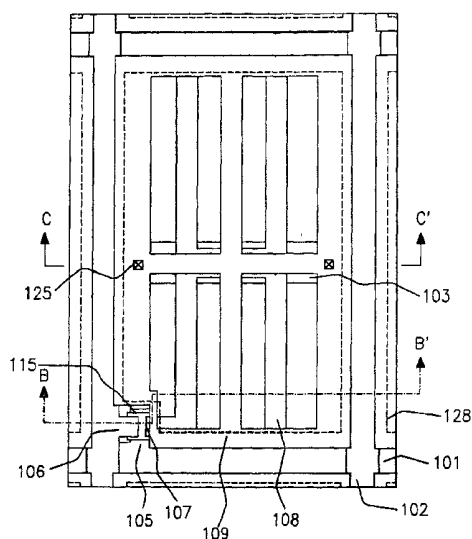


FIG.1a
PRIOR ART

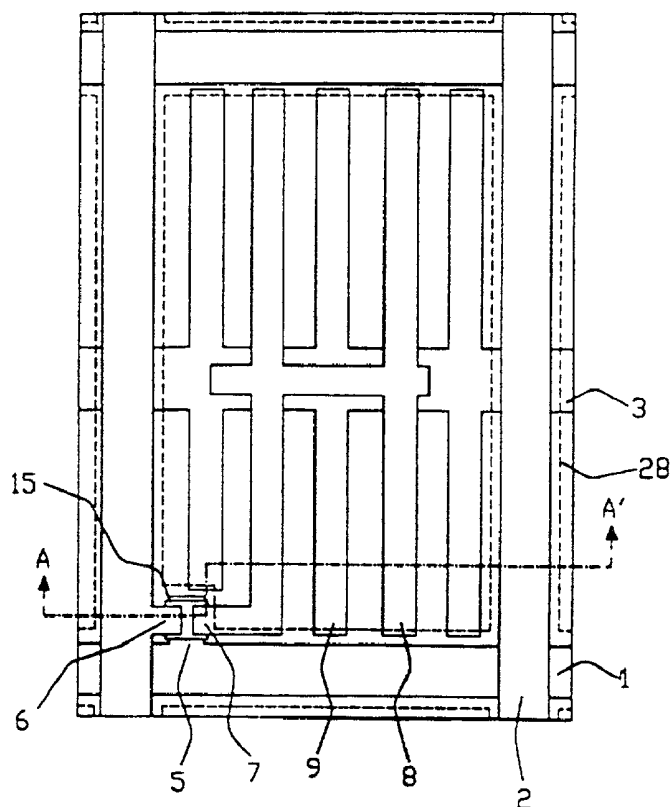


FIG.1b
PRIOR ART

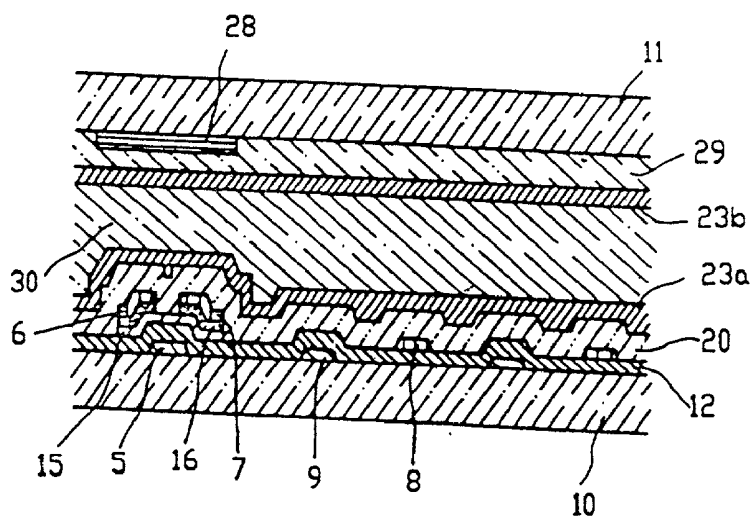


FIG. 2a

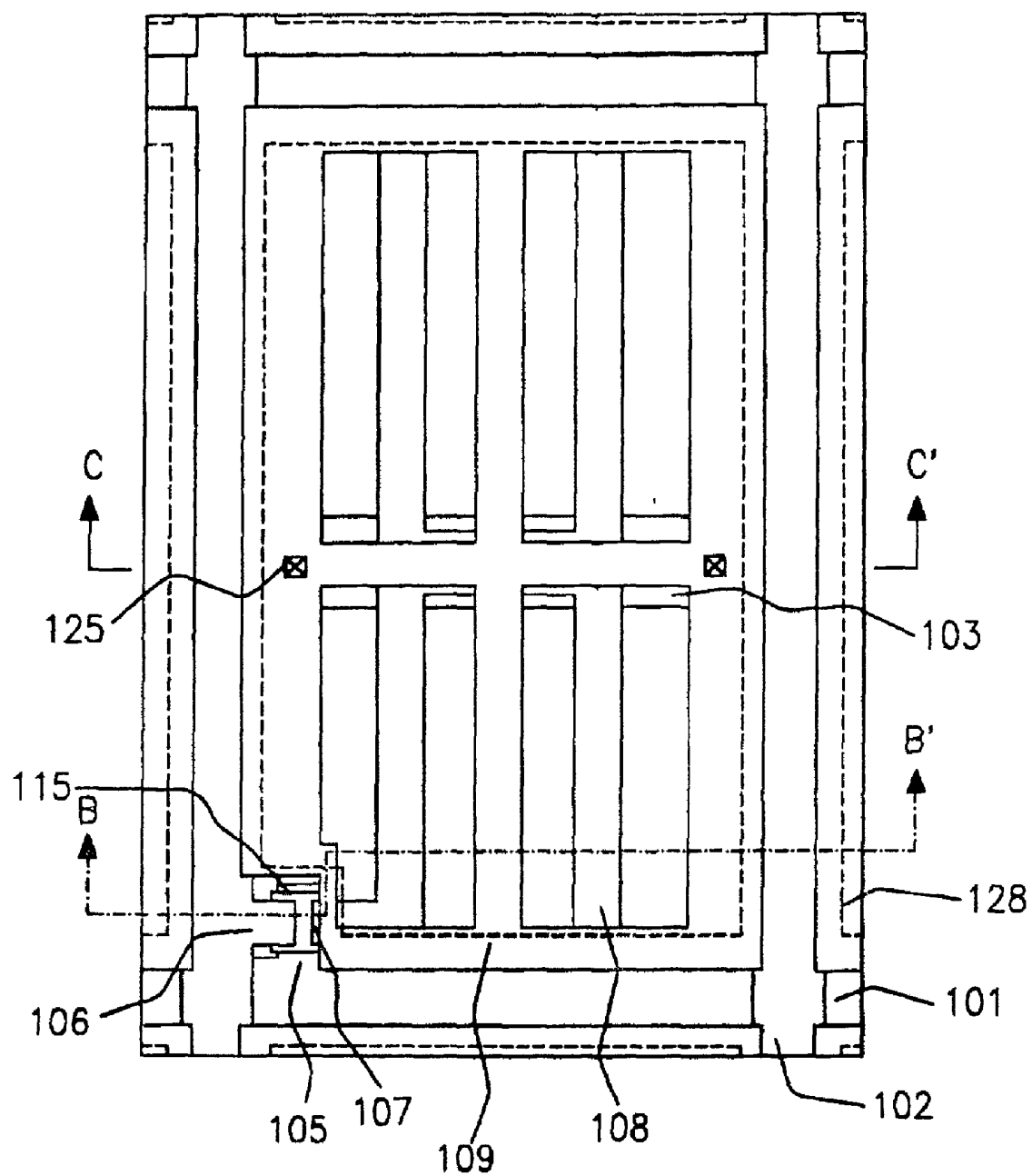


FIG.2b

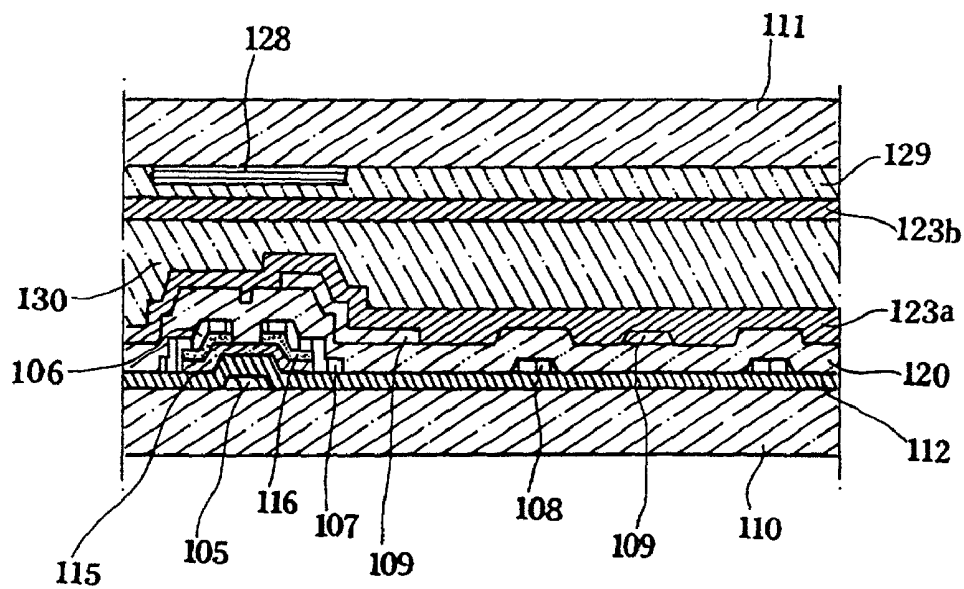


FIG.2c

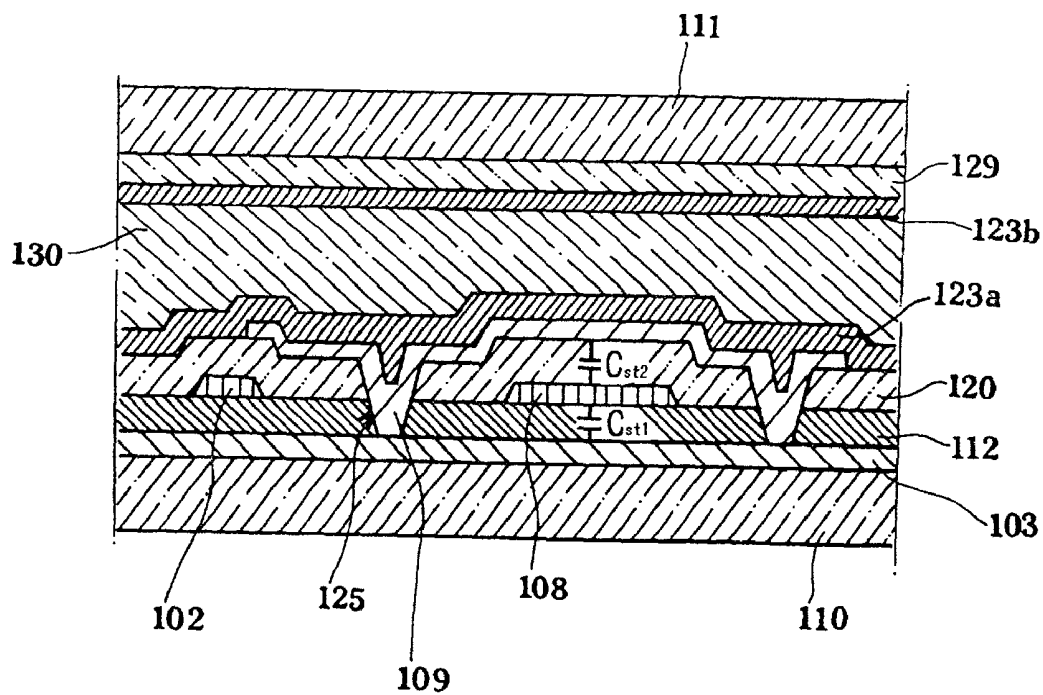


FIG.3

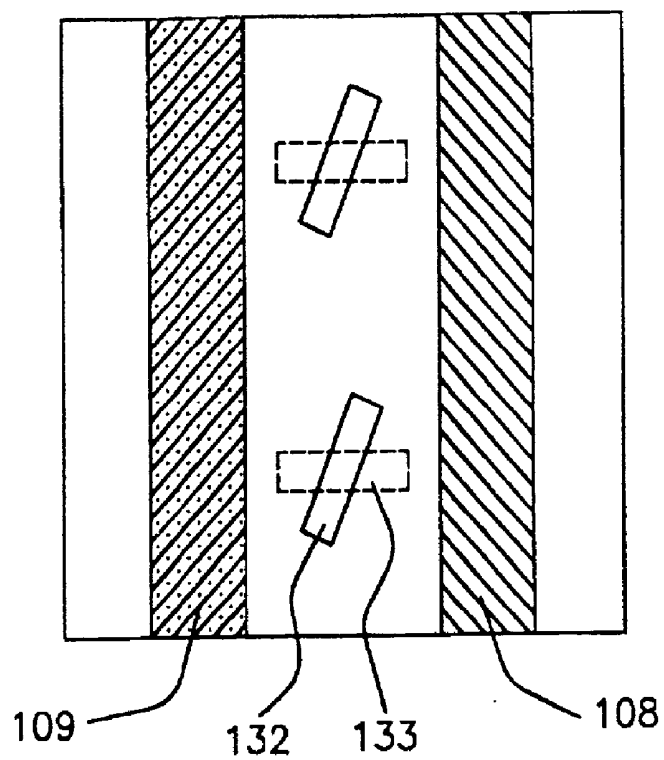


FIG.4

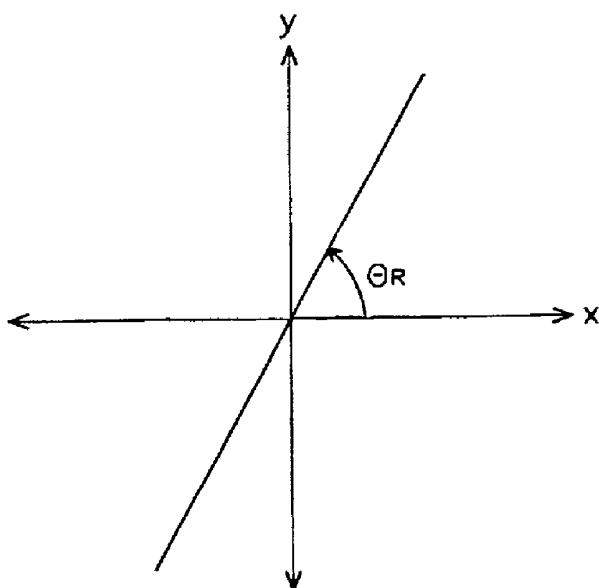


FIG.5

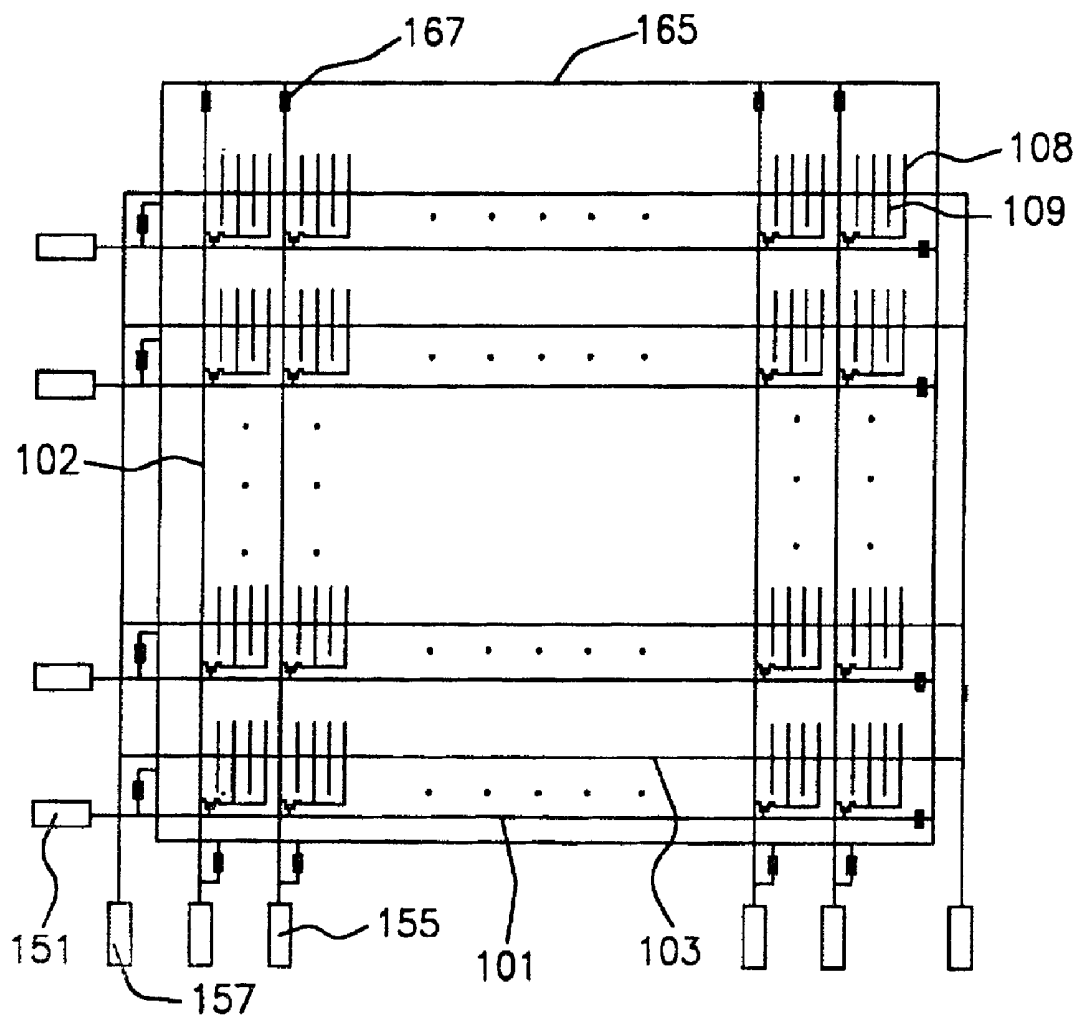


FIG.6a

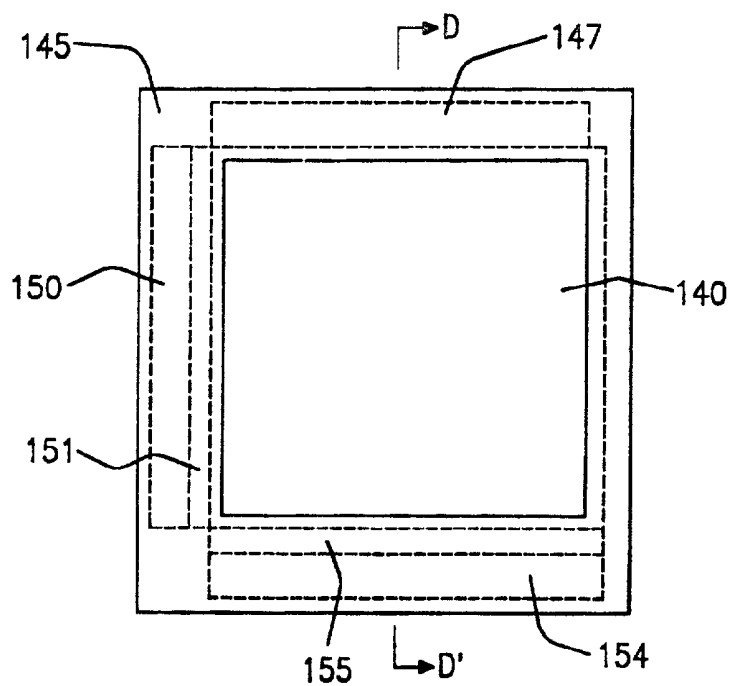
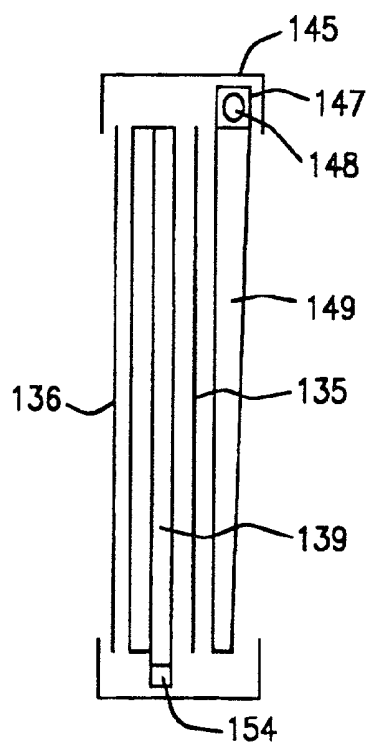


FIG.6b



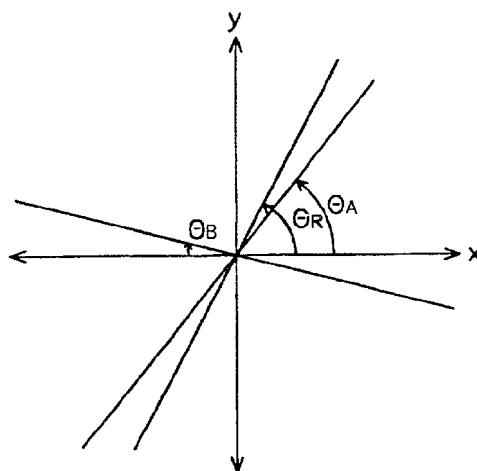


FIG.9a

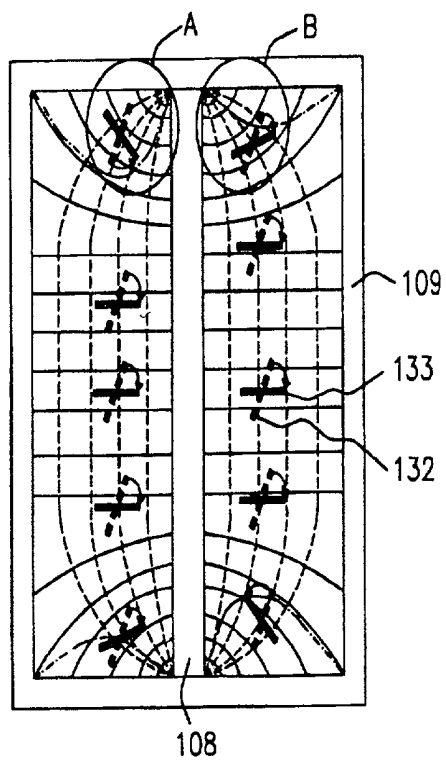
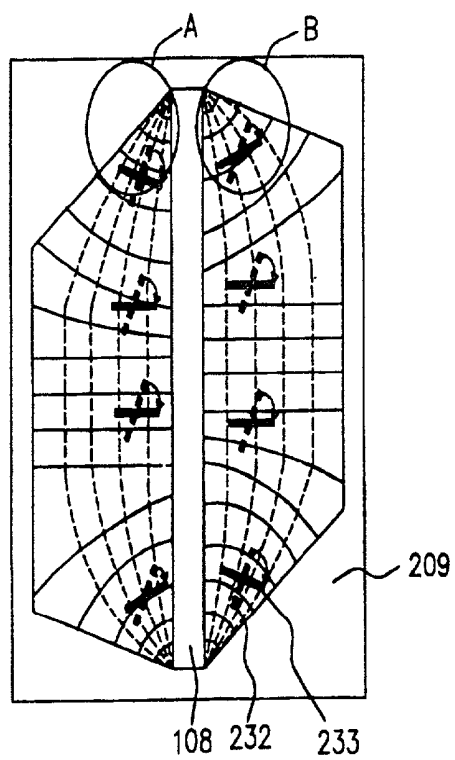
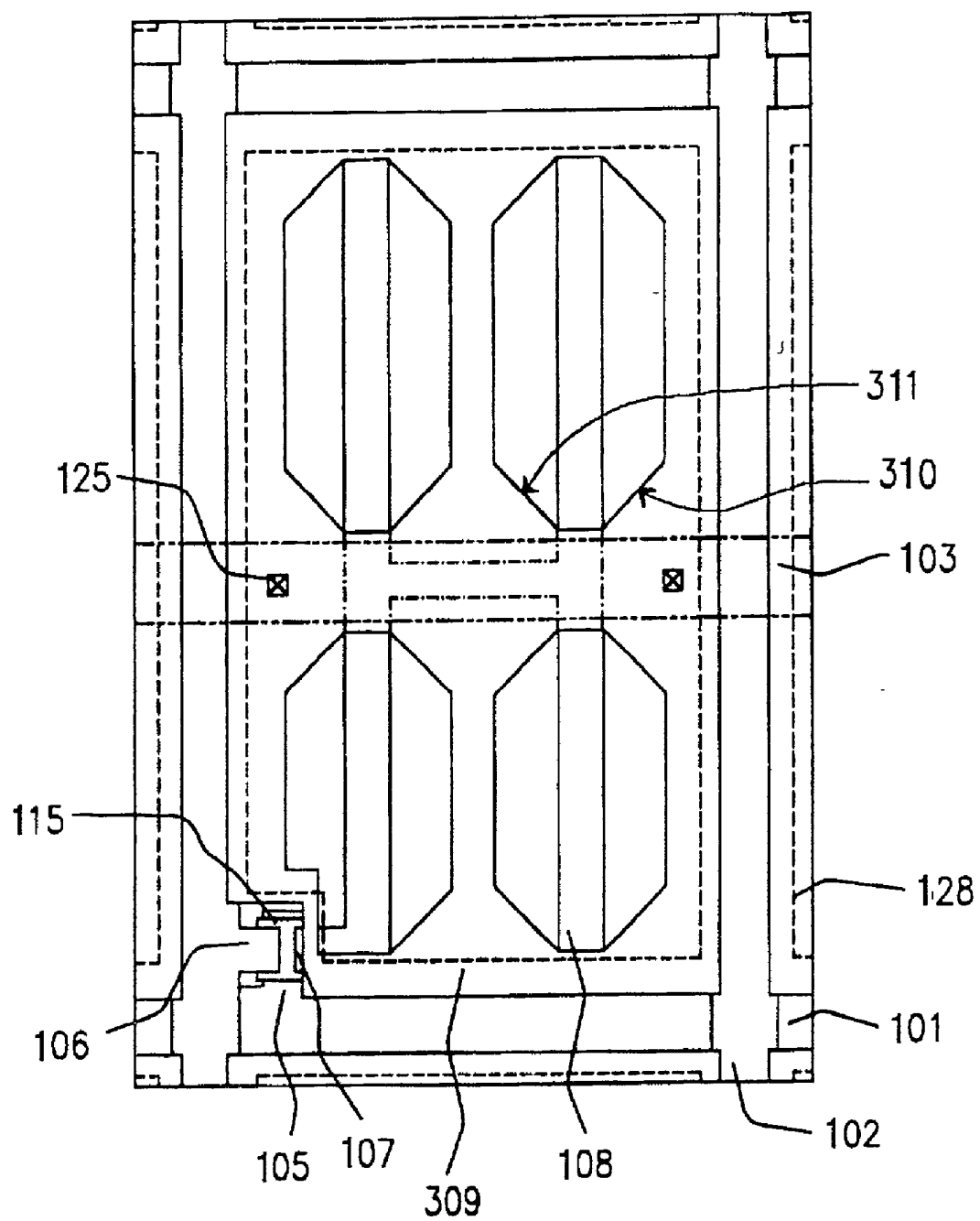


FIG.9b





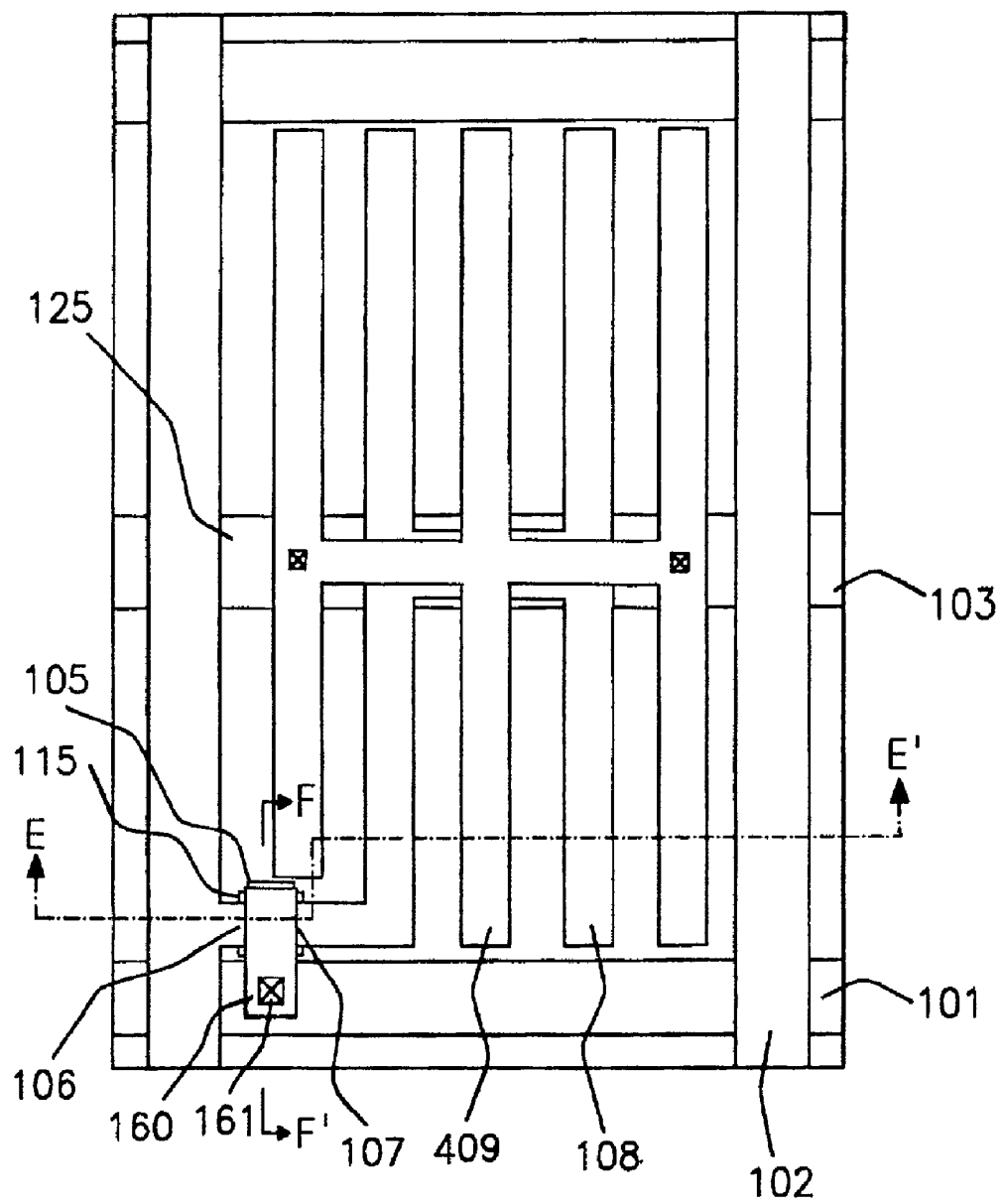


FIG.11b

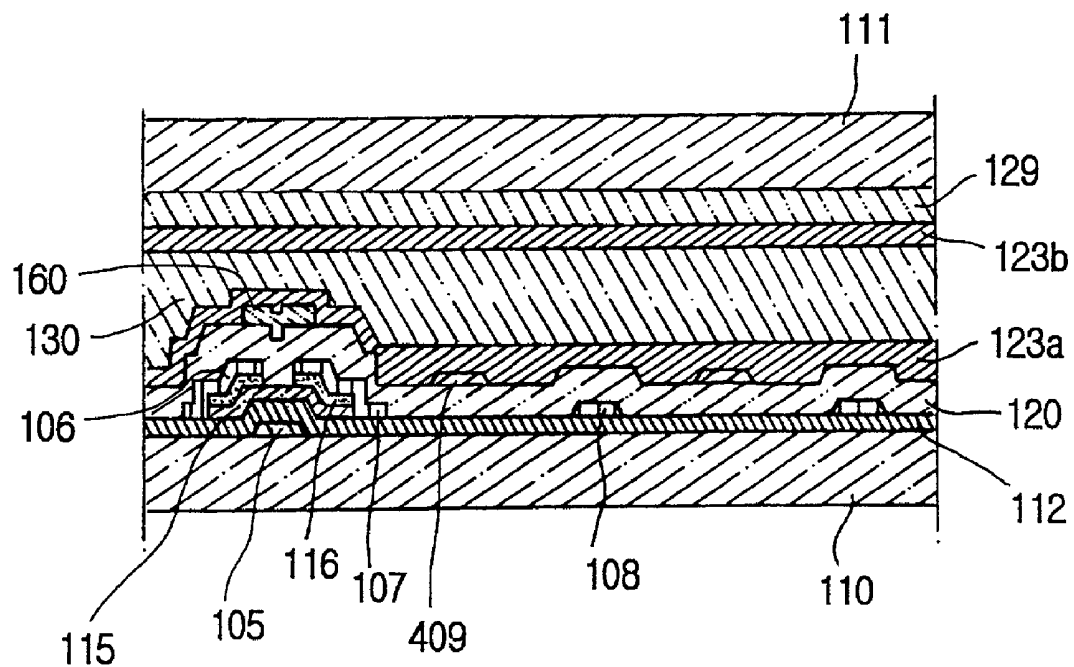


FIG.11c

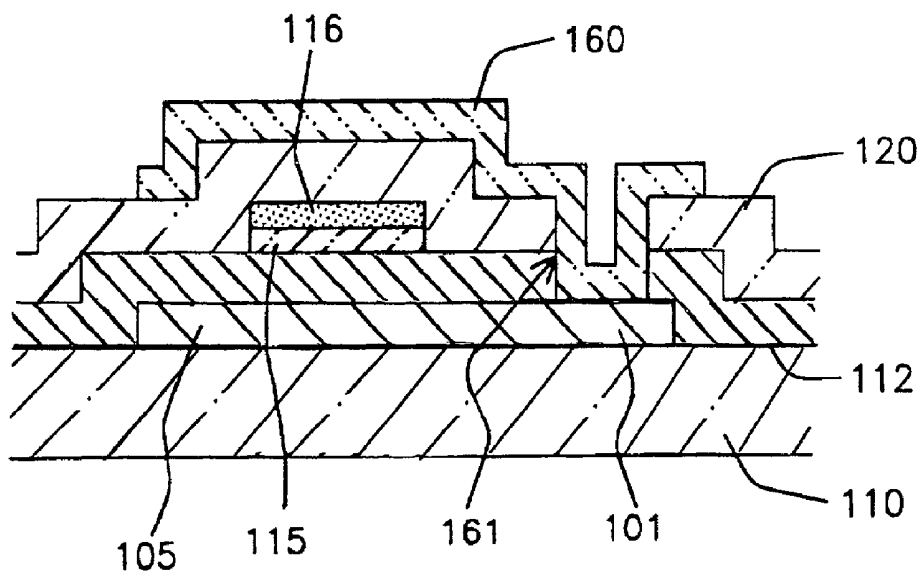
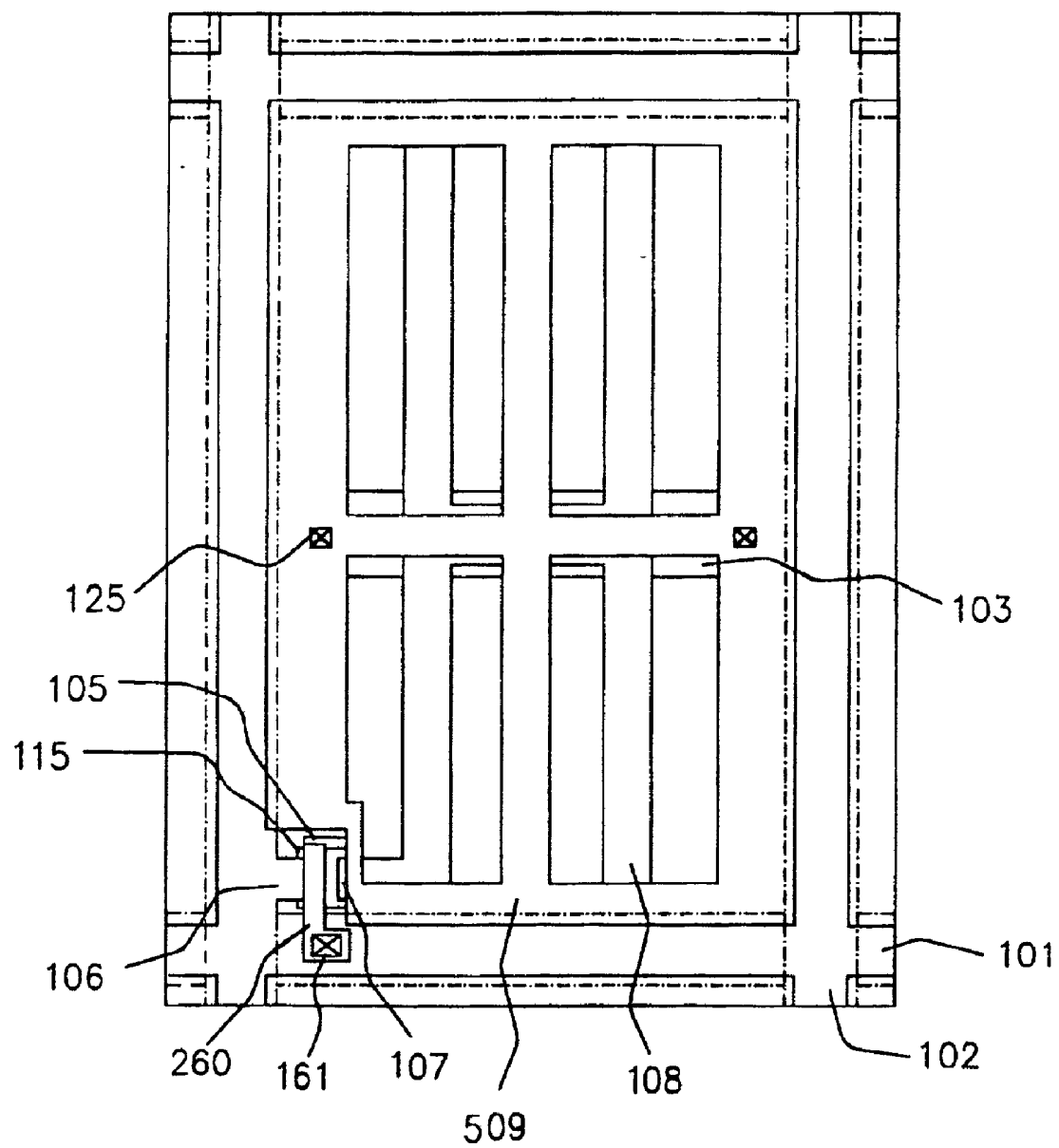


FIG.12



IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a liquid crystal display device, and more particularly to an in-plane switching mode liquid crystal display device, wherein the aperture ratio is improved, the driving voltage is decreased, and the fabricating cost is reduced.

[0002] Recently, the thin film transistor liquid crystal display device (TFT LCD) has been used as a display device of a portable television and a notebook computer, etc., but this TFT LCD has a small viewing angle.

[0003] In order to solve this problem, a twisted nematic LCD having optical compensation plates and a multi-domain LCD, etc., have been introduced. In these LCDs, however, since the contrast ratio depends on the viewing angle direction, the color of the image is shifted.

[0004] For a wide viewing angle, the in-plane switching mode LCD is disclosed in JAPAN DISPLAY 92 p547, Japanese Patent Unexamined Publication No. 7-36058, Japanese Patent Unexamined Publication No. 7-225538, and ASIA DISPLAY 95 P707, and etc.

[0005] FIG. 1a and FIG. 1b are respectively plane and sectional views showing the conventional in-plane switching mode liquid crystal display device (IPS mode LCD), where FIG. 1b is a sectional view taken along line A-A' of FIG. 1a. As shown in these figures, a gate bus line 1 and a data bus line 2 are formed on a first substrate 10, defining a pixel. Although only one pixel is drawn in the figures, the real liquid crystal display device has a plurality of pixels. A common bus line 3 is aligned in the pixel, being parallel to the gate bus line 1. A thin film transistor (TFT) is disposed at the cross of the gate and data bus lines 1 and 2. As shown in FIG. 1b, the TFT comprises a gate electrode 5, a gate insulator 12, an active layer 15, an n⁺ layer 16, a source electrode 6, and a drain electrode 7. In the pixel, a data electrode 8 and a common electrode 9 are formed parallel to the data bus line 2. A portion of the data electrode 8 which overlaps the common bus line 3 is formed to obtain a storage capacitor which functions as maintaining a grey level voltage applied into the data electrode 8. The common electrode 9 is connected to the common bus line 3. The data electrode 8 is formed on the gate insulator 12 and is connected to the drain electrode 7. The TFT, the data electrode 8 and the gate insulator 12 are covered with a passivation layer 20. Thereon, a first alignment layer 23a is coated to determine the alignment direction.

[0006] On a second substrate 11, a black mask 28 is formed to prevent a leakage of light through the regions of the TFT and the gate and data bus lines 1 and 2. Thereon, a color filter layer 29 and a second alignment layer 23b are formed. Between the first and second substrates 10 and 11, a liquid crystal layer 30 is formed.

[0007] When a voltage is applied to the conventional IPS mode LCD, electric field parallel to the substrates 10 and 11 is generated between the data and common electrodes 8 and 9. Liquid crystal molecules in the pixel are rotated according to the electric field, controlling the amount of light passing through the liquid crystal layer 30.

[0008] However, the conventional IPS mode LCD has the following problems.

[0009] Firstly, because the area for storage capacitor occupies quite a portion of the pixel region as well as the data and common electrodes are made of opaque metals, the aperture ratio is lowered.

[0010] Secondly, because the electric field applied to the LC layer is weakened by both the gate insulator 12 and the passivation layer 20 formed over the two electrodes 8 and 9, the driving speed of the LC molecules is decreased, and consequently the driving voltage is increased.

[0011] Thirdly, because the data bus line 2 should be apart from the pixel region to the extent of not generating the crosstalk problem, the pixel region is decreased, thereby lowering the aperture ratio.

[0012] Fourthly, when the black mask is formed on the second substrate, the fabricating cost is increased and the aperture ratio is lowered by the inaccurate lamination of the two substrates.

SUMMARY OF THE INVENTION

[0013] An object of the present invention is to provide an in-plane switching mode liquid crystal display device wherein the aperture ratio is improved, the driving voltage is decreased, and the fabricating cost is reduced.

[0014] In order to achieve the object, the in-plane switching mode liquid crystal display device comprises first and second substrates, a plurality of gate and data bus lines which are aligned on said first substrate to define a plurality of pixel regions, a common bus line aligned in said pixel regions of said first substrate, a thin film transistor formed at each of said pixel regions of said first substrate and comprising a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode, a data electrode formed to be parallel to a first direction on said gate insulator and having a portion overlapping said common bus line for forming a first storage capacitor, a passivation layer formed over said data electrode and said thin film transistor, a common electrode formed on said passivation layer so as to overlap said gate and data bus lines and having a portion overlapping said data electrode for forming a second storage capacitor, and a liquid crystal layer formed between said first and second substrates.

[0015] Said common electrode is formed of ITO and is connected electrically to said common electrode through a first hole formed in said gate insulator and said passivation layer.

[0016] Said gate and data bus line may be formed of high conductive metal layers such as Mo metal layer, Mo/Al/Mo triple metal layers, or Cr/Al/Cr triple metal layers in order to prevent signal delay in said gate and data bus lines which is generated by being overlapped with said common electrode.

[0017] In the in-plane switching mode liquid crystal display device according to the present invention, the passivation layer and the gate insulator do not absorb the electric field applied to the liquid crystal layer because the common electrode is disposed above the two insulating layers. Accordingly, the driving voltage is lowered. Further, because the areas for storage capacitor can be decreased, the aperture ratio is much more improved. Furthermore, because

the common electrode overlaps the gate and data bus lines to block the electric effect of the two bus lines, the crosstalk problem can be removed. Accordingly, the pixel region can be enlarged improving the aperture ratio. In addition, because the common electrode **109** is formed out of ITO to obtain IOP(ITO on passivation) structure, the contacting electric resistance between the pads and the driving circuits is decreased as well as the aperture ratio is improved.

[0018] According to another aspect of the present invention, the in-plane switching mode liquid crystal display device is provided, wherein said common electrode has an oblique side inclined relative to said first direction. The object of this embodiment is to prevent the problem in that disclination is generated in the region the common electrode crosses with the data electrode.

[0019] According to further aspect of the present invention, the in-plane switching mode liquid crystal display device is provided which further comprises a metal layer on said passivation layer in the region of said thin film transistor.

[0020] Said metal layer and said common electrode are formed of opaque metals including Mo, and function as black mask.

[0021] For obtaining IOP structure, said metal layer and said common electrode is formed of a double metal layer ITO/Mo which is formed by depositing Mo and indium tin oxide in the name order.

[0022] Said metal layer can be connected electrically to said data bus line through a second hole which is formed in said gate insulator and said passivation layer. In this case, the metal layer functions as a back gate electrode, increasing the switching speed of said thin film transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] FIG. 1a and FIG. 1b are respectively plane and sectional views showing the conventional in-plane switching mode liquid crystal display device.

[0024] FIG. 2a is a plane view showing a first embodiment of the present invention.

[0025] FIG. 2b and FIG. 2c are respectively sectional views taken along line B-B' and C-C' of FIG. 2a.

[0026] FIG. 3 is a view showing the operation of liquid crystal molecules in the first embodiment.

[0027] FIG. 4 is a view showing the alignment direction in the first embodiment.

[0028] FIG. 5 is a view showing the TFT array structure of the present invention.

[0029] FIG. 6a and FIG. 6b are respectively plane and sectional views showing the structure of the IPS mode LCD according to the present invention.

[0030] FIG. 7 is a plane view showing a second embodiment of the present invention.

[0031] FIG. 8 is a view showing the alignment direction and the direction of first and second oblique sides of the second embodiment.

[0032] FIG. 9a and FIG. 9b are views the direction of electric field and the operation of LC molecules in the first and second embodiments respectively.

[0033] FIG. 10 is a plane view showing a third embodiment of the present invention.

[0034] FIG. 11a is a plane view showing a fourth embodiment of the present invention.

[0035] FIG. 11b and FIG. 11c are respectively sectional views taken along lines E-E' and F-F' of FIG. 11a.

[0036] FIG. 12 is a plane view showing a fifth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0037] Hereinafter, in-plane switching mode LCDs according to the present invention are described in detail accompanying the figures.

[0038] FIG. 2a, FIG. 2b and FIG. 2c are views showing a first embodiment according to the present invention, where FIG. 2b and FIG. 2c are respectively sectional views taken along line B-B' and line C-C' of the FIG. 2a. As shown in these figures, gate and data bus lines **101** and **102** are formed on a first substrate **110**, defining a pixel. Although only one pixel is drawn in these figures, the real liquid crystal display device has a plurality of pixels. In the pixel, a common bus line **103** is formed parallel to the gate bus line **101**. At the cross of the gate and data bus lines **101** and **102**, a thin film transistor(TFT) is formed as shown in FIG. 2b which comprises a gate electrode **105**, a gate insulator **112**, an active layer **115**, a n⁺ layer **116**, a source electrode **106**, and a drain electrodes **107**. In the pixel, data and common electrodes **108** and **109** are disposed parallel to the data bus line **102**. Over the TFT and the data electrode **108**, a passivation layer **120** is formed, and the common electrode **109** is formed thereon to be parallel to the data electrode **108** and overlap the gate and data bus lines **102** and **103**. Over the common electrode **109** and the passivation layer **120**, a first alignment layer **123a** is formed.

[0039] As in the conventional IPS mode LCD, the data electrode **108** has a portion overlapping the common bus line **103** for obtaining a first storage capacitor(C_{st1}) as shown in FIG. 2a and 2c. In addition, the common electrode **109** has a portion overlapping the data electrode **108** for obtaining a second storage capacitor(C_{st2}).

[0040] The common electrode **109** is connected to the common bus line **103** through a first hole **125** which is formed in the passivation layer **120** and the gate insulator **112**, and it functions as blocking the electric effect of the two bus lines **101** and **102** to prevent the crosstalk problem.

[0041] The gate electrode **105**, the gate bus line **101**, and the common bus line **103** are formed by patterning double metal layers (Mo/Al) which is deposited by sputtering an Al layer having a thickness of 2000 Å and a Mo layer having a thickness of 1000 Å in the name order. The gate insulator **112** is formed thereon by depositing an inorganic insulating layer such as silicon nitride having a thickness of 4000 Å by a chemical vapor deposition method. The active layer **115** and the n⁺ layer **116** are formed by depositing and etching an amorphous silicon(a-Si) layer having a thickness of 1700 Å and a n⁺ a-Si layer having a thickness of 300 Å. The data

bus line **102**, the data electrode **108**, the source electrode **106**, and the drain electrode **107** are formed by depositing and etching a Cr metal layer having a thickness of 1500 Å.

[0042] The TFT, and the data electrode **108** are covered with a passivation layer **120** such as silicon oxide and silicon nitride having a thickness of 2000 Å. On the passivation layer **120**, the common electrode **109** is formed by depositing and etching a transparent conducting layer such as indium tin oxide(ITO) having a thickness of 500 Å.

[0043] Over the common electrode **109** and the passivation layer **120**, a first alignment layer **123a** is formed by coating polyimide or photo-alignment materials. The polyimide alignment layer is rubbed for determining the alignment direction. On the other hand, the photo-alignment layer such as polyvinylcinnamate(PVCN) or polysiloxane based materials is exposed to a ultra violet light for determining the alignment direction.

[0044] As shown in the FIG. 2c, the data and common electrodes **108** and **109** have portions for first and second storage capacitors (C_{st1} , C_{st2}). Accordingly, the total storage capacitor (C_{st}) in the present invention becomes the sum of the first and second storage capacitors (C_{st1} , C_{st2}). The storage capacitor (C_{st}) is double the conventional storage capacitor(C_{st}), so that the area for storage capacitor can be reduced to half the conventional area, thereby improving the aperture ratio.

[0045] As shown in FIG. 3b, on a second substrate **111**, a black mask **128** and a color filter layer **129** are formed. An overcoat layer may be formed thereon for the flatness and stability of the surface thereof. The black mask **128** prevents a leakage of light through the regions of TFT and gate, data and common bus lines **101**, **102**, and **103**. The black mask **128** is made of a Cr or a CrOx metal layer having a thickness of 0.1 μm and a width of 10 μm. The color filter layer **129** has R, G, and B color filter elements in each pixels. On the color filter layer **129**, a second alignment layer **123b** is formed by coating polyimide or photo-alignment materials. The second alignment layer **123b** is rubbed or exposed to UV light for determining the alignment direction. A liquid crystal layer **130** is formed between the two substrates **110** and **111** by injecting liquid crystal in vacuum state.

[0046] FIG. 3 is a view showing the operation of a liquid crystal molecule in the IPS mode LCD according to the present invention. FIG. 4 is a view showing the alignment direction, where Y axis direction indicates the extension direction of the data and common electrodes **108** and **109**, and θ_R indicates the angle between the alignment direction and X axis direction. When a voltage is not applied to the device, the liquid crystal molecules are aligned according to the alignment direction. When a voltage is applied to the device, electric field parallel to the substrates is generated between the common and data electrodes **109** and **108**, and thereby the liquid crystal molecules **132** rotates clockwise according to the electric field. In this figure, a reference number **133** indicates the liquid crystal molecules after applying the voltage.

[0047] FIG. 5 is a view showing the TFT array structure of the present invention. The gate and data bus lines **101** and **102** are connected to gate and data driving circuits through gate and data pads **151** and **155** respectively. The gate and data bus lines **101** and **102** are connected to a grounding

wiring **165** through an electrostatic shielding circuit **167** composed of TFT. Also the common bus line **103** is grounded through the common pad **157**.

[0048] Although not illustrated in the figure, the gate, data and common pads **151**, **155** and **157** are made of first, second and third metal layers. The first metal layer is formed of Mo/Al double metal layers together with the gate electrode **105** and common bus line **103**. The second metal layer is formed of Cr together with the source and drain electrodes **106** and **107**. The third metal layer is formed of ITO together with the common electrode **109**. In order to connect the pads to the driving circuits, it is need to etch the gate insulator **112** and the passivation layer **120** in the pad region. The two insulating layers in the pad region are etched when the hole **125** is formed. In the prior art, an oxide layer is generated on the pads by the exposure to the air, causing a problem that the contacting electric resistance is increased when connecting the pads to the driving circuits. However, in this embodiment, because the third metal layer of the pads is made of ITO for obtaining IOP(ITO On Passivation) structure, the above-mentioned problem is not generated.

[0049] FIG. 6a and FIG. 6b are plane and sectional views showing the structure of the in-plane switching mode LCD according to the present invention, where the FIG. 6b is a sectional view taken along line D-D' of the FIG. 6a. As shown in these figures, gate and data driving circuits **150** and **154** are disposed in a frame **145** outside the display region **140**. The gate and data driving circuits **150** and **154** are connected to the gate and data bus lines **101** and **102** through the gate and data pads **151** and **154** respectively. A backlight housing **147** is disposed on the upper side of the frame **145**. In the backlight housing **147**, a backlight **148** is disposed to project a light into a liquid crystal panel **139** through a light pipe **149**. Between the light pipe **149** and the liquid crystal panel **139**, a polarizer **135** is disposed to polarize the light linearly. An analyzer **136** is disposed on the front of the panel **139**.

[0050] The advantages of the first embodiment according to the present invention are summarized as follows.

[0051] Firstly, the passivation layer **120** and the gate insulator **112** do not absorb the electric field applied to the liquid crystal layer **130** because the common electrode **109** is disposed above the two insulating layers **112** and **120**. Accordingly, the driving voltage is lowered.

[0052] Secondly, because the areas for storage capacitor can be decreased, the aperture ratio is much more improved.

[0053] Thirdly, because the common electrode **109** overlaps the gate and data bus lines **101** and **102** to block the electric effect of the two bus lines **101** and **102**, the crosstalk problem can be removed. Accordingly, the pixel region can be enlarged improving the aperture ratio.

[0054] Fourthly, because the common electrode **109** is formed out of ITO to obtain IOP structure, the contacting electric resistance between the pads and the driving circuits is decreased as well as the aperture ratio is improved.

[0055] FIG. 7 is a view showing a second embodiment of the present invention. Hereinafter, constituent elements similar to those of the first embodiment are denoted by the same reference numbers. As shown in this figure, this embodiment differs from the first embodiment in that a

common electrode **209** has first and second oblique sides **120** and **121**. FIG. 8 is a view showing the alignment direction and the direction of the first and second oblique sides of the second embodiment, where Y axis indicates the extension direction of the data electrode **108**. In region A, the first oblique side **210** is inclined counterclockwise to X axis direction with an angle θ_A . In region B, the second oblique side **210** is inclined clockwise to X axis direction with an angle θ_B . The alignment direction is determined to be inclined counterclockwise to X axis direction with an angle θ_R in the range of 0° to 90° . The angle θ_A is determined to be in the range of θ_R to 90° . The angle θ_B is determined to be in the range of $90^\circ - \theta_R$ to 90° . The figures show a case where the angle θ_R is larger than 45° , and thereby the angle θ_A is larger than the angle θ_B . On the contrary, when the angle θ_R is smaller than 45° , the angle θ_B is determined to be larger than the angle θ_A .

[0056] The object of this embodiment is to prevent the problem of the first embodiment in that disclination is generated in the region the common electrode **209** crosses with the data electrode **109**.

[0057] In the first embodiment, the electric field is generated between the common and data electrodes **108** and **109** as shown in FIG. 9a. In the middle region of the opening portion, the direction of electric field is perpendicular to the extension direction of the electrodes **108** and **109**. When voltage is applied to the device, in the middle region, the LC molecules **132** are given with a clockwise turning force according to the electric field perpendicular to the extension direction of the electrodes **108** and **109**, and thereby they rotate clockwise to be aligned perpendicular to the extension direction of the electrodes. On the other hand, in regions A and B where the common electrode **109** crosses with the data electrode **108**, electric field is deformed not to be perpendicular to the extension direction of the electrodes **108** and **109**. When the voltage is applied to the electrodes **108** and **109**, in the regions A and B, the LC molecules **132** are aligned to be different from the middle region. Particularly in the region bounded by chain lines, the LC molecules are given with a counterclockwise turning force according to the deformed electric field, and thereby they rotate in opposite direction to those in the middle region. Consequently, in the border region denoted by chain lines, the alignment of LC molecules **132** is not defined, thereby generating disclination. Particularly when using liquid crystal having a low viscosity for lowering the driving voltage, since the interaction between the LC molecules **132** is weak, a possibility of generating the disclination is increased to deteriorate the image quality. In this figure, reference number **133** denotes LC molecules after applying the voltage.

[0058] However, in the second embodiment, since the common electrode **209** has first and second oblique sides **210** and **211**, as shown in FIG. 7, the electric field is slightly deformed in the regions A and B, as shown in FIG. 9b. The electric field gives a clockwise turning force to the LC molecules **232** in the regions A and B. Accordingly, although using liquid crystal having a low viscosity for lowering the driving voltage, LC molecules **232** in regions A and B rotate in the same direction with those in the middle region, thereby preventing the disclination. In FIG. 9b, reference number **233** denotes LC molecules after applying the voltage.

[0059] The second embodiment has an aperture ratio lower than the first embodiment, and however has a more improved image quality by preventing the disclination. In this case, it is preferable to form the common electrode **209** out of ITO for improving the aperture ratio.

[0060] FIG. 10 is a view showing a third embodiment. This embodiment is similar to the second embodiment excepting the angles θ_A and θ_B of the common electrode **309**. It is determined in this embodiment that the angles θ_A , θ_B and θ_R are 45° , 45° , and 75° respectively. In region B, because the angle θ_B is in said range of $90^\circ - \theta_R$ to 90° , the LC molecules are given with a clockwise turning force, thereby not generating the disclination. In the other hand, in region A, since the angle θ_A is out of said range of θ_R to 90° , the LC molecules are given with a counterclockwise turning force. However, unless using liquid crystal having a low viscosity, the disclination is not generated with the assistance of interaction between the LC molecules. Further, considering the viscosity, the angle θ_B can be determined to be less than 25° , $90^\circ - \theta_R$, for improving the aperture ratio.

[0061] FIG. 11a, 11b, and 11c are plane and sectional views showing the fourth embodiment, where FIG. 11b and 11c are sectional views taken along lines E-E' and F-F' of FIG. 11a.

[0062] In this embodiment, as shown in these figures, the data and common electrodes **108** and **409** have portions for first and second storage capacitors (C_{st1} , C_{st2}) as in the previous embodiments. This embodiment differs from the previous embodiments in that the common electrode does not overlap the gate and data bus lines **101** and **102**, and a light shielding electrode **160** is formed on the passivation layer **120** in the region of the TFT. The common electrode **409** and the light shielding electrode **160** are formed together by sputtering and etching Mo metal layer having a thickness of 1000 \AA . Because the light shielding electrode **160** functions as a black mask for the TFT, as shown in FIG. 11b, the black mask is not formed in the region of TFT. For obtaining IOP structure, the two electrodes **409** and **160** are formed of metal layers including ITO, and it is preferable that they are formed of a double layer ITO/Mo which is formed by depositing Mo metal layer and ITO in the same order. The light shielding electrode **160** is formed to overlap a portion of the gate bus line **101** so as to be connected with the gate bus line **101** through a second hole **161** formed in the gate insulator **112** and the passivation layer **120**. Accordingly, the light shielding electrode **160** is provided with the same voltage as the gate electrode **105**.

[0063] In this embodiment, since the light shielding electrode **160** overlaps the TFT with the passivation layer **120** interposed therebetween in order to prevent a light incident on the active layer **115** of the TFT. Accordingly, there is no need to form a black mask in the region of TFT, decreasing the fabricating cost. Further, the leakage current is prevented which is generated by excitation of the active layer **115** when the active layer **115** is exposed to light, so that a backlight having a high light intensity can be used improving the luminosity of the device.

[0064] In addition, since the light shielding electrode **160** is connected with the gate bus line for obtaining the same voltage as the gate electrode **105**, it functions as a back gate electrode increasing the switching current of the TFT. Accordingly, switching speed of the TFT is increased so that

the same switching speed as the prior art can be obtained using TFT of relatively small size.

[0065] FIG. 12 is a view showing a fifth embodiment. As shown in this figure, this embodiment is similar to the fourth embodiment except that a common electrode 509 overlaps the gate and data bus lines 101 and 102 as the first, second, and third embodiments.

[0066] The common electrode 509 and a light shielding electrode 260 are formed of opaque metals as the fourth embodiment, and function as a light shielding layer so that there is no need to form a black mask in the regions of the TFT, and the two bus lines 101 and 102. Accordingly, the fabricating cost for the black mask is reduced, and prevented is the conventional problem in that the aperture ratio is lowered by inaccurate lamination when forming the black mask on the second substrate. Further, as the fourth embodiment, the light shielding electrode 260 prevents a light incident on the active layer.

[0067] In the first, second, third, and fifth embodiments, a parasitic capacitor may be formed between the common electrode and the gate and data bus lines, causing the signal delay in the two bus lines. This signal delay problem can be removed by forming the gate and data bus lines out of low resistance metal layers such as Mo metal layer, Mo/Al/Mo triple metal layers or Cr/Al/Cr triple metal layers.

[0068] The present invention is characterized in that the common electrode is formed on the passivation layer 120, and the data and common electrodes have portions for first and second storage capacitors (C_{st1} , C_{st2}). Accordingly, the passivation layer 120 and the gate insulator 112 do not absorb the electric field applied to the liquid crystal layer 130 because the common electrode is disposed above the two insulating layers 112 and 120. Accordingly, the driving voltage is lowered. Further, because the areas for storage capacitor can be decreased, the aperture ratio is much more improved. Furthermore, because the common electrode is formed out of ITO for obtaining IOP structure, the contacting electric resistance between the pads and the driving circuits is decreased as well as the aperture ratio is improved.

[0069] In first, second, third, and fifth embodiments according to the present invention, because the common electrode overlaps the gate and data bus lines to block the electric effect of the two bus lines, the crosstalk problem can be removed. Accordingly, the pixel region can be enlarged improving the aperture ratio.

[0070] In fourth and fifth embodiments, the light shielding electrode functions as a back gate electrode for increasing the switching speed of TFT, and prevents a leakage current caused by excitation of the active layer. Particularly in the fifth embodiment, since the light shielding electrode and the common electrode function as a black mask, there is no need to form the black mask in the regions of TFT and the two bus lines 101 and 102, removing the problems generated when forming the black mask on the second substrate.

[0071] While the preferred form of the present invention has been described, it is to be understood that modifications will be apparent to those skilled in the art without departing from the spirit of the invention.

[0072] The scope of the invention, therefore, is to be determined solely by the following claims.

What is claimed is:

1. An in-plane switching mode liquid crystal display device comprising:

first and second substrates;

a plurality of gate and data bus lines which are aligned on said first substrate to define a plurality of pixel regions;

a common bus line aligned in said pixel regions of said first substrate;

a thin film transistor formed at each of said pixel regions of said first substrate and comprising a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

a data electrode formed to be parallel to a first direction on said gate insulator and having a portion overlapping said common bus line for forming a first storage capacitor;

a passivation layer formed over said data electrode and said thin film transistor;

a common electrode formed on said passivation layer so as to overlap said gate and data bus lines and having a portion overlapping said data electrode for forming a second storage capacitor; and

a liquid crystal layer formed between said first and second substrates.

2. The device according to claim 1, wherein said common electrode is connected electrically to said common electrode through a first hole formed in said gate insulator and said passivation layer.

3. The device according to claim 1, wherein said data bus lines are formed of high conductive metal layers.

4. The device according to claim 3, The device according to claim 4, wherein said data bus lines include Mo metal layer, Mo/Al/Mo triple metal layers, or Cr/Al/Cr triple metal layers.

5. The device according to claim 1, wherein said common electrode includes indium tin oxide.

6. The device according to claim 1, wherein said common electrode has an oblique side inclined to a second direction perpendicular to said first direction.

7. The device according to claim 6, wherein said common electrode includes indium tin oxide.

8. The device according to claim 1, further comprising an alignment layer formed over said common electrode and said passivation layer.

9. The device according to claim 8, wherein an alignment direction of said alignment layer is determined to be inclined counterclockwise to said second direction with a first angle θ_1 .

10. The device according to claim 9, wherein said first angle θ_1 is in the range of 45° to 90°.

11. The device according to claim 9, wherein said common electrode have a first oblique counterclockwise inclined to said second direction with a second angle θ_2 , and a second oblique clockwise inclined to said second direction with a third angle θ_3 .

12. The device according to claim 11, wherein said second angle θ_2 is in the range of said first angle θ_1 to 90°.

13. The device according to claim 11, wherein said third angle θ_3 is in the range of 90°- θ_1 to 90°.

14. The device according to claim 11, wherein said first angle θ_1 is 75° .

15. The device according to claim 11, wherein said second angle θ_2 is 45° .

16. The device according to claim 11, wherein said third angle θ_3 is 45° .

17. The device according to claim 1, further comprising a metal layer formed on said passivation layer in the region of said thin film transistor.

18. The device according to claim 17, wherein said metal layer and said common electrode are formed of the same metal.

19. The device according to claim 17, wherein said metal layer and said common electrode include Mo.

20. The device according to claim 17, wherein said metal layer and said common electrode include indium tin oxide.

21. The device according to claim 17, wherein said metal layer and said common electrode include a double metal layer ITO/Mo which is formed by depositing Mo and indium tin oxide in the name order.

22. The device according to claim 17, wherein said metal layer is connected electrically to said data bus line through a second hole which is formed in said gate insulator and said passivation layer.

23. The device according to claim 22, wherein said metal layer overlaps a portion of said gate bus line, and said second hole is formed in the region of said portion.

24. An in-plane switching mode liquid crystal display device comprising:

first and second substrates;

a plurality of gate and data bus lines which are aligned on said first substrate to define a plurality of pixel regions;

a common bus line aligned in said pixel regions of said first substrate;

a thin film transistor formed at each of said pixel regions of said first substrate and comprising a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

a data electrode formed on said gate insulator and having a portion overlapping said common bus line for forming a first storage capacitor;

a passivation layer formed over said data electrode and said thin film transistor;

a common electrode formed on said passivation layer and having a portion overlapping said data electrode for forming a second storage capacitor;

a metal layer formed on said passivation layer in the region of said thin film transistor; and

a liquid crystal layer formed between said first and second substrates.

25. The device according to claim 24, wherein said common electrode is connected to said common bus line through a first hole formed in said gate insulator and said passivation layer.

26. The device according to claim 24, wherein said metal layer and said common electrode is formed of the same metal.

27. The device according to claim 24, wherein said metal layer and said common electrode include Mo.

28. The device according to claim 24, wherein said metal layer and said common electrode include indium tin oxide.

29. The device according to claim 24, wherein said metal layer and said common electrode include a double metal layer ITO/Mo which is formed by depositing Mo and indium tin oxide in the name order.

30. The device according to claim 24, wherein said metal layer is connected electrically to said data bus line through a second hole which is formed in said gate insulator and said passivation layer.

31. The device according to claim 30, wherein said metal layer overlaps a portion of said gate bus line, and said second hole is formed in the region of said portion.

32. An in-plane switching mode liquid crystal display device comprising:

first and second substrates having a plurality of pixel regions;

a common bus line formed in said pixel regions;

a first insulating layer formed on said common electrode;

a data electrode formed on said gate insulator and having a portion overlapping said common bus line for forming a first storage capacitor;

a second insulating layer formed on said data electrode;

a common electrode formed on said passivation layer so as to have an oblique side inclined to the extension direction of said data electrode and having a portion overlapping said data electrode for forming a second storage capacitor; and

a liquid crystal layer formed between said first and second substrates.

* * * * *

专利名称(译)	面内切换模式液晶显示装置		
公开(公告)号	US20020067455A1	公开(公告)日	2002-06-06
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[标]申请(专利权)人(译)	KOMATSU HIROSHI		
申请(专利权)人(译)	KOMATSU HIROSHI		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	KOMATSU HIROSHI		
发明人	KOMATSU, HIROSHI		
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摘要(译)

本发明公开了一种面内切换模式液晶显示装置，包括第一和第二基板，形成在所述第一基板上以限定多个像素区域的多条栅极和数据总线，在每个像素区域中排列的公共总线。第一基板，形成在第一基板的每个像素区域的薄膜晶体管（TFT），数据电极，形成在TFT的栅极绝缘体上，并且具有与公共总线重叠的部分，用于形成第一存储电容器，形成在数据电极和TFT上方的钝化层，公共电极，形成在钝化层上，以便与栅极线和数据总线重叠，并具有与所述数据电极重叠的部分，用于形成第二存储电容器，以及液体在第一和第二基板之间形成的晶体层。

