



US007812910B2

(12) **United States Patent**  
**Lee**

(10) **Patent No.:** **US 7,812,910 B2**  
(45) **Date of Patent:** **Oct. 12, 2010**

(54) **LIQUID CRYSTAL DISPLAY DEVICE**

(75) Inventor: **Do Young Lee**, Seoul (KR)

(73) Assignee: **LG Display Co., Ltd.**, Seoul (KR)

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 884 days.

(21) Appl. No.: **11/638,519**

(22) Filed: **Dec. 14, 2006**

(65) **Prior Publication Data**

US 2007/0132900 A1 Jun. 14, 2007

(30) **Foreign Application Priority Data**

Dec. 14, 2005 (KR) ..... 10-2005-0123064

(51) **Int. Cl.**

**G02F 1/1343** (2006.01)

(52) **U.S. Cl.** ..... **349/143; 349/141; 349/142**

(58) **Field of Classification Search** ..... **349/141-143**  
See application file for complete search history.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

6,657,699	B2 *	12/2003	Matsumoto	.....	349/156
6,791,652	B2 *	9/2004	Yang et al.	.....	349/141
6,876,420	B2 *	4/2005	Hong et al.	.....	349/141
2002/0018166	A1 *	2/2002	Matsumoto et al.	.....	349/141
2002/0044247	A1 *	4/2002	Ko et al.	.....	349/141

**FOREIGN PATENT DOCUMENTS**

CN 1677476 A 10/2005

JP	11-344725	A	12/1999
JP	2000-29073	A	1/2000
JP	2001-56476	A	2/2001
JP	2002-72250	A	3/2002
JP	2002-287712	A	10/2002
JP	2004-86226	A	3/2004

**OTHER PUBLICATIONS**

Office Action issued Oct. 6, 2009 in corresponding Japanese Application No. 2006-337100.

Office Action issued Feb. 16, 2010 in corresponding Japanese Application No. 2006-337100.

Japanese Office Action in counterpart Japanese patent application, dated Jun. 1, 2010.

\* cited by examiner

*Primary Examiner*—Julie-Huyen L Ngo

(74) *Attorney, Agent, or Firm*—Morgan, Lewis & Bockius LLP

(57) **ABSTRACT**

A liquid crystal display device includes gate and data lines on a first substrate, wherein the gate lines cross the data lines to define sub-pixels, thin film transistors adjacent to where the gate lines cross the data lines, pixel electrodes connected to the thin film transistors, common electrodes at left and right sides of the sub-pixels, wherein a first parasitic capacitance between a first data line arranged at the left side of a first sub-pixel and an adjacent first common electrode is smaller than a second parasitic capacitance between a second data line arranged at the right side of the first sub-pixel and an adjacent second common electrode, and a second substrate bonded to the first substrate with a layer of liquid crystal molecules there between.

**12 Claims, 7 Drawing Sheets**

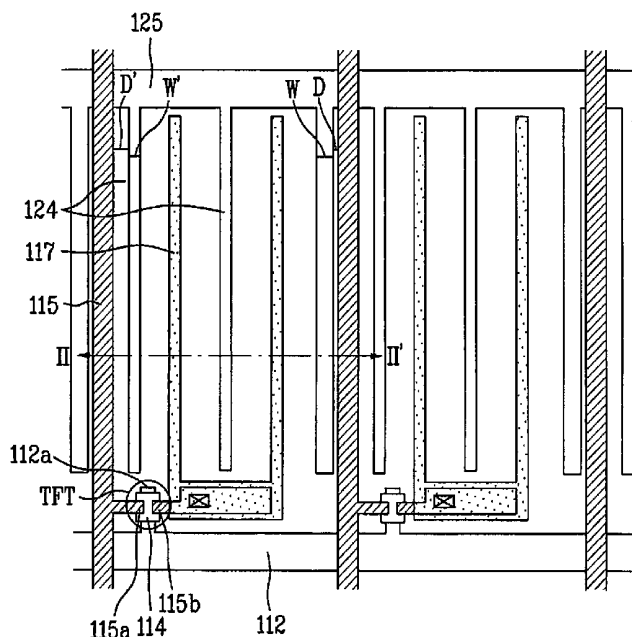


FIG. 1

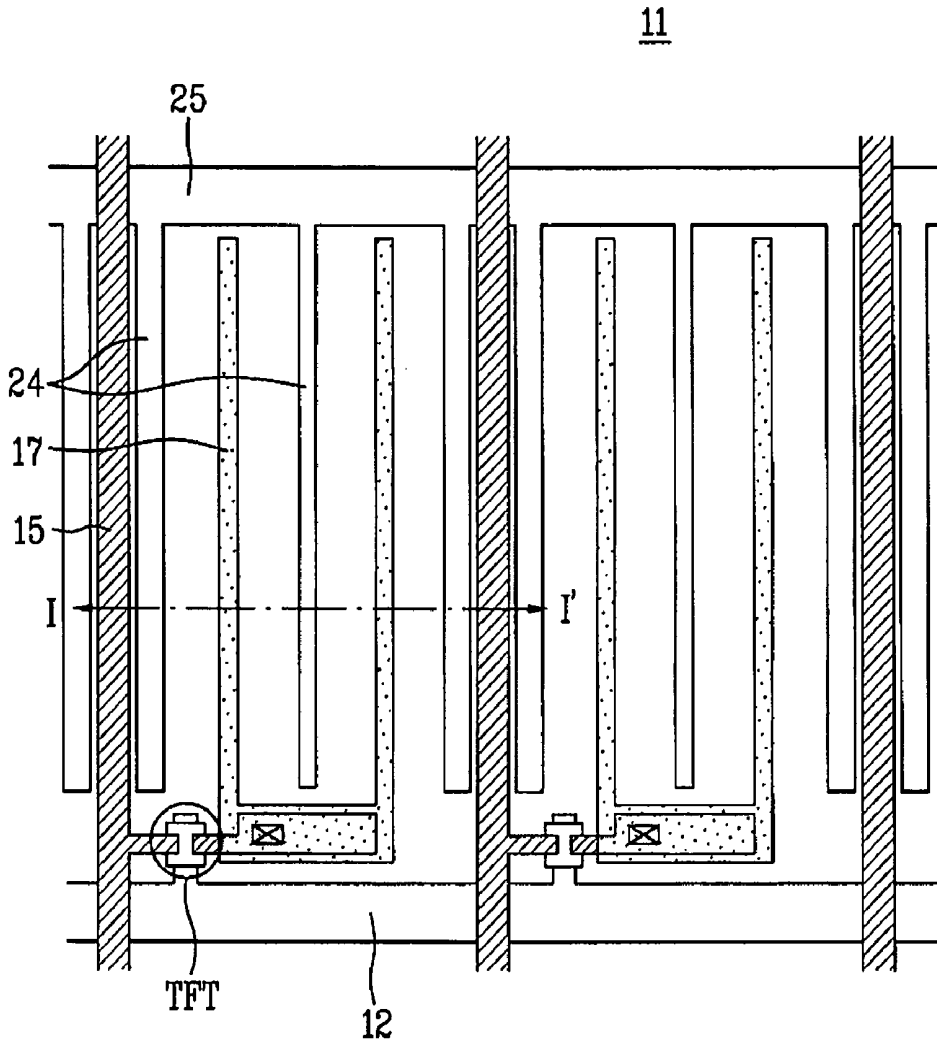


FIG. 2

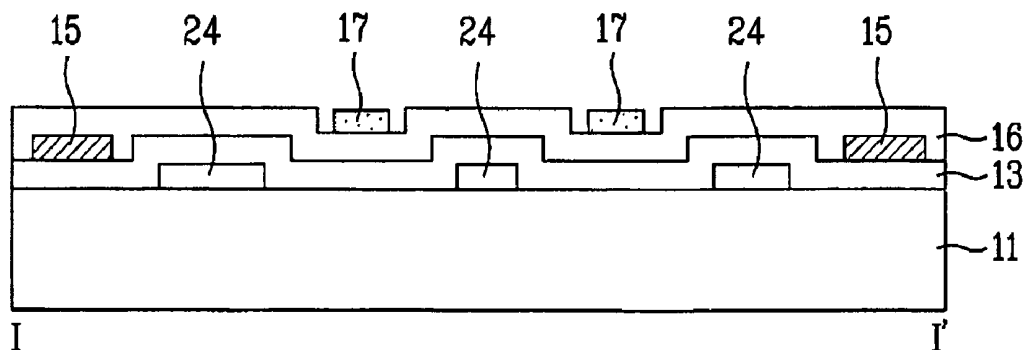


FIG. 3

R	G	B			R	G	B			R	G	B					
			R	G	B				R	G	B				R	G	B
R	G	B			R	G	B			R	G	B					
			R	G	B				R	G	B				R	G	B

FIG. 4

R	G	B			R	G	B			R	G	B		
R	G	B			R	G	B			R	G	B		
R	G	B			R	G	B			R	G	B		
R	G	B			R	G	B			R	G	B		

FIG. 5A

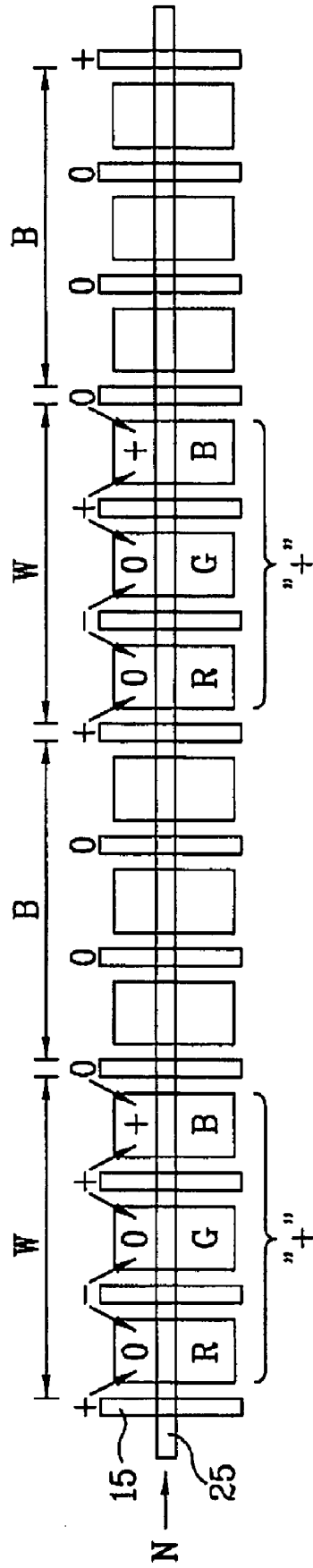


FIG. 5B

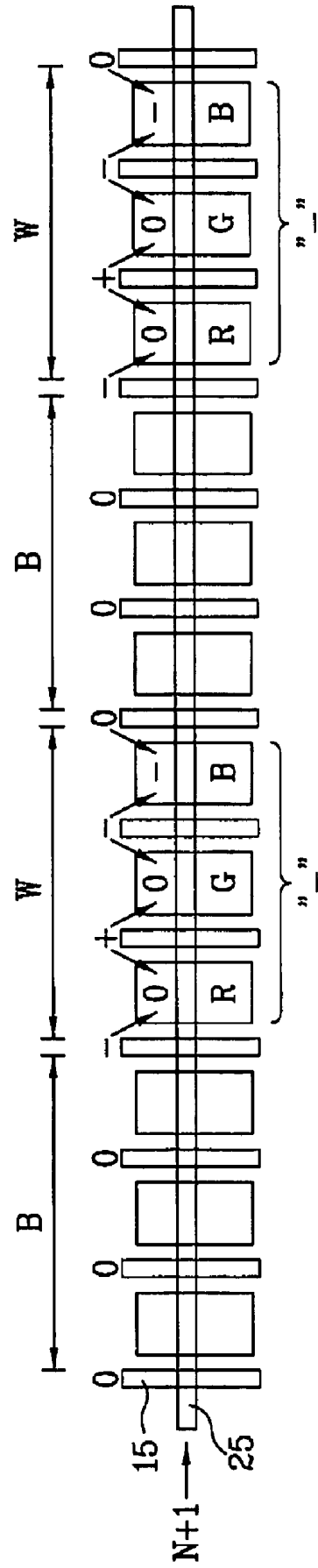


FIG. 6A

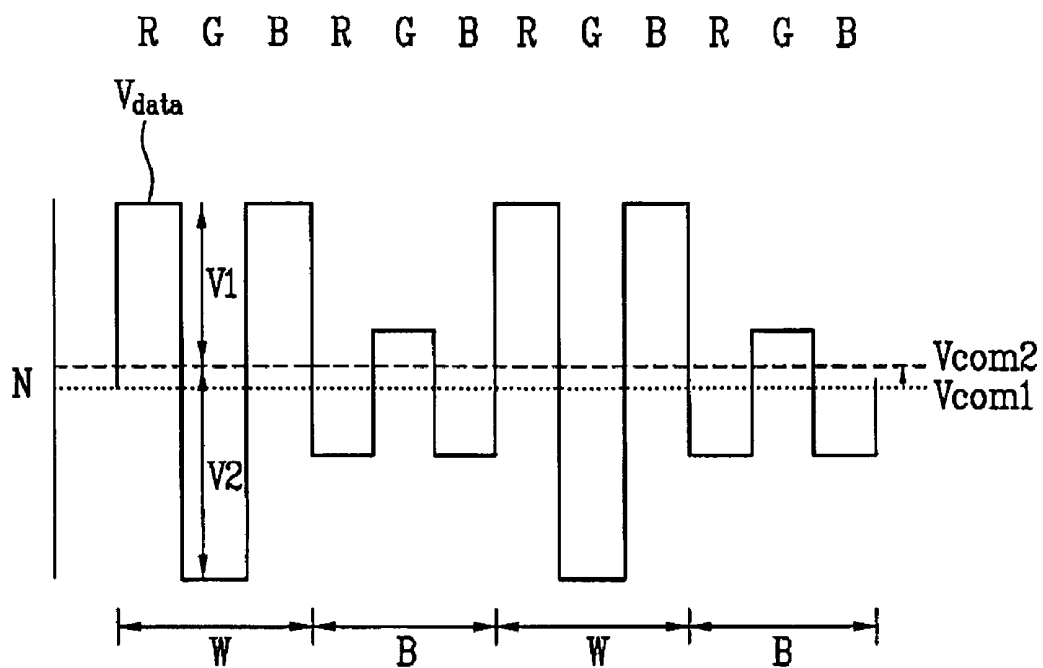


FIG. 6B

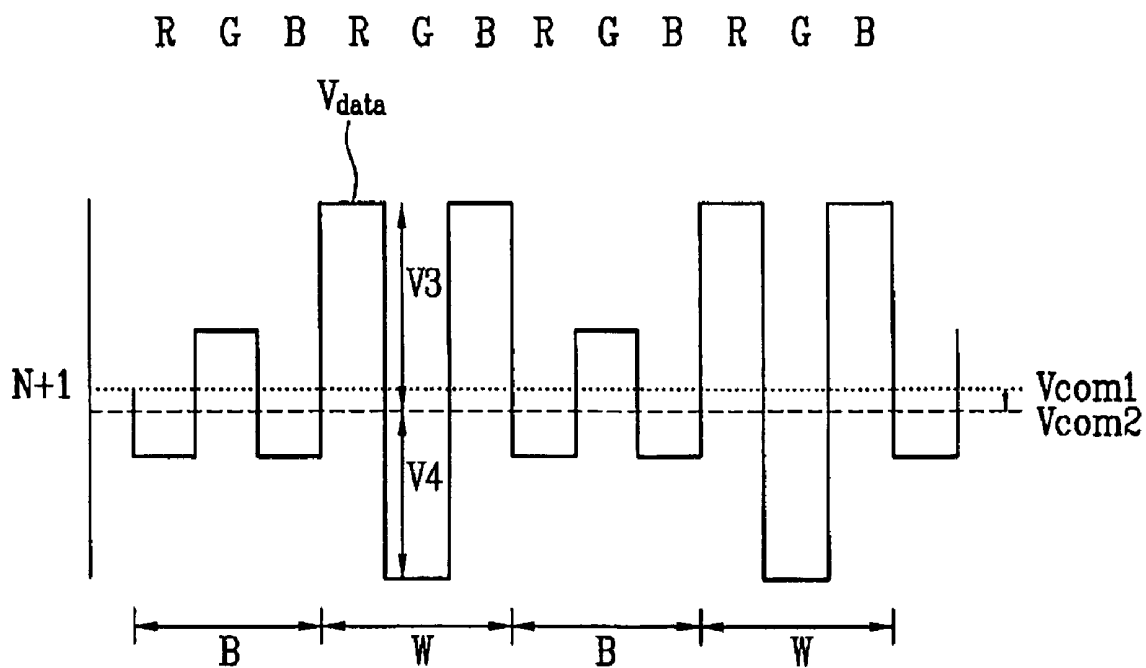


FIG. 7

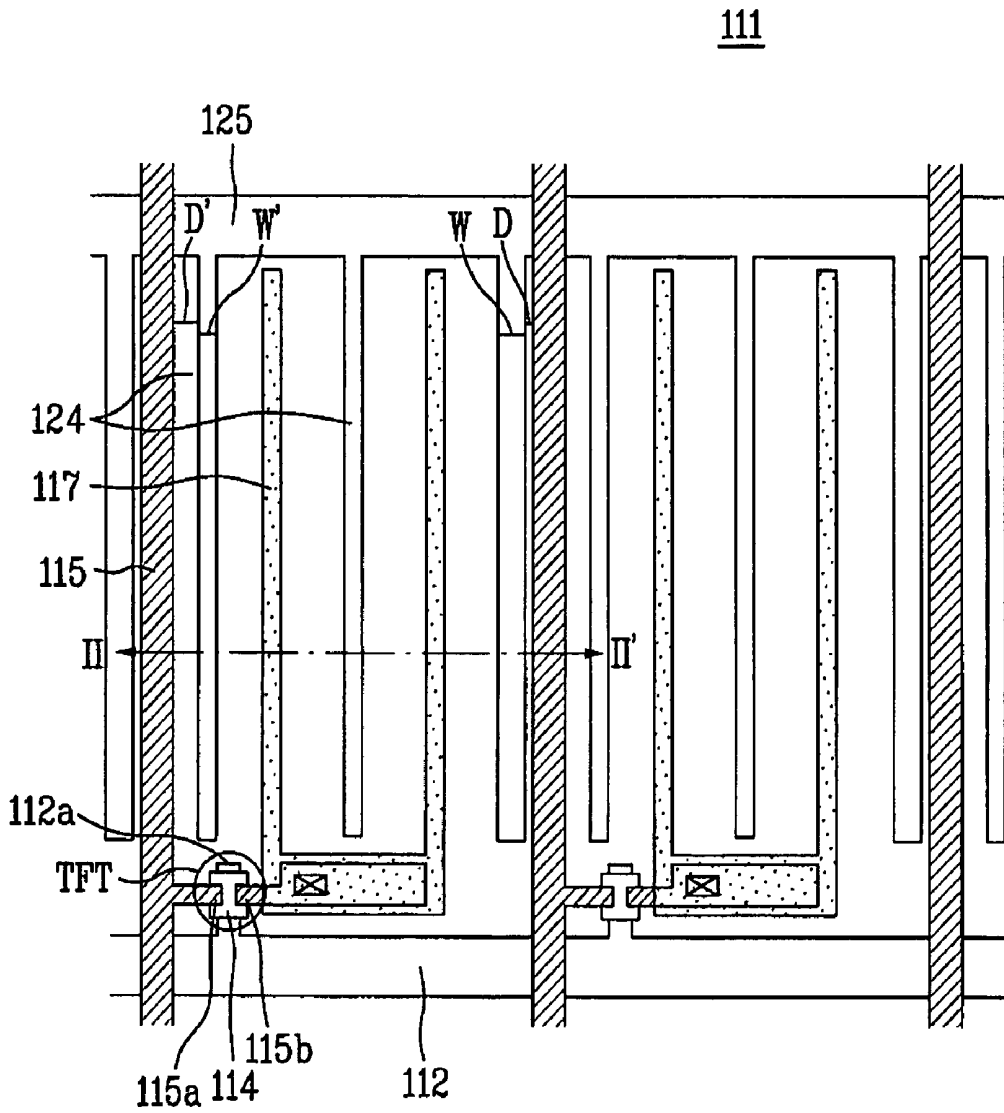


FIG. 8

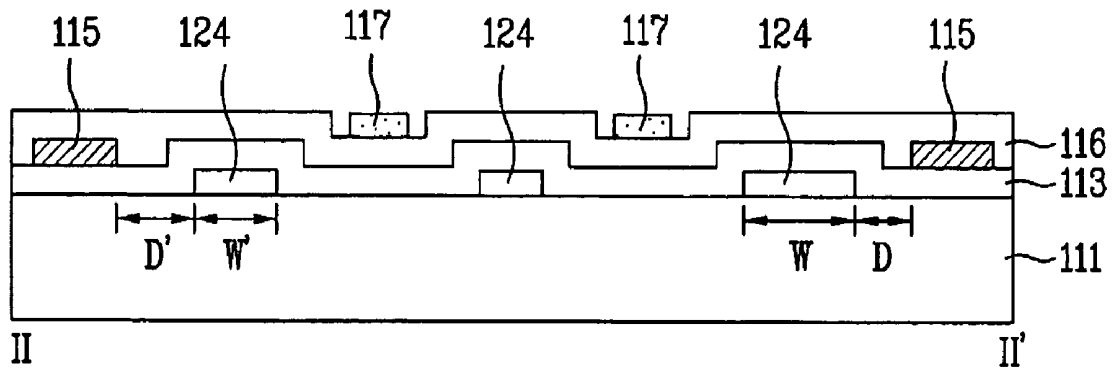


FIG. 9

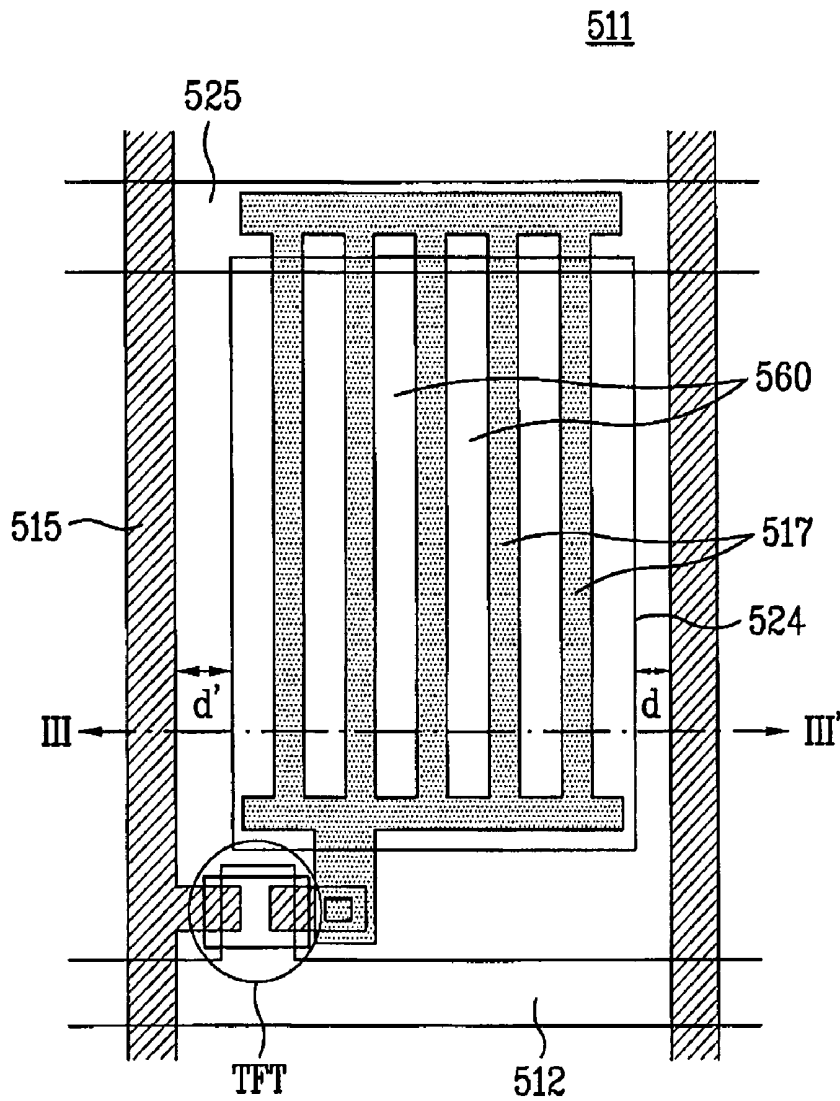


FIG. 10

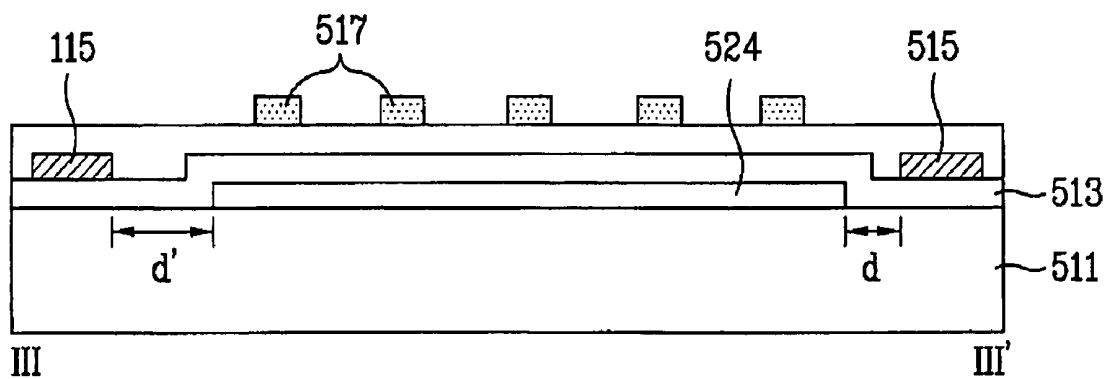


FIG. 11A

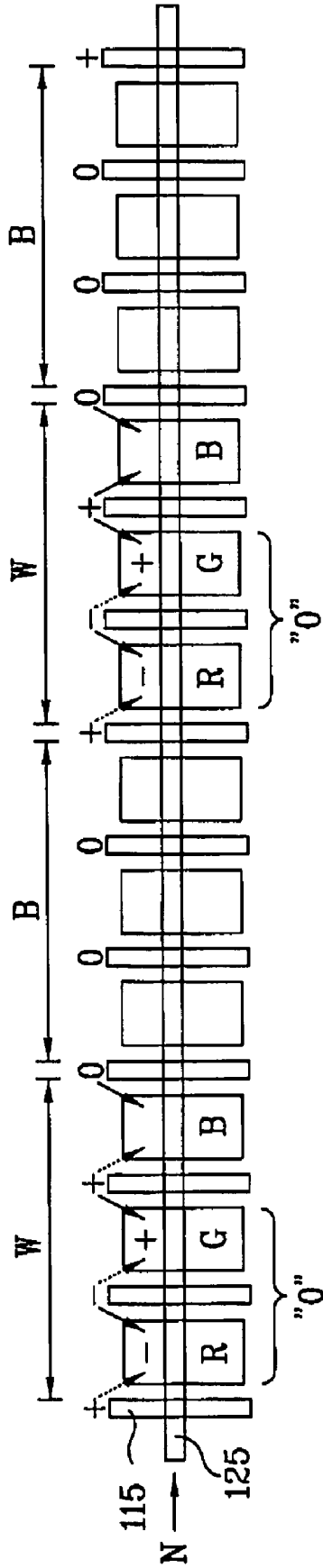
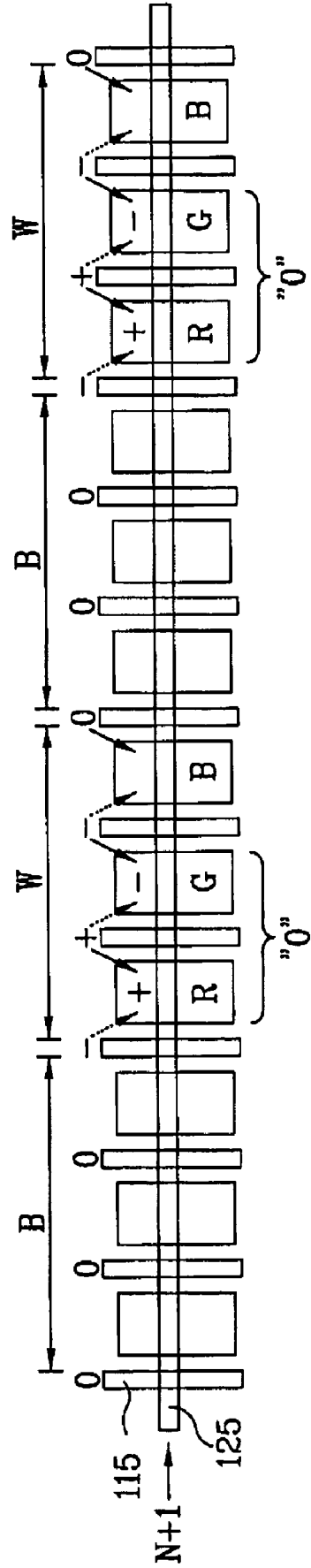


FIG. 11B



## LIQUID CRYSTAL DISPLAY DEVICE

This application claims the benefit of the Korean Patent Application No. 10-2005-123064, filed on Dec. 14, 2005, which is hereby incorporated by reference in its entirety.

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

Embodiments of the invention relate to a display device, and more particularly to a liquid crystal display (LCD) device.

## 2. Discussion of the Related Art

Recently, active matrix LCD devices are widely used in flat TVs, portable computers, monitors, and so on due to their performance capabilities, such as high speed, high contrast and high resolution. Among the active matrix LCD devices, a twisted nematic (TN) mode LCD device is typically used. The TN mode LCD device drives a liquid crystal director twisted at an angle  $90^\circ$  by applying a voltage to two electrodes respectively arranged on two substrates. The TN mode LCD device provides excellent contrast and color reproduction but has a narrow viewing angle.

To solve the problem of narrow viewing angle in the TN mode LCD device, an in-plane switching (IPS) mode LCD device has been developed in which two electrodes are formed on one substrate and a liquid crystal director is controlled by a horizontal electric field generated between the two electrodes. However, the (IPS) mode LCD device has a low aperture ratio and poor transmittance. To improve aperture ratio and transmittance of the IPS mode, a fringe field switching (FFS) mode LCD device has been developed in which a relative electrode and a pixel electrode are positioned such that a liquid crystal director is controlled by a fringe electric field formed between the relative electrode and the pixel electrode.

FIG. 1 is a plan view illustrating a related art IPS mode LCD device, FIG. 2 is a cross-sectional view taken along line I-I' of FIG. 1, FIG. 3 is a plan view illustrating an LCD device driven in a checkerboard pattern, FIG. 4 is a plan view illustrating an LCD device driven in a vertical pattern, FIGS. 5A and 5B illustrate driving of a checkerboard pattern according to the related art, and FIGS. 6A and 6B are timing diagrams illustrating driving of a checkerboard pattern according to the related art.

The related art IPS mode LCD device includes a thin film transistor (TFT) array substrate, a color filter array substrate, and a liquid crystal layer. The TFT array substrate and the color filter array substrate are bonded to each other with a layer of liquid crystal molecules interposed between the two array substrates. As show in FIGS. 1 and 2, the TFT array substrate 11 includes gate lines 12, data lines 15, and thin film transistors. The gate lines 12 vertically cross the data lines 25 to define sub-pixels. Each of the thin film transistors is arranged adjacent to where gate lines 12 and data lines 15 cross. A passivation layer 16 is formed over the TFT array, including the thin film transistors.

Each sub-pixel includes common lines 25, a plurality of common electrodes 24, and a plurality of pixel electrodes 17. The common lines are arranged in parallel with the gate lines 12. The common electrodes 24 extend from the common lines 25 and are arranged in parallel with the data lines 15. The pixel electrodes 17 and the common electrodes 24 are alternately arranged in parallel. The pixel electrodes 17 are connected to the thin film transistors. When a signal  $V_{com}$  is transmitted to the common electrode 24 and a signal  $V_{data}$  passing through the thin film transistor is transmitted to the

pixel electrode 17, a horizontal electric field  $E$  is generated. However, parasitic capacitance  $C_{dc}$  may occur between the data line 15 and the common electrode 24 located in the outmost corner of the sub-pixel.

The color filter array substrate includes red (R), green (G) and blue (B) color filter layers arranged at constant intervals to display colors. A black matrix layer divides R, G and B cells from one another and shields light. The respective R, G, and B color filter layers are formed to collectively correspond to the pixels so that each pixel has at least R, G, and B color sub-pixels. Typically, the sub-pixels having R, G, and B colors are driven independently. A color of one pixel is displayed by combination of the R, G, and B sub-pixels.

The R, G, and B color filter layers are positioned depending on their arrangement method, such as a stripe arrangement, a mosaic arrangement, a delta arrangement, and a quad arrangement. The stripe arrangement, as shown in FIGS. 3 and 4, is when the R, G, and B color filter layers are sequentially arranged in a horizontal direction so as to have the same colors arranged in a vertical direction. The R, G, and B sub-pixels of the aforementioned related art LCD device are all turned on/off to display black (B) or white (W) so as to check picture quality characteristics, such as residual images, flicker, and green tint.

As shown in FIG. 3, the LCD device may be driven in a checkerboard pattern in which an Nth turned-on pixel and an N+1th turned-on pixel are separated by at least one pixel within a line and are offset with respect to turned-on pixels of another line. As shown in FIG. 4, the LCD device may be driven in a vertical pattern in which an Nth turned-on pixel and an N+1th turned-on pixel are arranged at the same position for each line in a vertical direction and are separated by at least one pixel within a line.

In a case where the LCD device is driven in the checkerboard pattern, as shown in FIGS. 5A and 5B, voltages of positive polarity (+) and negative polarity (-) are applied in a horizontal direction by a dot inversion mode and the voltages are applied in a vertical direction by the dot inversion mode through the data line 15. At this time, the LCD device is driven so that white (W) and black (B) of the Nth line are opposite to white (W) and black (B) of the N+1th line in a vertical direction.

Voltages are applied through the data line 15 and the common electrode 24 to turn-on and turn-off sub-pixels. For example, a data voltage  $V_{data}$  is applied to the Nth line in such a manner that voltages of positive polarity (+) and negative polarity (-) are applied by an alternating current (AC) and levels of the data voltage are varied to display black and white while a common voltage  $V_{com1}$  is applied to the Nth line by a direct current (DC). The layer of liquid crystal molecules is driven by the potential difference between the data voltage  $V_{data}$  on the pixel electrode 17 and the common voltage  $V_{com1}$  on the common electrode 24.

As shown in FIGS. 5A and 6A, voltages of high level sequentially having positive polarity (+), negative polarity (-), and positive polarity (+) are applied to the Nth line by a dot inversion mode with respect to R, G, and B sub-pixels so as to display white. On the other hand, either voltage of low level or no voltage is applied to the Nth line by a dot inversion mode with respect to R, G, and B sub-pixels so as to display black.

As shown in FIGS. 5B and 6B, voltages of high level sequentially having positive polarity (+), negative polarity (-), and positive polarity (+) are applied to the N+1th line by a dot inversion mode with respect to R, G, and B sub-pixels so as to display white. On the other hand, either voltages of low

level or no voltages are applied to the N+1th line by a dot inversion mode with respect to R, G, and B sub-pixels so as to display black.

The polarity of the data voltage applied to the Nth line is opposite to the polarity of the data voltage applied to the N+1th line in the dot inversion mode. If the data voltage is applied by a two-dot inversion mode, polarity of the data voltage is opposite to the polarity of the data voltage every two lines. For example, the data voltage V<sub>data</sub> of positive polarity (+), negative polarity (-), and positive polarity (+) is applied to the R, G, and B sub-pixels of the Nth and N+1th lines while the data voltage V<sub>data</sub> of negative polarity (-), positive polarity (+), and negative polarity (-) is applied to the R, G, and B sub-pixels of the N+2th and N+3th lines.

The related art LCD device has several problems. When the data voltage V<sub>data</sub> is applied to the Nth line by an AC voltage and the common voltage V<sub>com1</sub> is also applied thereto by a DC voltage, fluctuation of the common voltage is amplified between the data line 15 and its adjacent common electrode 24 due to interference from the parasitic capacitance C<sub>dc</sub> of a coupling between the data voltage V<sub>data</sub> and the common voltage V<sub>com1</sub>. Thus, as shown in FIGS. 6A and 6B, coupling occurs in which the common voltage V<sub>com1</sub> becomes the common voltage V<sub>com2</sub>, which can be either higher or lower than the actual applied common voltage V<sub>com1</sub>.

As shown in FIG. 5A, in the R sub-pixel of the Nth line, a coupling can be generated between the common electrode and the left data line. More specifically, the common electrode is connected with the common line 25 that carries the common voltage V<sub>com1</sub> and the left data line 15 carries the data voltage V<sub>data</sub> of positive polarity (+) that creates a coupling that offsets a coupling generated between the common electrode and the right data line, which carries the data voltage having a negative polarity (-). In the G sub-pixel of the Nth line, a coupling generated between the common electrode and the left data line, which carries a data voltage having a negative polarity (-), is offset by a coupling generated between the common electrode and the right data line, which carries a data voltage of positive polarity (+). However, in the B sub-pixel of the Nth line, a coupling is generated between the common electrode and the left data line, where carries a data voltage of positive polarity (+), but an offset coupling is not generated between the common electrode and the right data line, which carries a reference voltage flows (0). As a result, in the B sub-pixel of the Nth line, a sufficient offset coupling is not obtained due to the data voltage of positive polarity (+) through the left data line that is not offset.

Fluctuations of the common voltage are amplified in the Nth line due to the non-offset coupling of the Nth line in the B sub-pixel. Thus, as shown in FIG. 6A, the common voltage V<sub>com1</sub> is amplified to a more positive polarity (+) and the V<sub>com1</sub> become a common voltage V<sub>com2</sub>. When the V<sub>com2</sub> flowing in the common line becomes higher than the applied common DC voltage V<sub>com1</sub> due to the non-offset coupling, the voltage difference V<sub>2</sub> between the voltages V<sub>data</sub> and V<sub>com2</sub> applied to the G sub-pixel becomes greater than the voltage difference V<sub>1</sub> between the voltages V<sub>data</sub> and V<sub>com2</sub> applied to the R and B sub-pixels. In this case, a greenish phenomenon occurs in which green is brighter than it should be. This is because rotation of the liquid crystal molecules increases to more strongly display a color as the voltage difference increases.

By contrast, in case of the N+1th line, as shown in FIG. 5B, coupling generated in the R and G sub-pixels is offset but a coupling generated in the B sub-pixel remain due to the data voltage of negative polarity (-) through the left data line. As a result, fluctuation of the common voltage is amplified in the

N+1th line due to the non-offset coupling generated in the B sub-pixel. Thus, as shown in FIG. 6B, the V<sub>com1</sub> is amplified toward a more negative polarity (-) and the V<sub>com1</sub> become a common voltage V<sub>com2</sub>. When the V<sub>com2</sub> flowing in the common line becomes lower than the applied common DC voltage V<sub>com1</sub> due to the non-offset coupling, the voltage difference V<sub>4</sub> between the voltages V<sub>data</sub> and V<sub>com2</sub> applied to the G sub-pixel becomes greater than the voltage difference V<sub>4</sub> between the voltages V<sub>data</sub> and V<sub>com2</sub> applied to the R and B sub-pixels. In this case, a greenish phenomenon occurs in which green is brighter than is should be.

#### SUMMARY OF THE INVENTION

Accordingly, embodiments of the invention are directed to an LCD device that substantially obviates one or more problems due to limitations and disadvantages of the related art.

An object of embodiments of the invention is to provide an LCD device that prevents a greenish phenomenon from occurring.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a liquid crystal display device includes gate and data lines on a first substrate, wherein the gate lines cross the data lines to define sub-pixels, thin film transistors adjacent to where the gate lines cross the data lines, pixel electrodes connected to the thin film transistors, common electrodes at left and right sides of the sub-pixels, wherein a first parasitic capacitance between a first data line arranged at the left side of a first sub-pixel and an adjacent first common electrode is smaller than a second parasitic capacitance between a second data line arranged at the right side of the first sub-pixel and an adjacent second common electrode, and a second substrate bonded to the first substrate with a layer of liquid crystal molecules therebetween.

In another aspect, a liquid crystal display device includes gate and data lines on a first substrate to define sub-pixels, thin film transistors adjacent to where the gate lines cross the data lines, pixel electrodes connected to the thin film transistors, common electrodes at left and right sides of the sub-pixels, wherein a first parasitic capacitance between a first data line arranged at the left side of a first sub-pixel and an adjacent first common electrode is different from a second parasitic capacitance between a second data line arranged at the right side of the first sub-pixel and an adjacent second common electrode, and a second substrate bonded to the first substrate with a layer of liquid crystal molecules therebetween.

It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate

embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

FIG. 1 is a plan view illustrating the related art IPS mode LCD device;

FIG. 2 is a cross-sectional view taken along line I-I' of FIG. 1;

FIG. 3 is a plan view illustrating an LCD device driven in a checkerboard pattern;

FIG. 4 is a plan view illustrating an LCD device driven in a vertical pattern;

FIGS. 5A and 5B illustrate driving of a checkerboard pattern according to the related art;

FIGS. 6A and 6B are timing diagrams illustrating driving of a checkerboard pattern according to the related art;

FIG. 7 is a plan view illustrating an IPS mode LCD device according to an embodiment of the invention;

FIG. 8 is a cross-sectional view taken along line II-II' of FIG. 7;

FIG. 9 is a plan view illustrating an FFS mode LCD device according to an embodiment of the invention;

FIG. 10 is a cross-sectional view taken along line III-III' of FIG. 9; and

FIGS. 11A and 11B illustrate driving of a checkerboard pattern according to an embodiment of the invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

FIG. 7 is a plan view illustrating an IPS mode LCD device according to an embodiment of the invention, and FIG. 8 is a cross-sectional view taken along line II-II' of FIG. 7. As shown in FIGS. 7 and 8, a thin film transistor array substrate **111** of an IPS mode LCD device according to an embodiment of the invention includes gate lines **112** arranged in a row, data lines **115** vertically crossing the gate lines **112** to define R, G, and B sub-pixels, thin film transistors formed adjacent to where the gate lines **112** cross the data lines **115**, common lines **125** arranged in parallel with the gate lines **112**, a plurality of common electrodes **124** connected with the common lines **125** and formed inside the sub-pixels, and pixel electrodes **117** contacting drain electrodes **115b** of the thin film transistors and formed in parallel with the common electrodes **124** to generate an horizontal electric field E. The common electrodes **124** arranged at left and right sides of the sub-pixels have different widths so as to make their respective parasitic capacitance C<sub>dc</sub> different such that the parasitic capacitances C<sub>dc</sub> at the left and right sides of the sub-pixels have different values.

The width W' of the common electrode **124** arranged at the left side of the sub-pixel is smaller than the width W of the common electrode **124** arranged at the right side of the sub-pixel so that the parasitic capacitances C<sub>dc</sub> at the left and right sides of the sub-pixel are different from each other. More specifically, the parasitic capacitance C<sub>dc</sub> between the data line **115** arranged at the right side of the sub-pixel and its adjacent common electrode **124** is greater than the parasitic capacitance C<sub>dc</sub> between the data line **115** arranged at the left side of the sub-pixel and its adjacent common electrode **124**. By increasing the parasitic capacitance C<sub>dc</sub> between the data line **115** arranged at the right side of the sub-pixel and its

adjacent common electrode **124**, sufficient offset coupling can be obtained in each sub-pixel such that a data common voltage is not amplified.

In the alternative, different parasitic capacitances C<sub>dc</sub> at the left and right sides of the sub-pixel can be generated by common electrodes arranged at the left and right sides of the sub-pixel having uniform widths but the distance between a data line and its adjacent common electrode arranged at the left and right sides of the sub-pixel is different. In other words, the distance D' between the data line and its adjacent common electrode arranged at the left side of the sub-pixel is greater than the distance D between the data line and its adjacent common electrode arranged at the right side of the sub-pixel while both data lines have the same width. In yet another alternative, different parasitic capacitances at the left and right sides of the sub-pixel can be obtained by common electrodes having different widths and at different distances from their adjacent common electrode.

Each of the thin film transistors includes a gate electrode **112a** diverged from the gate line **112**, a gate insulating layer **113** formed on the entire surface including the gate electrode **112a**, a semiconductor layer **114** formed on the gate insulating layer **113** above the gate electrode **112a**, and source and drain electrodes **115a** and **115b** respectively formed at both ends of the semiconductor layer **114**. The source electrodes **115a** is diverged from the data line **115**. The pixel electrodes **117** and the common electrodes **124** are alternately formed in the sub-pixel to form an horizontal electric field E. The common electrodes **124** are connected electrically with the common line **125** to receive a signal V<sub>com</sub> from the common line **125** and the pixel electrodes **117** are connected electrically with the drain electrode **115b** to receive a signal V<sub>data</sub> from the drain electrode **115b**.

The gate insulating layer **113** is also interposed between the gate and data lines **112** and **115** to insulate the gate and data lines **112** and **115** from each other. A passivation layer is interposed between the data line and the pixel electrode to insulate the data line and the pixel electrode from each other. The common line **125** and the common electrode **124** can be formed in the same layer as the gate line **112**.

In the alternative, the common line **125** can be formed in the same layer as the gate line **112** while the common electrode can be formed in the same layer as the pixel electrode. In this case, the common electrode provided at the left and right sides of the sub-pixel is formed in the same layer as the gate line. Accordingly, the common electrode provided at the left and right sides of the sub-pixel becomes adjacent to the data lines by interposing the gate insulating layer therebetween. As a result, the parasitic capacitances C<sub>dc</sub> are generated between the common electrode **124** provided at the left and right sides of the sub-pixel, the adjacent data lines **115**, and the gate insulating layer **113** that insulates the common electrode from the adjacent data lines **115**.

FIG. 9 is a plan view illustrating an FFS mode LCD device according to an embodiment of the invention, and FIG. 10 is a cross-sectional view taken along line III-III' of FIG. 9. As shown in FIGS. 9 and 10, a TFT array substrate **511** of the FFS mode LCD device according to an embodiment of the invention includes gate and data lines **512** and **515** formed of metal, vertically crossing each other to define sub-pixels, TFTs adjacent to crossings of the gate lines **512** and the data lines **515**, a single body common electrode **524** formed of a transparent metal inside the sub-pixels, and pixel electrodes **517** connected with the TFTs, overlapping the single body common electrode **524**, and having slits **560** having the same shape.

The distances between the data lines arranged at left and right sides of each sub-pixel and the adjacent portions of the

single body common electrode are different so as to make parasitic capacitance  $C_{dc}$  at the left and right sides of each sub-pixel different. In other words, the distance  $D'$  between the data line 515 arranged at the left side of the sub-pixel and its adjacent common electrode 524 is greater than the distance  $D$  between the data line 515 at the right side of the sub-pixel and adjacent portion of the single body common electrode 524. In this case, the parasitic capacitance between the data lines 515 arranged at the right side of the sub-pixel and its adjacent portion of the single body common electrode 524 is greater than the parasitic capacitance between the data lines 515 arranged at the left side of the sub-pixel and its adjacent portion of the single body common electrode 524. By increasing the parasitic capacitance  $C_{dc}$  between the data line 115 arranged at the right side of the sub-pixel and its adjacent portion of the common electrode 124, sufficient offset coupling can be obtained in each sub-pixel such that a data common voltage is not amplified.

The single body common electrode 524 contacts the common line 525 to receive the signal  $V_{com}$  while the pixel electrode 517 receives a signal  $V_{data}$  that has passed through the TFT. In this case, a fringe electric field occurs between the common electrode 524 and the pixel electrode 517 through the slit 560. Since a gate insulating layer 513 is interposed between the gate line 512 and the data line 515, the parasitic capacitances  $C_{dc}$  are generated between the common electrode 524 provided at the left and right sides of the sub-pixel, the adjacent data lines 515, and the gate insulating layer 513 that insulates the common electrode 524 from the adjacent data lines 515. Because the distances between the common electrode at the left and right sides of the sub-pixel and the adjacent data lines are different, the parasitic capacitances are different.

Although not shown, each of the IPS mode TFT array substrate and the FFS mode TFT array substrate is bonded to a color filter array substrate with a layer of liquid crystal layer molecules therebetween. The color filter array substrate includes a black matrix formed at the sides of the sub-pixel to prevent light leakage from occurring, and R, G, and B color filter layers formed in the black matrix to display colors.

The respective R, G, and B color filter layers are formed to collectively correspond to the pixels so that each pixel has at least R, G, and B color sub-pixels. Typically, the sub-pixels having R, G, and B colors are driven independently. A color of one pixel is displayed by combination of the R, G, and B sub-pixels.

FIGS. 11A and 11B illustrate driving of a checkerboard pattern according to an embodiment of the invention. In the case where the LCD device is driven in a checkerboard pattern, as shown in FIGS. 11A and 11B, data voltages of positive polarity (+) and negative polarity (-) are applied in a horizontal direction by a dot inversion mode and also the data voltages are applied in a vertical direction by the dot inversion mode. The LCD device is driven so that white (W) and black (B) of the Nth line are opposite to white (W) and black (B) of the N+1th line in a vertical direction. Voltages of a high level with a sequence of positive polarity (+), negative polarity (-), and positive polarity (+) are applied to the R, G, and B sub-pixels by the dot inversion mode so as to display white. On the other hand, either voltages of low level or no voltage are applied to the R, G, and B sub-pixels so as to display black.

The data voltage  $V_{data}$  is applied by an alternating current (AC) so as to allow the voltages of positive polarity (+) and negative polarity (-), which can be at different levels to display gray scale. Also, the common signal  $V_{com1}$  is applied by a direct current (DC) voltage. The layer of liquid crystal

molecules is driven by the potential difference between the data voltage on the pixel electrode and the common voltage on the common electrode.

In the case of the R sub-pixel of the Nth line, as shown in FIG. 11A, the parasitic capacitance generated between the common electrode and the left data line that carries the voltage of positive polarity (+) is weaker than the parasitic capacitance generated between the common electrode and the right data line that carries the voltage of negative polarity (-) such that the R sub-pixel maintains an appropriate bias voltage of negative polarity (-). In the case of the G sub-pixel of the Nth line, the parasitic capacitance generated between the common electrode and the left data line that carries a voltage of negative polarity (-) is weaker than the parasitic capacitance generated between the common electrode and the right data line that carries the voltage of positive polarity (+) such that the G sub-pixel maintains an appropriate bias voltage of positive polarity (+). Further, the stronger parasitic capacitance of negative polarity (-) in the R sub-pixel offsets the stronger parasitic capacitance of positive polarity (+) in the G sub-pixel.

In the case of the B sub-pixel of the Nth line, a parasitic capacitance is generated between the common electrode and the left data line that carries the voltage of positive polarity (+) but a coupling is not generated between the common electrode and the right data line where a reference voltage flows. The parasitic capacitance between the common electrode and the left data line is negligible. Accordingly, since the voltage of the common electrode is not amplified in the Nth line, the voltage difference between the common voltage and the data voltage applied to the G sub-pixel becomes the same as the voltage difference between the common voltage and each data voltage applied to the R, B sub-pixels so that the greenish phenomenon does not occur.

In the case of the N+1th line, as shown in FIG. 11B, coupling in the R and G sub-pixels also offset each other and coupling between the left data line applied with the data voltage of negative polarity and its adjacent common electrode in the B sub-pixel remain. But, since a distance between the left data line and its adjacent common electrode is greater than distance between the left data line and its adjacent common electrode in the B sub-pixel, the parasitic capacitance generated between the left data line of the sub-pixel and its adjacent common electrode is negligible, and thus the common voltage is not amplified. As a result, since the common voltage is not shifted, the voltage difference between the common voltage and the data voltage applied to the G sub-pixel becomes the same as the voltage difference between the common voltage and each data voltage applied to the R and B sub-pixels so that the greenish phenomenon does not occur.

While it has been described above that the pixel and common electrodes of the IPS mode LCD device and the pixel electrodes and the slits of the FFS mode LCD device are formed in a vertical direction (data line direction), they can alternatively be formed in a horizontal direction (gate line direction). Also, while embodiments of the invention have been described with regard to an IPS mode LCD device and an FFS mode LCD device, embodiments of the invention are not limited to these types of devices and can be applied to all LCD devices with common electrodes at the sides of the sub-pixel that have a greenish problem due to parasitic capacitance generated between the common electrode and its adjacent data line.

Since the parasitic capacitance between the data lines arranged at the right side of the sub-pixel and its adjacent common electrode becomes greater than the parasitic capacitance between the data lines arranged at the left side of the

sub-pixel and its adjacent common electrode, the common voltage can be prevented from being shifted by coupling between the data line and its adjacent common electrode. Accordingly, since the common voltage applied to the G sub-pixel becomes the same common voltage used for the R and B sub-pixels, the greenish phenomenon does not occur. Thus, an accurate color rendering capability is maintained.

It will be apparent to those skilled in the art that various modifications and variations can be made in the liquid crystal display device of embodiments of the invention without departing from the spirit or scope of the invention. Thus, it is intended that embodiments of the invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display device comprising:  
gate and data lines on a first substrate, wherein the gate lines cross the data lines to define sub-pixels;  
thin film transistors adjacent to where the gate lines cross the data lines;  
pixel electrodes connected to the thin film transistors;  
common electrodes at left and right sides of the sub-pixels, wherein a first parasitic capacitance between a first data line arranged at the left side of a first sub-pixel and an adjacent first common electrode is smaller than a second parasitic capacitance between a second data line arranged at the right side of the first sub-pixel and an adjacent second common electrode; and  
a second substrate bonded to the first substrate with a layer of liquid crystal molecules therebetween,  
wherein both of the common and pixel electrodes have a straight shape, a first distance between the first data line and the first common electrode is greater than a second distance between the second data line and the second common electrode, and a first width of the first common electrode is different from a second width of the second common electrode.
2. The liquid crystal display device as claimed in claim 1, wherein the pixel electrodes and the common electrodes are alternately arranged in parallel.
3. The liquid crystal display device as claimed in claim 2, wherein the liquid crystal layer is driven in an in-plane switching (IPS) mode by an horizontal electric field between the pixel electrode and the common electrode.
4. The liquid crystal display device as claimed in claim 2, wherein the common electrodes are formed in the same layer as the pixel electrodes.

5. The liquid crystal display device as claimed in claim 1, wherein the first width of the first common electrode arranged at the left side of the sub-pixel is smaller than the second width of a second common electrode arranged at the right side of the sub-pixel.

6. The liquid crystal display device as claimed in claim 1, wherein the second substrate includes a red color filter layer, a green color filter layer, and a blue color filter layer, which are formed in each pixel.

7. The liquid crystal display device as claimed in claim 6, wherein the red, green and blue color filter layers are arranged in the order of red, green and blue.

8. The liquid crystal display device as claimed in claim 1, further comprising insulating layers between the data lines and the common electrodes.

9. The liquid crystal display device as claimed in claim 8, wherein the common lines are formed in the same layer as the gate lines.

10. The liquid crystal display device as claimed in claim 1, wherein the common electrodes are connected to common lines.

11. A liquid crystal display device comprising:  
gate and data lines on a first substrate to define sub-pixels;  
thin film transistors adjacent to where the gate lines cross the data lines;  
pixel electrodes connected to the thin film transistors;  
common electrodes at left and right sides of the sub-pixels, wherein a first parasitic capacitance between a first data line arranged at the left side of a first sub-pixel and an adjacent first common electrode is different from a second parasitic capacitance between a second data line arranged at the right side of the first sub-pixel and an adjacent second common electrode; and  
a second substrate bonded to the first substrate with a layer of liquid crystal molecules There between,  
wherein both of the common and pixel electrodes have a straight shape, a first distance between the first data line and the first common electrode is different from a second distance between the second data line and the second common electrode, and an width of the first common electrode is different from an width of the second common electrode.

12. The liquid crystal display device as claimed in claim 11, wherein the pixel electrodes and the common electrodes are alternately arranged in parallel.

\* \* \* \* \*

专利名称(译)	液晶显示装置		
公开(公告)号	<a href="#">US7812910</a>	公开(公告)日	2010-10-12
申请号	US11/638519	申请日	2006-12-14
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG.PHILIPS LCD CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE DO YOUNG		
发明人	LEE, DO YOUNG		
IPC分类号	G02F1/1343		
CPC分类号	G02F1/136286 G02F1/134363 G02F2001/13606		
优先权	1020050123064 2005-12-14 KR		
其他公开文献	US20070132900A1		
外部链接	<a href="#">Espacenet</a> <a href="#">USPTO</a>		

摘要(译)

液晶显示装置包括在第一基板上的栅极线和数据线，其中栅极线与数据线交叉以限定子像素，与栅极线交叉的数据线相邻的薄膜晶体管，与薄膜连接的像素电极晶体管，子像素左侧和右侧的公共电极，其中布置在第一子像素左侧的第一数据线与相邻的第一公共电极之间的第一寄生电容小于第二寄生电容之间的第一寄生电容第二数据线设置在第一子像素和相邻的第二公共电极的右侧，第二基板与第一基板结合，其间具有一层液晶分子。

