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(19) **United States**(12) **Patent Application Publication****Lee et al.**(10) **Pub. No.: US 2008/0143909 A1**(43) **Pub. Date: Jun. 19, 2008**(54) **LIQUID CRYSTAL DISPLAY DEVICE AND
METHOD OF FABRICATING THE SAME**(75) Inventors: **Jung Il Lee**, Gyeonggi-Do (KR);
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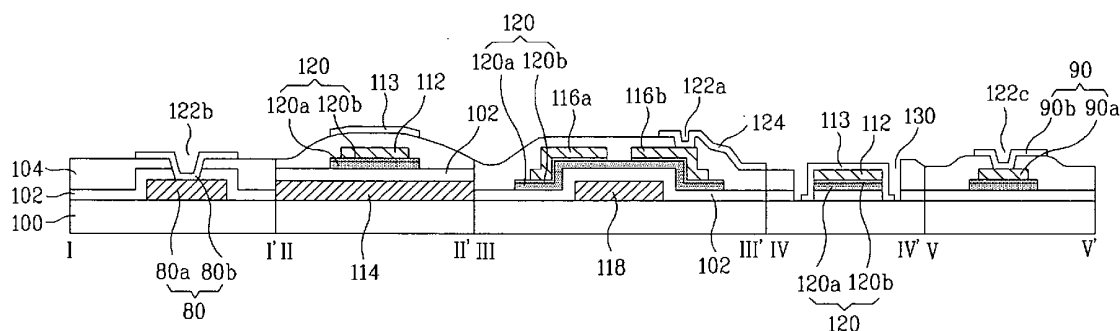
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(52) **U.S. Cl. 349/46; 349/43; 438/151; 257/E21.535**
(57) **ABSTRACT**

An LCD device includes plurality of gate lines and data lines crossing each other to define pixel regions on a substrate. A thin film transistor (TFT) resides at a crossing portion of the gate lines and the data lines and a pixel electrode is electrically connected with the TFT. The TFT includes a gate electrode, a gate insulation layer on the gate electrode and a semiconductor layer on the gate insulation layer. A portion of the data line and the semiconductor layer form a composite layer between adjacent pixel electrodes in which a line width of data line is the same as a line width of semiconductor layer. A method of fabricating the LCD device includes etching a passivation layer using a mask pattern and etching the semiconductor layer using the mask pattern and a portion of the data line as an etch mask to form the composite layer.



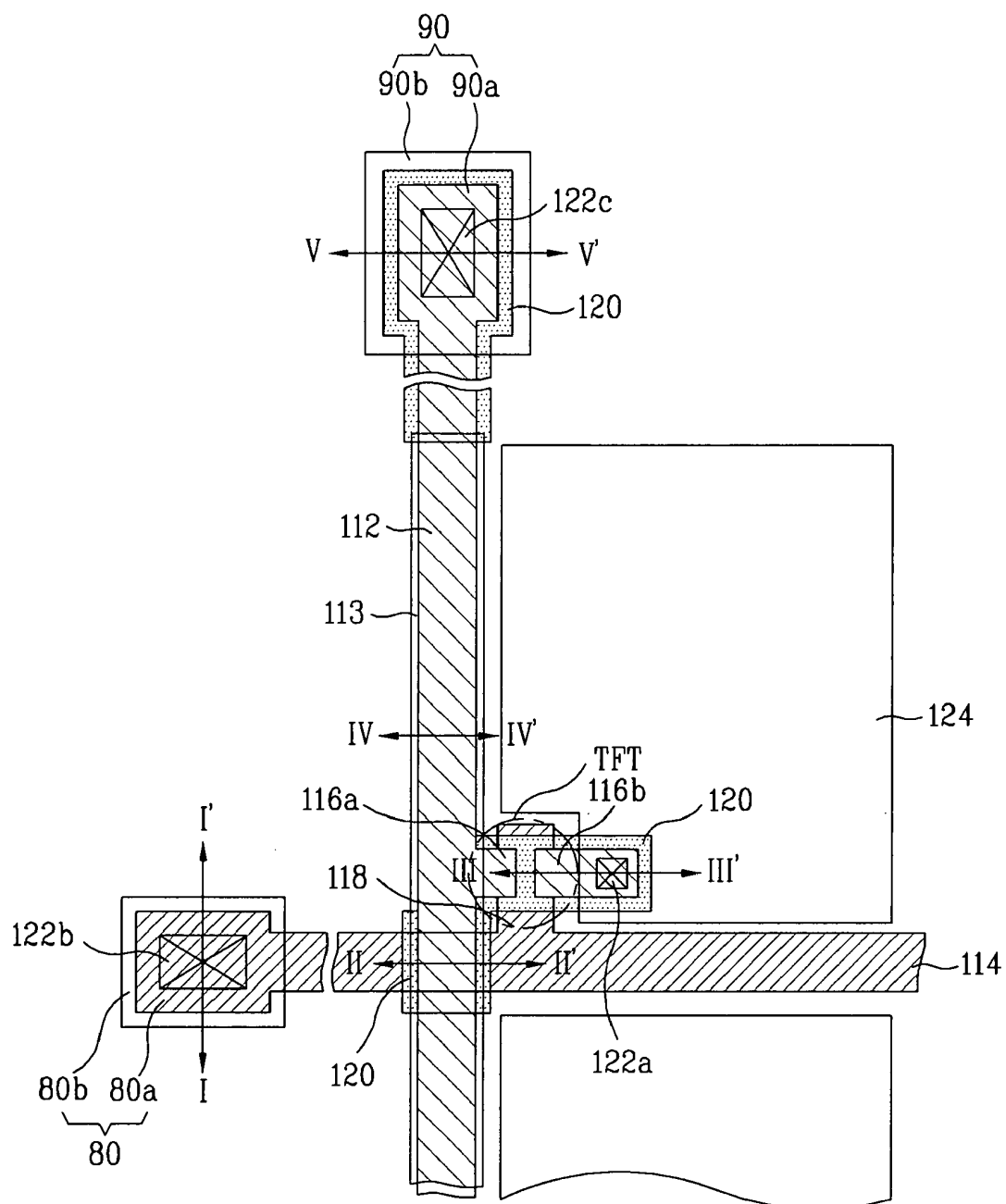


FIG. 3

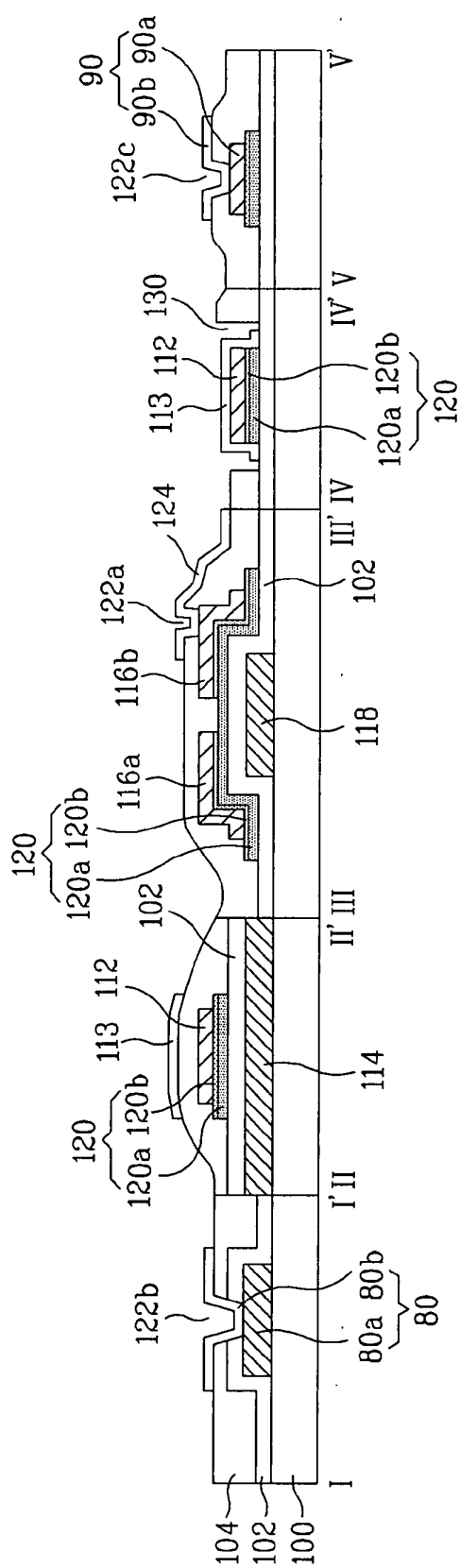


FIG. 4A

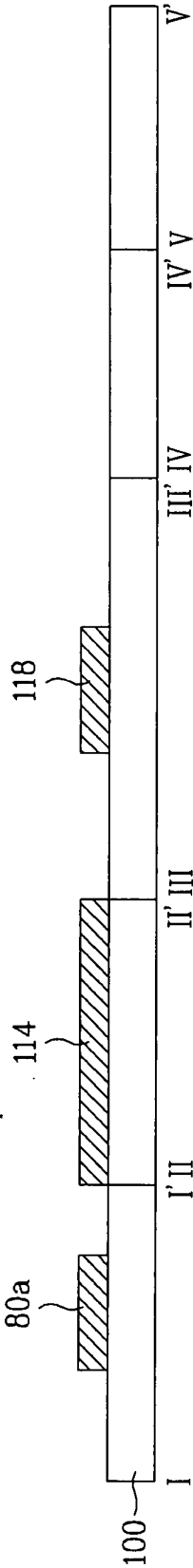


FIG. 4C

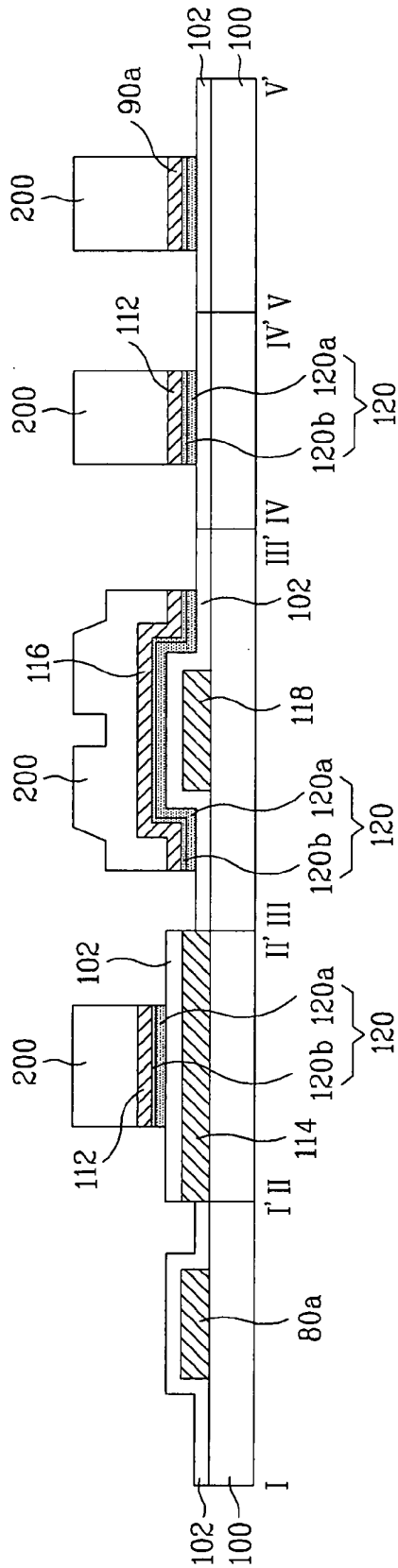


FIG. 4D

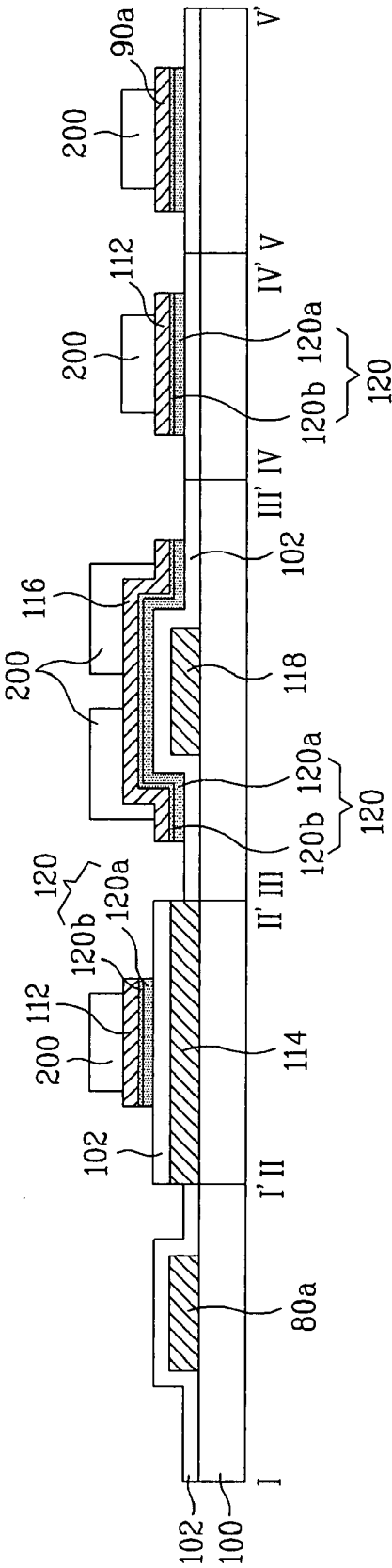


FIG. 4F

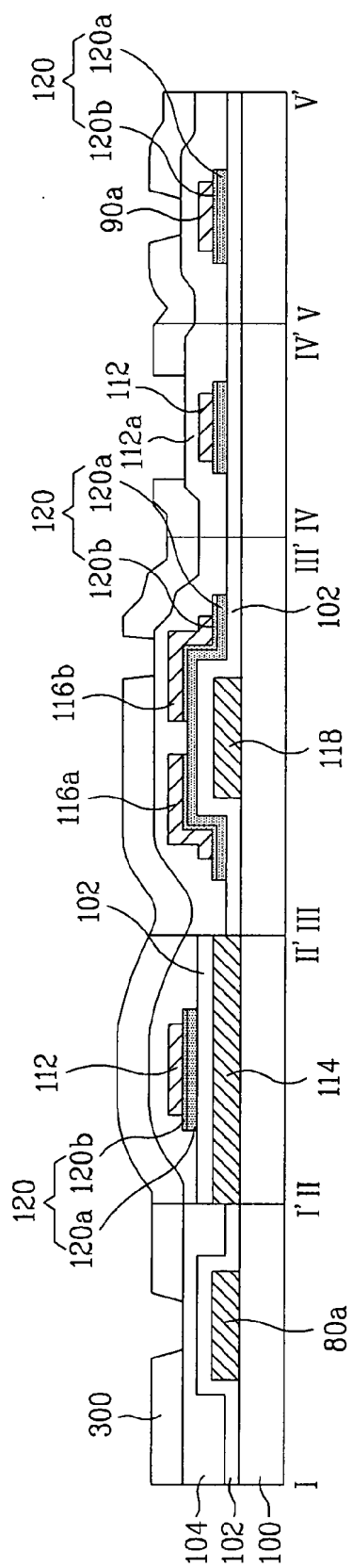
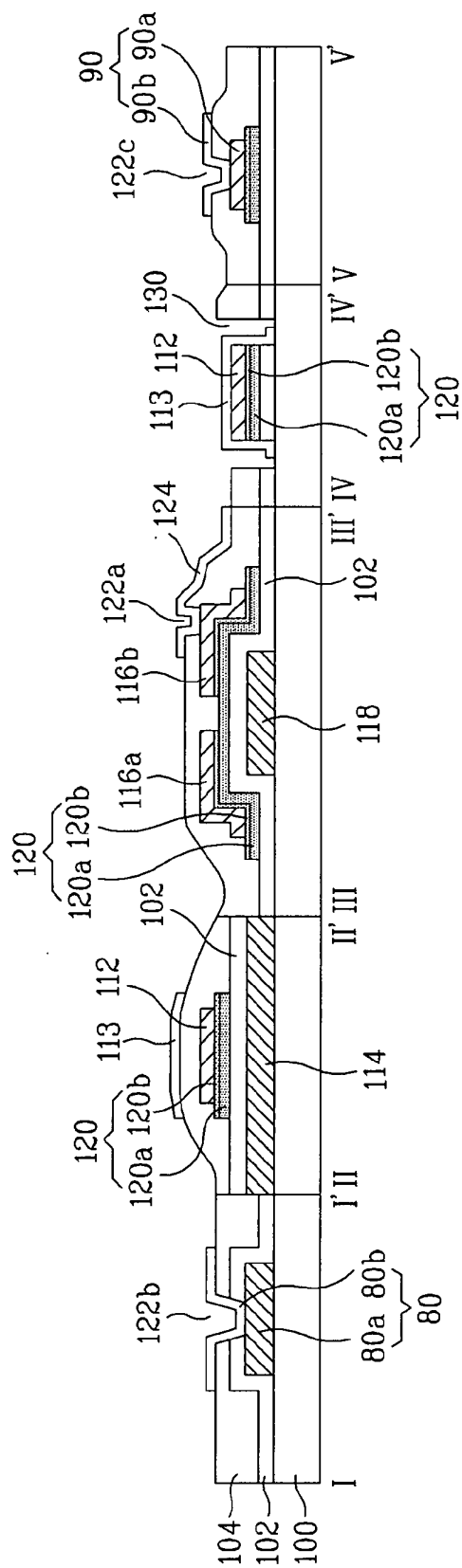


FIG. 4H



LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME

[0001] This application claims the benefit of Korean Patent Application No. 2006-128468 filed on Dec. 15, 2006, which is hereby incorporated by reference as if fully set forth herein.

TECHNICAL FIELD

[0002] The present invention relates to a liquid crystal display (LCD) device and a method of fabricating the same and, more particularly, to an LCD device to improve an aperture ratio by decreasing a line width of semiconductor layer provided below a data line, and a method of fabricating the same.

BACKGROUND

Discussion of the Related Art

[0003] Recently, LCD devices have received increased attention because they offer a high-tech, high-value added product in which the LCD device has low power consumption and good portability.

[0004] Generally, the LCD device includes a thin film transistor array substrate, a color filter array substrate and a liquid crystal layer, wherein the liquid crystal layer is formed between the thin film transistor array substrate and the color filter array substrate.

[0005] The thin film transistor array substrate includes a plurality of gate and lines crossing each other to define a plurality of pixel regions; a plurality of thin film transistors corresponding to switching elements, wherein each thin film transistor is provided adjacent to a crossing portion of the gate and data lines; and a plurality of pixel electrodes respectively formed in the pixel regions.

[0006] The color filter array substrate includes color filters to represent various colors; and a black matrix to divide the color filters and to prevent light leakage.

[0007] The thin film transistor array substrate is fabricated by a plurality of semiconductor processes and mask processes, whereby the fabrication process of the thin film transistor array substrate is complicated, and the fabrication cost thereof is increased.

[0008] Accordingly, a new method has been proposed to decrease the mask processes, wherein a semiconductor layer pattern, a data line pattern and a source/drain pattern including source and drain electrodes are completed by one mask process. That is, a first etching process is provided to form the source/drain pattern and semiconductor layer having the same pattern, and a second etching process is provided to separate the source and drain electrodes from each other.

[0009] Using this method, the semiconductor layer may be fabricated by one etching step. However, the data line positioned on the semiconductor layer is fabricated by two etching steps. Thus, the line width of the data line is smaller than the line width of semiconductor layer positioned under the data line.

[0010] Accordingly, the semiconductor layer protrudes toward the pixel region at both sides of the data line. In order to decrease the influence of parasitic capacitance, the pixel electrode of pixel region is formed at a predetermined distance from the data line and the semiconductor layer. As a

result, the area of pixel electrode is decreased in proportion to the distance that semiconductor layer protrudes beyond the data line.

SUMMARY

[0011] In one embodiment, an LCD device includes a substrate including a plurality of gate lines and a plurality of data lines crossing each other to define a plurality of pixel regions on the substrate. A thin film transistor (TFT) resides at crossing portions of the gate lines and the data lines, each TFT including a semiconductor layer electrically coupled to a corresponding data line and a drain electrode electrically coupled to a pixel electrode. The data lines and the semiconductor layer make a composite line in regions on the substrate between adjacent pixel electrodes in which a line width of the data line is substantially the same as a line width of the semiconductor layer.

[0012] In another embodiment, an LCD device includes a substrate including a gate line and a data line crossing each other to define a pixel region on the substrate. A thin film transistor (TFT) resides at a crossing portion of the gate line and the data line. The TFT includes a gate electrode connected to the gate line, a gate insulation layer overlying the gate electrode, a semiconductor layer overlying the gate insulation layer, a source electrode overlying the semiconductor layer and connected to the data line, and a drain electrode. A pixel electrode connected to the drain electrode, and a portion of the data line overlies a portion of the semiconductor layer in a region adjacent to the pixel electrode where a line width of the data line is substantially the same as a line width of the semiconductor layer in the region adjacent to the pixel electrode.

[0013] In yet another embodiment, a method for fabricating an LCD device includes forming a gate line and a gate electrode on a substrate and sequentially forming a gate insulating layer, a semiconductor layer, and a metal layer overlying the substrate and the gate line and the gate electrode. Source and drain electrodes and a data line are formed and a passivation layer is formed overlying the source and drain electrodes. A mask pattern is formed on passivation layer, in which the mask has an opening over a portion of the data line. The passivation layer is etched using the mask pattern and the semiconductor layer is etched using the mask pattern and a portion of the data line as an etch mask to form a composite layer in which the semiconductor layer and the portion of the data line have substantially the same line width.

[0014] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWING

[0015] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0016] FIG. 1 is a plane view of illustrating an LCD device according to a preferred embodiment of the present invention;

[0017] FIG. 2 is a cross section view of illustrating an alternative embodiment of an LCD device along section lines I-I' to V-V' of FIG. 1; and

[0018] FIG. 3 is a cross section view of illustrating another LCD device along section lines I-I' to V-V' of FIG. 1; and

[0019] FIGS. 4A to 4H are cross section views illustrating a method of fabricating the LCD device shown in FIG. 2.

DETAILED DESCRIPTION

[0020] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0021] FIG. 1 is a plane view of illustrating an LCD device according to a preferred embodiment of the present invention. FIG. 2 is a cross section view of illustrating an LCD device along I-I' to V-V' of FIG. 1.

[0022] As illustrated in FIGS. 1 and 2, the LCD device according to the preferred embodiment of the present invention includes a gate line 114 and a data line 112 crossing each other to define a pixel region on a substrate 100; a thin film transistor (TFT) formed at a crossing portion of the gate line 114 and the data line 112; a pixel electrode 124 electrically connected with the thin film transistor (TFT) through a first contact hole 122a; a gate pad 80 electrically connected with the gate line 114; a data pad 90 electrically connected with the data line 112; a line hole 130 to expose the data line 112 and the periphery thereof; and a data passivation pattern 113 to surround the exposed data line 112. Those skilled in the art will realize that a display device includes many such pixel regions arranged in an array.

[0023] The thin film transistor (TFT) includes a gate electrode 118 diverged from the gate line 114; a gate insulation layer 102 formed on an entire surface of the substrate 100 including the gate electrode 118; a semiconductor layer 120 formed on the gate insulation layer 102 above the gate electrode 118; and source and drain electrodes 116a and 116b diverged from the data line 112 and formed at both sides of the semiconductor layer 120.

[0024] When the data line 112 is positioned on the semiconductor layer 120, a line width of data line 112 is the same as or is smaller than a line width of semiconductor layer 120.

[0025] The semiconductor layer 120 includes an active layer 120a and an ohmic contact layer 120b. The semiconductor layer 120 overlies the gate electrode 118 with the gate insulation layer 102 therebetween, and is also formed below the data line 112 and a data lower pad 90a. Importantly, if the semiconductor layer 120 is positioned below the data line 112 between the adjacent pixel electrodes 124, the line width of semiconductor layer 120 is the same as the line width of data line 112. If the semiconductor layer 120 is positioned at the crossing of the gate line 114 and the data line 112, the line width of semiconductor layer 120 is the same as or is larger than the line width of data line 112. In case of the semiconductor layer 120 below the data lower pad 90a, the line width of semiconductor layer 120 is the same as or is larger than the line width of data lower pad 90a.

[0026] The gate pad 80 includes a lower gate pad 80a extended from the gate line 114; and an upper gate pad 80b electrically connected with the lower gate pad 80a through a second contact hole 122b.

[0027] The data pad 90 includes a lower data pad 90a extended from the data line 112; and an upper data pad 90b electrically connected with the lower data pad 90a through a third contact hole 122c.

[0028] Then, a passivation layer 104 is formed on the source/drain pattern including the source and drain electrodes 116a and 116b, the data line 112 and the lower data pad 90a, wherein the passivation layer 104 exposes the drain electrode 116b, the lower data pad 90a and the data line 112.

[0029] Also, the upper gate pad 80b and the upper data pad 90b are formed on the same layer as the pixel electrode 124, and are formed of the same material as the pixel electrode 124.

[0030] Then, a data protection pattern 113 covers the upper and lateral sides of corresponding data line 112 exposed by the line hole 130 and the lateral side of semiconductor layer 120 positioned below the corresponding data line 112. At this time, the data protection pattern 113 is formed of the same material as that of the pixel electrode 124, and the data protection pattern 113 is formed in the line hole 130.

[0031] By removing the passivation layer 104 and gate insulation layer 102 surrounding the data line 112, the line hole 130 exposes the upper surface of substrate 100 as well as the data line 112.

[0032] In addition, the line hole 130 may be formed as shown in FIG. 3. As shown in FIG. 3, the line hole 130 exposes the data line 112 and the upper surface of gate insulation layer 102 by removing the passivation layer 104 surrounding the data line 112.

[0033] FIGS. 4A to 4H are cross section views illustrating a method of fabricating an LCD device shown in FIG. 2.

[0034] First, as illustrated in FIG. 4A, a gate metal layer is formed on the substrate 100 by a deposition method using sputtering. Then, the gate metal layer is patterned by photolithography, whereby a gate pattern including the gate line 114, the gate electrode 118 and the lower gate pad 80a is formed on the substrate 100.

[0035] Then, as illustrated in FIG. 4B, the gate insulation layer 102, the semiconductor layer 120 including the active layer 120a and ohmic contact layer 120b, and a source and drain metal layer 116 are sequentially formed on the substrate 100 over the gate pattern.

[0036] The gate insulation layer 102 may be formed of an inorganic insulation material of silicon oxide (SiO_x) or silicon nitride (SiN_x). Also, the source and drain metal layer 116 may be formed in a single-layered structure or multi-layered structure of molybdenum (Mo), titanium (Ti), tantalum (Ta), molybdenum alloy (Mo alloy), copper (Cu), aluminum (Al) or aluminum neodymium (AlNd).

[0037] Then, a photoresist layer (not shown) is formed on the source and drain metal layer 116. Thereon, a second mask (not shown) using a diffraction mask or a half-tone mask is provided. In this case, the second mask includes a closed part to block the incident light; a semi-transmission part or diffraction part to transmit the incident light partially; and a transmission part to transmit the incident light.

[0038] As the photoresist layer is exposed and developed using the second mask, a first photoresist pattern 200 is formed at different thicknesses, wherein the first photoresist pattern 200 is positioned on the predetermined portions including the lower data pad 90a, the source and drain electrodes 116a and 116b, and the data line 112. In other words, the predetermined portion of first photoresist pattern 200 to

separate the source and drain electrodes from each other is made relatively thinner. (Indented region shown in FIG. 4B).

[0039] As illustrated in FIG. 4C, the source and drain metal layer 116, except the portion for the source and drain pattern, is removed by wet etching using the first photoresist pattern 200 as a mask. Then, the semiconductor layer 120 except the portion for the semiconductor pattern is removed by the dry etching using the first photoresist pattern 200 as a mask.

[0040] As illustrated in FIG. 4D, the thickness of first photoresist pattern 200 is decreased by ashing. Therefore, the predetermined portion of first photoresist pattern 200 to separate the source and drain electrodes from each other is removed.

[0041] As illustrated in FIG. 4E, the source and drain pattern is wet-etched using the first photoresist pattern 200 as a mask, so that the source and drain electrodes 116a and 116b are separated from each other. Then, the ohmic contact layer 120b exposed by the dry etching is removed. At this time, the source and drain electrode pattern is formed by the wet-etching processes of two times. Thus, the width of data line 112 is smaller than the width of semiconductor layer 120 positioned therebelow, and the width of source and drain electrodes 116a and 116b is smaller than the width of semiconductor layer 120 positioned therebelow.

[0042] For example, if the data line 112 is formed of the dry-etchable metal of molybdenum (Mo), the semiconductor layer 120 positioned below the data line 112 is protruding about 1~3 μm at both sides of the data line 112. In the meantime, if the data line 112 is formed of the wet-etchable metal of copper (Cu), the semiconductor layer 120 positioned below the data line 112 is protruding about 3~5 μm at both sides of the data line 112. In this case, the difference between the line width of semiconductor layer 120 and the line width of data line 112 formed by the wet-etchable metal of copper (Cu) is larger than the difference between the line width of semiconductor layer 120 and the line width of data line 112 formed by the dry-etchable metal of molybdenum (Mo).

[0043] As shown in FIG. 4F, a passivation layer 104 is formed on an entire surface of the substrate including the lower gate pad 80a and the source and drain pattern. The passivation layer 104 may be formed of the inorganic insulation material which is the same as the gate insulation layer 102; the acrylic-based organic compound of which dielectric constant is small; or the organic insulation material of BCB or PFCB.

[0044] Then, a photoresist layer (not shown) is formed on the passivation layer 104, and is then exposed and developed using a third mask. As a result, a second photoresist pattern 300 is formed, which exposes the predetermined portions of passivation layer 104 provided on the lower gate pad 80a, the drain electrode 116b, the data line 112 and the lower data pad 90a.

[0045] As shown in FIG. 4G, the first to third contact holes 122a, 122b and 122c and line hole 130 are formed through an etching process using the second photoresist pattern 300 as a mask. After the etching process, the first contact hole 122a exposes the drain electrode 116b through the passivation layer 104; the second contact hole 122b exposes the lower gate pad 80a through the passivation layer 104 and the gate insulation layer 102; the third contact hole 122c exposes the lower data pad 90a through the passivation layer 104; and the line hole 130 exposes the upper and lateral sides of data line 112 through the passivation layer 104 and gate insulation

layer 102, and exposes the lateral side of semiconductor layer 120 positioned therebelow, and the upper surface of substrate 100.

[0046] An etching process is also carried out to remove portions of the semiconductor layer 120 protruding beyond the data line 112 in area exposed by the line hole 130. By removing the passivation layer 104 exposed by the second photoresist pattern 300; and the semiconductor layer 120 protruding at both sides of the data line 112 when forming the line hole 130, the line width of semiconductor layer 120 positioned below the data line 112 between the adjacent pixel electrodes 124 is identical to the line width of data line 112. Also, the passivation layer remains at the crossing of the gate line 114 and the data line 112, to thereby prevent the semiconductor layer 120 and the gate insulation layer 102 positioned below the data line 112 from being etched.

[0047] In order to form the line hole shown in FIG. 3, a slit mask or a half-tone mask is used. Following is the example using the slit mask. The slit mask is formed of a transmission part corresponding to first to third contact holes 122a, 122b and 122c; a slit part corresponding to the line hole 130; and a closed part corresponding to the passivation layer 104.

[0048] Through the etching process using the photoresist pattern formed by the exposure and development using the slit mask, the first to third contact holes 122a, 122b and 122c are formed and the line hole 130 passing through the passivation layer 104 is formed. When forming the line hole 130, the semiconductor layer 120 protruding at both sides of data line 112 is removed so that the semiconductor layer 120 positioned below the data line has the same line width as that of the data line 122.

[0049] As illustrated in FIG. 4H, the first to third contact holes 122a, 122b and 122c and the line hole 130 are formed. A transparent conductive material (not shown) is deposited on the passivation layer 104 to cover the data line 112. The transparent conductive material may be formed of Indium Tin Oxide (ITO), Tin Oxide (TO), Indium Zinc Oxide (IZO), or Indium Tin Zinc Oxide (ITZO).

[0050] Then, a transparent conductive pattern including the pixel electrode 124, the data protection pattern 113, the upper data pad 90b and the upper gate pad 80b is formed by photolithography and etching using a fourth mask (not shown).

[0051] The data protection pattern 113 covers the lateral side of semiconductor layer 120 and the upper and lateral sides of data line 112 exposed by the line hole 130. Also, the data protection pattern 113 overlies the data line 112 with the passivation layer 104 therebetween where the data line 112 crosses over the gate line 114.

[0052] The data protection pattern 113 is formed to prevent the semiconductor layer 120 and data line 112 exposed by the line hole 130 from being etched by an etchant used when forming the pixel electrode 124.

[0053] As mentioned above, the LCD device according to the present invention and the method of fabricating the same have the following advantages.

[0054] In the LCD device according to the present invention and the method of fabricating the same, the line width of semiconductor layer underlying the data line is decreased so that the area of pixel electrode is increased in proportion to the decreased line width of semiconductor layer, thereby improving the aperture ratio of LCD device.

[0055] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of

the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

1. An LCD device comprising:
 - a substrate including a plurality of gate lines and a plurality of data lines crossing each other to define a plurality of pixel regions on the substrate; and
 - a thin film transistor (TFT) formed at crossing portions of the gate lines and the data lines, each TFT including a semiconductor layer electrically coupled to a corresponding data line and a drain electrode electrically coupled to a pixel electrode,
 - wherein the data lines and the semiconductor layer comprise a composite line in regions on the substrate between adjacent pixel electrodes, and
 - wherein a line width of the data line is substantially the same as a line width of the semiconductor layer in the composite line.
2. The LCD device of claim 1 further comprising a data protection layer covering the composite line.
3. The LCD device of claim 1 further comprising a passivation layer overlying gate lines, the data lines, and the TFT, the passivation layer having a line opening exposing the composite line.
4. The LCD device of claim 1, wherein the composite line extends on the substrate beyond an edge of the pixel electrode to a data pad, and wherein opposite edges of the semiconductor layer protrude beyond opposite edges of the data line at the data pad.
5. The LCD device of claim 4 wherein a position at which the opposite edges of the semiconductor layer protrude beyond the opposite edges of the data line is substantially coincident with the edge of the pixel electrode.
6. An LCD device comprising:
 - a substrate including a gate line and a data line crossing each other to define a pixel region on the substrate;
 - a thin film transistor (TFT) formed at a crossing portion of the gate line and the data line,
 - the TFT including a gate electrode connected to the gate line, a gate insulation layer overlying the gate electrode, a semiconductor layer overlying the gate insulation layer, a source electrode overlying the semiconductor layer and connected to the data line, and a drain electrode; and
 - a pixel electrode connected to the drain electrode,
 - wherein a portion of the data line overlies a portion of the semiconductor layer in a region adjacent to the pixel electrode, and
 - wherein a line width of the data line is substantially the same as a line width of the semiconductor layer in the region adjacent to the pixel electrode.
7. The LCD device of claim 6, wherein the data line and the semiconductor layer extend on the substrate beyond an edge of the pixel electrode to a data pad, and wherein opposite edges of the semiconductor layer protrude beyond opposite edges of the data line at the data pad.
8. The LCD device of claim 7 wherein a position at which the opposite edges of the semiconductor layer protrude beyond the opposite edges of the data line is substantially coincident with the edge of the pixel electrode.
9. The LCD device of claim 6 further comprising a passivation layer overlying gate line, the data line, and the TFT, the

passivation layer having a line opening exposing the portion of the data line in the region adjacent to the pixel electrode.

10. The LCD device of claim 9, wherein the data line and the semiconductor layer and the gate insulation layer comprise a composite layer in the region adjacent to the pixel electrode, the composite layer having a top surface and sidewalls, and wherein a data protection layer overlies the top surface and the sidewalls of the composite layer.

11. The LCD device of claim 9, wherein the data line and the semiconductor layer comprise a composite layer overlying the gate insulation layer in the region adjacent to the pixel electrode, the composite layer having a top surface and sidewalls, and wherein a data protection layer overlies the top surface and the sidewalls of the composite layer.

12. The LCD device of claim 6, wherein the data line, and the source and drain electrodes comprise at least one of molybdenum (Mo), titanium (Ti), tantalum (Ta), molybdenum alloy (Mo alloy), copper (Cu), aluminum (Al) or aluminum neodymium (AlNd).

13. The LCD device of claim 6, wherein the gate insulating layer comprises silicon oxide or silicon nitride,

14. A method for fabricating an LCD device, the method comprising:

- forming a gate line and a gate electrode on a substrate;
- sequentially forming a gate insulating layer, a semiconductor layer, and a metal layer overlying the substrate and the gate line and the gate electrode;

- forming source and drain electrodes and a data line;

- forming a passivation layer overlying the source and drain electrodes, and forming a mask pattern on passivation layer, the mask having an opening over a portion of the data line; and

- etching the passivation layer using the mask pattern and etching the semiconductor layer using the mask pattern and a portion of the data line as an etch mask to form a composite layer in which the semiconductor layer and the portion of the data line have substantially the same line width.

15. The method of claim 14, wherein forming source and drain electrodes comprises:

- forming a photoresist layer on the metal layer and differentially exposing the photoresist layer to form a mask having a thin photoresist portion in a region overlying the gate electrode;

- carrying out a first etching process using the mask to a partially etch the metal layer; and

- carrying out a second etching process using the mask to etch the semiconductor layer.

- wherein the second etching process erodes the thin photoresist portion and etches the metal layer underling the thin photoresist layer to form source and drain electrodes and a data line in which the semiconductor layer protrudes beyond opposite edges of the data line;

16. The method of claim 15, wherein differentially exposing the photoresist layer comprises exposing the photoresist layer using a mask having a closed portion to block incident light, a diffraction portion to partially transmit incident light, and a transmission portion to transmit incident light.

17. The method of claim 15, wherein carrying out a first etching process comprises carrying out a wet etching process and wherein carrying out a second etching process comprises carrying out a dry etching process.

18. The method of claim 17, wherein forming a metal layer comprises forming molybdenum Mo layer, and wherein the

semiconductor layer protrudes about 1 μm to about 3 μm beyond the opposite edges of the data line in the second portion of a data line.

19. The method of claim **17**, wherein forming a metal layer comprises forming a copper (Cu) and wherein the semiconductor layer protrudes about 3 μm to about 5 μm beyond the opposite edges of the data line in the second portion of a data line.

20. The method of claim **14** further comprising:
forming contact holes in the passivation layer;
forming a pixel electrode overlying the passivation layer;
and
forming a data line protection layer covering the composite layer.

* * * * *

专利名称(译)	液晶显示装置及其制造方法		
公开(公告)号	US20080143909A1	公开(公告)日	2008-06-19
申请号	US11/821162	申请日	2007-06-22
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG 飞利浦LCD CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE JUNG IL ROH SEUNG KWANG		
发明人	LEE, JUNG IL ROH, SEUNG KWANG		
IPC分类号	G02F1/136 G02F1/155 H01L21/20		
CPC分类号	G02F1/1368 H01L27/124 H01L27/1288		
优先权	1020060128468 2006-12-15 KR		
其他公开文献	US8018564		
外部链接	Espacenet USPTO		

摘要(译)

LCD装置包括彼此交叉的多条栅极线和数据线，以在基板上限定像素区域。薄膜晶体管（TFT）位于栅极线和数据线的交叉部分，像素电极与TFT电连接。TFT包括栅电极，栅电极上的栅极绝缘层和栅极绝缘层上的半导体层。数据线和半导体层的一部分在相邻的像素电极之间形成复合层，其中数据线的线宽与半导体层的线宽相同。制造LCD器件的方法包括使用掩模图案蚀刻钝化层，并使用掩模图案和数据线的一部分作为蚀刻掩模蚀刻半导体层以形成复合层。

