US 20070268419A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2007/0268419 A1**

Yang (43) **Pub. Date: Nov. 22, 2007**

(54) **ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

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(21) Appl. No.: **11/878,426**

(22) Filed: **Jul. 24, 2007**

Related U.S. Application Data

(62) Division of application No. 11/166,923, filed on Jun. 27, 2005, now Pat. No. 7,256,061.

(30) **Foreign Application Priority Data**

Aug. 3, 2004 (KR) 10-2004-0061047

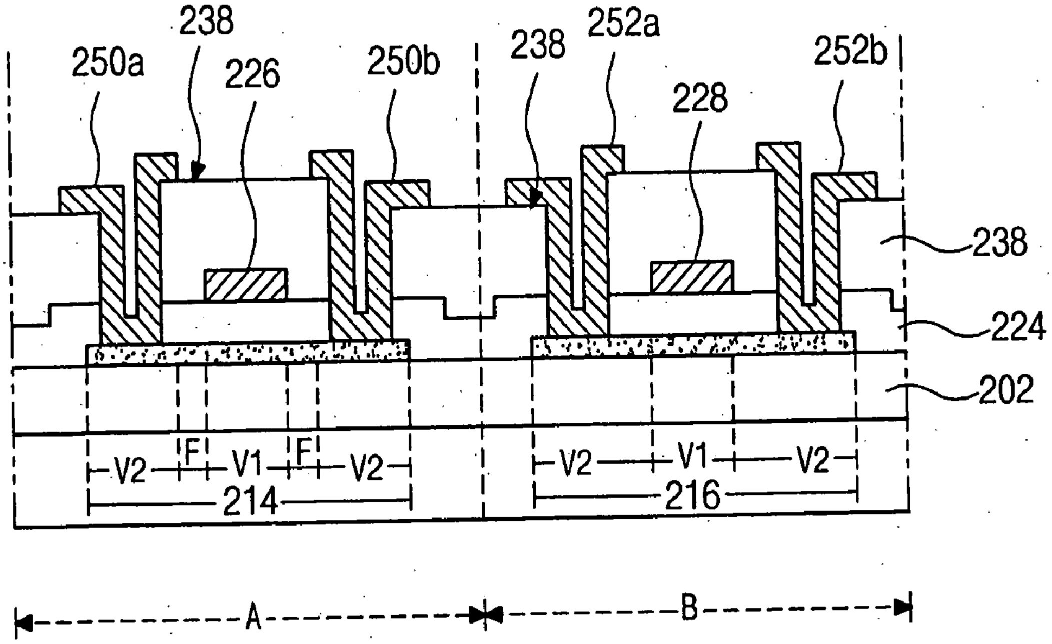
Publication Classification

(51) **Int. Cl.**
G02F 1/1343 (2006.01)

(52) **U.S. Cl.** **349/39**

(57) **ABSTRACT**

An array substrate for a liquid crystal display device includes a substrate including a first driving region, a second driving region, and a pixel region, the pixel region including a switching region and a storage region; a first n-type transistor in the first driving region, a second p-type transistor in the second driving region; a third transistor in the switching region, the third transistor including a gate electrode, an active layer, a source electrode, and a drain electrode; an extension portion in the storage region and extending from the active layer; a metal pattern on the extension portion; a storage line over the metal pattern; and a pixel electrode in the pixel region and contacting the third transistor, wherein the metal pattern, the storage line and the pixel electrode form first, second and third electrodes of a storage capacitor that includes a first capacitor and a second capacitor parallel to each other.



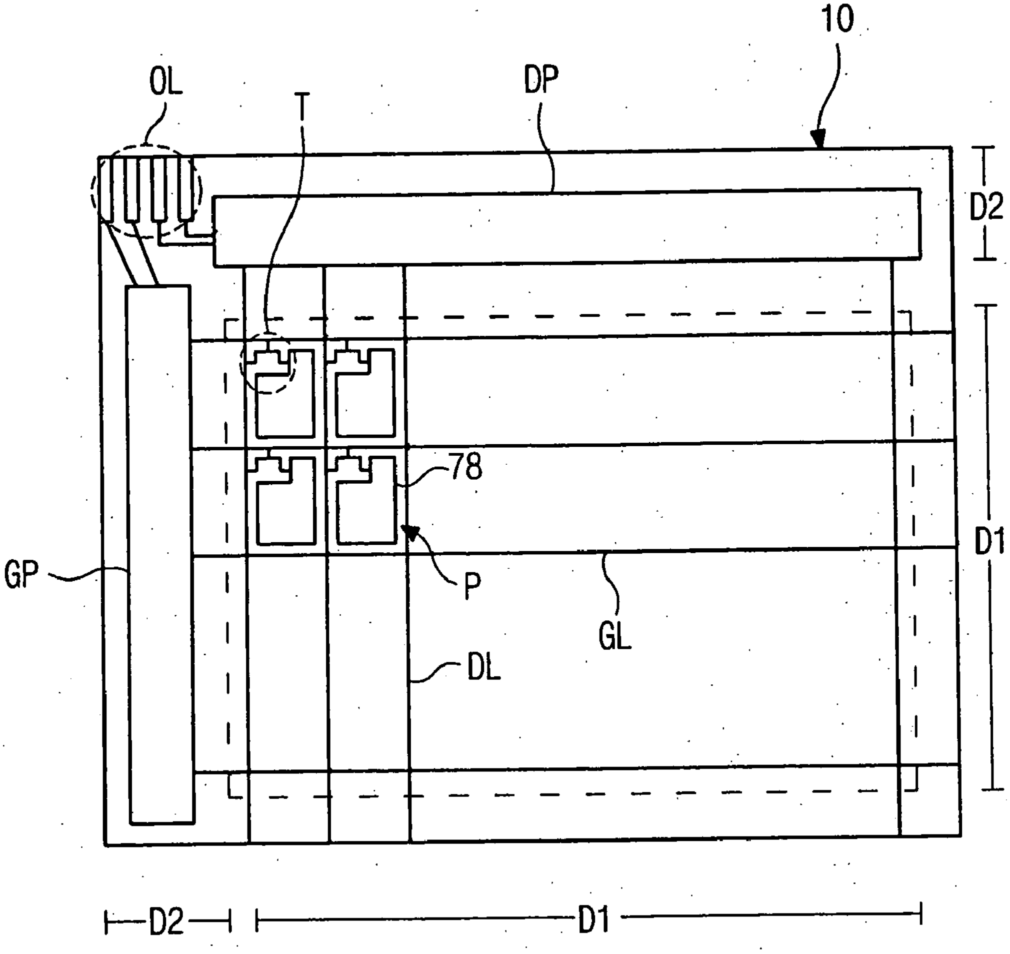


FIG. 1

(RELATED ART)

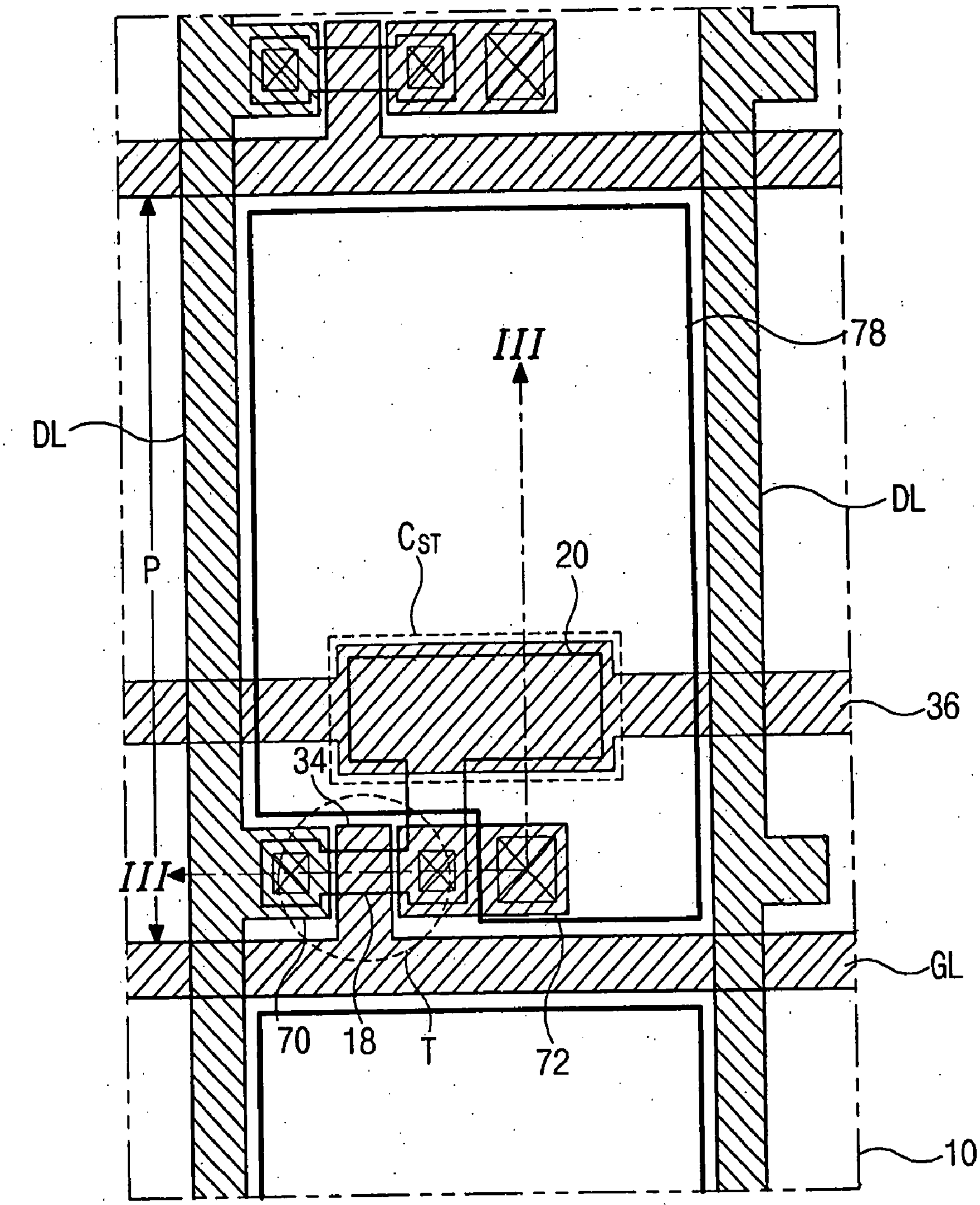


FIG. 2

(RELATED ART)

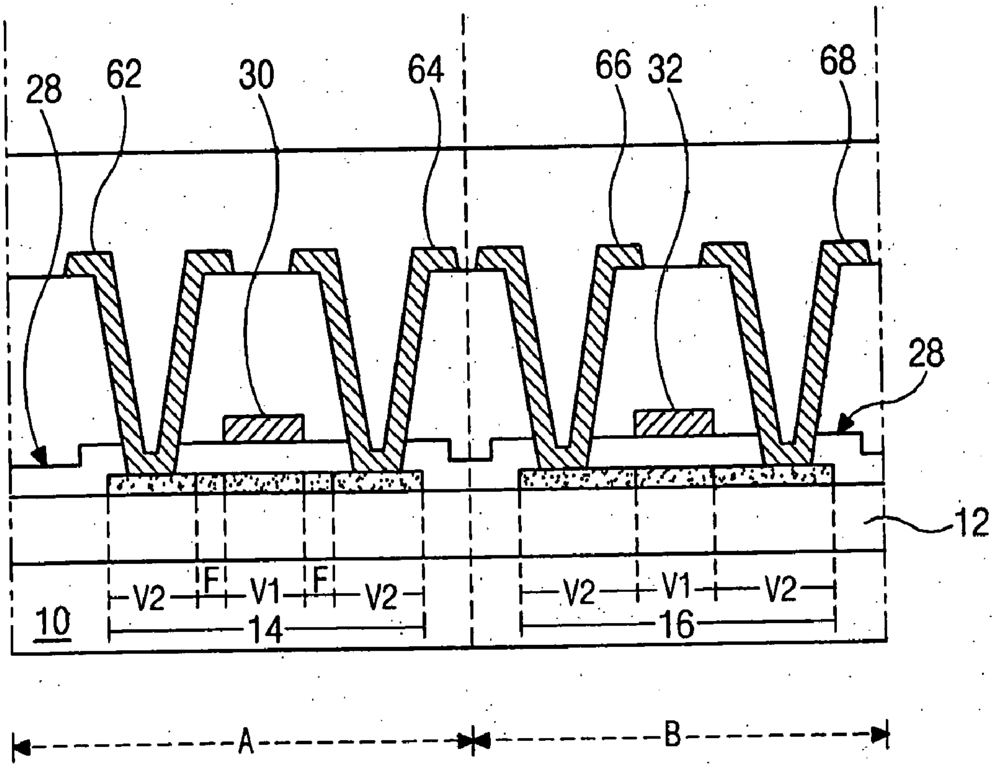


FIG. 3A
(RELATED ART)

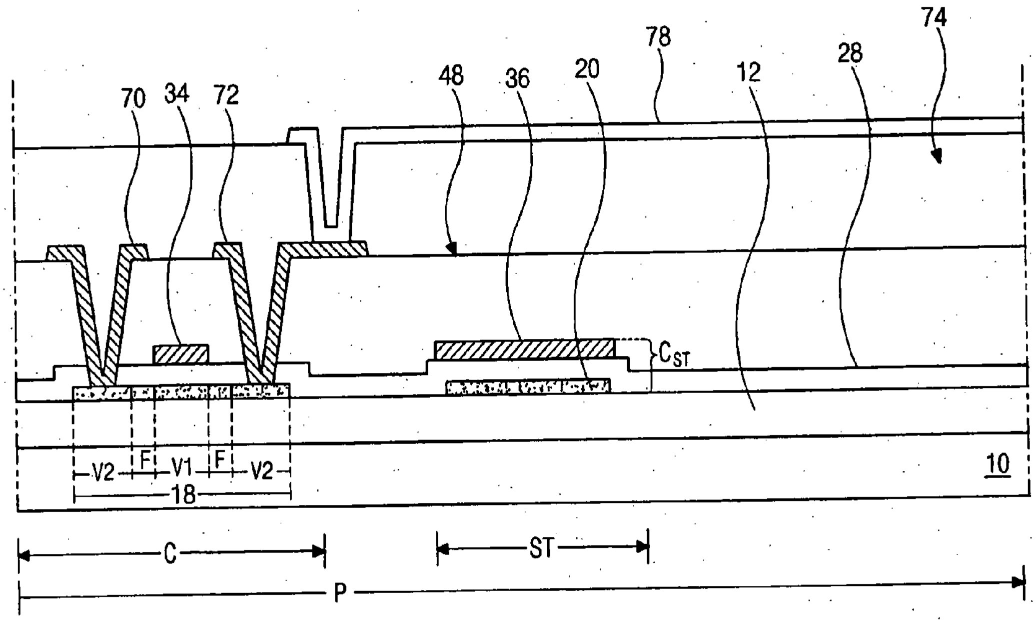


FIG. 3B

(RELATED ART)

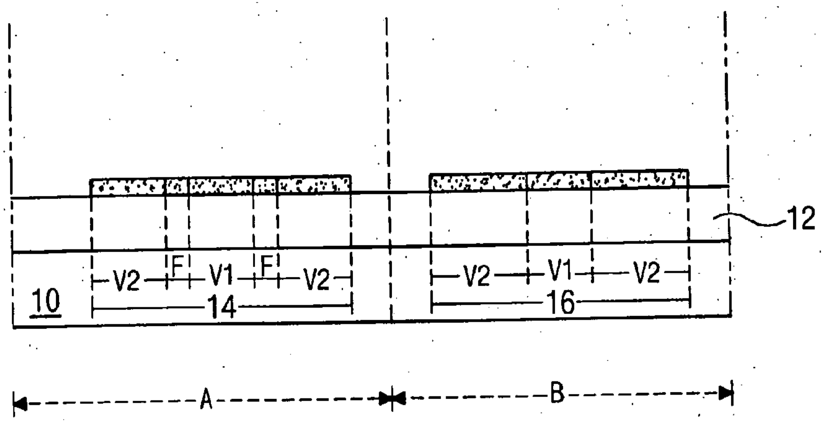


FIG. 4A
(RELATED ART)

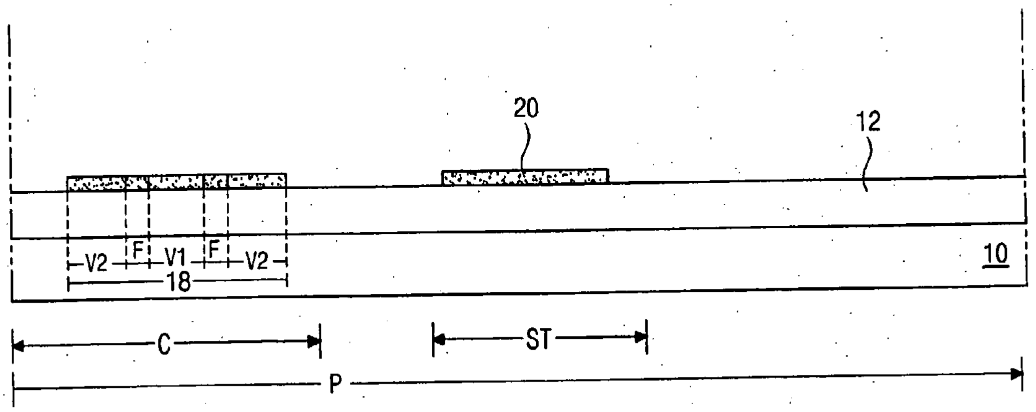


FIG. 4B
(RELATED ART)

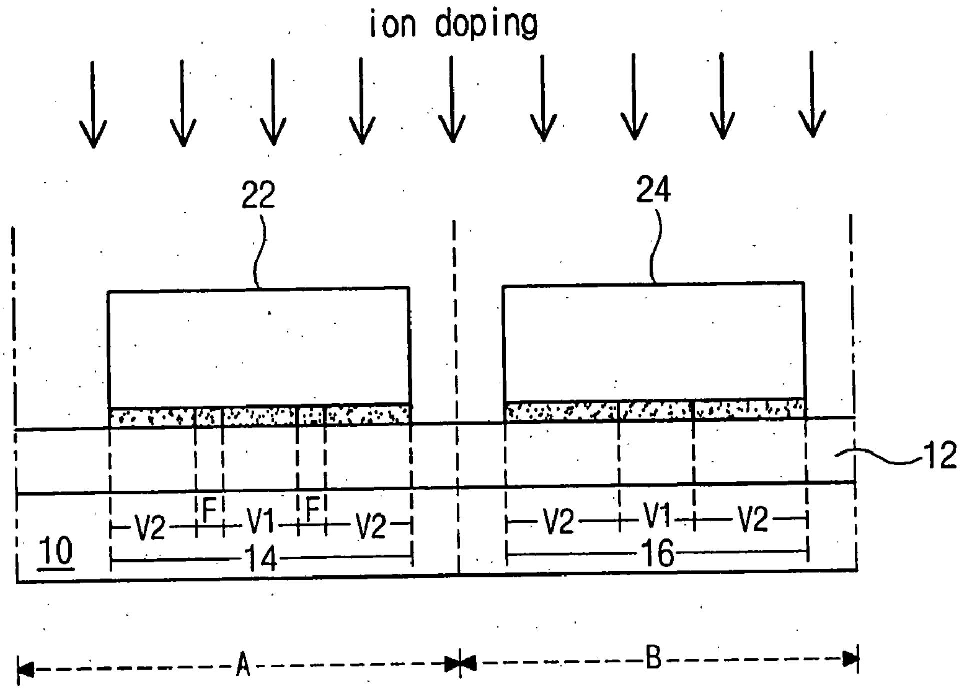


FIG. 5A

(RELATED ART)

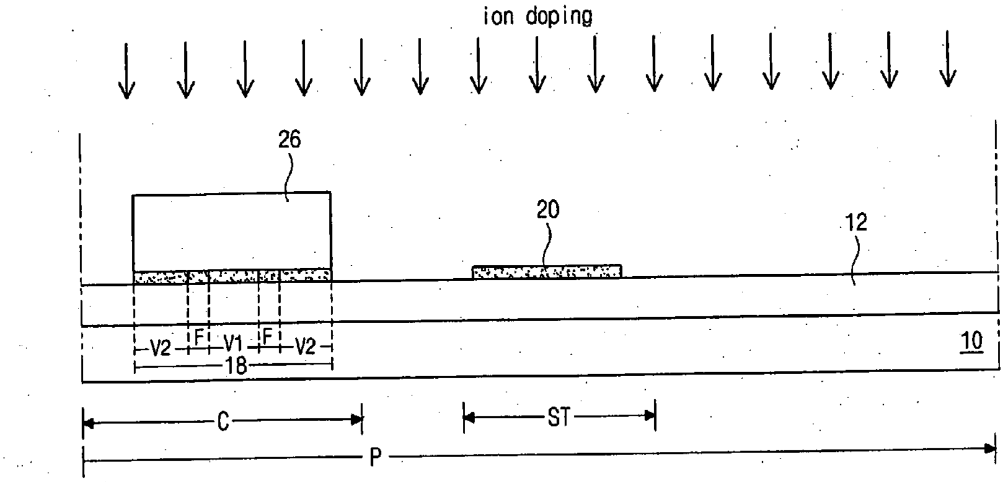


FIG. 5B

(RELATED ART)

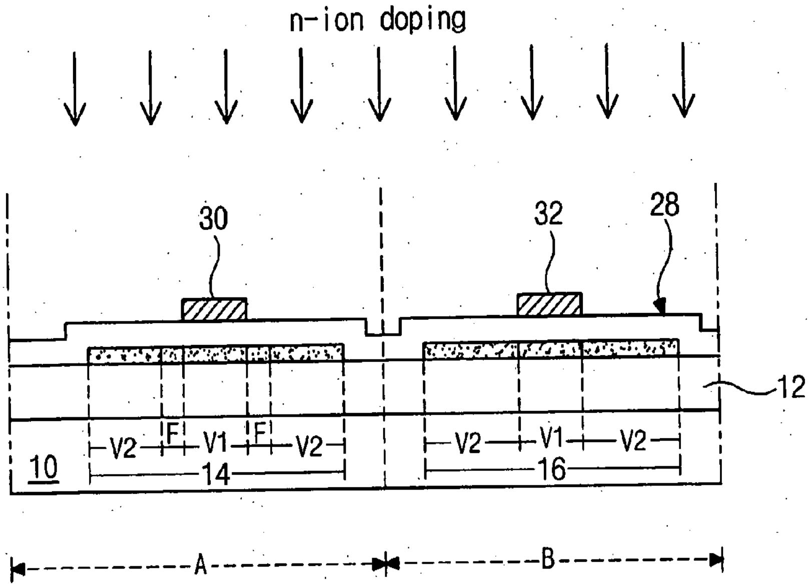


FIG. 6A

(RELATED ART)

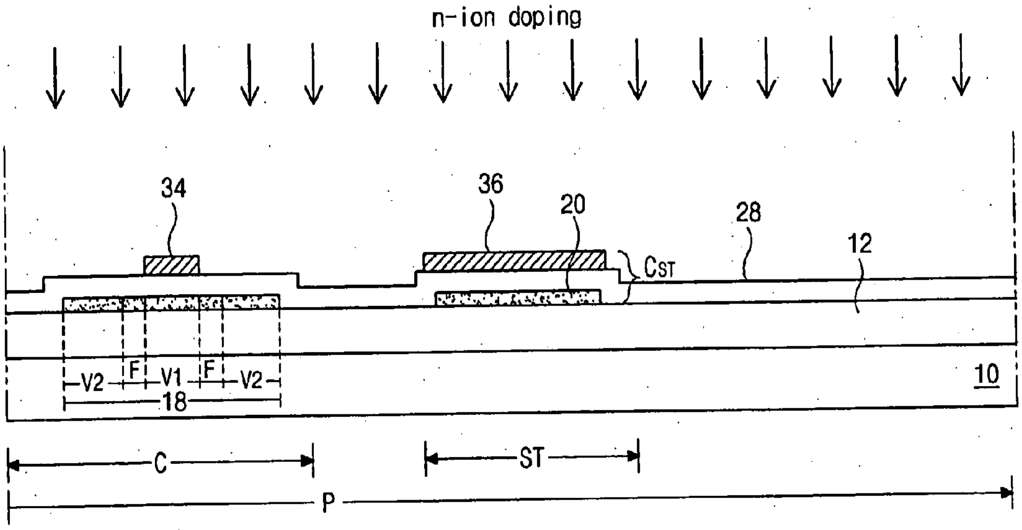


FIG. 6B

(RELATED ART)

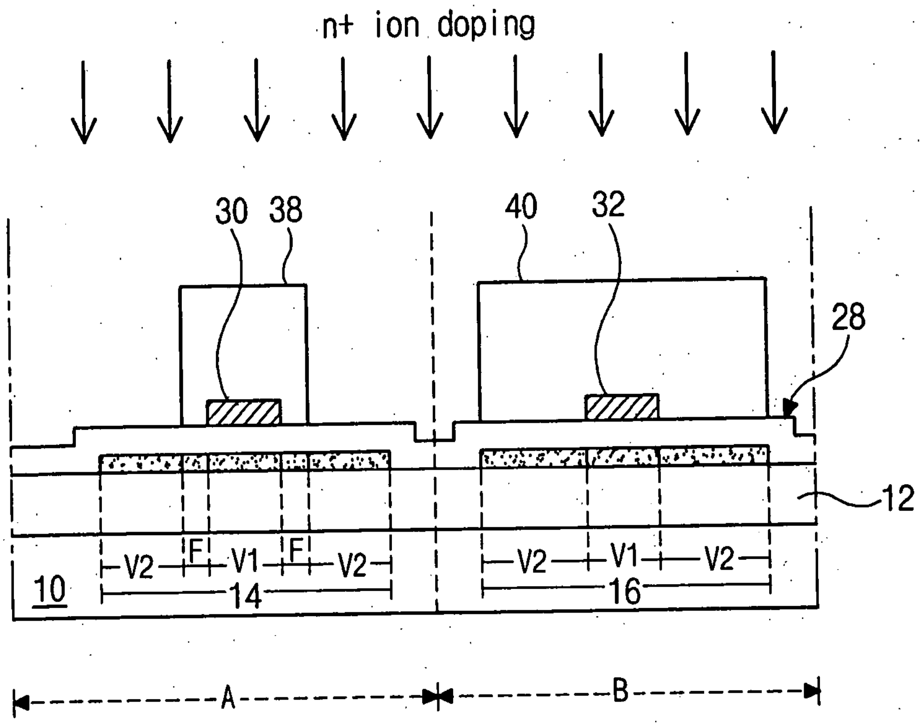


FIG. 7A

(RELATED ART)

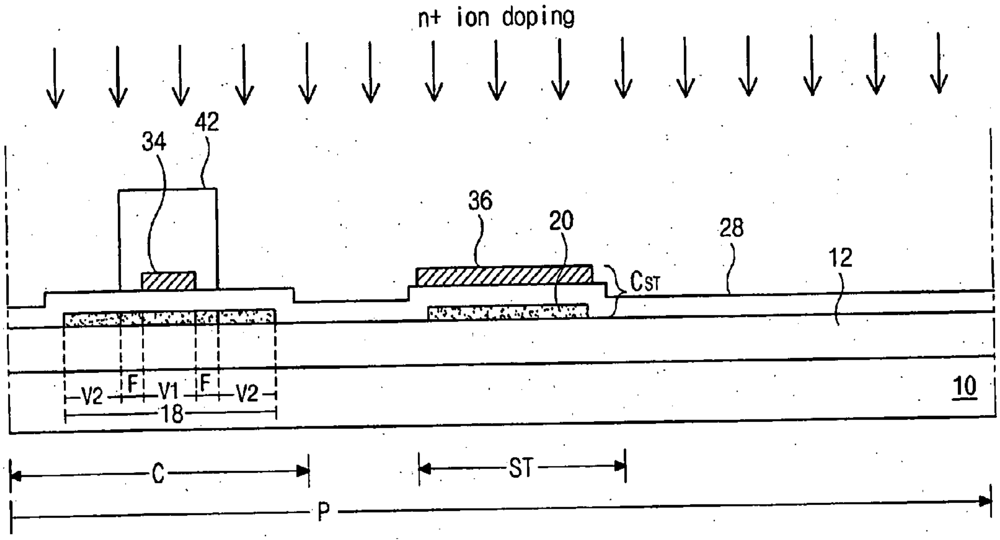


FIG. 7B

(RELATED ART)

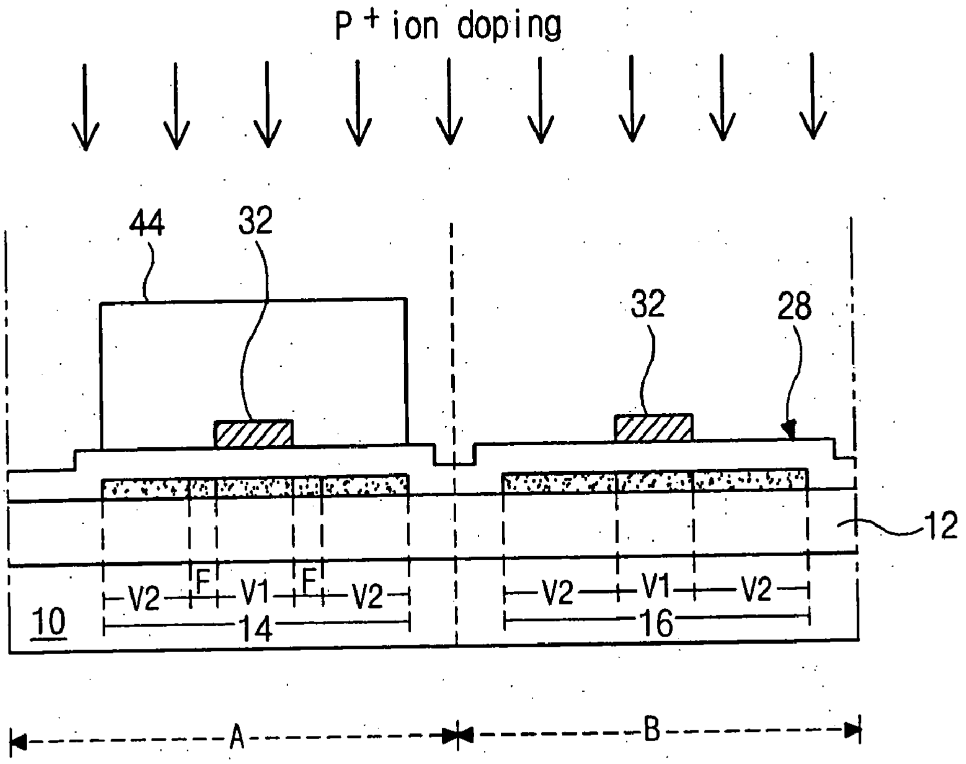


FIG. 8A

(RELATED ART)

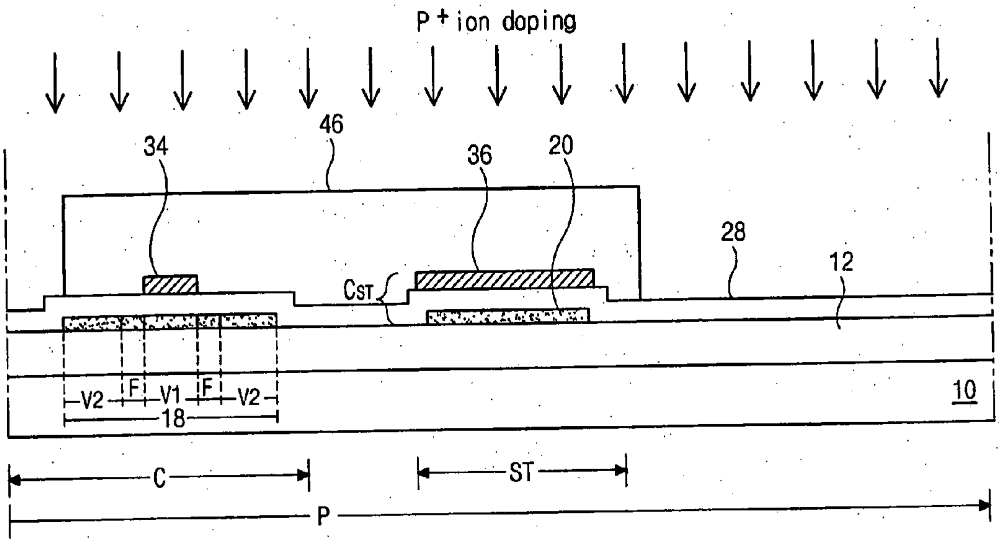


FIG. 8B

(RELATED ART)

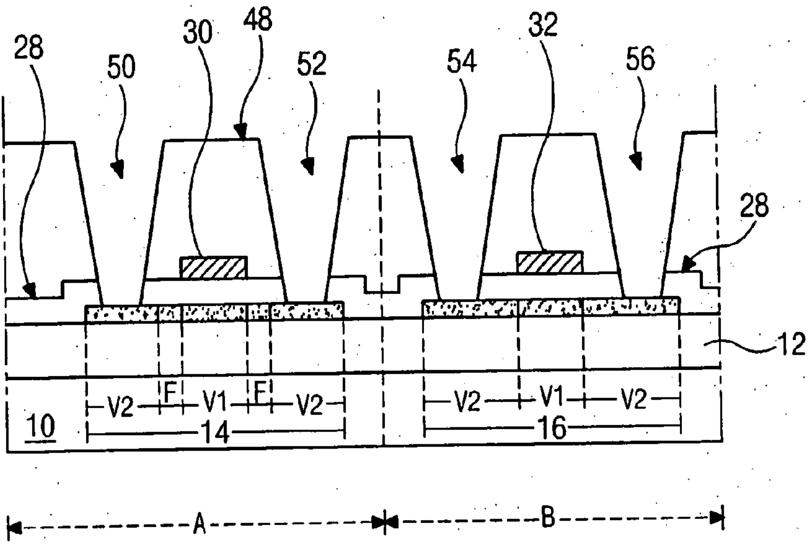


FIG. 9A

(RELATED ART)

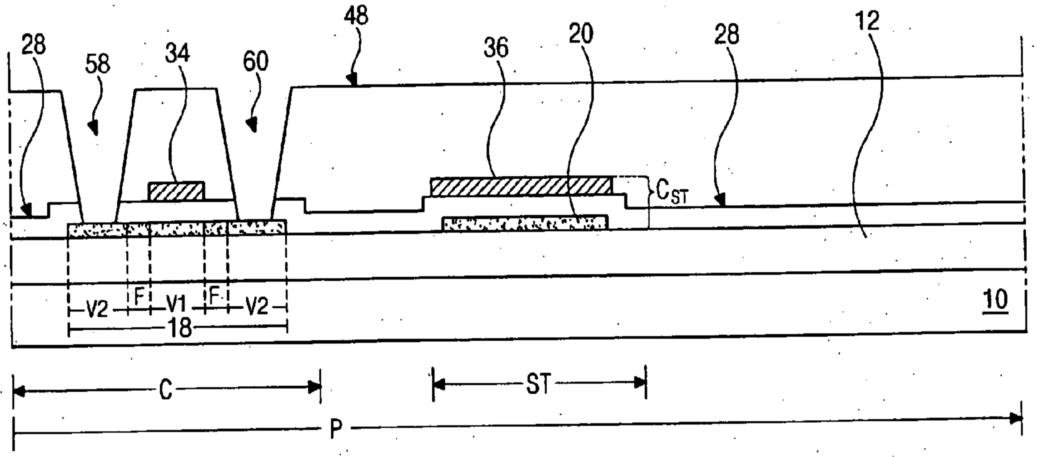


FIG. 9B

(RELATED ART)

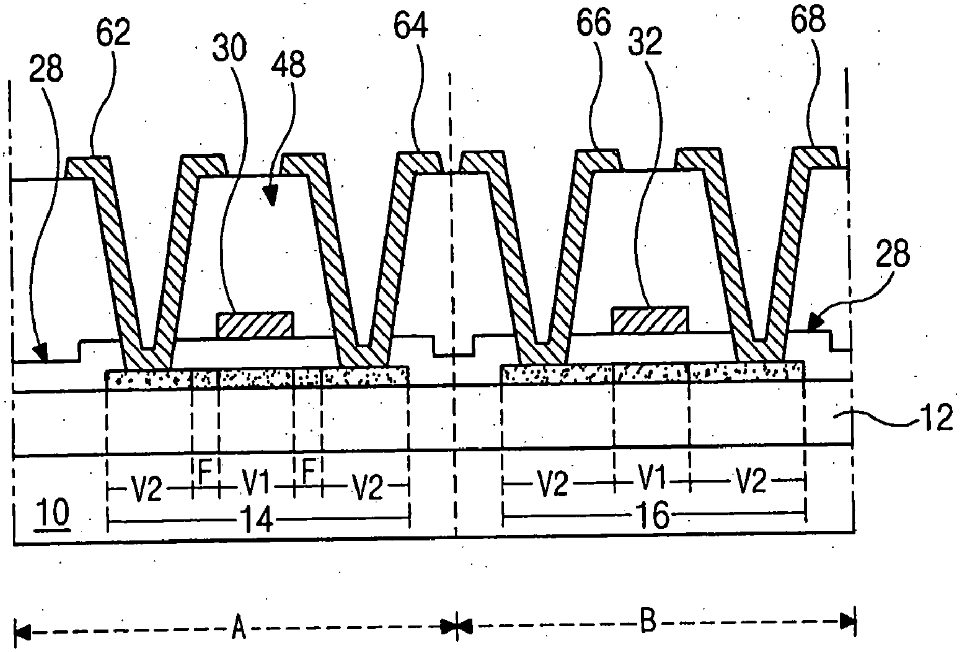


FIG. 10A

(RELATED ART)

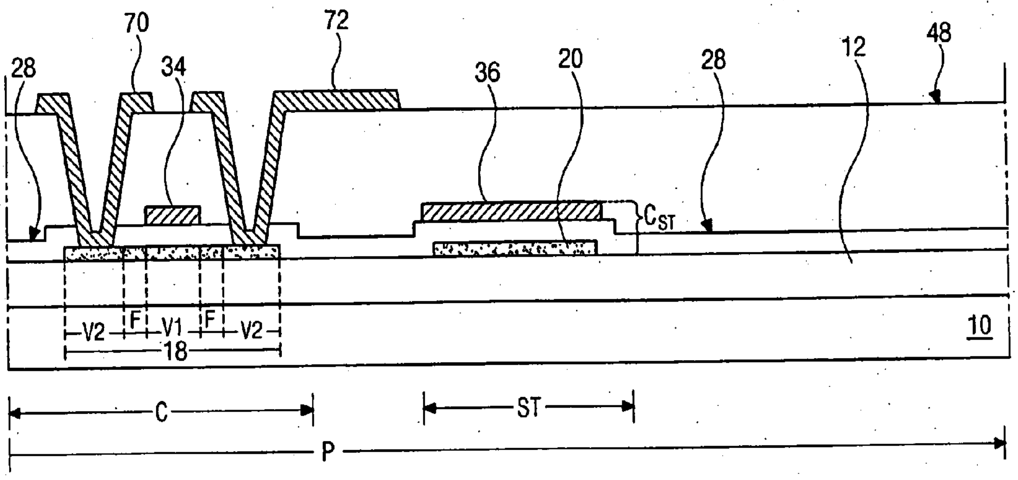


FIG. 10B

(RELATED ART)

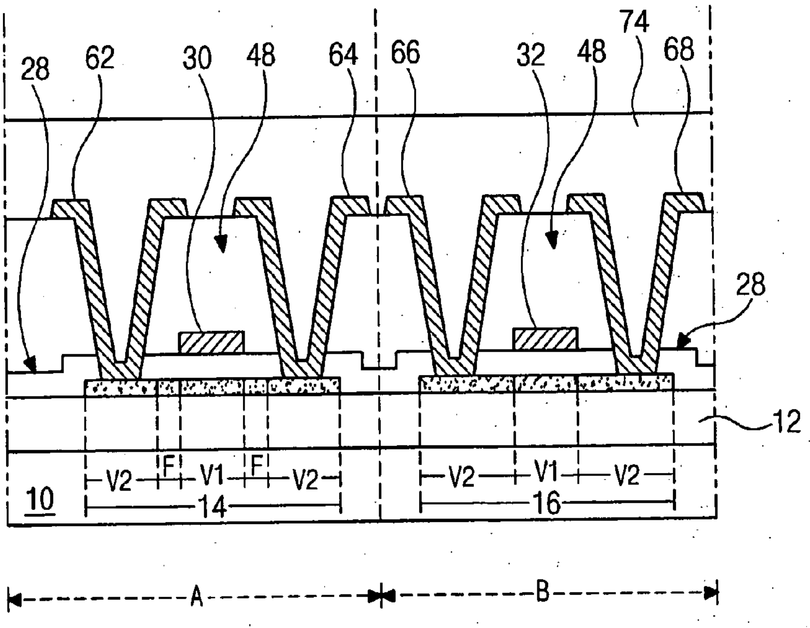


FIG. 11A

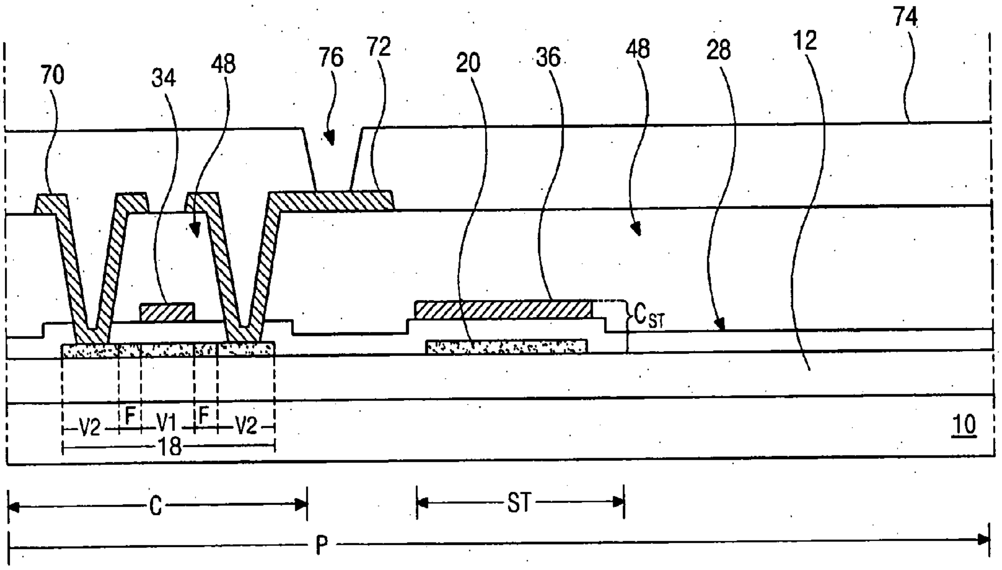


FIG. 11B

(RELATED ART)

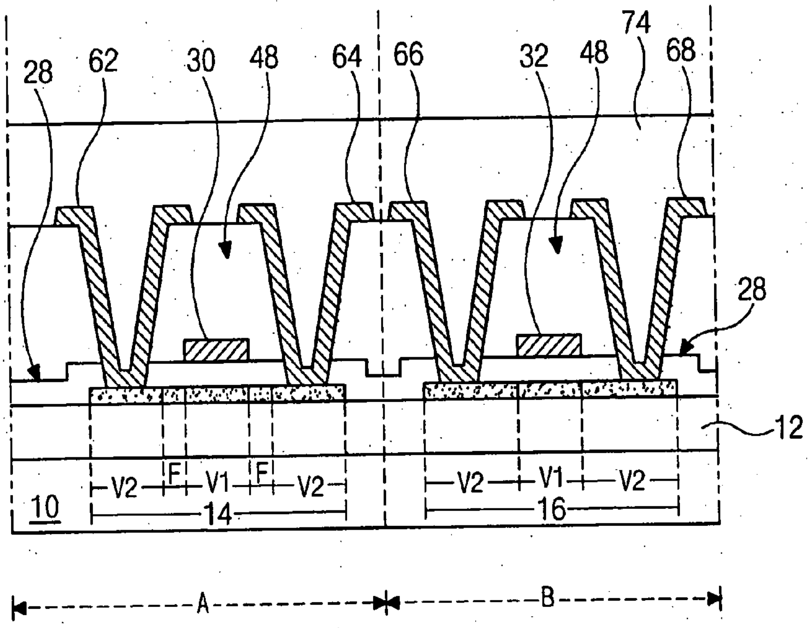


FIG. 12A

(RELATED ART)

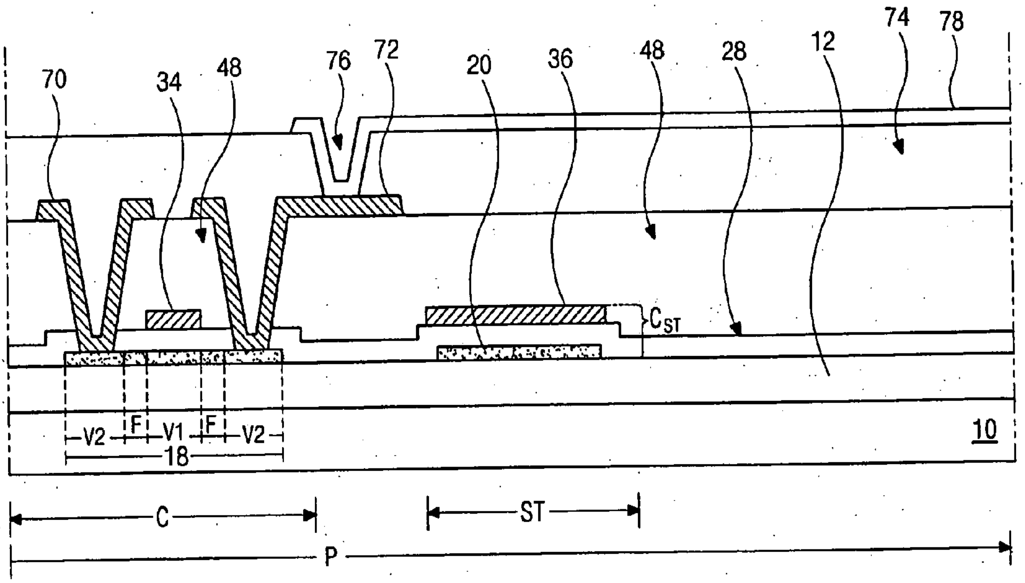


FIG. 12B

(RELATED ART)

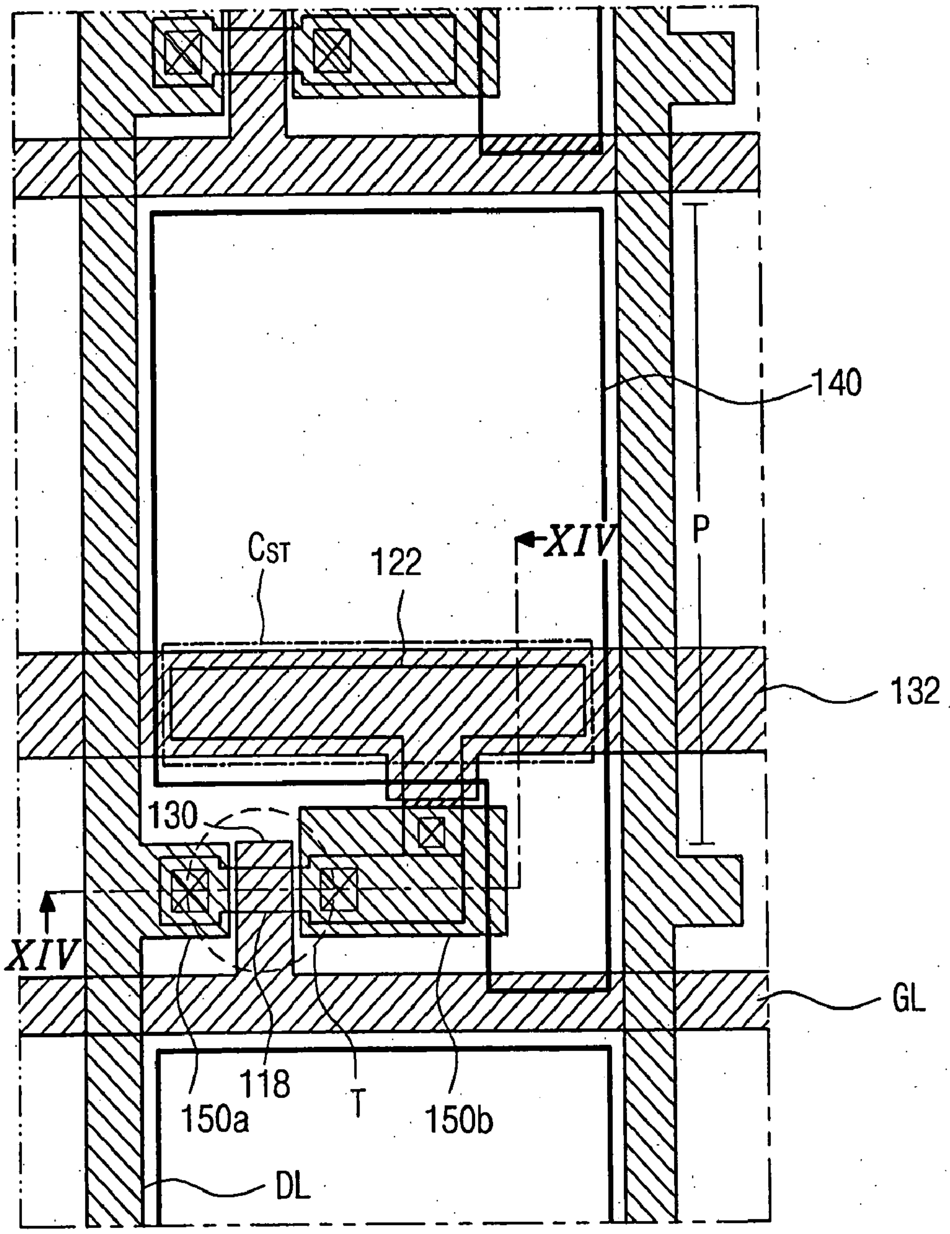


FIG. 13

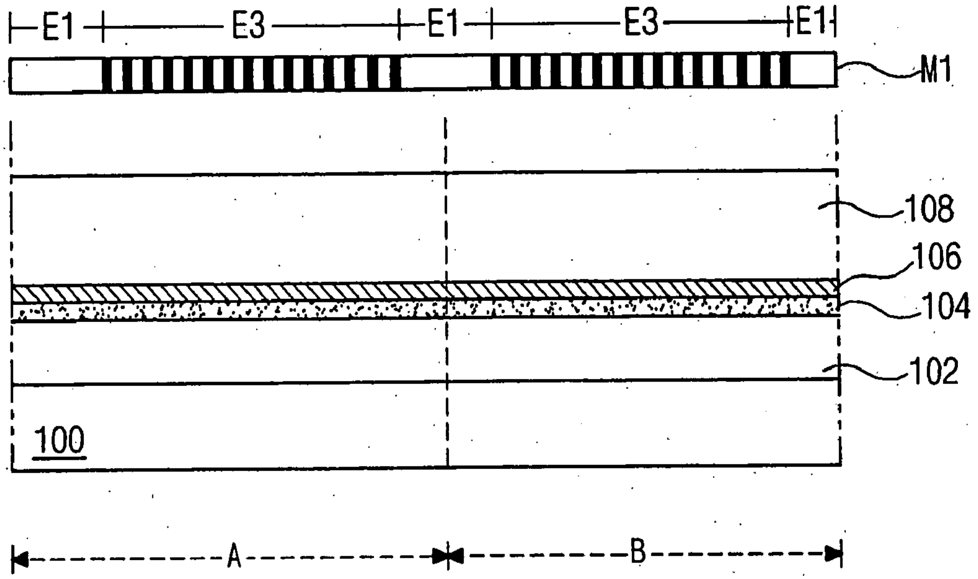


FIG. 14A

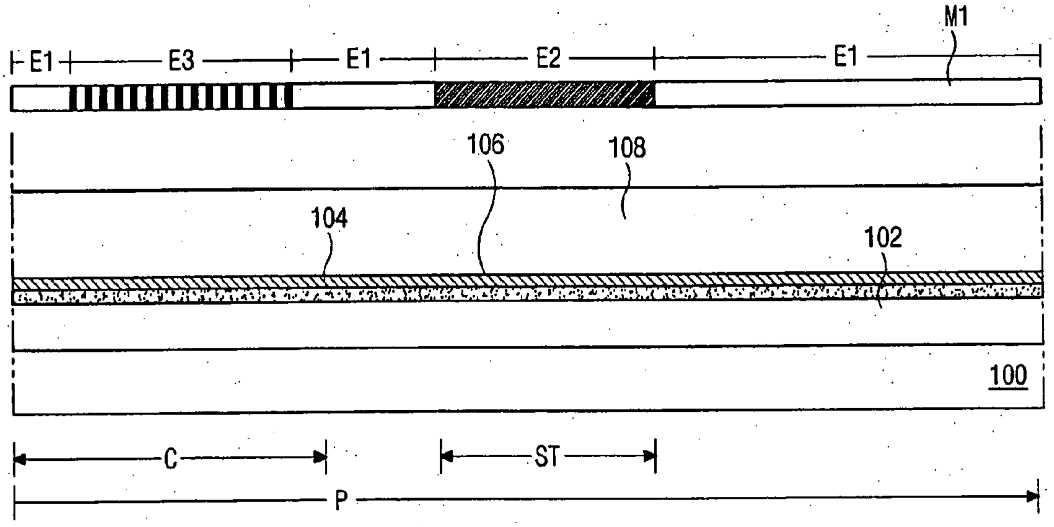


FIG. 14B

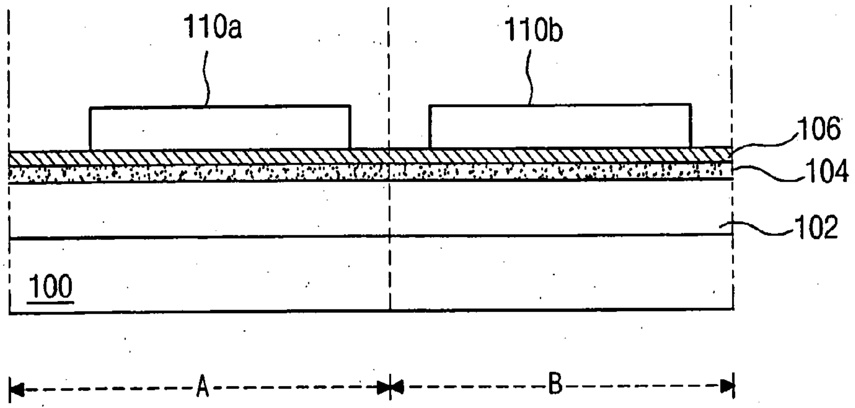


FIG. 15A

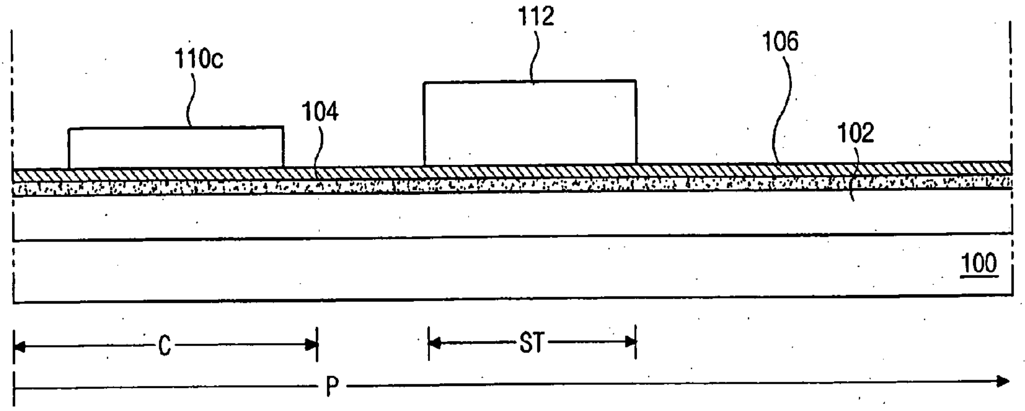


FIG. 15B

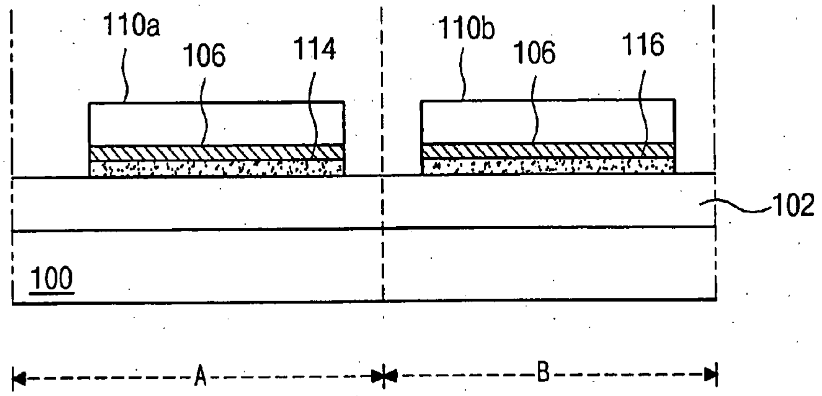


FIG. 16A

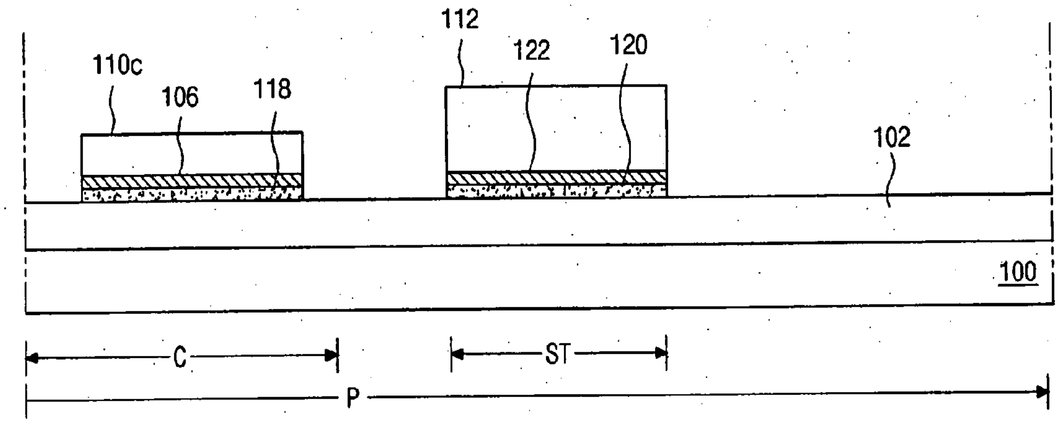


FIG. 16B

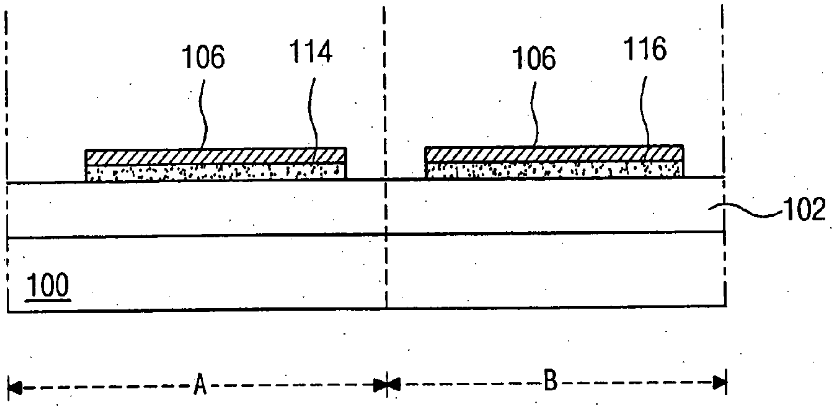


FIG. 17A

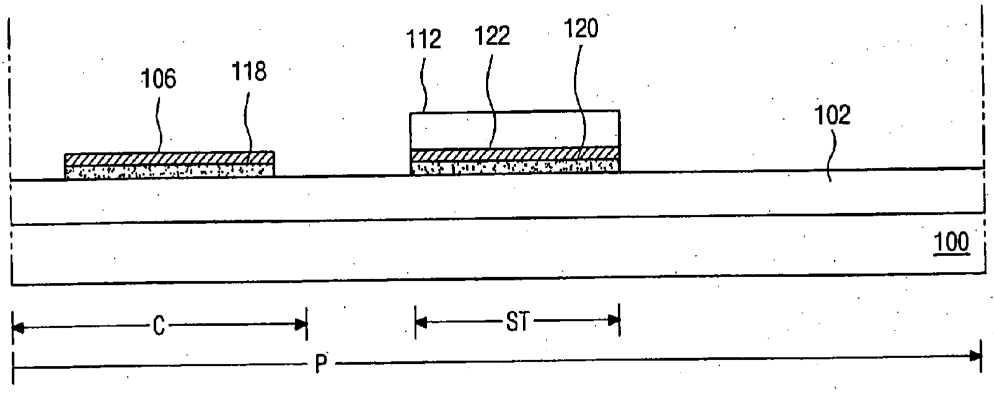


FIG. 17B

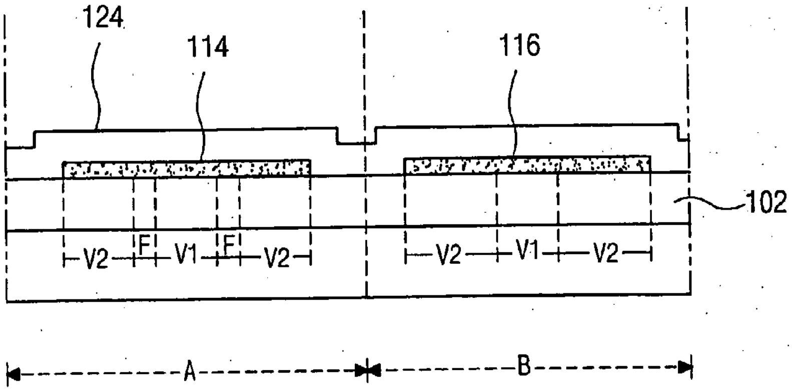


FIG. 18A

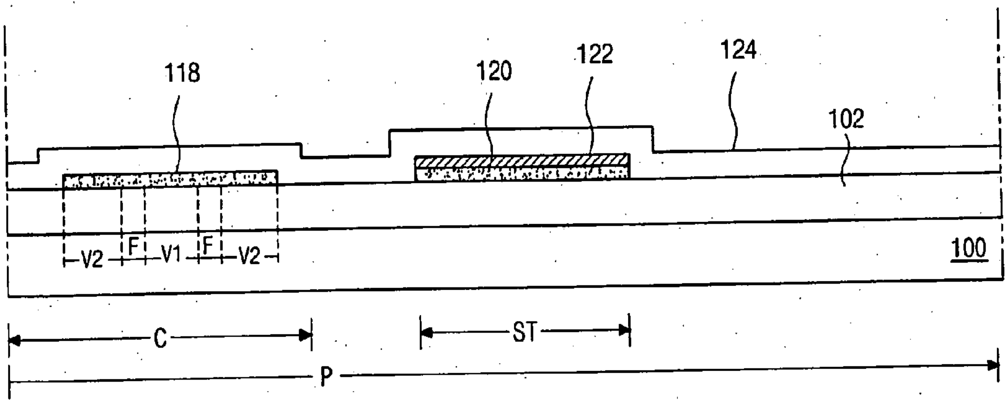


FIG. 18B

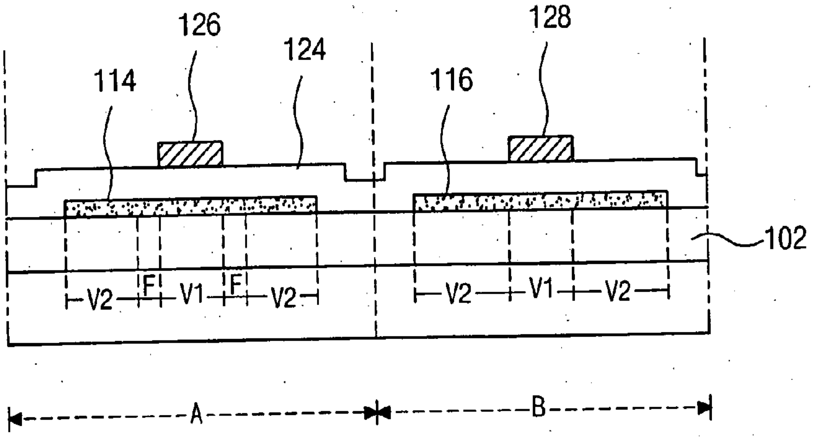


FIG. 19A

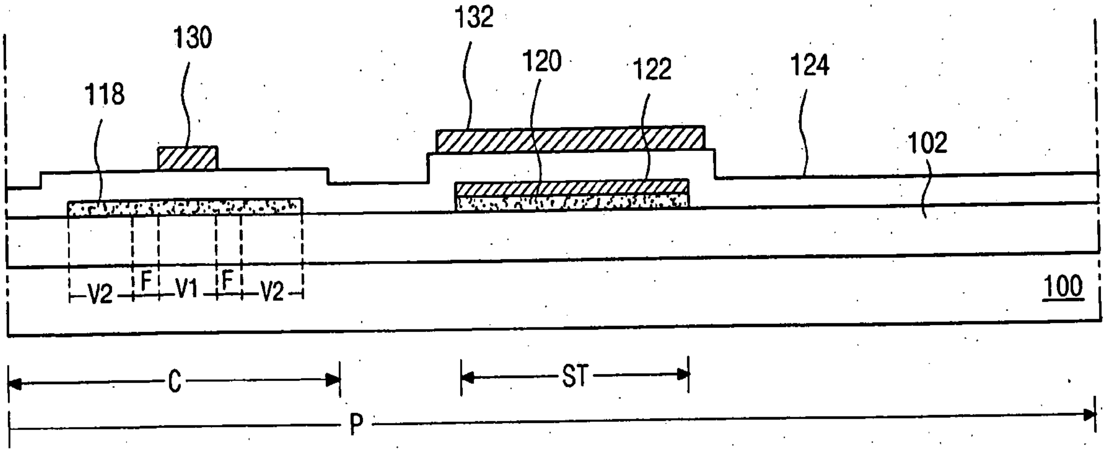


FIG. 19B

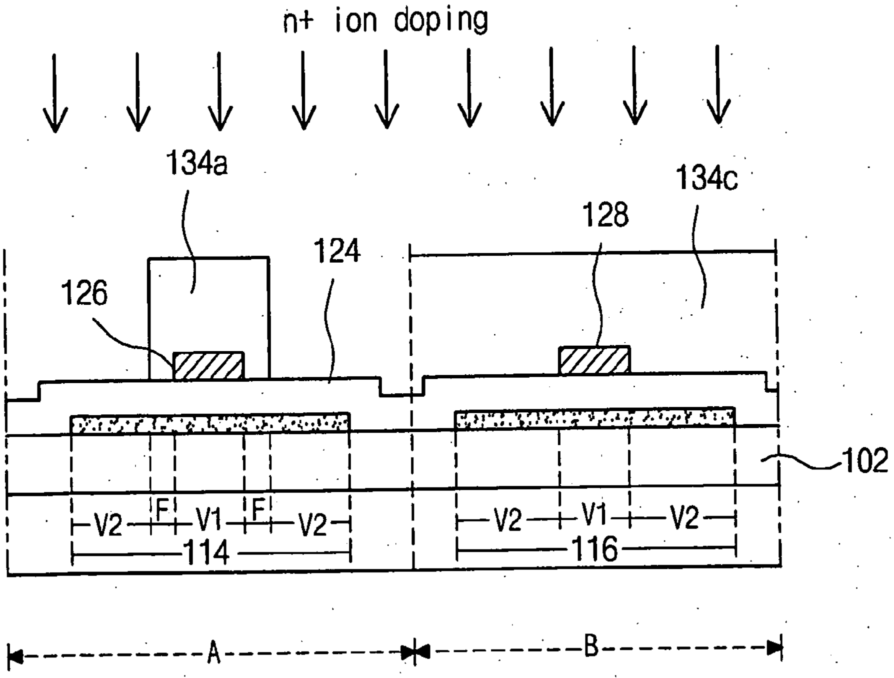


FIG. 20A

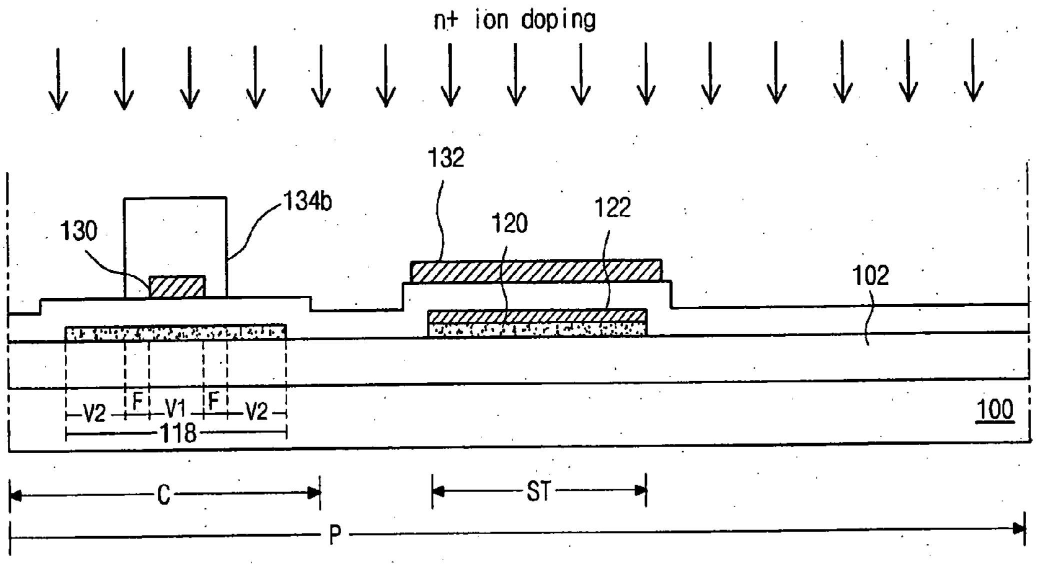


FIG. 20B

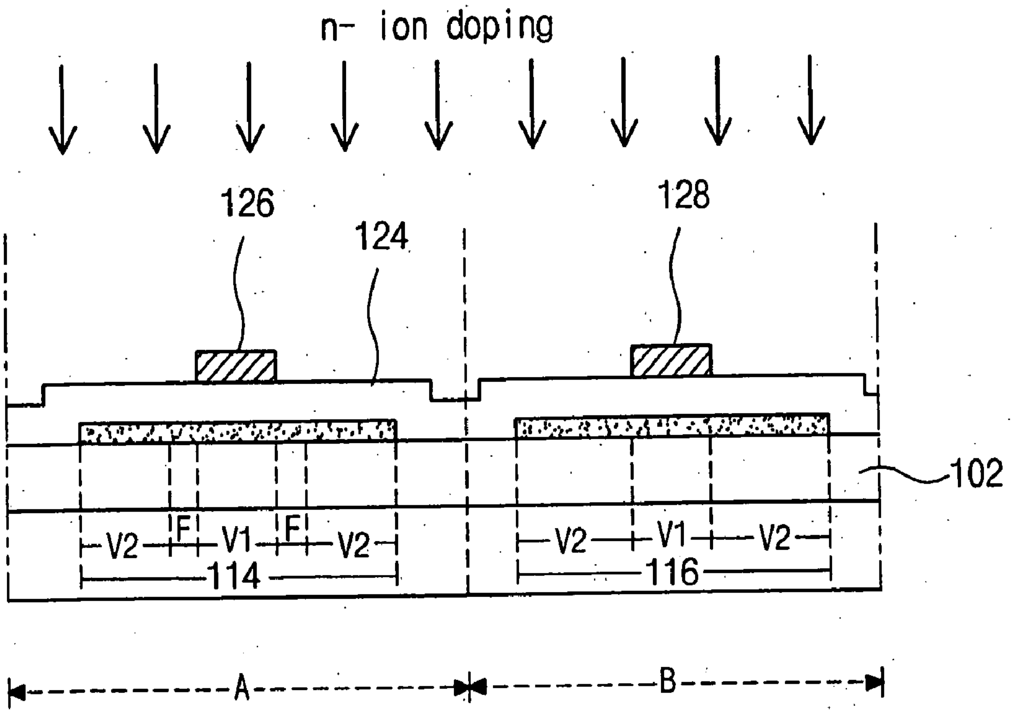


FIG. 21A

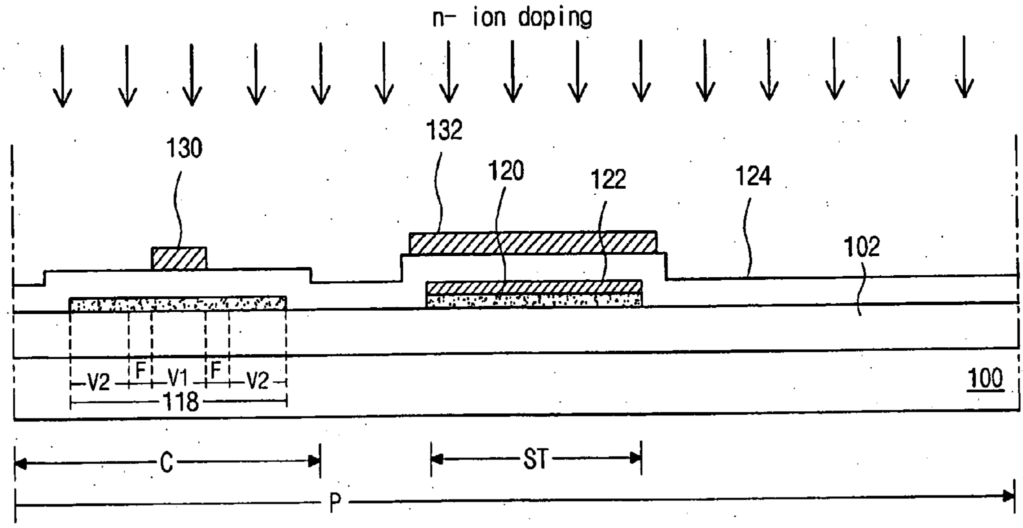


FIG. 21B

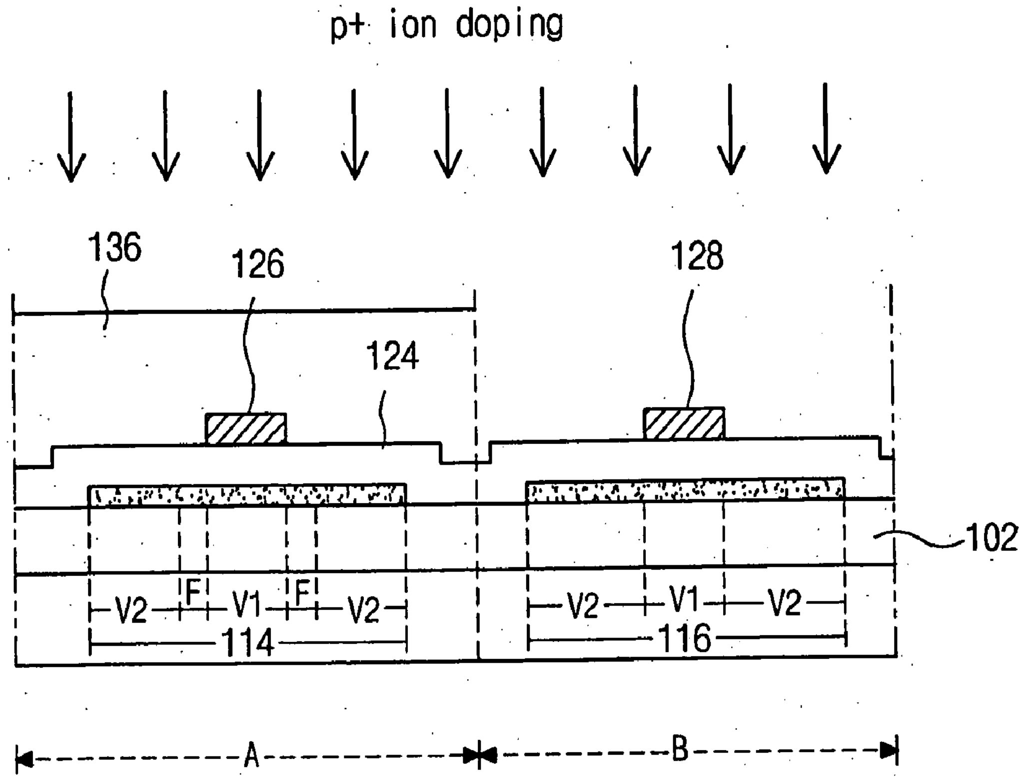


FIG. 22A

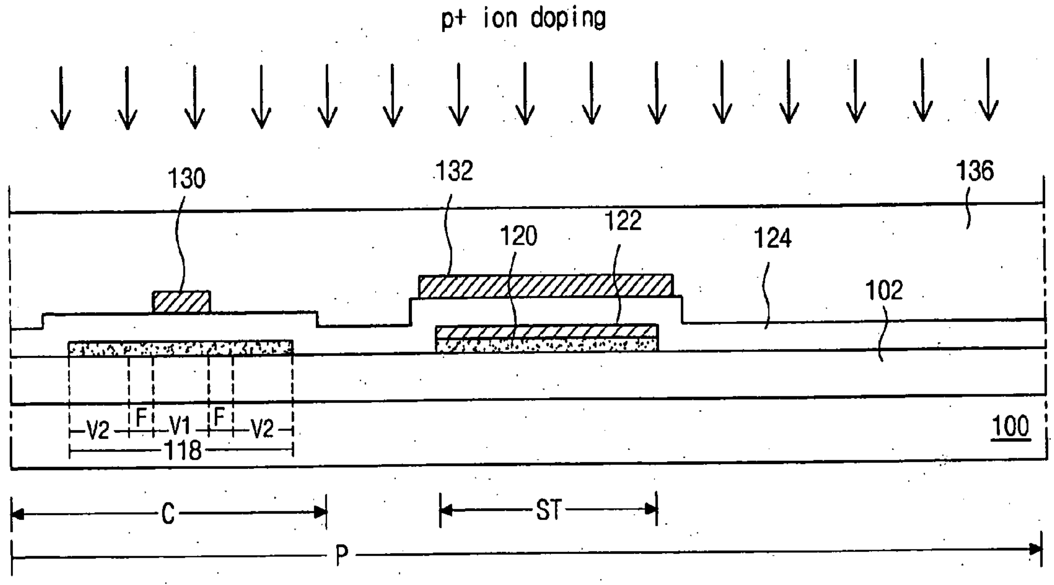


FIG. 22B

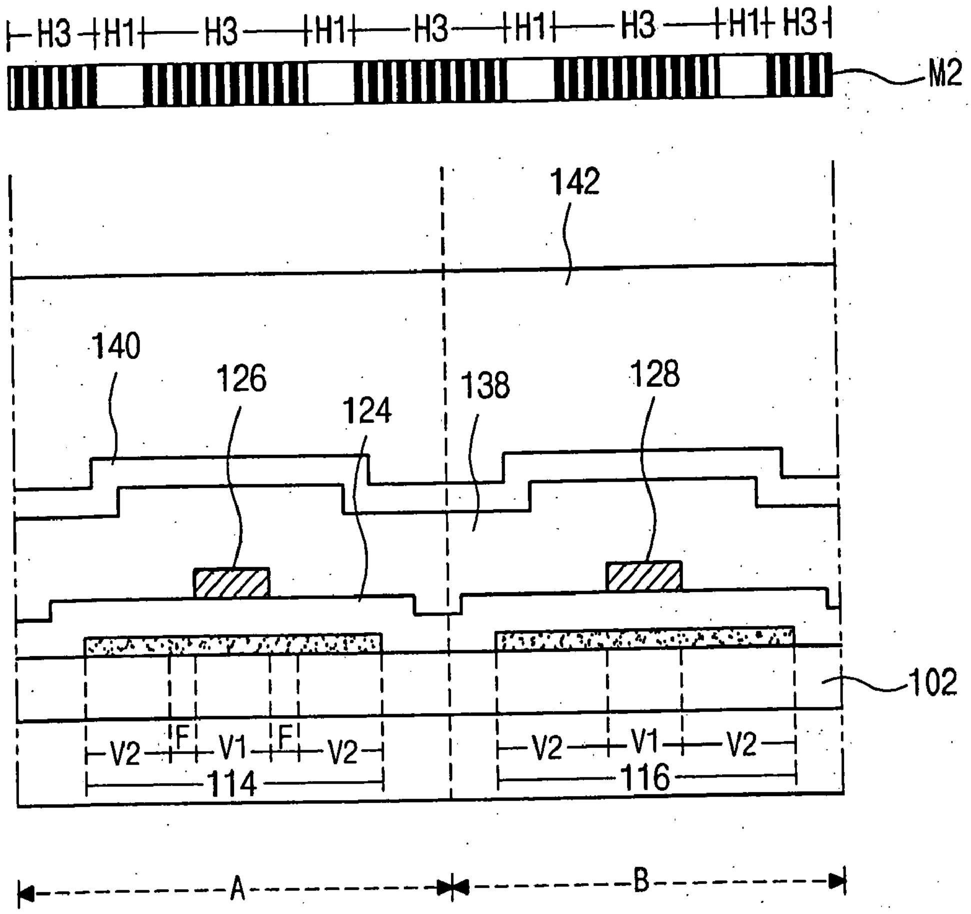
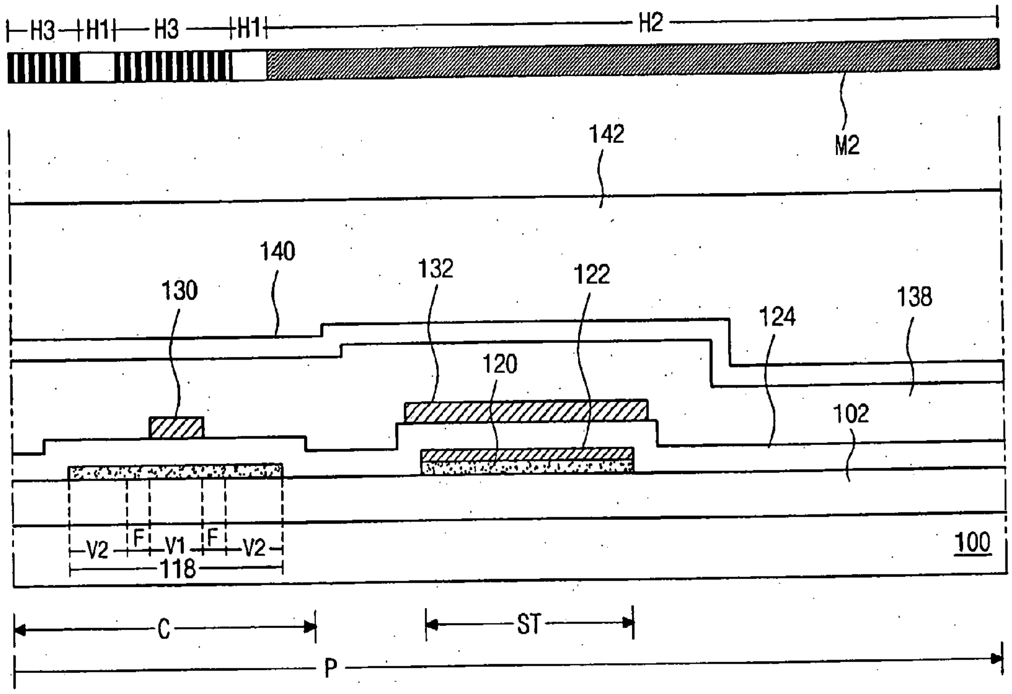

H3
H1
H3
H1
H3
H1
H3
H1
H3
M2
142
140
126
124
138
128
102
V2
F
V1
F
V2
114
V2
V1
V2
116
A
B

FIG. 23A


H3
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H3
H1
H2
M2
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124
120
102
V2
F
V1
F
V2
118
100
C
ST
P

FIG. 23B

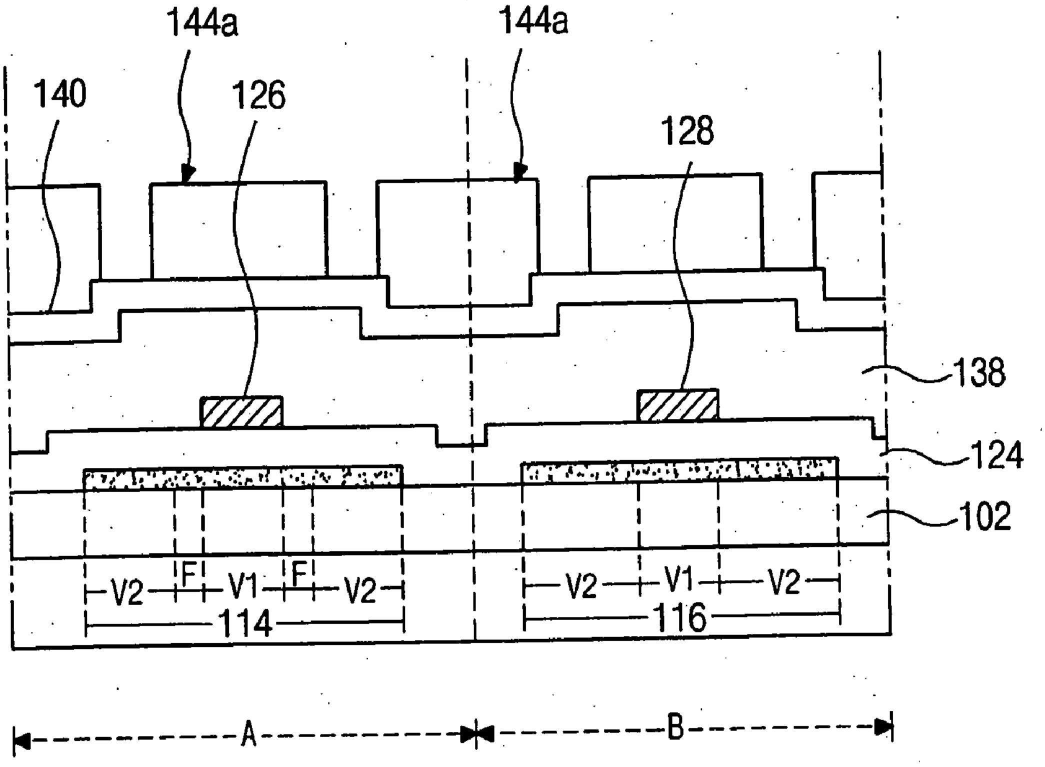
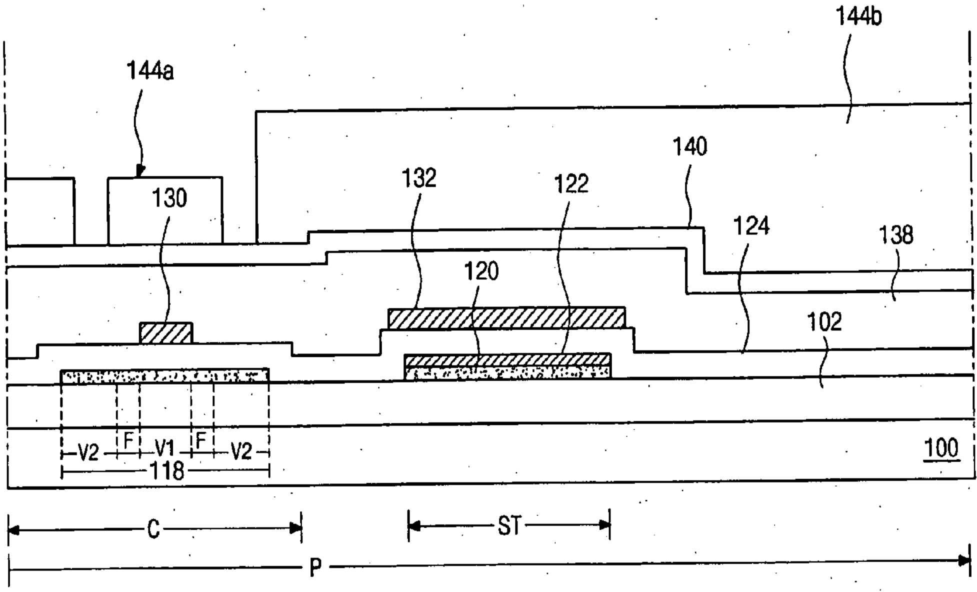


FIG. 24A


144b
144a
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122
130
124
138
120
102
V2
F
V1
F
V2
118
100
C
ST
P

FIG. 24B

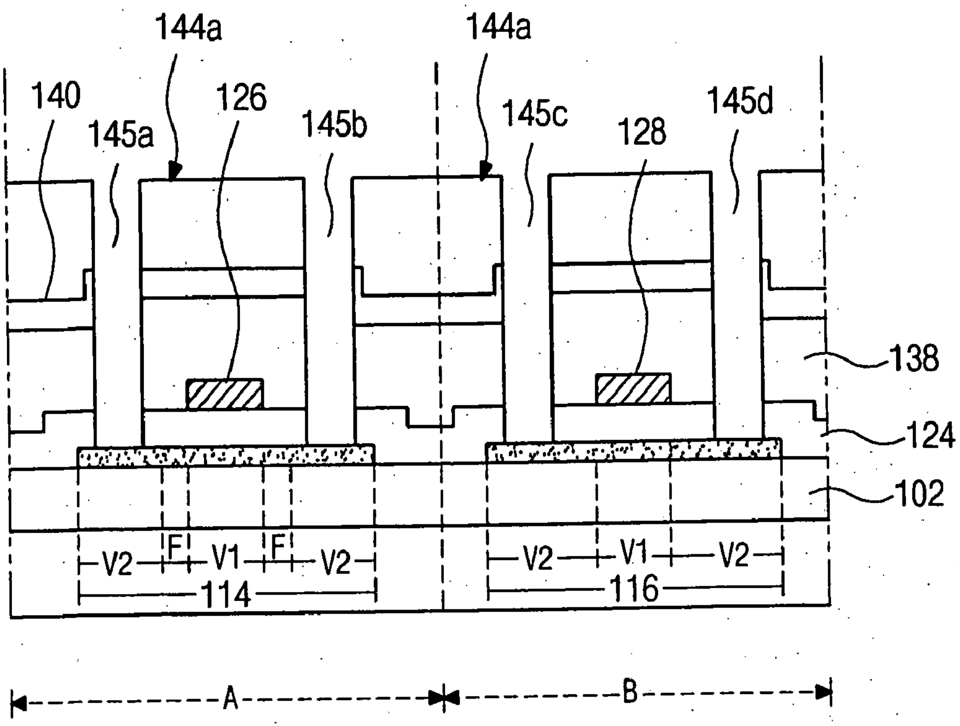

144a
144a
140
145a
126
145b
145c
128
145d
138
124
102
V2
F
V1
F
V2
114
V2
V1
V2
116
A
B

FIG. 25A

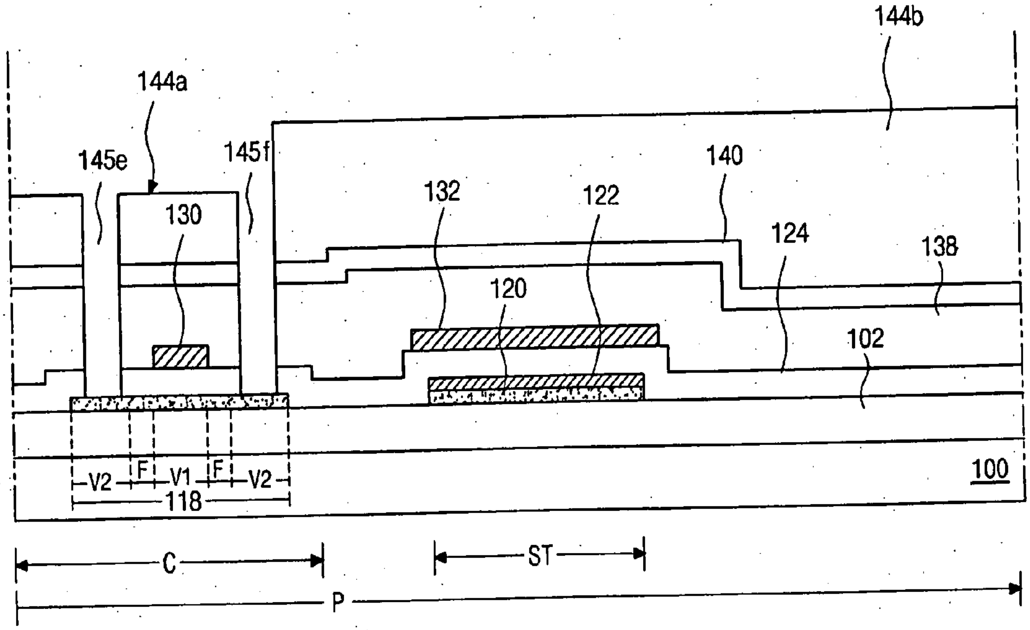


FIG. 25B

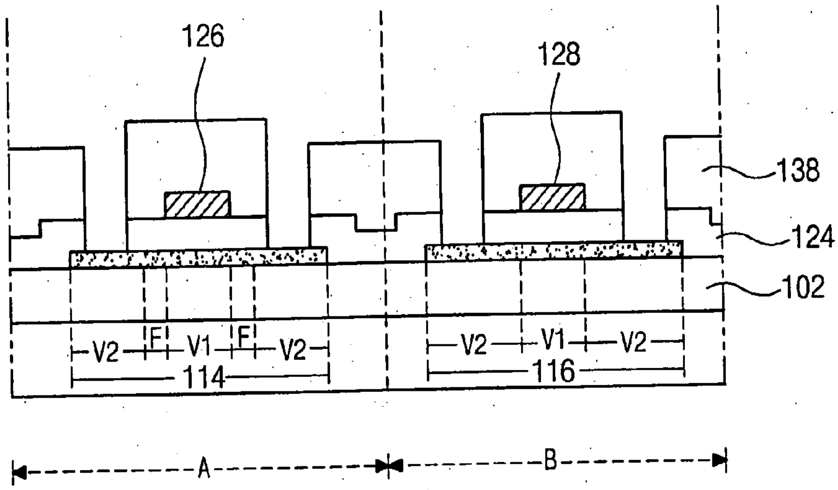


FIG. 26A

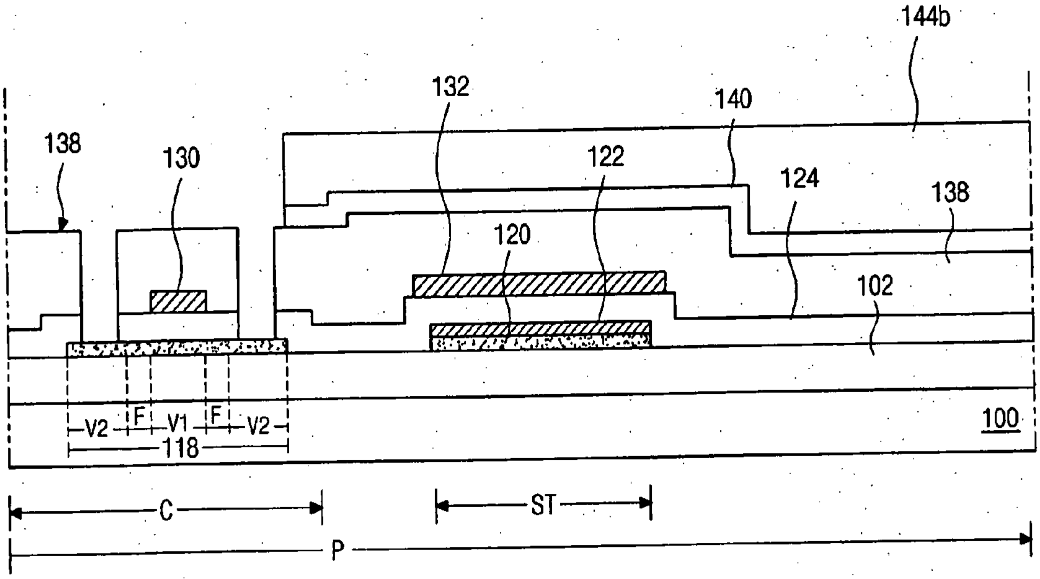


FIG. 26B

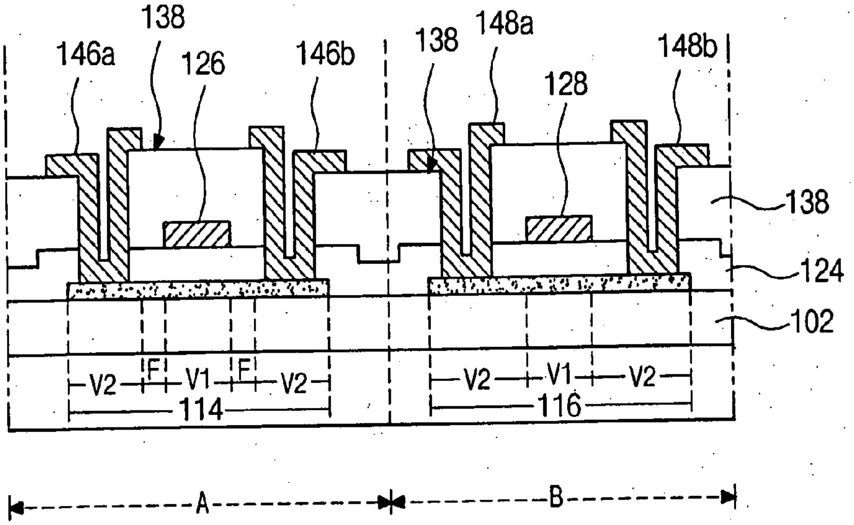
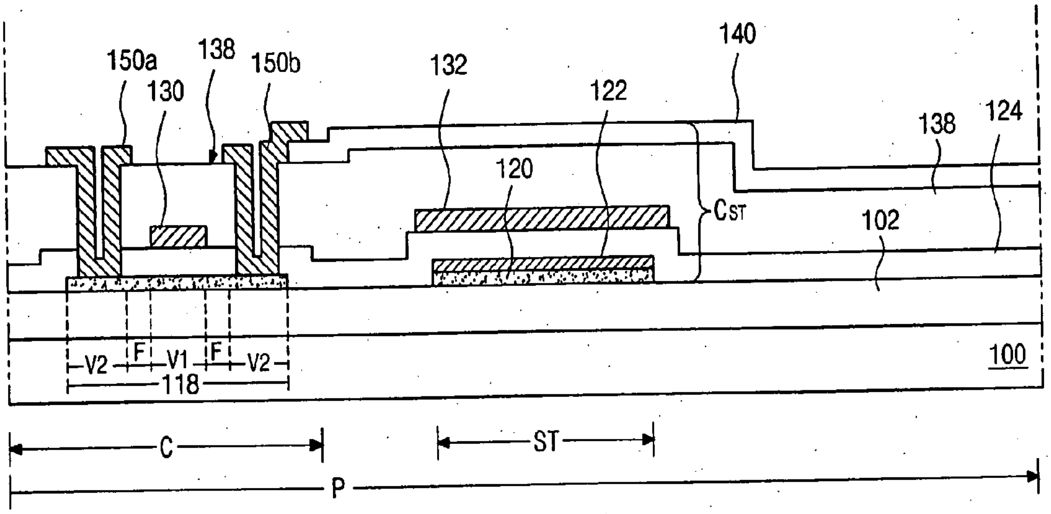


FIG. 27A


150a
138
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132
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CST
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V2
F
V1
F
V2
118
100
C
ST
P

FIG. 27B

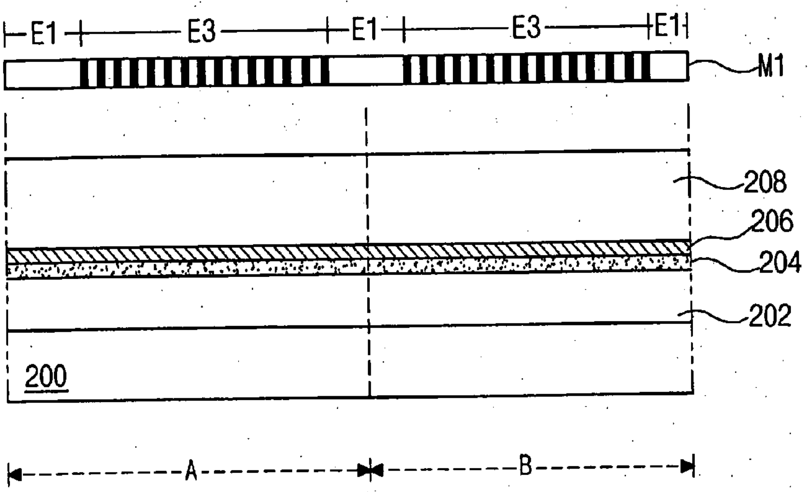

FIG. 28A

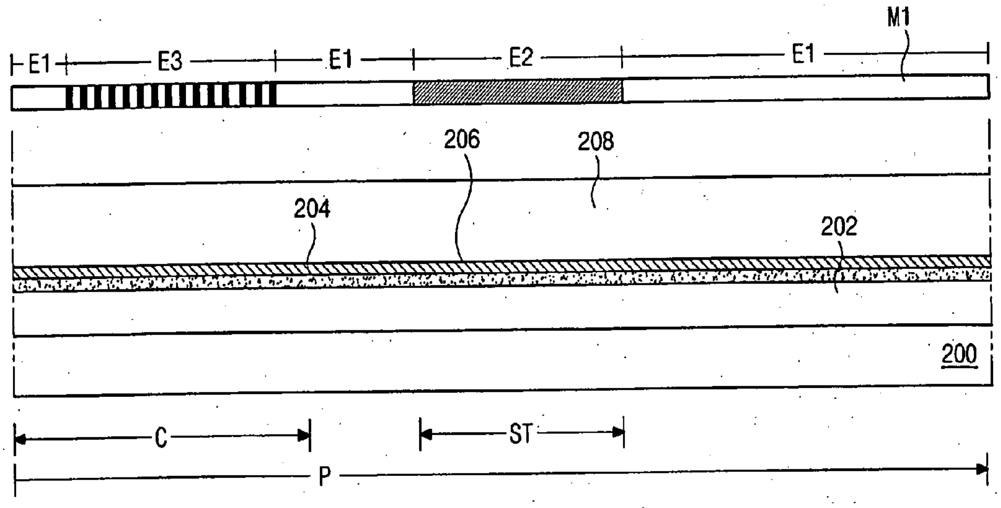

FIG. 28B

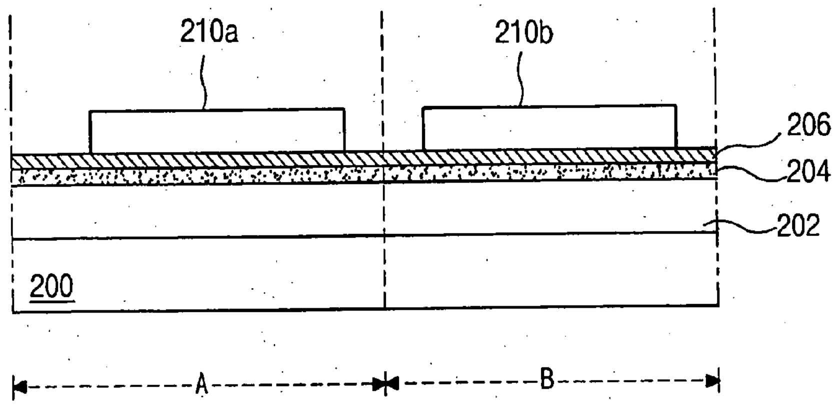

FIG. 29A

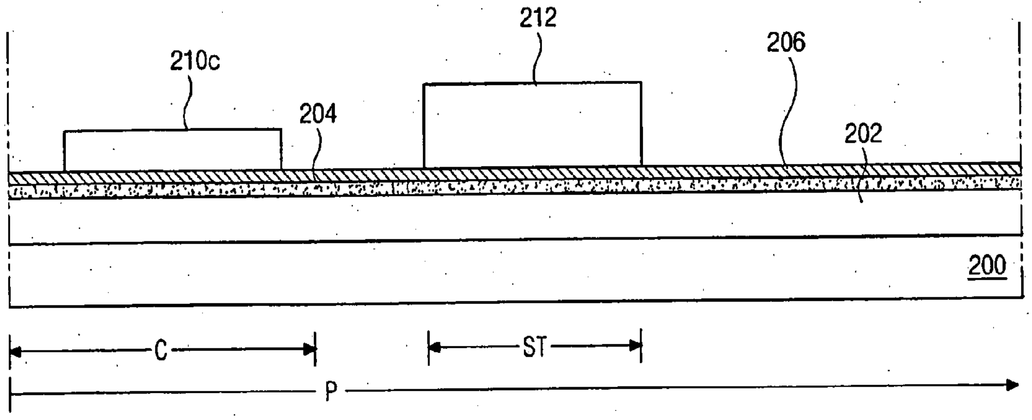

FIG. 29B

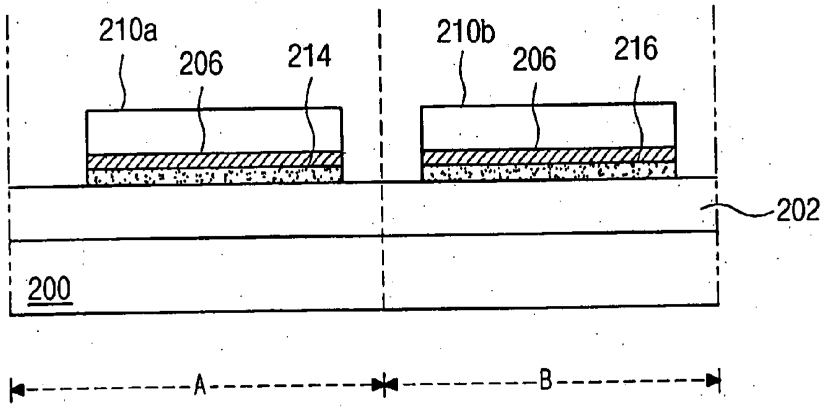

FIG. 30A

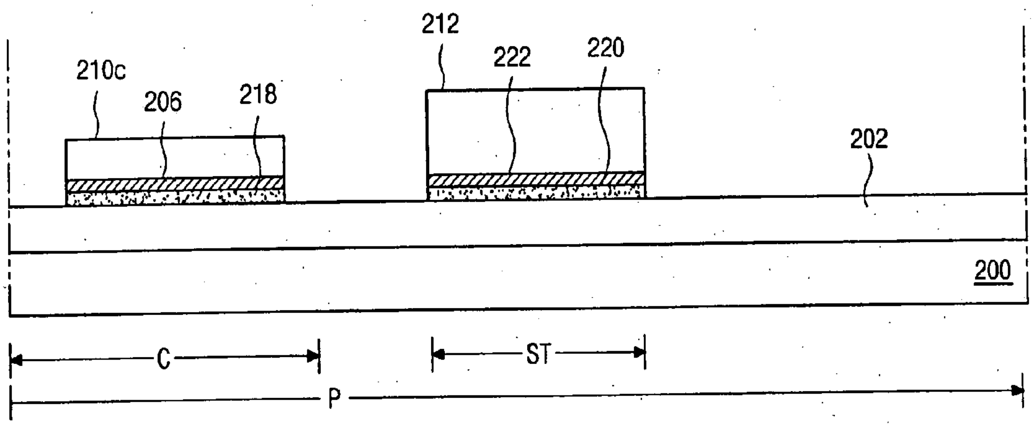

FIG. 30B

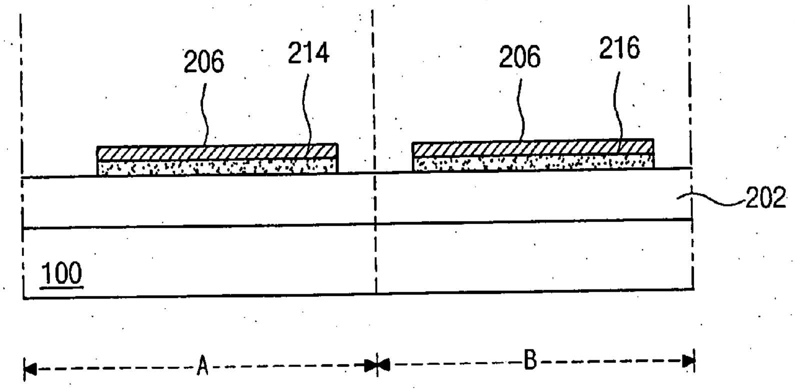

FIG. 31A

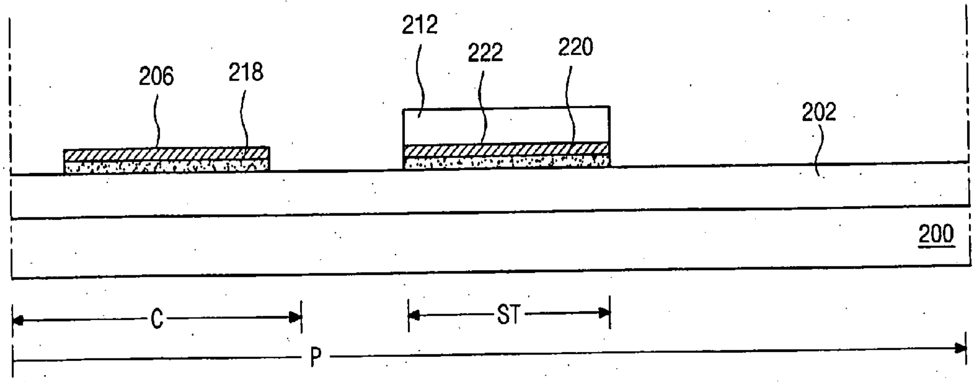

FIG. 31B

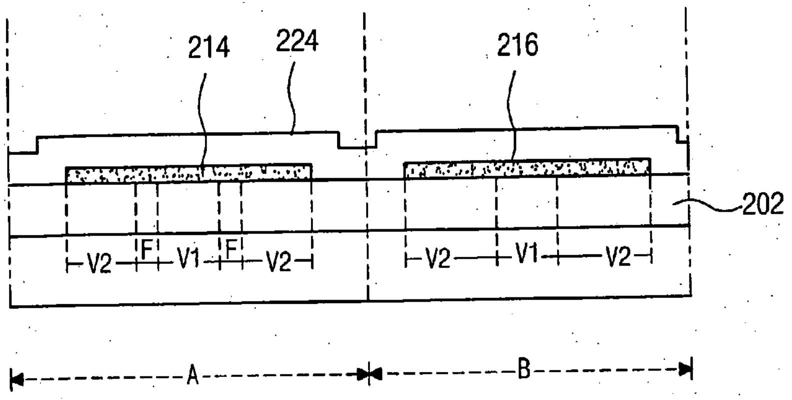

FIG. 32A

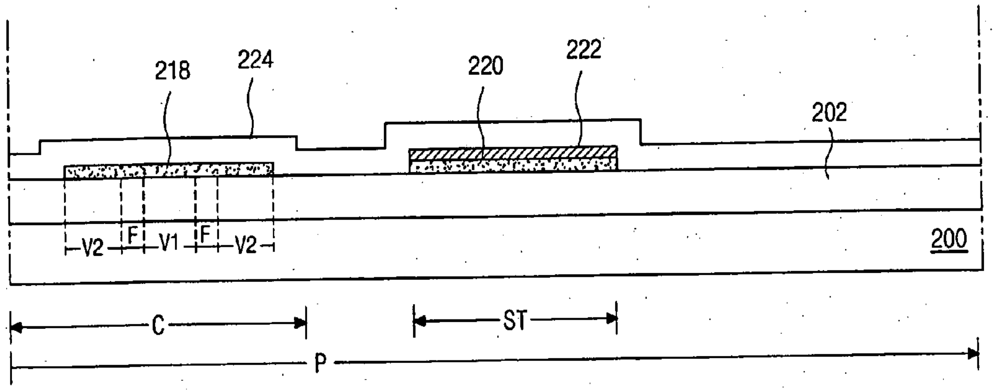

FIG. 32B

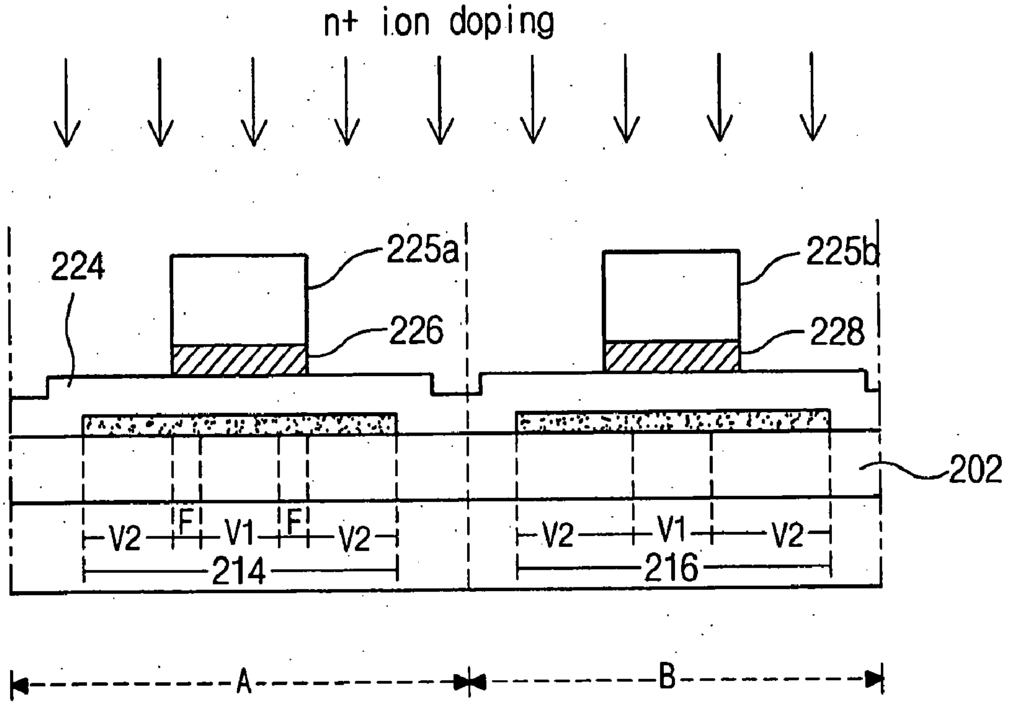
n+ ion doping
224
225a
226
225b
228
202
V2
F
V1
F
V2
214
V2
V1
V2
216
A
B

FIG. 33A

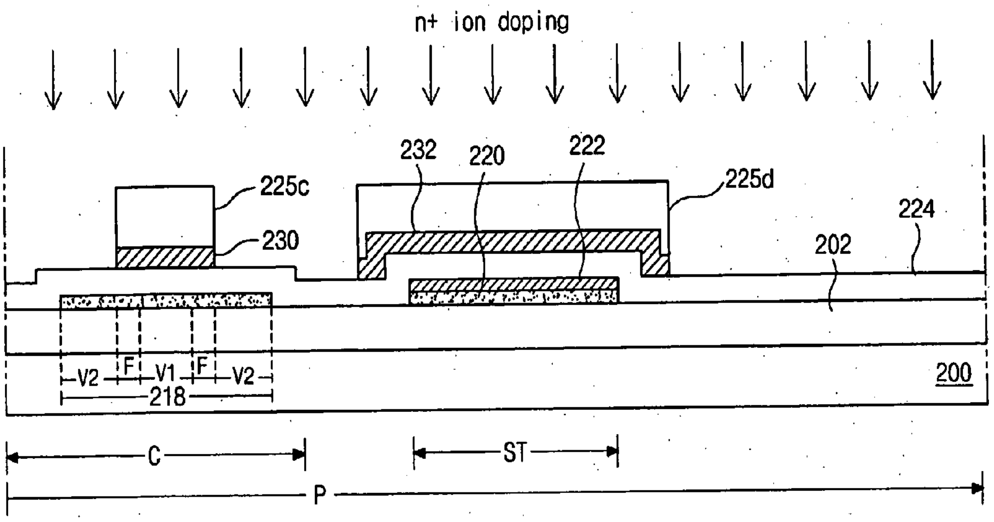

FIG. 33B

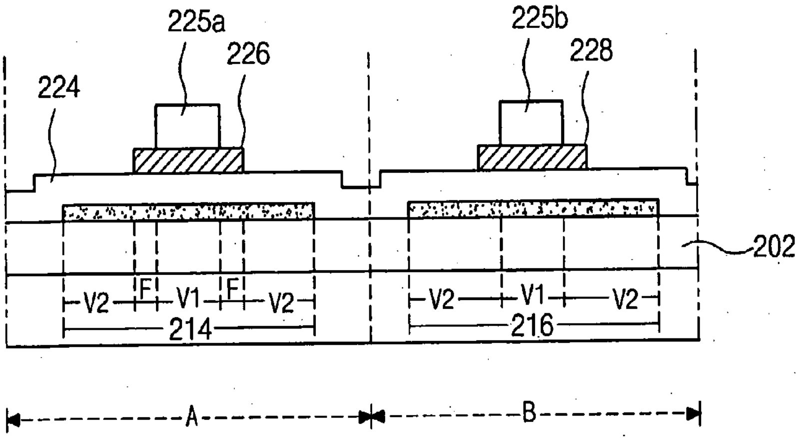

FIG. 34A

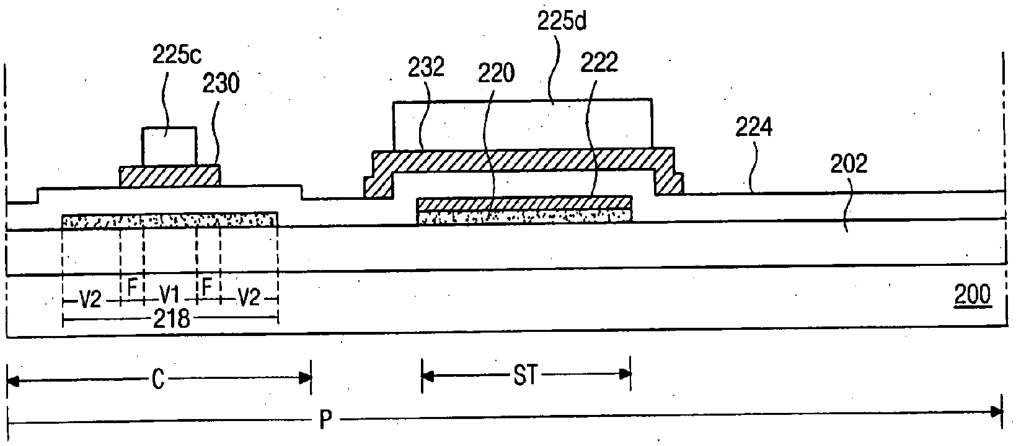

FIG. 34B

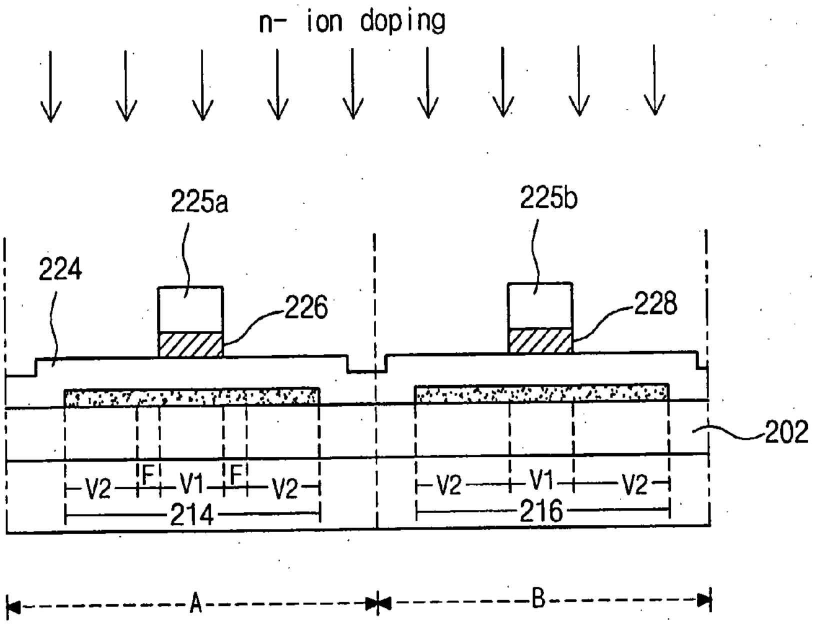

FIG. 35A

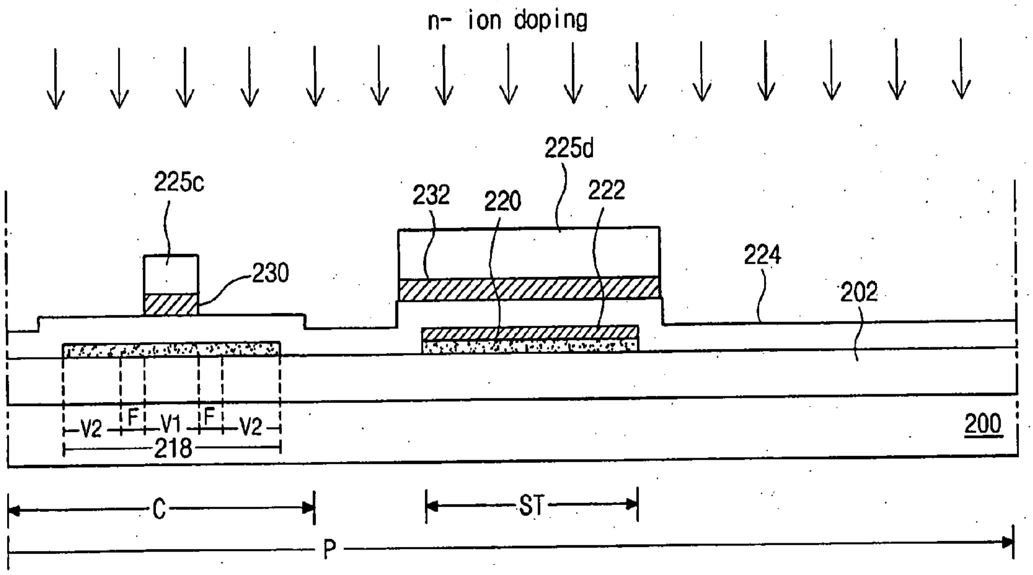
n- ion doping
225d
225c
232
220
222
230
224
202
V2
F
V1
F
V2
218
200
C
ST
P

FIG. 35B

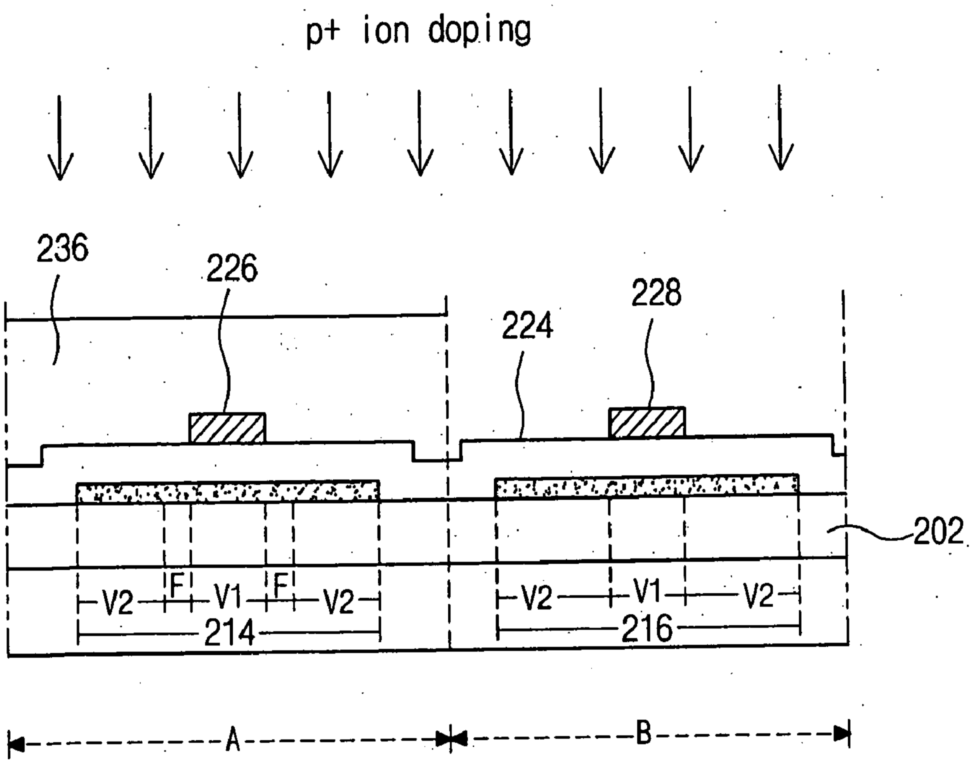

FIG. 36A

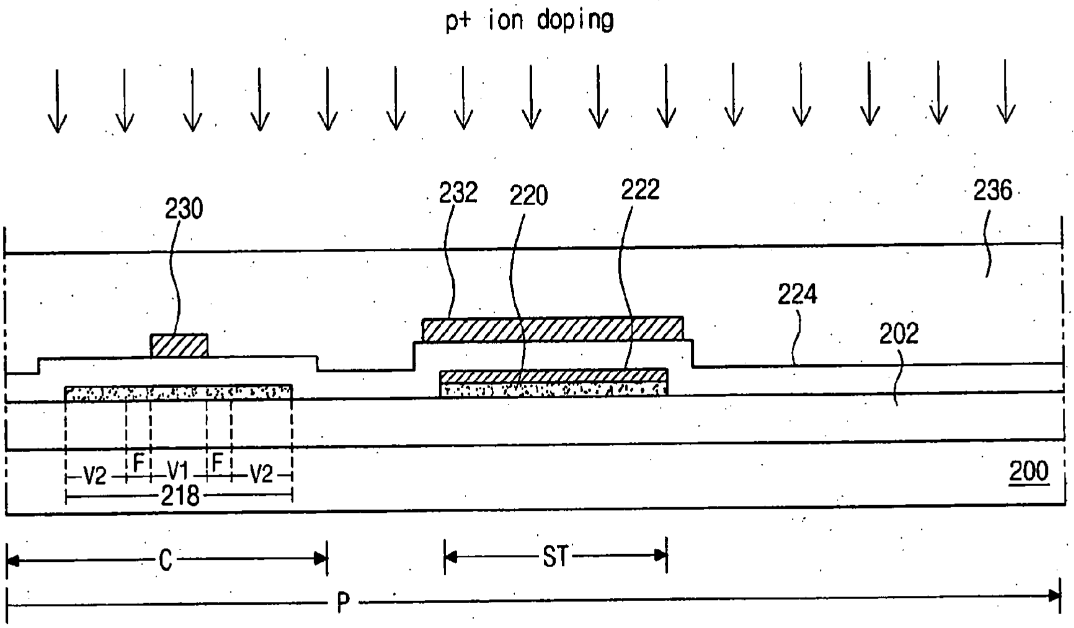

FIG. 36B

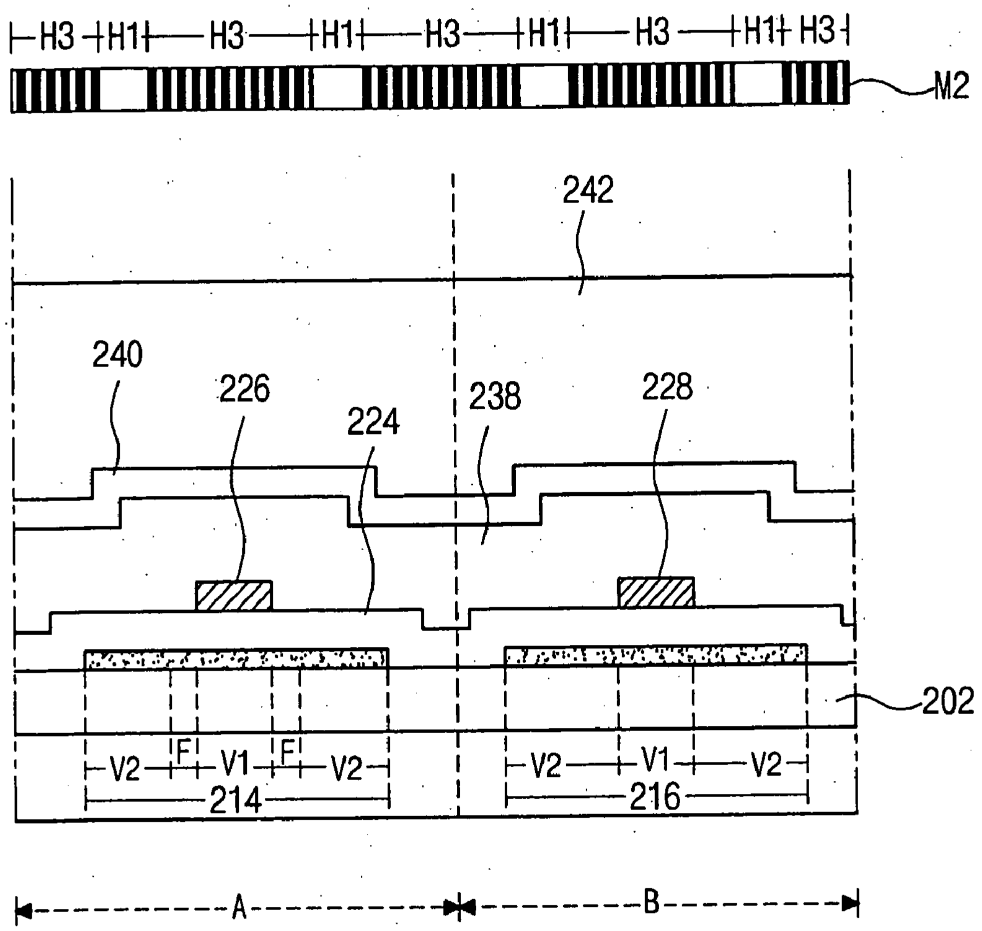
H3
H1
H3
H1
H3
H1
H3
H1
H3
M2
242
240
226
224
238
228
202
V2
F
V1
F
V2
214
V2
V1
V2
216
A
B

FIG. 37A

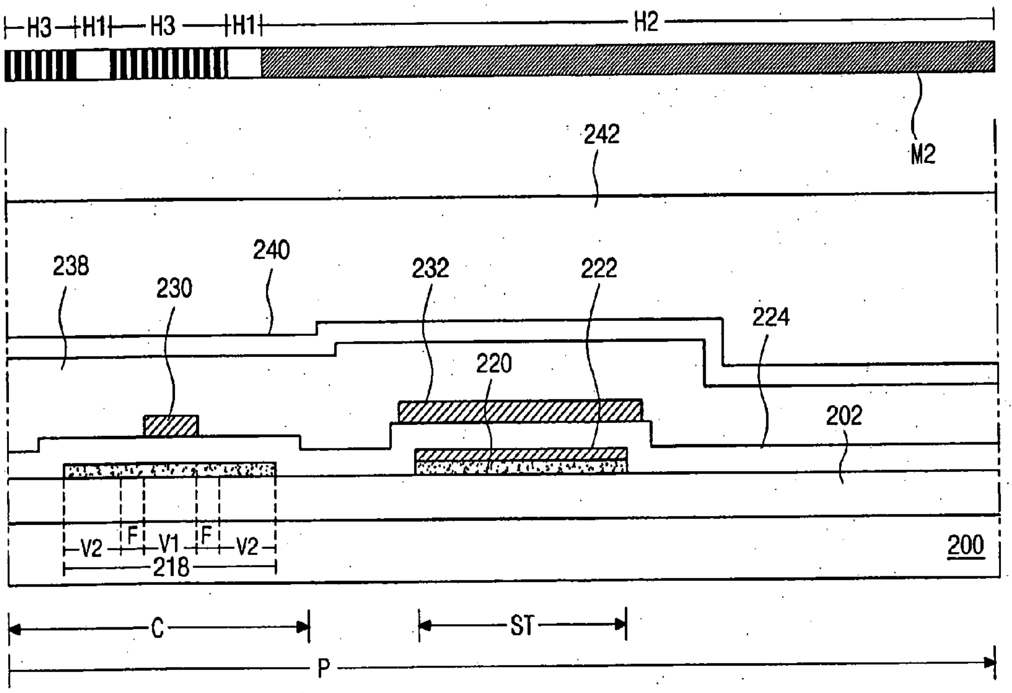
H3
H1
H3
H1
H2
M2
242
238
240
230
232
222
224
220
202
V2
F
V1
F
V2
218
200
C
ST
P

FIG. 37B

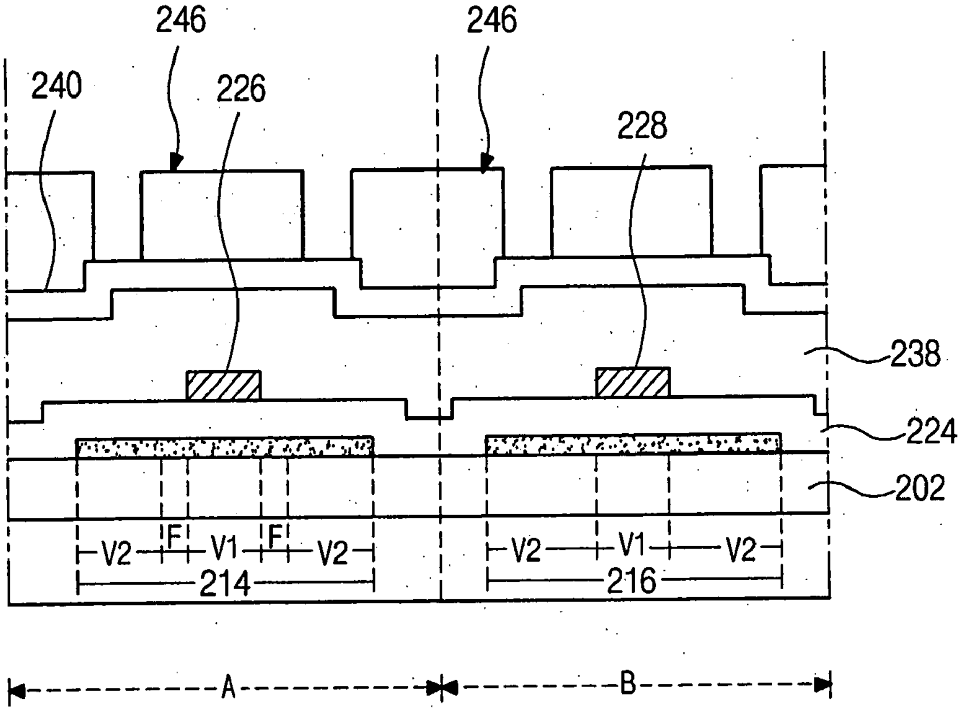

FIG. 38A

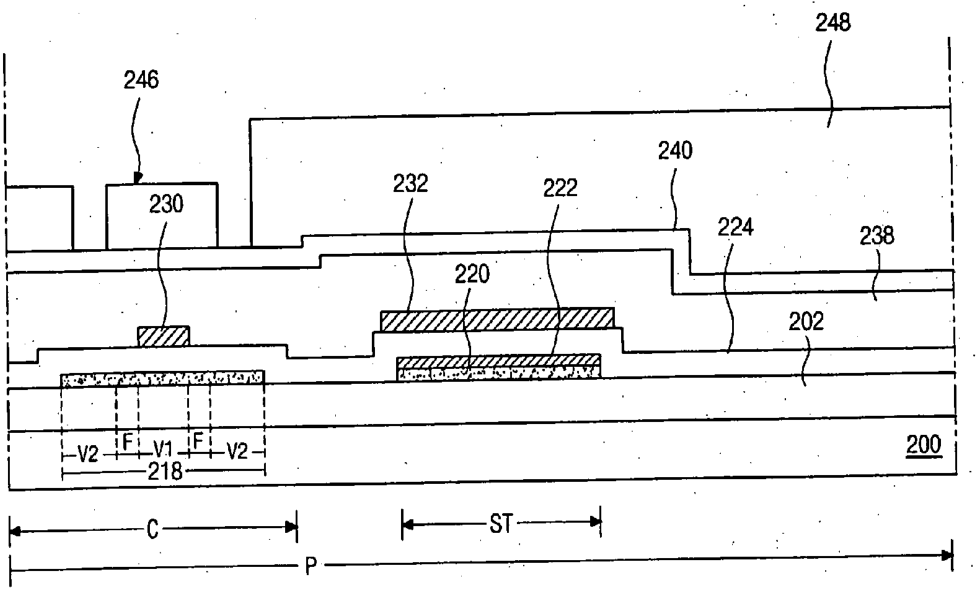

FIG. 38B

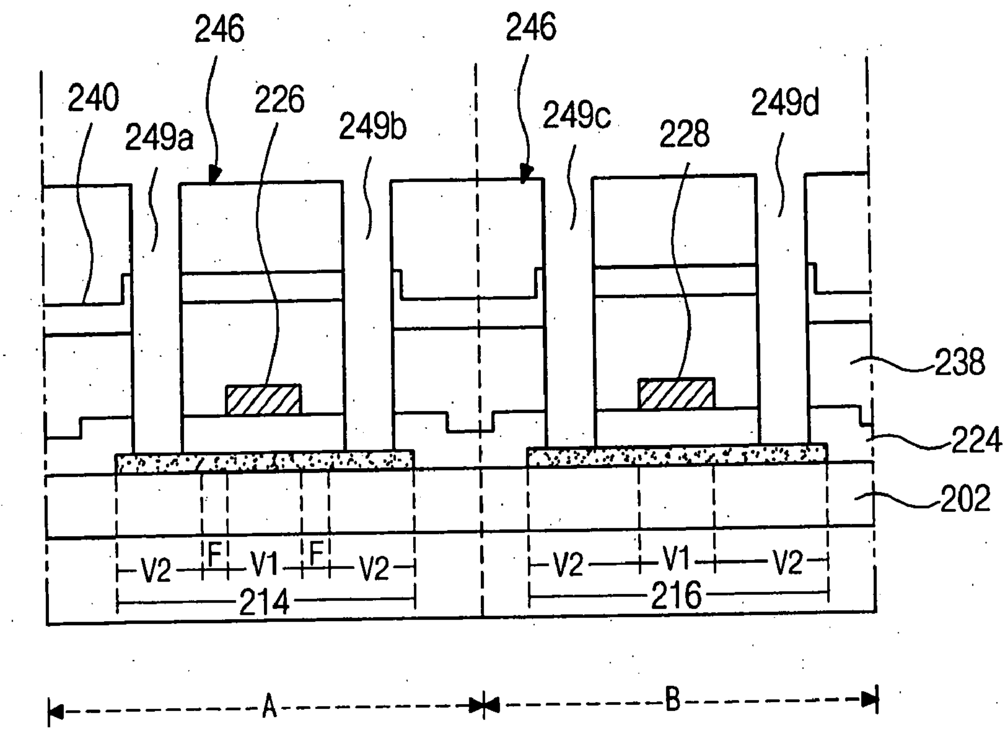
246
246
240
249a
226
249b
249c
228
249d
238
224
202
V2
F
V1
F
V2
214
V2
V1
V2
216
A
B

FIG. 39A

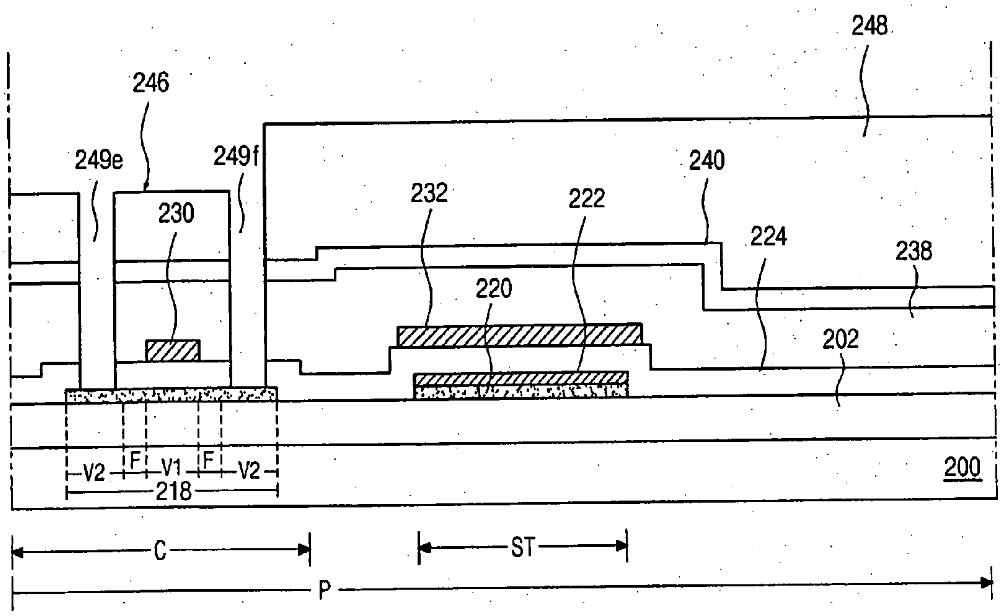

FIG. 39B

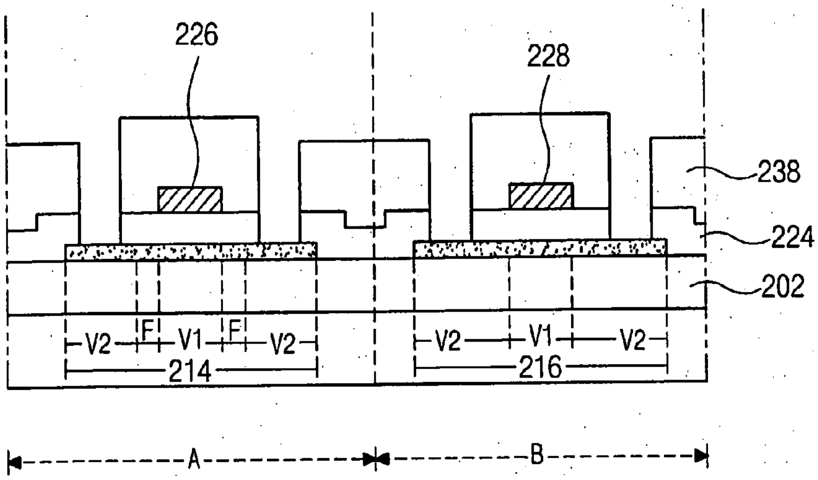

FIG. 40A

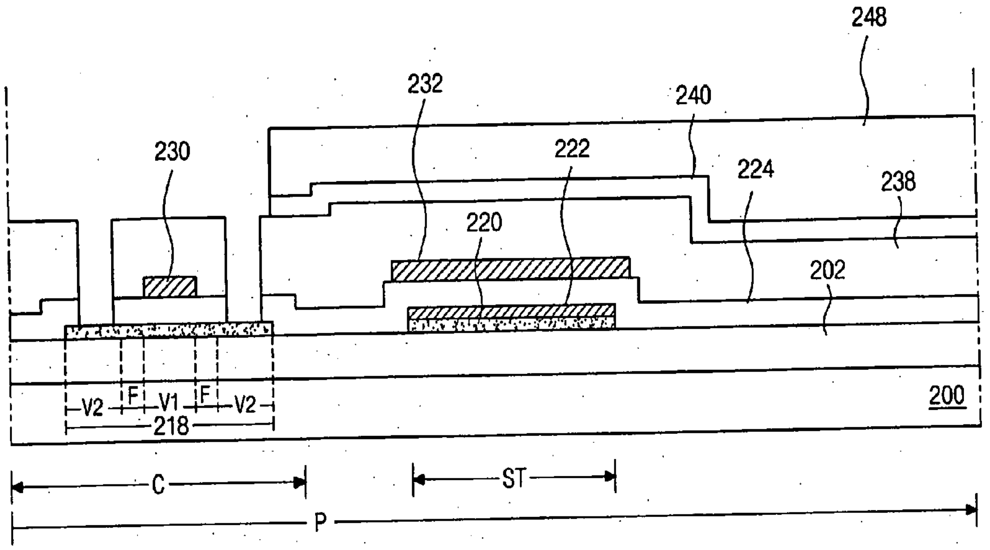

FIG. 40B

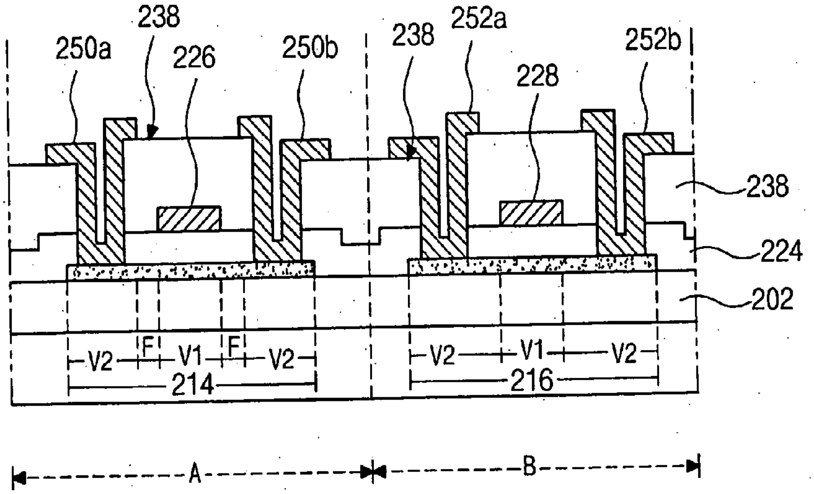

FIG. 41A

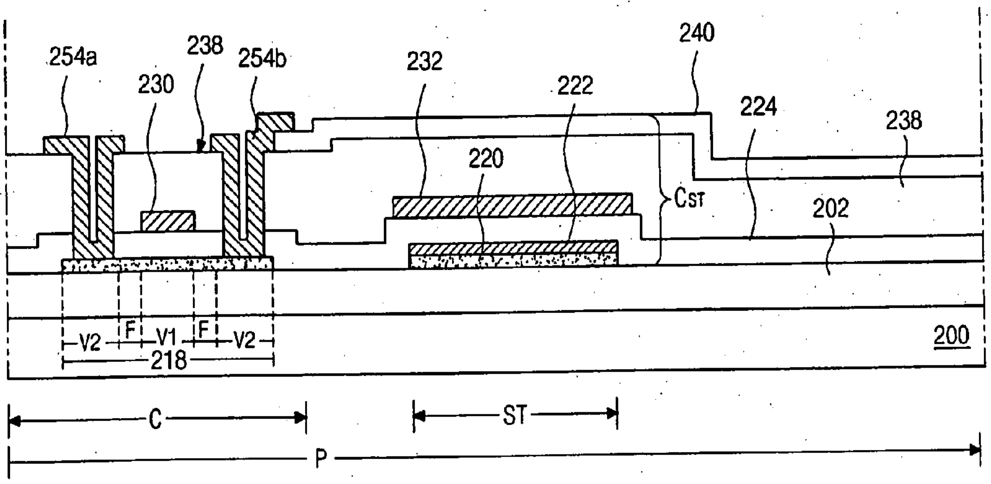
254a
238
254b
230
232
222
240
224
238
220
CST
202
V2
F
V1
F
V2
218
200
C
ST
P

FIG. 41B

ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

[0001] This application claims the benefit of Korean Patent Application No. 2004-0061047 filed in Korea on Aug. 3, 2004, which is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display device and more particularly, to an array substrate for a liquid crystal display device and a method of manufacturing the same.

[0004] 2. Discussion of the Related Art

[0005] A liquid crystal display (LCD) device includes an upper substrate, a lower substrate and a liquid crystal layer disposed between the upper and lower substrates. The LCD device uses an optical anisotropy of liquid crystal to produce an image. An electric field is used to control the light transmittance of the liquid crystal layer by varying the arrangement of liquid crystal molecules.

[0006] One substrate of the LCD device includes a thin film transistor that acts as a switching element. An LCD device, which includes the thin film transistor, is referred to as an active matrix liquid crystal display (AMLCD) device and it has a high resolution and can display an excellent moving image. Hydrogenated amorphous silicon (a-Si:H) is widely used as an active layer of the thin film transistor because the hydrogenated amorphous silicon can be formed on a large, low cost substrate such as glass.

[0007] However, the hydrogenated amorphous silicon includes weak Si—Si bonds and dangling bonds due to disordered atomic arrangement. Thus, when light or an electric field is applied, there may be stability problems in the hydrogenated amorphous silicon used as the active layer of the thin film transistor. Additionally, the thin film transistor including the hydrogenated amorphous silicon has a low field effect mobility of about 0.1 to 1.0 $cm^2/V\cdot s$ and is difficult to be used for a driver integrated circuit (driver IC) that controls the thin film transistor. The driver IC usually includes CMOS (complementary metal-oxide-semiconductor) transistors that require crystalline silicon as active layers. Because of this, the driver IC is usually connected to the array substrate using a TAB (tape automated bonding) system. This adds significant cost to the LCD device.

[0008] To avoid the limitations of amorphous silicon, LCD devices incorporating polycrystalline silicon as an active layer are being researched and developed. Polycrystalline silicon is highly beneficial because it is much better suited for use in the driver IC than amorphous silicon. Thus, polycrystalline silicon has the advantage that the number of fabrication steps could be reduced because a thin film transistor and a driver IC could be formed on the same substrate, eliminating the need for TAB bonding. Furthermore, the field effect mobility of polycrystalline silicon is 100 to 200 times greater than that of amorphous silicon. Polycrystalline silicon is also optically and thermally stable.

[0009] FIG. **1** is a schematic view showing an array substrate of a liquid crystal display device having driver integrated circuits (driver ICs) according to the related art. Referring to FIG. **1**, the array substrate includes a display region D**1** and a non-display region D**2** on an insulating substrate **10**. In the display region D**1**, gate lines GL are formed along a first direction, and data lines DL are formed along a second direction perpendicular to the first direction. The gate lines GL and the data lines DL cross each other to define pixel regions P. The pixel regions P form a matrix. In each pixel region P, a switching element T and a pixel electrode **78**, which is connected to the switching element T, are formed. In the non-display region D**2**, gate and data driving portions GP and DP are disposed. The gate driving portion GP is disposed in the left region of the substrate **10** in the context of the figure, and the data driving portion DP is disposed in the top region of the substrate **10** in the context of the figure. The gate driving portion GP, which includes a plurality of driver ICs, supplies an address signal to the gate lines GL, and the data driving portion DP, which also includes a plurality of driver ICs, supplies an image signal to the data lines DL.

[0010] The gate driving portion GP and the data driving portion DP are electrically connected to an outer control circuit (not shown) with signal input terminals OL which are formed on one edge of the substrate **10**, so that the outer control circuit (not shown) controls the driver ICs of the gate driving portion GP and the data driving portion DP. The outer control circuit (not shown) applies signals to the gate and data driving portions GP and DP through the signal input terminals OL.

[0011] The gate driving portion GP and the data driving portion DP include driver ICs having a CMOS (complementary metal-oxide-semiconductor) transistor as an inverter which changes a direct current into an alternating current. The CMOS transistor comprises an n-channel MOS transistor (or n-type MOS transistor), in which electrons are the majority carriers, and a p-channel MOS transistor (or p-type MOS transistor), in which holes are the majority carriers. Therefore, in an n-channel MOS transistor, most of the current is carried by negatively charged electrons, and in a p-channel MOS transistor, most of the conduction is carried by positively charged holes. The thin film transistor T of the display region D**1** and the CMOS transistor (not shown) of the non-display region D**2** may use polycrystalline silicon as an active layer, and thus can be formed on the same substrate **10**.

[0012] FIG. **2** is a plan view illustrating a pixel region of an array substrate including a polycrystalline silicon thin film transistor according to the related art. Referring to FIG. **2**, a gate line GL is formed along a direction on a substrate **10**, and a data line DL crosses the gate line GL to define a pixel region P. A thin film transistor T is formed at the crossing portion of the gate and data lines GL and DL. The thin film transistor T includes an active layer **18** of polycrystalline silicon, a gate electrode **34** over the active layer **18**, and source and drain electrodes **70** and **72** contacting the active layer **18**. A pixel electrode **78** is formed in the pixel region P and is connected to the drain electrode **72**. A storage capacitor C_{ST} is also formed in the pixel region P. The storage capacitor C_{ST} includes an impurity-doped polycrystalline silicon pattern **20**, as a first electrode, and a storage line **36**, as a second electrode. The storage line **36** is disposed over the impurity-doped polycrystalline silicon pattern **20** and traverses the pixel region P.

[0013] FIGS. **3**A and **3**B are cross-sectional views of an array substrate including driver ICs according to the related art. FIG. **3**A illustrates a CMOS transistor in a driving region, and FIG. **3**B illustrates a pixel region including a switching element. FIG. **3**B corresponds to a cross-section taken along the line III-III of FIG. **2**. Referring to FIGS. **3**A and **3**B, a buffer layer **12** is formed on a substrate **10**. A CMOS transistor is formed in a driving region including a first driving region A and a second driving region B. The CMOS transistor is composed of an n-type MOS transistor and a p-type MOS transistor in the first and second driving regions A and B, respectively. An n-type thin film transistor, as a switching element, is formed in a switching region C of a pixel region P, and a storage capacitor C_{ST} is formed in a storage region ST of the pixel region P. A pixel electrode **78** is also formed in the pixel region P and is connected to the n-type thin film transistor.

[0014] More particularly, first, second and third active patterns **14**, **16** and **18** are formed in the first driving region A, the second driving region B and the switching region C, respectively. Each of the first, second and third active patterns **14**, **16** and **18** is formed of polycrystalline silicon and includes an intrinsic portion V**1** and doped portions V**2**. The first and third active patterns **14** and **18** include a lightly doped drain (LDD) portion F between the intrinsic portion V**1** and each doped portion V**2**. The LDD portion F includes impurities of low density and prevents leakage current of an off-state, that is, applying reverse bias to a thin film transistor. An extension portion **20** extends from the third active pattern **18** into the pixel region P.

[0015] A gate insulating layer **28** is formed on the entire surface of the substrate **10** including the first, second and third active patterns **14**, **16** and **18**. First, second and third gate electrodes **30**, **32** and **34** are formed on the gate insulating layer **28**. The first, second and third gate electrodes **30**, **32** and **34** correspond to the intrinsic portions of the first, second and third active patterns **14**, **16** and **18**, respectively. A storage line **36** traversing the pixel region P is also formed on the gate insulating layer **38**. The storage line **36** is disposed over the extension portion **20**. The extension portion **20** and the storage line **36** function as a first electrode and a second electrode, respectively, to form the storage capacitor C_{ST}. An inter insulating layer **48** is formed on the entire surface of the substrate **10** including the first, second and third gate electrodes **30**, **32** and **34** and the storage line **36**. The inter insulating layer **48** and the gate insulating layer **28** include contact holes exposing the doped portions of the first, second and third active patterns **14**, **16** and **18**.

[0016] First source and drain electrodes **62** and **64**, second source and drain electrodes **66** and **68**, and third source and drain electrodes **70** and **72** are formed on the inter insulating layer **48**. The first source and drain electrodes **62** and **64** contact the exposed doped portions V**2** of the first active pattern **14**, the second source and drain electrodes **66** and **68** contact the exposed doped portions V**2** of the second active pattern **16**, and the third source and drain electrodes **70** and **72** contact the exposed doped portions V**2** of the third active pattern **18**. A pixel electrode **78** is formed on a passivation layer **74** in the pixel region P and is connected to the third drain electrode **72** in the switching region C. As stated above, the n-type thin film transistor in the switching region C and the CMOS transistor in the driving region are formed on the same substrate through the same processes.

[0017] A manufacturing method of an array substrate including driver ICs according to the related art will be explained hereinafter with reference to attached drawings.

[0018] FIGS. **4**A and **4**B to FIGS. **12**A and **12**B are cross-sectional views illustrating a manufacturing method of an array substrate including driver ICs according to the related art. FIGS. **4**B to **12**B illustrate a pixel region including a switching element and correspond to cross-sections taken along the line III-III of FIG. **2**. Referring to FIGS. **4**A and **4**B, a driving region, which includes a first driving region A and a second driving region B, and a pixel region P, which includes a switching region C and a storage region ST, are defined on a substrate **10**. A buffer layer **12** is formed on the substrate **10** by depositing silicon oxide (SiO_2).

[0019] First, second and third active patterns **14**, **16** and **18** are formed on the buffer layer **12** in the first driving region A, the second driving region B and the switching region C, respectively, through a first mask process. The first, second and third active patterns **14**, **16** and **18** are formed of polycrystalline silicon. Each of the first, second and third active patterns **14**, **16** and **18** includes an intrinsic portion V**1** and doped portions V**2**. The first and third active patterns **14** and **18** further include a lightly doped drain (LDD) portion F between the intrinsic portion V**1** and each doped portion V**2**. An extension portion **20** is also formed on the buffer layer **12** in the storage region ST. The extension portion **20** extends from the third active pattern **18**.

[0020] In FIGS. **5**A and **5**B, first, second and third photoresist patterns **22**, **24** and **26** are formed on the first, second and third active patterns **14**, **16** and **18**, respectively, by coating a photoresist material on the entire surface of the substrate **10** and then patterning the photoresist material through a second mask process. The extension portion **20** is not covered with the photoresist patterns **22**, **24** and **26** and is exposed. Next, n^+or p^+ion doping is performed in the exposed extension portion **20**. The doped extension portion **20** functions as an electrode for a storage capacitor. The first, second and third photoresist patterns **22**, **24** and **26** are removed.

[0021] In FIGS. **6**A and **6**B, a gate insulating layer **28** is formed on the substrate **10** including the doped extension portion **20** by depositing an inorganic insulating material such as silicon nitride (SiN_X) or silicon oxide (SiO_2). First, second and third gate electrodes **30**, **32** and **34** are formed on the gate insulating layer **28** by sequentially depositing and then patterning aluminum (Al) or an aluminum alloy such as AlNd through a third mask process. The first, second and third gate electrodes **30**, **32** and **34** correspond to the intrinsic portions of the first, second and third active patterns **14**, **16** and **18**, respectively. A storage line **36** is also formed on the gate insulating layer **28** over the extension portion **20** in the storage region ST. The extension portion **20** and the storage line **36** form a storage capacitor C_{ST} and function as first and second electrodes of the storage capacitor C_{ST}, respectively. Subsequently, n^-ion doping, in which n-type impurities are lightly doped, is carried out on the entire surface of the substrate **10** including the first, second and third gate electrodes **30**, **32** and **34**. Thus, n-type ions are lightly doped in the LDD portions F of the first and third active patterns **14** and **18** and the doped portions V**2** of the first, second and third active patterns **14**, **16** and **18**.

[0022] In FIGS. **7**A and **7**B, a photoresist material is coated on the entire surface of the substrate **10** where n^-ion doping is performed and then is patterned through a fourth mask process, to thereby form fourth, fifth and sixth photoresist patterns **38**, **40** and **42**. The fourth photoresist pattern **38** covers the first gate electrode **30** and the LDD portions F of the first active pattern **14**. The fifth photoresist pattern **40** covers the second gate electrode **32** and the second active pattern **16**. The sixth photoresist pattern **42** covers the third gate electrode **34** and the LDD portions F of the third active pattern **18**. Here, the doped portions V**2** of the first and third active patterns **14** and **18** are exposed. Next, n^+ion doping is performed on the entire surface of the substrate **10** including the fourth, fifth and sixth photoresist patterns **38**, **40** and **42**. Therefore, n-type ions are heavily doped in the doped portions V**2** of the first and third active patterns **14** and **18**. The fourth, fifth and sixth photoresist patterns **38**, **40** and **42** are then removed.

[0023] In FIGS. **8**A and **8**B, a photoresist material is coated on the substrate **10** where n^+ion doping is performed. Then, the photoresist material is patterned through a fifth mask process, to thereby form seventh and eighth photoresist patterns **44** and **46**. The seventh photoresist pattern **44** covers the first gate electrode **30** and the first active pattern **14**, and the eighth photoresist pattern **46** covers the third gate electrode **34** and the third active pattern **18**. The eighth photoresist pattern **46** also covers the storage line **36**. Subsequently, p^+ion doping is performed on the entire surface of the substrate **10** including the seventh and eighth photoresist patterns **44** and **46**, and p-type ions are heavily doped in the doped portions V**2** of the second active pattern **16**. The seventh and eighth photoresist patterns **44** and **46** are then removed.

[0024] In FIGS. **9**A and **9**B, an inter insulating layer **48** is formed on the entire surface of the substrate **10** where p^+ion doping is performed. The inter insulating layer **48** is patterned through a sixth mask process to form first, second, third, fourth, fifth and sixth contact holes **50**, **52**, **54**, **56**, **58** and **60**. The first and second contact holes **50** and **52** expose the doped portions V**2** of the first active pattern **14**, the third and fourth contact holes **54** and **56** expose the doped portions V**2** of the second active pattern **16**, and the fifth and sixth contact holes **58** and **60** expose the doped portions V**2** of the third active pattern **18**. The inter insulating layer **48** is formed of silicon oxide (SiO_2).

[0025] In FIGS. **10**A and **10**B, first source and drain electrodes **62** and **64**, second source and drain electrodes **66** and **68**, and third source and drain electrodes **70** and **72** are formed the inter insulating layer **48** by sequentially depositing and then patterning, a metallic material mentioned above through a seventh mask process. The first source and drain electrodes **62** and **64** contact the doped portions V**2** of the first active pattern **14** through the first and second contact holes **50** and **52**. The second source and drain electrodes **66** and **68** contact the doped portions V**2** of the second active pattern **16** through the third and fourth contact holes **54** and **56**. The third source and drain electrodes **70** and **72** contact the doped portions V**2** of the third active pattern **18** through the fifth and sixth contact holes **58** and **60**.

[0026] In FIGS. **11**A and **11**B, a passivation layer **74** is formed on the entire surface of the substrate **10** including the source electrodes **62**, **66** and **70** and the drain electrodes **64**, **68** and **72** thereon. The passivation layer **74** is patterned through an eighth mask process to thereby form a drain contact hole **76**. The drain contact hole **76** exposes the third drain electrode **72** in the switching region C.

[0027] In FIGS. **12**A and **12**B, a pixel electrode **78** is formed on the passivation layer **74** in the pixel region P by sequentially depositing and patterning a transparent conductive material through a ninth mask process. The pixel electrode **78** contacts the third drain electrode **72** through the drain contact hole **76**.

[0028] The array substrate of the related art may be fabricated through the above-mentioned mask processes. However, problems may frequently occur because the related art array substrate is fabricated through a large number of mask processes, each mask process including several steps, such as cleaning, coating a photoresist layer, exposing through a mask, developing the photoresist layer, and etching. In addition, manufacturing time and costs are increased, and productivity of the processes is lowered.

SUMMARY OF THE INVENTION

[0029] Accordingly, the present invention is directed to an array substrate for a liquid crystal display device and a method of manufacturing the same that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

[0030] An object of the present invention is to provide an array substrate having driver integrated circuits and a method of manufacturing the same at a low cost.

[0031] Another object of the present invention is to provide an array substrate having driver integrated circuits and a method of manufacturing the same using reduced number of processes.

[0032] Another object of the present invention is to provide an array substrate having driver integrated circuits and a method of manufacturing the same that increase productivity.

[0033] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0034] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for a liquid crystal display device includes a substrate including a first driving region, a second driving region, and a pixel region, the pixel region including a switching region and a storage region; a first n-type transistor in the first driving region, a second p-type transistor in the second driving region; a third transistor in the switching region, the third transistor including a gate electrode, an active layer, a source electrode, and a drain electrode; an extension portion in the storage region and extending from the active layer; a metal pattern on the extension portion; a storage line over the metal pattern; and a pixel electrode in the pixel region and contacting the third transistor, wherein the metal pattern, the storage line and the pixel electrode form first, second and third electrodes of a storage capacitor, and wherein the storage capacitor includes a first capacitor and a second capacitor, the first capacitor parallel to the second capacitor.

[0035] In another aspect, a method of manufacturing a liquid crystal display device includes forming first, second and third active patterns, an extension portion and a metal pattern on a substrate using a first mask, the substrate having a driving region and a pixel region, the first and second active patterns disposed in first and second driving regions of the driving region, the third active pattern disposed in a switching region of the pixel region, and the extension portion and the metal pattern disposed in a storage region of the pixel region; forming a gate insulating layer on the substrate including the first, second and third active patterns, the extension portion and the metal pattern; forming first, second and third gate electrodes and a storage line on the gate insulating layer using a second mask, the first, second and third gate electrodes corresponding to center portions of the first, second and third active patterns, and the storage line disposed over the metal pattern; sequentially doping n^+ions and n^-ions in the first and third active patterns using a third mask; doping p^+ions into the second active pattern using a fourth mask; forming an inter insulating layer and a transparent conductive layer on the substrate including the p^+ion doped second active pattern; patterning the inter insulating layer and the transparent conductive layer using a fifth mask to thereby expose portions of the first, second and third active patterns and to form a pixel electrode in the pixel region; and forming first source and drain electrodes, second source and drain electrodes and third source and drain electrodes using a sixth mask, the first source and drain electrodes contacting the exposed portions of the first active pattern, the second source and drain electrodes contacting the exposed portions of the second active pattern, and the third source and drain electrodes contacting the exposed portions of the third active pattern.

[0036] In another aspect, a method of manufacturing a liquid crystal display device includes forming first, second and third active patterns, an extension portion and a metal pattern on a substrate using a first mask, the substrate having a first driving region, a second driving region, and a pixel region including a switching region and a storage region, the first and second active patterns disposed in the first and second driving regions, the third active pattern disposed in the switching region, and the extension portion and the metal pattern disposed in the storage region; forming a gate insulating layer on the substrate including the first, second and third active patterns, the extension portion and the metal pattern; doping n^+ions and n^-ions in the first and third active patterns and then forming first, second and third gate electrodes and a storage line on the gate insulating layer using a second mask, the first, second and third gate electrodes corresponding to center portions of the first, second and third active patterns, the storage line disposed over the metal pattern; doping p^+ions into the second active pattern using a third mask; forming an inter insulating layer and a transparent conductive layer on the substrate including the p^+ion doped second active pattern; patterning the inter insulating layer and the transparent conductive layer using a fourth mask to expose portions of the first, second and third active patterns and to form a pixel electrode in the pixel region; and forming first source and drain electrodes, second source and drain electrodes, and third source and drain electrodes using a fifth mask, the first source and drain electrodes contacting the exposed portions of the first active pattern, the second source and drain electrodes contacting the exposed portions of the second active pattern, the third source and drain electrodes contacting the exposed portions of the third active pattern.

[0037] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0039] FIG. **1** is a schematic view showing an array substrate of a liquid crystal display device having driver integrated circuits according to the related art.

[0040] FIG. **2** is a plan view illustrating a pixel region of an array substrate including a polycrystalline silicon thin film transistor according to the related art.

[0041] FIGS. **3**A and **3**B are cross-sectional views of an array substrate including driver ICs according to the related art.

[0042] FIGS. **4**A and **4**B to FIGS. **12**A and **12**B are cross-sectional views illustrating a manufacturing method of an array substrate including driver ICs according to the related art.

[0043] FIG. **13** is a plan view of an exemplary pixel region of an array substrate including a polycrystalline silicon thin film transistor according to an embodiment of the present invention.

[0044] FIG. **14**A is a cross-sectional view illustrating the formation of a metal layer in a driving region of the array substrate of FIG. **13** using a first mask process in accordance with an embodiment of the present invention.

[0045] FIG. **14**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a metal layer in a pixel region of the array substrate of FIG. **13** during the first mask process.

[0046] FIG. **15**A is a cross-sectional view of the formation of a photoresist pattern in a driving region of the array substrate of FIG. **13** during the first mask process.

[0047] FIG. **15**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the first mask process.

[0048] FIG. **16**A is a cross-sectional view of the formation of a metal pattern in a driving region of the array substrate of FIG. **13** during the first mask process.

[0049] FIG. **16**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a metal pattern in a pixel region of the array substrate of FIG. **13** during the first mask process.

[0050] FIG. **17**A is a cross-sectional view of an ashing of a photoresist pattern in a driving region of the array substrate of FIG. **13** during the first mask process.

[0051] FIG. **17**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating an ashing of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the first mask process.

[0052] FIG. **18**A is a cross-sectional view of the formation of a gate insulating layer in a driving region of the array substrate of FIG. **13** following the first mask process.

[0053] FIG. **18**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a gate insulating layer in a pixel region of the array substrate of FIG. **13** following the first mask process.

[0054] FIG. **19**A is a cross-sectional view of the formation of a plurality of electrodes in a driving region of the array substrate of FIG. **13** during a second mask process.

[0055] FIG. **19**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of an electrode and a storage line in a pixel region of the array substrate of FIG. **13** during the second mask process.

[0056] FIG. **20**A is a cross-sectional view of the formation of a photoresist pattern in a driving region of the array substrate of FIG. **13** during a third mask process.

[0057] FIG. **20**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the third mask process.

[0058] FIG. **21**A is a cross-sectional view showing an ion doping of a driving region of the array substrate of FIG. **13** during a third mask process.

[0059] FIG. **21**B is a cross-sectional view along line XIV-XIV of FIG. **13** showing an ion doping of a pixel region of the array substrate of FIG. **13** during the third mask process.

[0060] FIG. **22**A is a cross-sectional view of the formation of a photoresist pattern in a driving region of the array substrate of FIG. **13** during a fourth mask process.

[0061] FIG. **22**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the fourth mask process.

[0062] FIGS. **23**A and **24**A are cross-sectional views of the formation of a photoresist pattern in a driving region of the array substrate of FIG. **13** during a fifth mask process.

[0063] FIGS. **23**B and **24**B are cross-sectional views along line XIV-XIV of FIG. **13** illustrating the formation of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the fifth mask process.

[0064] FIG. **25**A is a cross-sectional view of the formation of a plurality of contact holes in a driving region of the array substrate of FIG. **13** during the fifth mask process.

[0065] FIG. **25**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a plurality of contact holes in a pixel region of the array substrate of FIG. **13** during the fifth mask process.

[0066] FIG. **26**A is a cross-sectional view of an ashing process performed in a driving region of the array substrate of FIG. **13** during the fifth mask process.

[0067] FIG. **26**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating an ashing process performed in a pixel region of the array substrate of FIG. **13** during the fifth mask process.

[0068] FIG. **27**A is a cross-sectional view of the formation of a plurality of electrodes in a driving region of the array substrate of FIG. **13** during a sixth mask process.

[0069] FIG. **27**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a plurality of electrodes in a pixel region of the array substrate of FIG. **13** during the sixth mask process.

[0070] FIGS. **28**A and **28**B to FIGS. **41**A and **41**B are cross-sectional views illustrating a manufacturing method of an array substrate including driver ICs according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0071] Reference will now be made in detail to the illustrated exemplary embodiments of the present invention, which are illustrated in the accompanying drawings.

[0072] FIG. **13** is a plan view of an exemplary pixel region of an array substrate including a polycrystalline silicon thin film transistor according to an embodiment of the present invention. Referring to FIG. **13**, one or more gate line GL is formed along a first direction on a substrate. One or more data line DL is formed on the substrate along a second direction perpendicular to the first direction. The one or more gate line GL and the one or more data line DL cross each other to define a pixel region P.

[0073] A thin film transistor T is formed at the crossing portion of the gate and data lines GL and DL. The thin film transistor T includes an active layer **118** of polycrystalline silicon, a gate electrode **130** over the active layer **118**, and source and drain electrodes **150***a* and **150***b* contacting the active layer **118**. A pixel electrode **140** is formed in the pixel region P and is connected to the drain electrode **150***b*.

[0074] A storage capacitor C^{ST} is also formed in the pixel region P. The storage capacitor C^{ST} includes two parallel capacitors. The first of the two parallel capacitors is formed by a metal pattern **122** and a storage line **132**. The second of the two parallel capacitors is formed by the storage line **132** and the pixel electrode **140**. The metal pattern **122** is disposed on an extension portion (not shown) extending from the active layer **118** and is electrically connected to the drain electrode **150***b*. The storage line **132** overlaps the metal pattern **122**. The pixel electrode **140** overlaps the storage line **132** and is connected the drain electrode **150***b*. Hereinafter, a method of manufacturing an array substrate including driver integrated circuits (ICs) according to an embodiment of the present invention will be explained with reference to attached drawings.

[0075] FIG. **14**A is a cross-sectional view illustrating the formation of a metal layer in a driving region of the array substrate of FIG. **13** using a first mask process in accordance with an embodiment of the present invention. FIG. **14**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a metal layer in a pixel region of the array substrate of FIG. **13** during the first mask process. Referring to FIG. **14**A, a first driving region A and a second driving region B are defined on a substrate **100**. Referring to FIG. **14**B, a pixel region P, which includes a switching region C and a storage region ST, is defined on the substrate **100**. A buffer layer **102** is formed on the substrate **100**, including the first and second driving regions A and B, and the pixel region P, by depositing, for example, silicon nitride (SiN_X) or silicon oxide (SiO_2). A polycrystalline silicon layer **104** and a metal layer **106** are formed on the buffer-layer **102**. The polycrystalline silicon layer **104** may be formed by sequentially depositing, dehydrogenating, and crystallizing amorphous silicon (a-Si:H).

[0076] Next, a photoresist layer **108** is formed on the metal layer **106** by coating a photoresist material. A mask M1 is disposed over the photoresist layer **108**. The mask M1 includes a transmitting portion E1, a blocking portion E2 and a half transmitting portion E3. The half transmitting portion E3 may include a semitransparent film or slits. The half transmitting portion E3 corresponds to the first driving region A, the second driving region B and the switching region C. The blocking portion E2 corresponds to the storage region ST, and the transmitting portion E1 corresponds to the other regions. The photoresist layer **108** is exposed to light through the mask M1. Then, the photoresist layer **108** is developed.

[0077] FIG. **15**A is a cross-sectional view of the formation of a photoresist pattern in a driving region of the array substrate of FIG. **13** during the first mask process. FIG. **15**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the first mask process. Referring to FIGS. **15**A and **15**B, first, second, third and fourth photoresist patterns **110***a*, **110***b*, **110***c* and **112** are formed. The first, second, and third photoresist patterns **110***a*, **110***b* and **110***c* are formed in the first driving region A, the second driving region B and the switching region C, respectively. The first, second, and third photoresist patterns **110***a*, **110***b* and **110***c* have a first thickness. The fourth photoresist pattern **112** is formed in the storage region ST and is thicker than the first to third photoresist patterns **110***a*, **110***b* and **110***c*. The first to fourth photoresist patterns **110***a*; **110***b*, **110***c*, and **112** expose portions of the metal layer **106** in the pixel region P and the first and second driving regions A and B.

[0078] FIG. **16**A is a cross-sectional view of the formation of a metal pattern in a driving region of the array substrate of FIG. **13** during the first mask process. FIG. **16**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a metal pattern in a pixel region of the array substrate of FIG. **13** during the first mask process. Referring to FIGS. **16**A and **16**B, the exposed portions of the metal layer **106** and the polycrystalline silicon layer **104** thereunder are removed. The metal layer **106** may be removed by a wet etch method. The polycrystalline silicon layer **104** may be removed by a dry etch method. The remaining pattern on the buffer layer **102** in the first driving region A includes a polycrystalline silicon patterned layer **114**, the metal patterned layer **106**, and the photoresist pattern **110***a* in stacking order. The remaining pattern on the buffer layer **102** in the second driving region B includes a polycrystalline silicon patterned layer **116**, a metal patterned layer **106**, and the photoresist pattern **110***b* in stacking order. The remaining pattern on the buffer layer **102** in the switching region C of the pixel region P includes a polycrystalline silicon patterned layer **118**, the metal patterned layer **106**, and the photoresist pattern **110***c* in stacking order. The remaining pattern on the buffer layer **102** in the storage region ST of the pixel region P includes a polycrystalline silicon patterned layer **120**, the metal patterned layer **122**, and the photoresist pattern **112** in stacking order.

[0079] FIG. **17**A is a cross-sectional view of an ashing process of a photoresist pattern in a driving region of the array substrate of FIG. **13** during the first mask process. FIG. **17**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating an ashing of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the first mask process. Referring to FIGS. **17**A and **17**B, an ashing process is performed. The first, second and third photoresist patterns **110***a*, **110***b* and **110***c* shown in FIGS. **16**A and **16**B are removed by the ashing process, thereby exposing the metal layer **106** in the first driving region A, the second driving region B and the switching region C. The thickness of the fourth photoresist pattern **112** is also reduced by the ashing process.

[0080] FIG. **18**A is a cross-sectional view of the formation of a gate insulating layer in a driving region of the array substrate of FIG. **13** following the first mask process. FIG. **18**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a gate insulating layer in a pixel region of the array substrate of FIG. **13** following the first mask process. Referring to FIGS. **18**A and **18**B, the exposed metal layer **106** is removed from the first and second driving regions A and B and the switching region C, and the fourth photoresist pattern **112** is removed from the storage region ST. First, second, and third active patterns **114**, **116**, and **118** are formed on the buffer layer **102** in the first driving region A, the second driving region B, and the switching region C, respectively. An extension portion **120** and a metal pattern **122** are formed on the buffer layer **102** in the storage region ST. The extension portion **120** extends from the third active pattern **118**, and the metal pattern **122** is disposed on the extension portion **120**. Each of the first, second and third active patterns **114**, **116** and **118** includes an intrinsic portion V1 and doped portions V2 at both sides of the intrinsic portion V1. The first and third active patterns **114** and **118** further include a lightly doped drain (LDD) portion F between the intrinsic portion V1 and each doped portion V2. Then, a gate insulating layer **124** is formed on the entire surface of the substrate **100** covering the first, second and third active patterns **114**, **116** and **118**, the extension portion **120** and the metal pattern **122** thereon. The gate insulating layer **124** may be formed of an inorganic insulating material such as silicon nitride (SiN_X) or silicon oxide (SiO_2).

[0081] FIG. **19**A is a cross-sectional view of the formation of a plurality of electrodes in a driving region of the array substrate of FIG. **13** during a second mask process. FIG. **19**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of an electrode and a storage line in a pixel region of the array substrate of FIG. **13** during the second mask process. Referring to FIGS. **19**A and **19**B, first, second and third gate electrodes **126**, **128** and **130** and a storage line **132** are formed on the gate insulating layer **124** by sequentially depositing and patterning a metallic material through a second mask process. The metallic material may include aluminum (Al), an aluminum alloy (AlNd), copper (Cu), molybdenum (Mo), tungsten (W) or chromium (Cr). The first, second and third gate electrodes **126**, **128** and **130** correspond to the intrinsic portions V1 of the first, second and third active patterns **114**, **116** and **118**, respectively. The storage line **132** is disposed over the metal pattern **122** in the storage region ST. As shown in FIG. **13**, the storage line **132** crosses the pixel region P. Concurrently, a gate line GL (shown in FIG. **13**) is formed and is connected to the third gate electrode **130** in the switching region C.

[0082] FIG. **20**A is a cross-sectional view of the formation of a photoresist pattern in a driving region of the array substrate of FIG. **13** during a third mask process. FIG. **20**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the third mask process. Referring to FIGS. **20**A and **20**B, a photoresist material is coated on the entire surface of the substrate **100** to cover the first, second and third gate electrodes **126**, **128** and **130** and the storage line **132**. Then, the photoresist material is patterned through a third mask process to form fifth, sixth and seventh photoresist patterns **134***a*, **134***b* and **134***c*. The fifth photoresist pattern **134***a* covers the first gate electrode **126** and the LDD portions F of the first active pattern **114**. The sixth photoresist pattern **134***b* covers the third gate electrode **130** and the LDD portions F of the third active pattern **118**. The seventh photoresist pattern **134***c* covers the second gate electrode **128** and the second active pattern **116**. Here, the doped portions V2 of the first and third active patterns **114** and **118** are exposed. In this embodiment of the present invention, no resist pattern is formed in the pixel region P excluding the switching region C. In another embodiment of the present invention, another photoresist pattern may be formed in the pixel region P excluding the switching region C. Next, n^+ion doping is performed on the entire surface of the substrate **100**, including the fifth, sixth and seventh photoresist patterns **134***a*, **134***b* and **134***c*. Therefore, n-type ions are heavily doped in the doped portions V2 of the first and third active patterns **114** and **118**.

[0083] FIG. **21**A is a cross-sectional view showing an ion doping of a driving region of the array substrate of FIG. **13** during a third mask process. FIG. **21**B is a cross-sectional view along line XIV-XIV of FIG. **13** showing an ion doping of a pixel region of the array substrate of FIG. **13** during the third mask process. Referring to FIGS. **21**A and **21**B, the fifth, sixth and seventh photoresist patterns **134***a*, **134***b* and **134***c* are removed, and the first, second and third gate electrodes **126**, **128** and **130** are exposed. N^-ion doping is carried out on the entire surface of the substrate **100** where n^+doping was performed. Here, the first, second and third gate electrodes **126**, **128** and **130** are used as a doping mask. Thus, the LDD portions F of the first and third active patterns **114** and **118** and the doped portions V2 of the first, second and third active patterns **114**, **116** and **118** are lightly doped with n-type ions. The doped portions V2 of the first and third active patterns **114** and **118** are heavily doped with n-type ions, because the n^-ion doping process doped more n-type ions in the doped portions V2 of the first and third active patterns **114** and **118**.

[0084] FIG. **22**A is a cross-sectional view of the formation of a photoresist pattern in a driving region of the array substrate of FIG. **13** during a fourth mask process. FIG. **22**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the fourth mask process. Referring to FIGS. **22**A and **22**B, a photoresist material is coated on the entire surface of the substrate **100** where n^-ion doping was performed. The photoresist material is patterned through a fourth mask process to form an eighth photoresist pattern **136**. The eighth photoresist pattern **136** covers the first driving region A and the pixel region P and exposes the second driving region B.

[0085] Subsequently, p^+ion doping is performed on the entire surface of the substrate **100** including the eighth photoresist pattern **136** thereon, and p-type ions are heavily doped in the doped portions V2 of the second active pattern **116**. Although the n-type ions are doped in the doped portions V2 of the second active pattern **116**, there is no influence of the n-type ions because the concentration of the p-type ions is extremely high compared to the n-type ions.

[0086] FIGS. **23**A and **24**A are cross-sectional views of the formation of a photoresist pattern in a driving region of the array substrate of FIG. **13** during a fifth mask process. FIGS. **23**B and **24**B are cross-sectional views along line XIV-XIV of FIG. **13** illustrating the formation of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the fifth mask process. Referring to FIGS. **23**A and **23**B, the eighth photoresist pattern **136** shown in FIGS. **22**A and **22**B is removed. An inter insulating layer **138** and a transparent conductive layer **140** are sequentially formed on the entire surface of the substrate **100** where p^+ion doping is performed, including the first, second and third gate electrodes **126**, **128** and **130**, and the storage line **132**. The inter insulating layer **138** is formed of an inorganic insulating material, such as silicon nitride (SiN_X) or silicon oxide (SiO_2). The transparent conductive layer **140** is formed of a transparent conductive material, such as indium tin oxide (ITO) or indium zinc oxide (IZO).

[0087] A photoresist layer **142** is formed on the transparent conductive layer **140** by coating a photoresist material. A mask M2 is disposed over the photoresist layer **142**. The mask M2 includes a transmitting portion H1, a blocking portion H2 and a half transmitting portion H3. The transmitting portion H1 corresponds to the doped portions V2 of the first, second and third active patterns **114**, **116** and **118**. The blocking portion H2 corresponds to the pixel region P, and the half transmitting portion H3 corresponds to the other regions. The photoresist layer **142** is exposed to light through the mask M2 and developed. Accordingly, as illustrated in FIGS. **24**A and **24**B, ninth and tenth photoresist patterns **144***a* and **144***b* are formed. The ninth photoresist pattern **144***a* is disposed in the first driving region A, the second driving region B, and the switching region C, and exposes portions of the transparent conductive layer **140** corresponding to the doped portions V2 of the first, second and third active patterns **114**, **116** and **118**. The tenth photoresist pattern **144***b* is disposed in the pixel region P excluding the switching region C. The tenth photoresist pattern **144***b* is thicker than the ninth photoresist pattern **144***a*.

[0088] FIG. **25**A is a cross-sectional view of the formation of a plurality of contact holes in a driving region of the array substrate of FIG. **13** during the fifth mask process. FIG. **25**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a plurality of contact holes in a pixel region of the array substrate of FIG. **13** during the fifth mask process. Referring to FIGS. **25**A and **25**B, the exposed portions of the transparent conductive layer **140**, and the inter insulating layer **138** and the gate insulating layer **124** underneath, are sequentially removed. Thereby, first, second, third, fourth, fifth and sixth contact holes **145***a*, **145***b*, **145***c*, **145***d*, **145***e* and **145***f* are formed. The contact holes **145***a*, **145***b*, **145***c*, **145***d*, **145***e* and **145***f* expose the doped portions V2 of the first, second and third active patterns **114**, **116** and **118**. Although not shown, a contact hole is also formed through the fifth mask process to expose the metal pattern **122**.

[0089] FIG. **26**A is a cross-sectional view of an ashing process performed in a driving region of the array substrate of FIG. **13** during the fifth mask process. FIG. **26**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating an ashing process performed in a pixel region of the array substrate of FIG. **13** during the fifth mask process. Referring to FIGS. **26**A and **26**B, the ninth photoresist pattern **144***a* of FIGS. **25**A and **25**B is removed through an ashing process, and the transparent conductive layer **140** of FIGS. **25**A and **25**B is exposed in the first driving region A, the second driving region B and the switching region C. The thickness of the tenth photoresist pattern **144***b* is reduced, and an edge of the tenth photoresist pattern **144***b* is removed. Then, the exposed transparent conductive layer **140** of FIGS. **25**A and **25**B is removed to thereby expose the inter insulating layer **138** in the first driving region A, the second driving region B and the switching region C.

[0090] FIG. **27**A is a cross-sectional view of the formation of a plurality of electrodes in a driving region of the array substrate of FIG. **13** during a sixth mask process. FIG. **27**B is a cross-sectional view along line XIV-XIV of FIG. **13** illustrating the formation of a plurality of electrodes in a pixel region of the array substrate of FIG. **13** during the sixth mask process. Referring to FIGS. **27**A and **27**B, the tenth photoresist pattern **144***b* (shown in FIG. **26**B) is removed, exposing the transparent conductive layer **140** in the pixel region P. The exposed transparent conductive layer **140** becomes a pixel electrode **140**. First source and drain electrodes **146***a* and **146***b*, second source and drain electrodes **148***a* and **148***b*, and third source and drain electrodes **150***a* and **150***b* are formed on the substrate **100** including the pixel electrode **140** thereon by sequentially depositing and patterning a metallic material through a sixth mask process. The metallic material can be, for example, chromium (Cr), molybdenum (Mo), tungsten (W), titanium (Ti), aluminum (Al), an aluminum alloy such as AlNd, or copper (Cu).

[0091] The first source and drain electrodes **146***a* and **146***b* contact the doped portions V2 of the first active pattern **114** through the first and second contact holes **145***a* and **145***b*, respectively. The second source and drain electrodes **148***a* and **148***b* contact the doped portions V2 of the second active pattern **116** through the third and fourth contact holes **145***c* and **145***d*, respectively. The third source and drain electrodes **150***a* and **150***b* contact the doped portions V2 of the third active pattern **118** through the fifth and sixth contact holes **145***e* and **145***f*, respectively. The third drain electrode **150***b* contacts the pixel electrode **140**. Although not shown, the third drain electrode **150***b* also contacts the metal pattern **122**. Thus, the metal pattern **122**, the storage line **132** and the pixel electrode **140** function as first, second and third electrodes to form a storage capacitor C_{ST}. In this embodiment of the present invention, the storage capacitor C_{ST} includes two parallel capacitors. In this embodiment of the present invention, the array substrate including the driver ICs is manufactured through six-mask processes.

[0092] FIG. **28**A is a cross-sectional view illustrating the formation of a metal layer in a driving region of an array substrate using a first mask process in accordance with another embodiment of the present invention. FIG. **28**B is a cross-sectional view illustrating the formation of a metal layer in a pixel region of the array substrate of FIG. **13** during the first mask process. Referring to FIG. **28**A, a first driving region A and a second driving region B are defined on a substrate **200**. Referring to FIG. **28**B, a pixel region P, which includes a switching region C and a storage region ST, is defined on the substrate **200**. A buffer layer **202** is formed on the substrate **200**, including the first and second driving regions A and B, and the pixel region P, by depositing, for example, silicon nitride (SiN_X) or silicon oxide (SiO_2). A polycrystalline silicon layer **204** and a metal layer **206** are formed on the buffer layer **202**. The polycrystalline silicon layer **204** may be formed by sequentially depositing, dehydrogenating, and crystallizing amorphous silicon (a-Si:H).

[0093] Next, a photoresist layer **208** is formed on the metal layer **206** by coating a photoresist material. A mask M1 is disposed over the photoresist layer **208**. The mask M1 includes a transmitting portion E1, a blocking portion E2 and a half transmitting portion E3. The half transmitting portion E3 may include a semitransparent film or slits. The half transmitting portion E3 corresponds to the first driving region A, the second driving region B and the switching region C. The blocking portion E2 corresponds to the storage region ST, and the transmitting portion E1 corresponds to the other regions. The photoresist layer **208** is exposed to light through the mask M1. Then, the photoresist layer **208** is developed.

[0094] FIG. **29**A is a cross-sectional view of the formation of a photoresist pattern in a driving region of an array substrate during the first mask process. FIG. **29**B is a cross-sectional view illustrating the formation of a photoresist pattern in a pixel region of the array substrate during the first mask process. Referring to FIGS. **29**A and **29**B, first, second, third and fourth photoresist patterns **210***a*, **210***b*, **210***c* and **212** are formed. The first, second, and third photoresist patterns **210***a*, **210***b* and **210***c* are formed in the first driving region A, the second driving region B and the switching region C, respectively. The first, second, and third photoresist patterns **210***a*, **210***b* and **210***c* have a first thickness. The fourth photoresist pattern **212** is formed in the storage region ST and is thicker than the first to third photoresist patterns **210***a*, **210***b* and **210***c*. The first to fourth photoresist patterns **210***a*, **210***b*, **210***c*, and **212** expose portions of the metal layer **206** in the pixel region P and the first and second driving regions A and B.

[0095] FIG. **30**A is a cross-sectional view of the formation of a metal pattern in a driving region of an array substrate during the first mask process. FIG. **30**B is a cross-sectional view illustrating the formation of a metal pattern in a pixel region of the array substrate of FIG. **13** during the first mask process. Referring to FIGS. **30**A and **30**B, the exposed portions of the metal layer **206** and the polycrystalline silicon layer **204** thereunder are removed. The metal layer **206** may be removed by a wet etch method. The polycrystalline silicon layer **204** may be removed by a dry etch method. The remaining pattern on the buffer layer **202** in the first driving region A includes a polycrystalline silicon patterned layer **214**, a metal patterned layer **206**, and the photoresist pattern **210***a* in stacking order. The remaining pattern on the buffer layer **202** in the second driving region B includes a polycrystalline silicon patterned layer **216**, a metal patterned layer **206**, and the photoresist pattern **210***b* in stacking order. The remaining pattern on the buffer layer **202** in the switching region C of the pixel region includes a polycrystalline silicon patterned layer **218**, a metal patterned layer **206**, and the photoresist pattern **210***c* in stacking order. The remaining pattern on the buffer layer **202** in the storage region ST of the pixel region includes a polycrystalline silicon patterned layer **220**, a metal patterned layer **222**, and the photoresist pattern **212** in stacking order.

[0096] FIG. **31**A is a cross-sectional view of an ashing of a photoresist pattern in a driving region of an array substrate during the first mask process. FIG. **31**B is a cross-sectional view illustrating an ashing of a photoresist pattern in a pixel region of the array substrate of FIG. **13** during the first mask process. Referring to FIGS. **31**A and **31**B, an ashing process is performed. The first, second and third photoresist patterns **210***a*, **210***b* and **210***c* from FIGS. **30**A and **30**B are removed by the ashing process, thereby exposing the metal layer **206** in the first driving region A, the second driving region B and the switching region C. The thickness of the fourth photoresist pattern **212** is also reduced by the ashing process.

[0097] FIG. **32**A is a cross-sectional view of the formation of a gate insulating layer in a driving region of an array substrate following the first mask process. FIG. **32**B is a cross-sectional view illustrating the formation of a gate insulating layer in a pixel region of the array substrate of FIG. **13** following the first mask process. Referring to FIGS. **32**A and **32**B, the exposed metal layer **206** is removed from the first and second driving regions A and B and the switching region C, and the fourth photoresist pattern **212** is removed from the storage region ST. First, second, and third active patterns **214**, **216**, and **218** are formed on the buffer layer **202** in the first driving region A, the second driving region B, and the switching region C, respectively. An extension portion **220** and a metal pattern **222** are formed on the buffer layer **202** in the storage region ST. The extension portion **220** extends from the third active pattern **218**, and the metal pattern **222** is disposed on the extension portion **220**. Each of the first, second and third active patterns **214**, **216** and **218** includes an intrinsic portion V1 and doped portions V2 at both sides of the intrinsic portion V1. The first and third active patterns **214** and **218** further include a lightly doped drain (LDD) portion F between the intrinsic portion V1 and each doped portion V2. Then, a gate insulating layer **224** is formed on the entire surface of the substrate **200** covering the first, second and third active patterns **214**, **216** and **218**, the extension portion **220** and the metal pattern **222** thereon. The gate insulating layer **224** may be formed of an inorganic insulating material such as silicon nitride (SiN_X) or silicon oxide (SiO_2).

[0098] FIG. **33**A is a cross-sectional view of the formation of a plurality of electrodes in a driving region of an array substrate during a second mask process. FIG. **33**B is a cross-sectional view illustrating the formation of an electrode and a storage line in a pixel region of the array substrate during the second mask process. Referring to FIGS. **33**A and **33**B, a metallic material (not shown) is deposited on the gate insulating layer **224**. Next, photoresist is coated on the metallic material and then is patterned through a second mask process to thereby form fifth, sixth, seventh and eighth photoresist patterns **225***a*, **225***b*, **225***c* and **225***d*. The metallic material is etched by using the fifth, sixth, seventh and eighth photoresist patterns **225***a*, **225***b*, **225***c* and **225***d*. Thus, first, second and third gate electrodes **226**, **228** and **230** and a storage line **232** are formed on the gate insulating layer **224**. The metallic material may include aluminum (Al), an aluminum alloy (AlNd), copper (Cu), molybdenum (Mo), tungsten (W) or chromium (Cr). The first, second and third gate electrodes **226**, **228** and **230** correspond to the intrinsic portions V1 of the first, second and third active patterns **214**, **216** and **218**, respectively. The first and third gate electrodes **226** and **230** also cover the LDD portions F of the first and third active patterns **214** and **218**. The second gate electrode **228** partially covers the doped portions V2 of the second active pattern **216**. The storage line **232** is disposed over the metal pattern **222** in the storage region ST. The storage line **232** may cross the pixel region P similarly to the storage line **132** in FIG. **13**. Concurrently, a gate line GL (shown in FIG. **13**) is formed and is connected to the third gate electrode **230** in the switching region C.

[0099] Next, n^+ion doping is performed on the entire surface of the substrate **200** including the fifth, sixth, seventh and eighth photoresist patterns **225***a*, **225***b*, **225***c* and **225***d*. Therefore, n-type ions are heavily doped in the doped portions V2 of the first and third active patterns **214** and **218** and in parts of the doped portions V2 of the second active pattern **216**.

[0100] Referring to FIGS. **34**A and **34**B, the fifth and seventh photoresist patterns **225***a* and **225***c* are partially removed by performing an ashing process such that peripheral portions of the first and third gate electrodes **226** and **230** corresponding to the LDD portions F of the first and third active patterns **214** and **218** are exposed. At this time, the sixth and eighth photoresist patterns **225***b* and **225***d* are also removed, and peripheral portions of the second gate electrode **228** and the storage line **232** are exposed. The exposed peripheral portions of the second gate electrode **228** and the storage line **232** have the same width as the exposed portions of the first and third gate electrodes **226** and **230**.

[0101] Referring to FIGS. **35**A and **35**B, the exposed peripheral portions of the first, second and third gate electrodes **226**, **228** and **230** and the storage line **232** of FIGS. **34**A and **34**B are removed. Thus, portions of the gate insulating layer **224** corresponding to the LDD regions F of the first and third active patterns **214** and **218** are exposed. Additionally, portions of the gate insulating layer **224** corresponding to the doped portions V2 of the second active pattern **216** are entirely exposed. The storage line **232** has a reduced width.

[0102] Next, n^-ion doping is carried out on the entire surface of the substrate **200**. Here, the first, second and third gate electrodes **226**, **228** and **230** are used as a doping mask. Thus, n-type ions are lightly doped in the LDD portions F of the first and third active patterns **214** and **218** and the doped portions V2 of the first, second and third active patterns **214**, **216** and **218**. Since n-type ions are heavily doped in the doped portions V2 of the first and third active patterns **214**

and **218**, n-type ions are more doped in the doped portions V**2** of the first and third active patterns **214** and **218** by the n^-ion doping. The fifth, sixth, seventh and eighth photoresist patterns **225***a*, **225***b*, **225***c* and **225***d* are removed.

[0103] FIG. **36**A is a cross-sectional view of the formation of a photoresist pattern in a driving region of an array substrate during a third mask process. FIG. **36**B is a cross-sectional view illustrating the formation of a photoresist pattern in a pixel region of the array substrate during the third mask process. Referring to FIGS. **36**A and **36**B, photoresist is coated on the entire surface of the substrate **200** where n^-ion doping is performed. Then, the photoresist is patterned through a third mask process to thereby form a ninth photoresist pattern **236**. The ninth photoresist pattern **236** covers the first driving region A and the pixel region P and exposes the second driving region B.

[0104] Subsequently, p^+ion doping is performed on the entire surface of the substrate **200** including the ninth photoresist pattern **236** thereon, and p-type ions are heavily doped in the doped portions V**2** of the second active pattern **216**. At this time, a concentration of the p-type ions should be about 2.5 times the concentration of the n-type ions in the n^+ion doping. Therefore, although the n-type ions are doped in the doped portions V**2** of the second active pattern **216**, there is no influence of the n-type ions because the concentration of the p-type ions is higher than the concentration of the n-type ions. Accordingly, through the second and third mask processes, n-type ions are lightly doped in the LDD portions F of the first and the third active patterns **214** and **218**; n-type ions are heavily doped in the doped portions V**2** of the first and third active patterns **214** and **218**; and p-type ions are heavily doped in the doped portions V**2** of the second active pattern **216**.

[0105] FIGS. **37**A and **38**A are cross-sectional views of the formation of a photoresist pattern in a driving region of the array substrate during a fourth mask process. FIGS. **37**B and **38**B are cross-sectional views illustrating the formation of a photoresist pattern in a pixel region of the array substrate during the fourth mask process. Referring to FIGS. **37**A and **37**B, the ninth photoresist pattern **236** shown in FIGS. **36**A and **36**B is removed. An inter insulating layer **238** and a transparent conductive layer **240** are sequentially formed on the entire surface of the substrate **200** where p^+ion doping is performed. The inter insulating layer **238** is formed of an inorganic insulating material, such as silicon nitride (SiN_X) or silicon oxide (SiO_2). The transparent conductive layer **240** is formed of a transparent conductive material, such as indium tin oxide (ITO) or indium zinc oxide (IZO).

[0106] A photoresist layer **242** is formed on the transparent conductive layer **240** by coating a photoresist material. A mask M**2** is disposed over the photoresist layer **242**. The mask M**2** includes a transmitting portion H**1**, a blocking portion H**2** and a half transmitting portion H**3**. The transmitting portion H**1** corresponds to the doped portions V**2** of the first, second and third active patterns **214**, **216** and **218**. The blocking portion H**2** corresponds to the pixel region P, and the half transmitting portion H**3** corresponds to the other regions. The photoresist layer **242** is exposed to light through the mask M**2** and developed. Accordingly, as illustrated in FIGS. **38**A and **38**B, tenth and eleventh photoresist patterns **246** and **248** are formed. The tenth photoresist pattern **246** is disposed in the first driving region A, the second driving region B, and the switching region C, and exposes portions of the transparent conductive layer **240** corresponding to the doped portions V**2** of the first, second and third active patterns **214**, **216** and **218**. The eleventh photoresist pattern **248** is disposed in the pixel region P excluding the switching region C. The eleventh photoresist pattern **248** is thicker than the tenth photoresist pattern **246**.

[0107] FIG. **39**A is a cross-sectional view of the formation of a plurality of contact holes in a driving region of the array substrate during the fourth mask process. FIG. **39**B is a cross-sectional view illustrating the formation of a plurality of contact holes in a pixel region of the array substrate during the fourth mask process. Referring to FIGS. **39**A and **39**B, the exposed transparent conductive layer **240** and the underlying layers, including the inter insulating layer **238** and the gate insulating layer **224**, are sequentially removed to thereby form first, second, third, fourth, fifth and sixth contact holes **249***a*, **249***b*, **249***c*, **249***d*, **249***e* and **249***f* exposing the doped portions V**2** of the first, second and third active patterns **214**, **216** and **218**. Although not shown, a contact hole is also formed through the fourth mask process to expose the metal pattern **222**.

[0108] Referring to FIGS. **40**A and **40**B, the tenth photoresist pattern **246** shown in FIGS. **39**A and **39**B is removed through an ashing process, and the transparent conductive layer **240** of FIGS. **39**A and **39**B is exposed in the first driving region A, the second driving region B and the switching region C. At this time, the thickness of the eleventh photoresist pattern **248** is reduced, and an edge of the eleventh photoresist pattern **248** is removed. Next, the exposed transparent conductive layer **240** of FIGS. **39**A and **39**B is removed to thereby expose the inter insulating layer **238** in the first driving region A, the second driving region B and the switching region C. Then, the eleventh photoresist pattern **248** is removed, and the transparent conductive layer **240** in the pixel region P becomes a pixel electrode **240**.

[0109] FIG. **41**A is a cross-sectional view of the formation of a plurality of electrodes in a driving region of the array substrate during a fifth mask process. FIG. **41**B is a cross-sectional view illustrating the formation of a plurality of electrodes in a pixel region of the array substrate during the fifth mask process. Referring to FIGS. **41**A and **41**B, first source and drain electrodes **250***a* and **250***b*, second source and drain electrodes **252***a* and **252***b*, and third source and drain electrodes **254***a* and **254***b* are formed on the substrate **200** including the pixel electrode **240** thereon by sequentially depositing and patterning a metallic material through a fifth mask process. The metallic material includes chromium (Cr), molybdenum (Mo), tungsten (W), titanium (Ti), aluminum (Al), an aluminum alloy such as AlNd, or copper (Cu). The first source and drain electrodes **250***a* and **250***b* contact the doped portions V**2** of the first active pattern **214** through the first and second contact holes **249***a* and **249***b*. The second source and drain electrodes **252***a* and **252***b* contact the doped portions V**2** of the second active pattern **216** through the third and fourth contact holes **249***c* and **249***d*. The third source and drain electrodes **254***a* and **254***b* contact the doped portions V**2** of the third active patterns **218** through the fifth and sixth contact holes **249***e* and **249***f*. The third drain electrode **254***b* contacts the pixel electrode **240**. Although not shown, the third drain electrode **254***b* also contacts the metal pattern **222**. Therefore, the metal pattern

222, the storage line **232** and the pixel electrode **240** function as first, second and third electrodes to form a storage capacitor C_{ST}. The storage capacitor C_{ST} includes two parallel capacitors.

[0110] According to an other embodiment of the present invention, the array substrate including driver ICs may be manufactured through five-mask processes. Thus, the reduced number of processes lowers occurrence of problems. Manufacturing time is shortened, and manufacturing costs are reduced. Additionally, productivity of the device is improved.

[0111] It will be apparent to those skilled in the art that various modifications and variations can be made in the array substrate for liquid crystal display device and the method of manufacturing the same of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

1. An array substrate for a liquid crystal display device, comprising:

a substrate including a first driving region, a second driving region, and a pixel region, the pixel region including a switching region and a storage region;

a first n-type transistor in the first driving region, a second p-type transistor in the second driving region;

a third transistor in the switching region, the third transistor including a gate electrode, an active layer, a source electrode, and a drain electrode;

an extension portion in the storage region and extending from the active layer;

a metal pattern on the extension portion;

a storage line over the metal pattern; and

a pixel electrode in the pixel region and contacting the third transistor.

2. The array substrate according to claim 1, wherein the metal pattern, the storage line and the pixel electrode form first, second and third electrodes of a storage capacitor, and wherein the storage capacitor includes a first capacitor and a second capacitor, the first capacitor parallel to the second capacitor.

3. The array substrate according to claim 1, further comprising a gate line connected to the gate electrode and a data line connected to the source electrode.

4. The array substrate according to claim 1, wherein the active layer and the extension portion include polycrystalline silicon.

5. The array substrate according to claim 1, wherein the drain electrode electrically contacts the metal pattern and the pixel electrode.

6. The array substrate according to claim 2, wherein the first capacitor is formed by the metal pattern and the storage line, and the second capacitor is formed by the storage line and the pixel electrode.

7. The array substrate according to claim 1, wherein the first n-type transistor and the third transistor in the switching region have substantially the same structure.

8-26. (canceled)

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专利名称(译)	用于液晶显示装置的阵列基板及其制造方法		
公开(公告)号	US20070268419A1	公开(公告)日	2007-11-22
申请号	US11/878426	申请日	2007-07-24
[标]申请(专利权)人(译)	杨JOON YOUNG		
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IPC分类号	G02F1/1343		
CPC分类号	G02F1/13454 G02F1/136213 H01L27/1288 H01L29/78621 H01L27/1255 G02F2001/136236		
优先权	1020040061047 2004-08-03 KR		
其他公开文献	US7701521		
外部链接	Espacenet USPTO		

摘要(译)

一种液晶显示装置用阵列基板，包括：基板，包括第一驱动区域，第二驱动区域和像素区域;所述像素区域包括开关区域和存储区域;第一驱动区域中的第一n型晶体管，第二驱动区域中的第二p型晶体管;开关区域中的第三晶体管，第三晶体管包括栅电极，有源层，源电极和漏电极;存储区域中的延伸部分并从有源层延伸;延伸部分上的金属图案;金属图案上方的储存线;像素区域中的像素电极并与第三晶体管接触，其中金属图案，存储线和像素电极形成存储电容器的第一，第二和第三电极，该存储电容器包括彼此平行的第一电容器和第二电容器。