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(54) **THIN FILM TRANSISTOR LIQUID CRYSTAL DISPLAY PANEL AND METHOD OF FABRICATING THE SAME**

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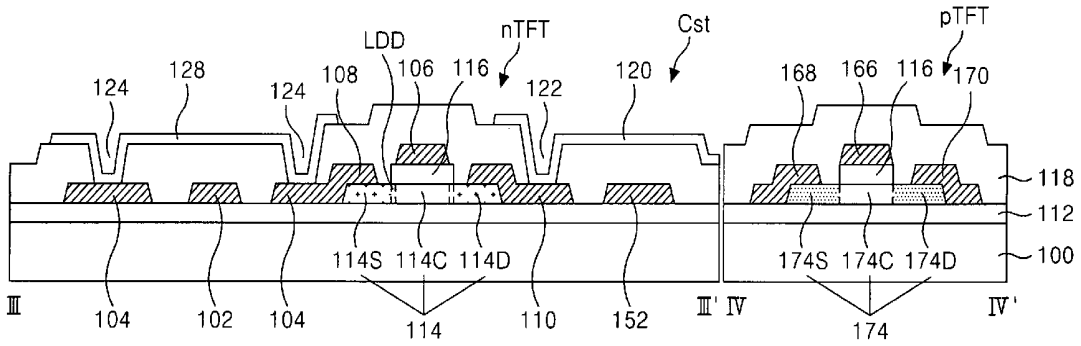
(57) **ABSTRACT**

A thin film transistor (TFT) liquid crystal display panel and fabrication method are described. The panel has a data line and a gate line connected with a TFT and formed on the same layer. One of data or gate lines is discontinuous and the other is continuous in a pixel region such that the continuous line bisects the discontinuous line. A passivation film protects the TFT. Contact holes penetrate the passivation film and expose segments of the discontinuous line. A contact electrode connects the segments through the contact holes.



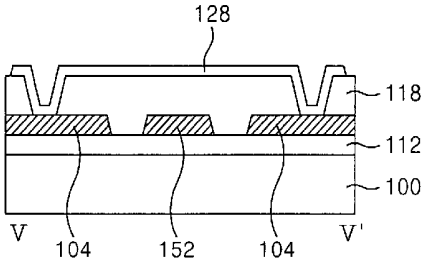



FIG. 1
RELATED ART

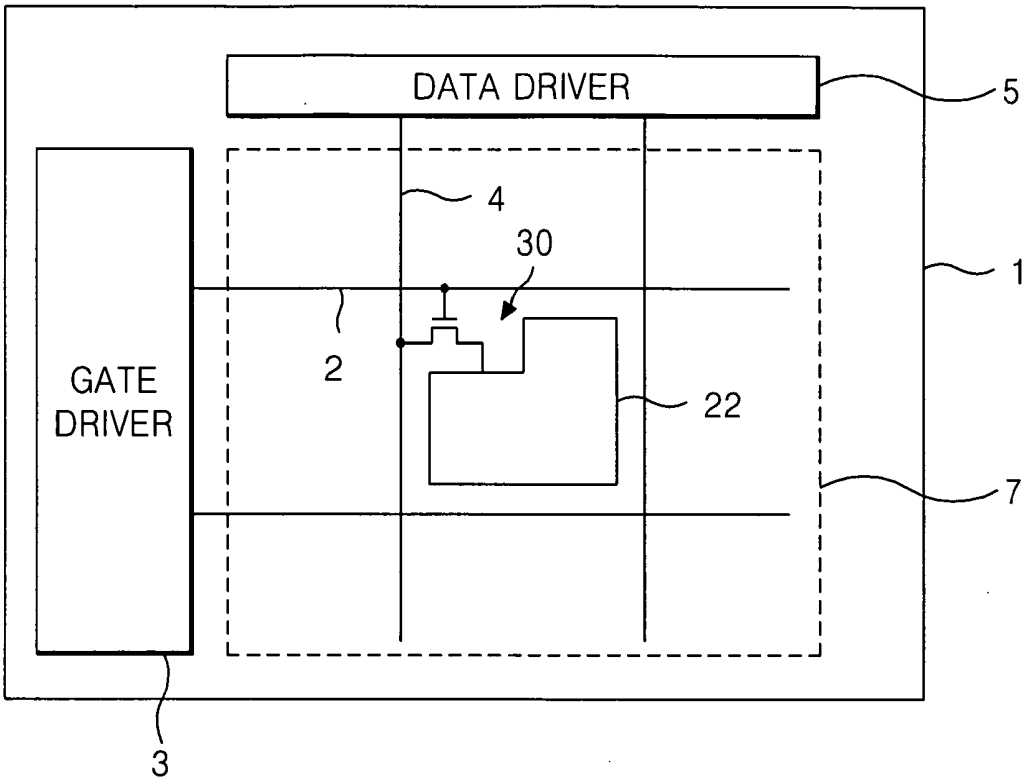


FIG. 2
RELATED ART

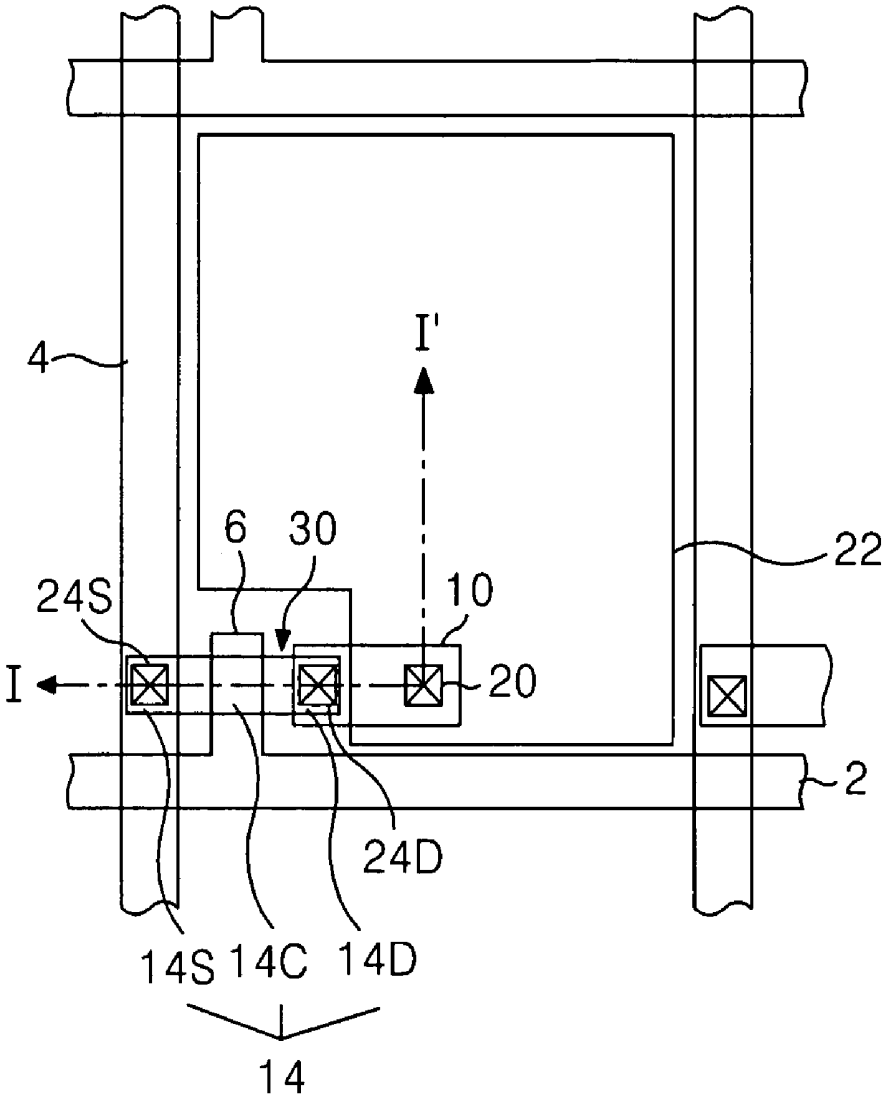


FIG.3
RELATED ART

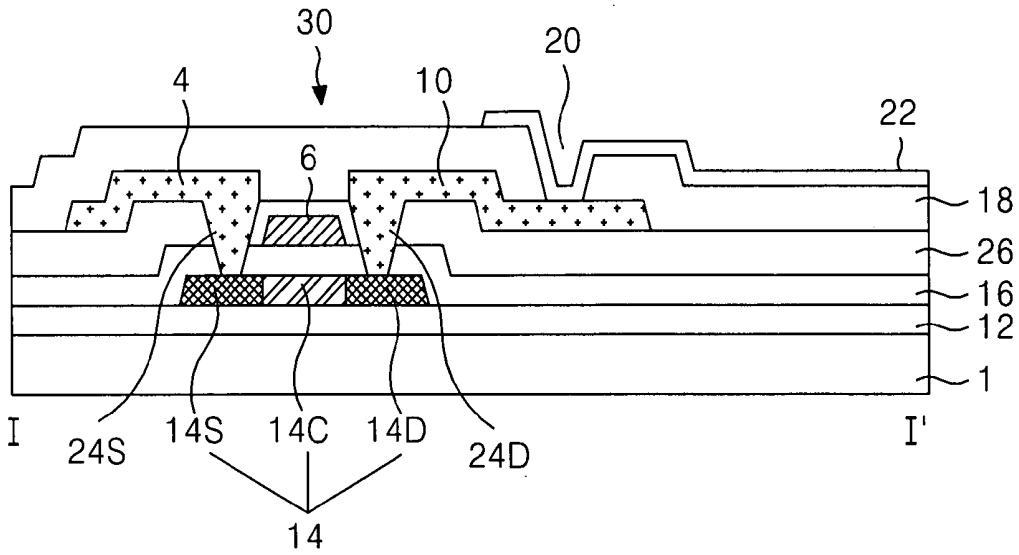


FIG. 4

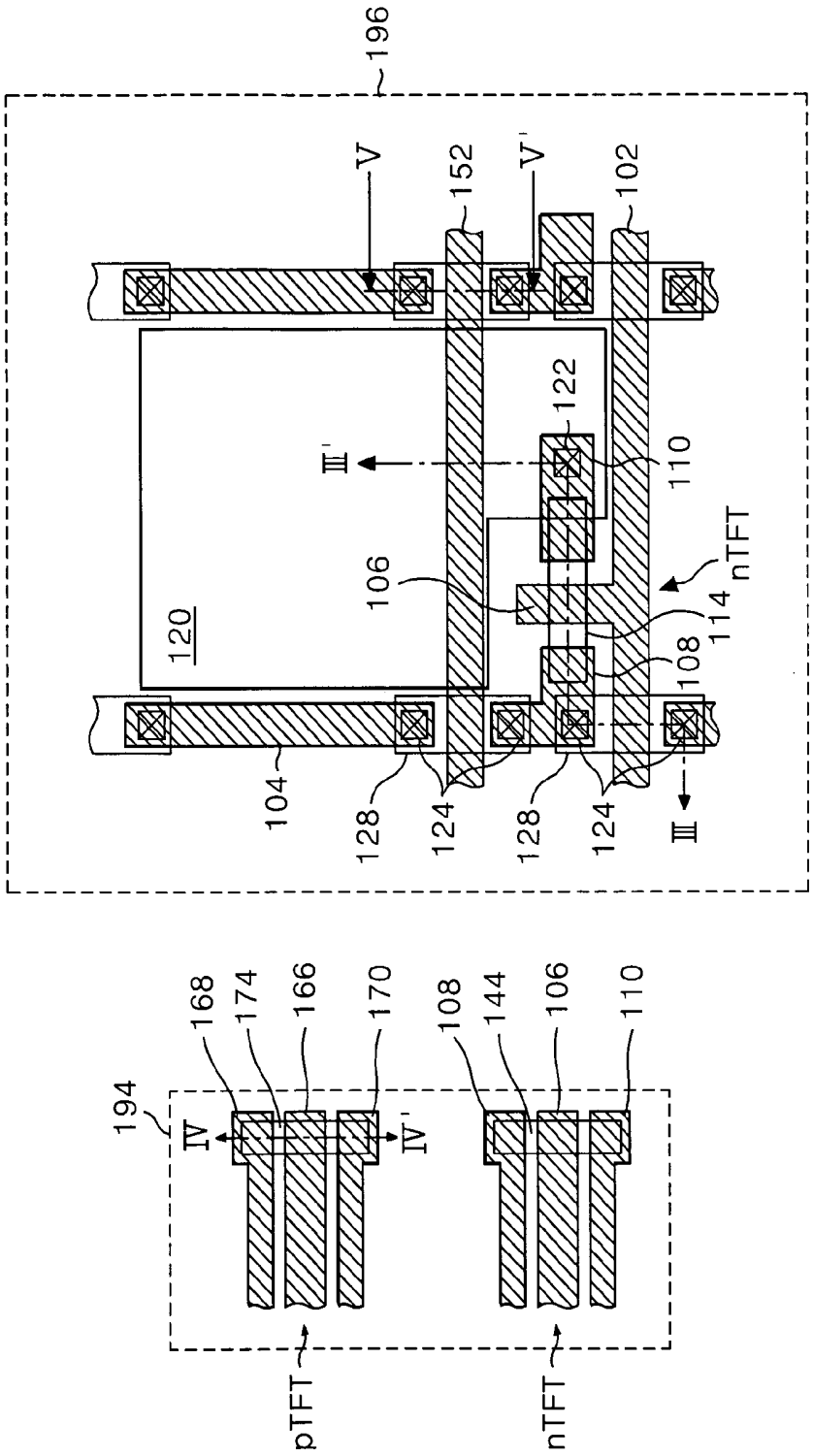

196
V
V'
152
102
122
110
III'
106
nTFT
114
108
120
104
128
124
128
124
III
194
168
174
166
170
108
144
106
110
IV
IV'
pTFT
nTFT

FIG. 5

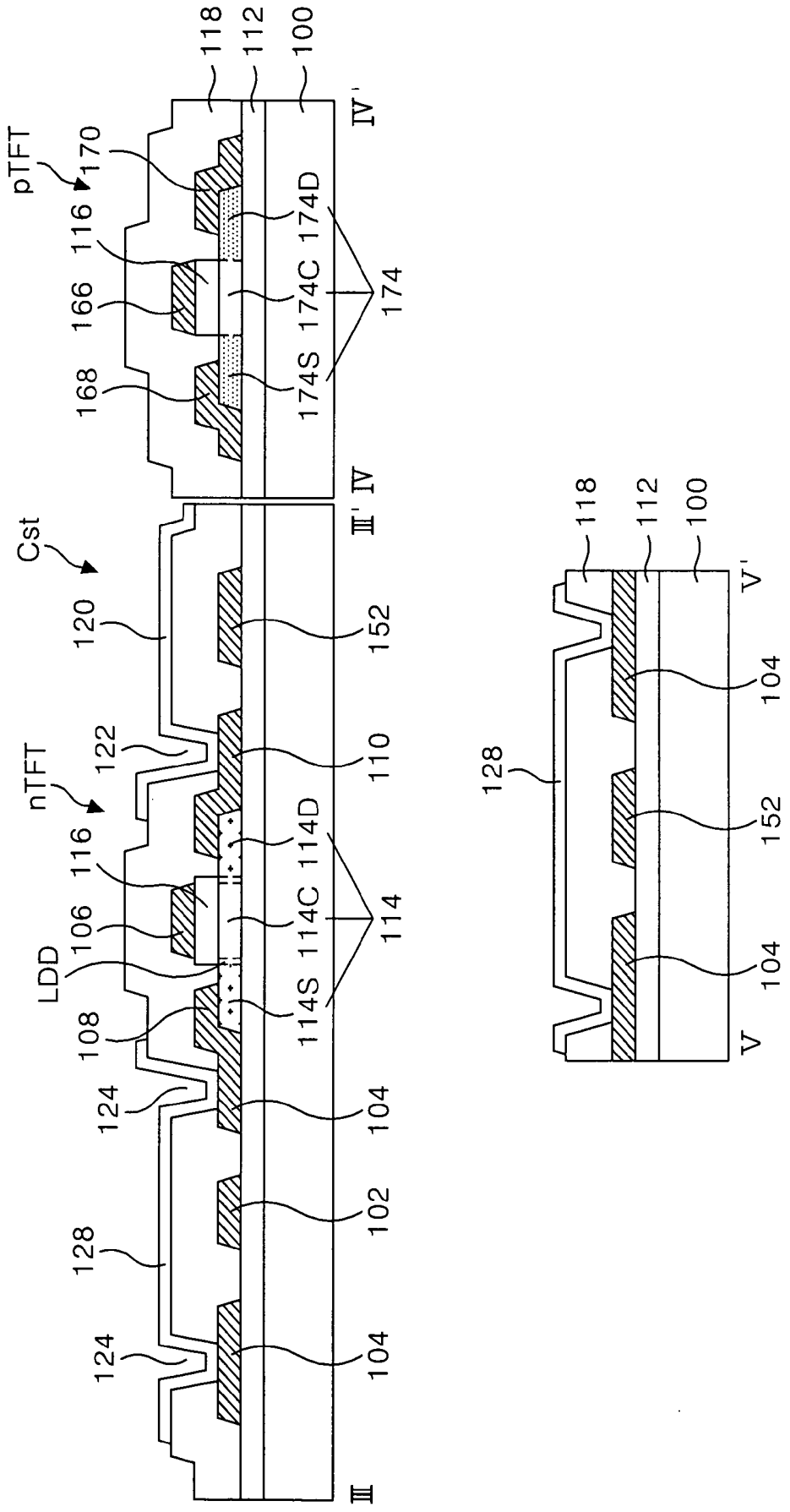

118
112
100
IV'
pTFT
170
116
166
168
174D
174C
174S
174
III' IV
Cst
120
152
122
110
nTFT
116
106
LDD
108
114D
114C
114S
114
124
104
128
102
124
104
III
V'
118
112
100
104
128
152
104
V

FIG.6A

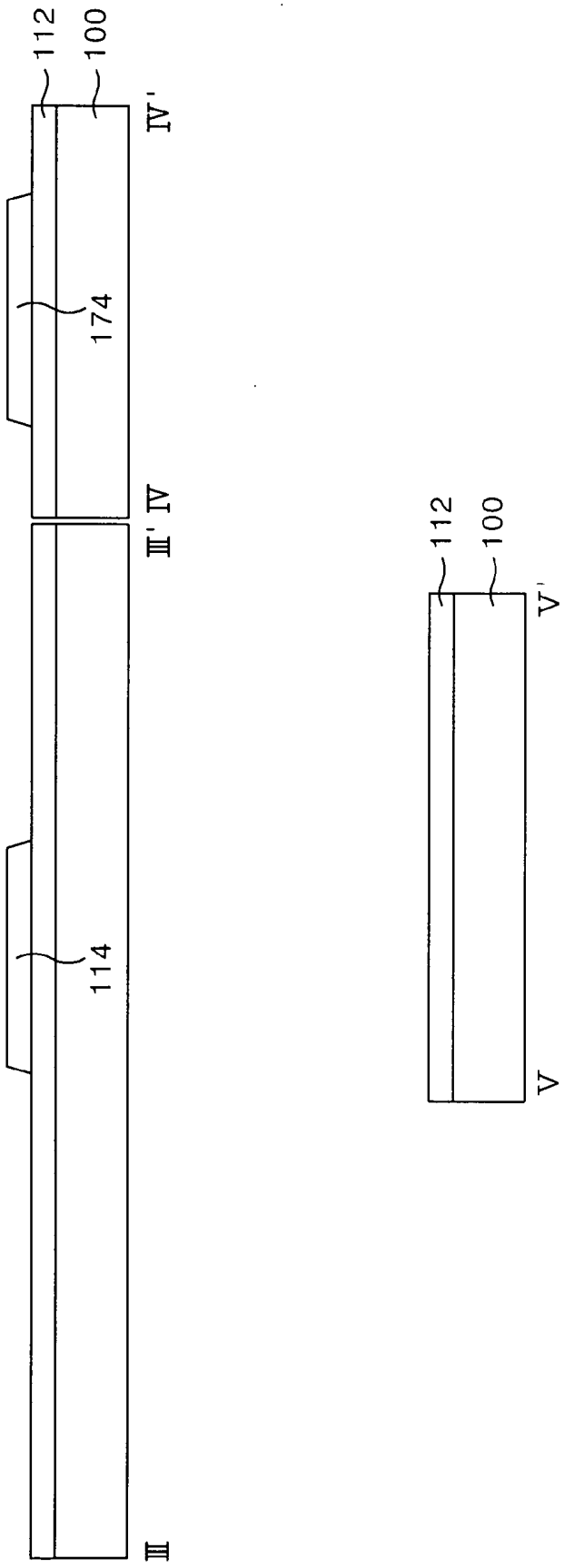


FIG.6B

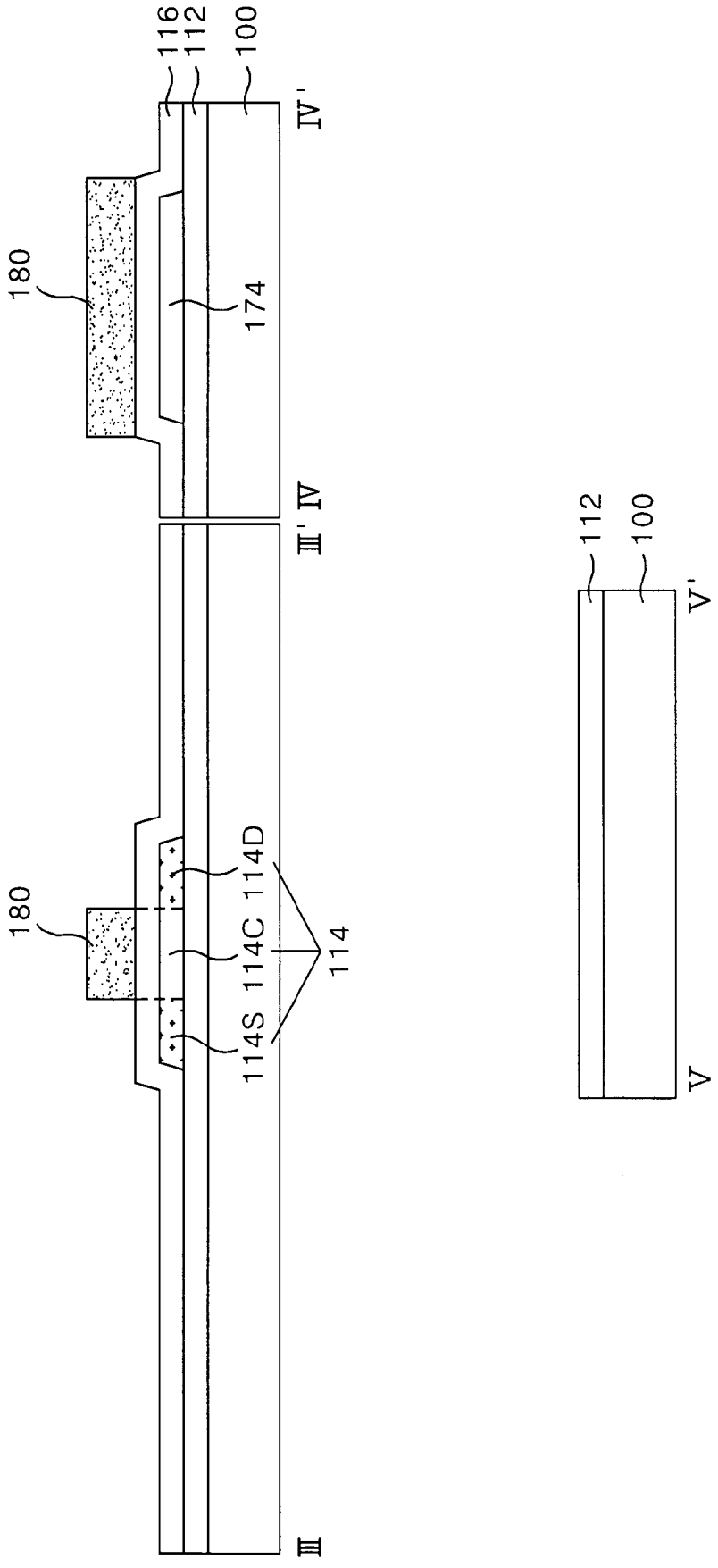

116
112
100
IV'
180
174
III' IV
180
114D
114C
114S
114
III
112
100
V'
V

FIG. 6C

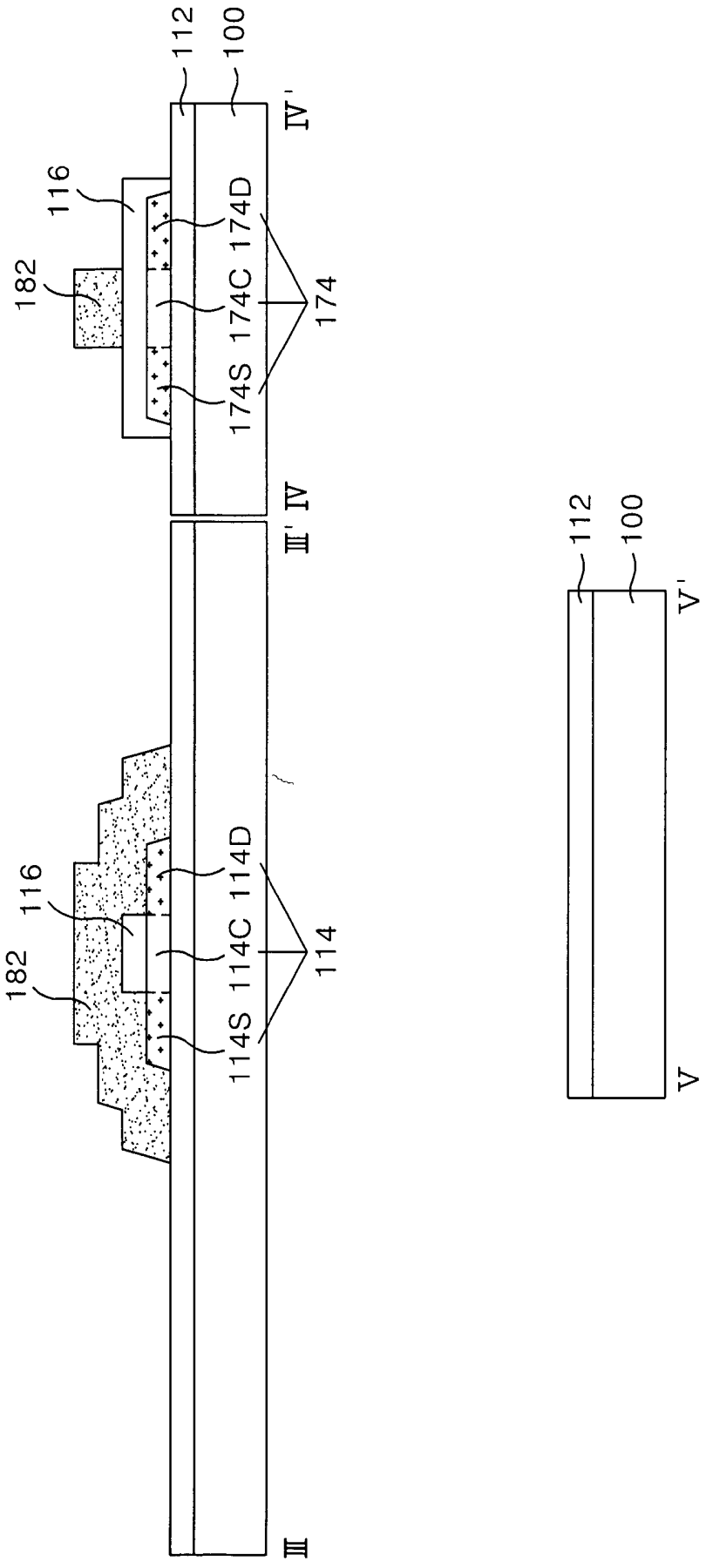

112
100
IV'
116
182
174D
174C
174S
174
III' IV
V'
V
114D
114C
114S
114
III

FIG.6D

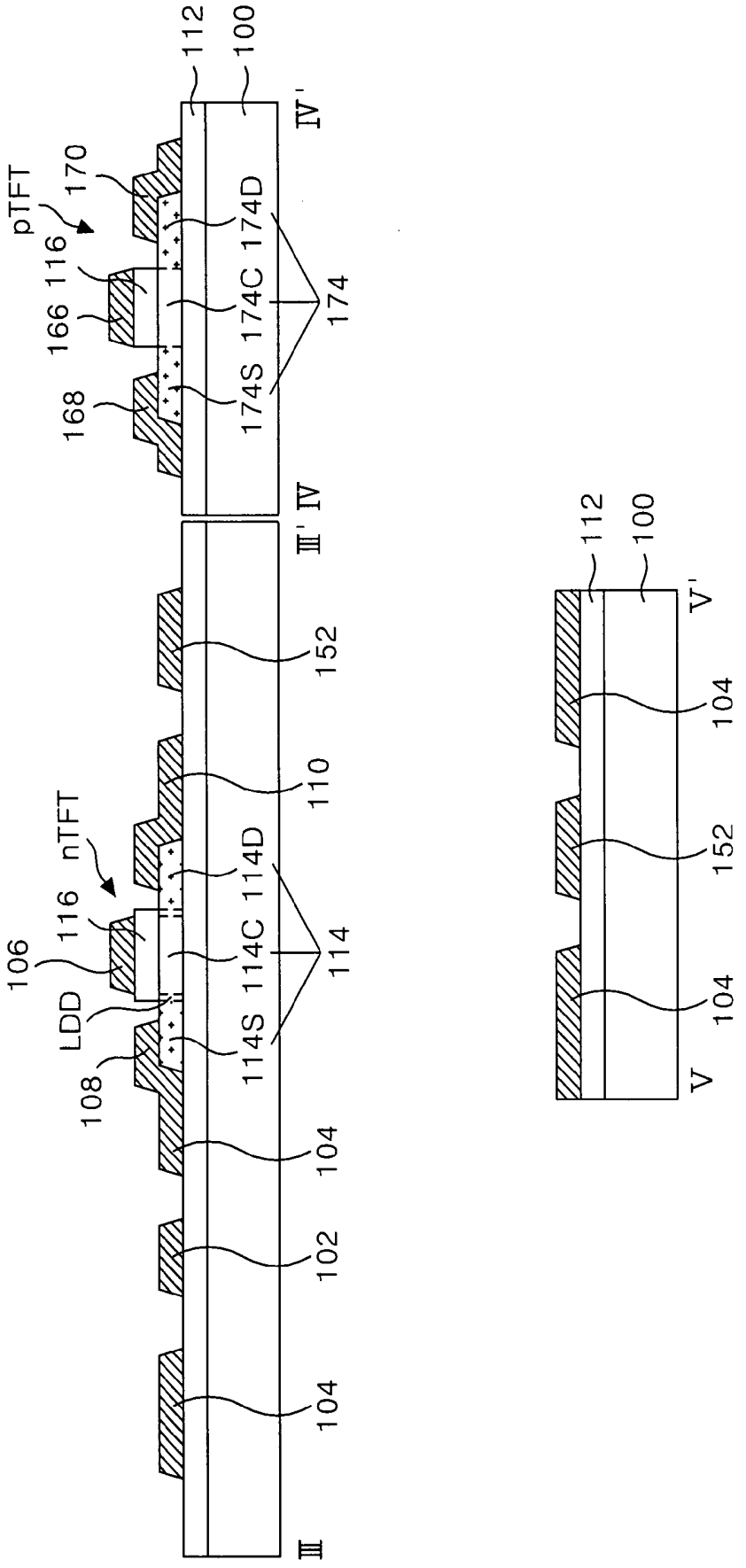

112
100
IV'
pTFT
170
116
166
168
174D
174C
174S
174
III' IV
152
110
nTFT
106
116
LDD
108
114D
114C
114S
114
104
102
104
III
V'
112
100
104
152
104
V

FIG.6E

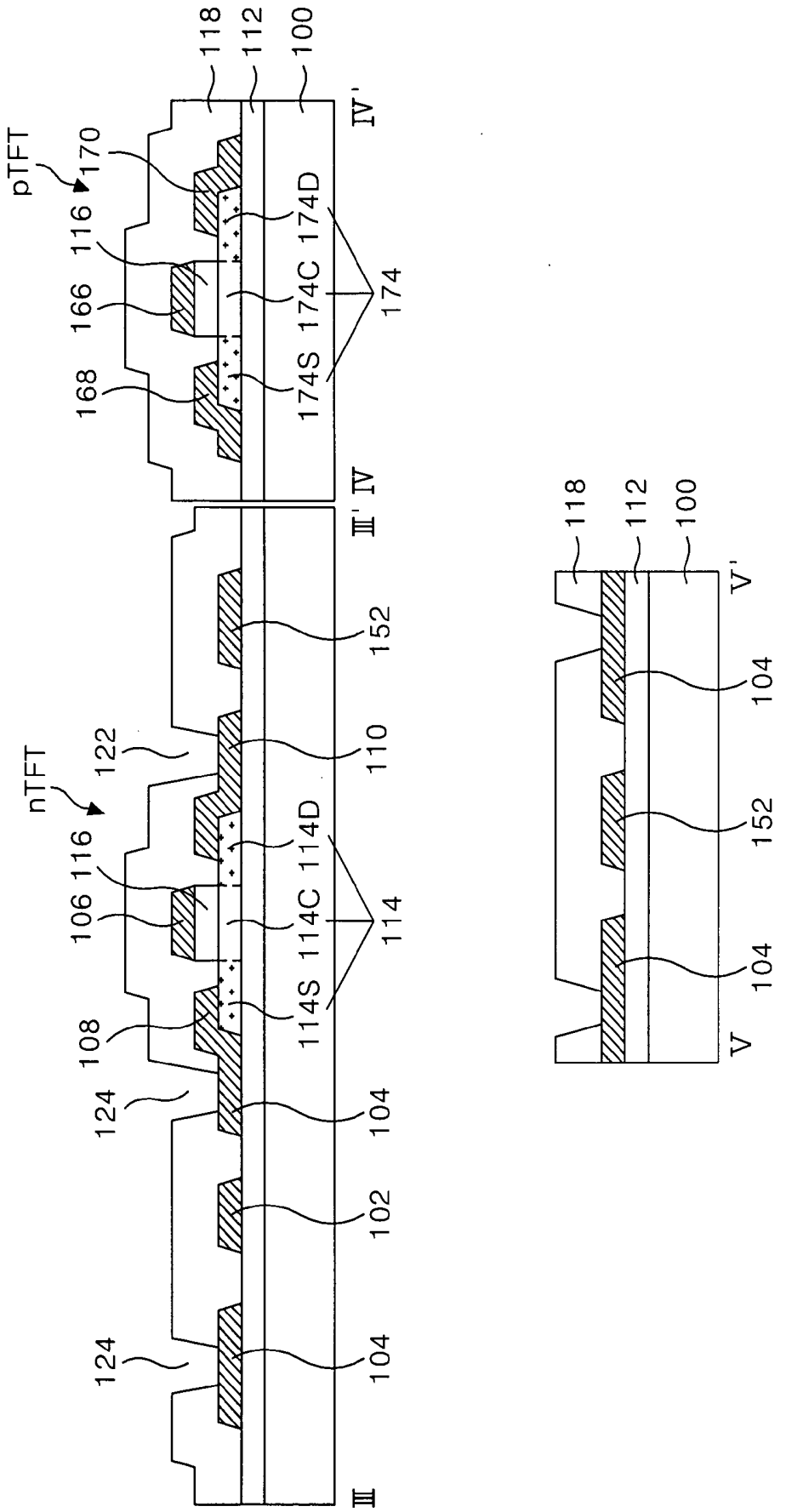
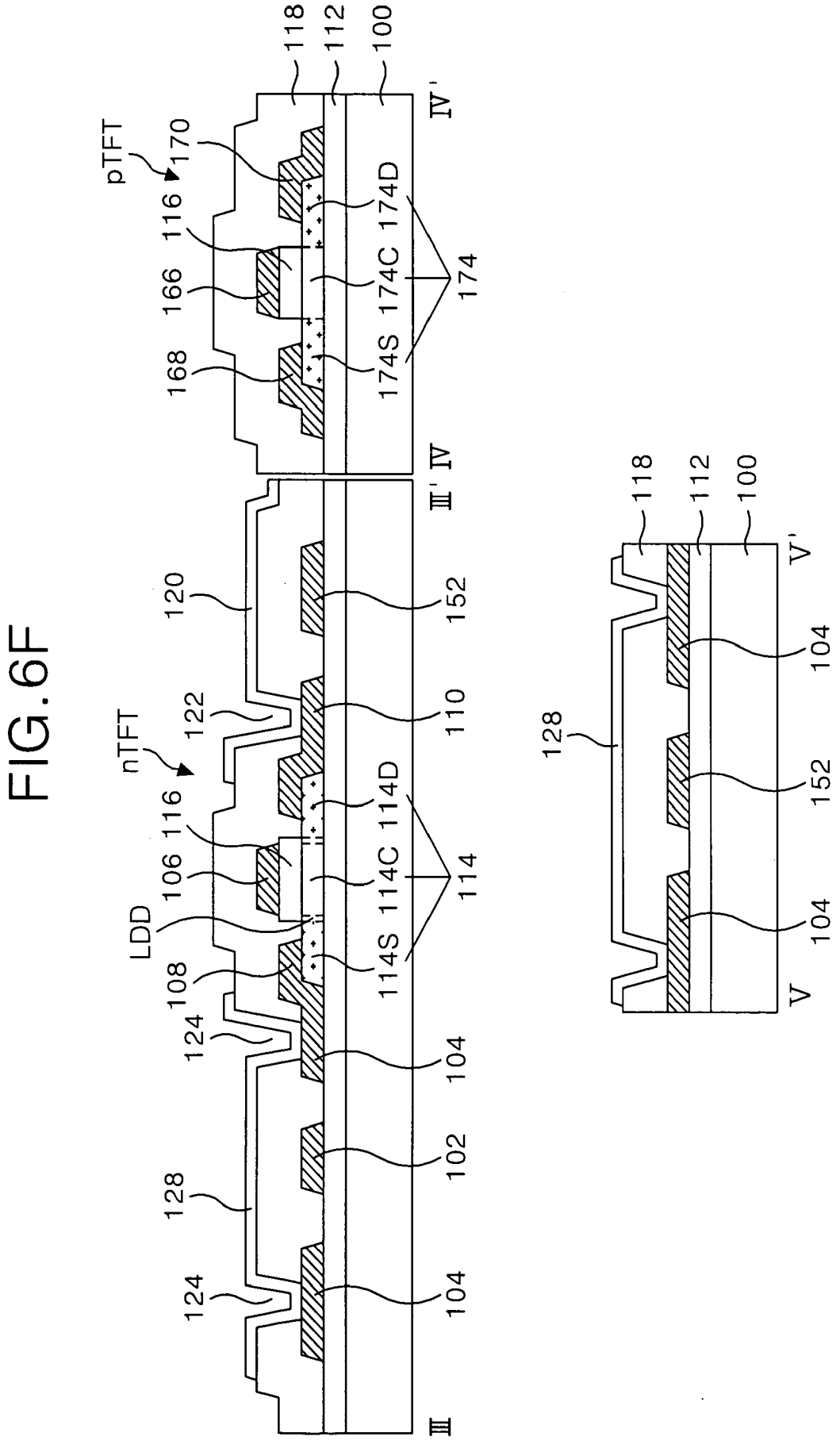

118
112
100
IV'
pTFT
170
116
166
168
174D
174C
174S
174
III' IV
152
122
110
nTFT
106
108
114D
114C
114S
114
124
104
102
III
V'
V

FIG. 6F


118
112
100
IV'
pTFT
170
116
166
168
174D
174C
174S
174
III' IV
120
152
122
110
nTFT
116
106
LDD
108
114D
114C
114S
114
124
104
128
102
124
104
III
118
112
100
V'
104
128
152
104
V

# THIN FILM TRANSISTOR LIQUID CRYSTAL DISPLAY PANEL AND METHOD OF FABRICATING THE SAME

[0001] This application claims the benefit of the Korean Patent Application No. P2005-58635 filed on Jun. 30, 2005, which is hereby incorporated by reference.

## TECHNICAL FIELD

[0002] The present embodiments are directed to a liquid crystal display panel using a poly silicon thin film transistor, and more particularly to a poly silicon thin film transistor liquid crystal display panel that is adaptive for simplifying a process, and a fabricating method thereof.

## BACKGROUND

[0003] Generally, a liquid crystal display LCD device has liquid crystal cells, which are arranged in a liquid crystal display panel in a matrix shape. The liquid crystal cells control light transmittance in accordance with a video signal, thereby displaying a picture.

[0004] A thin film transistor (hereinafter, referred to as 'TFT') is used as a switching device for independently supplying a video signal in each of the liquid crystal cells. Amorphous silicon or poly silicon is used for a semiconductor layer of such a TFT. When using poly silicon, which has a charge mobility 100 times faster than amorphous silicon, a drive circuit with a high response speed can be embedded in the liquid crystal display panel.

[0005] FIG. **1** briefly illustrates a TFT substrate of a related art poly liquid crystal display panel where a drive circuit is embedded.

[0006] A poly silicon TFT substrate shown in FIG. **1** includes a picture display area **7** where a TFT **30** and a pixel electrode **22** are formed at each pixel area defined by the crossing of a gate line **2** and the data line **4**; a data driver **5** for driving the data line **4** of the picture display area **7**; and a gate driver **3** for driving the gate line **2** of the picture display area **7**.

[0007] The picture display area **7** includes the TFT **30** and the pixel electrode **22** which are formed at each pixel area that is defined by the cross of a plurality of gate lines **2** and a plurality of data lines **4**. The TFT **30** charges a video signal from the data line **4** in the pixel electrode **22** in response to a scan signal of the gate line **2**. The pixel electrode **22** charged with the video signal generates a potential difference with a common electrode of a color filter substrate which faces a TFT substrate with liquid crystal therebetween, thereby making liquid crystal molecules rotate by dielectric anisotropy in accordance with the potential difference. The light transmittance is changed in accordance with the degree of rotation of the liquid crystal molecules, thereby realizing a gray level.

[0008] The gate driver **3** sequentially drives the gate line **2**.

[0009] The data driver **5** supplies a video signal to the data line **4** whenever the gate line **2** is driven.

[0010] FIG. **2** is a plane view illustrating an enlarged pixel area included in a picture display area **7** of the poly silicon TFT substrate shown in FIG. **1**, and FIG. **3** is a sectional diagram illustrating a pixel area of the TFT substrate shown in FIG. **2**, taken along the line I-I'.

[0011] The TFT substrate shown in FIGS. **2** and **3** includes a TFT **30** connected to the gate line **2** and the data line **4**, and a pixel electrode **22** connected to the TFT **30**. The TFT **30** is an NMOS TFT or a PMOS TFT, but only the NMOS TFT is explained below.

[0012] The TFT **30** includes a gate electrode **6** connected to the gate line **2**; a source electrode included in the data line **4**; and a drain electrode **10** connected to the pixel electrode **22** through a pixel contact hole **20** that penetrates a passivation film. The gate electrode **6** is formed to overlap a channel area **14**C of a semiconductor layer **14** which is formed on a buffer film **12** with a gate insulating film **16** therebetween. The source electrode and the drain electrode **10** are formed on an interlayer insulating film **26**. The interlayer insulating film **26** is also between the gate electrode **6** and the source and drain electrodes. The source electrode and the drain electrode **10** are respectively connected to a source area **14**S and a drain area **14**D of the semiconductor layer **14** into which n+ impurities are injected through a source contact hole **24**S and a drain contact hole **24**D which penetrates the interlayer insulating film **26** and the gate insulating film **16**.

[0013] The picture display area **7** of the poly silicon TFT substrate is formed by six mask processes as below.

[0014] Specifically, in a first mask process, a buffer film **12** is formed on a lower substrate **1** and the semiconductor layer **14** is formed thereon. The semiconductor layer **14** is formed by patterning a poly silicon layer with a photolithography process and an etching process using a first mask after depositing amorphous silicon on the buffer film **12** and crystallizing the deposited amorphous silicon with a laser to form the poly silicon.

[0015] In a second mask process, the gate insulating film **16** is formed on the buffer film **12** where the semiconductor layer **14** is formed, and the gate line **2** and the gate electrode **6** are formed thereon. The gate electrode **6** is used as a mask to inject n+ impurities into a non-overlapping area of the semiconductor layer **14**, thereby forming the source area **14**S and the drain area **14**D of the semiconductor layer **14**.

[0016] In a third mask process, the interlayer insulating film **26** is formed on the gate insulating film **16** where the gate line **2** and the gate electrode **6** are formed, and the source contact hole **24**S and the drain contact hole **24**D are formed to penetrate the interlayer insulating film **26** and the gate insulating film **16**.

[0017] In a fourth mask process, the drain electrode **10** and the data line **4** including the source electrode are formed on the interlayer insulating film **26**.

[0018] In a fifth mask process, the passivation film **18** is formed on the interlayer insulating film **26** where the data line **4** and the drain electrode **10** are formed, and a pixel contact hole **20** is formed to penetrate the passivation film **18** to expose the drain electrode **10**.

[0019] In a sixth mask process, a transparent pixel electrode **22** connected to the drain electrode **10** through the pixel contact hole **20** is formed on the passivation film **18**.

[0020] In this way, the picture display area **7** of the related art poly silicon TFT substrate is formed by the six mask

processes. However, the fabricating process is complicated because each mask process includes a number of processes, for example: a thin film deposition process, a cleaning process, a photolithography process, an etching process, a photo resist peeling process, an inspection process and so on.

[0021] Further, the related art poly silicon TFT substrate is used to form a CMOS TFT if a storage capacitor is formed in the picture display area **7** and the gate driver **3** and data driver **5** are formed. This increases the number of processes to nine mask processes, which further complicates the fabricating process. Accordingly, a method that reduces the number of mask processes of the poly silicon TFT substrate is desirable, at least for reasons of cost among others.

## BRIEF SUMMARY

[0022] By way of introduction only, a TFT LCD panel according to an aspect of the present invention comprises a first signal line; a second signal line separated by the first signal line; a first thin film transistor having a first semiconductor layer doped with a first impurity, a first gate electrode overlapping the first semiconductor layer with a first insulating pattern therebetween, a first source electrode and a first drain electrode separated from the first gate electrode and connected with the first semiconductor layer; a passivation film protecting the first thin film transistor; a first contact hole exposing the first drain electrode by penetrating the passivation film; a pixel electrode connected with the first drain electrode through the first contact hole; a plurality of second contact holes penetrating the passivation film such that ends of a separated part of the second signal line are exposed; and a first contact electrode connecting the separated parts of the second signal line through the second contact holes.

[0023] A TFT LCD panel according to another aspect of the present invention comprises gate, data, and storage lines disposed on the same layer in a display area of the liquid crystal display panel, at least one of the gate, data, or storage lines being discontinuous in the pixel region and at least one of the gate, data, or storage lines being continuous in the pixel region, the continuous line bisecting segments of the discontinuous line in the display area; a thin film transistor having a semiconductor layer, a gate electrode overlapping the semiconductor layer with an insulating pattern therebetween, and source and drain electrodes separated from the gate electrode and connected with the semiconductor layer; a passivation layer on the thin film transistor and the gate, data, and storage lines; and a contact electrode connecting the segments of the discontinuous line through second contact holes in the passivation layer.

[0024] A method of fabricating a TFT LCD panel according to an aspect of the present invention comprises forming a first semiconductor layer on a substrate; doping the first semiconductor layer with a first impurity to form a source area and a drain area of the first semiconductor layer; forming a first insulating pattern overlapping a channel area between the source and drain areas; forming a first conductive pattern group on the substrate, wherein the first conductive pattern group has a gate line, a first gate electrode connected with the gate line and overlapping the first insulating pattern, a first source electrode and a first drain electrode connected with the source and drain areas of the first semiconductor layer, respectively, and a data line connected with the first source electrode, at least one of the gate or data lines being discontinuous; forming a passivation film on the substrate where the first conductive pattern group is formed, a first contact hole that exposes the first drain electrode, and a second contact hole that exposes a part of the discontinuous line; and forming a pixel electrode connected with the first drain electrode through the first contact hole, and a first contact electrode that connects the discontinuous line through the second contact hole.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The following detailed description of the embodiments of the present invention reference the accompanying drawings, in which:

[0026] FIG. **1** is a block diagram briefly illustrating a related art poly silicon TFT substrate;

[0027] FIG. **2** is a plane view illustrating an enlarged pixel area of FIG. **1**;

[0028] FIG. **3** is a sectional diagram illustrating a pixel area shown in FIG. **2**, taken along the line I-I';

[0029] FIG. **4** is a plane view partially illustrating a poly silicon TFT substrate according to an embodiment of the present invention;

[0030] FIG. **5** is a sectional diagram illustrating the poly silicon TFT substrate shown in FIG. **4**, taken along the lines III-III' and IV-IV'; and

[0031] FIGS. **6**A to **6**F are sectional diagrams of a fabricating method of a poly silicon TFT substrate according to an embodiment.

## DETAILED DESCRIPTION

[0032] Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0033] With reference to FIGS. **4** to **6**F, embodiments of the present invention will be explained as follows.

[0034] FIG. **4** is a plane view illustrating part of a poly silicon TFT substrate according to an embodiment of the present invention, and FIG. **5** is a sectional diagram illustrating the TFT substrate shown in FIG. **4**, taken along the lines III-III' and IV-IV'.

[0035] A polysilicon TFT substrate shown in FIGS. **4** and **5** includes a picture display area **196** and a driver area **194** where a drive circuit is formed to drive a gate line **102** and a data line **104** of the picture display area **196**.

[0036] The picture display area **196** includes an nTFT (n-channel TFT) connected to the gate line **102** and the data line **104**, a pixel electrode **120** connected to the nTFT and a storage capacitor Cst. The driver area **194** includes a pTFT (p-channel TFT) and the nTFT which are connected in a CMOS structure.

[0037] The nTFT supplies a video signal of the data line **104** to the pixel electrode **120** in response to a gate signal of the gate line **102**. For this, the nTFT includes a first gate electrode **106** connected to the gate line **102**; a first source electrode **108** connected to the data line **104**; a first drain electrode **110** connected to the pixel electrode **120**; and a

first semiconductor layer **114** which forms a channel between the first source electrode **108** and the first drain electrode **110**. The first source electrode **108** and the first drain electrode **110** are respectively connected to a source area **114**S and a drain area **114**D of the first semiconductor layer **114**. And, the nTFT further includes a channel area **114**C for reducing an off-current and an LDD (lightly doped drain) area where n− impurities are injected between the source area **114**S and the drain area **114**D.

[**0038**] The pTFT includes a second semiconductor layer **174** formed on a buffer film **112**; a second gate electrode **166** which overlaps a channel area **174**C of a second semiconductor layer **174** with a gate insulating film **116** therebetween; and a second source electrode **168** and a second drain electrode **170** which are respectively connected to a source area **174**S and a drain area **174**D of the second semiconductor layer **174**. Herein, the source area **174**S and the drain area **174**D of the second semiconductor layer **174** are formed by having p impurities injected.

[**0039**] The pixel electrode **120** is connected to the first drain electrode **110** of the pixel display area **196** through a first contact hole **122** that penetrates a passivation film **118**. The pixel electrode **120** is charged with the video signal supplied from the nTFT and generates a potential difference with a common electrode which is formed in a color filter substrate (not shown). The potential difference causes a liquid crystal located in the color filter substrate and the TFT substrate to rotate by dielectric anisotropy. This causes the transmittance of the light that is incident through the pixel electrode **120** from a light source (not shown) to be controlled to transmit the light to the color filter substrate.

[**0040**] The storage capacitor Cst is formed by having the storage line **152** overlap the pixel electrode **120** with the passivation film **118** therebetween. The storage capacitor Cst stabilizes the video signal charged in the pixel electrode **120**.

[**0041**] The data line **104** is formed along with the gate line **102** and the storage line **152**. Hereby, the data line **104** is formed so as not to be short-circuited with the gate line **102** and the storage line **152**. For example, the data line **104**, as shown in FIG. **4**, is separated from the gate line **102** and the storage line **152** so as not to be short-circuited. The separated data line **104** is connected through a contact electrode **128** which is formed on the passivation film **118**.

[**0042**] Specifically, the contact electrode **128** is formed to be insulated from and to cross the gate line **102** or the storage line **152**, and is connected to both ends of separated the data line **104** through the contact hole **124** exposing both ends of the separated data line **104**. Accordingly, the data line **104** is discontinuous, that is, the data line **104** separated by the gate line **102** and/or the storage line **152**. The portions of the data line **104** are connected through the contact electrode **128**.

[**0043**] In other embodiments, the data line **104** maybe continuous and the gate line **102** and/or the storage line **152** discontinuous, that is, separated by the data line **104**. In this case, the separated gate line **102** or the storage line **152** is connected through the contact hole **124** penetrating the passivation film **118** as above and the contact electrode **128** crossing the data line **104**.

[**0044**] A fabricating method of a poly silicon TFT substrate of the present invention with such a configuration is specifically explained as follows.

[**0045**] FIGS. **6**A to **6**F sectional diagrams of a fabricating method of a poly silicon TFT substrate according to an embodiment of the present invention.

[**0046**] Referring to FIG. **6**A, the buffer film **112** is formed on the lower substrate **100**, and the first and second semiconductors **114**, **174** which are integrated by a first mask process are formed thereon.

[**0047**] Specifically, the buffer film **112** is formed by depositing an inorganic insulating material such as $SiO_2$ on the entire surface of the lower substrate **100**. The first and second semiconductors **114**, **174** are formed by forming an amorphous silicon thin film on the buffer film **112**, crystallizing the amorphous silicon thin film into a poly silicon thin film, and then patterning the poly silicon thin film by a photolithography process and an etching process using a first mask. A dehydrogenation process may then be performed for eliminating hydrogen atoms which exist within the amorphous silicon thin film before crystallizing the amorphous silicon thin film. One method of crystallizing the amorphous silicon thin film is a sequential lateral crystallization SLS method. In the SLS method, a laser beam is scanned in a horizontal direction, which causes the crystal grain to grow in the horizontal direction, thereby increasing the size of grain. The laser beam may be an excimer laser. This is only one of the methods of annealing using a laser.

[**0048**] Referring to FIG. **6**B, the gate insulating film **116** is formed on the buffer film **112** where the first and second semiconductor films **114**, **174** are formed. The source and drain areas **114**S, **114**D of the first semiconductor layer **114** are doped with n+ impurities. The gate insulating film **116** is then patterned by a second mask process.

[**0049**] Specifically, in one embodiment, the gate insulating film **116** is formed by depositing an inorganic insulating material such as $SiO_2$ on the entire surface of the buffer film **112** where the first and second semiconductor films **114**, **174** are formed.

[**0050**] For n+ doping, a first photo resist pattern **180** that covers or intercepts the second semiconductor layer **174** and the channel area **114**C of the first semiconductor layer **114** is formed by the photolithography process using the second mask. Subsequently, n+ doping is performed only in the drain area **114**D and the source area **114**S of the first semiconductor layer **114** having the first photo resist pattern **180** as a mask.

[**0051**] The gate insulating film **116** is then patterned by the etching process using the first photo resist pattern **180** as a mask. Accordingly, the gate insulating film **116** remains only at an overlapping part of the second semiconductor layer **174** and the channel area **114**C of the first semiconductor layer **114** as shown in FIG. **6**C. The first photo resist pattern **180** is then removed by a stripping process.

[**0052**] Referring to FIG. **6**C, by a third mask process, p+ doping is performed in the source area **174**S and the drain area **174**D of the second semiconductor layer **174**. The gate insulating film **116** is subsequently etched.

[**0053**] Specifically, in one embodiment, for p+ doping, a second photo resist pattern **182** that covers or intercepts the channel area **174**C of the second semiconductor layer **174** and the first semiconductor layer **114** is formed by the photolithography process using the third mask. Subsequently, p+ doping is performed only in the drain area **174**D and the source area **174**S of the second semiconductor layer **174** having the second photo resist pattern **182** as a mask.

[**0054**] The gate insulating film **116** which overlaps the source and drain areas **174**S, **174**D of the second semiconductor is then removed by the etching process using the

second photo resist pattern **182** as a mask. As a result, the gate insulating film **116** remains only in the channel areas **114**C, **174**C of the first and second semiconductor layers **114**, **174** as shown in FIG. **6**D.

[**0055**] Referring to FIG. **6**D, a first conductive pattern group is formed by a fourth mask process. The first conductive pattern group includes the gate line **102**, the gate electrode **106**, **166**, the data line **104**, the storage line **152**, the source electrode **108**, **168** and the drain electrode **110**, **170**.

[**0056**] Specifically, a first conductive layer is formed on a buffer film **112** where the gate insulating film **116** remains, and then the first conductive layer is patterned by the photolithography process and the etching process using the fourth mask, thereby forming the first conductive pattern group. The first conductive layer includes a metal layer that a metal material such as Mo, Ti, Cu, AlNd, Al, Cr, Mo alloy, Cu alloy, Al alloy and so on is deposited in a single layer or in a multiple layer. The source electrode **108**, **168** and the drain electrode **110**, **170** are separated so as not to be short-circuited, and the data line **104** is separated by the gate line **102** and/or the storage line **152**. In other embodiments, the gate line **102** and/or the storage line **152** may be formed to be separated by the data line **104**.

[**0057**] Subsequently, n− doping is performed through both sides of a gate insulating film **116** which is exposed at side of the gate electrode **106**, thereby forming the LDD area. The LDD area does not overlap the first gate electrode **106** in the channel area **114**C of the first semiconductor layer **114**.

[**0058**] Referring to FIG. **6**E, the passivation film **118** is formed on the buffer film **112** where the first conductive pattern group is formed. The first and second contact holes **122**, **124**, which penetrate the passivation film **118**, are formed by a fifth mask process.

[**0059**] Specifically, the passivation film **118** is formed by depositing an organic insulating material or an inorganic insulating material such as $SiO_2$ and SiNx on the entire surface of the buffer film **112** where the first conductive pattern group is formed. Subsequently, the passivation film **118** is patterned by the photolithography process and the etching process using the fifth mask, thereby forming a plurality of contact holes **122**, **124**.

[**0060**] Referring to FIG. **6**F, a second conductive pattern group is formed by a sixth mask process. The second conductive pattern group includes the pixel electrode **120** and the contact electrode **128** on the passivation film.

[**0061**] Specifically, a transparent conductive layer is formed on the passivation film **118**, and then is patterned by the photolithography process and the etching process using the sixth mask, thereby forming the second conductive pattern group. The transparent conductive layer may comprise ITO (indium tin oxide), TO (tin oxide), IZO (indium zinc oxide), and/or ITZO, for example. The pixel electrode **120** is connected to the first drain electrode **110** through a first contact hole **122**, and the contact electrode **124** is connected to the separated data line **104** through a second contact hole **124** to connect the separated data line **104**. In other embodiments, if the gate line **102** or the storage line **152** is separated, the contact electrode **124** is connected to the separated gate line **102** or storage line **152** through the second contact hole **124** to connect the separated gate line **102** or to connect the separated storage line **152**, respectively.

[**0062**] In this way, the poly silicon TFT substrate fabrication method forms the gate line **102**, the data line **104**, the storage line **152**, the gate electrode **106**, **166**, the source electrode **108**, **168** and the drain electrode **110**, **170** by the same mask process, thus it is possible to reduce the number of mask processes. Further, the poly silicon TFT substrate fabrication method forms the storage capacitor Cst by overlapping of the pixel electrode **120** and the storage line **152**. It is thus possible to reduce the number of the mask processes more than when the storage capacitor is formed by overlapping of the storage line and the semiconductor layer.

[**0063**] As described above, the poly silicon TFT substrate and the fabricating method thereof forms the data line and the source and drain electrodes along with the gate line and the storage line by the same mask process. The separated data line, gate line and/or storage line is connected to the contact electrode which is formed along with the pixel electrode. Further, the poly silicon TFT substrate and the fabricating method thereof forms the storage capacitor by overlapping of the pixel electrode and the storage line.

[**0064**] As a result, the poly silicon TFT substrate and the fabricating method thereof can reduce the number of processes to six mask processes. Accordingly, the material cost and equipment investment cost can be reduced and the yield can be improved.

[**0065**] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

**1**. A thin film transistor liquid crystal display panel, comprising:

a first signal line;

a second signal line separated by the first signal line;

a first thin film transistor having a first semiconductor layer doped with a first impurity, a first gate electrode overlapping the first semiconductor layer with a first insulating pattern therebetween, a first source electrode and a first drain electrode separated from the first gate electrode and connected with the first semiconductor layer;

a passivation film protecting the first thin film transistor;

a first contact hole penetrating the passivation film and exposing the first drain electrode;

a pixel electrode connected with the first drain electrode through the first contact hole;

a plurality of second contact holes penetrating the passivation film such that parts of the second signal line separated by the first signal line are exposed; and

a first contact electrode connecting the parts of the second signal line separated by the first signal line through the second contact holes.

**2**. The thin film transistor liquid crystal display panel according to claim 1, wherein the first signal line comprises a gate line connected with the first gate electrode, and the

second signal line comprises a data line separated by the gate line and connected with the first source electrode.

**3**. The thin film transistor liquid crystal display panel according to claim 1, wherein the first signal line comprises a data line connected with the first source electrode, and the second signal line comprises a gate line separated by the data line and connected with the first gate electrode.

**4**. The thin film transistor liquid crystal display panel according to claim 1, further comprising:

a first drive circuit to drive the first signal line; and

a second drive circuit to drive the second signal line,

wherein at least one of the first or second drive circuits comprises the first thin film transistor and a second thin film transistor that has a different semiconductor layer from the first thin film transistor.

**5**. The thin film transistor liquid crystal display panel according to claim 4, wherein the second thin film transistor comprises:

a second semiconductor layer doped with a second impurity;

a second gate electrode overlapping the second semiconductor layer with a second insulating pattern therebetween; and

a second source electrode and a second drain electrode separated from the second gate electrode and connected with the second semiconductor layer.

**6**. The thin film transistor liquid crystal display panel according to claim 1, further comprising a storage line overlapping the pixel electrode with the passivation film therebetween to form a storage capacitor,

wherein the first signal line comprises a gate line connected with the first gate electrode, and the second signal line comprises a data line separated by the gate line and connected with the first source electrode, or

wherein the first signal line comprises a data line connected with the first source electrode, and the second signal line comprises a gate line separated by the data line and connected with the first gate electrode.

**7**. The thin film transistor liquid crystal display panel according to claim 6, wherein the storage line is parallel to the gate line and the data line is separated by the storage line.

**8**. The thin film transistor liquid crystal display panel according to claim 6, wherein the storage line is parallel to the gate line and the storage line is separated by the data line.

**9**. The thin film transistor liquid crystal display panel according to claim 7, further comprising:

a plurality of third contact holes penetrating the passivation film such that sides of parts of the data line separated by the storage line are exposed; and

a second contact electrode connecting the parts of the data line separated by the storage line through the third contact holes.

**10**. The thin film transistor liquid crystal display panel according to claim 9, wherein the pixel electrode and the first and second contact electrodes comprise a transparent conductive layer.

**11**. The thin film transistor liquid crystal display panel according to claim 8, further comprising:

a plurality of third contact holes penetrating the passivation film such that sides of parts of the storage line separated by the data line are exposed; and

a second contact electrode connecting the parts of the storage line separated by the data line through the third contact holes.

**12**. The thin film transistor liquid crystal display panel according to claim 11, wherein the pixel electrode and the first and second contact electrodes comprise a transparent conductive layer.

**13**. The thin film transistor liquid crystal display panel according to claim 6, wherein the gate line, the data line, the gate electrode, the source electrode, the drain electrode and the storage line are formed of the same material.

**14**. The thin film transistor liquid crystal display panel according to claim 1, wherein the first semiconductor layer comprises:

a channel area overlapping the gate electrode; and

a source area and a drain area connected with the source electrode and the drain electrode, respectively, the source and drain areas doped with the first impurity.

**15**. The thin film transistor liquid crystal display panel according to claim 14, wherein the first semiconductor layer further comprises an LDD (lightly doped drain)region formed on sides of the channel area.

**16**. The thin film transistor liquid crystal display panel according to claim 5, wherein the second semiconductor layer comprises:

a channel area overlapping the gate electrode; and

a source area and a drain area connected with the source electrode and the drain electrode, respectively, the source and drain areas doped with the second impurity.

**17**. A method of fabricating a thin film transistor liquid crystal display panel, the method comprising:

forming a first semiconductor layer on a substrate;

doping the first semiconductor layer with a first impurity to form a source area and a drain area of the first semiconductor layer;

forming a first insulating pattern overlapping a channel area between the source and drain areas;

forming a first conductive pattern group on the substrate, wherein the first conductive pattern group has a gate line, a first gate electrode connected with the gate line and overlapping the first insulating pattern, a first source electrode and a first drain electrode connected with the source and drain areas of the first semiconductor layer, respectively, and a data line connected with the first source electrode, at least one of the gate or data lines being discontinuous;

forming a passivation film on the substrate where the first conductive pattern group is formed, a first contact hole that exposes the first drain electrode, and a second contact hole that exposes a part of the discontinuous line; and

forming a pixel electrode connected with the first drain electrode through the first contact hole, and a first contact electrode that connects the discontinuous line through the second contact hole.

18. The fabricating method according to claim 17, further comprising:

forming a second semiconductor layer on the substrate;

doping the second semiconductor layer with a second impurity to form a source area and a drain area of the second semiconductor layer;

forming a second insulating pattern overlapping a channel area between the source and drain areas of the second semiconductor layer; and

forming a second gate electrode overlapping the second insulating pattern, and a second source electrode and a second drain electrode connected with the source and drain areas of the second semiconductor layer on the substrate.

19. The fabricating method according to claim 18, wherein doping of the first impurity to formation of the first insulating pattern, and doping of the second impurity to formation of the second insulating pattern comprises:

forming an insulating film on the surface of the substrate containing the first and second semiconductor layers;

forming a first photo resist pattern shielding the second semiconductor layer and the channel area of the first semiconductor layer on the insulating film;

doping the first semiconductor with the first impurity using the first photo resist pattern as a mask;

forming the first insulating pattern by etching the insulating film using the first photo resist pattern as a mask;

forming a second photo resist pattern shielding the channel area of the second semiconductor layer and shielding the first semiconductor layer;

doping the second semiconductor layer with the second impurity using the second photo resist pattern as a mask; and

forming the second insulating pattern by etching the insulating film using the second photo resist pattern as a mask.

20. The fabricating method according to claim 17, further comprising forming an LDD region by doping the first semiconductor layer with a third impurity through sides of the first insulating pattern exposed by the gate electrode.

21. The fabricating method according to claim 17, further comprising forming a storage line overlapped by the pixel electrode with the passivation film therebetween on the substrate.

22. The fabricating method according to claim 21, further comprising:

forming at least one of the data or storage lines such that the at least one of the data or storage lines is discontinuous and forming a third contact hole to expose the at least one of the data or storage lines; and

forming a second contact electrode connecting the at least one of the data or storage lines through the third contact hole.

23. The fabricating method according to claim 22, wherein the pixel electrode and the first and second contact electrodes are formed of a transparent conductive layer.

24. The fabricating method according to claim 17, further comprising forming a buffer film between the substrate and the first semiconductor layer.

25. A thin film transistor liquid crystal display panel, comprising:

gate, data, and storage lines disposed on the same layer in a display area of the liquid crystal display panel, at least one of the gate, data, or storage lines being discontinuous in the display area and at least one of the gate, data, or storage lines being continuous in the display area, the continuous line bisecting segments of the discontinuous line in the display area;

a thin film transistor having a semiconductor layer, a gate electrode overlapping the semiconductor layer with an insulating pattern therebetween, and source and drain electrodes separated from the gate electrode and connected with the semiconductor layer;

a passivation layer on the thin film transistor and the gate, data, and storage lines; and

a contact electrode connecting the segments of the discontinuous line through first contact holes in the passivation layer.

26. The thin film transistor liquid crystal display panel according to claim 25, wherein the storage line is parallel to the gate line.

27. The thin film transistor liquid crystal display panel according to claim 26, wherein the data line is discontinuous and the gate line is continuous.

28. The thin film transistor liquid crystal display panel according to claim 27, wherein the storage line is continuous.

29. The thin film transistor liquid crystal display panel according to claim 26, wherein the gate line is discontinuous and the data line is continuous.

30. The thin film transistor liquid crystal display panel according to claim 29, wherein the storage line is discontinuous.

31. The thin film transistor liquid crystal display panel according to claim 25, further comprising a pixel electrode connected with the drain electrode through a second contact hole in the passivation layer, the storage line overlapping the pixel electrode with the passivation film therebetween to form a storage capacitor.

32. The thin film transistor liquid crystal display panel according to claim 31, wherein the pixel electrode and the contact electrode comprise a transparent conductive layer.

33. The thin film transistor liquid crystal display panel according to claim 25, wherein the gate, data, and storage lines and the gate, source, and drain electrodes are formed of the same material.

34. The thin film transistor liquid crystal display panel according to claim 25, wherein the semiconductor layer comprises:a channel area overlapping the gate electrode; source and drain areas connected with the source electrode and the drain electrode, respectively; and LDD regions formed between the channel and source areas and between the channel and drain areas.

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摘要(译)

描述了薄膜晶体管（TFT）液晶显示面板和制造方法。该面板具有数据线和与TFT连接并形成在同一层上的栅极线。数据或栅极线之一是不连续的，而另一个在像素区域中是连续的，使得连续线将不连续线平分。钝化膜保护TFT。接触孔穿透钝化膜并暴露不连续线的区段。接触电极通过接触孔连接各段。