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(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2005/0157220 A1**
Kim (43) **Pub. Date: Jul. 21, 2005**(54) **THIN FILM TRANSISTOR ARRAY
SUBSTRATE FOR LIQUID CRYSTAL
DISPLAY**(76) **Inventor: Dong-Gyu Kim, Suwon-city (KR)**

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(21) **Appl. No.: 11/079,734**(22) **Filed: Mar. 15, 2005****Related U.S. Application Data**(63) Continuation of application No. 09/964,645, filed on
Sep. 28, 2001, now Pat. No. 6,882,375.(30) **Foreign Application Priority Data**

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Publication Classification(51) **Int. Cl.⁷ G02F 1/1343; G02F 1/136**(52) **U.S. Cl. 349/38; 349/43**(57) **ABSTRACT**

A thin film transistor array substrate for a liquid crystal display includes a substrate, and a gate line assembly formed on the substrate to receive gate signals. The gate line assembly has gate lines proceeding in the horizontal direction, and gate electrodes connected to the gate lines. A storage capacitor line assembly proceeds in the horizontal direction. A gate insulating layer is formed on the substrate while covering the gate lines and the storage capacitor line assembly. A semiconductor pattern is formed on the gate insulating layer over the gate electrodes. A data line assembly is formed on the gate insulating layer. The data line assembly has data lines crossing over the gate lines to define pixel regions, source electrodes connected to the data lines while being placed on the semiconductor pattern, and drain electrodes facing the source electrodes around the gate electrodes while being placed on the semiconductor pattern. A protective layer covers the data line assembly and the semiconductor pattern with contact holes. Pixel electrodes are formed on the protective layer at the respective pixel regions such that the pixel electrodes are connected to the drain electrodes through the contact holes. The gate lines or the pixel electrodes are provided with repair members, and the repair members are partially overlapped with the front gate lines or the pixel electrodes.

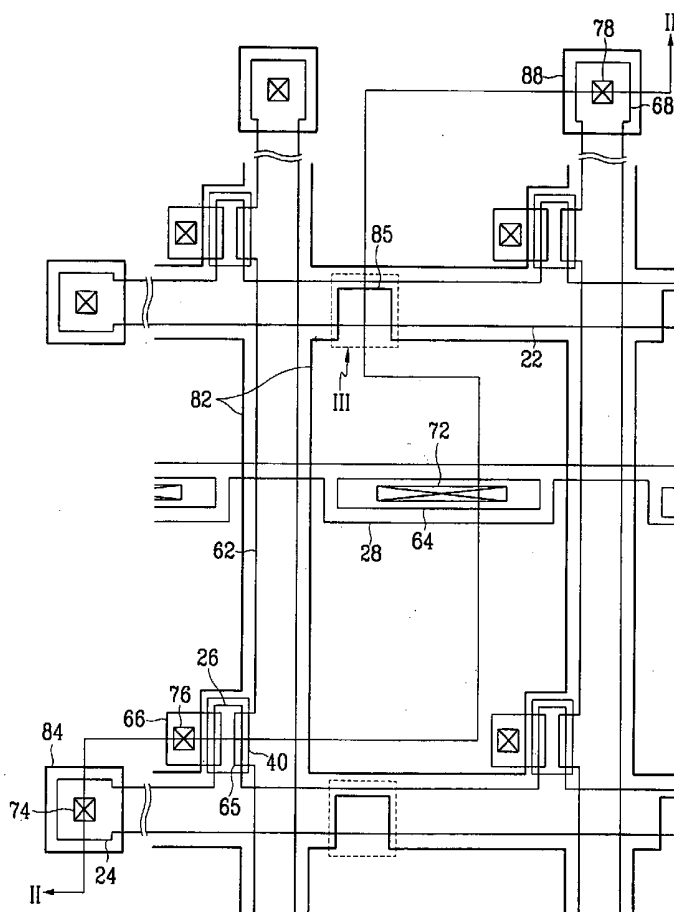


FIG. 1

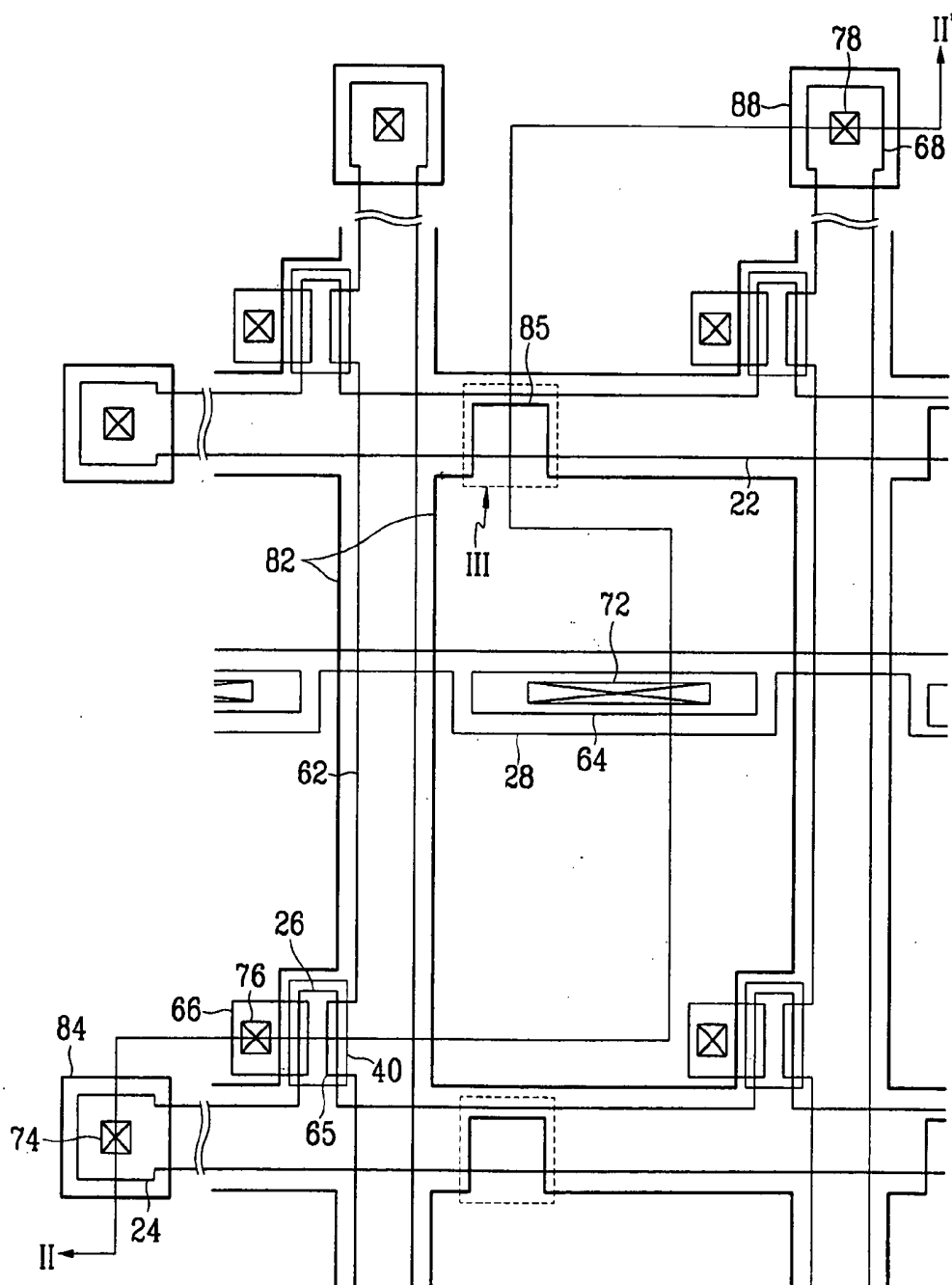


FIG. 2

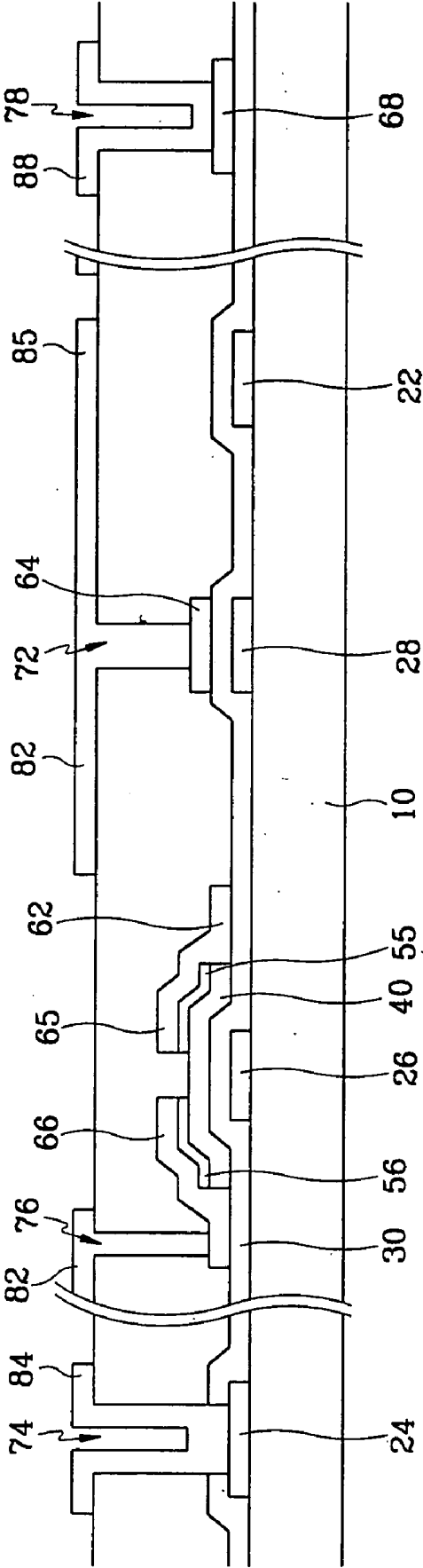


FIG. 3

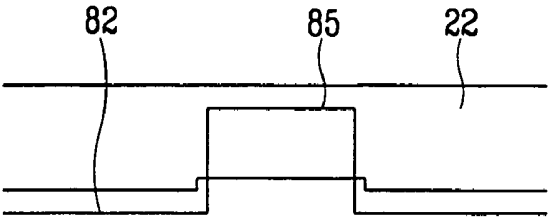


FIG. 4A

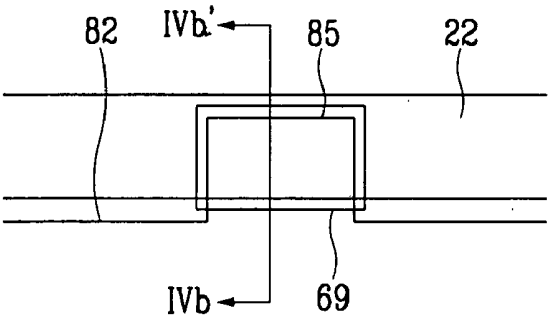


FIG. 4B

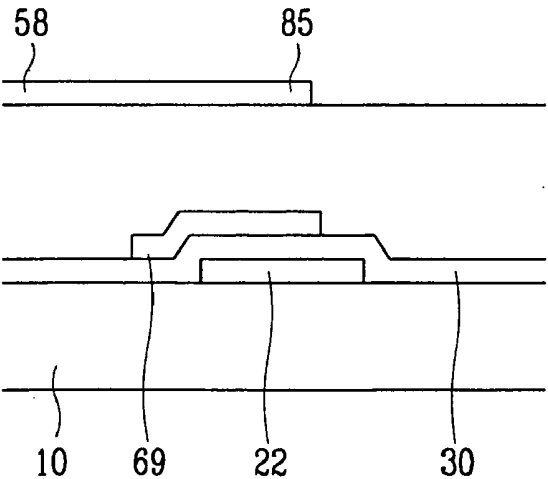


FIG. 5A

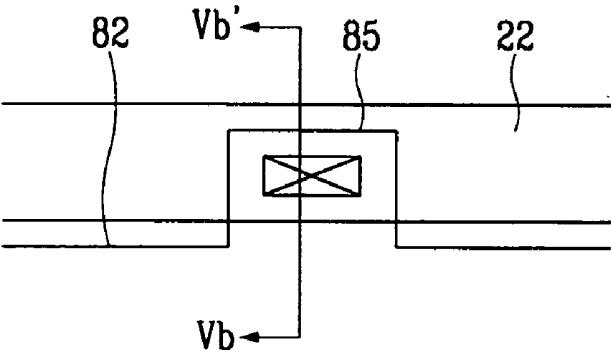


FIG. 5B

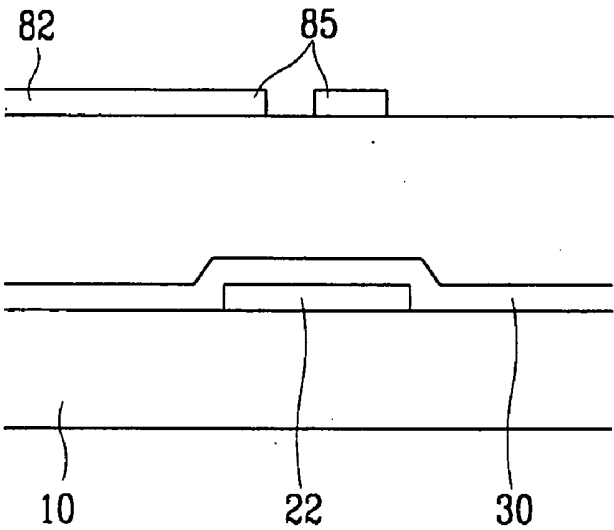


FIG. 6

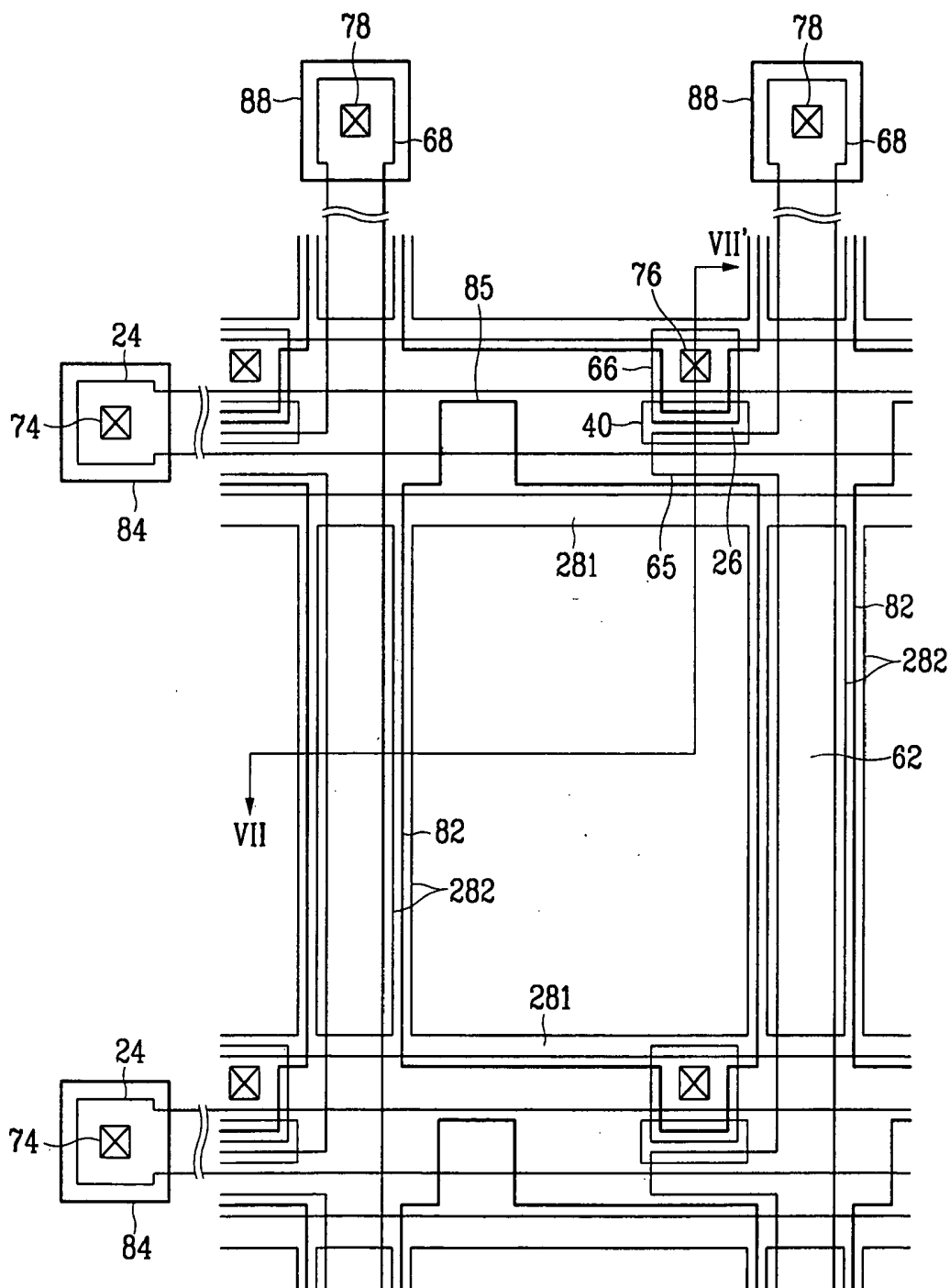


FIG. 7

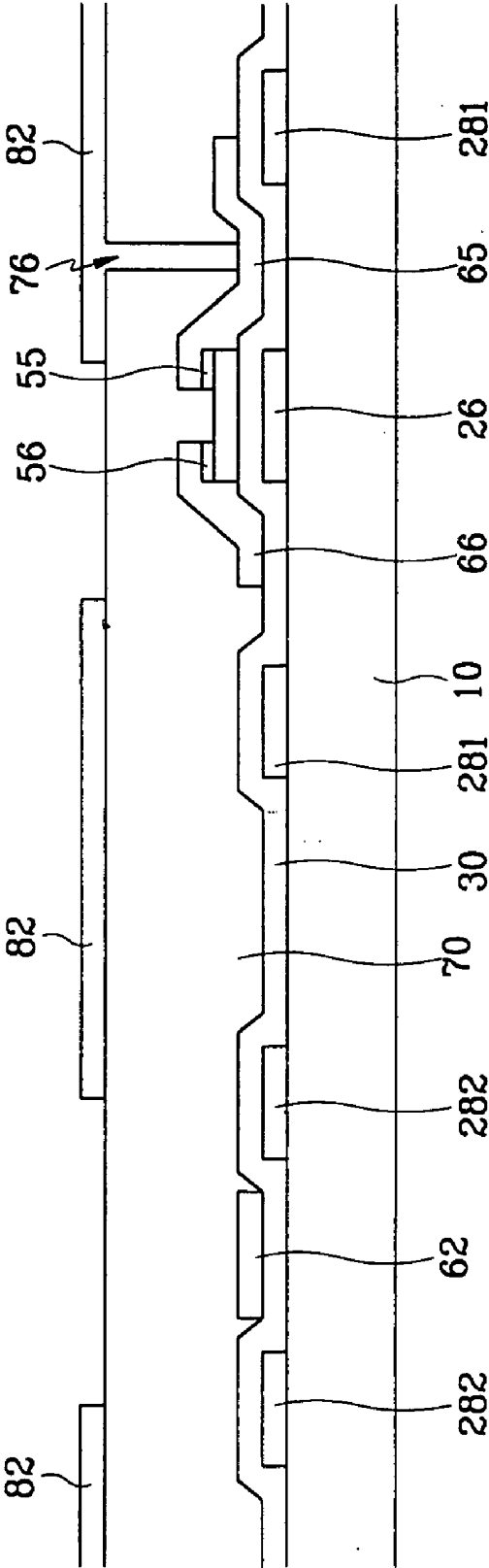
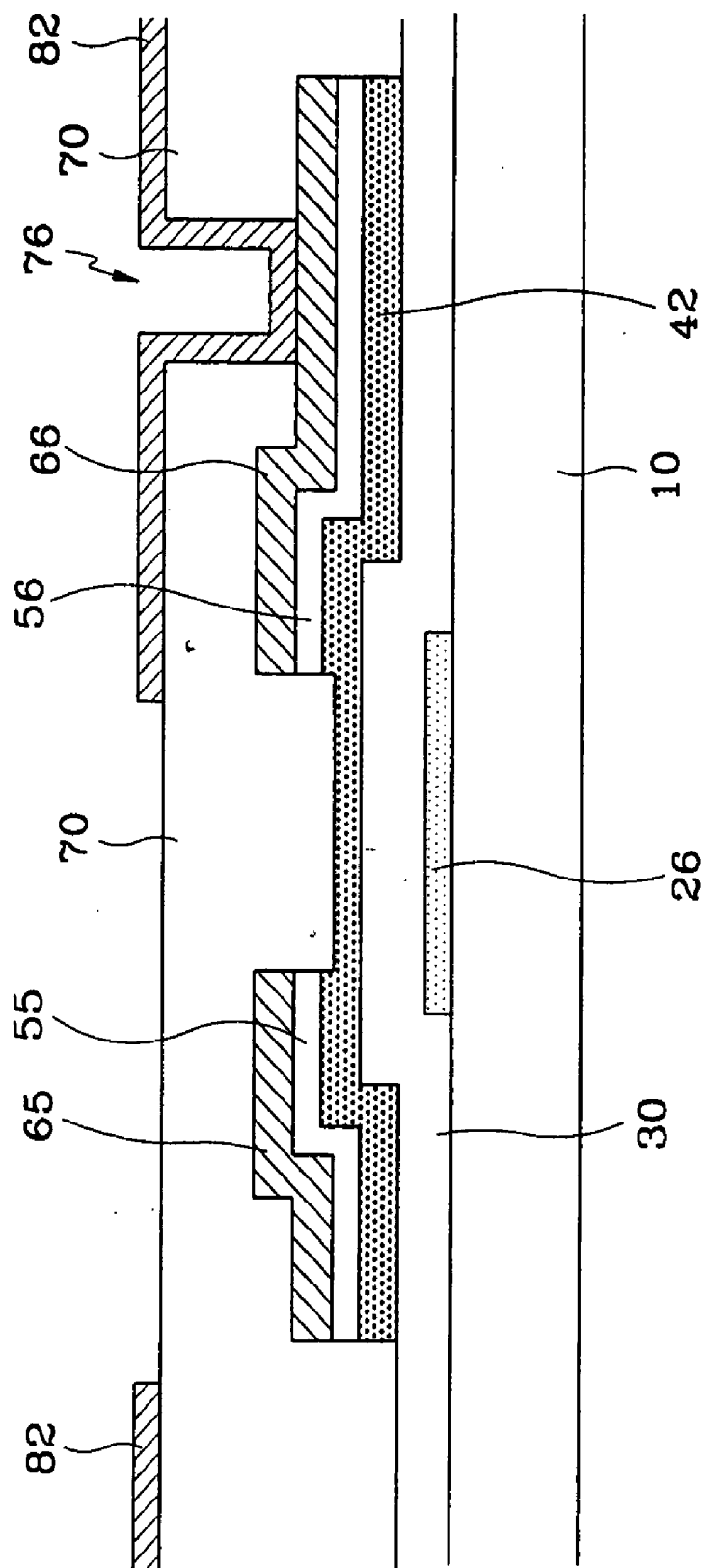


FIG. 10



THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to a thin film transistor array substrate for a liquid crystal display and, more particularly, to a thin film transistor array substrate having a pixel electrode to display images at unit pixel area.

[0003] (b) Description of the Related Art

[0004] Generally, a liquid crystal display has a structure where a liquid crystal is sandwiched between two substrates each having electrodes. By applying voltages to the respective electrodes, light transmission through the liquid crystal is controlled.

[0005] The liquid crystal display bears a matrix-type pixel structure with a plurality of pixels, and a pixel electrode is formed at each pixel region. The pixel electrode is driven by driving signals applied thereto via wiring lines. The pixel regions are defined by the crossing of gate lines and data lines. The gate lines and the data lines are connected to the pixel electrodes via switching circuits such as thin film transistors (TFTs). The switching circuit controls the picture signals applied to the pixel electrode based on the scanning signals from the gate line. A storage capacitor line is provided at each pixel region to form a storage capacitor together with the pixel electrode. The storage capacitor stores the present pixel signals applied to the pixel electrode until the arrival of subsequent pixel signals.

[0006] In the process of fabricating the above-structured thin film transistor array substrate, pixel defects are liable to be generated, causing increased production cost. Among such pixel defects, the white defect is easily visible to naked eyes because the pixel is displayed constantly bright. Therefore, it is preferable that the white defect should be shifted into a black defect where the pixel is displayed to be constantly dark.

[0007] The white defect is caused by contact failure between the pixel electrode and the switching element, or malfunction of the switching element. A dark image is initially displayed and, as time passes by, current leaks at the pixel electrode so that the pixel voltage is approximated up to the common voltage of the common electrode facing the pixel electrode. This results in a white defect.

[0008] Furthermore, the white defect may be caused by short circuit between the data line and the pixel electrode due to the residual conductive material, or short circuit between the pixel electrode and the common electrode.

[0009] Among the techniques of repairing such a white defect into a black defect, there is a technique where the pixel electrode is short-circuited with the gate line that is overlapped with the pixel electrode while receiving gate signals from the gate line. In this case, the gate line transmits the gate signals to the switching circuits of the neighboring pixel line. The gate line is overlapped with the pixel electrodes, thereby functioning as a part of storage capacitor.

[0010] However, in a liquid crystal display separately having a storage wiring line being provided to form storage capacitors while being overlapped with the pixel electrodes,

because the common voltage is transmitted to the separate storage wiring line, there is still a possibility of white defect even with short-circuiting between the storage wiring line and the pixel electrodes.

SUMMARY OF THE INVENTION

[0011] It is an object of the present invention to provide a thin film transistor array substrate for a liquid crystal display which has a pixel structure capable of repairing a white defect while bearing a separate storage line assembly.

[0012] This and other objects may be achieved by a thin film transistor array substrate for a liquid crystal display with the following features.

[0013] The thin film transistor array substrate is provided with repair members such that they are overlapped with the previous gate lines transmitting gate signals to pixel regions of a previous row. Here, the repair members are extended from pixel electrodes or gate lines, respectively.

[0014] Specifically, the thin film transistor array substrate includes a substrate, and a gate line assembly formed on the substrate to receive gate signals. The gate line assembly has gate lines proceeding in the horizontal direction, and gate electrodes connected to the gate lines. A storage capacitor line assembly proceeds in the horizontal direction to receive common voltages. A gate insulating layer is formed on the substrate while covering the gate lines and the storage capacitor line assembly. A semiconductor pattern is formed on the gate insulating layer over the gate electrodes. A data line assembly is formed on the gate insulating layer. The data line assembly has data lines crossing over the gate lines to define pixel regions, source electrodes connected to the data lines while being placed on the semiconductor pattern, and drain electrodes facing the source electrodes around the gate electrodes while being placed on the semiconductor pattern. A protective layer covers the data line assembly and the semiconductor pattern while bearing first and second contact holes. Pixel electrodes are formed on the protective layer at the respective pixel regions such that the pixel electrodes are connected to the drain electrodes through the first contact holes. The gate lines or the pixel electrodes are provided with repair members, and the repair members are partially overlapped with the front gate lines or the pixel electrodes.

[0015] The thin film transistor array substrate may further include storage capacitor conductive patterns overlapped with the storage capacitor line assembly while interposing the gate insulating layer. The storage capacitor conductive patterns are connected to the pixel electrodes through the second contact holes.

[0016] The storage capacitor line assembly may include double storage capacitor electrode lines horizontally formed at the top and the bottom of each pixel region, and storage capacitor electrodes vertically formed at the periphery of the pixel region while interconnecting the storage capacitor electrode lines.

[0017] The parts of the gate lines overlapped with the repair members preferably have a width smaller than other parts thereof.

[0018] The thin film transistor array substrate may further include subsidiary repair members disposed between the

repair members and the gate lines. The subsidiary repair members are preferably placed at the same plane as the data line assembly.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components.

[0020] **FIG. 1** is a plan view of a thin film transistor array substrate for a liquid crystal display according to a first preferred embodiment of the present invention;

[0021] **FIG. 2** is a cross sectional view of the thin film transistor array substrate taken along the II-II' line of **FIG. 1**;

[0022] **FIG. 3** is an amplified view of the thin film transistor array substrate shown in **FIG. 1** at the III portion thereof;

[0023] **FIG. 4A** illustrates a subsidiary repairing unit for the thin film transistor array substrate shown in **FIG. 1**;

[0024] **FIG. 4B** is a cross sectional view of the thin film transistor array substrate taken along the IVb-IVb' line of **FIG. 4A**;

[0025] **FIG. 5A** illustrates a ring-shaped repairing unit for the thin film transistor array substrate shown in **FIG. 1**;

[0026] **FIG. 5B** is a cross sectional view of the thin film transistor array substrate taken along the Vb-Vb' line of **FIG. 5A**;

[0027] **FIG. 6** is a plan view of a thin film transistor array substrate for a liquid crystal display according to a second preferred embodiment of the present invention;

[0028] **FIG. 7** is a cross sectional view of the thin film transistor array substrate taken along the VII-VII' line of **FIG. 6**;

[0029] **FIG. 8** is a plan view of a thin film transistor array substrate for a liquid crystal display according to a third preferred embodiment of the present invention; and

[0030] **FIGS. 9 and 10** are cross sectional views of the thin film transistor array substrate taken along the IX-IX' line and X-X' line of **FIG. 8**, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

[0032] **FIG. 1** is a plan view of a thin film transistor array substrate for a liquid crystal display according to a first preferred embodiment of the present invention, and **FIG. 2** is a cross sectional view of the thin film transistor array substrate taken along the II-II' line of **FIG. 1**.

[0033] As shown in the drawings, a gate line assembly and storage capacitor lines **28** with a single or multiple-layered structure are formed on an insulating substrate **10** of an aluminum-based conductive material. The gate line assembly

includes gate lines **22** proceeding in the horizontal direction, gate pads **24** connected to ends of the gate lines **22** to receive gate signals from the outside and transmit them to the gate lines **22**, and gate electrodes **26** for thin film transistors connected to the gate lines **22**. The storage capacitor lines **28** proceed in the horizontal direction while being overlapped with storage capacitor conductive patterns **64** to be electrically connected to pixel electrodes **82**, thereby forming storage capacitors. Common voltages that are applied to a common electrode of a counter substrate (not shown) facing the insulating substrate **10** are applied to the storage capacitor lines **28**. In case the gate line assembly has a multiple-layered structure, it may contain pad materials bearing a good contact characteristic with other materials. Gate signals may be transmitted to the storage capacitor lines **28**.

[0034] A gate insulating layer **30** is formed on the substrate **10** with silicon nitride to cover the gate line assembly and the storage capacitor lines **28**.

[0035] A semiconductor layer **40** is formed on the gate insulating layer **30** of the gate electrodes **24** with a semiconductor material such as amorphous silicon. Ohmic contact layers **55** and **56** are formed on the semiconductor layer **40** with silicide, or n+ hydrogenated amorphous silicon where n type impurities are doped at high concentration.

[0036] A data line assembly bearing a single or multiple-layered structure is formed on the ohmic contact layers **55** and **56** and the gate insulating layer **30** with a low resistance material such as silver or aluminum. The data line assembly includes data lines **62** proceeding in the vertical direction while crossing over the gate lines **22** to form matrix-typed pixel regions, and source electrodes **65** connected to the data lines **62** while being extended over the ohmic contact layer **55**. Data pads **68** are connected to one-sided ends of the data lines **62** to receive picture signals from the outside. Drain electrodes **66** are placed on the ohmic contact layer **56** opposite to the source electrodes **65** around the gate electrodes **26** while being separated from the source electrodes **65**. The data line assembly may further include storage capacitor conductive patterns **64** that are overlapped with the storage capacitor lines **28**, thereby forming storage capacitors.

[0037] A protective layer **70** is formed on the data line assembly and the semiconductor layer **40** exposed through the data line assembly with silicon nitride or an organic material bearing a good planarization characteristic.

[0038] The protective layer **70** is provided with contact holes **72**, **76** and **78** exposing the storage capacitor conductive patterns **64**, the drain electrodes **66**, and the data pads **68**, respectively. The protective layer **70** further has contact holes **74** exposing the gate pads **24** together with the gate insulating layer **30**.

[0039] Pixel electrodes **82** are formed on the protective layer **70** at pixel regions such that they are electrically connected to the storage capacitor conductive patterns **64** and the drain electrodes **66**. The pixel electrodes **82** have repair members **85** that are partially protruded while being overlapped with the neighboring front gate lines **22** for transmitting gate signals to the front pixel lines. As subsidiary gate **84** and a subsidiary data pad **88** are formed on the protective layer **70** such that they are connected to the gate

pad 24 and the data pad 68 through the contact holes 74 and 78. The pixel electrodes 82, and the subsidiary gate pad 84 and the subsidiary data pad 88 are formed with a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). The repair member 85 easily shifts the white defect occurring at the pixel when the pixel electrode 82 is floating, or receives a common voltage into a black defect nearly invisible with naked eyes. When the white defect occurs, the front gate line 22 is short-circuited with the pixel electrodes 82 through the repair members 85, and gate off voltages are applied to the pixel electrodes 82 without electric field in the normally white mode liquid crystal display. Consequently, an electric field of about 10V is formed between the pixel electrodes 82 and the common electrode, thereby shifting the white defect at the pixels into a black defect.

[0040] Since the pixel electrodes 82 are formed with a transparent conductive material, it may become difficult to find the correct position of the repair members 85 during the process of repairing the pixels through short-circuiting the repair members 85 with the gate lines 22 using laser. In order to solve such a problem, it is preferable that the parts of gate lines 22 corresponding to the repair members 85 is shaped differently from other parts. For instance, as shown in FIG. 3, the part of the gate line 22 overlapped with the repair member 85 may be narrower than other parts.

[0041] Furthermore, as shown in FIG. 2, the gate insulating layer 30 and the protective layer 70 are disposed between the gate lines 22 and the repair members 85. Thus, it may become difficult to short-circuit the gate lines 22 with the repair members 85 using laser. In order to solve such a problem, as shown in FIGS. 4A and 4B, subsidiary repair members 69 may be formed between the gate insulating layer 30 and the protective layer 70 at the same plane as the data line assembly. It is preferable that the subsidiary repair members 69 are partially extended external to the gate lines 22 to easily find the positions of the repair members 85.

[0042] As shown in FIGS. 5A and 5B, the structure of the repair member 85 may be ring-shaped with a central opening portion.

[0043] Meanwhile, in order to prevent short circuit of the storage capacitor lines while improving the pixel opening ratio, the storage capacitor lines may be formed with a different structure.

[0044] FIG. 6 is a plan view of a thin film transistor array substrate for a liquid crystal display according to a second preferred embodiment of the present invention, and FIG. 7 is a cross sectional view of the thin film transistor array substrate taken along the VII-VII' line of FIG. 6. In this preferred embodiment, other components of the thin film transistor array substrate are the same as those related to the first preferred embodiment except for the following features.

[0045] The gate lines 22 are partially used as gate electrodes 26. Storage capacitor line assembly proceeds in the horizontal direction. The storage capacitor line assembly includes storage capacitor electrode lines 281 placed at the top and the bottom of the pixels, and storage capacitor electrodes 282 interconnecting the storage capacitor electrode lines 281 while proceeding in the vertical direction at the periphery of pixels. In this structure, the short circuit of the storage capacitor line assembly 281 and 282 can be prevented. Furthermore, the storage capacitor line assembly 281 and 282 is overlapped with the periphery of the pixel

electrode while forming storage capacitors. This insures sufficient amount of storage capacity and opening ratio.

[0046] The semiconductor layer 40 is formed internally at the gate electrodes 26, and the source electrodes 65 proceed horizontally along the gate electrodes 26 while being extended over one side of ohmic contact layer 55. The drain electrodes 66 are formed on the otherside of ohmic contact layer 56 placed opposite to the source electrodes 65 with respect to the gate electrodes 26.

[0047] In this structure, the part of the gate line 22 overlapped with the repair member 85 may be formed narrower than other parts, and a subsidiary repair member may be provided between the repair member 85 and the gate line 22.

[0048] Meanwhile, the gate lines 22 may be partially protruded such that they bear repair members overlapped with the pixel electrodes. This structure will be explained with reference to FIGS. 8 to 10.

[0049] FIG. 8 is a plan view of a thin film transistor array substrate for a liquid crystal display according to a third preferred embodiment of the present invention. FIGS. 9 and 10 are cross sectional views of the thin film transistor array substrate taken along the IX-IX' line and the X-X' line of FIG. 8, respectively. In this preferred embodiment, other components of the thin film transistor array substrate are the same as those related to the first preferred embodiment except for the following features.

[0050] The front gate lines 22 that transmit gate signals to the neighboring pixels are partially protruded while overlapping the pixel electrodes 82.

[0051] Semiconductor patterns 42 and 48 are formed on the gate insulating layer 30. Ohmic contact patterns 55, 56 and 58 are formed on the semiconductor patterns 42 and 48 with amorphous silicon where n type impurities such as phosphorous (P) are doped at high concentration. The ohmic contact patterns 55, 56 and 58 lower the contact resistance between the underlying semiconductor patterns 42 and 48 and the overlying data line assembly, and bear the same outline as the data line assembly. That is, the first ohmic contact pattern 55 has the same outline as the data lines 62, the source electrodes 65 and the data pads 68, the second ohmic contact pattern 56 has the same outline as the drain electrodes 66, and the third ohmic contact pattern 58 has the same outline as the storage capacitor conductive patterns 64.

[0052] The semiconductor patterns 42 and 48 have the same outline as the data line assembly and the ohmic contact patterns 55, 56 and 58 except for the channel portions C. Specifically, the semiconductor pattern 48, the conductive pattern 64 and the ohmic contact pattern 58 for the storage capacitor have the same outline, but the semiconductor pattern 42 for the TFT differs in shape from the relevant portions of the data line assembly and the ohmic contact pattern. That is, the source and the drain electrodes 65 and 66 as well as the underlying ohmic contact patterns 55 and 56 are separated from each other at the channel portion C. However, the semiconductor pattern 42 for the TFT continuously proceeds at that channel portion C while forming a TFT channel.

[0053] As shown in FIGS. 5A and 5B, the repair member 25 may be formed with a ring shape.

[0054] As described above, in the first to third preferred embodiments of the present invention, the volume of overlapping between the repair member 85 of the pixel electrode

82 and the front gate line 22, or between the repair member 25 of the front gate line 22 and the pixel electrode 82 is preferably in the range of 5-10000 μm^2 .

[0055] A method for fabricating the thin film transistor array substrate will be now explained with reference to FIGS. 1 to 7.

[0056] A silver or aluminum-based layer bearing a low resistance is deposited onto an insulating substrate 10, and patterned through photolithography to thereby form a gate line assembly 22, 24 and 26, and a storage capacitor line assembly 28, 281 and 282.

[0057] Thereafter, a silicon nitride-based gate insulating layer 30, an amorphous silicon-based semiconductor layer, and a doped amorphous silicon-based layer are sequentially deposited onto the substrate 10. The semiconductor layer, and the doped amorphous silicon-based layer are patterned to thereby form a semiconductor pattern 40 and an ohmic contact pattern on the gate insulating layer 30 over the gate electrodes 26. At this time, the semiconductor pattern 40 and the ohmic contact pattern bear the same shape.

[0058] A conductive material is then deposited onto the substrate 10, and patterned through photolithography to thereby form a data line assembly. If the required storage capacity is sufficiently obtained, the storage capacitor conductive pattern 64 may be dispensed. As shown in FIGS. 4A and 4B, subsidiary repair members 69 may be formed on the same plane as the data line assembly to easily repair the possible white defect.

[0059] The ohmic contact pattern exposed through the data line assembly is etched to thereby complete ohmic contact patterns 55 and 56 around the gate electrode 26 while exposing the semiconductor pattern 40 between them. Thereafter, oxygen plasma is preferably performed with respect to the exposed semiconductor pattern 40 to stabilize the surface thereof.

[0060] Thereafter, an insulating material such as silicon nitride or an organic material bearing low dielectric property and good planarization characteristic is deposited onto the substrate 10 to thereby form a protective layer 70. The protective layer 70 is patterned together with the gate insulating layer 30 to thereby form contact holes 72, 74, 76 and 78 exposing the storage capacitor conductive patterns 64, the gate pads 24, the drain electrodes 66 and the data pads 68, respectively. If the storage capacitor conductive patterns 64 are absent, the contact holes 72 may be omitted.

[0061] Finally, an ITO or IZO-based layer is deposited onto the protective layer 70, and patterned through a mask to thereby form pixel electrodes 82, and subsidiary gate pads 84 and subsidiary data pads 88. The pixel electrodes 82 are connected to the storage capacitor conductive patterns 64 and the drain electrodes 66 through the contact holes 72 and 76, and have repair members 85 overlapped with the gate lines 22. The subsidiary gate pads 84 and the subsidiary data pads 88 are connected to the gate pads 24 and the data pads 68 through the contact holes 74 and 78.

[0062] Meanwhile, the semiconductor patterns 42 and 48, the ohmic contact patterns 55, 56 and 58, and the data line assembly are formed through photolithography using a photoresist pattern, and this simplifies the relevant processing steps. Specifically, after forming the gate line assembly, the gate insulating layer 30, an amorphous silicon-based

semiconductor layer, and a doped amorphous silicon-based layer are sequentially deposited onto the substrate 10. Thereafter, a conductive material is deposited onto the doped amorphous silicon-based layer, and a photoresist film is coated onto the conductive material-based layer. The photoresist film is then exposed to light with a mask with a light transmission control film to thereby form a photoresist pattern with partially different in thickness. The photoresist pattern has a first portion corresponding to the data line assembly, and a second portion corresponding to the channel portion with a thickness smaller than the first portion. Semiconductor patterns 42 and 48 are formed using the photoresist pattern as an etching mask. The second portion of the photoresist pattern is then removed. The conductive material-based layer placed at the channel portion is removed using the first portion of the photoresist pattern as an etching mask to thereby form a data line assembly. The doped amorphous silicon layer is removed using the data line assembly as an etching mask to thereby complete ohmic contact patterns 55, 56 and 58.

[0063] As described above, in the inventive thin film transistor array substrate for a liquid crystal display, repair members are provided at the pixel electrodes such that they overlap the front gate line, thereby making it possible to easily repair the white defect occurring at the pixel area.

[0064] While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

1-11. (canceled)

12. A thin film transistor array substrate, comprising:

a substrate;

a plurality of gate lines formed on the substrate

a plurality of data lines intersecting the gate lines;

a plurality of pixel regions defined by the intersecting of the gate lines and the data lines;

a plurality of pixel electrodes formed in the pixel regions, respectively; and

a plurality of repair members, each extended from the corresponding pixel electrode and overlapping a gate line of a previous row.

13. A thin film transistor array substrate, comprising:

a substrate;

a plurality of gate lines formed on the substrate a plurality of data lines intersecting the gate lines;

a plurality of pixel regions defined by the intersecting of the gate lines and the data lines;

a plurality of pixel electrodes formed in the pixel regions, respectively; and

a plurality of repair members, each extended from the gate line of a previous row and overlapping the corresponding pixel electrode.

* * * * *

专利名称(译)	用于液晶显示器的薄膜晶体管阵列基板		
公开(公告)号	US20050157220A1	公开(公告)日	2005-07-21
申请号	US11/079734	申请日	2005-03-15
[标]申请(专利权)人(译)	金东GYU		
申请(专利权)人(译)	金东GYU		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	KIM DONG GYU		
发明人	KIM, DONG-GYU		
IPC分类号	G02F1/1368 G02F1/136 G02F1/1362 G09F9/00 H01L29/786 G02F1/1343		
CPC分类号	G02F1/136213 G02F2001/136268 G02F1/136286 G02F1/136259		
优先权	1020010026721 2001-05-16 KR		
其他公开文献	US7791681		
外部链接	Espacenet USPTO		

摘要(译)

一种用于液晶显示器的薄膜晶体管阵列基板，包括基板和形成在基板上以接收栅极信号的栅极线组件。栅极线组件具有在水平方向上行进的栅极线，并且栅极电极连接到栅极线。存储电容器线组件沿水平方向前进。在基板上形成栅极绝缘层，同时覆盖栅极线和存储电容器线组件。在栅电极上方的栅极绝缘层上形成半导体图案。数据线组件形成在栅极绝缘层上。数据线组件具有跨越栅极线的数据线以限定像素区域，在放置在半导体图案上时连接到数据线的源极电极，以及在放置在半导体图案上的同时面向栅极电极的源极电极的漏极电极。保护层覆盖数据线组件和具有接触孔的半导体图案。像素电极形成在各个像素区域处的保护层上，使得像素电极通过接触孔连接到漏电极。栅极线或像素电极设置有修复构件，并且修复构件与前栅极线或像素电极部分地重叠。

