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(54) METHOD FOR REDUCING POWER CONSUMPTION OF AN LCD PANEL IN A STANDBY MODE

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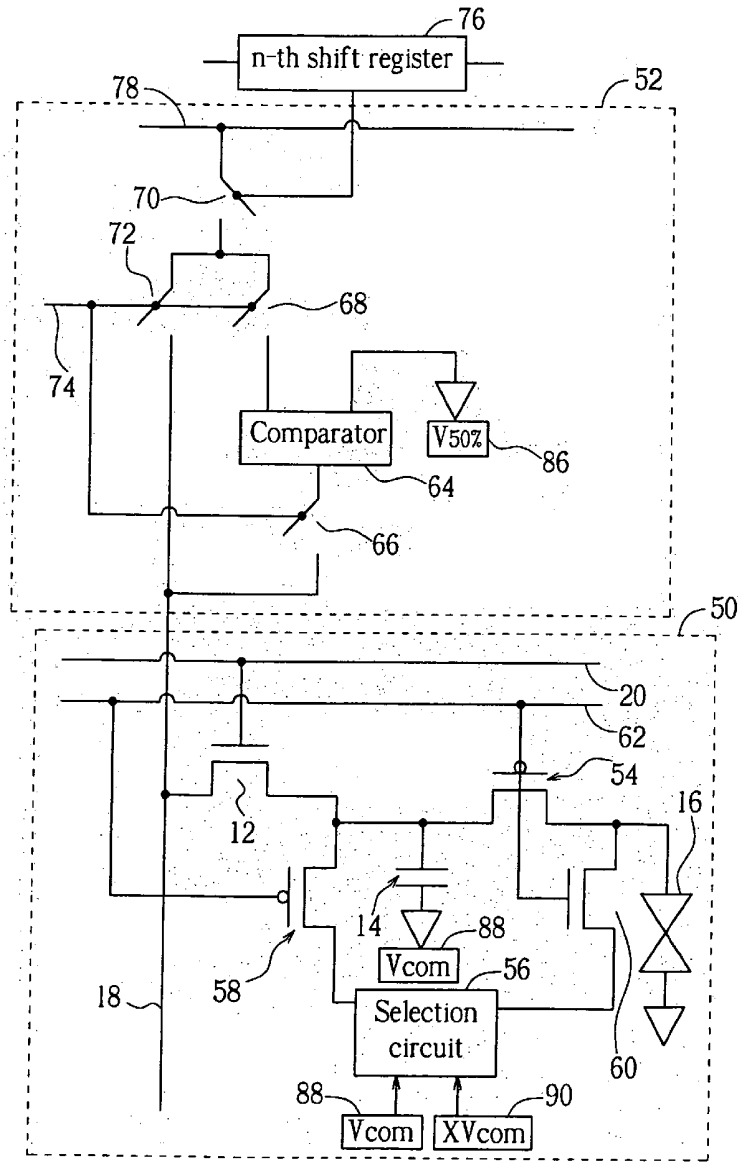
(57) **ABSTRACT**

A method for reducing power consumption of an LCD panel in a standby mode. The LCD panel includes a plurality of pixel drivers and a plurality of data drivers. Each pixel driver has a liquid crystal capacitor, a storage capacitor, a selection circuit, and four switches. Each data driver has a shift register, a comparator, and several switches. The method includes transmitting data from a signal line to the comparator and comparing the data with a reference voltage, then transmitting a corresponding control signal outputted from the comparator to the selection circuit via the data line, the selection circuit outputting a corresponding display signal to the liquid crystal capacitor according to the control signal.



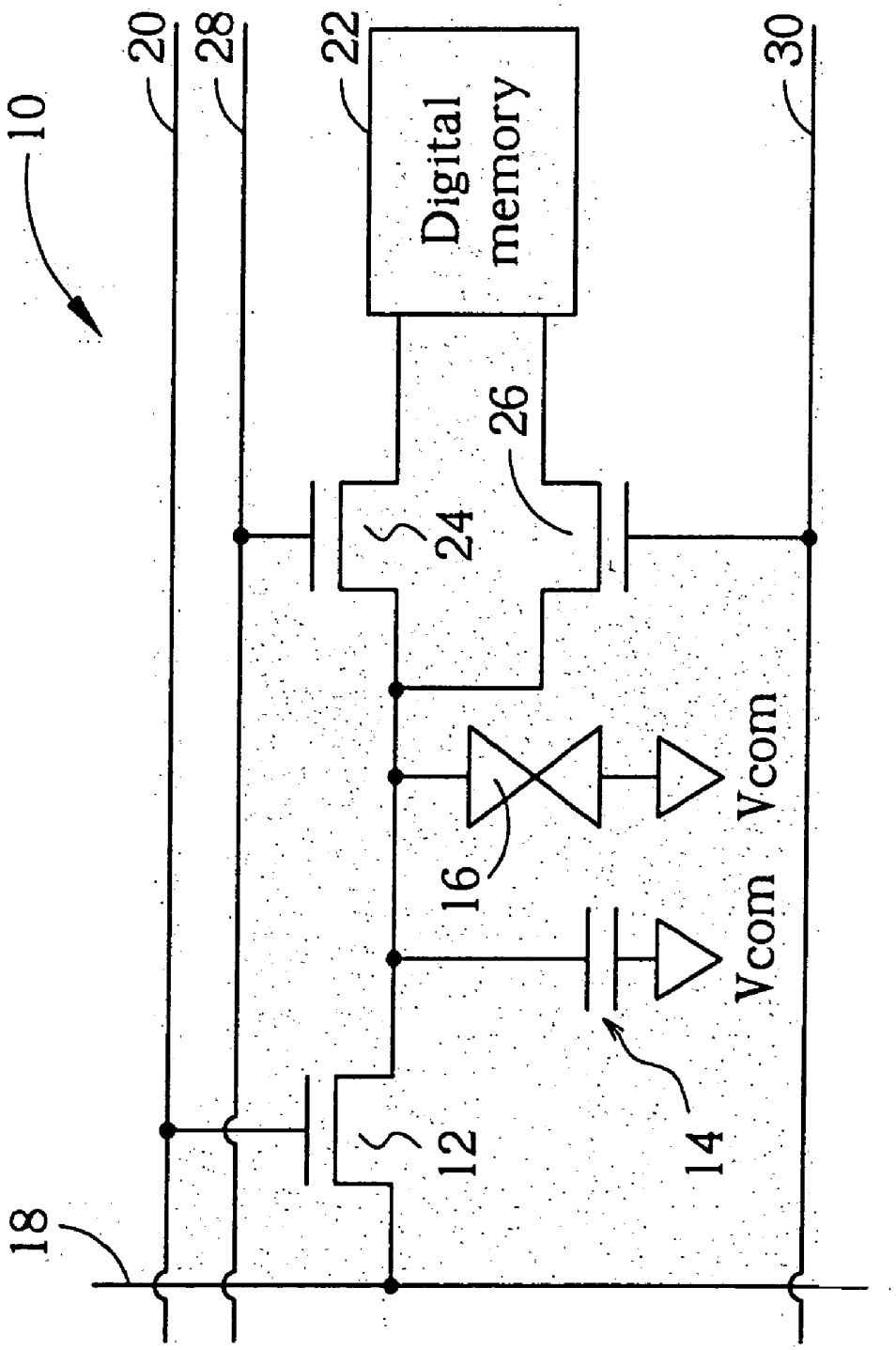


Fig. 1

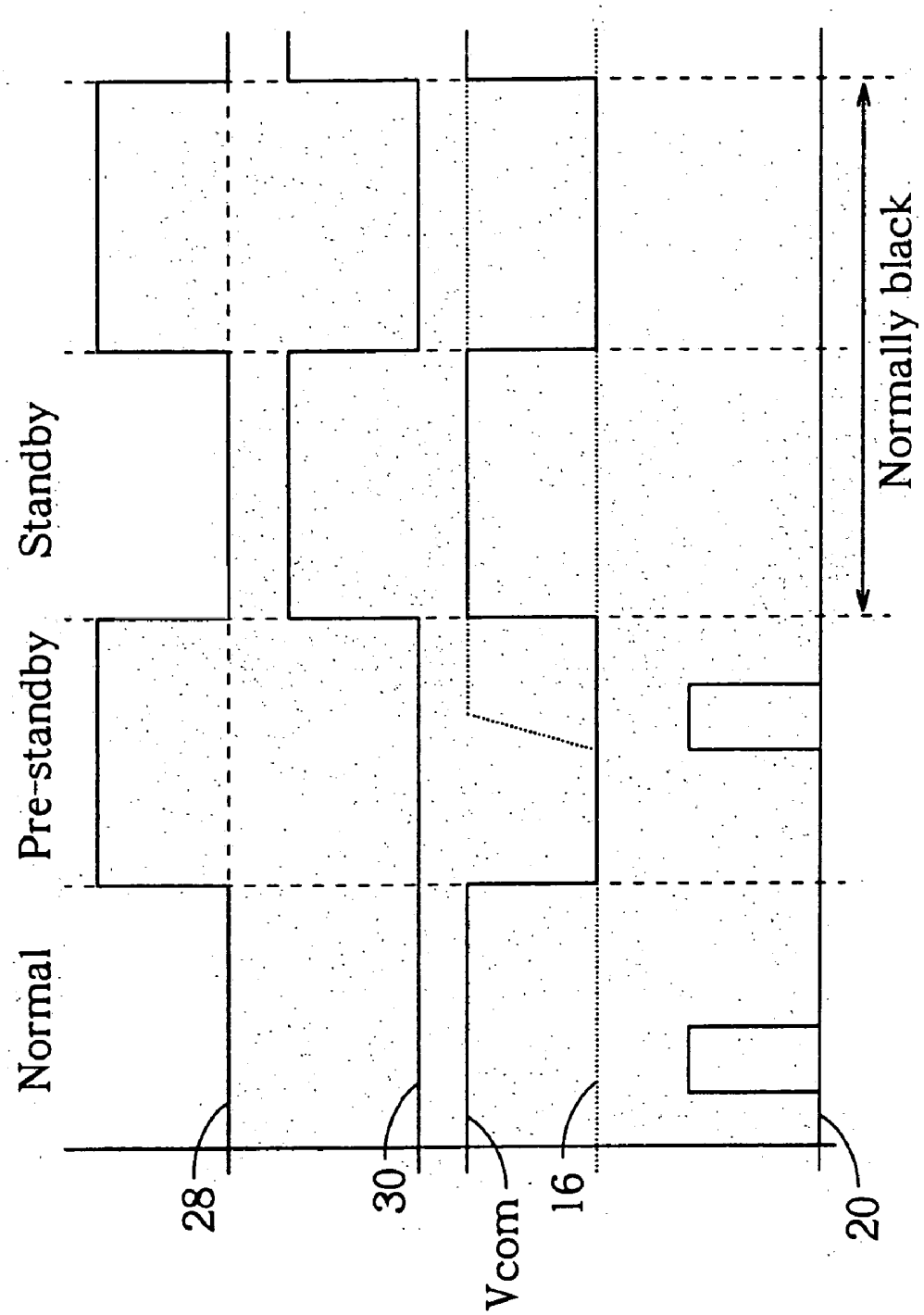


Fig. 2

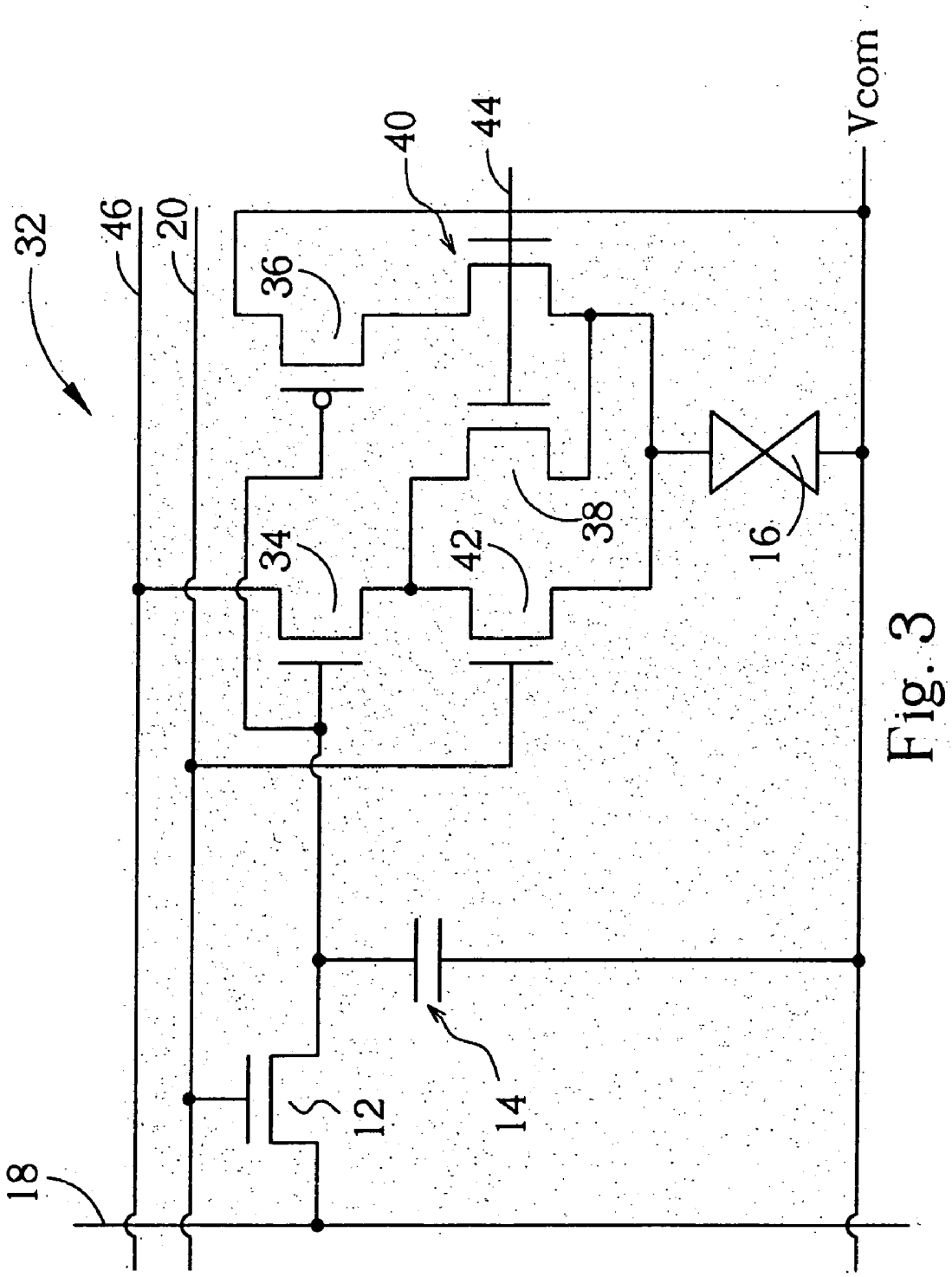


Fig. 3

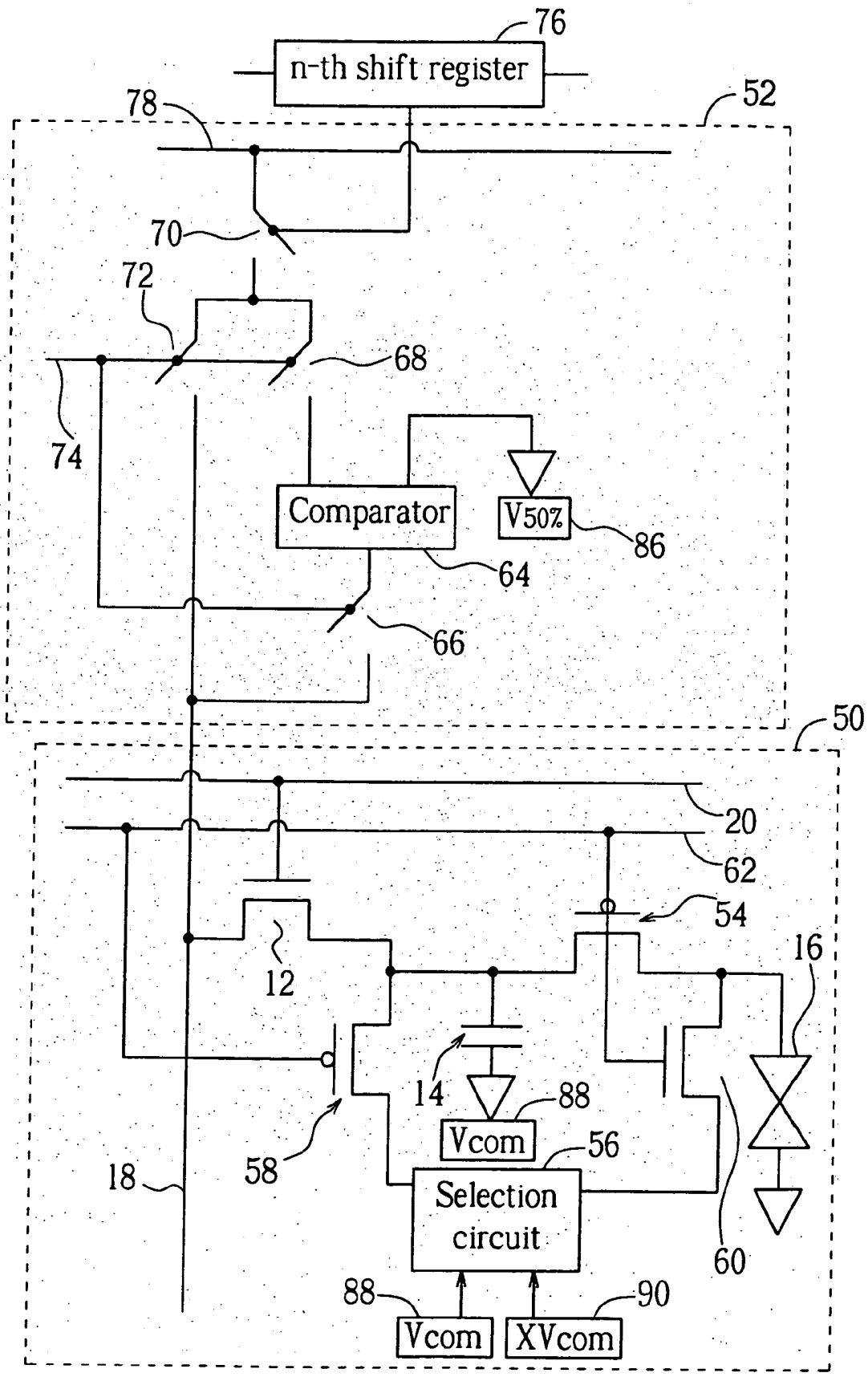

76
n-th shift register
78
52
70
72
68
74
Comparator
V50%
86
64
66
50
20
62
54
16
12
14
88
Vcom
56
58
18
Selection circuit
60
88
90
Vcom
XVcom

Fig. 4

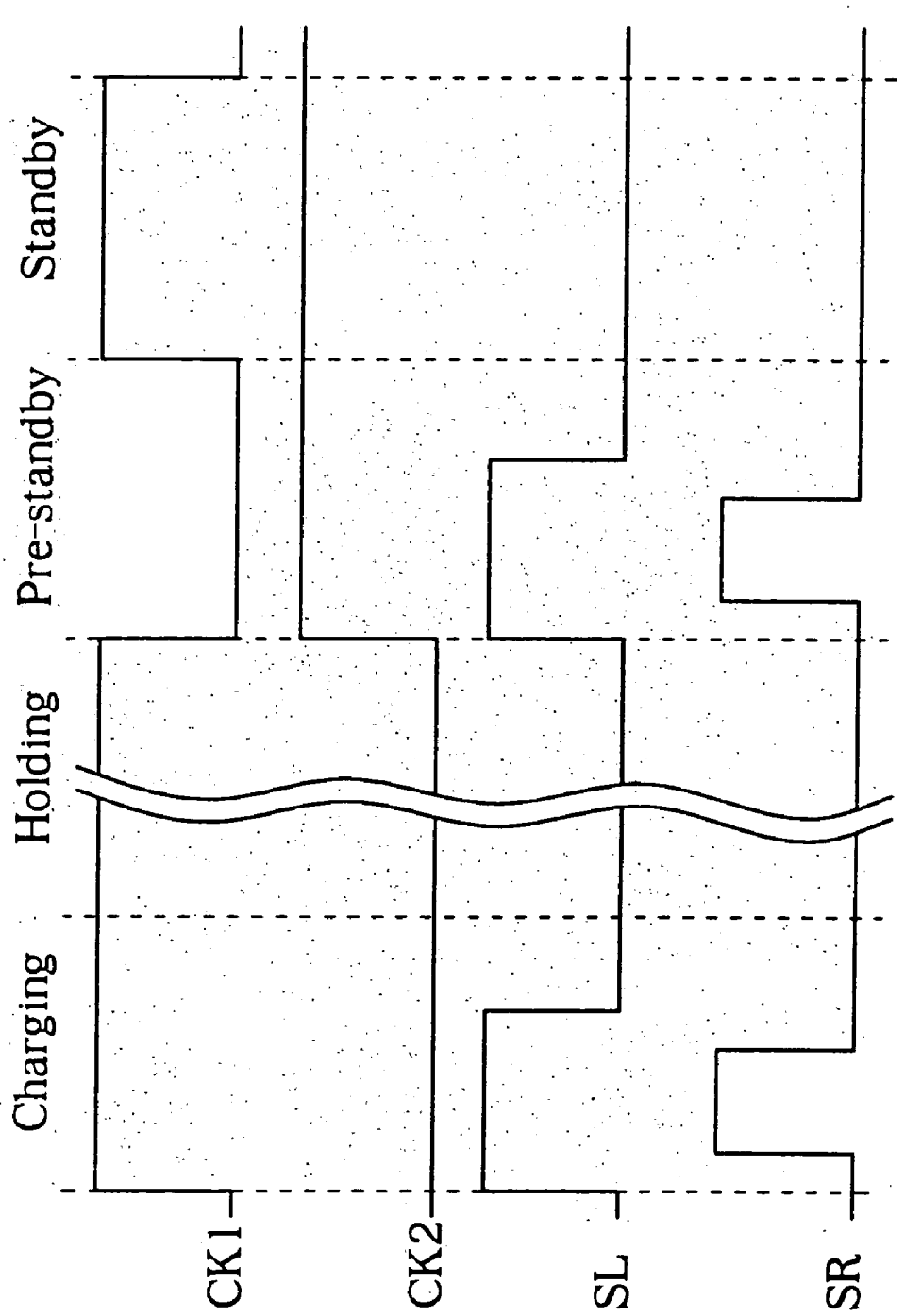
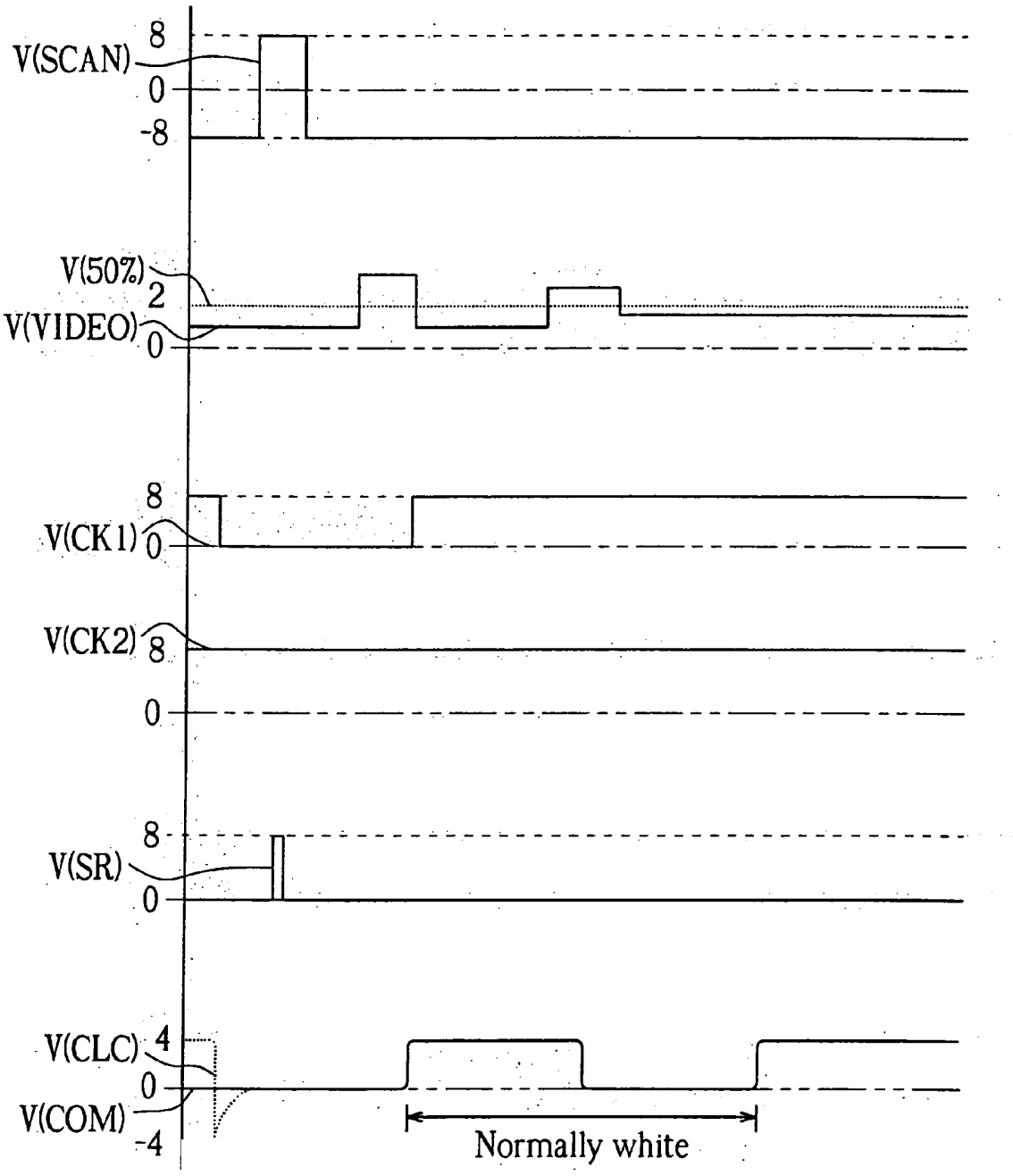


Fig. 5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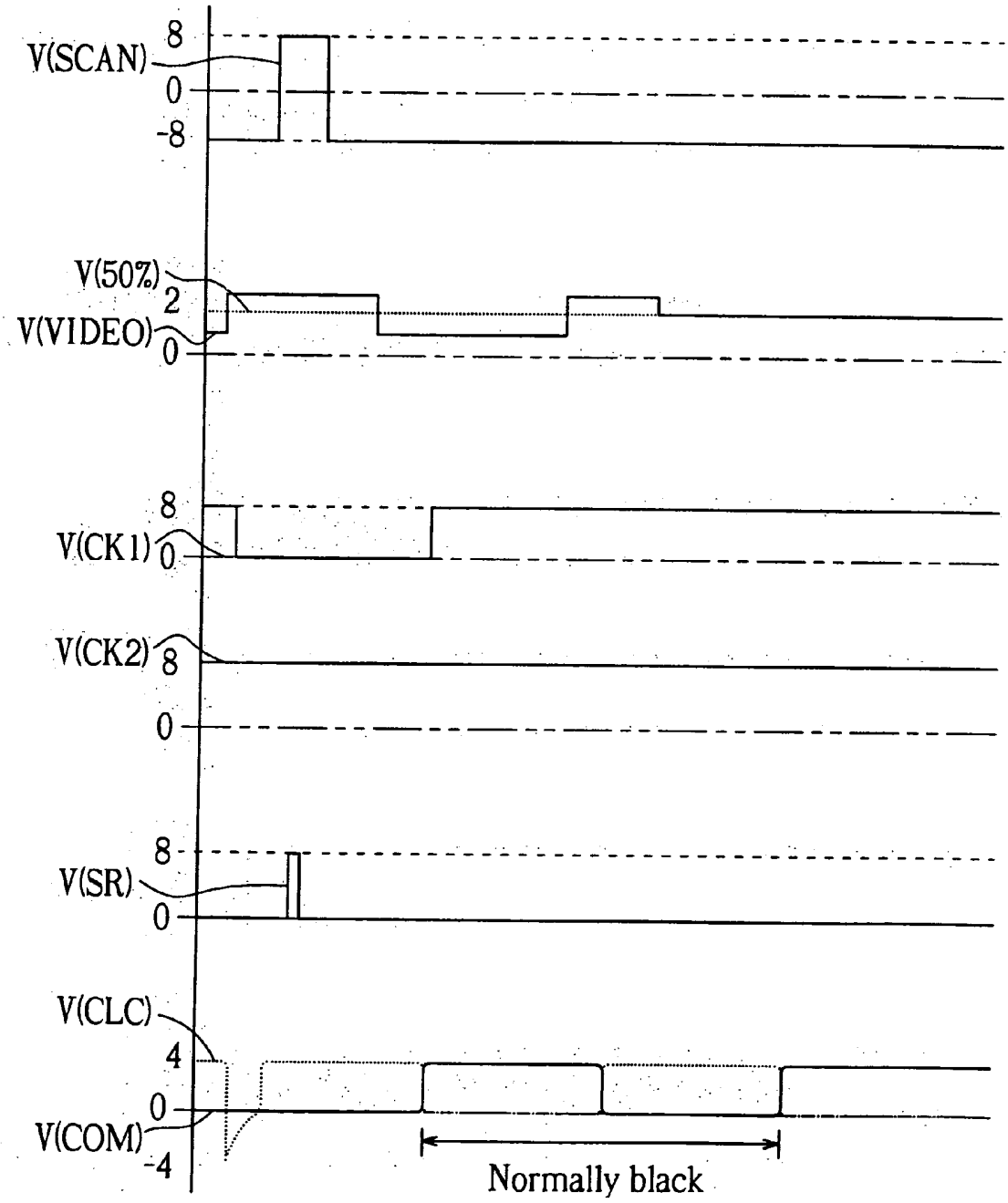
8
0
-8
V(50%)
2
V(VIDEO)
0
8
V(CK1)
0
V(CK2)
8
0
8
V(SR)
0
V(CLC)
4
0
V(COM)
-4
Normally white

Fig. 6


V(SCAN)
8
0
-8
V(50%)
2
V(VIDEO)
0
8
V(CK1)
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V(CK2)
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0
8
V(SR)
0
V(CLC)
4
0
V(COM)
-4
Normally black

Fig. 7

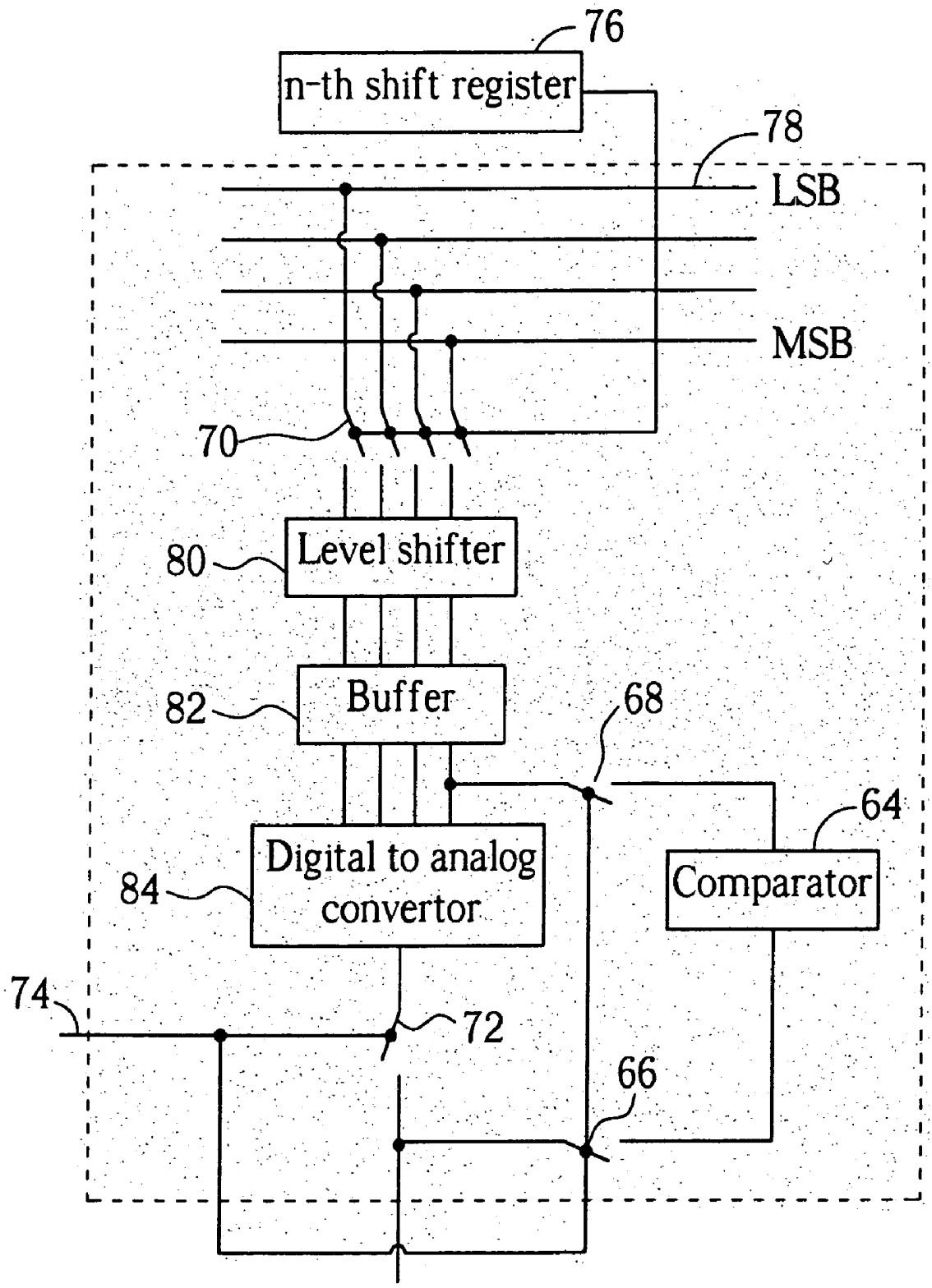
76
n-th shift register
78
LSB
MSB
70
80
Level shifter
82
Buffer
68
64
Digital to analog convertor
84
Comparator
74
72
66

Fig. 8

METHOD FOR REDUCING POWER CONSUMPTION OF AN LCD PANEL IN A STANDBY MODE

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display (LCD) panel, and more specifically, to a method of operation of a standby mode of an LCD panel.

[0003] 2. Description of the Prior Art

[0004] An LCD panel operating in a normal mode displays an image with high color, high contrast and high refresh rate, but consumes correspondingly high power.

[0005] Generally, the equation used in calculating the consumed power is: CV^2F+I_SV; where C is capacitance, V is voltage, F is frequency, and I_S is static current. The values of the capacitance and the voltage usually determine the size and resolution of the LCD panel, and the frequency determines the resolution and performance of a first switch. For reducing power consumption, the LCD panel displays a static image in low gray level via an circuit so that a lower voltage and frequency are transmitted in the data line.

[0006] Please refer to **FIG. 1** and **FIG. 2**. **FIG. 1** is a schematic diagram of an LCD panel pixel driver **10** with a digital memory **22** according to the prior art. **FIG. 1B** is a diagram of signals of the pixel driver **10**. In **FIG. 1**, the pixel driver **10** comprises a first switch **12**, a storage capacitor **14**, and a liquid crystal capacitor **16**. The signal of a scan line **20** turns on the first switch **12** so that the signal in the data line **18** is transmitted to the liquid crystal capacitor **16**. The storage capacitor **14** and liquid crystal capacitor **16** are connected in parallel for maintaining the voltage of liquid crystal capacitor **16**. Additionally the pixel driver **10** comprises a digital memory **22**. A first end of the pixel driver **10** is connected to a first end of liquid crystal capacitor **16**, and a second end of the pixel driver **10** is connected to the first end of the liquid crystal capacitor **16** through a third switch **24**. A second end of the liquid crystal capacitor **16** is connected to a common voltage V_{COM} that is an oscillating voltage. The second switch **24** and the third switch **26** are controlled by a first control line **28** and a second control line **30** respectively.

[0007] When the LCD panel operates in a normal mode, the first control line **28** turns off the second switch **24**, and the second control line **30** turns off the third switch **26**. The data in the data line **18** is transmitted to the liquid crystal capacitor **16** through the first switch **12**.

[0008] When the LCD panel operates in a standby mode, the data of the liquid crystal capacitor **16** is possibly a high voltage or a low voltage. **FIG. 2** is a schematic diagram showing the voltage of the liquid crystal capacitor **16** being a high voltage when the LCD panel operates in a standby mode. In **FIG. 2**, when the LCD panel operates in a pre-standby mode, the signal of the first control line **28** turns on the second switch **24** to transmit the high voltage stored in the liquid crystal capacitor **16** to the digital memory **22**. Then, when the LCD panel operates in standby mode, according to the oscillating cycle of the common voltage V_{COM}, the second switch **24** and the third switch **26** are turned on and off in turn to maintain a constant voltage difference is the liquid crystal capacitor **16** so that the LCD panel displays a black display. When the voltage stored in digital memory **22** in the pre-standby mode is a low voltage, according to the oscillating cycle of the common voltage V_{COM}, with the second switch **24** and the third switch **26** being turned on and off in turn, the voltage difference in the liquid crystal capacitor **16** is zero so that the LCD panel displays a white image. In addition, storing the voltage of the liquid crystal capacitor **16** in the digital memory **22** can temporarily stop output of the high-frequency voltage in the data line **18** for reducing power consumption.

[0009] Please refer to **FIG. 3**. **FIG. 3** is a schematic diagram of an LCD panel pixel driver **32** incorporating a dynamic memory **32** according to the prior art. In **FIG. 3**, the same elements of **FIG. 1** use the same symbols. In addition to the first switch **12**, the storage capacitor **14**, and the liquid crystal capacitor **16**, the pixel driver **32** further comprises a selection switch **34**, a complementary selection switch **36**, a first connection switch **38**, a second connection switch **40**, and an address switch **42**. When the LCD panel operates in the normal mode, the signal of the scan line **20** turns on the first switch **12** and the address switch **42**, and an updating signal line **44**, and turns off the first connection switch **38** and the second switch **40**, and further, inputs the signal in the data line **18** to the storage capacitor **14**. When the voltage stored in the storage capacitor **14** is a high voltage, the selection switch **34** is turned on to transmit the signal of a reference voltage line **46** to the liquid crystal capacitor **16**. When the voltage stored in the storage capacitor **14** is a low voltage, the selection switch **34** is turned off and the liquid crystal capacitor **16** maintains a constant voltage. The voltage of the liquid crystal capacitor **16** is controlled by the time that the first switch **12** and the address switch **42** are turned on by the scan line **20**.

[0010] When the LCD panel operates in the standby mode, the signal of the scan line **20** turns off the first switch **12** and the address switch **42**, and the signal of the updating signal line **44** turns on the first connection switch **38** and the second connection switch **40**. When the voltage stored in the storage capacitor **14** is a high voltage, the selection switch **34** is turned on and the complementary selection switch **36** is turned off, and the signal in the reference voltage line **46** is transmitted to the liquid crystal capacitor **16** through the first connection switch **38**. The LCD panel displays a black image. When the voltage stored in the storage capacitor **14** is a low voltage, the selection switch **34** is turned off and the complementary selection switch **36** is turned on, and the common voltage V_{COM} is transmitted to the liquid crystal capacitor **16** through the second connection switch **40**. The LCD panel displays a white image. Therefore, the storage capacitor **14** is identical to the dynamic memory element recording the voltage of the liquid crystal capacitor **16** when the LCD panel operates in a standby mode, and the high-frequency voltage in the data line is not transmitted for reducing power consumption.

[0011] When the LCD panel operates in a normal mode, higher voltage and frequency are transmitted in the data line **18** consuming more power. Therefore, after the LCD panel is operated in a standby mode, the transient voltage is recorded by the memory in the pixel driver so that the LCD panel displays a white or black image. However, when the pixel driver **10** in **FIG. 1** is combined with the digital memory **22**, the amount of transistors and signal lines

assembled in the pixel driver **10** is quite large so that the pixel driver **10** is only suitable for a reflective or half-reflective LCD panel. Additionally, the common voltage of the pixel driver **32** in **FIG. 3** is a non-oscillating signal that is not suitable for the purposes of reducing physical dimensions and power consumption.

SUMMARY OF INVENTION

[**0012**] It is therefore a primary objective of the claimed invention to provide a method for reducing power consumption of an LCD panel in a standby mode.

[**0013**] According to the claimed invention an LCD panel comprises a plurality of pixel drivers each comprising a liquid crystal capacitor, a storage capacitor, four switches; and a plurality of data drivers each comprising a shift register, a comparator, and a plurality of switches. The method includes the following steps: (a) transmitting data in a signal line to a data line, and turning on a second switch and turning off a forth switch to transmit data from the data line to the liquid crystal capacitor and the storage capacitor; and (b) transmitting the data in the signal line to the comparator, the comparator comparing the signal from the signal line and a reference voltage, outputting a corresponding control signal to a selection circuit of the pixel driver through the data line, and turning on the forth switch and turning off the second switch so that the selection circuit outputs a corresponding display signal to the liquid crystal capacitor according to the control signal.

[**0014**] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[**0015**] **FIG. 1** is a schematic diagram of an LCD panel pixel driver combined with a static according to the prior art.

[**0016**] **FIG. 2** is a diagram of signals of the pixel driver of **FIG. 1**.

[**0017**] **FIG. 3** is a schematic diagram of an LCD panel pixel driver combined with a dynamic memory according to the prior art.

[**0018**] **FIG. 4** is a schematic diagram of an LCD pixel driver and a data driver according to the present invention.

[**0019**] **FIG. 5** is a diagram of signals in the pixel driver of **FIG. 4**.

[**0020**] **FIG. 6** and **FIG. 7** are diagrams of voltages of the pixel driver and the data driver of **FIG. 4**.

[**0021**] **FIG. 8** is a schematic diagram of a second embodiment of a data driver according to the present invention.

DETAILED DESCRIPTION

[**0022**] Please refer to **FIG. 4**. **FIG. 4** is a schematic diagram of an LCD panel pixel driver **50** and a corresponding data driver **52** according to the present invention. A liquid crystal capacitor **16** is connected between a storage capacitor **14** and a data line **18**. The pixel driver **50** also comprises a selection circuit **56**, the input end of the selection circuit **56** being connected to the storage capacitor **14** and the output end of the selection circuit **56** being connected to the liquid crystal capacitor **16** through a forth switch **60**. The pixel driver **50** also includes a scan line **20** to control a first switch **12** and a second clock **62** to control a second switch **54**, a third switch **58**, and a forth switch **60**. The second switch **54** and the forth switch **60** are complementary switches. When the second switch **54** is turned on, the forth switch **60** is turned off, and when the second switch **54** is turned off, the forth switch **60** is turned on.

[**0023**] Additionally, the ground ends of the storage capacitor **14** and the liquid crystal capacitor **16** are connected to the common voltage V_{COM}, and the common voltage V_{COM} can be a constant level signal or an oscillating signal. In this embodiment, the oscillating signal is used as the common voltage V_{COM} for illustration.

[**0024**] The data driver **52** of the present invention includes a comparator **64**. The output end of the comparator **64** is connected to the data line through a seventh switch **66**, and the input end of the comparator **64** is connected to a fifth switch **70** through an eighth switch **68**. The data line **18** is connected to the fifth switch **70** through a sixth switch **72**. The data driver **52** also includes a first clock **74** to control the sixth switch **72**, the seventh switch **66**, and the eighth switch **68**. The sixth switch **72** and the eighth switch **68** are complementary switches, and the seventh switch **66** and the eighth switch **68** are turned on and off simultaneously. The LCD panel of the present invention also includes a shift register **76** to control the fifth switch **70**, which is connected to a video line **78**. When the fifth switch **70** is turned on, the data in the video line **78** is transmitted to the data line **18** or the comparator **64** according to the signal of the first clock **74**. Additionally, the comparator **64** and the selection circuit **56** in **FIG. 4** can have any kind of circuit structures provided that they perform as described. Also, the number of transistors used in the selection circuit **56** should be decreased when the pixel driver **50** is used in a transmission LCD panel application.

[**0025**] When the LCD panel operates in a normal mode, the seventh switch **66**, and the eighth switch **68** of the data driver **52** are turned off; the sixth switch **72**, the first switch **12** and the second switch **54** of the pixel driver **50** are turned on; and the third switch **58** and the forth switch **60** of the pixel driver **50** are turned off. When the fifth switch **70** is turned on, the data of the video line **78** is transmitted to the data line **18** through the sixth switch **72**, and the data line **18** charges the storage capacitor **14** and the liquid crystal capacitor **16** through the first switch **12**. Before the LCD panel operates in a power-saving mode, the LCD panel first operates in a pre-standby mode. The first switch **12**, the third switch **58**, and the forth switch **60** of the data driver **50** are turned on, and the second switch **54** is turned off. When the fifth switch **70** is turned on, the data of the video line **78** is transmitted to the comparator **64** through the eighth switch **68**. The comparator **64** compares the data of the video line **78** and a reference voltage $V_{50\%}$ **86** to output a control signal to data line **18** through the seventh switch **66**, and then the control signal is transmitted to the selection circuit **56** and storage capacitor **14** through the first switch **12** and the third switch **58**. The selection circuit **56** outputs a corresponding display signal to the liquid crystal capacitor **16** through the forth switch **60** according to the control signal. The reference voltage $V_{50\%}$ **86** is a 50% transmission pixel voltage. When the voltage of the video line **78** is higher than the

reference voltage $V_{50\%}$ **86**, the selection circuit **56** outputs an inverted common voltage XV_{COM} **90** to maintain a high voltage between the liquid crystal capacitor **16** according to the control signal to control the LCD panel to display a black image. The inverted common voltage XV_{COM} **90** and the common voltage V_{COM} **88** are complementary signals. In other words, when the voltage of the video line **78** is lower than the common voltage $V_{50\%}$ **86**, the selection circuit **56** outputs the common voltage V_{COM} **88** to maintain a low voltage in the liquid crystal capacitor **16** to control the LCD panel to display a white image. And then, the LCD panel operates in a standby mode. The voltage XV_{COM} or V_{COM} determined by the selection circuit **56** is transmitted to the liquid crystal capacitor **16** until the data driver **52** and the scan driver are turned on and the second clock CK2 is lower than a low-voltage, so that the LCD panel operates in a normal mode.

[**0026**] Please refer to **FIG. 5**. **FIG. 5** is a diagram of signals of the pixel driver **50** and the data driver **52**. As shown in **FIG. 5**, CK1 is the signal of the first clock **74**, CK2 is the signal of the second clock **62**, SL is the signal of the scan line **20**, and SR is the signal of the shift register **76**. When the LCD panel operates in a normal mode, there are two steps performed, namely a charging stage and a holding stage. In the charging stage, the first clock **74** turns on the sixth switch **72**, and turns off the seventh switch **66** and the eighth switch **68**; the second clock **62** turns on the second switch **54**, and turns off the third switch **58** and the forth switch **60**; the scan line turns on the first switch **12**; and the shift register **76** turns on the fifth switch **70** for a period to transmit the data of the video line **78** to the storage capacitor **14** and the liquid crystal capacitor **16** through the data line **18**. In the holding stage, the first clock **74** and the second clock **62** hold the same state, the scan line **20** turns off the first switch **12**, and the storage capacitor **14** maintains the voltage of the liquid crystal capacitor **16**.

[**0027**] There are two stages when the LCD panel operates in a power-saving mode, the pre-standby stage and the standby stage. In the pre-standby stage, the first clock **74** turns off the sixth switch **72**, and turns on the seventh switch **66** and the eighth switch **68**; the second clock **62** turns off the second switch **54**, and turns on the third switch **58** and the forth switch **60** when Vcom is required at the low voltage. When the scan line **20** turns on the first switch **12**, the shift register **76** turns on the fifth switch **70** for a period to transmit the data of the video line **78** to the comparator **64**, and the comparator **64** compares the data of the video line **78** and the reference voltage $V_{50\%}$ **86** and outputs the control signal to the selection circuit **56** and storage capacitor **14** according to the comparison result. And, the first clock **74** turns on the sixth switch **72** and turns off the seventh switch **66** and the eighth switch **68** to identify the result that the comparator **64** outputs. The state of the second clock **62** is held the same. When the voltage of the video line **78** is higher than the reference voltage $V_{50\%}$ **86**, the control signal is a high voltage and the selection circuit outputs the inverted common voltage XV_{COM} **90** to the liquid crystal capacitor **16**. When the voltage of video line **78** is lower than the reference voltage $V_{50\%}$ **86**, the control signal is a low voltage and the selection circuit **56** outputs a common voltage V_{COM} **88** to the liquid crystal capacitor **16**. At this time, the data driver **52**, shift register **76** and the scan driver could be turned off. In the standby stage, the voltage XV_{COM} or V_{COM} determined by the selection circuit **56** is transmitted to the liquid crystal capacitor **16** until the data driver **52** and scan driver are turned on. The scan driver restarts scanning and the second clock signal CK2 is lowered to a low voltage, and the LCD operates in the normal mode.

[**0028**] Please refer to **FIG. 6** and **FIG. 7**. **FIG. 6** and **FIG. 7** are diagrams of voltages of the pixel driver **50** and the data driver **52** in **FIG. 4** during operation. V(SCAN) is the voltage of the scan line **20**, V(VIDEO) is the voltage of the video line **78**, V(50%) is the reference voltage $V_{50\%}$ **86**, V(CK1)is the voltage of the first clock **74**, V(CK2) is the voltage of the second clock **62**, V(COM) is the voltage of common voltage V_{COM} **88**, and V(CLC) is the voltage of the liquid crystal capacitor **16**. When the LCD panel operates in the power-saving mode, the LCD panel first enters into the pre-standby stage. The low voltage of the first clock **74** turns off the sixth switch **72**, and turns on the seventh switch **66** and the eighth switch **68**; the high voltage of the second clock **62** turns off the second switch **54**, and turns on the third switch **58** and the forth switch **60**. When the voltage of the scan line **20** is raised to a high voltage to turn on the first switch **12**, the shift register **76** is raised to a high voltage to turn on the fifth switch **70** and transmit the voltage of the video line **78** to the comparator **64**. The comparator **64** compares the voltage of the video line **78** and the reference voltage $V_{50\%}$ **86**, outputs the control signal to the data line **18**, and transmits the control signal to the selection circuit **56** through the first switch **12** and the third switch **58**. The shift register **76** and the scan line **20** are lowered to a low voltage in turn to turn off the fifth switch **70** and the first switch **12**. When the selection circuit **56** receives the control signal that the comparator **64** has outputted, the voltage of the first clock **74** is raised to a high voltage turning on the sixth switch **72**, and turning off the seventh switch **66** and the eighth switch **68**. And then, the LCD panel operates in the standby mode. Referring to V(CLC) and V(COM) shown in the **FIG. 6**, when the voltage of the video line **78** is lower than the voltage $V_{50\%}$ **86**, the selection circuit **56** outputs the common voltage V_{COM} **88** to the liquid crystal capacitor **16**, the voltage difference in the liquid crystal capacitor **16** is zero, and the LCD panel displays a white image. Referring to V(CLC) and V(COM) shown in **FIG. 7**, when the voltage of video line **78** is higher than the reference voltage $V_{50\%}$ **86**, the selection circuit **56** outputs the inverted common voltage XV_{COM} **90** to the liquid crystal capacitor **16**, the voltage difference between the liquid crystal capacitor **16** is 4V, and the LCD panel displays a black image.

[**0029**] Please refer to **FIG. 8**. **FIG. 8** is a schematic diagram of a data driver according to a second embodiment of the present invention. When the data in the data line is digital, a level shifter **80**, a buffer **82**, and a digital-to-analog converter (DAC) **84** are disposed between the fifth switch **70** and the sixth switch **72**. Before being transmitted to the data line **18**, the digital data is regulated by the level shifter **80**, and the data is stored in buffer **82**. When the LCD panel operates in the normal mode, the first clock **74** turns on the sixth switch **72** and turns off the seventh switch **66** and the eighth switch **68**, and the data stored in buffer **82** is transmitted to the DAC **84** and transformed into a signal capable of charging the storage capacitor **14** and the liquid crystal capacitor **16** through the first switch **12**. When the LCD panel operates in the standby mode, the first clock **74** turns off the sixth switch **72** and turns on the seventh switch **66** and the eighth switch **68**. The MSB stored in the buffer **82** is transmitted to the comparator **64** as a digital signal

through the eighth switch **68**, and the comparator **64** compares the MSB and the reference voltage $V_{50\%}$ **86** and outputs the control signal to the data line **18** through the seventh switch **66**. The other operation process is the same as the process described referencing **FIG. 4** and is not repeated.

[**0030**] From the above description, a pixel driver is combined with the second switch **54**, the third switch **58**, the forth switch **60**, and the selection circuit **56**. In addition, the data driver **52** is combined with the comparator **64**. For turning on and off the second switch **54**, the third switch **58**, and the forth switch **60**, the pixel driver **50** of the present invention operates in a normal mode the same way the prior art pixel driver does. When the LCD panel operates in the pre-standby mode, the comparator **64** in the data driver **52** compares the voltage of the video line **78** and the reference voltage $V_{50\%}$ **86**, and outputs the control signal to the selection circuit **56** according to the comparison result. The selection circuit **56** then outputs the corresponding voltage to the liquid crystal capacitor **16** according to the control signal and controls the voltage of the liquid crystal capacitor **16**, being a high voltage or a low voltage, to control the LCD panel to display a white or black image. This further stops transmitting the high-frequency signal of the video line **78**, and turns off the data driver and the scan driver for reduced power consumption.

[**0031**] Compared with the prior art, the pixel driver **50** of the invention operating in the normal mode transmits the data in the video line **78** to the data line **18**, and charges the storage capacitor **14** and the liquid crystal capacitor **16** directly through the first switch **12**. Structurally, the pixel driver of the present invention is much the same as the conventional pixel driver. In addition, the conventional pixel driver **32** combined with the dynamic memory in the prior art uses a pulse width of time that the first switch **12** turns on to control the voltage of the storage capacitor **14**. The charge time of the liquid crystal capacitor **16** is determined by the voltage of the storage capacitor **14**. And, the liquid crystal capacitor **16** is not directly charged by the data line **18** so that there are may be some problems in operation. Additionally, an inverted or non-inverted common voltage V_{COM} is suitable for the pixel driver **50** in the present invention. When the common voltage V_{COM} is inverted, the peak voltage is smaller and the power consumption is reduced. The common voltage V_{COM} of the pixel driver **32** combined with the dynamic memory in the prior art is non-inverted, and is thus not suitable for power-saving and size reduction. Additionally, when the pixel driver **50** of the present invention operates in the standby mode, the number of transistor used in the selection circuit **56** for reducing power consumption is less than the number used in the pixel driver **32** combined with the dynamic memory in the prior art. When the comparator **64** is assembled in the driver circuit **52**, the number of transistor used in the pixel driver **50** in the invention can be decreased so that the pixel driver **50** is not only suitable for a reflective LCD panel or a half-reflective LCD panel, but it is also suitable for a transmission LCD panel.

[**0032**] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be constructed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A method for reducing power consumption of an LCD panel in a standby mode, the LCD panel comprising a plurality of pixel drivers and a plurality of data drivers, each pixel driver comprising:

a liquid crystal capacitor;

a storage capacitor connected to a data line and connected to the liquid crystal capacitor through a second switch; and

a selection circuit having an input end connected to the data line and an output end connected to the liquid crystal capacitor through a fourth switch;

each data driver comprising:

a comparator for comparing data from a video line with a reference voltage and outputting a corresponding control signal;

the method comprising:

(a) transmitting data of the video line to the data line, turning on the second switch and turning off the fourth switch to transmit the data from the data line to the liquid crystal capacitor and the storage capacitor; and

(b) transmitting data from the video line to the comparator and using the comparator to compare the data with the reference voltage, then transmitting a corresponding control signal outputted from the comparator to the selection circuit through the data line, and turning on the fourth switch and turning off the second switch so that the selection circuit outputs a corresponding display signal to the liquid crystal capacitor according to the control signal.

2. The method of claim 1 wherein the LCD panel further comprises a shift register, and the method further comprises using the shift register to control a fifth switch to transmit the data from the video line to the data line or to the comparator.

3. The method of claim 2 wherein the data driver further comprises a sixth switch connected between the fifth switch and the data line, and a seventh switch connected between the comparator and the data line; the method further comprising in step (a), the shift register turns on the fifth switch and a first clock turns on the sixth switch and turns off the seventh switch to transmit the data from the video line to the data line, and in step (b), the shift register turns on the fifth switch and the first clock turns off the sixth switch and turns on the seventh switch to output the control signal from the comparator to the data line.

4. The method of claim 3 wherein the data driver further comprises a level shifter connected to the fifth switch for adjusting a level of the data from the video line, a buffer connected to the level shifter for storing the data being output from the level shifter, and a digital to analog converter (DAC) connected between the buffer and the sixth switch for converting the digital data stored in the buffer to an analog signal, an input end of the comparator connected to an output end of the buffer.

5. The method of claim 1 wherein the pixel driver further comprises a first switch connected between the data line and the storage capacitor, the first switch being turned on by a scan line in step (a) and step (b); and a third switch

connected between the storage capacitor and the selection circuit, the third switch turning on and off at the same time as the fourth switch.

6. The method of claim 1 wherein in the step (b), when the voltage of the storage capacitor is higher than the reference voltage, the selection circuit outputs a black display signal to the liquid crystal capacitor; and when the voltage of the storage capacitor is lower than the reference voltage, the selection circuit outputs a white display signal to the liquid crystal capacitor.

7. The method of claim 1 wherein the reference voltage is a pixel voltage of approximately 50% light transmission.

8. The method of claim 1 wherein the storage capacitor and the liquid crystal capacitor are connected to a common voltage.

9. The method of claim 8 wherein the common voltage is an oscillating signal or a constant level signal.

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专利名称(译)	在待机模式下降低LCD面板的功耗的方法		
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摘要(译)

一种用于在待机模式下降低LCD面板的功耗的方法。 LCD面板包括多个像素驱动器和多个数据驱动器。每个像素驱动器具有液晶电容器，存储电容器，选择电路和四个开关。每个数据驱动器都有一个移位寄存器，一个比较器和几个开关。该方法包括将数据从信号线传输到比较器并将数据与参考电压进行比较，然后通过数据线将从比较器输出的相应控制信号传输到选择电路，选择电路输出相应的显示信号给液晶电容器根据控制信号。