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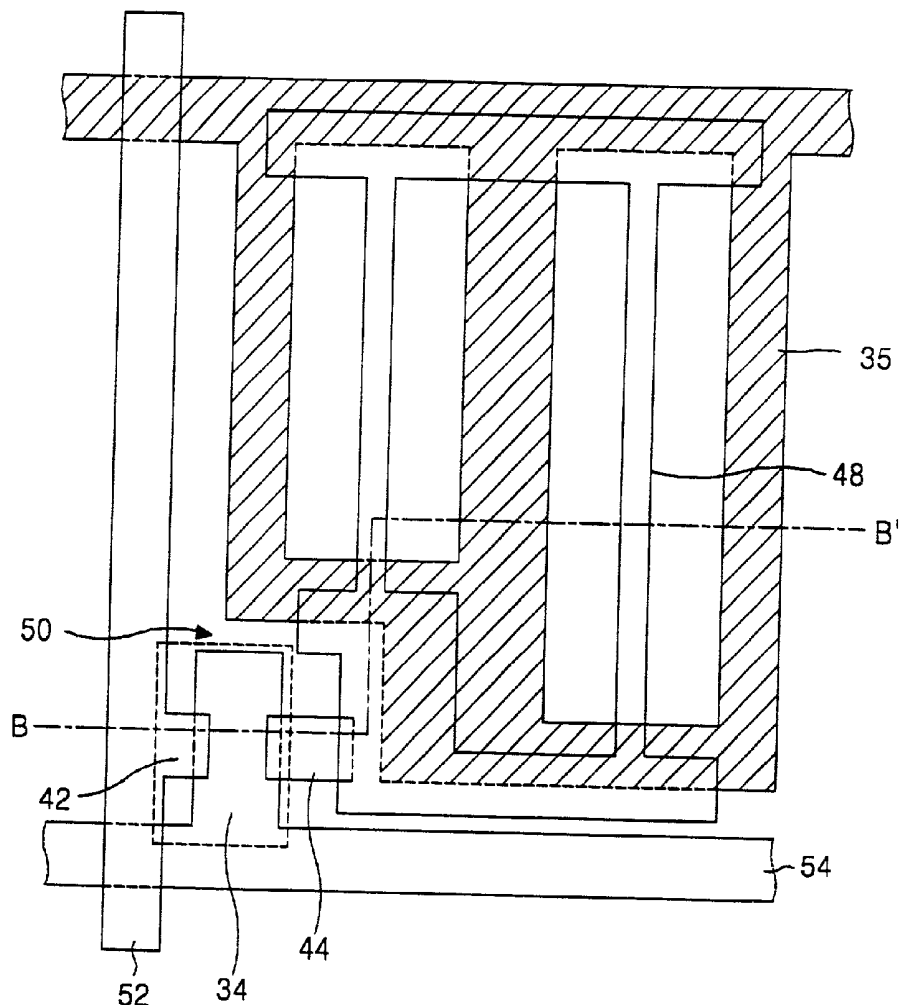


FIG. 1
CONVENTIONAL ART

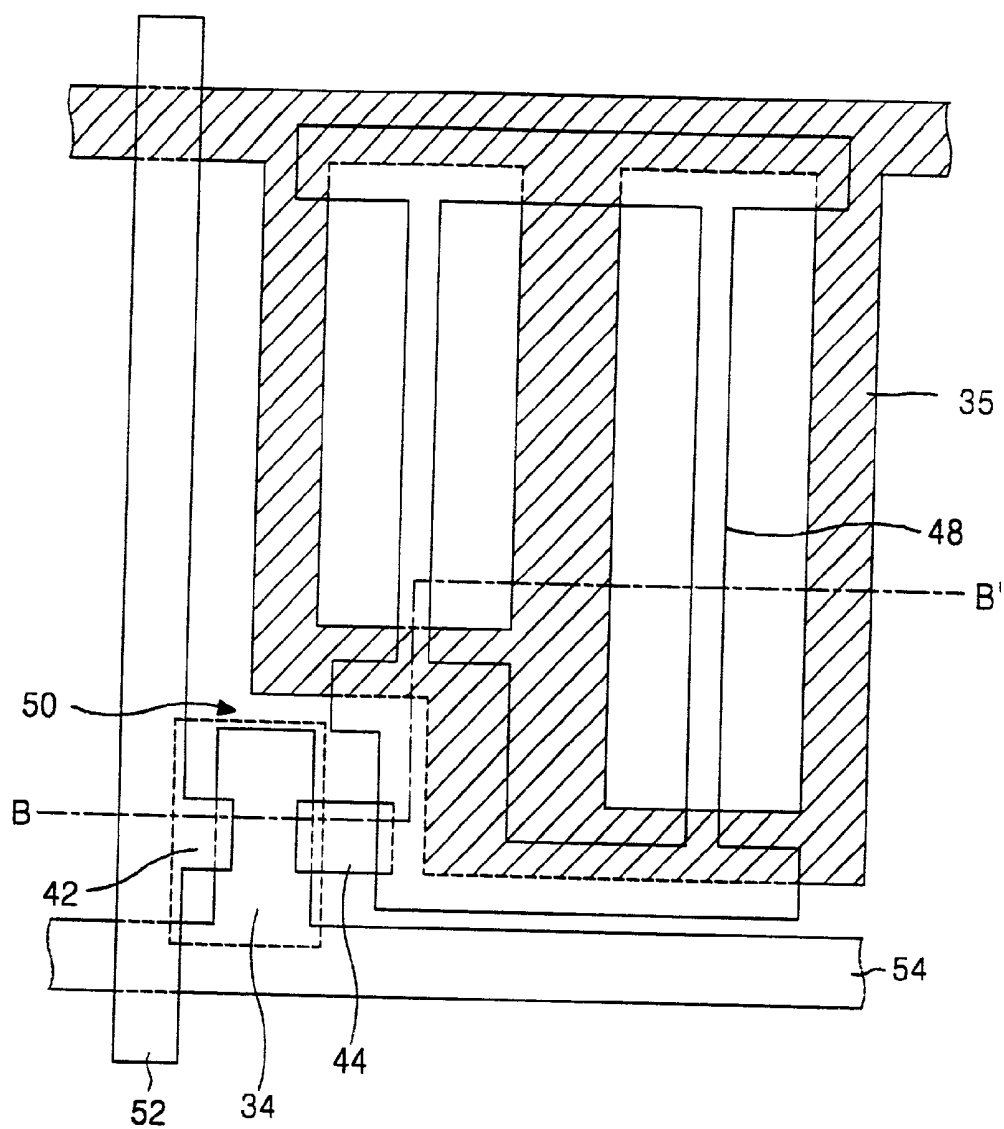


FIG. 2
CONVENTIONAL ART

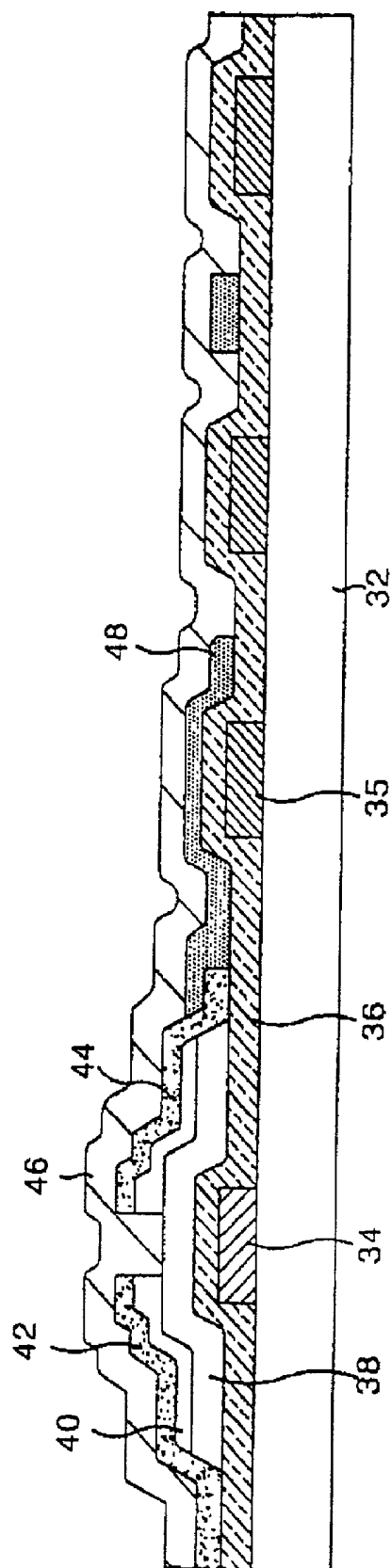


FIG. 4
CONVENTIONAL ART

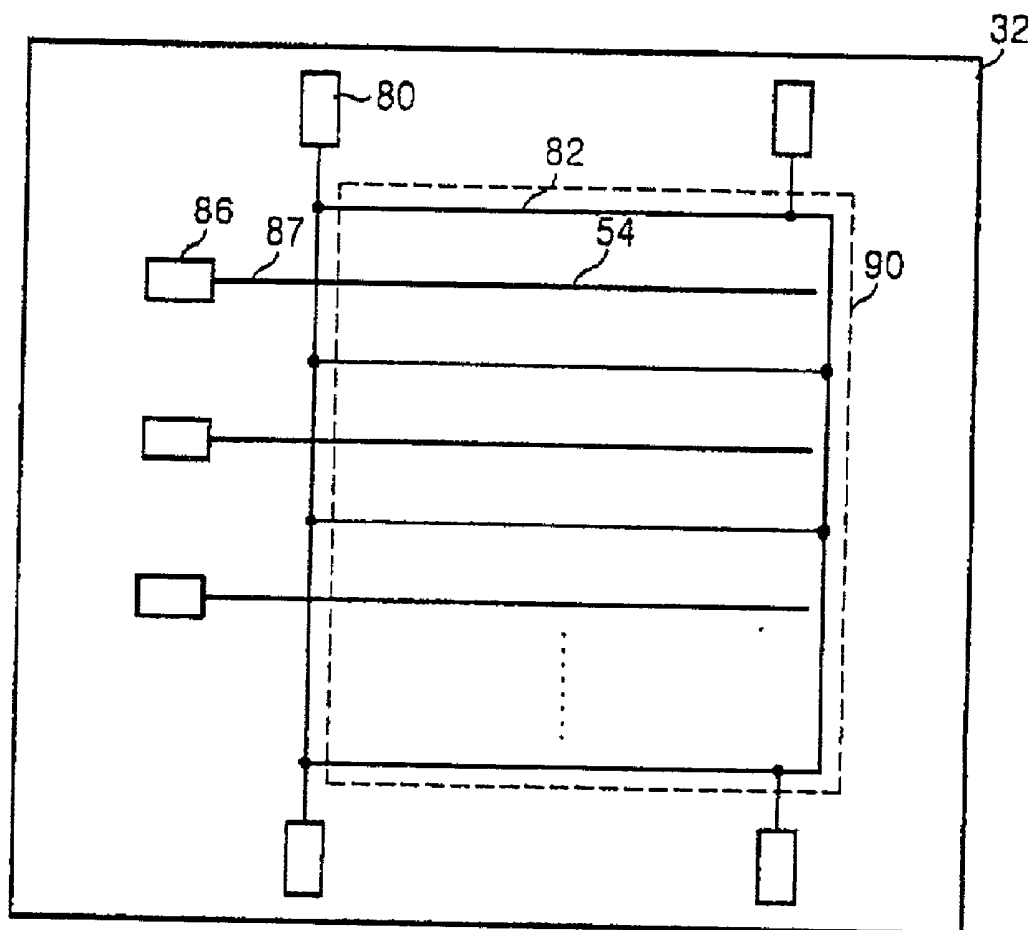


FIG. 5

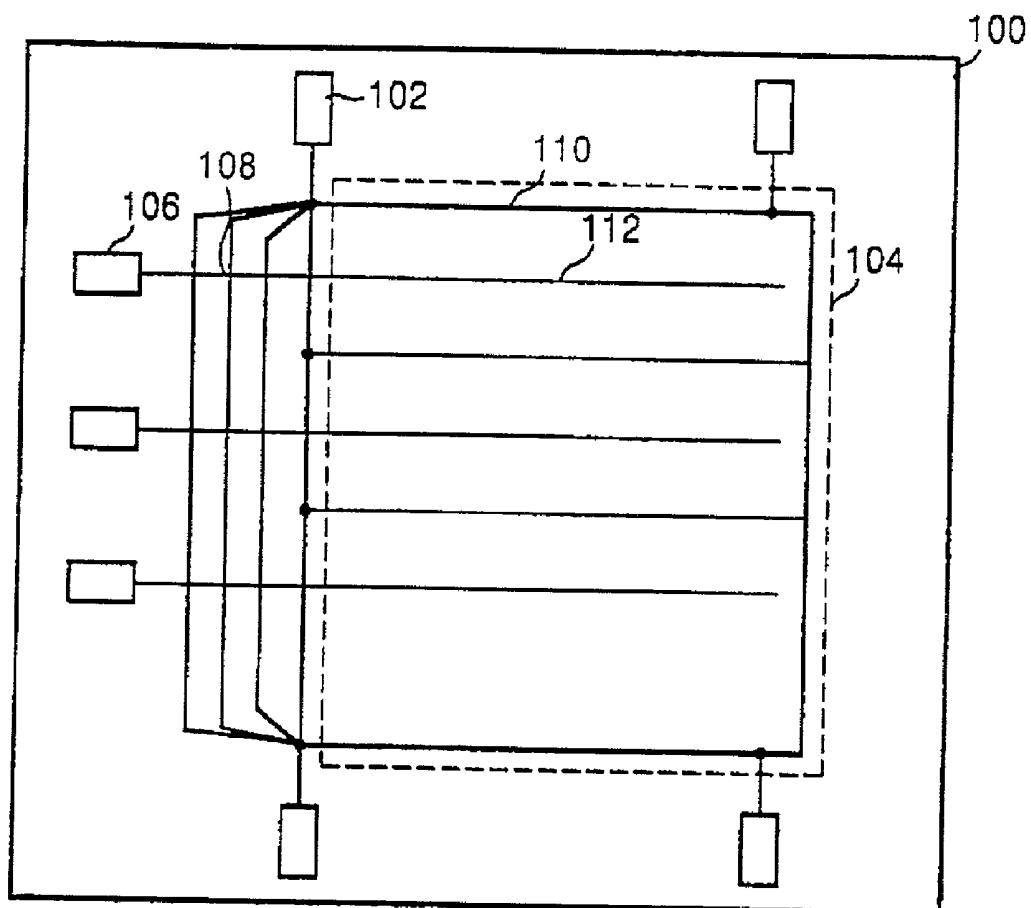
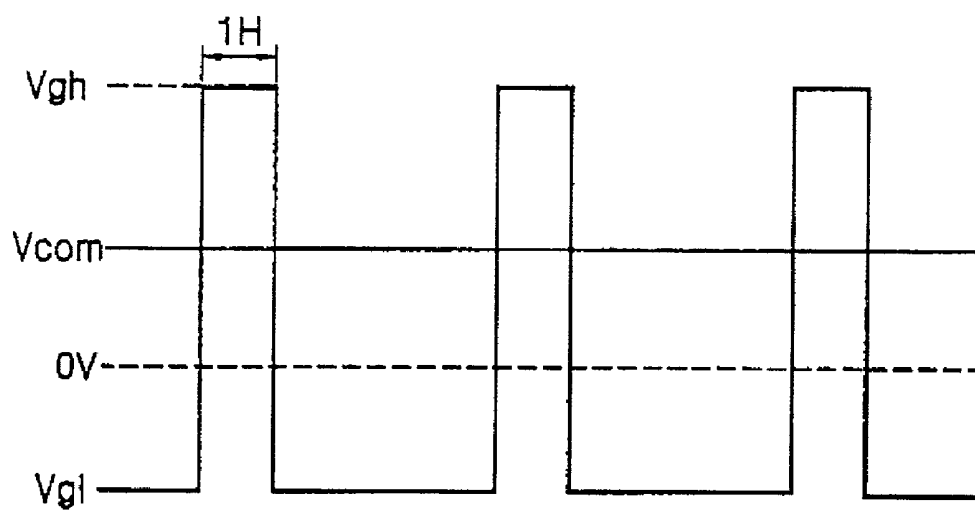


FIG. 6



IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

[0001] This application claims the benefit of Korean Patent Application No. P00-55034, filed on Sep. 19, 2000, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to a liquid crystal display device, and more particularly to a liquid crystal display device that is capable of eliminating a stain generated at an outer area of a thin film transistor array using an in-plane switching mode.

[0004] 2. Discussion of the Related Art

[0005] Generally, a liquid crystal display of active matrix driving system uses thin film transistors (TFTs) as switching devices to display a natural moving picture. Since such a liquid crystal display can be made into a device that is smaller than a cathode ray tube ("CRT"), it is commercially available for use in monitors such as portable televisions, notebook personal computers and laptop personal computers, etc.

[0006] The active matrix liquid crystal display (LCD) displays a picture corresponding to video signals, such as television signals, on a pixel (or picture element) matrix having pixels arranged at each crossing of gate lines and data lines. Each pixel includes a liquid crystal cell for controlling transmitted light in accordance with a voltage level of a data signal from a data line. The TFT is installed at the crossing point of the gate line and the data line to switch a data signal to be transferred to the liquid crystal cell in response to a scanning signal (i.e., a gate pulse) from the gate line.

[0007] Such a liquid crystal display can be largely classified as twisted nematic (TN) mode, in which a vertical electric field is applied, and an in-plane switching (IPS) mode, in which a horizontal electric field is applied to have a wide viewing angle. How an LCD is classified depends on the direction of an electric field driving the liquid crystal.

[0008] The IPS mode LCD has an advantage over the TN mode LCD in that, in an IPS mode LCD, a liquid crystal within a pixel area is rotated in the horizontal direction by a horizontal electric field to have a wide viewing angle.

[0009] Referring to FIG. 1, the IPS mode LCD includes a TFT 50 provided at a crossing of a data line 52 and a gate line 54, pixel electrodes 48 arranged in a matrix in a cell area between the data line 52 and the gate line 54, and a common electrode 35 formed in parallel to the pixel electrodes 48 in the pixel area. As shown in FIG. 2, the TFT 50 is provided on a rear substrate 32. The TFT 50 includes a gate electrode 34 connected to the gate line 54, a source electrode 42 connected to the data line 52, a drain electrode 44 connected to the pixel electrode 48, and an active layer 38 defining a channel between the source electrode 42 and the drain electrode 44.

[0010] The gate electrode 34, the gate line 54 and the common electrode 35 are formed by depositing a metal such as chrome (Cr), etc. on the rear substrate 32 and then patterning it. Herein, the common electrode 35 is patterned

into a plurality of strips within the pixel area. A gate insulating film 36 made from an inorganic dielectric material such as SiN_x , etc. is entirely deposited on the rear substrate 32 provided with the gate electrode 34, the gate line 54 and the common electrode 35. Semiconductor layers consisting of the active layer 38 made from amorphous silicon (a-Si) and an ohmic contact layer 40 made from a-Si doped with n+ ions are disposed sequentially on the gate insulating film 36. Then, the source electrode 42, the drain electrode 44 and the data line 52 made from a metal material are provided to cover the semiconductor layers 38 and 40. In this case, the source electrode 42 and the drain electrode 44 are patterned in such a manner to be spaced by a predetermined channel width from each other. Thereafter, indium-tin-oxide (ITO) is deposited and then patterned to form the pixel electrode 48. Herein, the pixel electrode 48 is connected to the drain electrode 44 and is patterned into a plurality of strips that partially overlap and alternate with the common electrode 35 within the pixel area. Subsequently, an ohmic contact layer 40 is etched along a channel defined between the source electrode 42 and the drain electrode 44 to expose the active layer 38. A protective film 46 made from SiN_x or SiO_x , etc. is entirely deposited on the rear substrate 32 to cover and thus protect the TFT 50 and the pixel electrode 48.

[0011] As shown in FIG. 3, the rear substrate 32, which is provided with the TFT array, is opposed to a front substrate 72, which is provided with black matrices 74 and color filters 76. A liquid crystal layer 78 is interposed between the rear and front substrates 32 and 72. The pixel electrode 48 and the common electrode 35 oppose each other horizontally. When a gate high pulse is applied to the gate electrode 34 of the TFT 50, an electric field corresponding to a difference voltage between a data voltage and a common voltage is applied between the pixel electrode 48 and the common electrode 35. During a scanning period, a channel is defined between the source electrode 42 and the drain electrode 44. Liquid crystal molecules in the liquid crystal layer 78 are driven with the horizontal electric field to control a quantity of transmitted light inputted from a back light.

[0012] Referring to FIG. 4, common lines 82 are formed on the rear substrate 32 in parallel to the gate lines 54. The common lines 82 commonly apply a common voltage from an external driver to the common electrode 35 within a TFT array 90. The common voltage lines 82 within the TFT array 90 are formed at an outer area adjacent to the TFT array 90 and are connected, via common voltage pads 80, to the external driver. The gate line 54 is connected, via the gate pad 86 and a gate link 87, to the external driver. The gate link 87, formed at the outer area of the TFT array 90, connects the gate line 54 to the gate pad 86 to deliver a gate voltage from the external driver to the TFT array 90. Further, data pads, data links and data lines (not shown) for delivering a data voltage to the TFT array 90 are provided on the rear substrate 32.

[0013] Referring again to FIG. 3, a liquid crystal 78 is injected between the rear substrate 32 and the front substrate 72 over the TFT array area, the gate pad area and the gate link area. In this case, the liquid crystal at the gate pad area and the gate link area is coupled with only a gate voltage applied to the gate link 87, via the gate pad 86 upon driving of the LCD to thereby cause deterioration of the liquid crystal.

[0014] More specifically, an electric field corresponding to a voltage difference between a data voltage of the pixel electrode **48** and a common voltage of the common electrode **35** (wherein the pixel electrode **48** is horizontally opposed to the common electrode **35** for each cell) is applied to the liquid crystal **78** of the TFT array **90** when a gate high voltage is applied to the gate electrode **34**. Such electric field is maintained during a period when a gate low voltage is applied. By this horizontal electric field, the liquid crystal **78** is driven to control a quantity of a light transmitted from the back light. Generally, a data voltage having the opposite polarity for each successive frame is applied to the liquid crystal **78** to prevent deterioration of the liquid crystal. On the other hand, a gate voltage having the same polarity for each frame is applied to a liquid crystal at the outer area of the TFT array **90**, particularly, in the gate link area, for the majority of a frame period. More specifically, a gate high voltage of about +20V is applied to each gate line **54** for a relatively short time during one frame period. A gate low voltage of about -5V is supplied during the remaining portion of the frame period, which is the majority of the frame period. Thus, a gate low voltage having a direct current component is applied to the liquid crystal in the gate link area during the majority of the frame period, thus causing deterioration of the liquid crystal over time. Moreover, liquid crystal deterioration at the gate link area is diffused into the liquid crystal in the vicinity of the edge of the TFT array **90**. As a result, a stain is generated at the periphery of the LCD because of such deterioration of the liquid crystal, thus degrading picture quality and reliability.

SUMMARY OF THE INVENTION

[0015] Accordingly, the present invention is directed to an in-plane switching mode liquid crystal display device that substantially obviates one or more problems due to the limitations and disadvantages of the related art.

[0016] Accordingly, it is an object of the present invention to provide a liquid crystal display device that is capable of preventing deterioration of liquid crystal at the outer area of an IPS mode TFT array.

[0017] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0018] In order to achieve these and other objects of the invention, an in-plane switching mode liquid crystal display device according to an embodiment of the present invention includes a plurality of data lines for applying data signals to a thin film transistor array; a plurality of gate lines for applying gate signals to the thin film transistor array; a plurality of gate links extended from the plurality of gate lines into the outer area of the thin film transistor array; and a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, to apply a common voltage to the thin film transistor array.

[0019] These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings.

[0020] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0022] In the drawings:

[0023] **FIG. 1** is a plan view showing a structure of a conventional IPS mode LCD device;

[0024] **FIG. 2** is a sectional view of the LCD device taken along the B-B' line in **FIG. 1**;

[0025] **FIG. 3** is a sectional view representing a driving characteristic of the LCD device shown in **FIG. 1**;

[0026] **FIG. 4** is a schematic plan view showing an electrode arrangement of the LCD device shown in **FIG. 1**;

[0027] **FIG. 5** is a plan view showing an electrode arrangement of a LCD device according to an embodiment of the present invention; and

[0028] **FIG. 6** is a driving waveform diagram of voltages applied to the gate line and the common voltage line shown in **FIG. 5**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0029] Reference will now be made in detail to the preferred embodiment of the present invention, example of which is illustrated in the accompanying drawings.

[0030] Referring to **FIG. 5**, there is shown a liquid crystal display (LCD) device according to an embodiment of the present invention. The LCD device includes a TFT array **104** for displaying a picture on a rear substrate **100**, a plurality of common voltage pads **102** and a plurality of common voltage lines **110** for applying a common voltage from an external driver to the TFT array **104**, and a plurality of gate pads **106** and a plurality of gate lines **112**.

[0031] In **FIG. 5**, the common voltage lines **110** are formed in parallel to the gate lines **112** within the TFT array **104**. The common voltage lines **110** within the TFT array **104** are commonly connected by the common voltage lines **110** crossing the gate links **108** at an outer area of the TFT array **104**. In particular, a plurality of common voltage lines **110** also is provided at the outer area of the TFT array **104** to apply a common voltage to a liquid crystal at the outer area thereof. Further, the common voltage lines **110** are connected to the external driver via the common voltage pads **102** formed at the outer area of the TFT array **104**. The gate pads **106** connected to the external driver are connected to the gate lines **112** within the TFT array **104** via the gate links **108**.

[0032] Gate voltages V_{gh} and V_{gl} and a common voltage V_{com} having waveforms as shown in **FIG. 6** are applied to the TFT array **104**. Referring to **FIG. 6**, a common voltage

Vcom of +5V is applied to the common voltage lines **110**, while a gate high voltage of about +20V and a gate low voltage Vgl of about -5V are applied to the gate lines **112**. The TFTs provided within the TFT array **104** are switched by the gate high voltage applied to the TFT array **104** via the gate pads **106** and the gate links **108** to drive the liquid crystal cells. In this case, the gate low voltage Vgl, which is applied for the majority of the duration period of the gate voltages Vgh and Vgl, is loaded on a liquid crystal at the outer area of the TFT array **104** by the gate links **108** and is distributed and reduced by the common voltage Vcom applied to the common voltage lines **110** crossing the gate links **108**. The gate voltage applied to a liquid crystal at the gate link area is distributed by the common voltage lines as mentioned above, so that deterioration of liquid crystal can be prevented.

[0033] As described above, according to the present invention, a plurality of common voltage lines is provided at the outer area of the TFT array in such a manner to cross the gate links, thereby allowing a gate voltage loaded on a liquid crystal at the gate link area is distributed and reduced by the common voltage. Accordingly, deterioration of liquid crystal caused by the gate voltage at the outer area of the TFT array can be prevented to eliminate a generation of stain.

[0034] It will be apparent to those of skill in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An in-plane switching mode liquid crystal display device comprising:

- a plurality of data lines for applying data signals to a thin film transistor array;
- a plurality of gate lines for applying gate signals to the thin film transistor array;
- a plurality of gate links extended from the plurality of gate lines into an outer area of the thin film transistor array; and
- a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, for applying a common voltage to the thin film transistor array.

2. The in-plane switching liquid crystal display device according to claim 1, wherein the common voltage lines are provided at the thin film transistor array to be in parallel to the gate lines.

3. The in-plane switching liquid crystal display device according to claim 1, wherein the common voltage is approximately +5V.

4. The in-plane switching liquid crystal display device according to claim 1, wherein the gate signals include a gate low voltage signal of approximately -5V.

5. The in-plane switching liquid crystal display device according to claim 1, wherein the gate signals include a gate high voltage signal of approximately +20V.

6. An in-plane switching mode liquid crystal display device, comprising:

first and second substrates;

a plurality of data lines;

a plurality of gate lines perpendicular to the data lines;

a plurality of thin film transistors at crossing points of the data and gate lines and forming a thin film transistor array on the first substrate;

a plurality of gate links extended from the plurality of gate lines into an area outside of the thin film transistor array; and

a plurality of common voltage lines parallel to the gate lines and crossing the gate links.

7. The in-plane switching liquid crystal display device of claim 6, further comprising:

a plurality of gate pads connected to the gate links and electrically disposed between the gate links and an external power source; and

a plurality of common voltage pads connected to the common voltage lines and electrically disposed between the common voltage lines and the external power source.

8. The in-plane switching liquid crystal display device of claim 7, wherein the gate pads are located in the area outside of the thin film transistor array.

9. The in-plane switching liquid crystal display device of claim 7, wherein the common voltage pads are located in the area outside of the thin film transistor array.

10. An in-plane switching mode liquid crystal display device comprising:

a plurality of data lines for applying data signals to a thin film transistor array;

a plurality of gate lines for applying gate signals to the thin film transistor array;

a plurality of signal pads in a signal pad area outside the thin film transistor array; and

a plurality of common lines, at least one of said common lines extending between the signal pads and the thin film transistor array.

11. The in-plane switching liquid crystal display device of claim 10, wherein the signal pads are gate pads for applying the gate signals to the gate lines.

12. The in-plane switching liquid crystal display device of claim 11, wherein the at least one common line crosses the gate lines in an area between the gate pads and the thin film transistor array.

13. The in-plane switching liquid crystal display device of claim 11, wherein the at least one common line is parallel to the data lines.

14. The in-plane switching liquid crystal display device of claim 10, wherein the signal pads are data pads for applying the data signals to the data lines.

15. The in-plane switching liquid crystal display device of claim 14, wherein the at least one common line crosses the data lines in an area between the data pads and the thin film transistor array.

16. The in-plane switching liquid crystal display device of claim 14, wherein the at least one common line is parallel to the data lines.

专利名称(译)	面内切换模式液晶显示装置		
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申请号	US09/887337	申请日	2001-06-25
[标]申请(专利权)人(译)	宋DUK		
申请(专利权)人(译)	宋DUK		
当前申请(专利权)人(译)	宋DUK		
[标]发明人	SONG IN DUK		
发明人	SONG, IN DUK		
IPC分类号	G02F1/136 G02F1/1333 G02F1/1343 G02F1/1345		
CPC分类号	G02F1/134363 G02F1/1345 G02F2001/133388 G02F2201/121		
优先权	1020000055034 2000-09-19 KR		
其他公开文献	US6806935		
外部链接	Espacenet USPTO		

摘要(译)

一种液晶显示装置，其能够防止在IPS模式TFT阵列的外部区域处产生的液晶劣化。在该器件中，多条数据线将数据信号施加到薄膜晶体管阵列，并且多条栅极线将栅极信号施加到薄膜晶体管阵列。多条栅极链路从栅极线延伸到薄膜晶体管阵列的外部区域。以这样的方式提供多条公共电压线以跨越栅极链路以将公共电压施加到薄膜晶体管阵列。因此，可以防止由TFT阵列的外部区域处的栅极电压引起的液晶劣化，以消除污点的产生。

