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(54) **LOW-COST LARGE-SCREEN WIDE-ANGLE FAST-RESPONSE LIQUID CRYSTAL DISPLAY APPARATUS**

Publication Classification

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(51) **Int. Cl.**
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(57) **ABSTRACT**

The present invention discloses a super large wide-angle high-speed response liquid crystal display apparatus manufactured by using a photolithographic procedure for three times. The invention adopts a halftone exposure technology to form a gate electrode, a common electrode, a pixel electrode and a contact pad, and then uses the halftone exposure technology to form a silicon (Si) island and a contact hole, and a general exposure technology to form a source electrode, a drain electrode and an orientation control electrode. A passivation layer uses a masking deposition method. A film is formed by using a P-CVD method, or a protective area is formed at a local area by using an ink coating method or spray method, and a TFT array substrate used for the super large wide-angle high-speed response liquid crystal display apparatus manufactured by using a photolithographic procedure for three times can be produced.

(73) Assignee: **Mikuni Electron Co. Ltd.**,
Ibaraki Prefecture (JP)

(21) Appl. No.: **12/558,086**

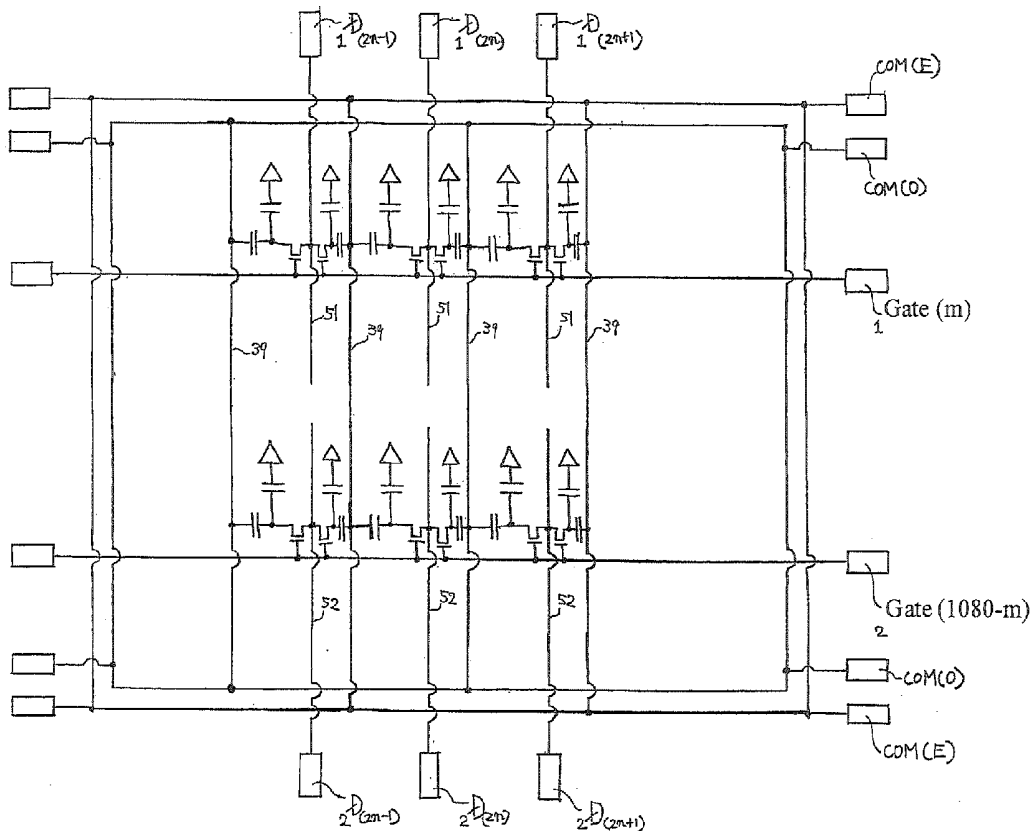
(22) Filed: **Sep. 11, 2009**

Related U.S. Application Data

(62) Division of application No. 11/743,749, filed on May 3, 2007.

Foreign Application Priority Data

Jun. 15, 2006 (JP) JP 2006-202563



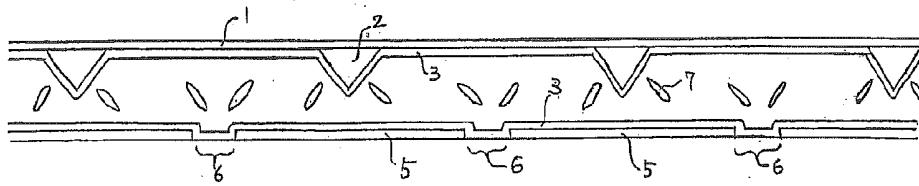


Fig. 1

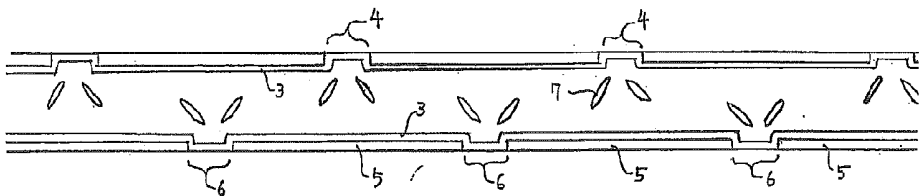


Fig. 2

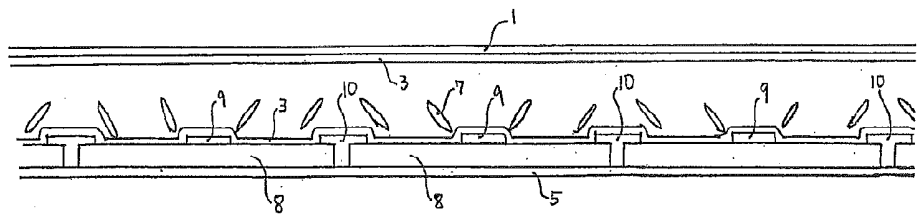


Fig. 3

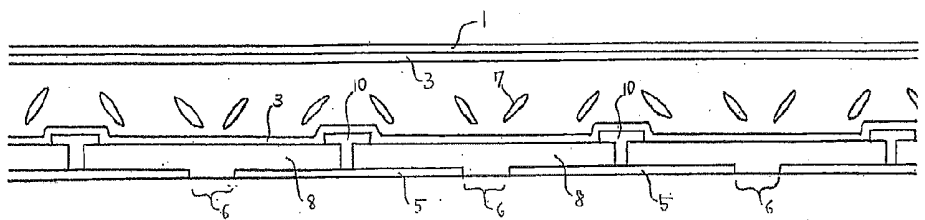


Fig. 4

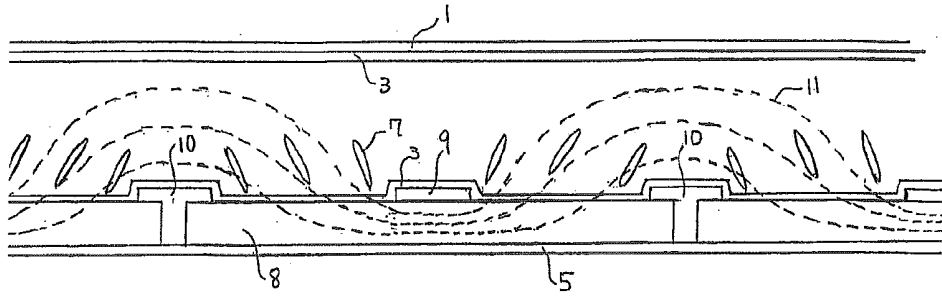


Fig. 5

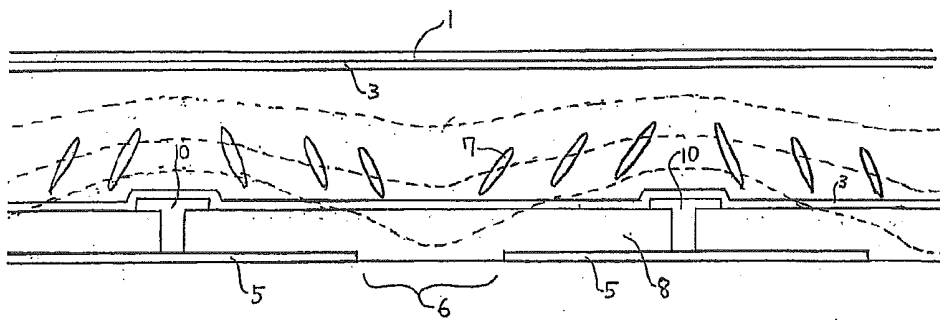


Fig. 6

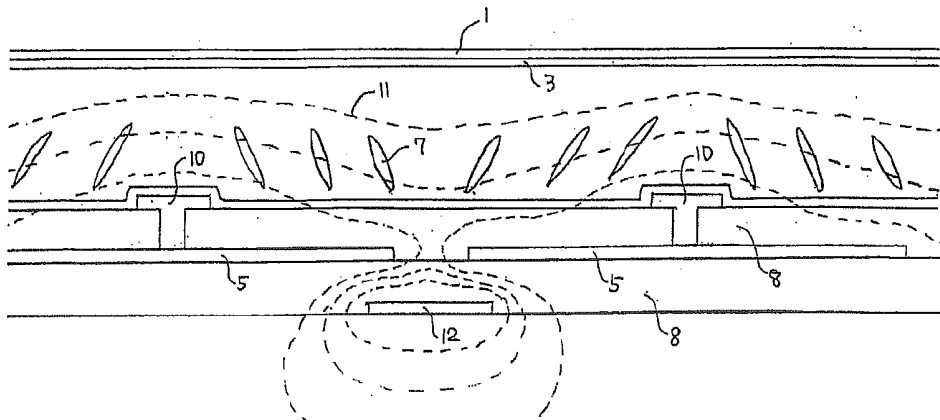


Fig. 7

Photolithographic procedure for 3 times (Halftone exposure for 2 times)

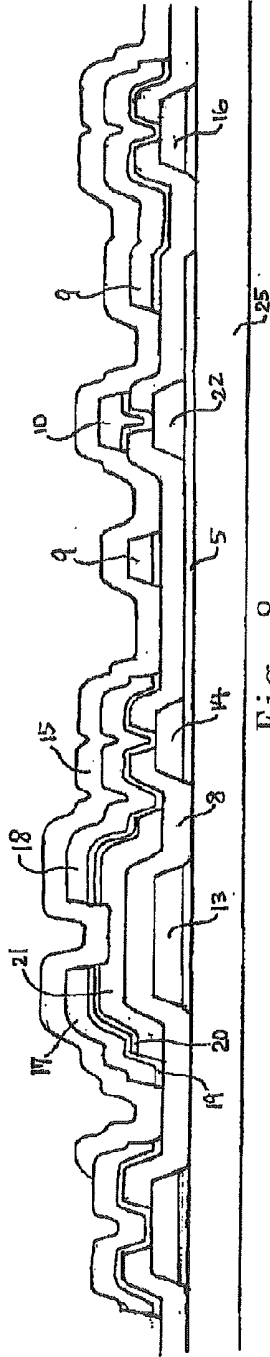


Fig. 8

Photolithographic procedure for 3 times (Halftone exposure for 2 times)

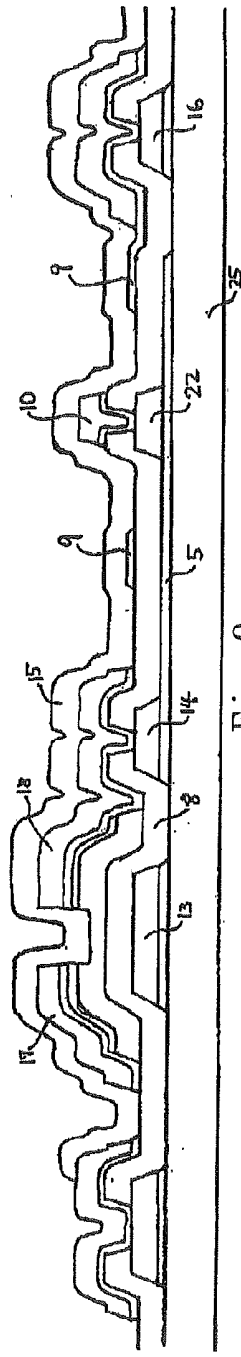


Fig. 9

Photolithographic procedure for 3 times (Halftone exposure for 2 times)

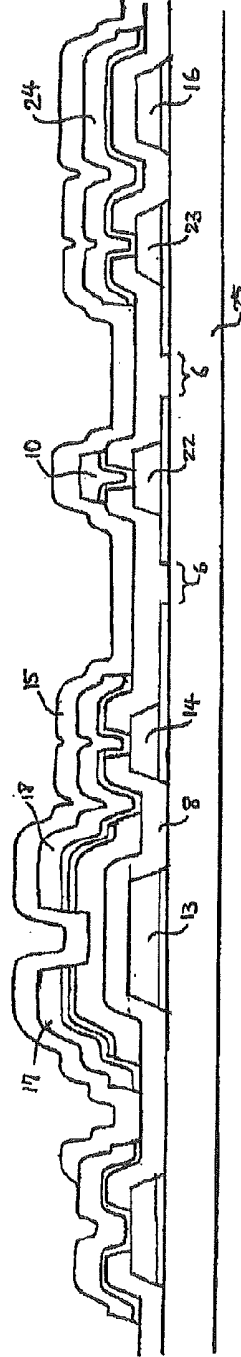


Fig. 10

Photolithographic procedure for 4 times (Halftone exposure for 2 times)

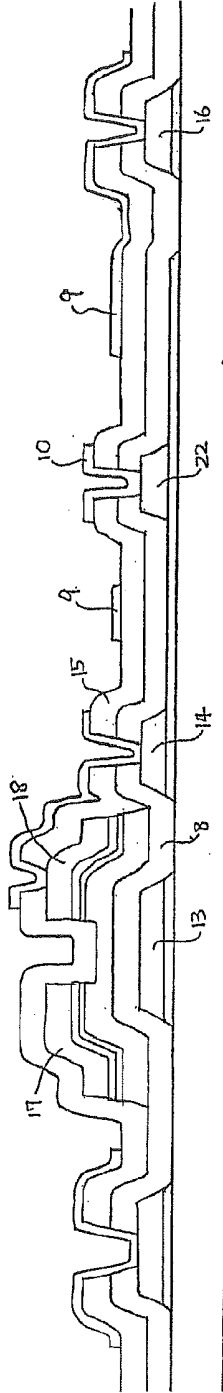


Fig. 11

Photolithographic procedure for 4 times (Halftone exposure for 2 times)

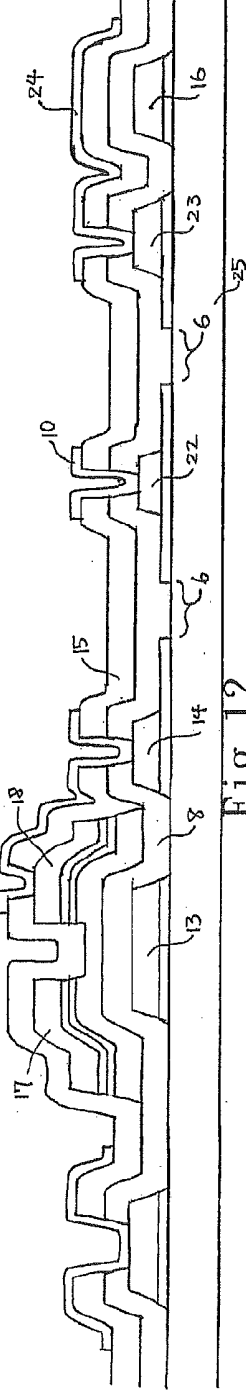


Fig. 12

Photolithographic procedure for 4 times (Halftone exposure for 2 times)

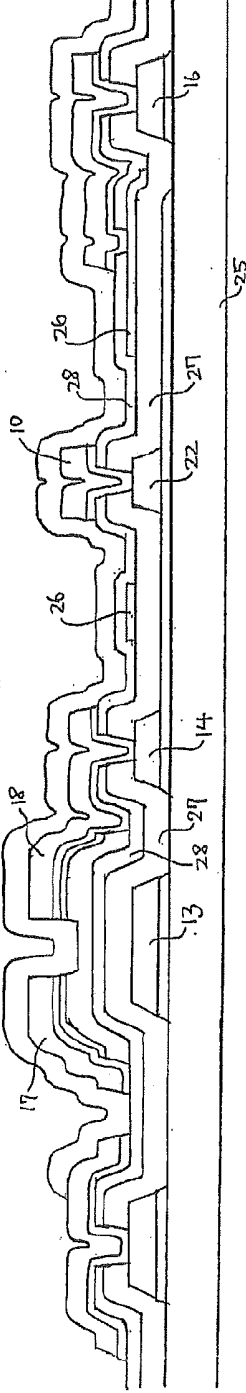


Fig. 13

Photolithographic procedure for 4 times (One time of halftone exposure)

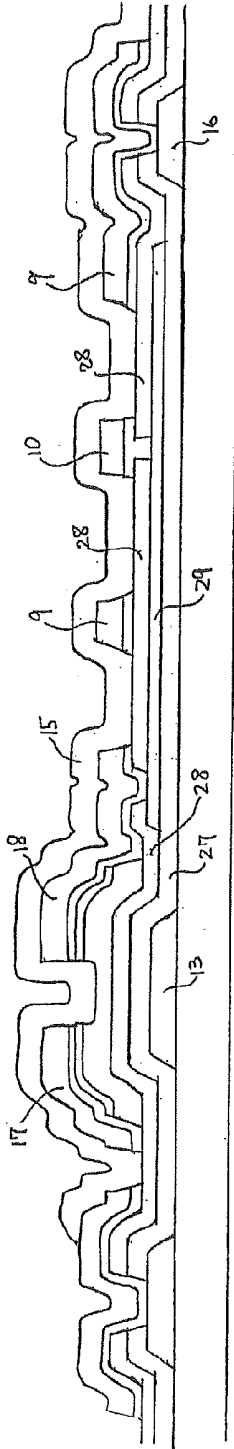


Fig. 14

Photolithographic procedure for 4 times (One time of halftone exposure)

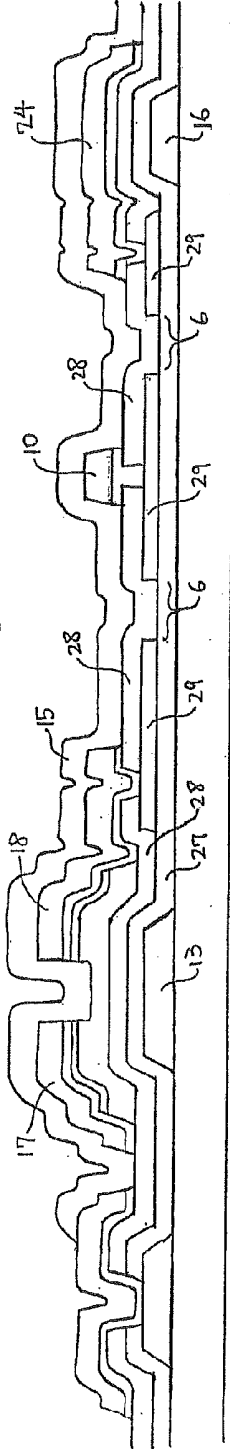


Fig. 15

Photolithographic procedure for 4 times (One time of halftone exposure)

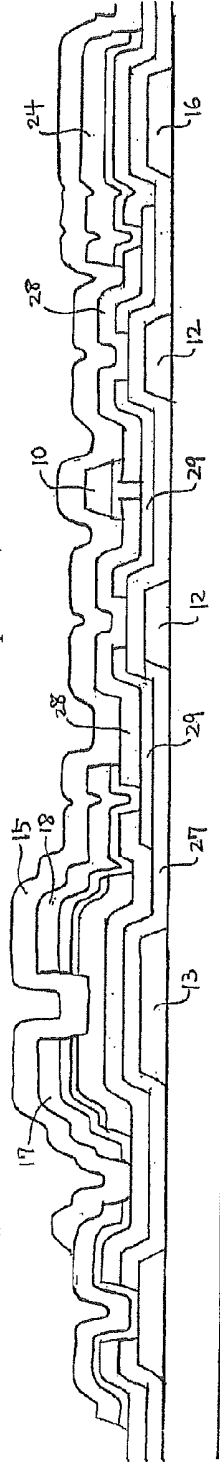


Fig. 16

Photolithographic procedure for 4 times (Half-tone exposure for 1 time)

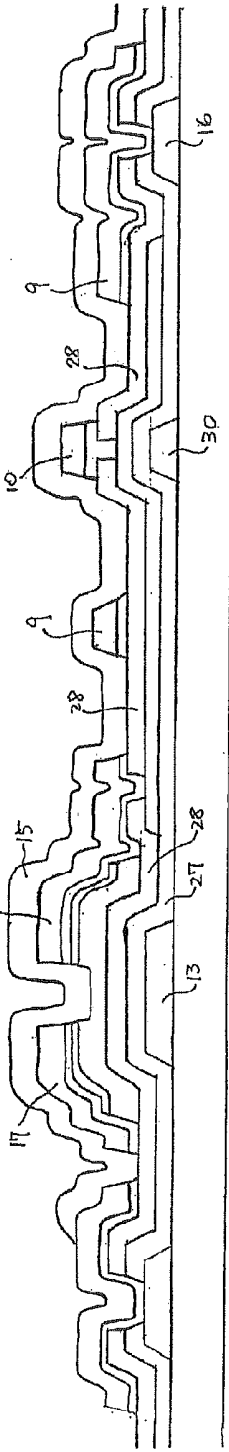


Fig. 17

Photolithographic procedure for 4 times (Half-tone exposure for 1 time)

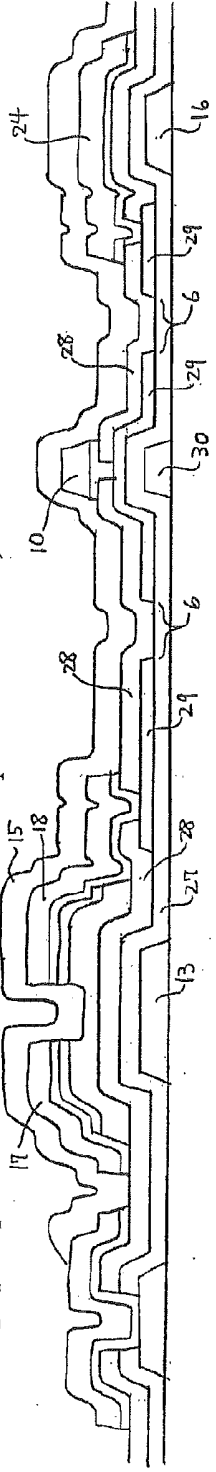


Fig. 18

Photolithographic procedure for 4 times (Half-tone exposure for 1 time)

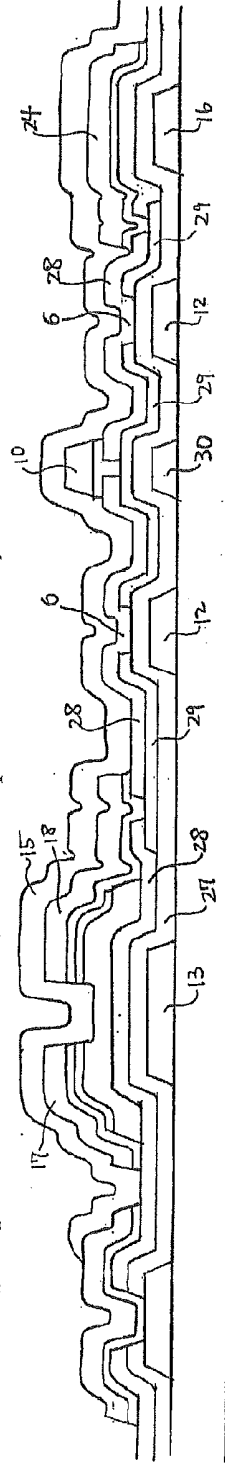


Fig. 19

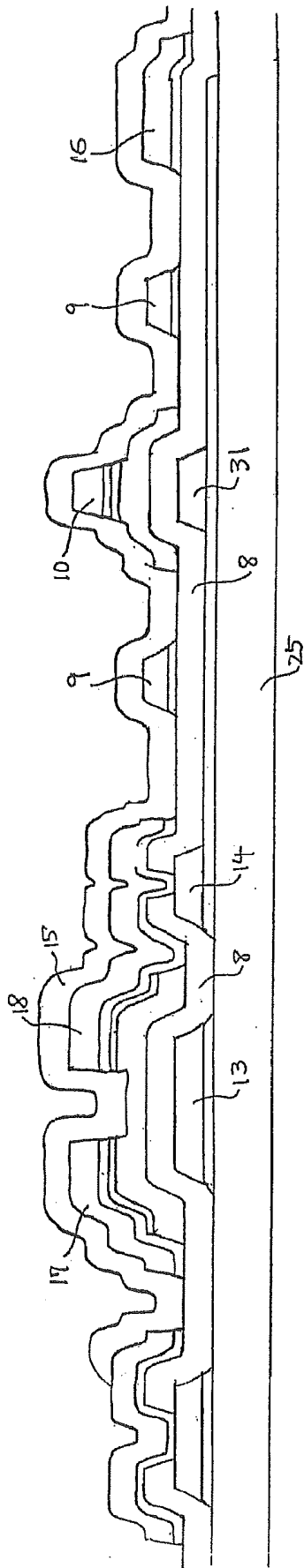


Fig. 20

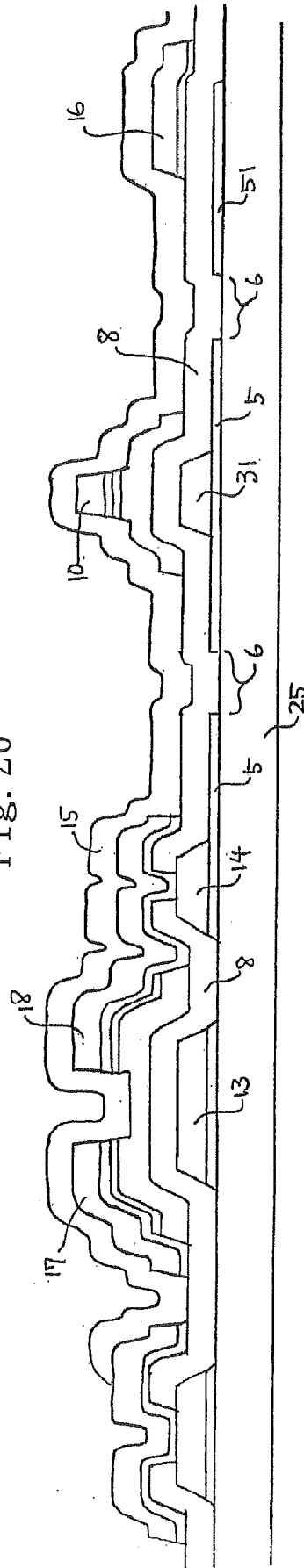


Fig. 21

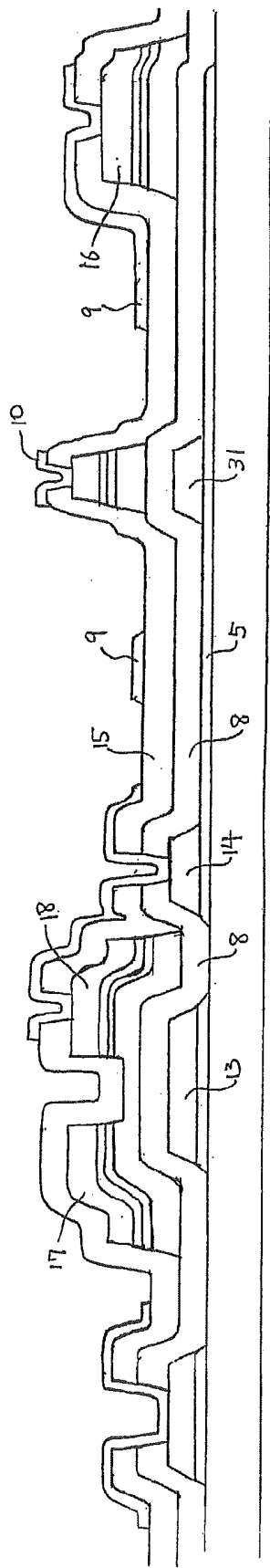


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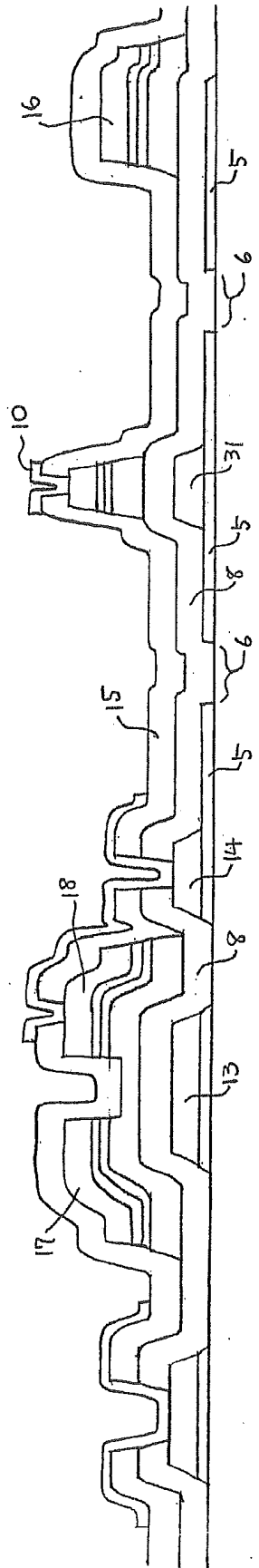


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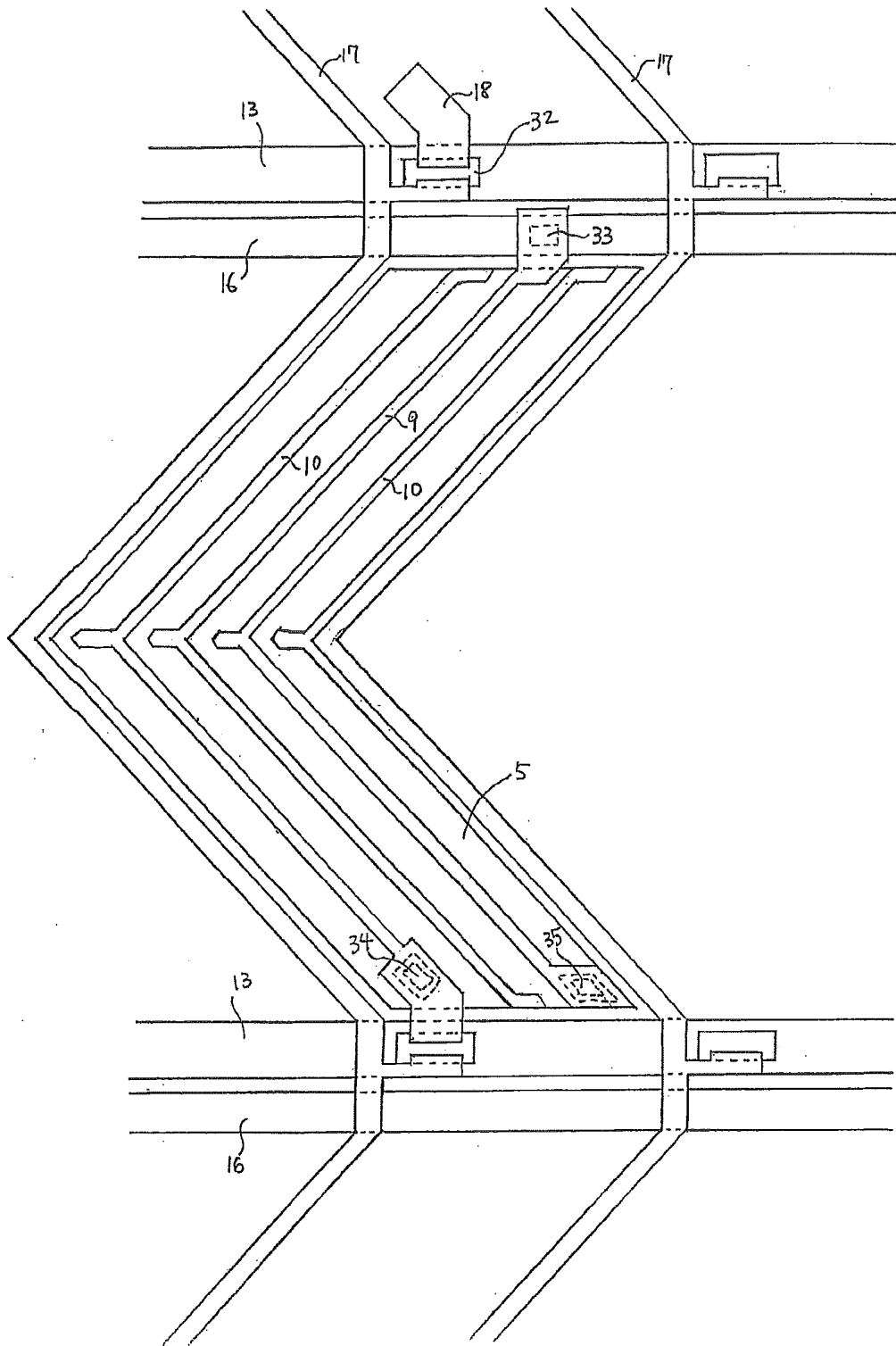


Fig. 24

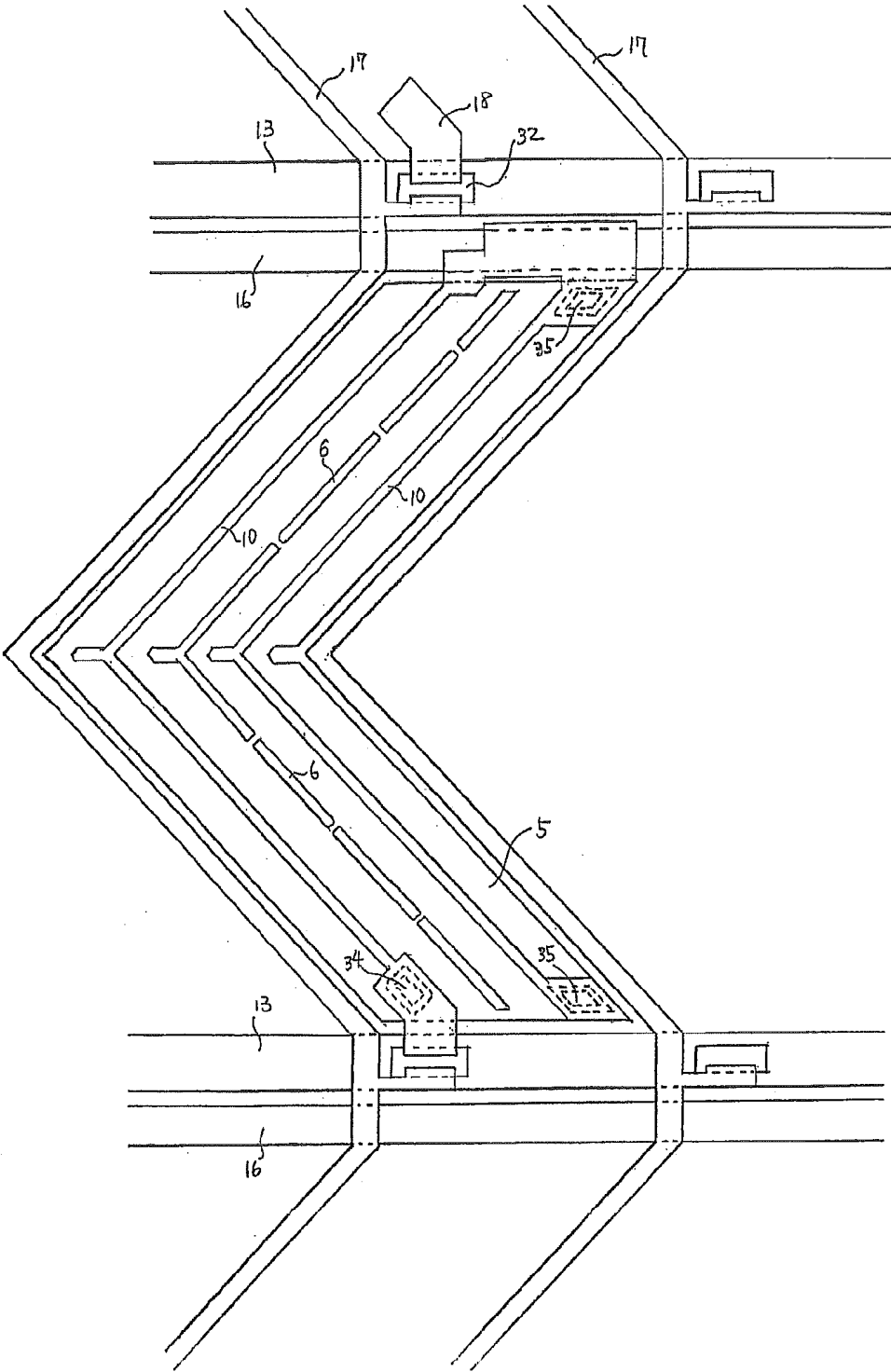


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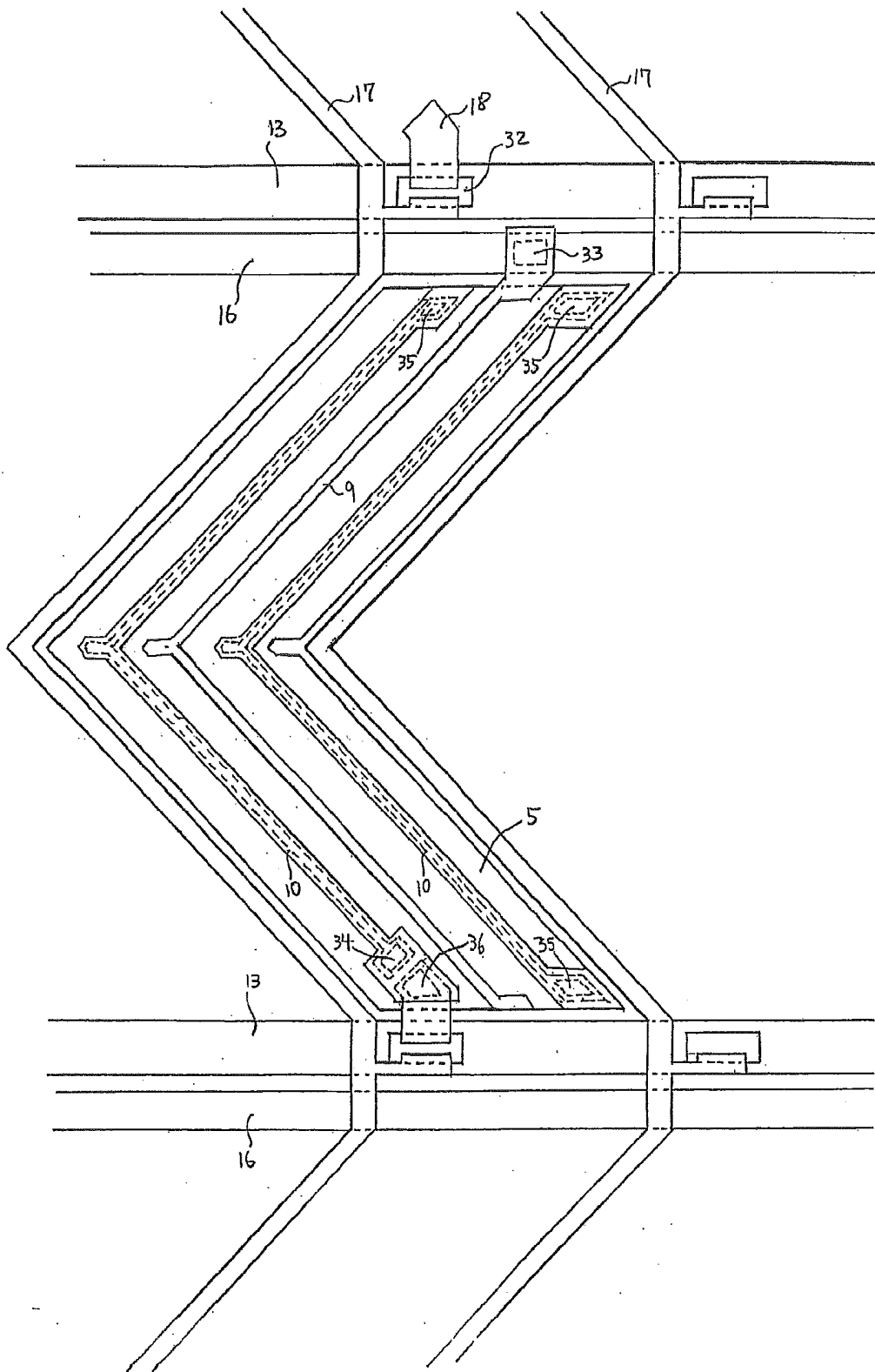


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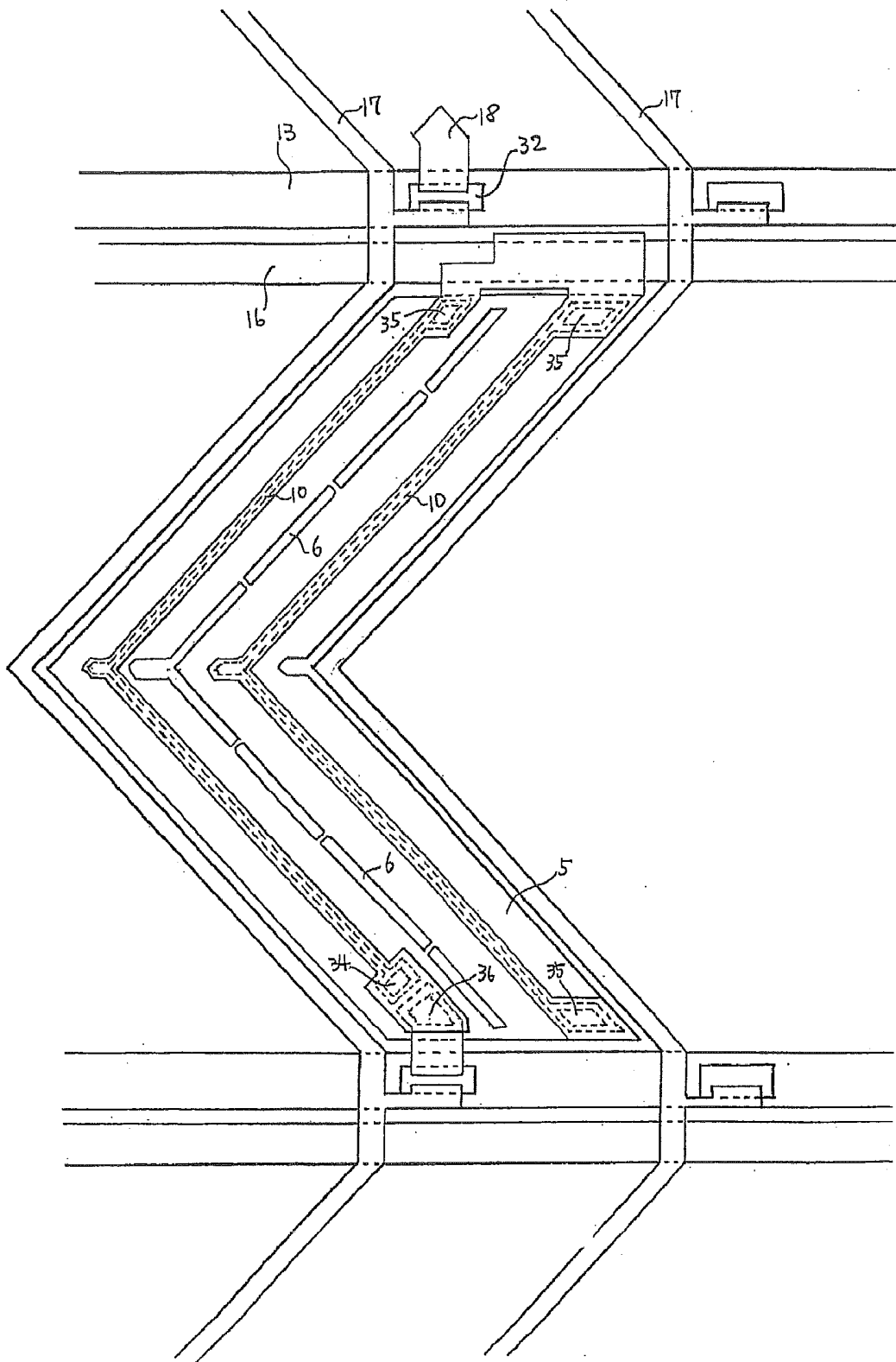


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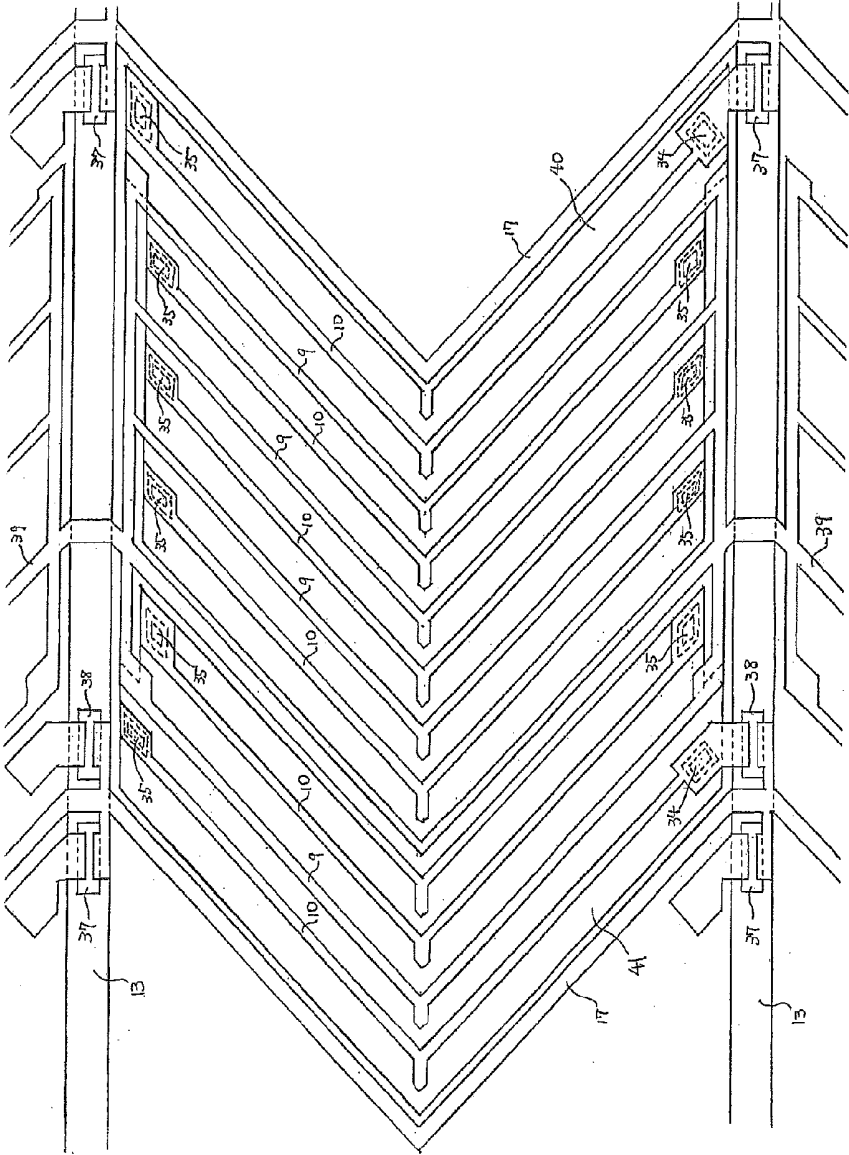


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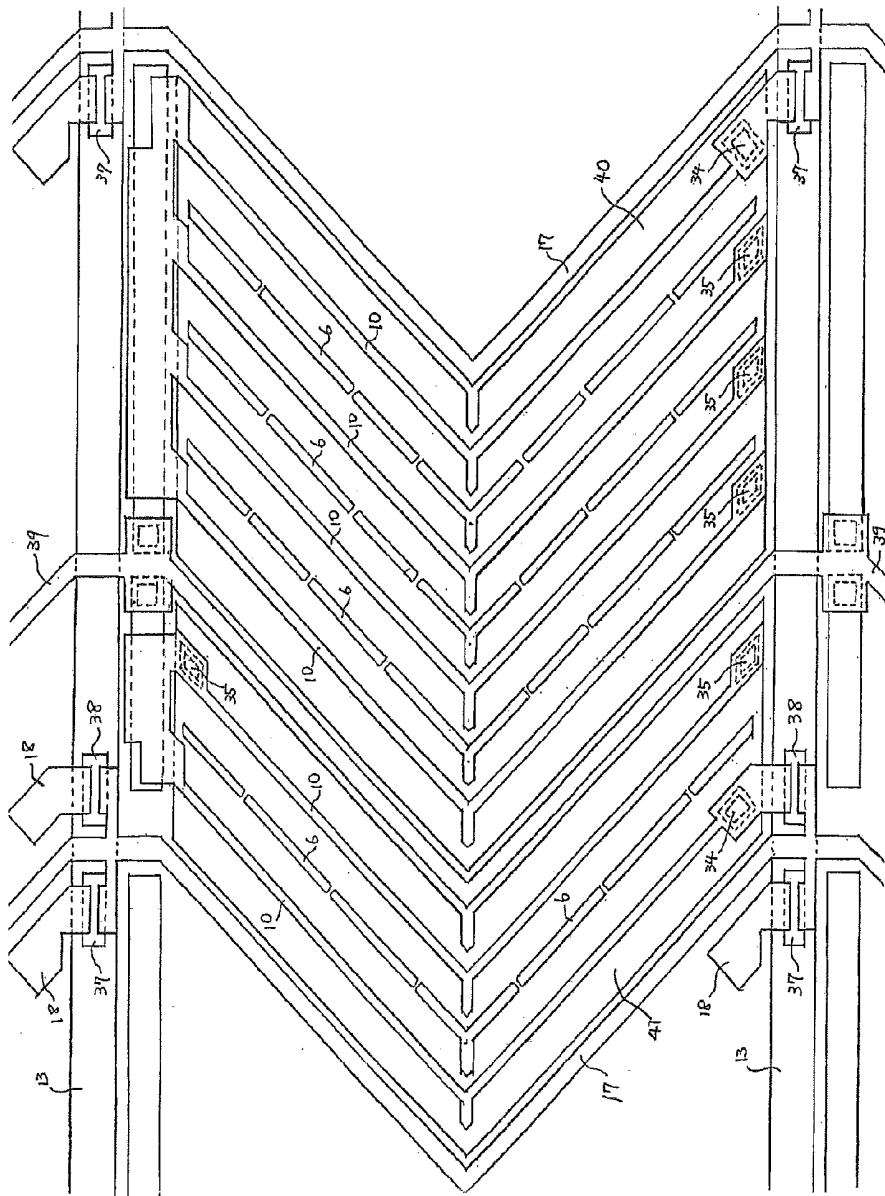


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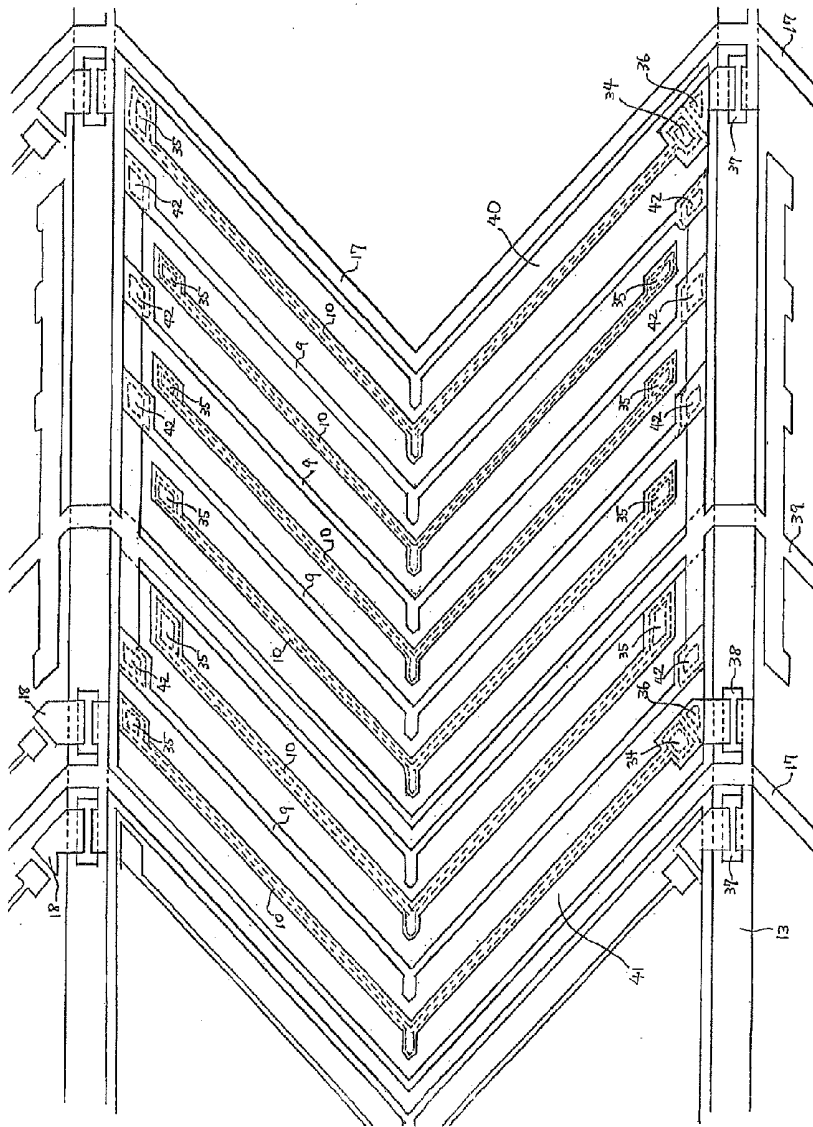


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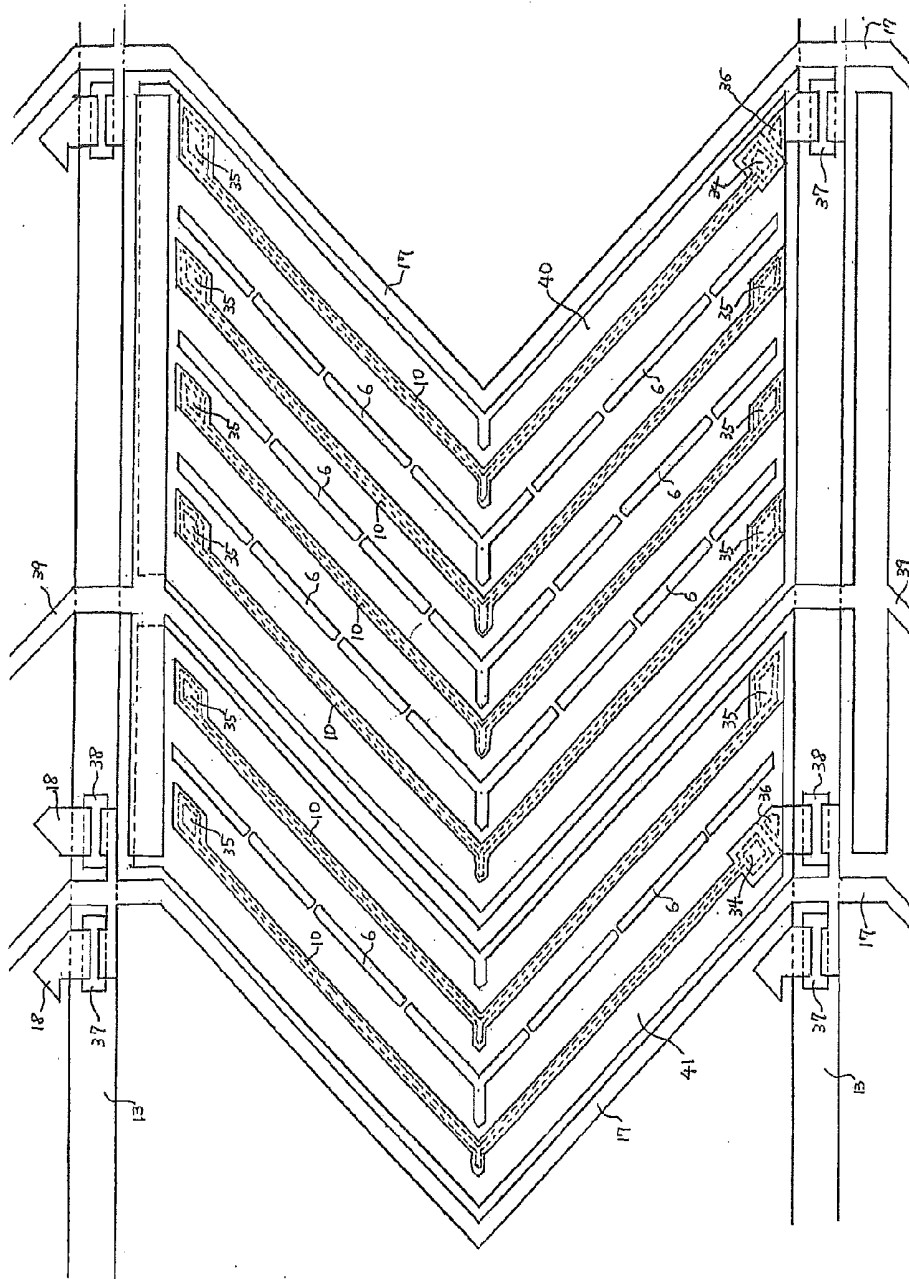


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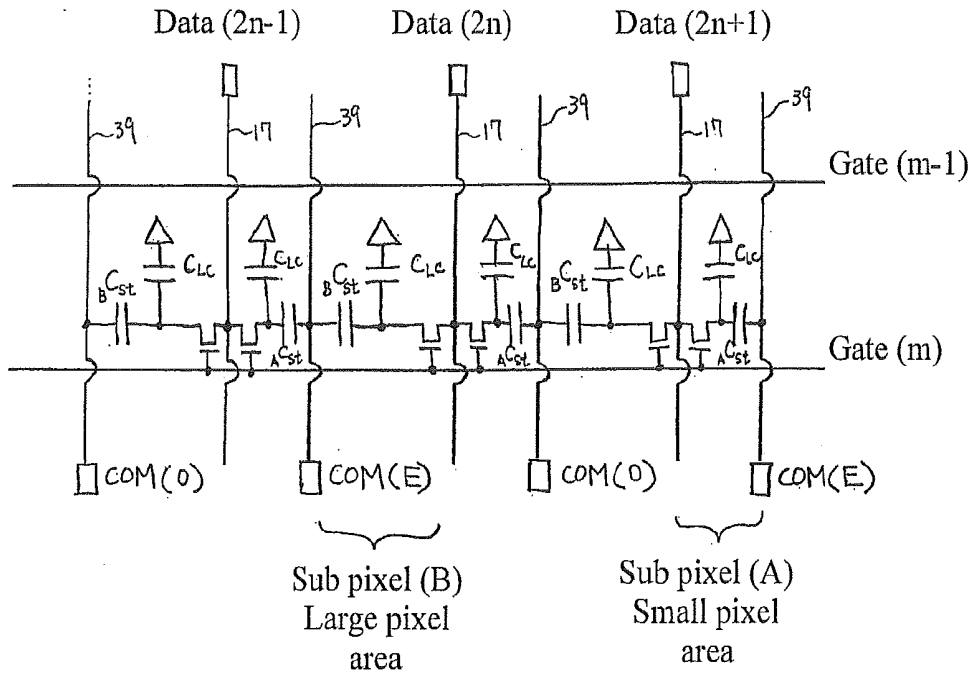


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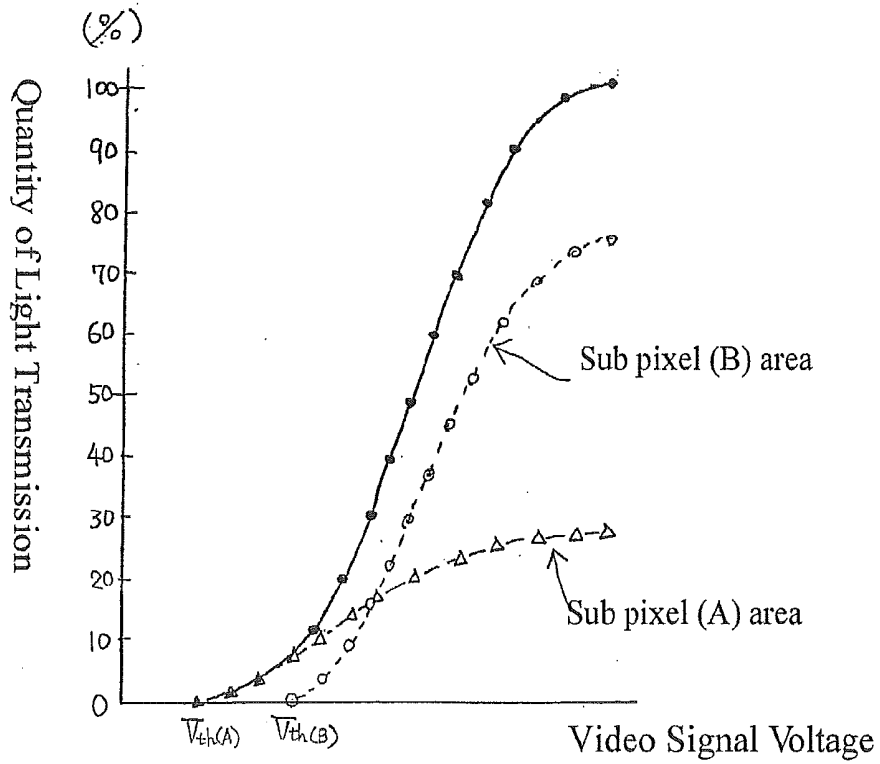


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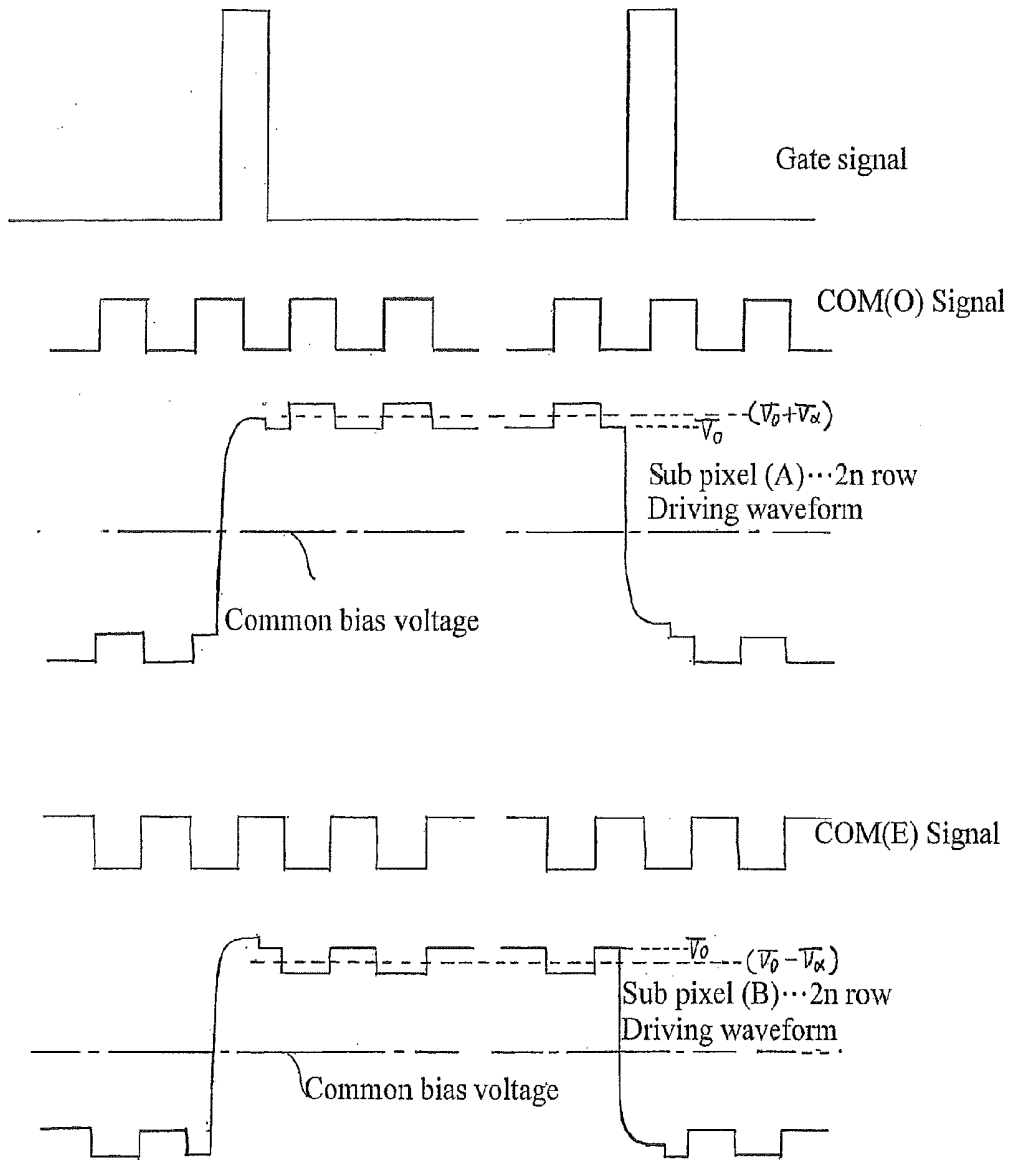


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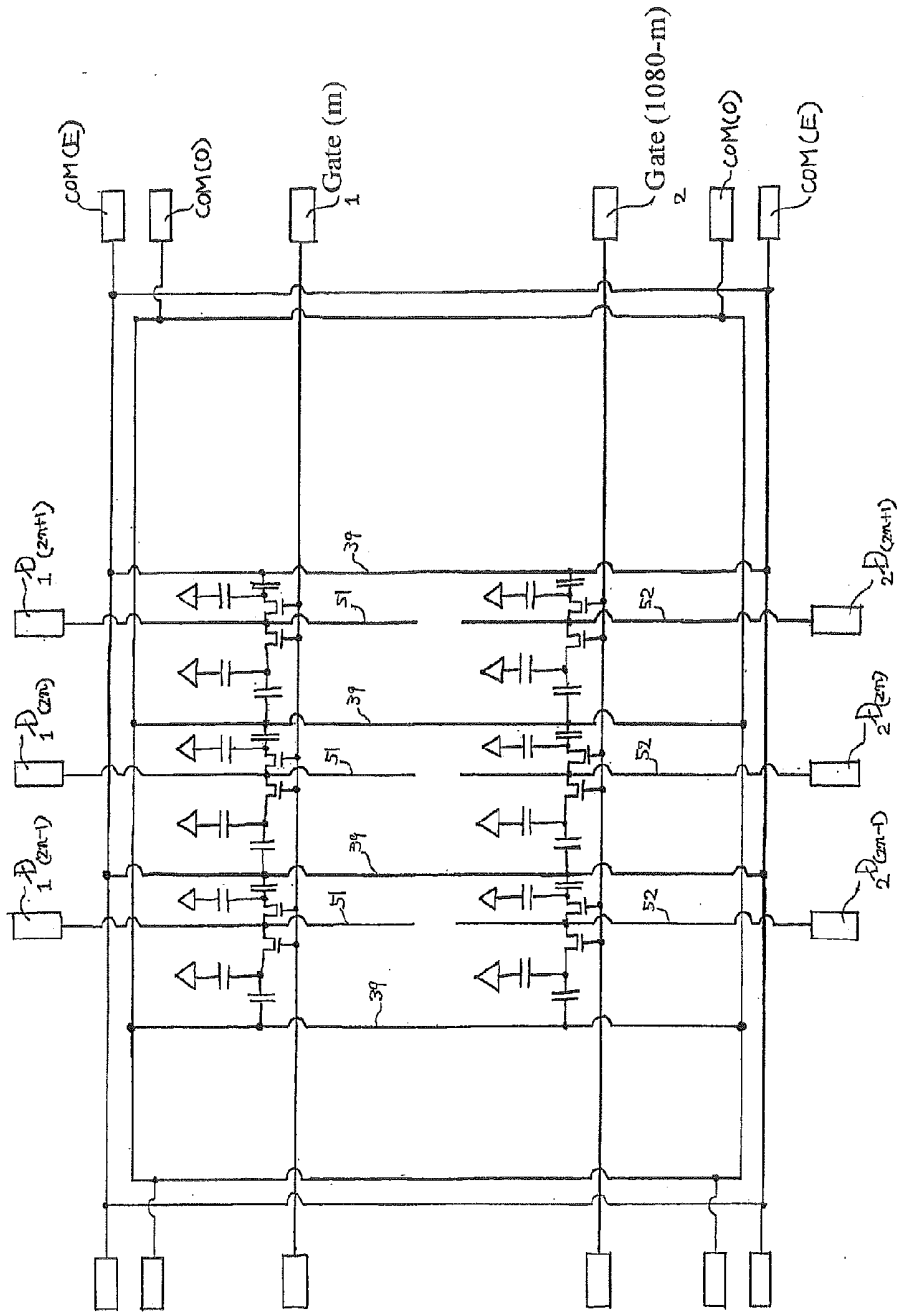


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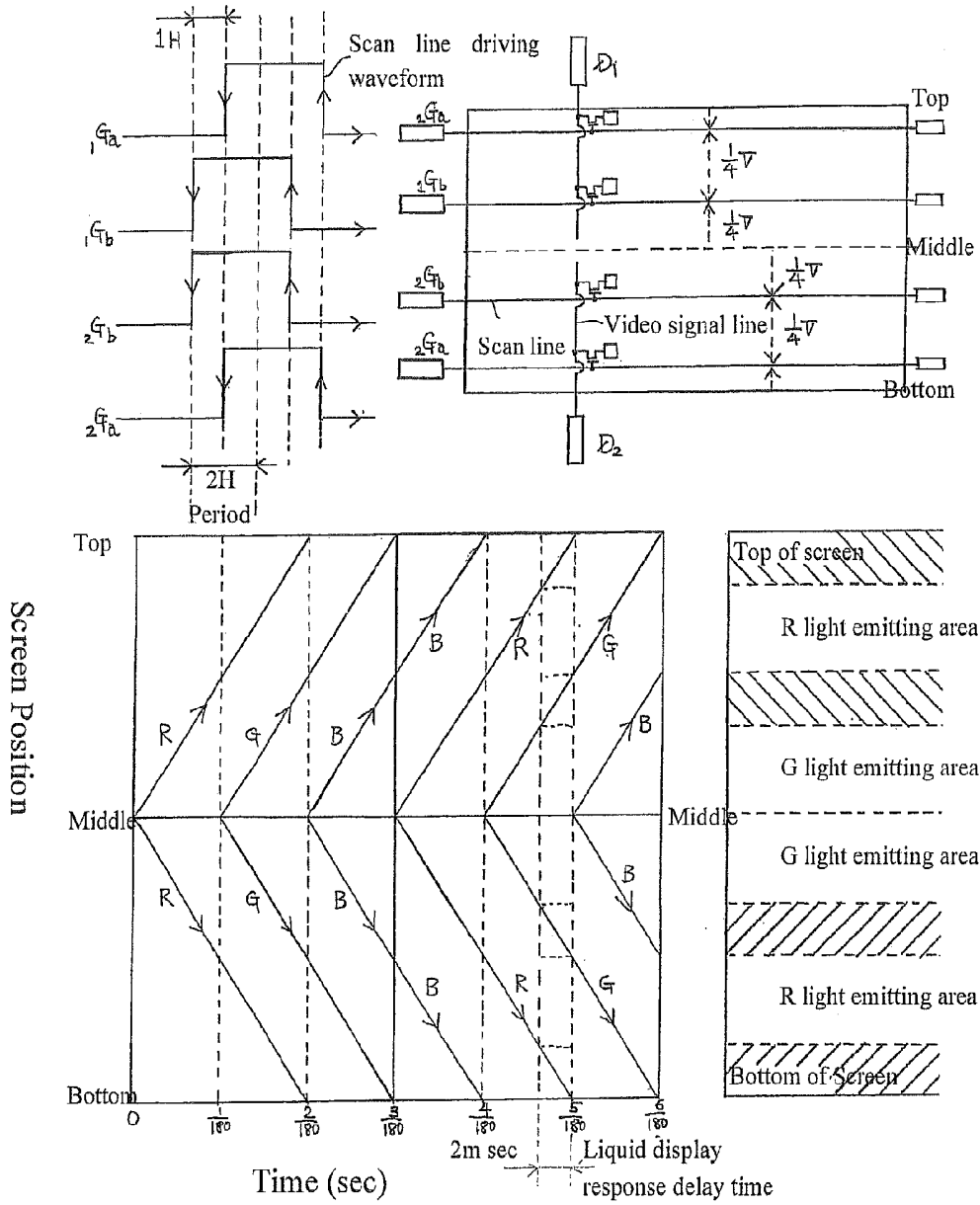


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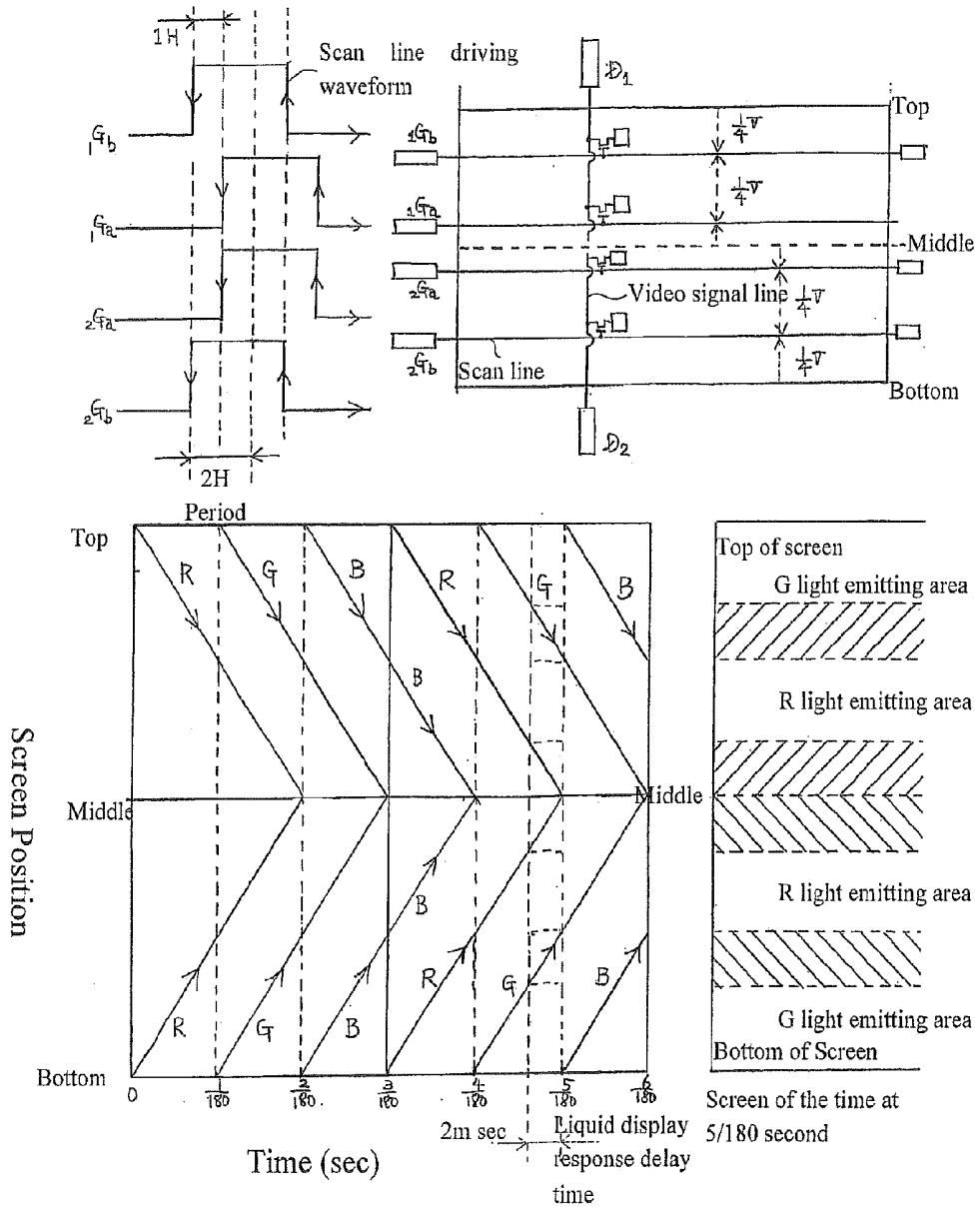


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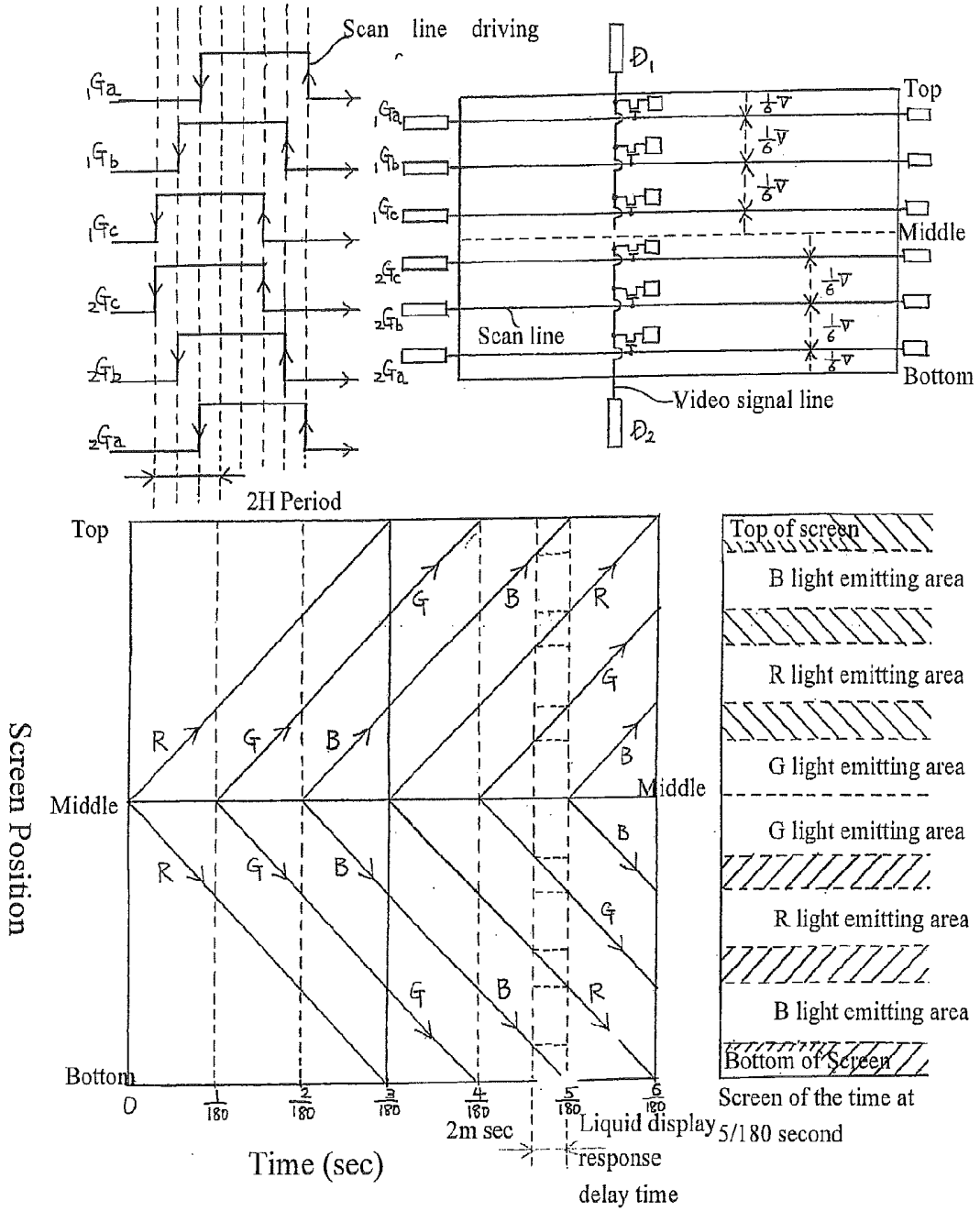


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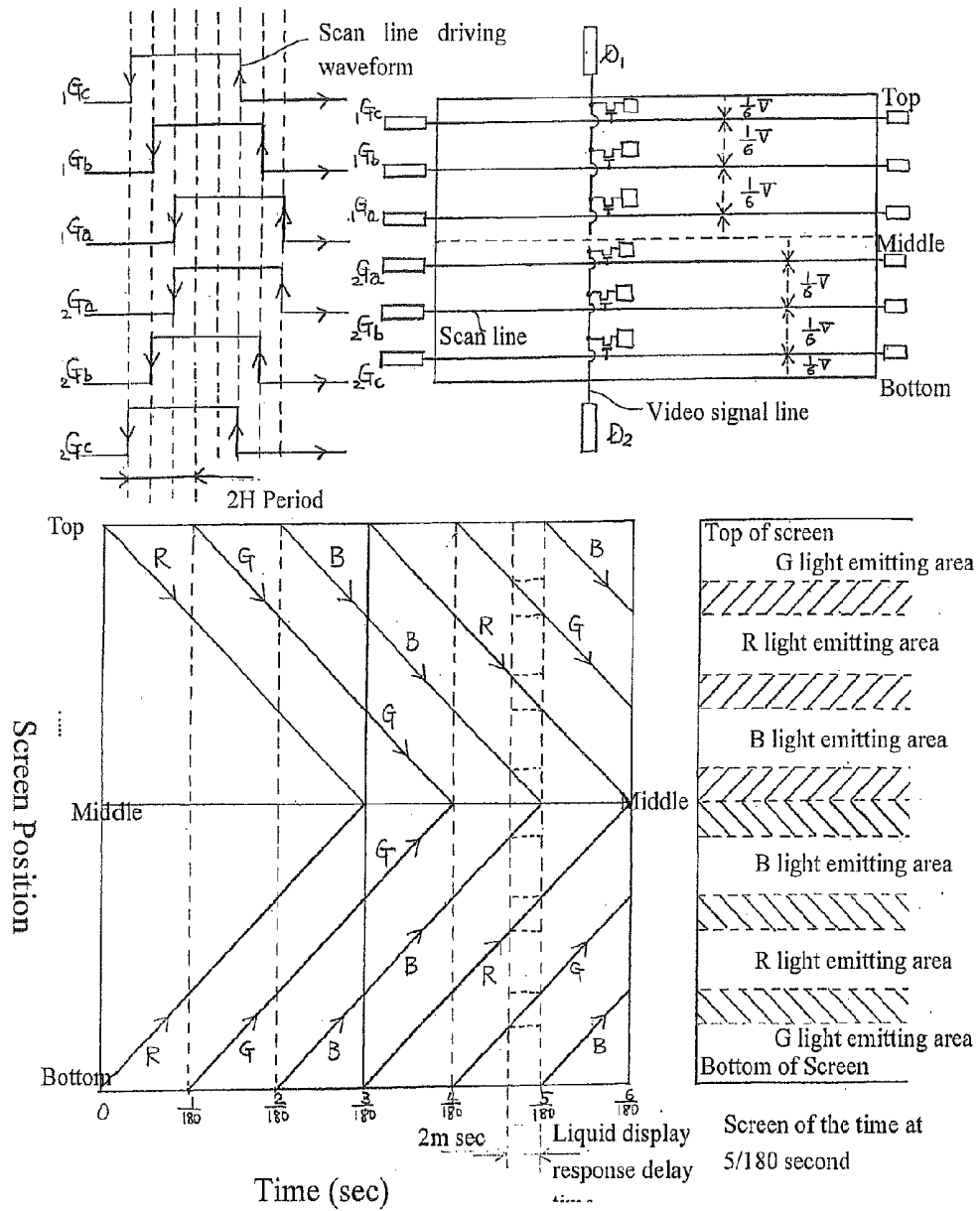


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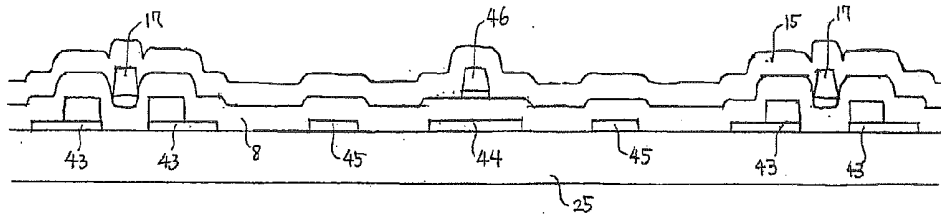


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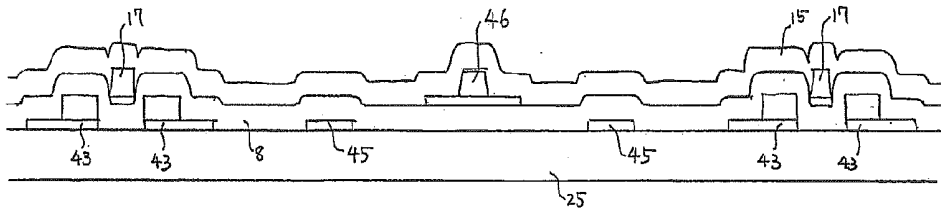


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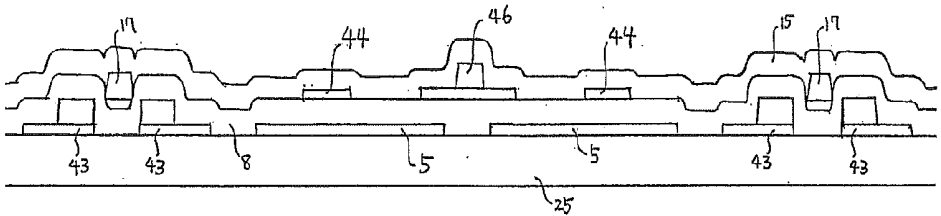


Fig. 42

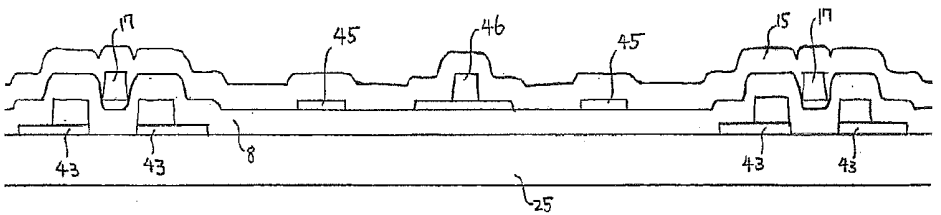


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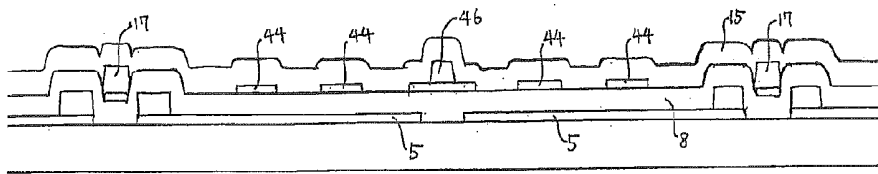


Fig. 44

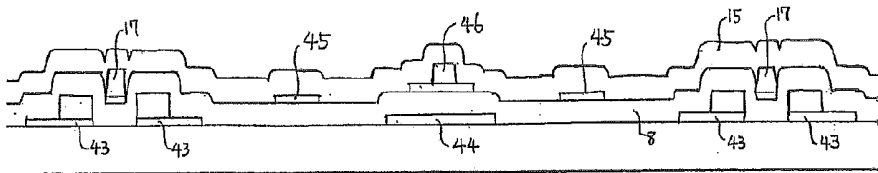


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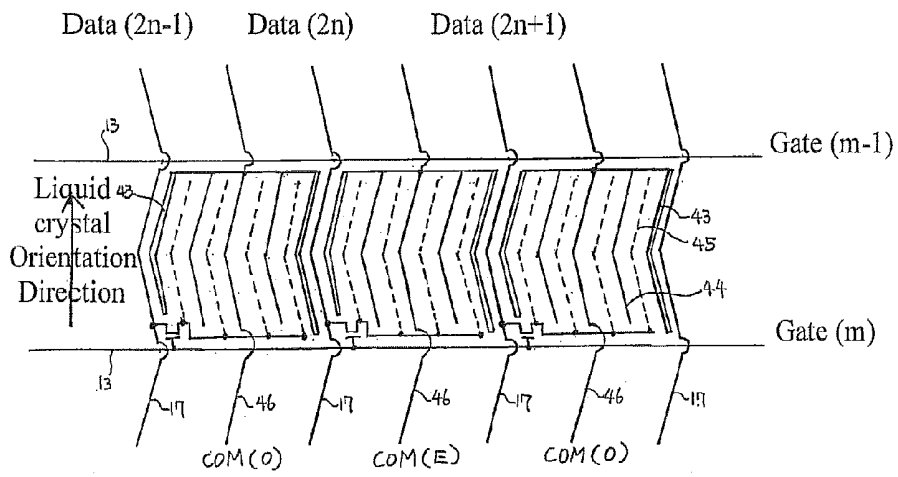


Fig. 46

Photolithographic procedure for 3 times (Halftone exposure for 3 times)

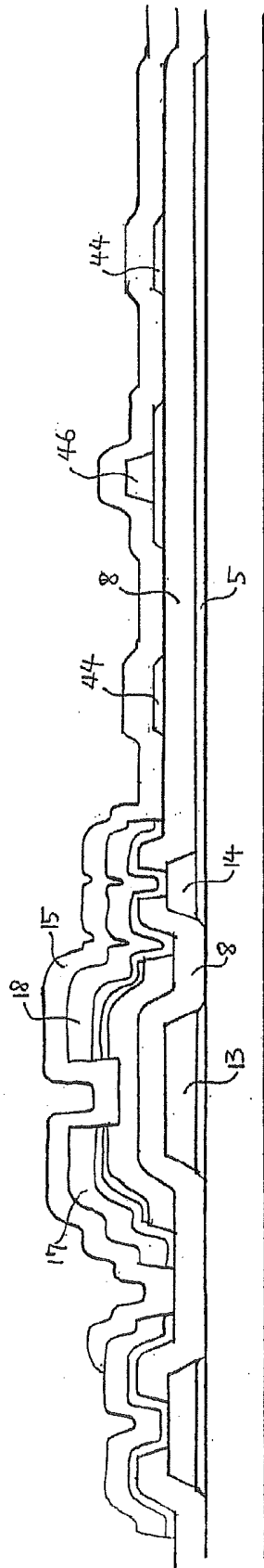


Fig. 47

Photolithographic procedure for 3 times (Halftone exposure for 3 times)

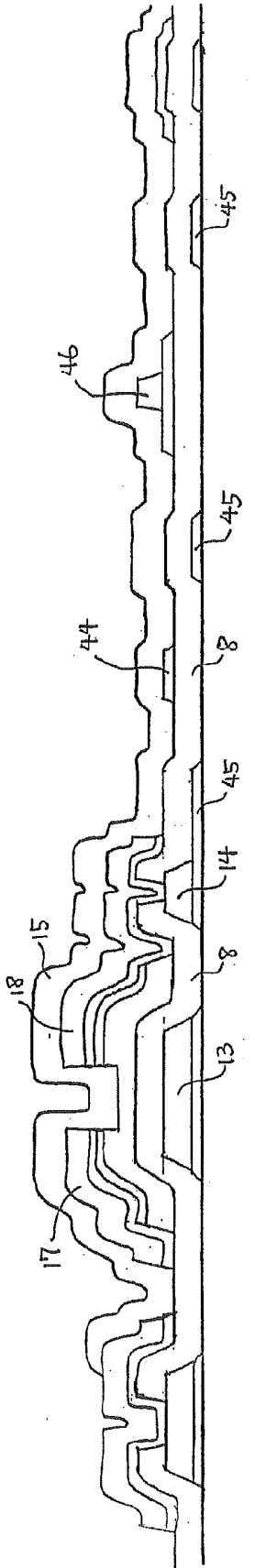


Fig. 48

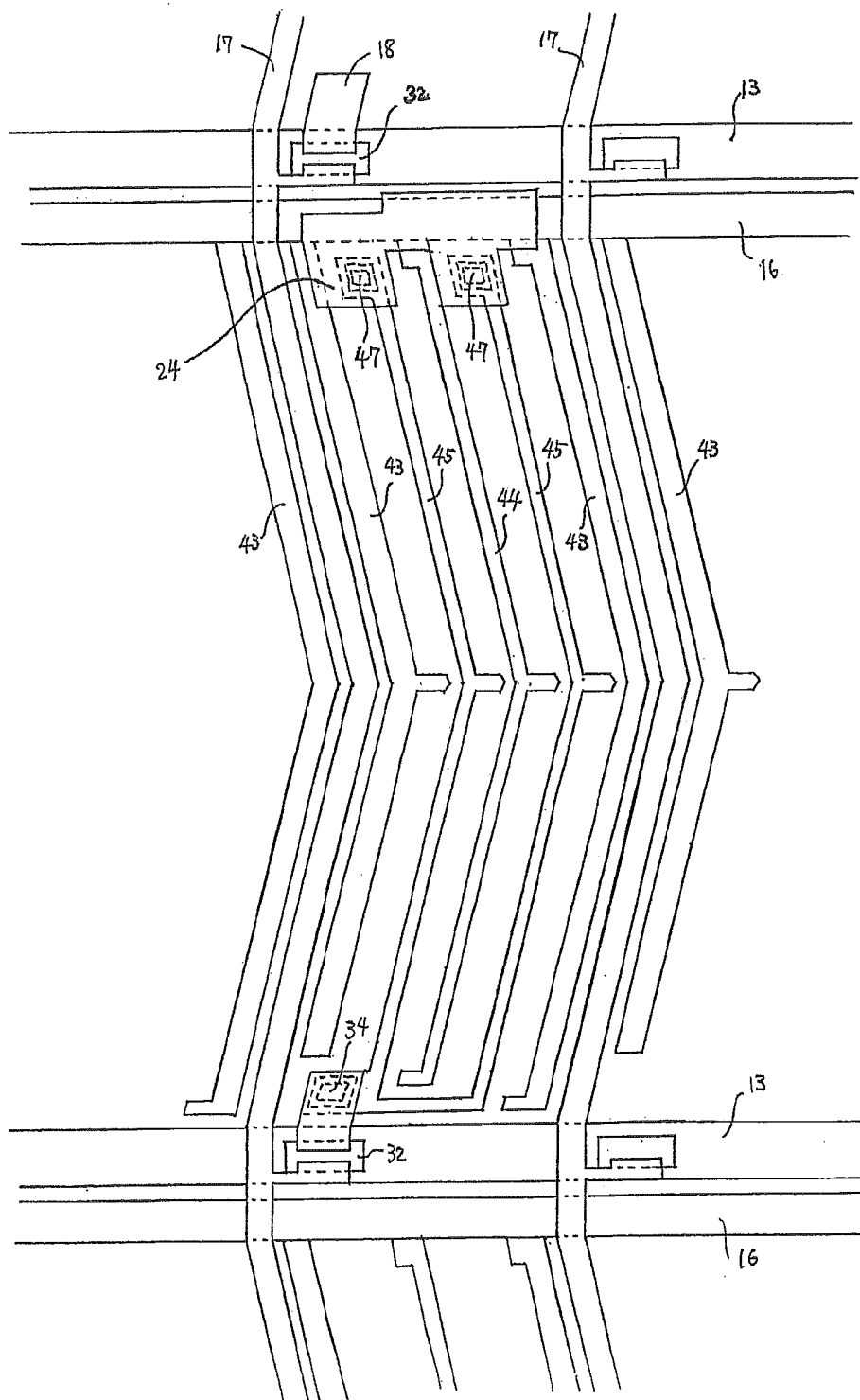


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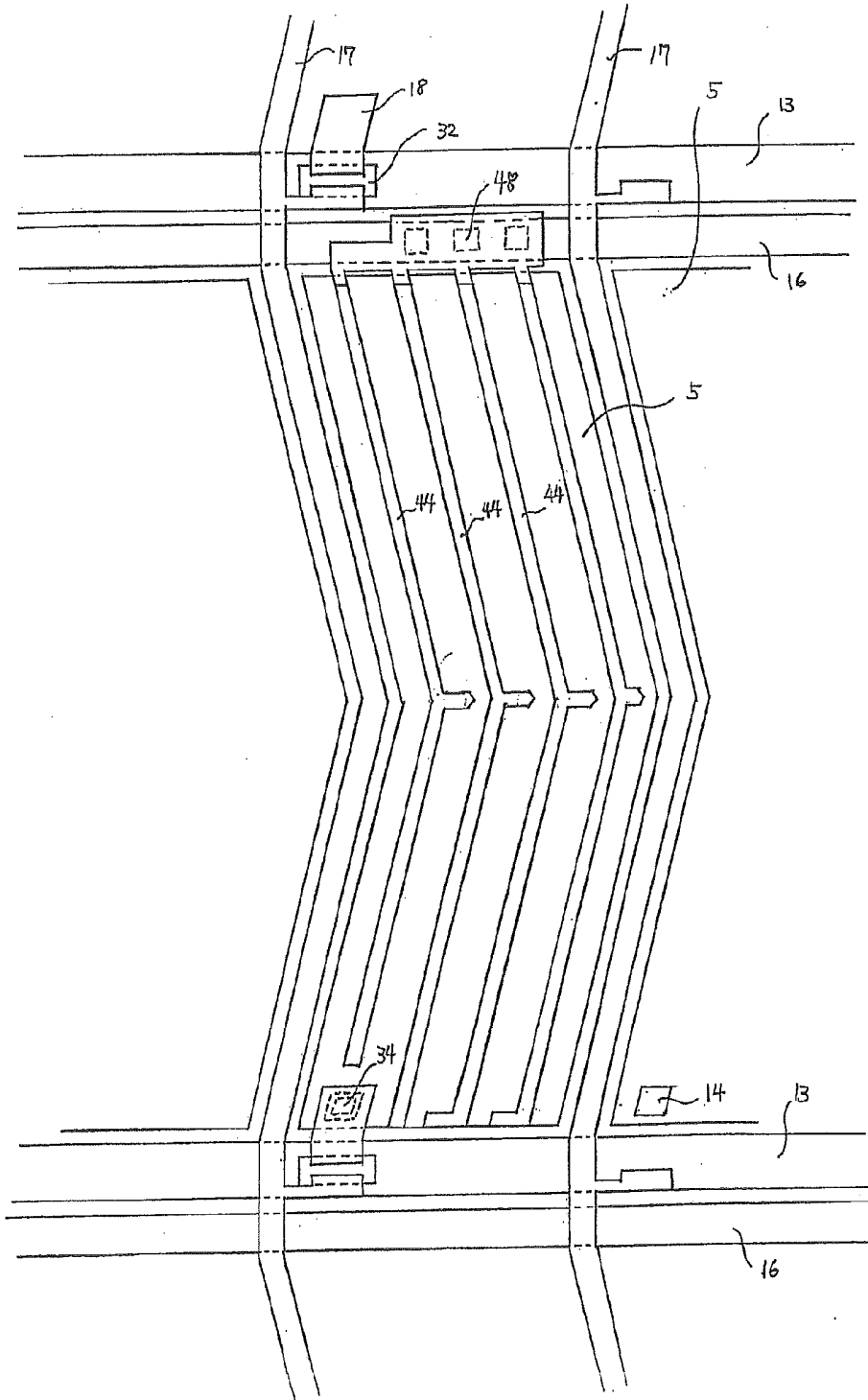


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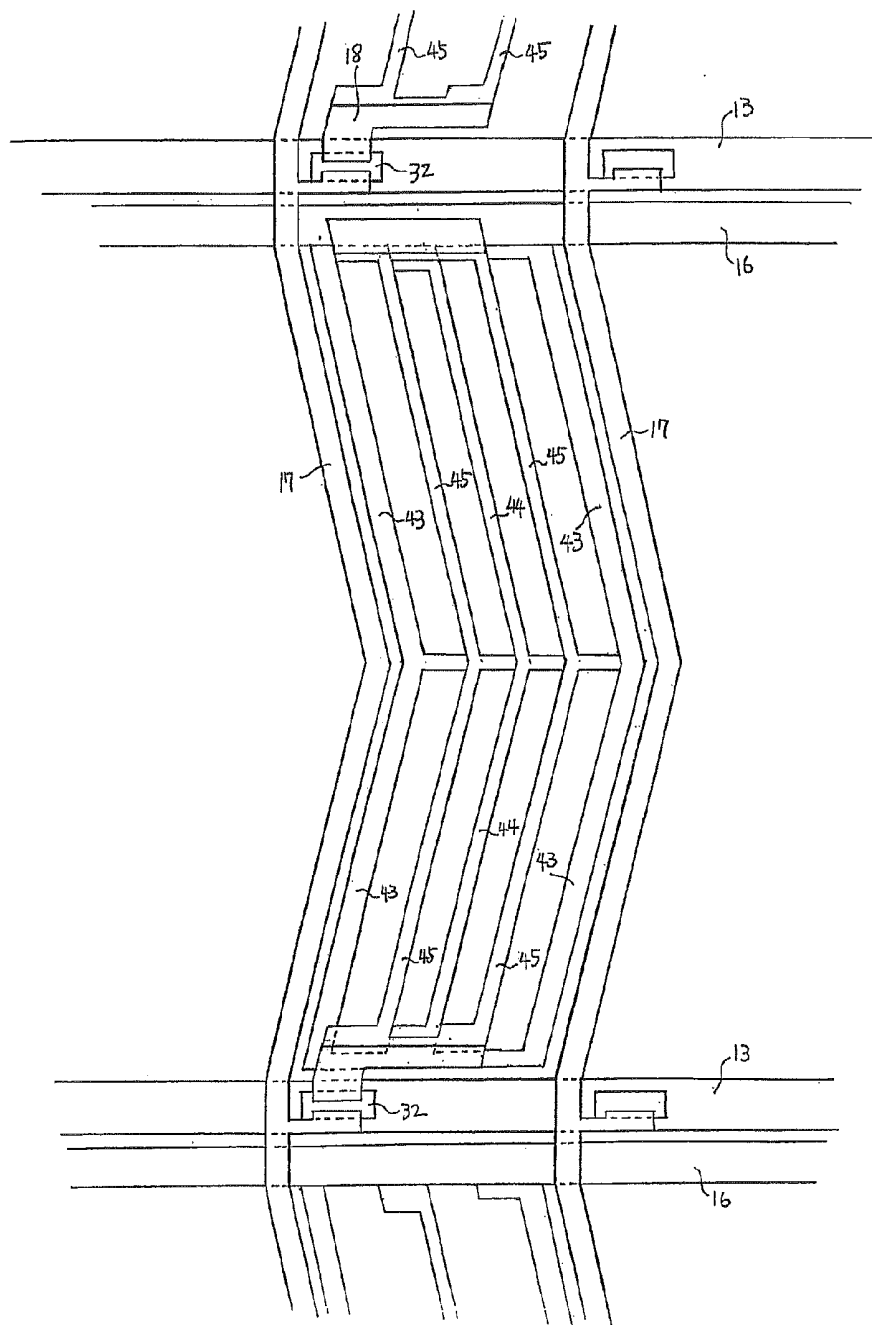


Fig. 51

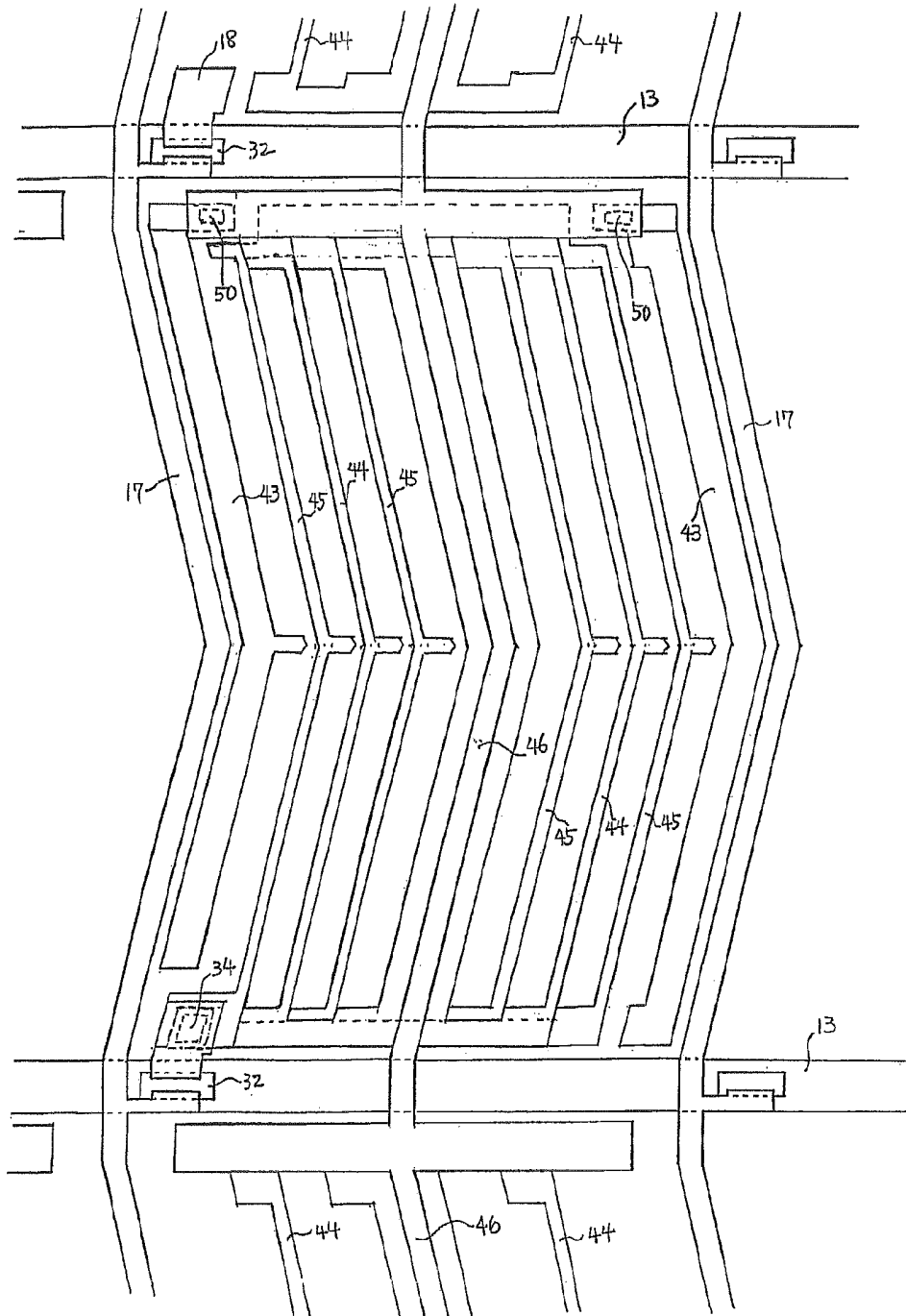


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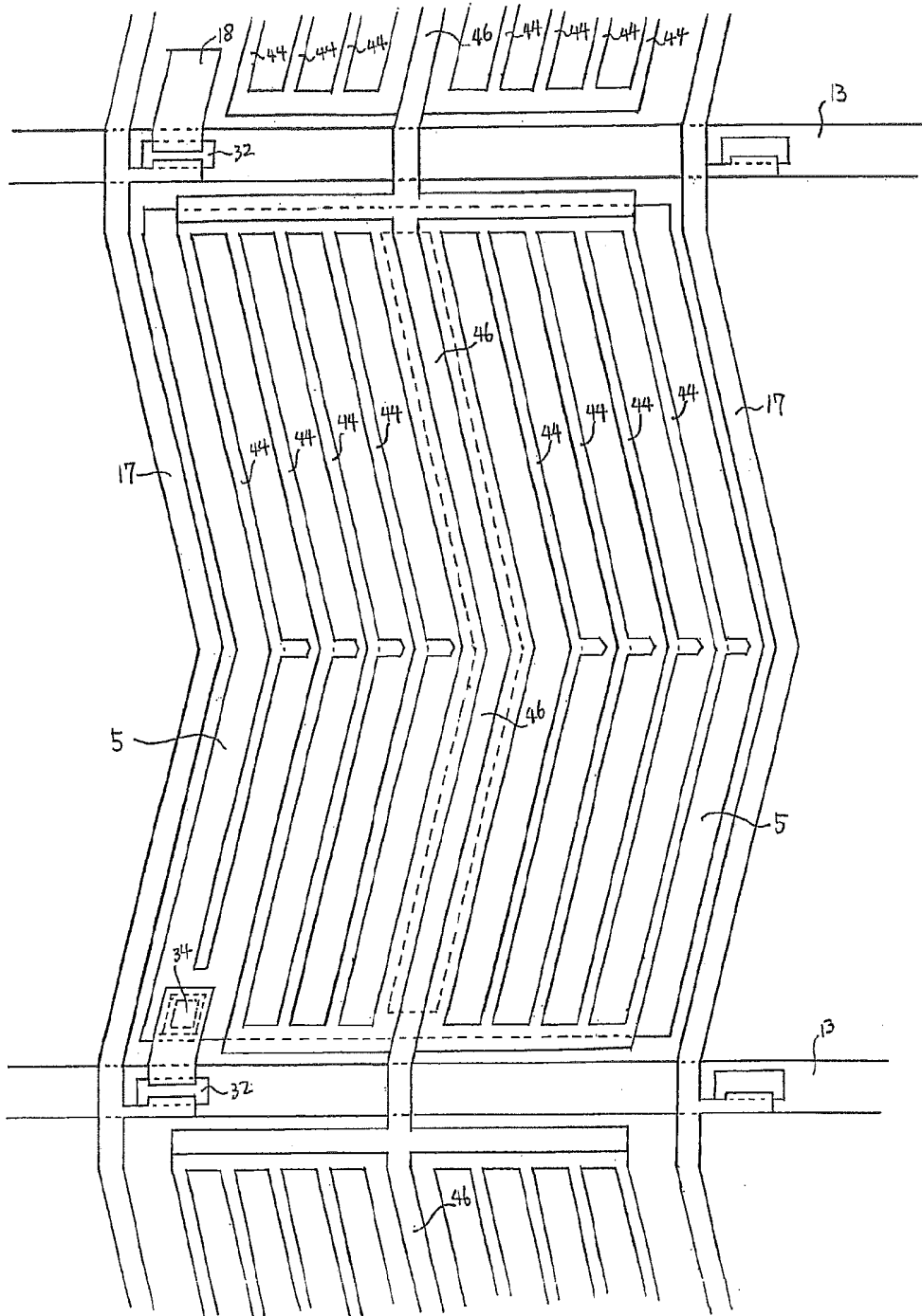


Fig. 54

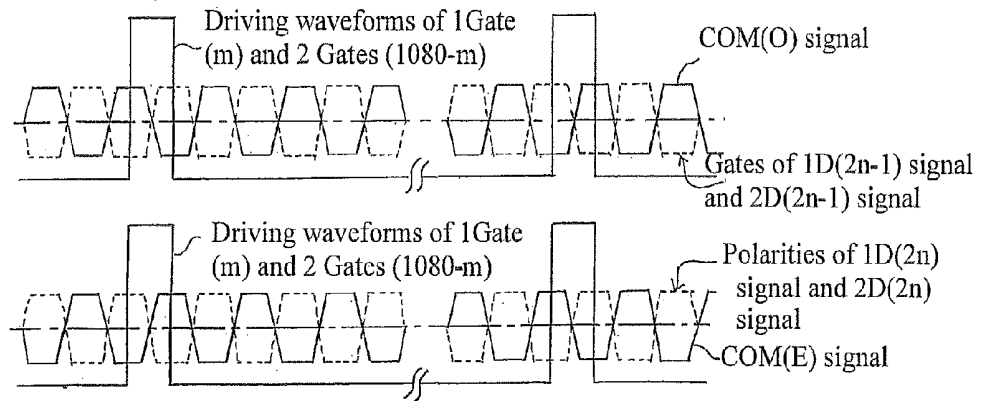


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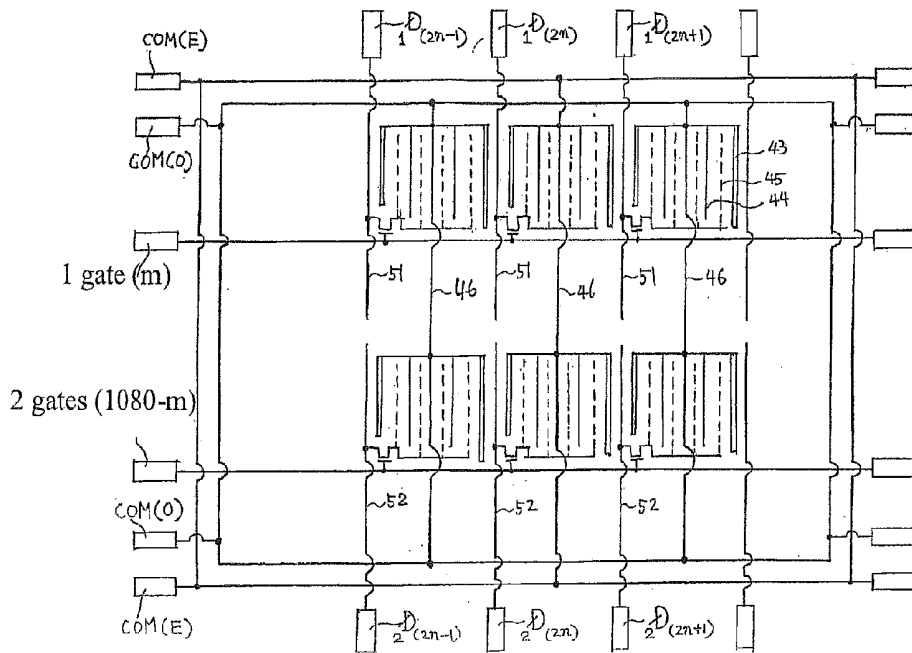


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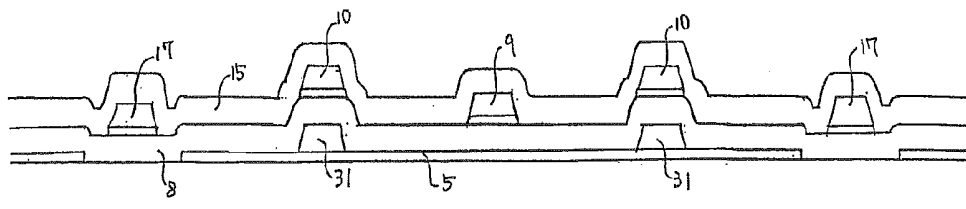


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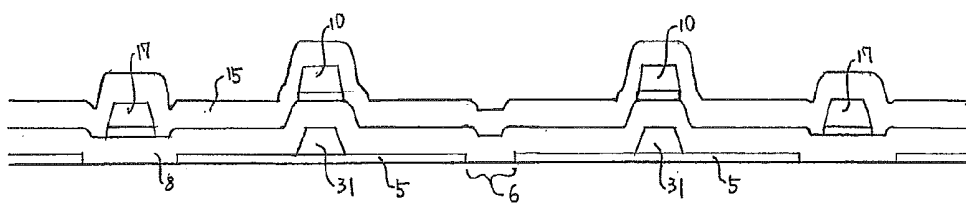


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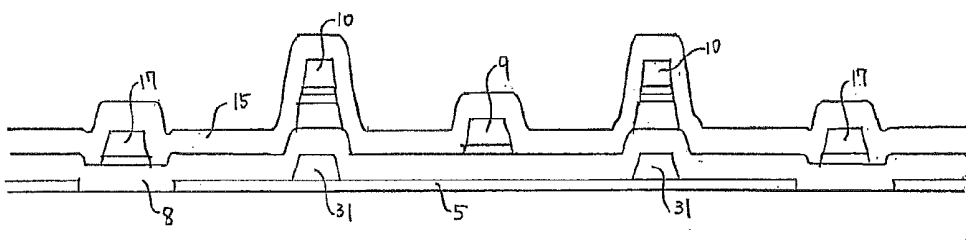


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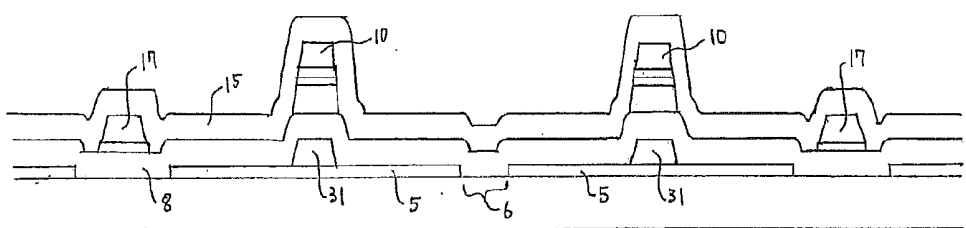
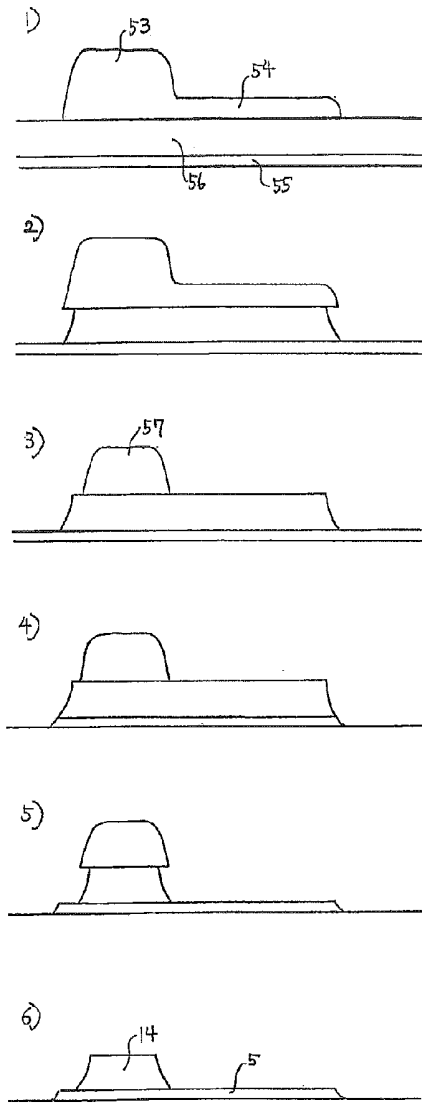
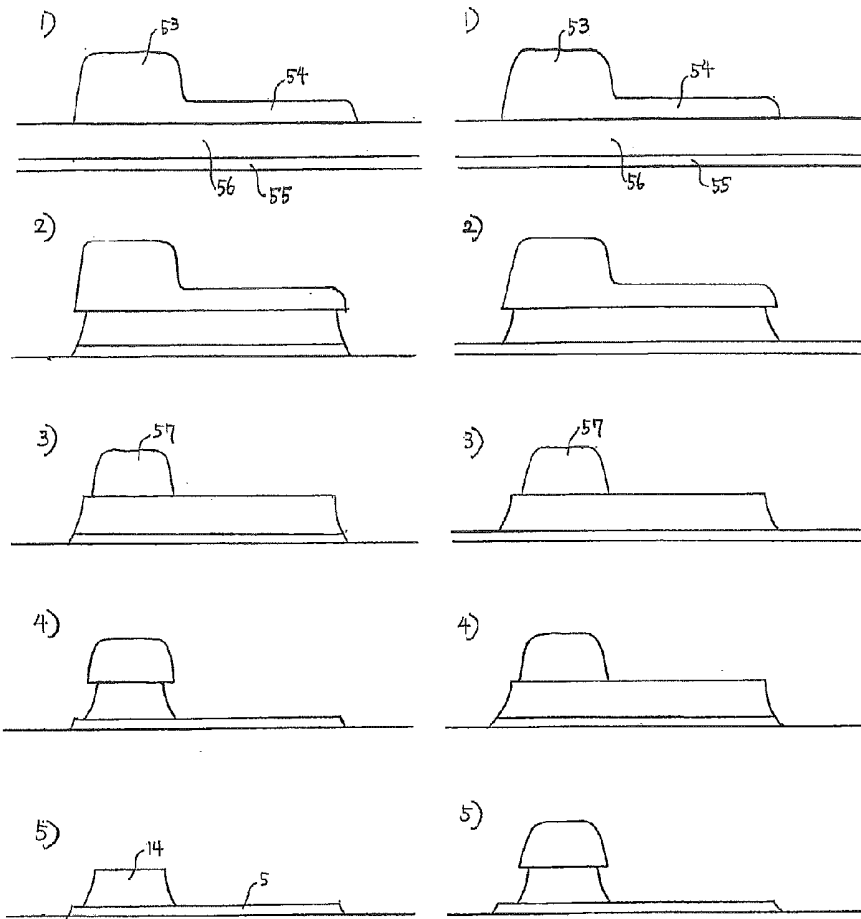


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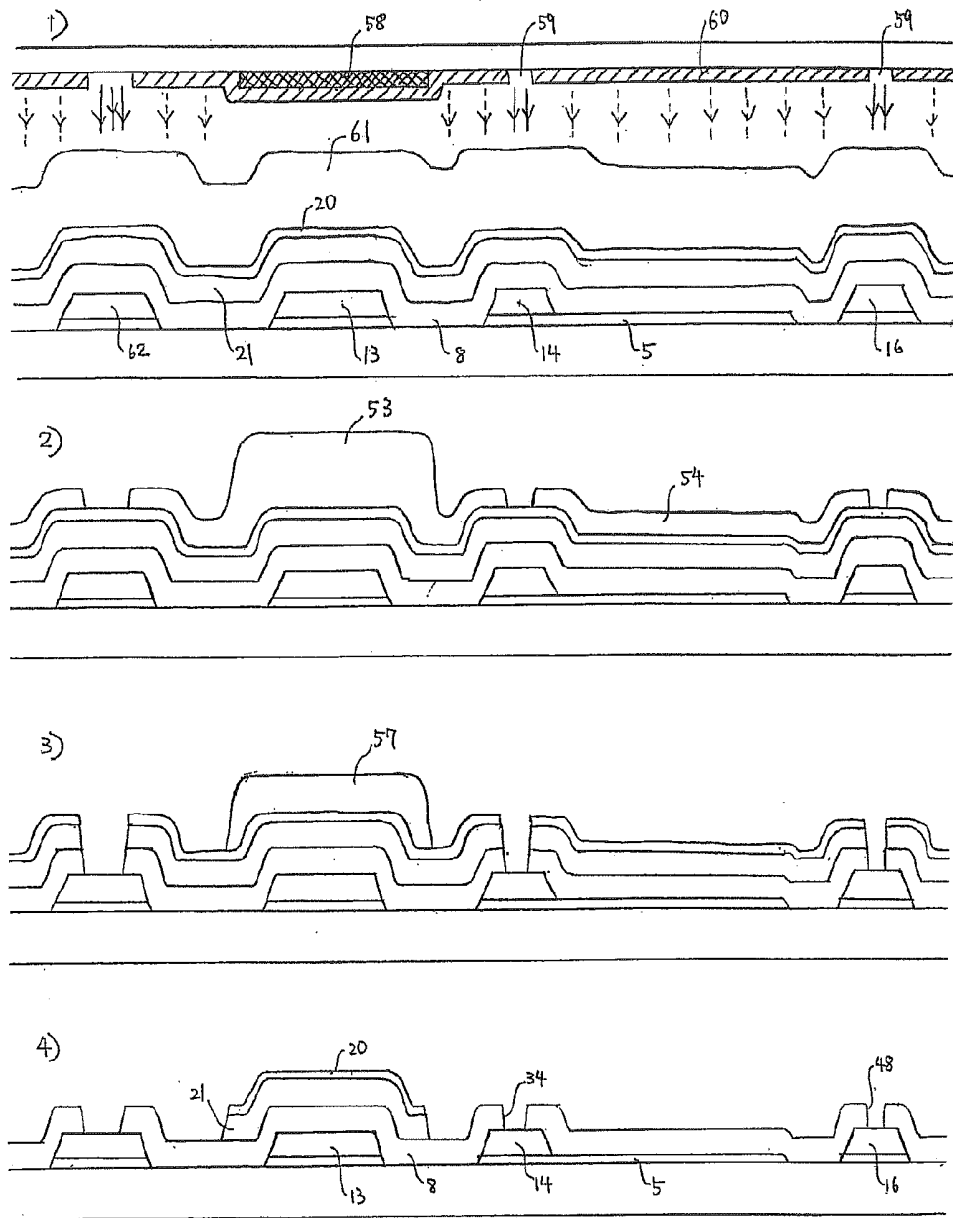


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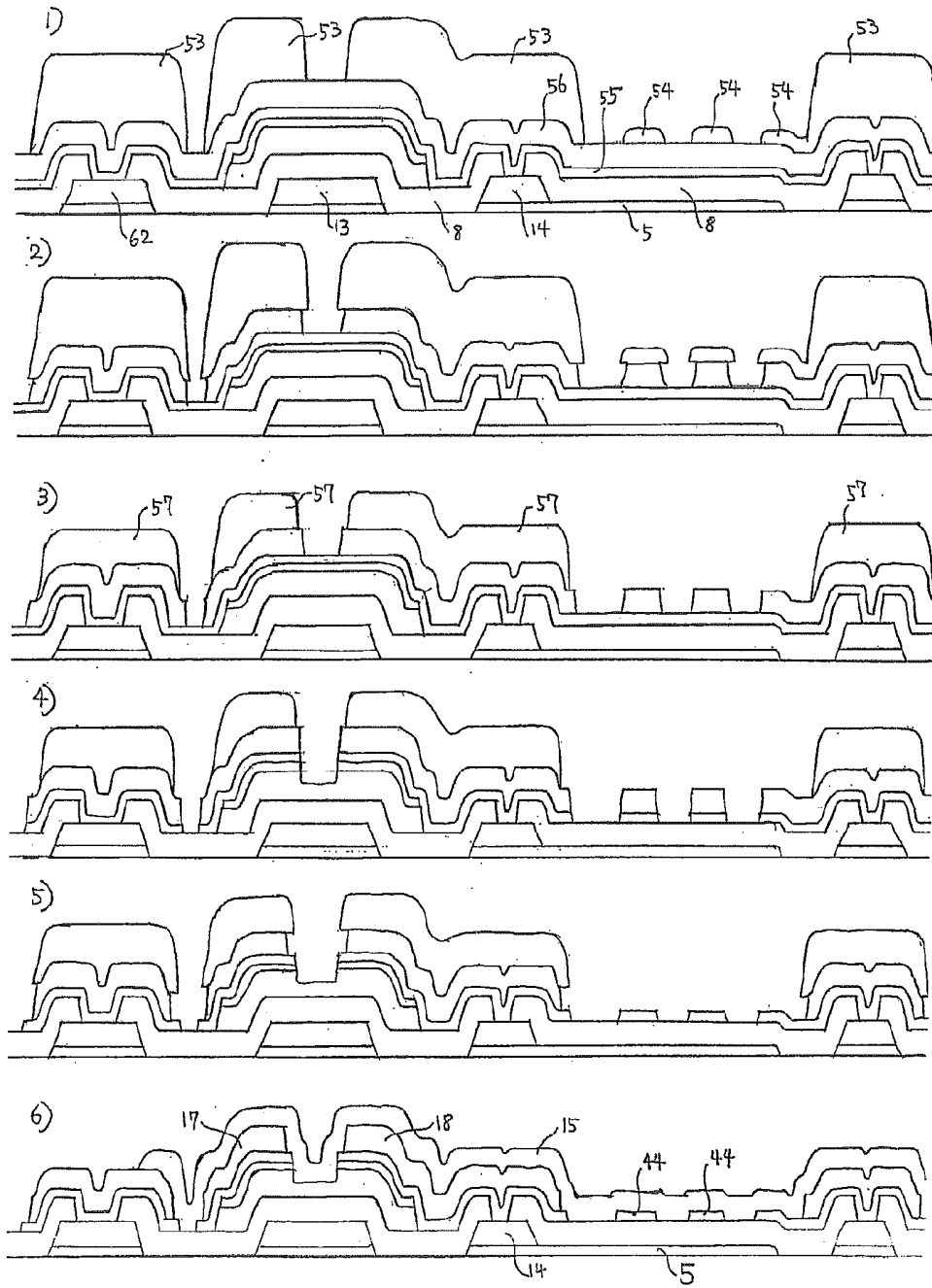


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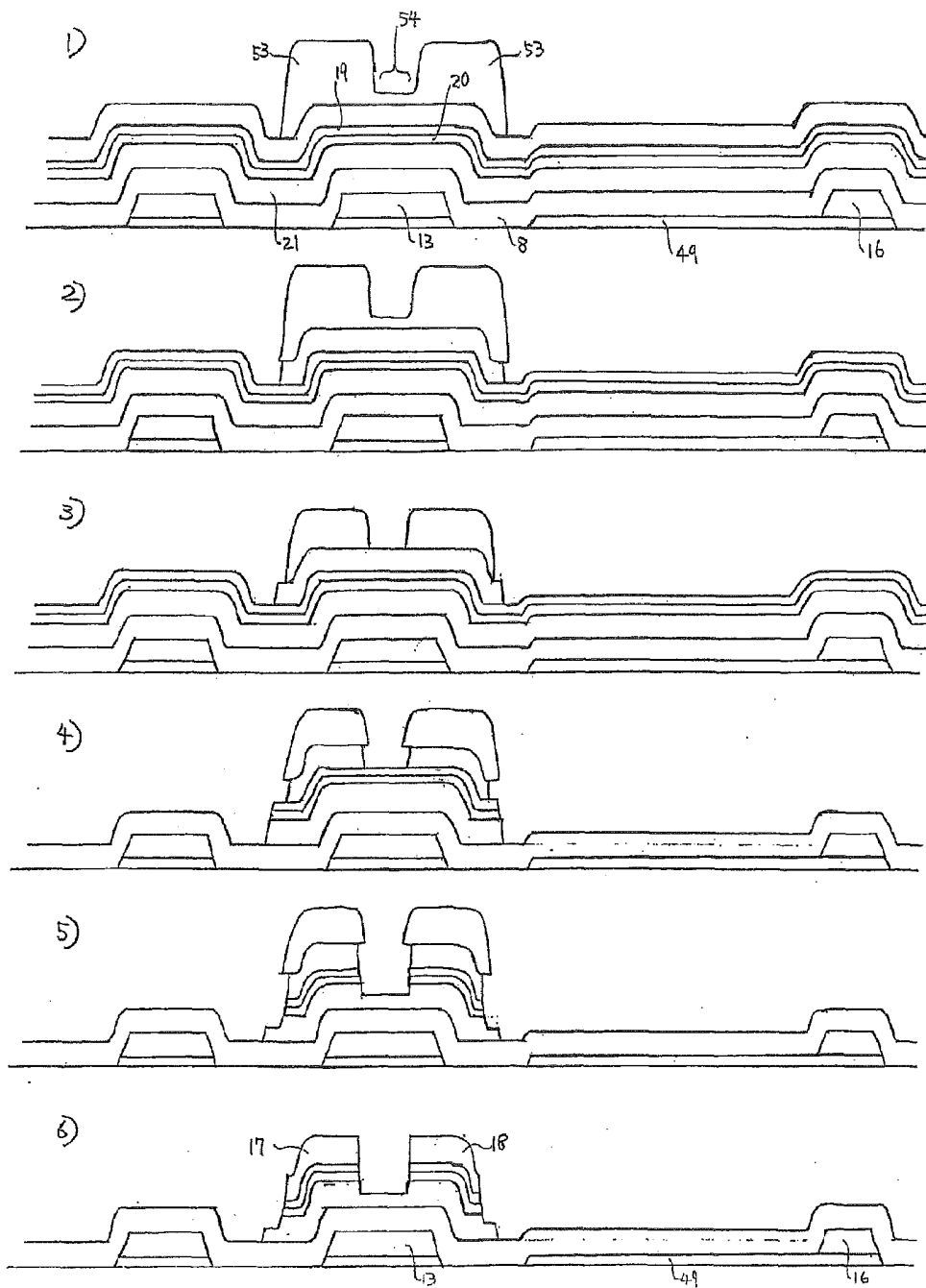


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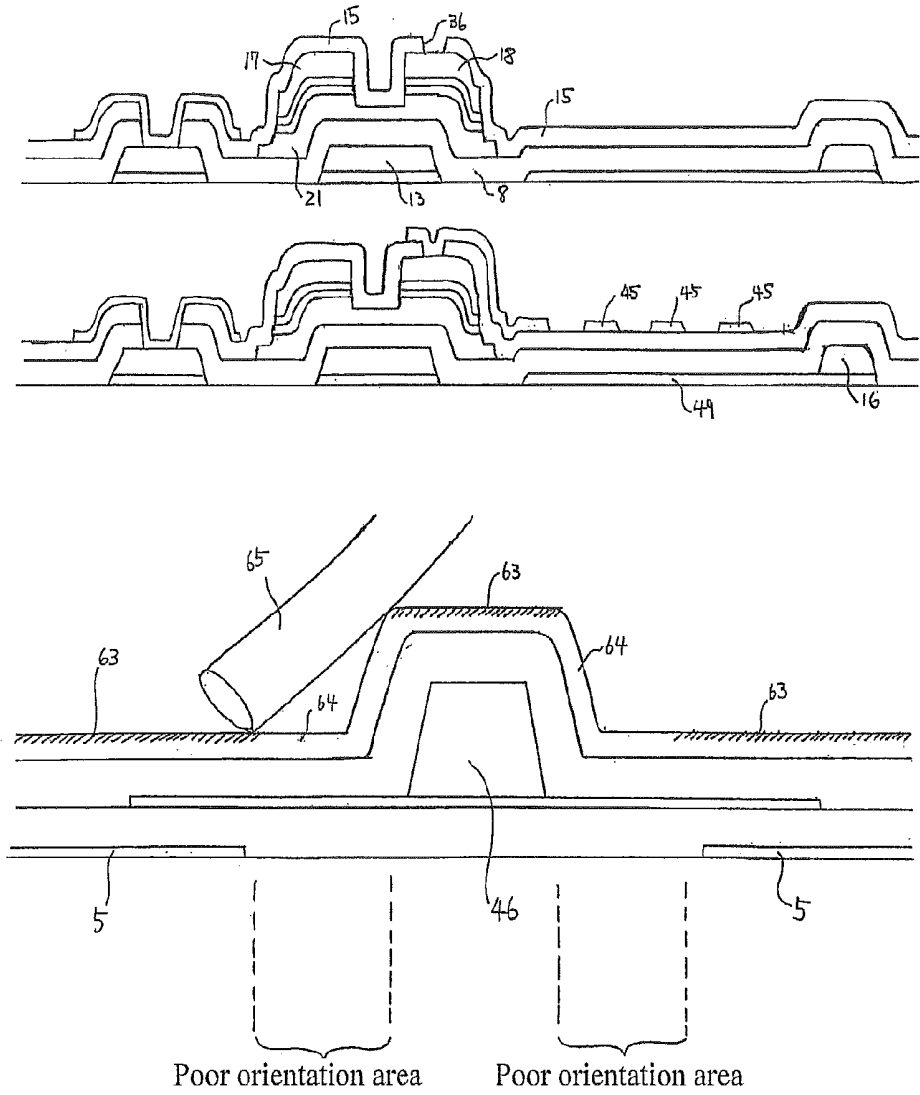


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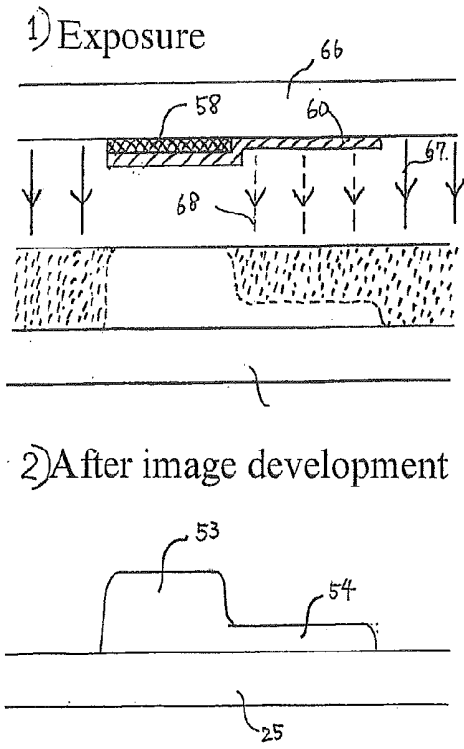


Fig. 67

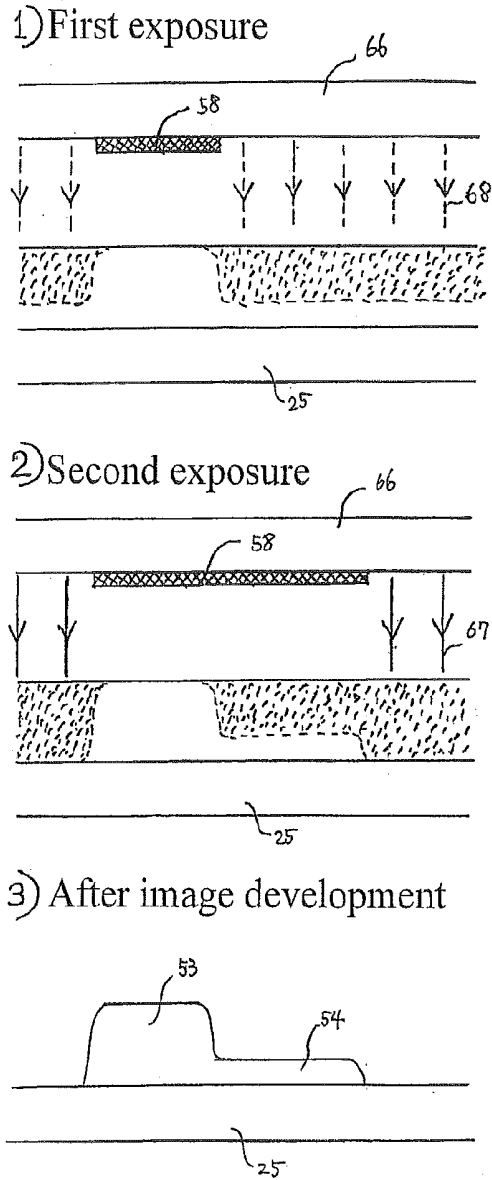


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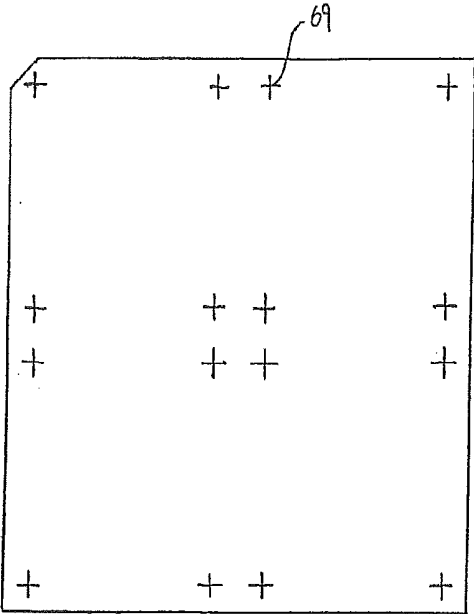


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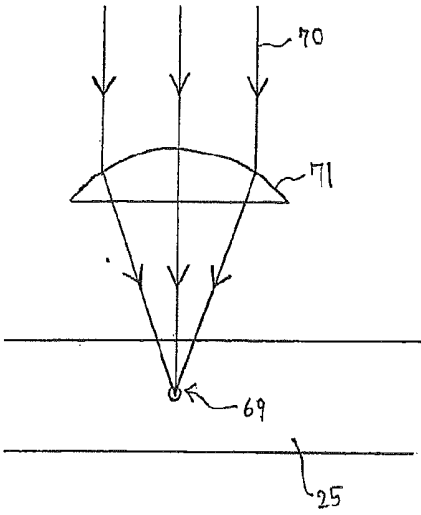


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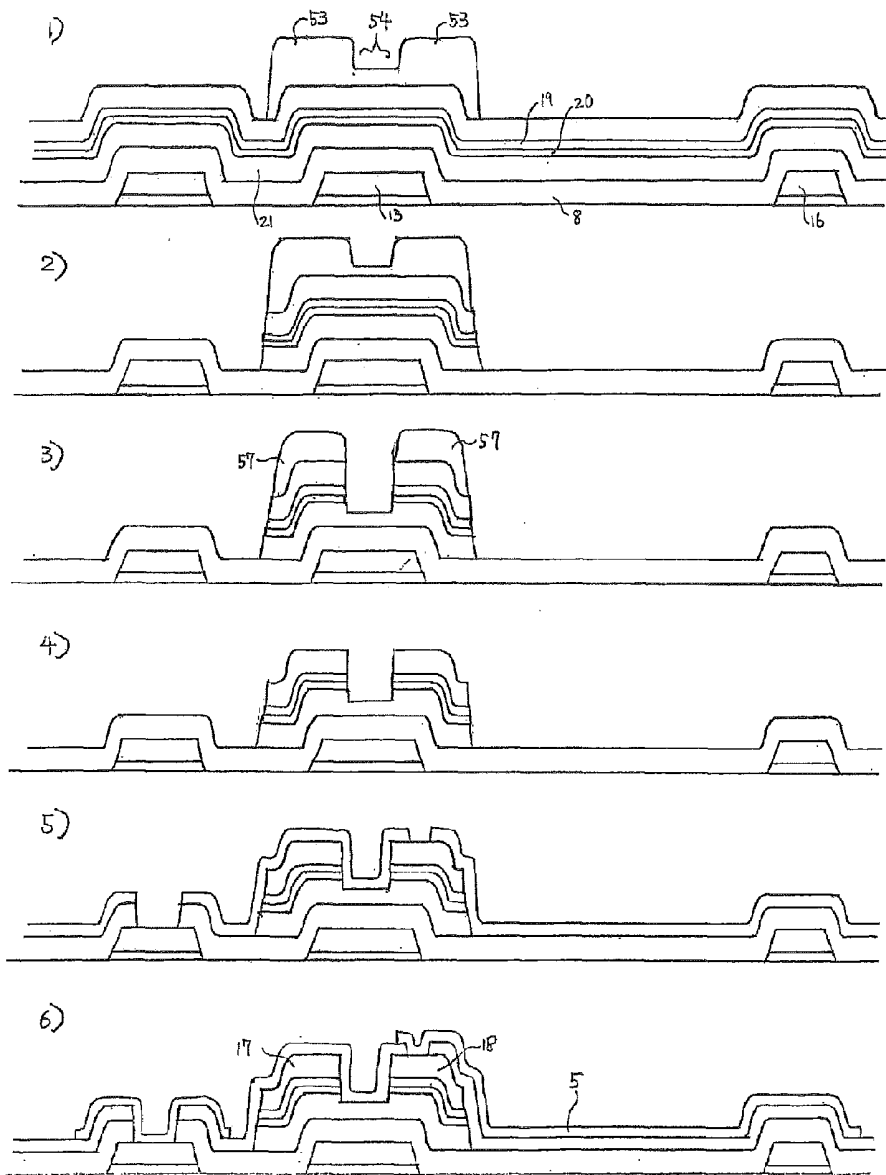


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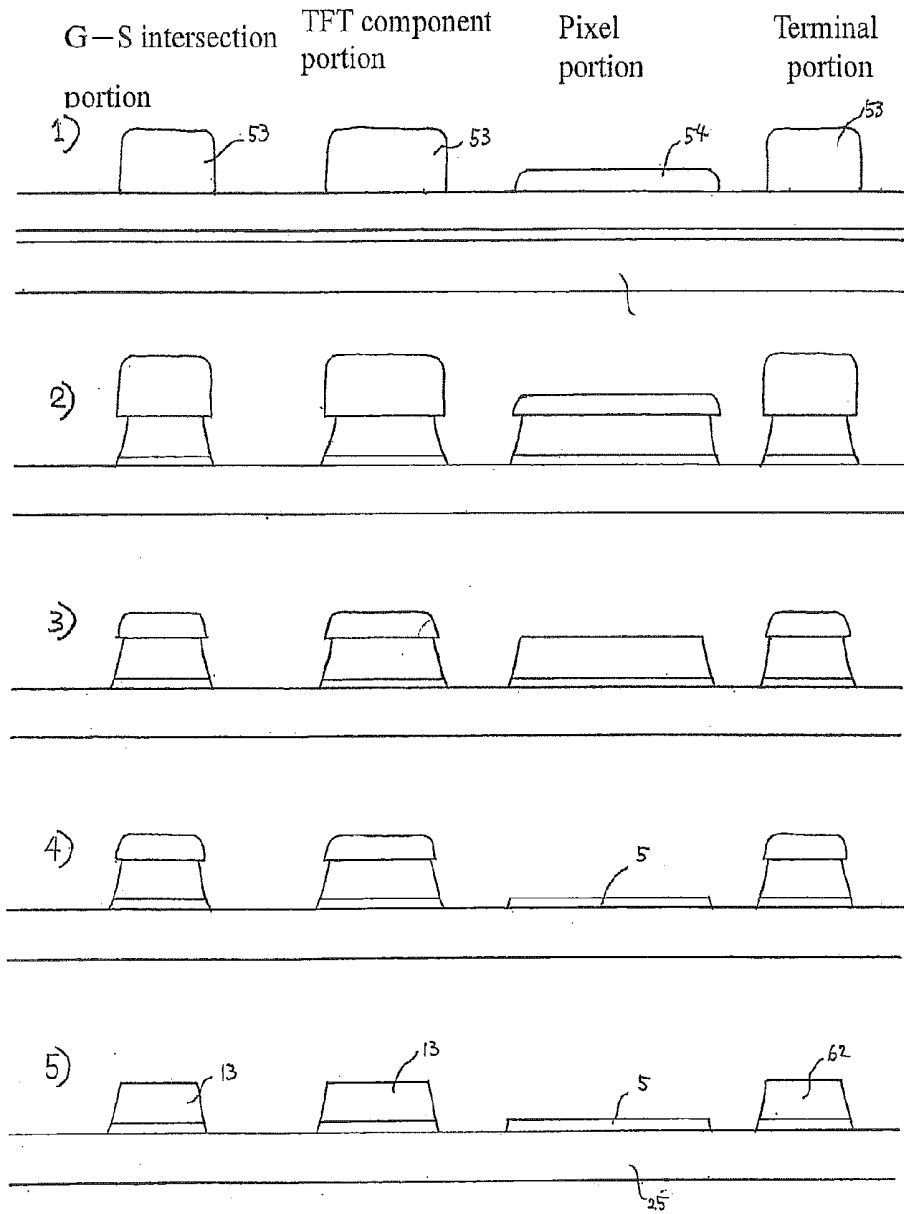


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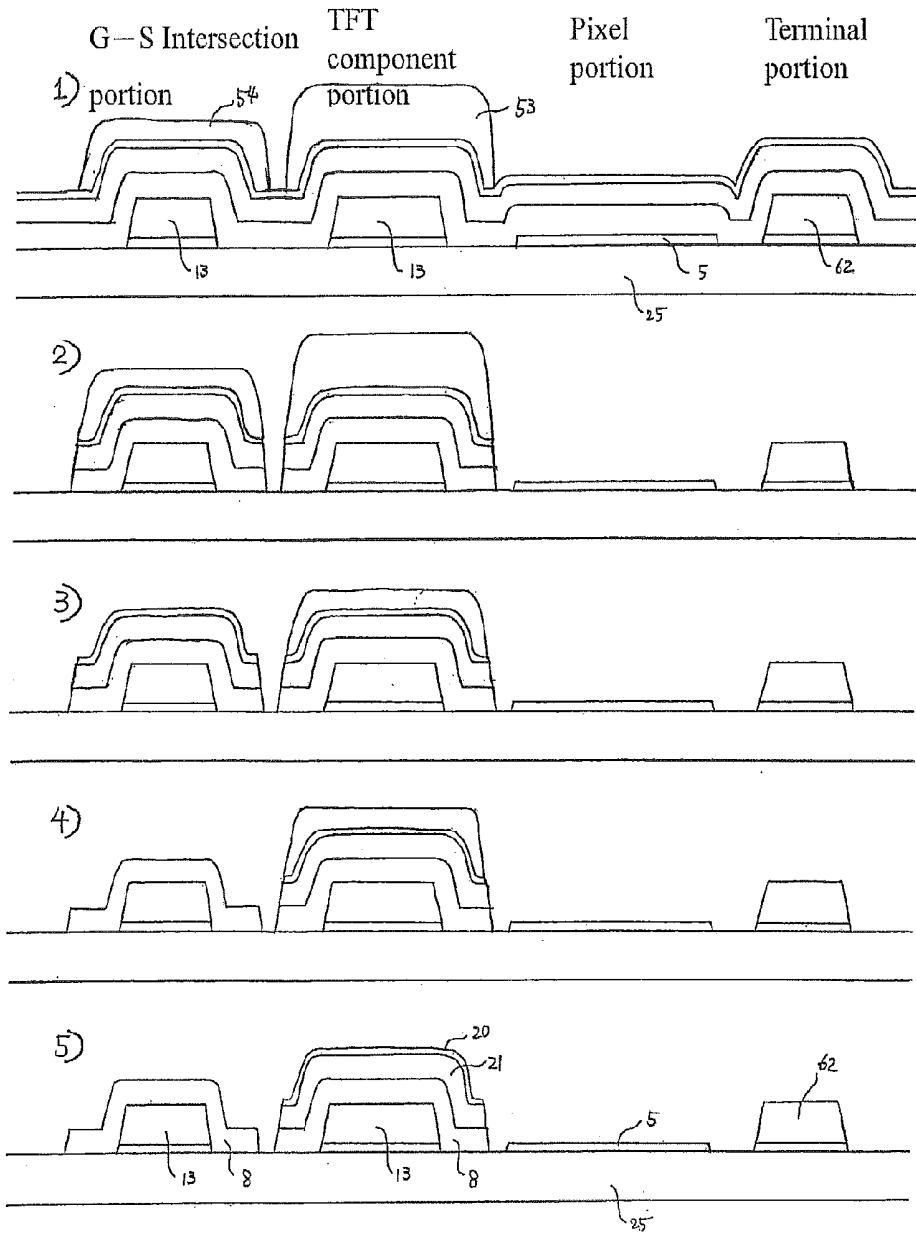


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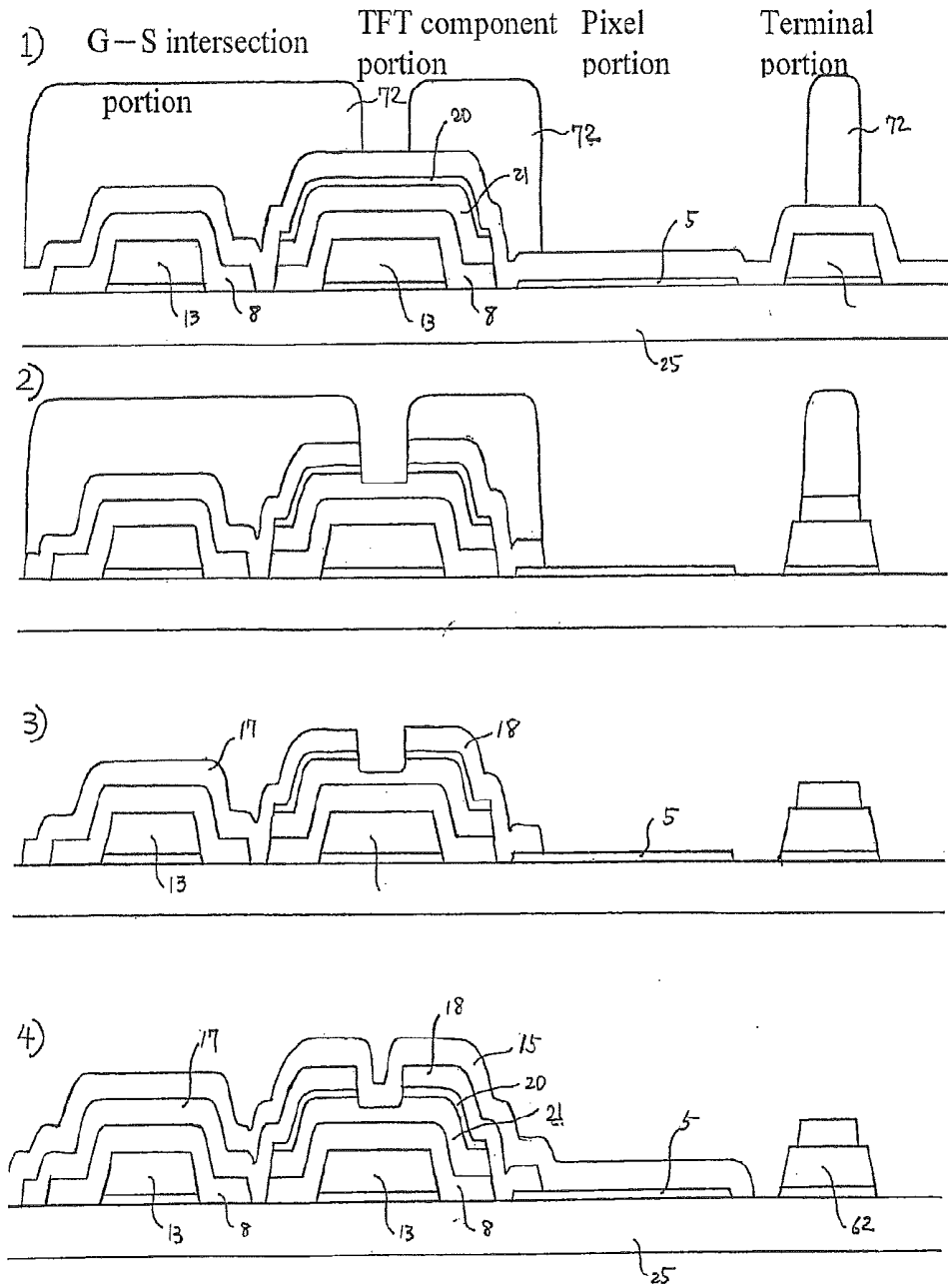


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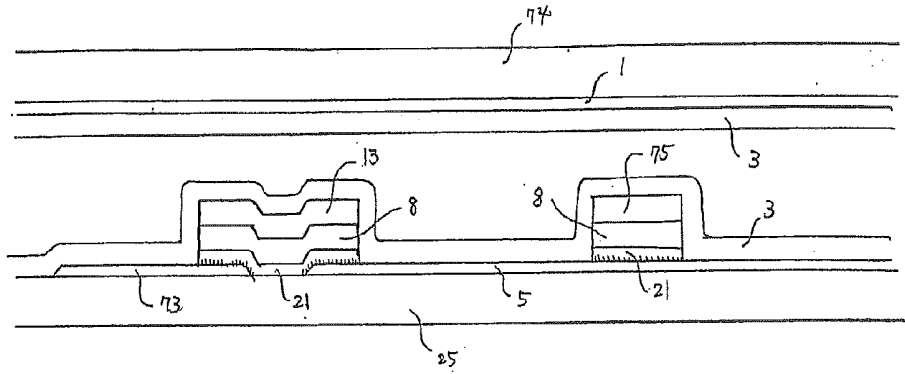


Fig. 75
(Prior Art)

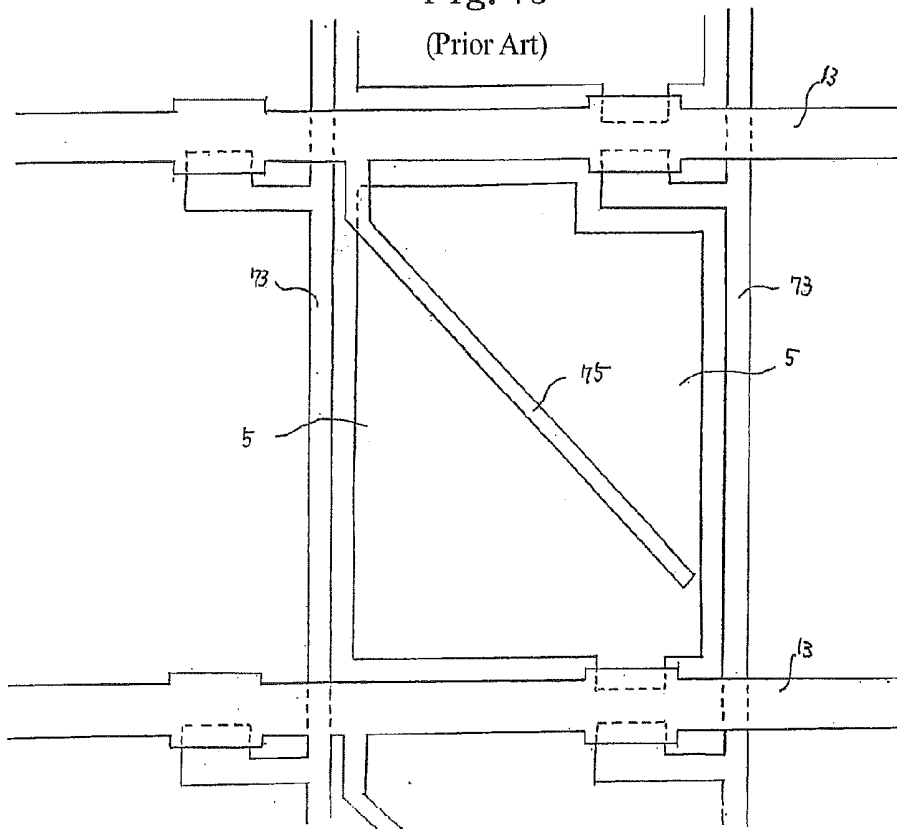


Fig. 76
(Prior Art)

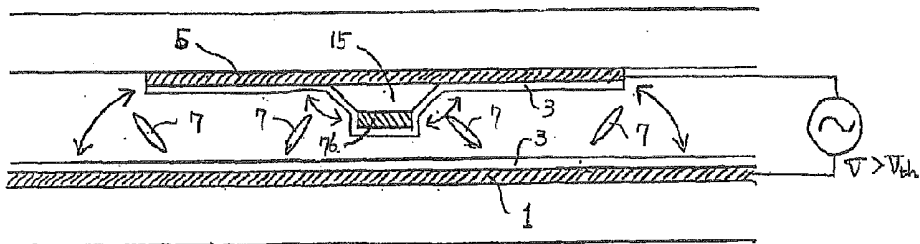


Fig. 77
(Prior Art)

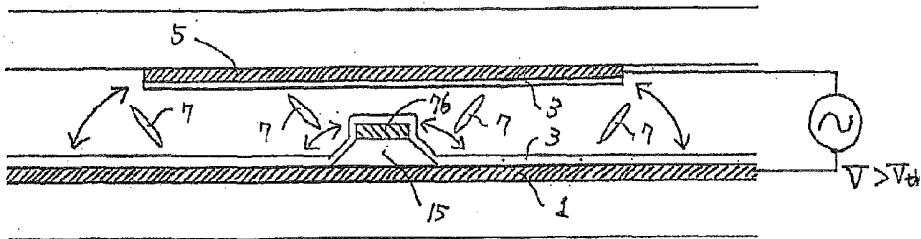


Fig. 78
(Prior Art)

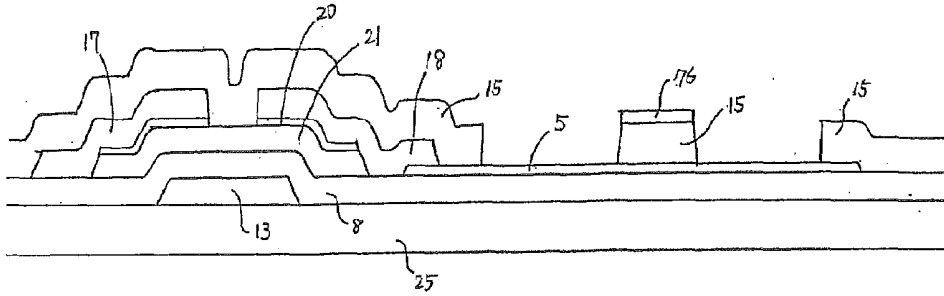


Fig. 79

(Prior Art)

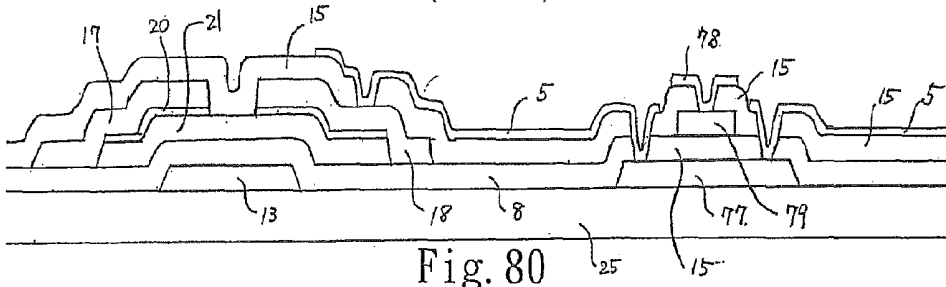


Fig. 80

(Prior Art)

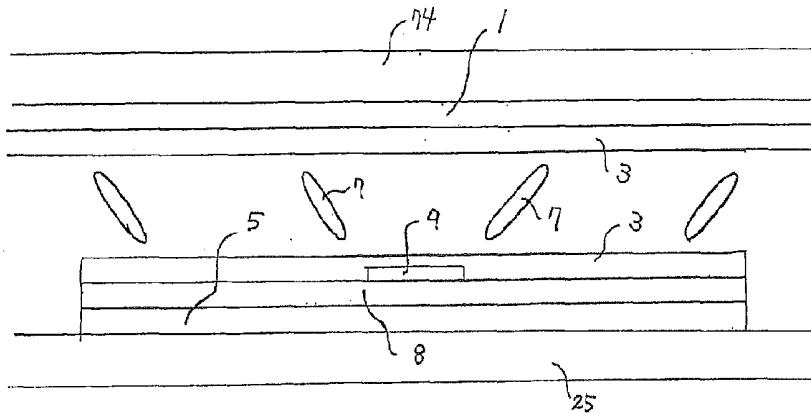


Fig. 81

(Prior Art)

Fig. 82

MVA Mode Using a Photolithographic Procedure for Three Times (A)

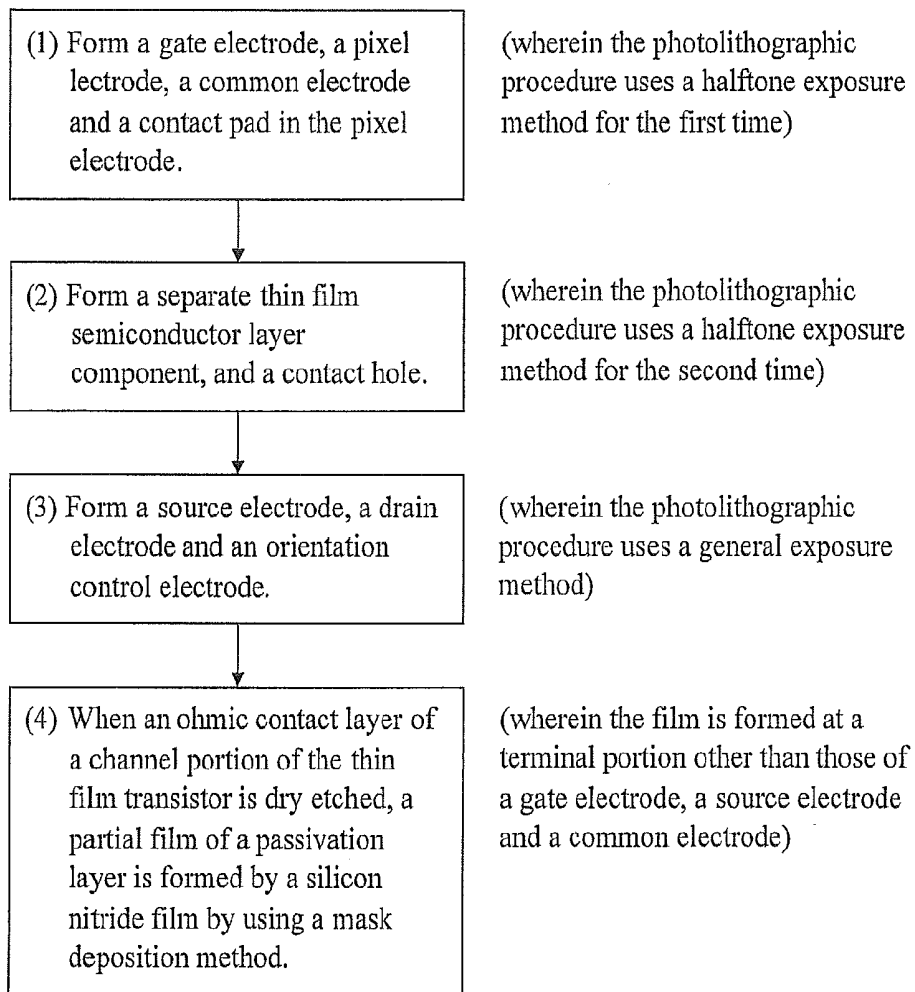


Fig. 83

MVA Mode Using a Photolithographic Procedure for Three Times (B)

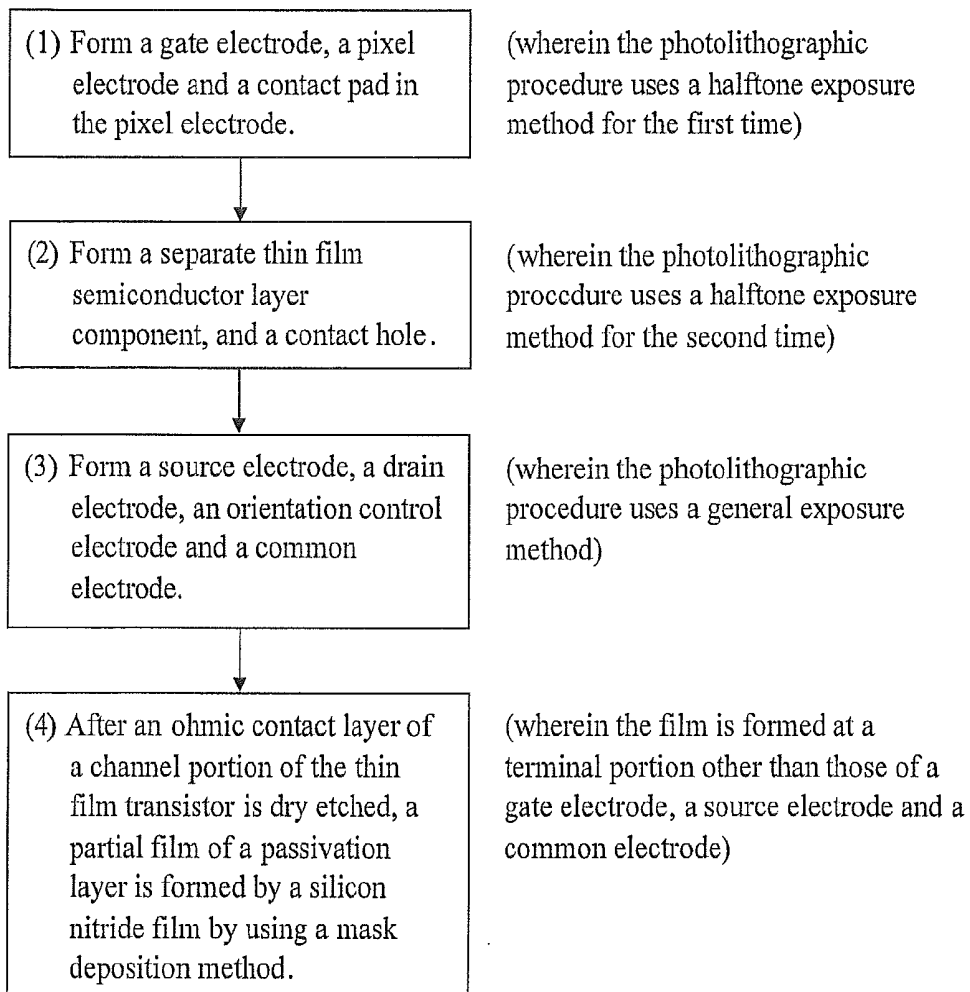


Fig. 84
IPS Mode Using a Photolithographic Procedure for Three Times (C)

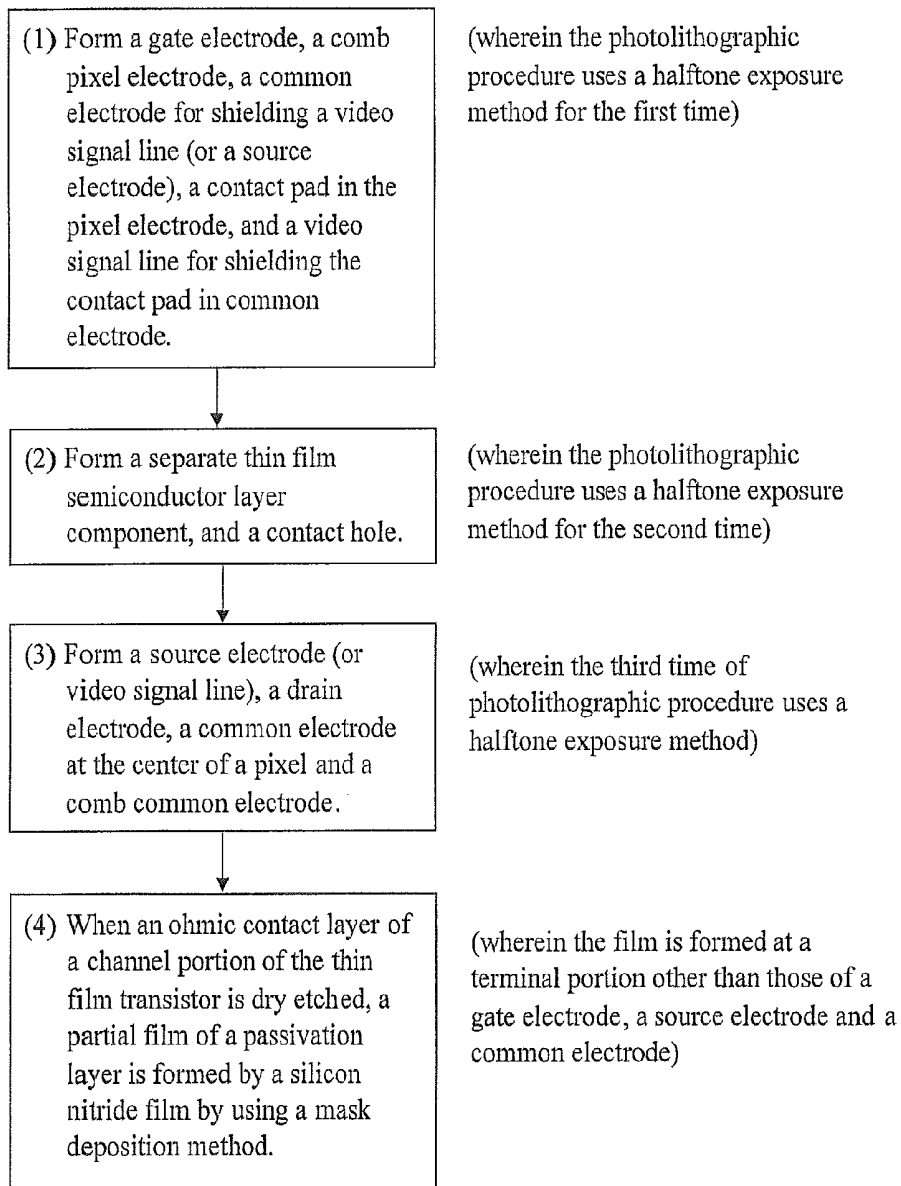
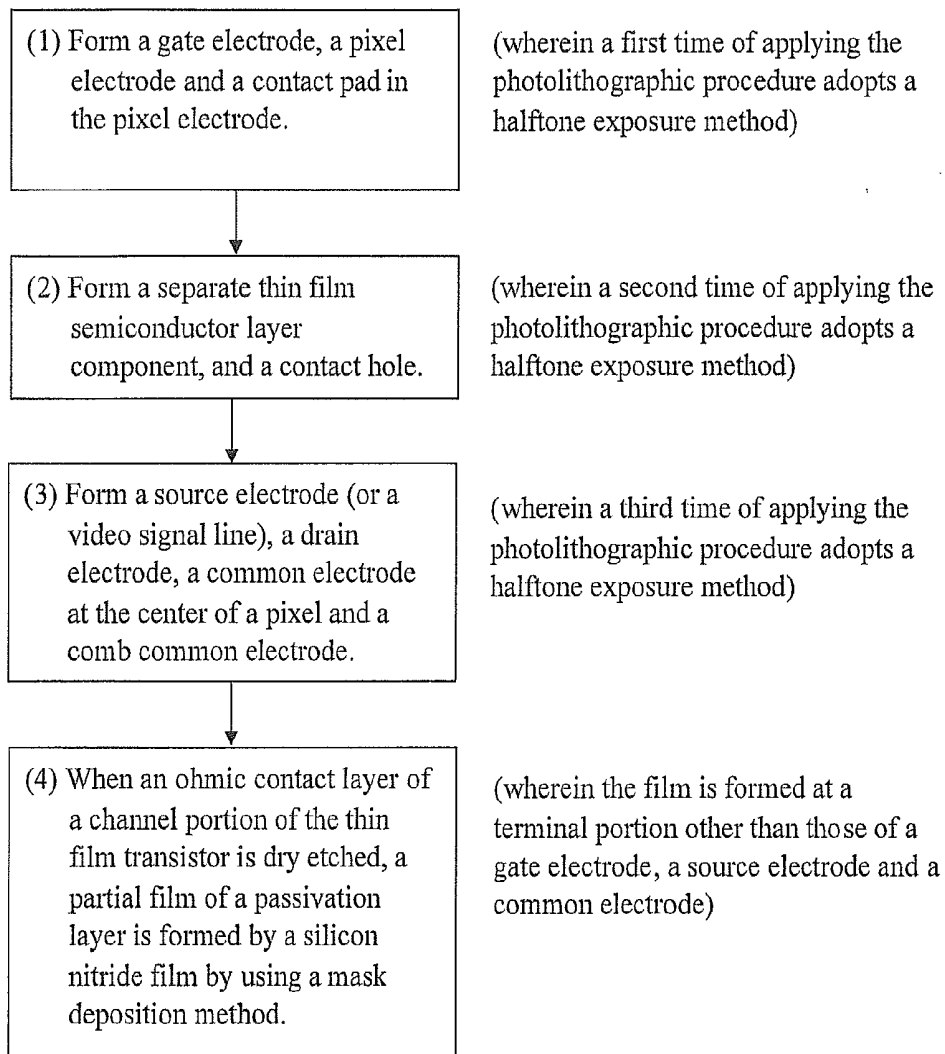


Fig. 85

FFS Mode Using a Photolithographic Procedure for Three Times (D)



**LOW-COST LARGE-SCREEN WIDE-ANGLE
FAST-RESPONSE LIQUID CRYSTAL DISPLAY
APPARATUS**

RELATED APPLICATIONS

[0001] This application is a divisional application claiming priority to Ser. No. 11/743,749, filed on May 3, 2007.

FIELD OF THE INVENTION

[0002] The present invention relates to a large-screen wide-angle liquid crystal display apparatus manufactured by using a halftone exposure method.

BACKGROUND OF THE INVENTION

[0003] In multi-domain vertical alignment (MVA) liquid crystal display apparatuses, an orientation control electrode for controlling an alignment of a liquid crystal molecule has been disclosed in Japan Laid Open Patents Nos. 07-230097, 11-109393 and 2001-042347.

SUMMARY OF THE INVENTION

[0004] In view of the shortcomings of the prior art, the inventor of the present invention based on years of experience in the related industry to conduct researches and experiments, and finally developed a large-screen wide-angle liquid crystal display apparatus in accordance with the present invention to overcome the foregoing shortcomings.

[0005] Therefore, it is a primary objective of the present invention to adopt a prior art orientation control electrode of an LCD panel structure to correspond to smaller pixels. Since only one type of orientation control electrode is used only, and the edge field effect of a pixel electrode is adopted, therefore it is not applicable for larger pixels.

[0006] At present, the mainstream of multi-domain vertical alignment (MVA) liquid crystal display apparatus generally uses a bump or slit electrode for the alignment control of the sides of a color filter (CF) substrate, and this method can make a proper alignment if the pixel is large, but the cost of CF substrates is high, and becomes an obstacle for manufacturing a large-screen liquid crystal TV by a low cost.

[0007] Therefore, it is a primary objective of the present invention to reduce the number of photolithographic procedures of the TFT active matrix substrate and the CF substrate during the manufacture of the TFT active matrix liquid crystal display apparatus, in order to shorten the manufacturing procedure, lowering the manufacturing cost, and improving the yield rate.

[0008] The technical measures taken by the present invention are described as follows.

[0009] In Measure 1, unstable and swinging discrimination lines are avoided, and two types of orientation control electrodes are installed at an upper layer of a pixel electrode through an insulating film, and between common electrodes corresponding to the pixel electrodes. With the foregoing two different types of orientation control electrodes, the oblique direction of anisotropic liquid crystal molecules having a negative dielectric constant can be controlled precisely.

[0010] In Measure 2, one type of orientation control electrode is installed at an upper layer of a pixel electrode through an insulating film, and a slender slit is formed in the pixel electrode, and these two alignment control mechanisms can control the oblique direction of anisotropic liquid crystal molecules having a negative dielectric constant precisely.

[0011] In Measure 3, the orientation control electrodes as used in Measures 1 and 2 is connected to the pixel electrodes as closer to the substrate as possible.

[0012] In Measure 4, the alignment control mechanisms as used in Measures 1 and 2 provides four perfect area alignments for a curvature of 90 degrees at a position proximate to the center of the pixel.

[0013] In Measure 5, a halftone exposure method is introduced into the manufacturing process of the TFT array substrate to reduce the number of photolithographic procedures.

[0014] In Measure 6, a basic unit pixel is divided into two sub pixels, and the common electrodes are installed parallelly on a video signal line, and the common electrodes of odd-numbered rows and even-numbered rows switch signals with different polarities in each scan period, and produce different voltages applied to the liquid crystal molecules of the two sub pixels.

[0015] With Measures 1 and 2, the TFT array substrate has all alignment control functions, and thus it is not necessary to form a pad or slit on the CF substrate for the alignment control, so that the MVA LCD panel can be manufactured with a low-cost CF substrate to lower the cost and improve the yield rate.

[0016] With Measure 3, the orientation control electrode connected to the pixel electrode is proximate to the substrate for enhancing the rotational torque of an electric field of anisotropic liquid crystal molecules having negative dielectric constant and acted at the vertical alignment, so as to achieve a high-speed response.

[0017] With Measure 4, unnecessary discrimination lines can be avoided to improve the overall light transmission rate of the screen and reduce unevenness of the LCD panel.

[0018] With Measures 1, 2 and 5, the processing costs for both CF substrate and TFT array substrate can be lowered, and thus the manufacturing cost of MVA LCD panels can be lowered significantly; the production efficiency can be improved, and the yield rate can be enhanced.

[0019] With Measures 5 and 6, the liquid crystal alignment control mechanism can be manufactured by a very simple manufacturing process, and the correction of γ curve can be achieved by a very simple circuit, and thus a little cost is incurred for enhancing the display quality of a MVA liquid crystal display apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 is a cross-sectional view of a conventional MVA LCD panel;

[0021] FIG. 2 is a cross-sectional view of a conventional MVA LCD panel;

[0022] FIG. 3 is a cross-sectional view of a MVA LCD panel of the present invention;

[0023] FIG. 4 is a cross-sectional view of a MVA LCD panel of the present invention;

[0024] FIG. 5 is a schematic view of the principle of a MVA LCD panel of the present invention;

[0025] FIG. 6 is a schematic view of the principle of a MVA LCD panel of the present invention;

[0026] FIG. 7 is a schematic view of the principle of a MVA LCD panel of the present invention;

[0027] FIG. 8 is a cross-sectional view of a MVA LCD panel adopting a TFT matrix substrate in accordance with the present invention;

[0028] FIG. 9 is a cross-sectional view of a TFT array substrate used for a MVA LCD panel in accordance with the present invention;

[0029] FIG. 10 is a cross-sectional view of a TFT array substrate used for a MVA LCD panel in accordance with the present invention;

[0030] FIG. 11 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0031] FIG. 12 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0032] FIG. 13 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0033] FIG. 14 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0034] FIG. 15 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0035] FIG. 16 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0036] FIG. 17 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0037] FIG. 18 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0038] FIG. 19 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0039] FIG. 20 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0040] FIG. 21 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0041] FIG. 22 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0042] FIG. 23 is a cross-sectional view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0043] FIG. 24 is a planar view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0044] FIG. 25 is a planar view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0045] FIG. 26 is a planar view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0046] FIG. 27 is a planar view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0047] FIG. 28 is a planar view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0048] FIG. 29 is a planar view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0049] FIG. 30 is a planar view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0050] FIG. 31 is a planar view of a TFT array substrate used in a MVA LCD panel in accordance with the present invention;

[0051] FIG. 32 shows a circuit model of a TFT array substrate of field-order driven MVA LCD panel in accordance with the present invention;

[0052] FIG. 33 shows a relation between the brightness and the signal voltage applied to a MVA LCD panel as depicted in FIG. 32;

[0053] FIG. 34 is a waveform diagram of a MVA LCD panel as depicted in FIG. 21;

[0054] FIG. 35 shows a circuit model of a TFT array substrate that is divided into upper and lower field-order driven MVA LCD panels in accordance with the present invention;

[0055] FIG. 36 illustrates a field-order driving method that divides a screen into upper and lower sections and writes data from the center of the screen to the upper or lower section of the screen in accordance with the present invention;

[0056] FIG. 37 illustrates a field-order driving method that divides a screen into upper and lower sections and writes data from the upper or lower sections of the screen towards the center of the screen in accordance with the present invention;

[0057] FIG. 38 illustrates a field-order driving method that divides a screen into upper and lower sections and writes data from the center of the screen to the upper or lower section of the screen in accordance with the present invention;

[0058] FIG. 39 illustrates a field-order driving method that divides a screen into upper and lower sections and writes data from the upper or lower sections of the screen towards the center of the screen in accordance with the present invention;

[0059] FIG. 40 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0060] FIG. 41 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0061] FIG. 42 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0062] FIG. 43 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0063] FIG. 44 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0064] FIG. 45 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0065] FIG. 46 shows a circuit model of a circuit of a TFT array substrate of a field-order driven horizontal electric field LCD panel in accordance with the present invention;

[0066] FIG. 47 is a cross-sectional view of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0067] FIG. 48 is a cross-sectional view of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0068] FIG. 49 is a planar view of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0069] FIG. 50 is a planar view of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0070] FIG. 51 is a planar view of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0071] FIG. 52 is a planar view of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0072] FIG. 53 is a planar view of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0073] FIG. 54 is a planar view of a TFT array substrate of a horizontal electric field LCD panel in accordance with the present invention;

[0074] FIG. 55 is a waveform diagram of a horizontal electric field LCD panel as depicted in FIG. 54;

[0075] FIG. 56 shows a circuit model of a TFT array substrate of a field-order driven horizontal electric field LCD panel that divides a display screen into upper and lower sections in accordance with the present invention;

[0076] FIG. 57 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a MVA LCD panel in accordance with the present invention;

[0077] FIG. 58 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a MVA LCD panel in accordance with the present invention;

[0078] FIG. 59 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a MVA LCD panel in accordance with the present invention;

[0079] FIG. 60 is a cross-sectional view of a basic unit pixel of a TFT array substrate of a MVA LCD panel in accordance with the present invention;

[0080] FIG. 61 is a cross-sectional view of a manufacturing flow that adopts a halftone exposure method to form a contact pad for a pixel electrode in accordance with the present invention;

[0081] FIG. 62 is a cross-sectional view of a manufacturing flow that adopts a halftone exposure method to form a contact pad for a pixel electrode in accordance with the present invention;

[0082] FIG. 63 is a cross-sectional view of a manufacturing flow that adopts a halftone exposure method to give an island effect to a semiconductor layer of a thin film transistor component and form a contact hole in accordance with the present invention;

[0083] FIG. 64 is a cross-sectional view of a manufacturing flow that forms a source electrode, a drain electrode, a terminal electrode, and comb common electrode in accordance with the present invention;

[0084] FIG. 65 is a cross-sectional view of a flow of manufacturing a thin film transistor substrate by a halftone exposure method in accordance with the present invention;

[0085] FIG. 66 illustrates the structure of a horizontal electric field active matrix substrate at a center pixel common electrode of the center of a basic unit pixel;

[0086] FIG. 67 illustrates a masking principle of a halftone exposure applied in the present invention;

[0087] FIG. 68 illustrates the principle of a halftone multiple exposure method applied in the present invention;

[0088] FIG. 69 illustrates a first photolithographic procedure that needs to align at a mark when using a halftone multiple exposure method in accordance with the present invention;

[0089] FIG. 70 illustrates the principle of aligning with a mark by a halftone multiple exposure method that uses a pulse laser in a glass substrate in accordance with the present invention;

[0090] FIG. 71 is a cross-sectional view of a manufacturing flow of using a halftone exposure method to form a thin film transistor substrate in accordance with the present invention;

[0091] FIG. 72 is a cross-sectional view of a manufacturing flow of using a halftone exposure method to form a scan line portion, a pixel electrode and a terminal portion of a thin film transistor substrate in accordance with the present invention;

[0092] FIG. 73 shows a cross-sectional view of a manufacturing flow of using a halftone exposure method to give an island effect to a semiconductor layer of a thin film transistor component and expose a pixel electrode and a terminal portion completely;

[0093] FIG. 74 shows a cross-sectional view of a manufacturing flow before forming a source electrode and a drain electrode in the process of manufacturing a thin film transistor component as illustrated in FIGS. 73 and 74;

[0094] FIG. 75 is cross-sectional view of the structure forming a TFT array substrate of an orientation control electrode connected to a scan line and disposed on the previously formed pixel electrode;

[0095] FIG. 76 is a planar view of a TFT array substrate as depicted in FIG. 75;

[0096] FIG. 77 is a cross-sectional view of forming a vertical alignment cell of one type of orientation control electrode connected to a common electrode and disposed on the previously formed pixel electrode;

[0097] FIG. 78 is a cross-sectional view of a vertical alignment cell of one type of orientation control electrode connected to a pixel electrode and disposed on the previously formed plate electrode;

[0098] FIG. 79 is a cross-sectional view of a structure of forming only one type of orientation control electrode on a pixel electrode of the previously formed TFT array substrate;

[0099] FIG. 80 is a cross-sectional view of a structure of forming only one type of orientation control electrode on a pixel electrode of the previously formed TFT array substrate;

[0100] FIG. 81 is a cross-sectional view of a structure of forming only one type of orientation control electrode on a pixel electrode of the previously formed TFT array substrate;

[0101] FIG. 82 illustrates a manufacturing flow of performing the photolithographic procedure for three times that uses a MVA TFT array substrate to apply a halftone exposure method for two times;

[0102] FIG. 83 illustrates a manufacturing flow of performing the photolithographic procedure for three times that uses a MVA TFT array substrate to apply a halftone exposure method for two times;

[0103] FIG. 84 illustrates a manufacturing flow of performing the photolithographic procedure for three times that uses an IPS TFT array substrate to apply a halftone exposure method for three times; and

[0104] FIG. 85 illustrates a manufacturing flow of performing the photolithographic procedure for three times that uses an IPS TFT array substrate to apply a halftone exposure method for three times.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0105] To make it easier for our examiner to understand the objective, innovative features and performance of the present

invention, we use a preferred embodiment and the accompanying drawings for a detailed description of the present invention.

[0106] Referring to FIGS. 1 and 2 for cross-sectional views of a current mainstream MVA LCD panel, a mechanism for controlling the direction of movements both is installed separately on upper and lower substrates to control the vertical alignment of anisotropic liquid crystal molecules of a negative dielectric constant. Since the discrimination line of an LCD panel using this method is constant without swinging, therefore uneven display rarely occurs, and LCD panels with high quality of display can be produced at a good yield rate. However, it is necessary to form a slit or a bump disposed on a lateral side of a CF substrate corresponding to a TFT substrate for the structure as shown in FIGS. 1 and 2 to control the liquid crystal alignment, and the production cost of the CF substrate is higher than that of the TN CF substrate. To lower the cost of the CF substrate, all liquid crystal alignment control functions are built in the TFT substrate side.

[0107] Referring to FIGS. 75 to 81 for an embodiment of a CF substrate side having no alignment control function as disclosed in the previous patents, these CF substrates cannot be used as large substrates. These prior arts can be used for small pixels only. Since an edge field effect of a pixel electrode is used, therefore these substrates are not appropriate for the large pixel electrodes used for the liquid crystal TV.

[0108] With the two basic structures as shown in FIGS. 3 and 4, a TFT substrate side has all of the liquid crystal alignment control functions. In the TFT substrate side as shown in FIG. 3, two different liquid crystal orientation control electrodes are installed between the common electrode of the substrate and corresponding to the pixel electrode to successfully form an equal-potential distribution as shown in FIG. 5. In FIG. 4, one type of orientation control electrode is installed on a pixel electrode at the TFT substrate side and between the slit for alignment control and the pixel electrode corresponding to the common electrode of the substrate to successfully form an equal-potential distribution as shown in FIG. 6. Even for a structure as shown in FIG. 7 instead of the structure as shown in FIG. 6, the similar equal-potential distribution can be formed successfully.

[0109] From FIGS. 5 to 7, a liquid crystal orientation control electrode connected to a pixel electrode is installed at an upper layer of the pixel electrode. The closer the distance from the common electrode of the CF substrate, the more similar is the equal-potential distribution diagram of the pixel electrode through another type of liquid crystal orientation control electrode formed by an insulating film. Since the liquid crystal orientation control electrode not connected to the pixel electrode yet is connected to a common electrode same potential of the corresponding substrate.

[0110] If a cell gap is greater than 5 μm , the structure of a pixel electrode of a TFT substrate connected to the liquid crystal orientation control electrode in accordance with the present invention almost has no effect. However, if the cell gap is below 3 μm , the effect is significant. If the cell gap is below 2.5 μm , a sufficiently equal-potential distribution diagram is formed for controlling the alignment of liquid crystal molecules.

[0111] Referring to FIGS. 24 and 26 for planar views of Embodiment 1 of a TFT substrate, two types of different orientation control electrodes are formed at an upper layer of a pixel electrode, and an orientation control electrode installed at the middle of a pixel is coupled to a gate electrode

and installed parallel with a common electrode. Another orientation control electrode with a different alignment control is passed and disposed at a contact pad in the pixel electrode and coupled to the pixel electrode. Referring to FIGS. 57 and 59 for a cross-sectional view of Embodiment 1 of the present invention, the height of orientation control electrode of the pixel electrode is increased to get closer to the common electrode of the substrate as much as possible.

[0112] Referring to FIGS. 8, 9 and 11 for cross-sectional views a TFT portion as depicted in FIGS. 20, 24 and 26 respectively, the pixel electrode must be installed at a lower layer to form a liquid crystal orientation control electrode at an upper layer of the pixel electrode in accordance with the present invention, and thus its characteristic resides on that the photolithographic procedure is used for producing a pixel electrode. FIG. 8 shows a process of using the photolithographic procedure for three times as depicted in FIG. 82. To shorten the manufacturing process, the present invention adopts a halftone exposure method, characterized in that an exposure method as shown in FIGS. 67 and 68 is used for producing two or more types of photoresist thicknesses after the image is developed.

[0113] In the first of the three times of photolithographic procedure as shown in FIG. 82, a gate electrode, a pixel electrode, a common electrode and a contact pad in a pixel electrode are formed. In the first procedure, two manufacturing processes exist as shown in FIGS. 61 and 62, and either one of the two manufacturing processes can be used for forming the pixel electrode, but it is preferable to select a shorter process as shown in FIG. 61. If the thickness of the orientation control electrode as shown in FIG. 9 is reduced, and the halftone exposure method is used in the third time photolithographic procedure, it is preferable to select the process as shown in FIG. 62.

[0114] Since aluminum alloy is used for making a scan line (or a gate electrode) in this invention, therefore ITO cannot be used in the pixel electrode, because a partial battery reaction will result, and the abnormal corrosion or ITO blackening issues usually occur. As a result, the pixel electrode is generally a transparent electrode made of a thin film oxide such as titanium nitride or zirconium nitride.

[0115] The nitride of the transparent pixel electrode and the P-SiNx_o of the gate insulating film cannot have a large selectivity for creating a contact hole by a y etching method, and the manufacturing processes of the previous embodiments as shown in FIGS. 72 to 74 cannot be used anymore. To solve this problem, the present invention uses an aluminum alloy series contact pad to solve the aforementioned problem.

[0116] In the second time of the photolithographic procedure, the thin film semiconductor components are separated and the contact hole is formed, and this procedure is illustrated in FIG. 63. Since this procedure also adopts the halftone exposure method, therefore the procedure of the first time can be used for performing two operations. The process adopted in FIGS. 11 and 26 is a halftone exposure process other than that adopted in FIG. 82, and the halftone exposure method as illustrated in FIG. 65 is used for separating the thin film semiconductor components while forming a source electrode and a drain electrode. The halftone exposure process as shown in FIG. 65 is very similar to the halftone exposure process as shown in FIG. 71, but the halftone exposure process as shown in FIG. 65 is more difficult to take place. When a positive photo-resist layer at a thin area is removed by an oxygen plasma method in the foregoing embodiment as

shown in FIG. 71, sidewalls of a thin film semiconductor layer are oxidized, and the oxidization takes place easily at the time of removing an ohmic contact layer (n+a—silicon layer) of a channel portion of the thin film transistor component, but an even removal cannot be achieved. In the situation as shown in FIG. 65, the thin film semiconductor layer is protected by a metal barrier layer completely when the positive photo-resist layer at the thin area is removed by the oxygen plasma method, and thus the oxidization almost will not take place at the sidewalls.

[0117] In the third photolithographic procedure as shown in FIG. 82, an exposure method is generally used for forming a source electrode, a drain electrode and an orientation control electrode as shown in FIG. 8. In FIG. 9, the third photolithographic procedure also adopts a photolithographic procedure that uses a halftone exposure method as shown in FIG. 64.

[0118] In FIGS. 8, 9 and 20, the third photolithographic procedure is used for forming two different types of orientation control electrodes at an upper layer of the pixel electrode through the insulating film. In FIG. 11, a fourth photolithographic procedure is used for forming two different types of orientation control electrodes, such that an oblique direction of vertical alignment negative dielectric constant anisotropic liquid crystal molecules as shown in FIGS. 3 and 5.

[0119] In FIGS. 8, 9 and 20, a passivation film is a P—SiNx film formed partially by using a CVD method. An ink-jet printing method or a plate offset printing method is used to coat a passivation film made of an organic compound such as BCB. The shortcoming of the process shown in FIG. 11 resides on that a short circuit may occur easily at the common electrode of the corresponding substrate when two different types of orientation control electrodes are formed on the passivation film.

[0120] Referring to FIGS. 25 and 27 for planar views of Embodiment 2 of TFT substrate in accordance with the present invention, a slit is formed on the pixel electrode for the alignment control, and a liquid crystal alignment control electrode connected to the pixel electrode is formed at an upper layer of the pixel electrode through the insulating film. Referring to FIGS. 58 and 60 for cross-sectional views of Embodiment 2 of a pixel, Embodiment 2 similar to Embodiment 1 also installs the orientation control electrode connected to the pixel electrode at a position proximate to the substrate, and thus its characteristic resides on that each type of electrodes and semiconductor layers is installed at a lower layer of the orientation control electrode.

[0121] Embodiments 1 and 2 of the present invention include all alignment control functions at the TFT substrate side. Compared with the previous methods as shown in FIGS. 1 and 2, the methods adopted by the present invention as shown in FIGS. 3 and 4 also have the existing short-circuit problem at the same layer of a video signal line while the orientation control electrode is being formed. Therefore, the pixel structures as shown in FIGS. 24 to 27 are avoided, and a structure having a curvature of 90 degrees at the center of the pixel is used instead. The video signal line and the orientation control electrode of this structure are arranged in parallel and equidistantly with each other, so as to reduce the chance of having a short circuit.

[0122] Referring to FIGS. 10, 12 and 21 for cross-sectional views of the TFT portions as shown in FIGS. 21, 25 and 27 respectively, the basic principle of the Embodiment 2 as illustrated in FIGS. 5 and 6 adopts an alignment control slit for determining the oblique direction of the liquid crystal mol-

ecules correctly, but Embodiment 1 cannot increase the strength of electric field as Embodiment 1 does. Therefore, the response rate of Embodiment 2 is slower than that of Embodiment 1. In the application of displaying animations, it is appropriate to adopt Embodiment 1 for the manufacture of LCD panels. From the planar views as shown in FIGS. 24 and 26, many metal wires are installed densely on the same layer in Embodiment 1, and thus the existing short circuit problem may occur easily. In addition to the short-circuit issue, the voltage applied to the pixel electrode of Embodiments 1 and 2 is not 100% applied to the liquid crystal layer, and thus the shortcoming of requiring a higher driving voltage as shown in FIGS. 1 and 2 still exists. Since the CF substrate can use a low-cost CF substrate which has about the same cost of TN, therefore the product competitiveness can be improved. Particularly, it is not necessary to use a field order driven LCD panel of the CF substrate, which must align the upper and lower substrates as shown in FIGS. 1 and 2, but the present invention does not need any manufacture on the substrate as shown in FIGS. 3 and 4. Such arrangement simply needs to form a substrate with a transparent electrode film, and requires no adjustment of alignment theoretically.

[0123] Referring to FIGS. 28 to 31 for planar views of the TFT substrate in accordance with Embodiment 3 of the present invention and FIG. 32 for a circuit model of the TFT substrate of the invention, a basic unit pixel is divided by the video signal line into two sub pixels: sub pixel A and sub pixel B. The ratio of areas of the sub pixel A to the sub pixel B is approximately equal to 1:2. FIG. 34 shows a driving signal waveform of an LCD panel in accordance with Embodiment 3 of the present invention. Even though the data is obtained from the same video signal line, the phase is changed by different common electrode as shown in FIG. 34, since each pixel electrode is combined with a capacitor of a different common electrode, and a horizontal period (H period) is applied, and the waveform of a signal with an opposite polarity maintains the effective voltage of the sub pixel A greater than the effective voltage of the sub pixel B. FIG. 33 shows the quantity of light transmission of the LCD panel when the signal waveform is driven, and the threshold voltage of the liquid crystals of the sub pixel A and the sub pixel B can be changed for correcting γ .

[0124] FIG. 83 shows the process of manufacturing the TFT substrates as illustrated in FIGS. 28 to 31, and FIG. 82 illustrates Embodiments 1 and 2. A common electrode is manufactured in the first the photolithographic procedure. In Embodiment 3 as shown in FIG. 32, it is not necessary to arrange the video signal line in parallel with the common electrode, and thus the common electrode is manufactured by the third photolithographic procedure as shown in FIG. 83.

[0125] FIG. 35 shows a circuit model of the TFT substrate when a high-precision super large LCD panel is manufactured. FIGS. 36 to 39 show the method of driving a TFT substrate as illustrated in FIG. 35. FIGS. 36 to 39 relate to the field order driving method. Since the display screen is divided into two: an upper screen and a lower screen, therefore the video signal line is also divided into two: an upper video signal line and a lower video signal line, and the video signals of the same polarity are applied.

[0126] The common electrode has not been divided into two, but both upper and lower portions integrated. FIGS. 36 and 38 show that video signals are written from the center of the screen to the upper and lower screens in order to prevent the blocks of the upper and lower screens from being sepa-

rated. FIGS. 37 and 39 show that video signals are written from the upper and lower screens to the center of the screen. To divide the display screen into two, the horizontal scan period is extended to two times of 2H. FIGS. 36 and 37 show that the horizontal scan period is divided into two, such that different video signals can be written for two pixels by two different multitasking methods. FIGS. 38 and 39 show that the horizontal scan period is divided into three, such that different video signals can be written for three pixels by three multitasking methods.

[0127] Referring to FIGS. 53 and 45 for a planar view and a cross-sectional view of an IPS TFT substrate in accordance with Embodiment 4 of the present invention, and FIG. 84 for the manufacturing process of an IPS TFT substrate in accordance with Embodiment 4 of the present invention, three times of photolithographic procedure adopting three times of halftone exposure method are conducted. FIG. 46 shows a circuit model of a TFT substrate as illustrated in FIG. 53. The center of a pixel and the video signal are arranged in parallel with the common electrode. FIG. 56 shows a circuit model of a TFT substrate when a high-precision supper large LCD panel is manufactured. FIG. 55 shows a driving waveform diagram of a TFT substrate as illustrated in FIG. 56. Signal waveforms of different polarities are applied on even-numbered rows and odd-numbered rows, and signal waveforms of different polarities are applied to the even-numbered rows and odd-numbered row of video signal waveforms, and a signal with an opposite polarity is applied to the common electrode of each corresponding video signal line.

[0128] Even the modes of liquid crystals are different, the circuit models of the common electrode and the video signal line is identical to those as shown in FIG. 35. The IPS TFT substrate as shown in FIG. 56 can also adopt the same field order driving method of Embodiment 3. Similar to the process as shown in FIG. 35, the process as shown in FIG. 56 divides the display screen into two: an upper screen and a lower screen, and thus the video signal line is also divided into two: an upper video signal line and a lower video signal line, and the polarity of video signals are the same.

[0129] The common electrode has not been divided into two, but it is connected from top to bottom as a whole. To prevent the blocks of upper and lower screens from being separated, the video signals are written from the center of the screen upward or downward, or the video signals are written from the top or bottom of the screen towards the center of the screen. The driving method for the scan lines is identical to that of Embodiment 3.

[0130] Referring to FIGS. 54 and 44 for a planar view and a cross-sectional view of a FFS TFT substrate in accordance with Embodiment 5 of the present invention respectively, FIG. 47 for a cross-sectional view of a portion of a thin film transistor, and FIG. 85 for the manufacturing process of a FFS TFT substrate in accordance with Embodiment 5 of the present invention, the photolithographic procedure is conducted for three times, and a halftone exposure method is applied for all of the three times. The three times of Embodiments 4 and 5 use the halftone exposure method as shown in FIG. 66. Unlike the vertical alignment LCD panel, a horizontal electric field panel requires different orientation processing procedure (such as the friction processing). To prevent having a poor alignment area, it is necessary to minimize the roughness of the TFT substrate. However, the planar views of FIGS. 53 and 54 show that the thickness of elec-

trodes is increase to lower the resistance of a common electrode at the center of the screen.

[0131] Since a poor alignment area as shown in FIG. 66 must occur in both IPS and FFS modes, therefore the shortcoming of unable to show the black color for a black potential exists. To minimize the poor alignment area, it is necessary to apply the halftone exposure method for three times.

[0132] FIGS. 61 and 62 use the manufacturing process as illustrated in FIG. 85, the process of the halftone exposure method is applied for one time, and any one can be selected. FIG. 63 illustrates the process of applying the halftone exposure method for the second time, and FIG. 64 illustrates the process of applying the halftone exposure method for three times, and FIG. 65 illustrates the process of performing the photolithographic procedure for four times for manufacturing the FFS TFT substrate. The halftone exposure method is applied for two times.

[0133] Even if the FFS TFT substrate as shown in FIG. 54 adopts the same driving method as the IPS TFT substrate as shown in FIG. 53, all circuit models of the TFT substrate as shown in FIG. 56 can be applicable for the FFS mode of FIG. 54. If the driving method of FIG. 55 is used, the FFS mode with a high driving voltage can be driven easily. Since the FFS mode can produce a strong electric field, therefore the response rate of the liquid crystal molecules is smaller than that of the IPS mode and applicable for the field order driving method. Particularly, a high voltage can be applied to the LCD panels as shown in FIGS. 55 and 56, and thus such method is considered as a driving method applicable for high-speed operations, and most suitable for the field order driving method for the divided upper and lower screens as shown in FIGS. 36 to 39.

What is claimed is:

1. A method of fabricating MVA active matrix substrate, and said substrate constituting an active matrix display device, characterized in that: a photolithographic procedure is performed three times for the manufacture:

- (1) forming a gate electrode, a pixel electrode, a common electrode and a contact pad in said pixel electrode (wherein said photolithographic procedure using a halftone exposure method for the first time);
- (2) forming a separate thin film semiconductor layer component, and a contact hole (wherein said photolithographic procedure using a halftone exposure method for the second time);
- (3) forming a source electrode, a drain electrode and an orientation control electrode (wherein said photolithographic procedure using a general exposure method); such that after an ohmic contact layer of a channel portion of said thin film transistor is dry etched, a partial film of a passivation layer is formed by a silicon nitride film by using a mask deposition method (wherein said film is formed at a terminal portion other than those of a gate electrode, a source electrode and a common electrode).

2. A method of fabricating MVA active matrix substrate, and said substrate constituting an active matrix display device, characterized in that: a photolithographic procedure is performed three times for the manufacture:

- (1) forming a gate electrode, a pixel electrode and a contact pad in said pixel electrode (wherein said photolithographic procedure uses a halftone exposure method for the first time);

- (2) forming a separate thin film semiconductor layer component, and a contact hole (wherein said photolithographic procedure uses a halftone exposure method for the second time);
- (3) forming a source electrode, a drain electrode, an orientation control electrode and a common electrode (wherein said photolithographic procedure uses a general exposure method); such that after an ohmic contact layer of a channel portion of said thin film transistor is dry etched, a partial film of a passivation layer is formed by a silicon nitride film by using a mask deposition method (wherein said film is formed at a terminal portion other than those of a gate electrode, a source electrode and a common electrode).
3. A MVA active matrix liquid crystal display apparatus, manufactured by a manufacturing method of claim 1.
4. A MVA active matrix liquid crystal display apparatus, manufactured by a manufacturing method of claim 2.
5. A MVA active matrix liquid crystal display apparatus, manufactured by a manufacturing method of claim 2, and characterized in that a basic unit pixel constitute an area of 2:1, and a video signal line (or a source electrode) is divided longitudinally into two, and said two divided pixel electrodes are coupled to each thin film transistor component respectively, and a source electrode of said two thin film transistor components is coupled to said video signal line that divides said pixel into two, and said two thin film transistor components are switched by a same scan line (or gate electrode), and said two divided pixel electrodes form a capacitor with different common electrode and insulating film aligned in parallel with said video signal wire, and said video signal wires are aligned in parallel on odd-numbered rows and even-numbered rows of said common electrode, and a voltage is applied to signals with different opposite polarities within a horizon-

tal scan period (H period), and said video signal line in said two divided pixel electrodes is used for applying a voltage greater than an effective signal of large pixel electrode liquid crystal molecules on small pixel electrode liquid crystal molecules.

6. A method of fabricating an IPS active matrix substrate, and said substrate constituting an active matrix display device, characterized in that: a photolithographic procedure is performed for three times for the manufacture:

- (1) forming a gate electrode, a comb pixel electrode, a common electrode for shielding a video signal line (or a source electrode), a contact pad in said pixel electrode, and a video signal line for shielding said contact pad in common electrode (wherein said photolithographic procedure uses a halftone exposure method for the first time);
- (2) forming a separate thin film semiconductor layer component, and a contact hole (wherein said photolithographic procedure uses a halftone exposure method for the second time);
- (3) forming a source electrode (or video signal line), a drain electrode, a common electrode at the center of a pixel and a comb common electrode (wherein said third time of photolithographic procedure uses a halftone exposure method), such that after an ohmic contact layer of a channel portion of said thin film transistor is dry etched, a partial film of a passivation layer is formed by a silicon nitride film by using a mask deposition method (wherein said film is formed at a terminal portion other than those of a gate electrode, a source electrode and a common electrode).
7. A horizontal electric field active matrix liquid crystal display apparatus, manufactured by a method of claim 6.

* * * * *

专利名称(译)	低成本大屏幕广角快速响应液晶显示装置		
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申请(专利权)人(译)	MIKUNI ELECTRON CO.LTD.		
当前申请(专利权)人(译)	知识产权DISCOVERY CO. , LTD.		
[标]发明人	TANAKA SAKAE SAMEJIMA TOSHIYUKI		
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摘要(译)

本发明公开了一种超大型广角高速响应液晶显示装置，采用光刻工艺制作三次。本发明采用半色调曝光技术形成栅极，公共电极，像素电极和接触垫，然后采用半色调曝光技术形成硅(Si)岛和接触孔，以及一般的曝光技术形成源电极，漏电极和取向控制电极。钝化层使用掩模沉积方法。通过使用P-CVD法形成膜，或者通过使用油墨涂覆方法或喷涂方法在局部区域形成保护区域，以及用于超大角度广角高速响应液体的TFT阵列基板可以制造通过使用光刻程序制造三次的晶体显示装置。

