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Bang et al.(10) **Pub. No.: US 2002/0080309 A1**(43) **Pub. Date: Jun. 27, 2002**(54) **LIQUID CRYSTAL DISPLAY PANEL****Publication Classification**(76) Inventors: **Yong Ik Bang**, Taegu-Kwangyokshi
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Park, Anyang-shi (KR)(51) **Int. Cl.⁷** **G02F 1/1343**
(52) **U.S. Cl.** **349/110**

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SONG K. JUNG**LONG ALDRIDGE & NORMAN LLP****Suite 600****701 Pennsylvania Avenue, N.W.****Washington, DC 20004 (US)**(57) **ABSTRACT**

A liquid crystal display (LCD) panel that has even luminance with high picture quality is disclosed. The LCD panel includes a first substrate provided with a plurality of gate and data lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement; a second substrate provided with a black matrix layer to shield portions other than the pixel region from light; and a liquid crystal layer injected between the first and second substrates, wherein the pixel regions at a surrounding portion have an aperture ratio lower than that of the pixel regions at the other portions.

(21) Appl. No.: **10/025,904**(22) Filed: **Dec. 26, 2001**(30) **Foreign Application Priority Data**

Dec. 22, 2000 (KR) 2000-80214

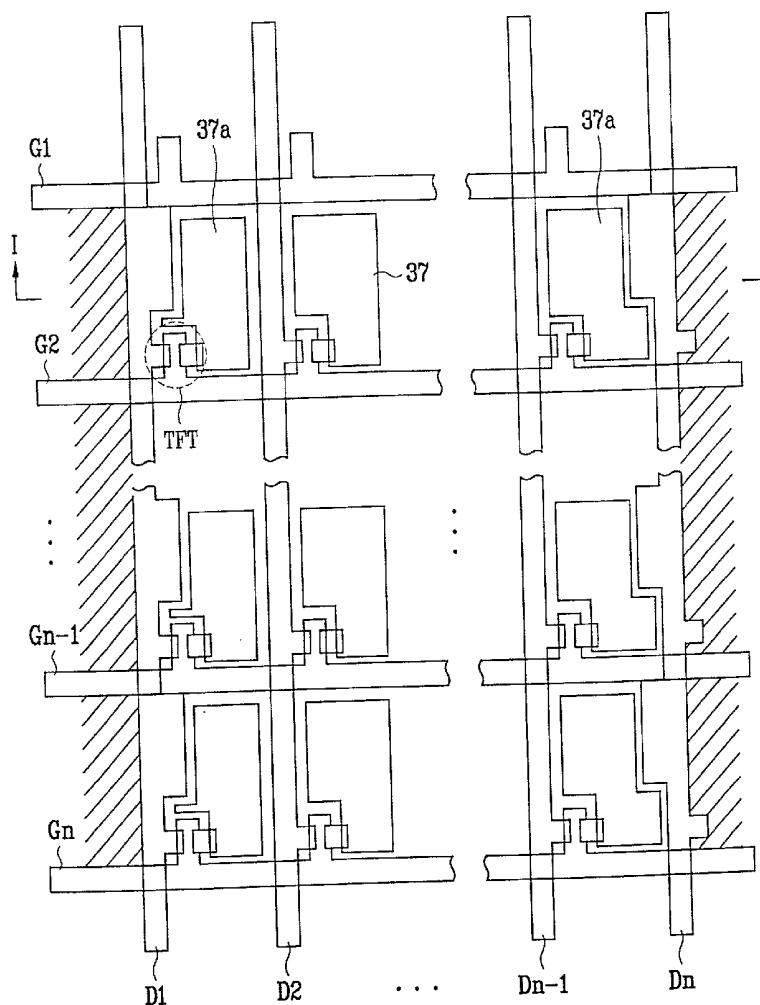


FIG. 1
Related Art

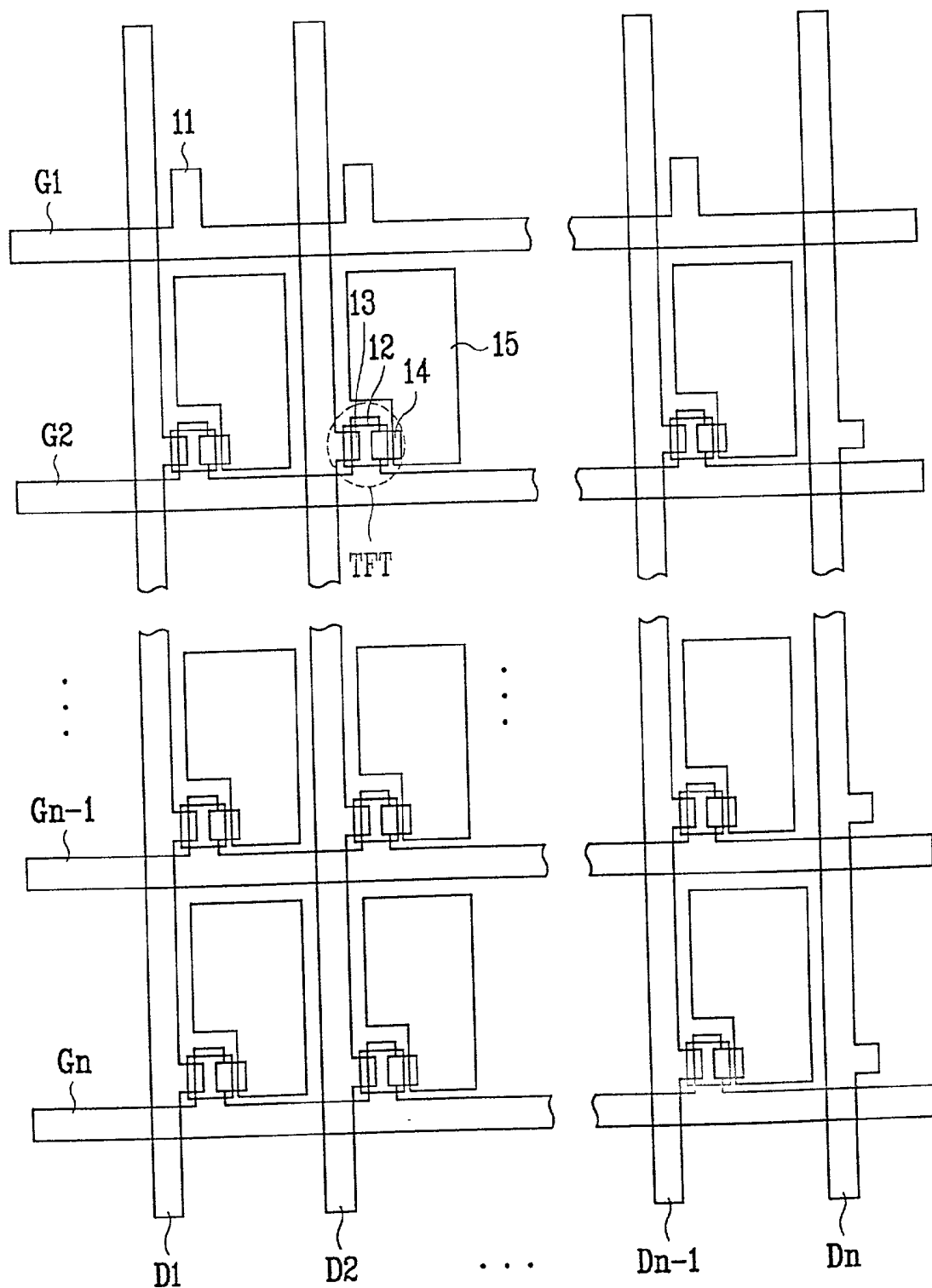


FIG. 2A
Related Art

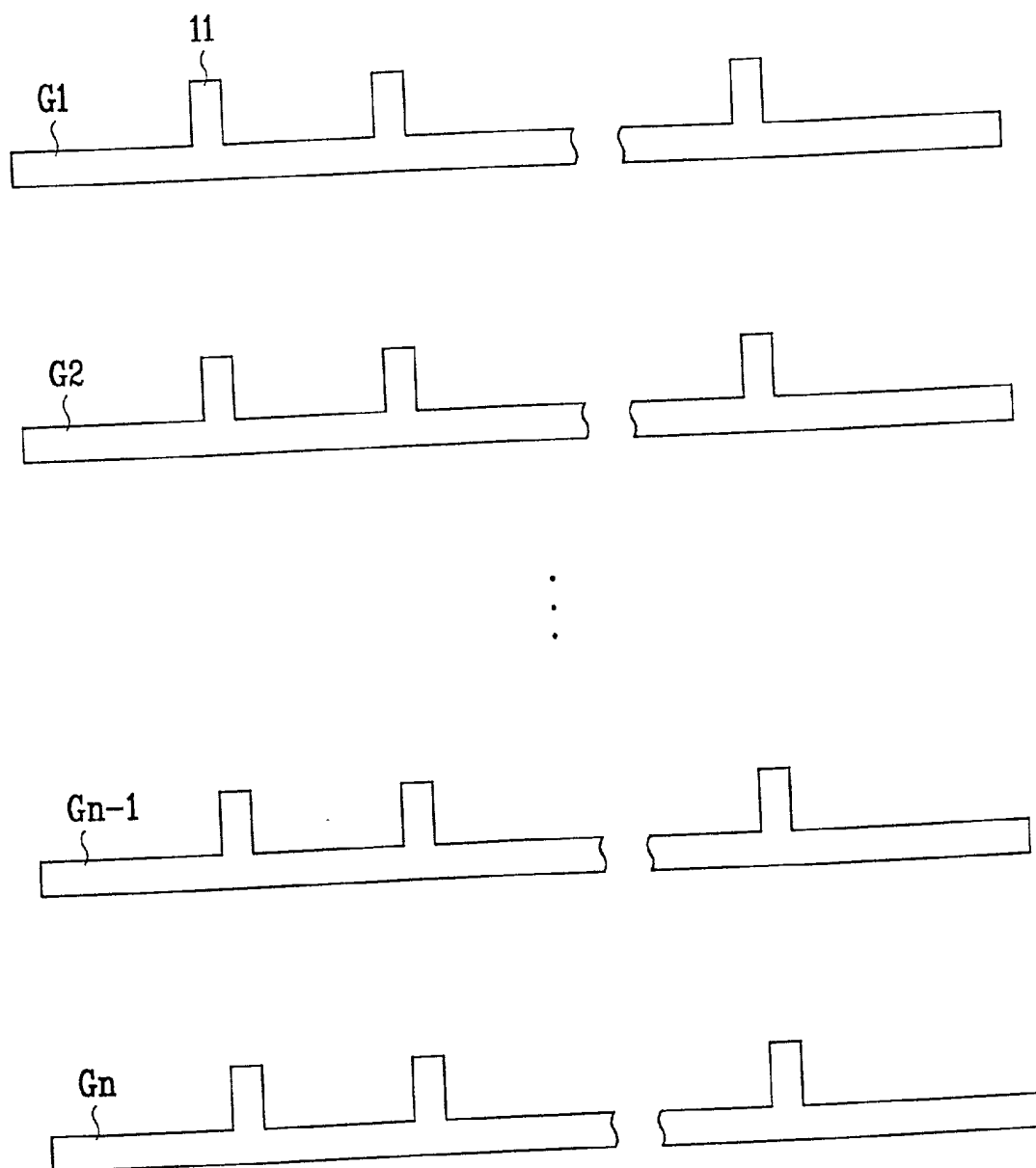


FIG.2B
Related Art

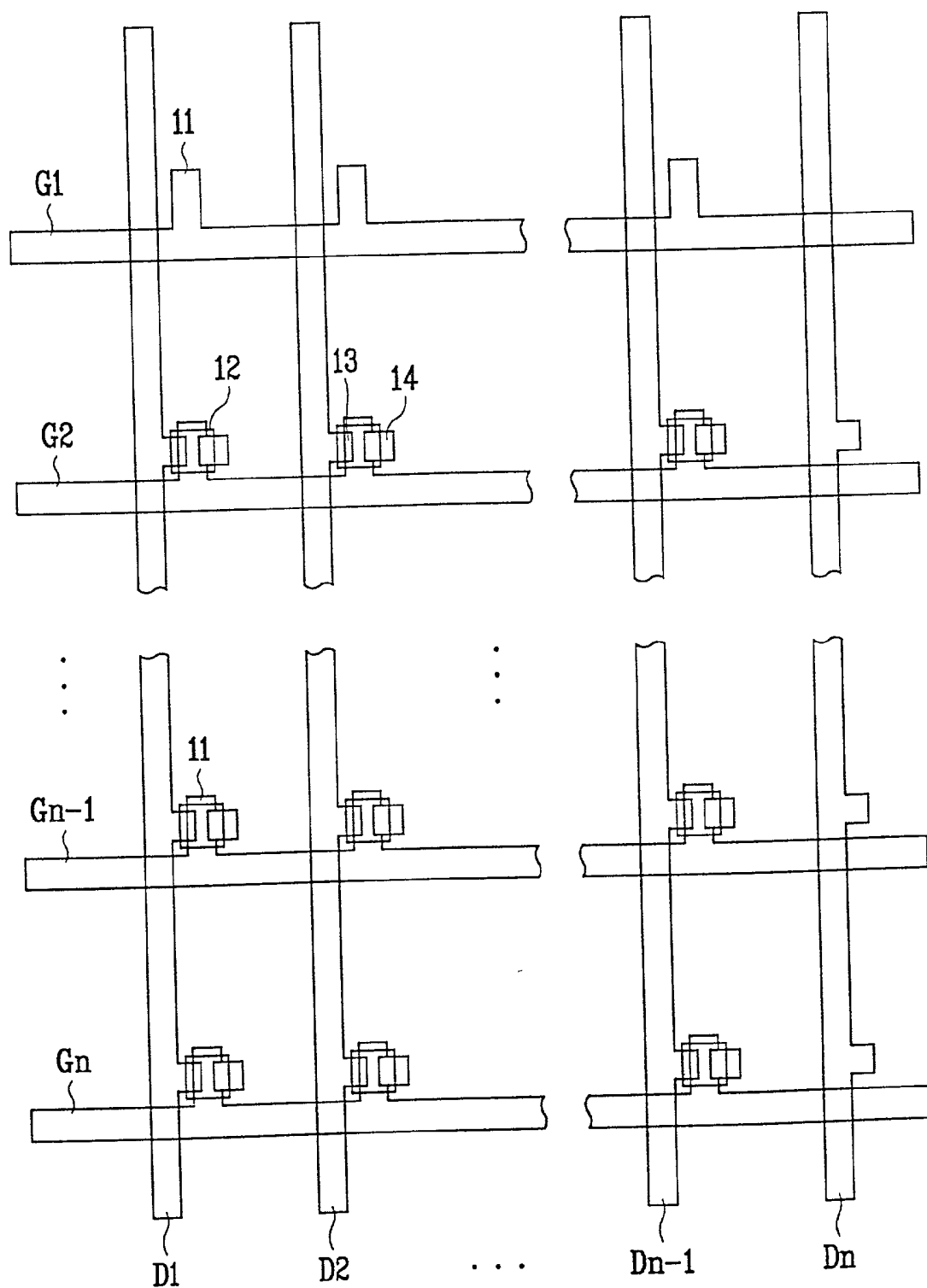


FIG. 2C
Related Art

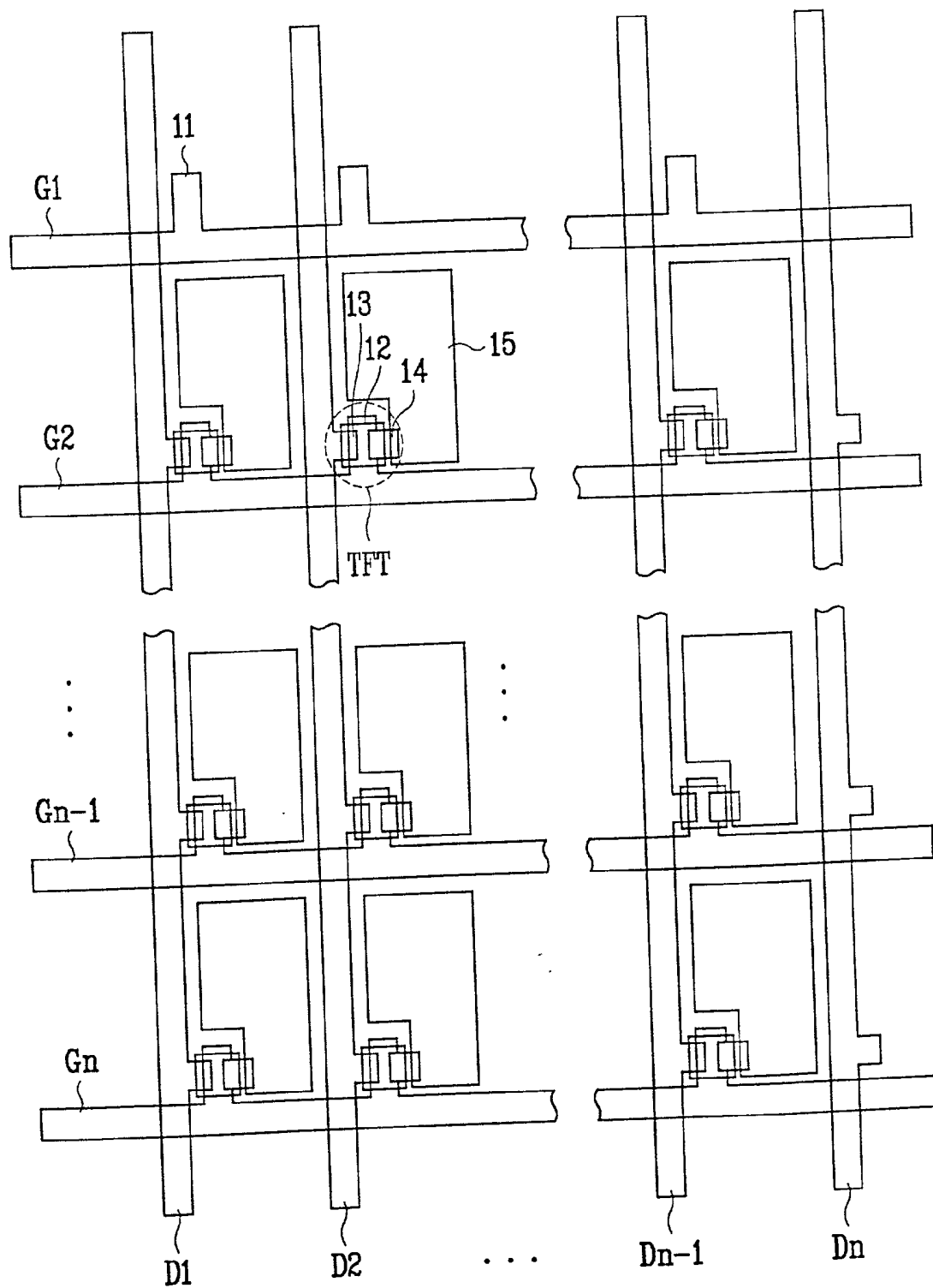


FIG. 3

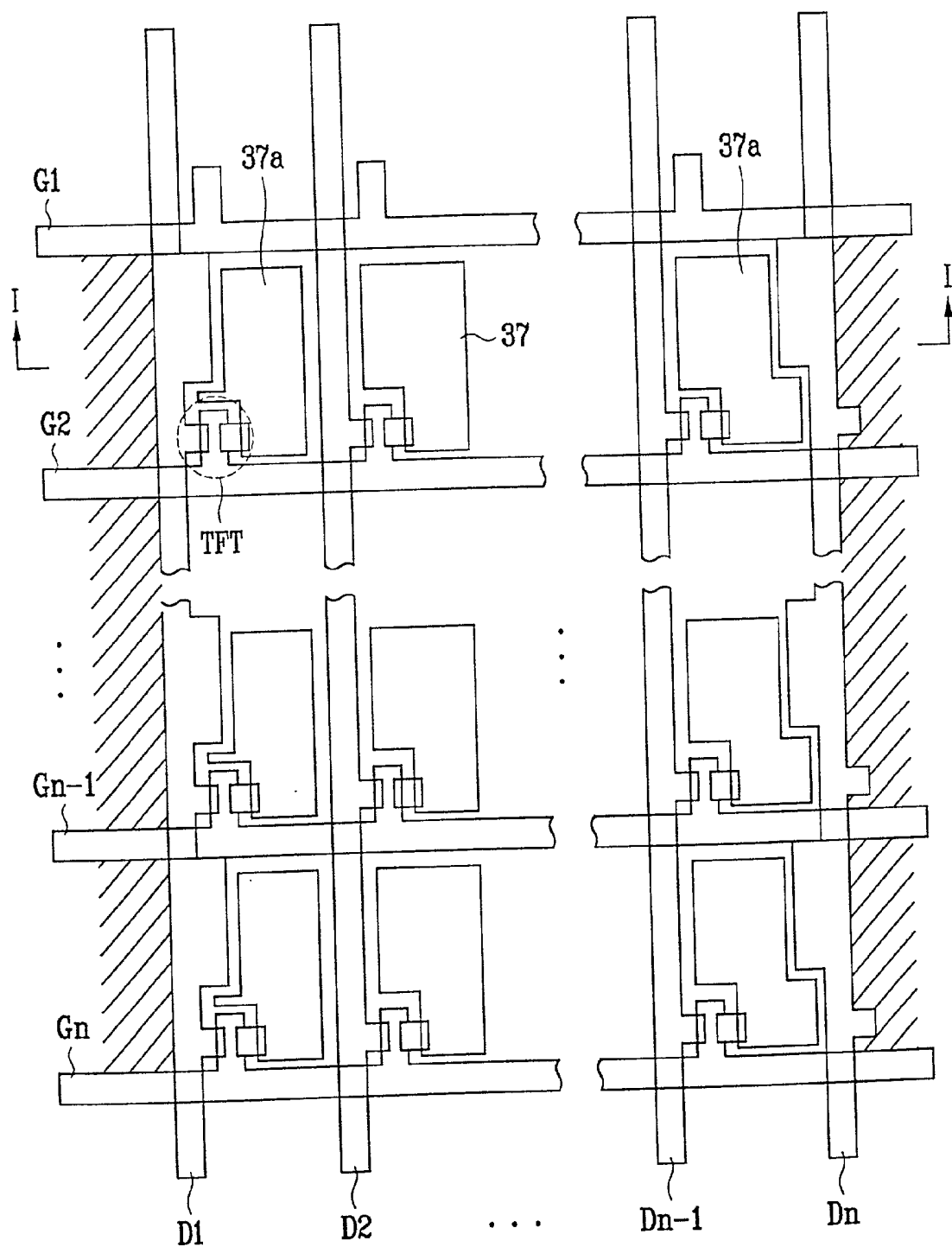


FIG. 4

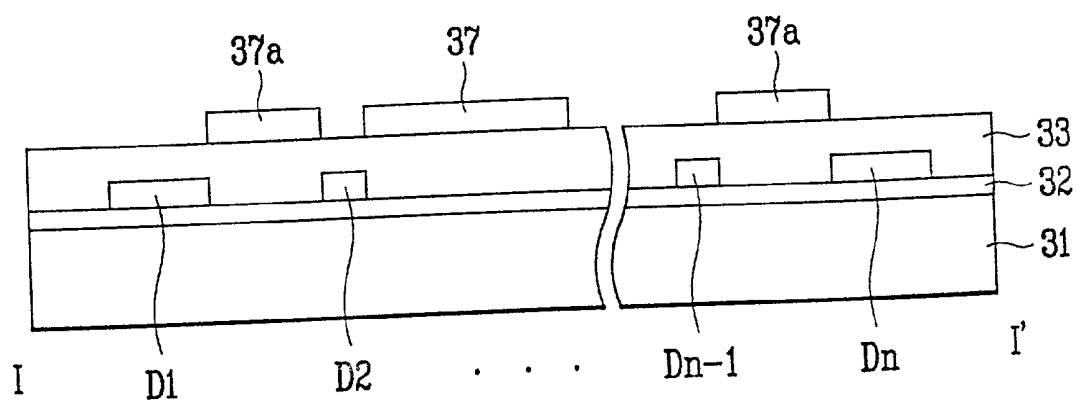


FIG. 5

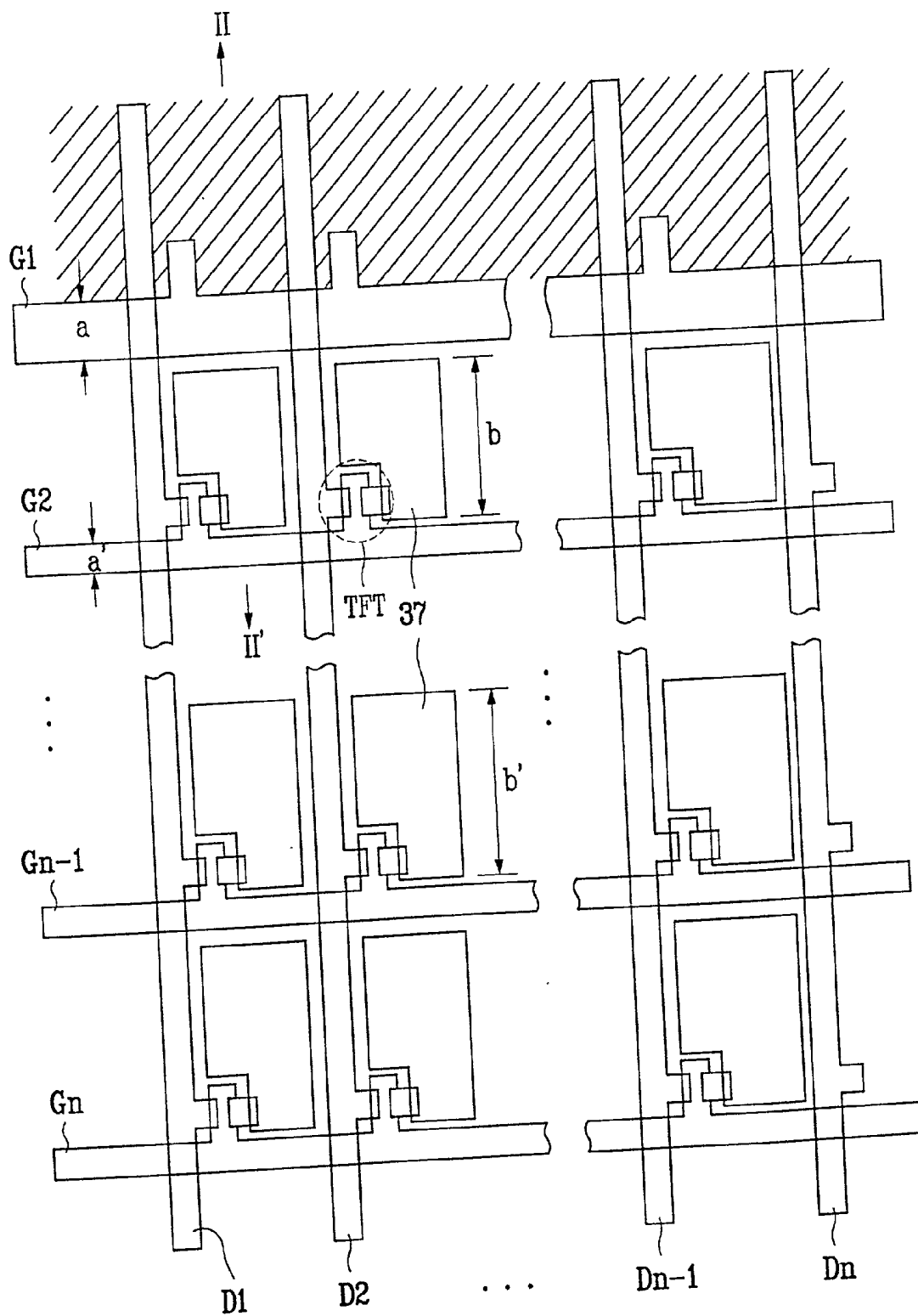


FIG. 6

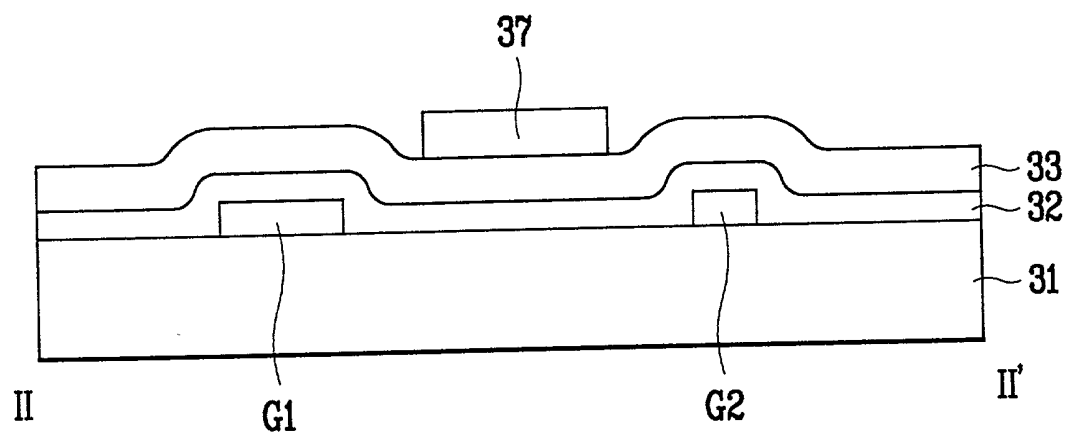


FIG. 7

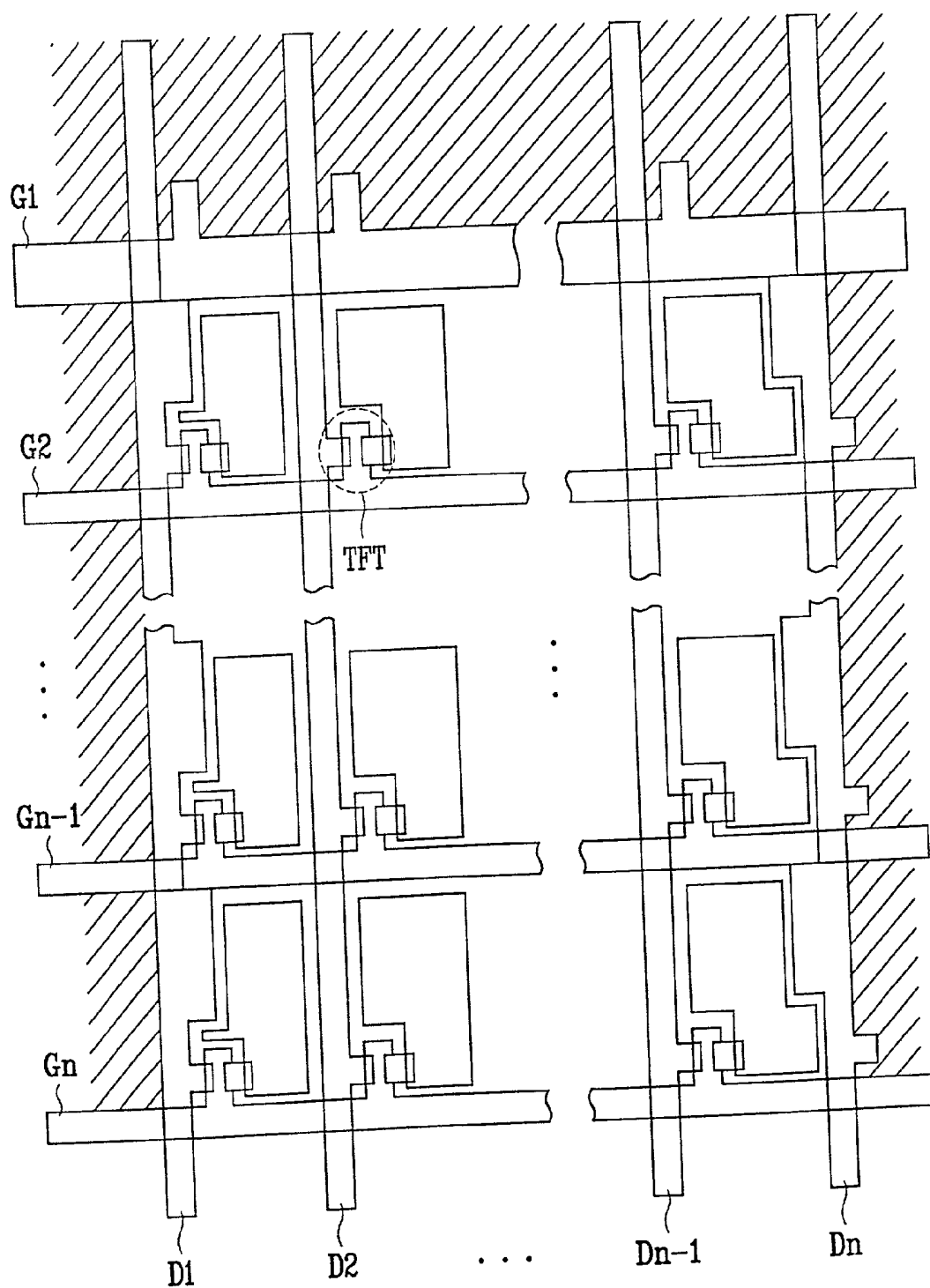


FIG. 8

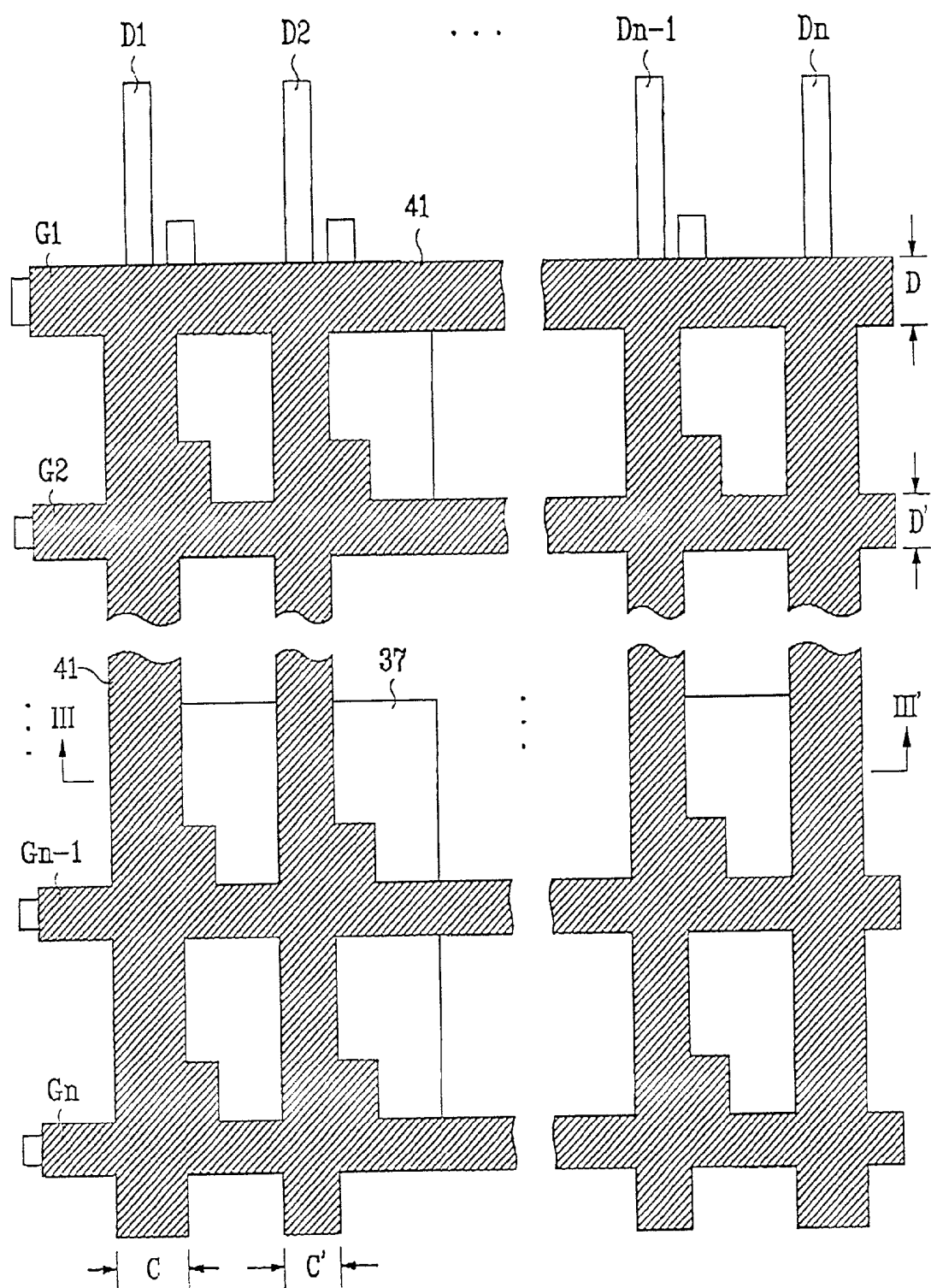


FIG. 9

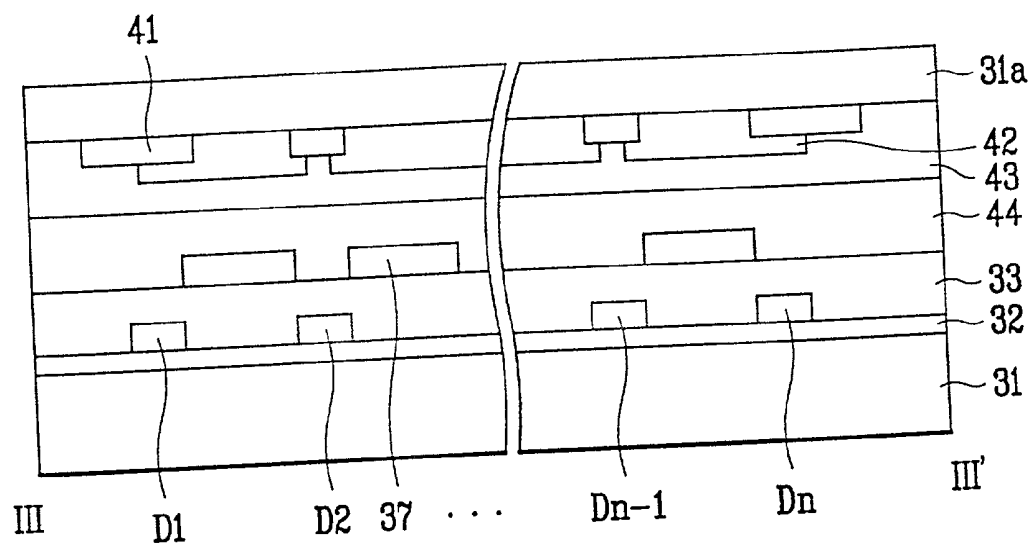


FIG.10

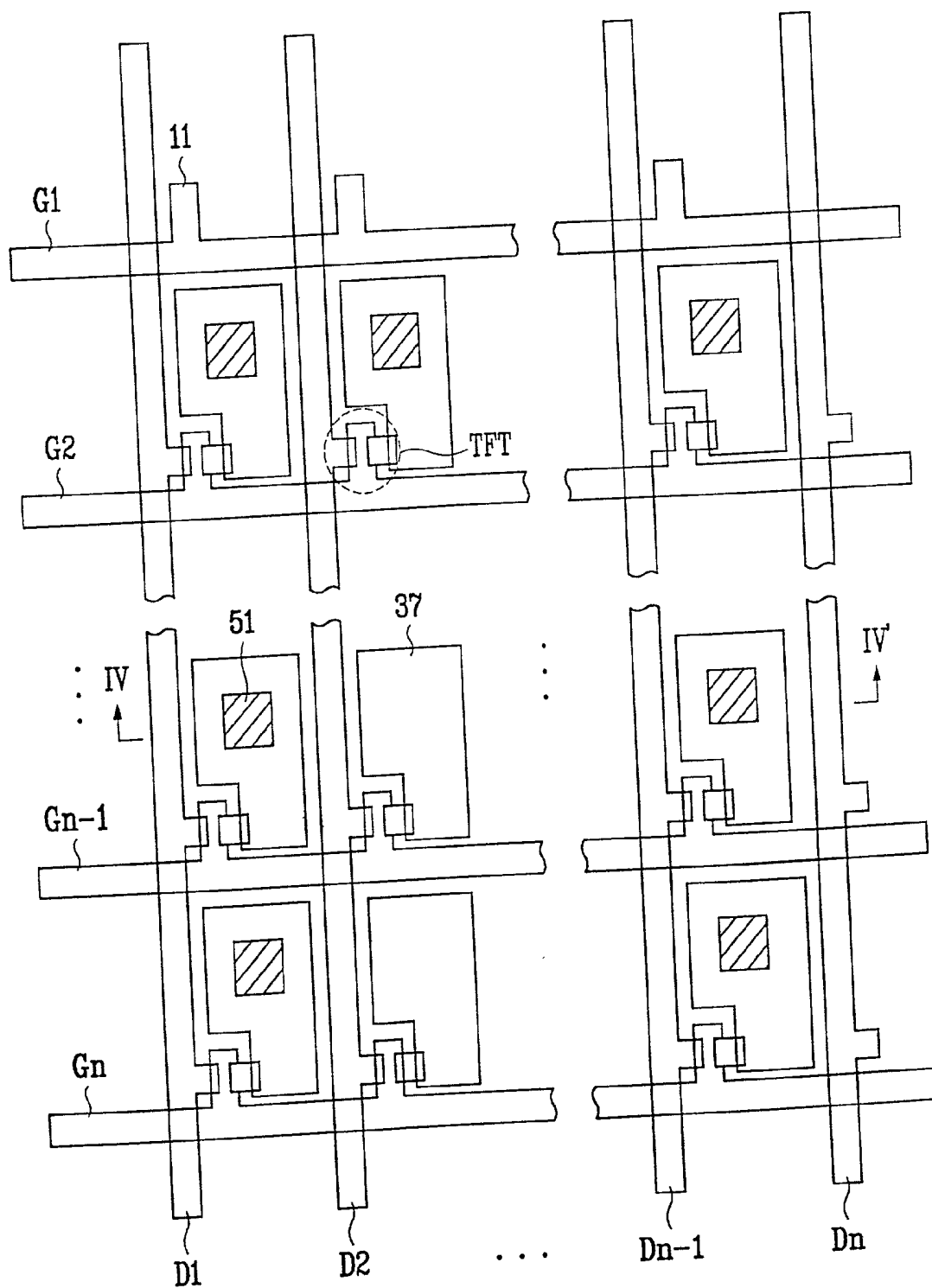
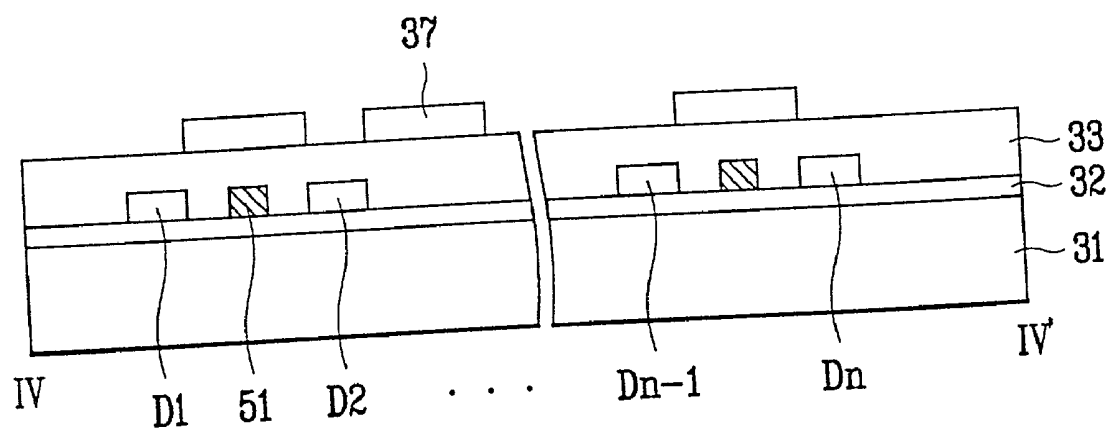


FIG.11



LIQUID CRYSTAL DISPLAY PANEL

[0001] This application claims the benefit of Korean Patent Application No. 2000-80214 filed on Dec. 22, 2000, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display (LCD) device, and more particularly, to an LCD panel that prevents luminance occurring in a contour of a cell region from being higher than that occurring in the cell region, thereby improving picture quality.

[0004] 2. Discussion of the Related Art

[0005] Rapid development within the fields of information and communication has caused an increase in the demand for thin, lightweight and low cost display devices for viewing information. Industries that develop displays are responding to these needs by placing high emphasis on developing flat panel type displays.

[0006] Historically, the Cathode Ray Tube (CRT) has been widely used as a display device in applications such as televisions, computer monitors, and the like, because CRT screens can display various colors with high luminance. However, the CRT cannot adequately satisfy present demands for display applications that require reduced volume and weight, portability, and low power consumption, while having a large screen size and high resolution. Out of this need, the display industry has placed high emphasis on developing flat panel displays to replace the CRT. Over the years, flat panel displays have found wide use in monitors for computers, spacecraft, and aircraft. Examples of flat panel display types currently used include the LCD, the electroluminescent display (ELD), the field emission display (FED), and the plasma display panel (PDP).

[0007] Characteristics required for an ideal flat panel display include a lightweight, high luminance, high efficiency, high resolution, high speed response time, low driving voltage, low power consumption, low cost, and natural color.

[0008] Generally, a phosphor material on a surface of the CRT emits light in an analog type based on an externally applied display timing signal and an externally applied data signal, so that a trace of an electron beam is controlled. On the other hand, the LCD controls the electric field applied to the liquid crystal located in each display so that transmittivity of light is controlled.

[0009] Development and application of thin film transistor (TFT) -LCD industries have been accelerated in accordance with the increase in the dimensions and increase in the resolution. To increase the productivity, many efforts have been focused on simplifying process steps and improving yield.

[0010] A related art LCD panel is now described with reference to FIG. 1.

[0011] FIG. 1 is a plan view illustrating a related art LCD panel.

[0012] As shown in FIG. 1, a plurality of gate lines G1, G2, . . . , Gn are arranged to cross a plurality of data lines D1, D2, . . . , Dn, so that a plurality of pixel regions are defined. A TFT is formed at each crossing point between the respective gate line and the respective data line. A pixel electrode 15 is formed in each pixel region.

[0013] The TFT includes a gate electrode 11 extending from the gate lines, a gate insulating film (not shown) over the gate electrode, a semiconductor layer 12 on the gate insulating film, and source and drain electrodes 13 and 14 on the semiconductor layer 12.

[0014] All the gate lines G1, . . . , Gn have substantially the same widths as one another. All the data lines D1, . . . , Dn also have substantially the same widths as one another.

[0015] A pixel electrode 15 including a transparent conductive material such as indium tin oxide (ITO) is formed in each pixel region. Each pixel electrode 15 has the same aperture ratio over the entire region of the panel.

[0016] As shown in FIG. 1, no pixel electrode is formed above the first gate line G1. Likewise, no pixel electrode is formed before the first data line D1 and the nth data line Dn.

[0017] The process for fabricating the aforementioned related art LCD panel will now be described with reference to FIG. 2A to FIG. 2C.

[0018] As shown in FIG. 2A, a gate electrode material, such as Al, Cr, Mo, Ta, and Al alloy, is formed on an insulating substrate by a sputtering process and then is patterned, so that the plurality of gate lines G1, G2, . . . , Gn having the gate electrode 11 are formed to have substantially the same widths.

[0019] Afterwards, the gate insulating film (not shown) of SiN_x or SiO_x is formed on the entire surface including the gate lines G1, G2, . . . , Gn. As shown in FIG. 2B, a semiconductor layer 12 used as a channel of the TFT is patterned on the gate insulating film over the gate electrode 11.

[0020] Subsequently, the plurality of data lines D1, D2, . . . , Dn are formed to cross the gate lines G1, G2, . . . , Gn. At the same time, the source and drain electrodes 13 and 14 are formed over the semiconductor layer 12. At this time, the data lines D1, D2, . . . , Dn have substantially the same width over the whole region of the panel.

[0021] As shown in FIG. 2C, a passivation film (not shown) is formed on the entire surface including the data lines D1, D2, . . . , Dn and the source and drain electrodes 13 and 14. A contact hole is then formed to expose the drain electrode 14. The pixel electrode 15 is formed to electrically connect with the drain electrode 14 through the contact hole.

[0022] At this time, since the respective pixel electrodes 15 have substantially the same area as one another over the whole region of the panel, they have the same aperture ratio as each other.

[0023] Thus, a TFT substrate is manufactured.

[0024] Although not shown, the TFT substrate and an opposing color filter substrate are prepared and attached to each other. A liquid crystal is then injected between the two substrates. Thus, the process for manufacturing the related art LCD panel is completed.

[0025] However, the related art LCD panel has several problems.

[0026] Since no electrode(pixel electrode) is formed before the first data line, after the last data line, or above the gate line, the electric field does not occur therein. Accordingly, in view of the whole region of the panel, the electric field intensity varies depending on the portion where the pixel electrode is formed and the portion where the pixel electrode is not formed, thereby causing difference in transmittivity therebetween.

[0027] According to the experiments, the transmittivity difference between the portion where the pixel electrode is formed and the portion where the pixel electrode is not formed is about 12%. Accordingly, luminance occurring before the first data line, after the last data line, or above the gate line is higher than that at the other portions. For this reason, picture quality is deteriorated.

SUMMARY OF THE INVENTION

[0028] Accordingly, the present invention is directed to an LCD panel that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0029] An object of the present invention is to provide an LCD panel that has even luminance with high picture quality.

[0030] Additional features and advantages of the invention will be set forth in the description that follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the scheme particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0031] To achieve these and other advantages in accordance with the present invention, as embodied and broadly described, a liquid crystal display panel includes a first substrate provided with a plurality of gate and data lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement; a second substrate provided with a black matrix layer to shield portions other than the pixel regions from light; and a liquid crystal layer injected between the first and second substrates, wherein the pixel regions in a peripheral portion of the matrix arrangement have an aperture ratio lower than that of the pixel region at the other portions in the matrix arrangement.

[0032] A first gate line among the gate lines has a greater width than widths of the other gate lines, and a first data line or a last data line among the data lines has a greater width than widths of the other data lines.

[0033] The black matrix layer corresponding to the first gate line, the first data line or the last data line has a greater width than widths of the black matrix layer corresponding to the other portions.

[0034] A light-shielding pattern is further provided in the pixel regions in the peripheral portion, and the pixel regions in the peripheral portion have an aperture ratio reduced by 10~15% more than aperture ratios of the pixel region at the other portions.

[0035] In another aspect of the present invention, a liquid crystal display panel includes a plurality of gate lines arranged in one direction at constant intervals; a plurality of data lines arranged at constant intervals to be substantially perpendicular to the gate lines to define a plurality of pixel regions in a matrix arrangement; and a plurality of pixel electrodes, wherein one pixel electrode is in each pixel region, wherein the pixel electrodes at a peripheral portion of the matrix arrangement are narrower than the pixel electrode at the other portions.

[0036] A gate line that does not drive the pixel electrode among the gate lines has a greater width than widths of the other gate lines. A first data line or a last data line among the data lines has a greater width than widths of the other data lines. The pixel electrodes adjacent to the first data line or the last data line have a smaller area than areas of the other pixel electrodes.

[0037] In still another aspect of the present invention, a liquid crystal display panel according to the present invention includes a first substrate provided with a plurality of gate and data lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement; a second substrate provided with a black matrix layer to shield portions other than the pixel regions from light; and a liquid crystal layer injected between the first and second substrates, wherein the black matrix layer corresponding to a first data line or a last data line among the data lines has a greater width than the black matrix layer corresponding to the other lines.

[0038] The black matrix layer corresponding to a first gate line among the gate lines has a greater width than the black matrix layer corresponding to the other gate lines.

[0039] In further another aspect of the present invention, a liquid crystal display panel includes a plurality of gate lines arranged in one direction at constant intervals; a plurality of data lines arranged at constant intervals to be substantially perpendicular to the gate lines to define a plurality of pixel regions in a matrix arrangement; and a plurality of light-shielding patterns in at least one of the pixel regions at a surrounding portion among the pixel regions.

[0040] The light-shielding patterns are in the pixel regions adjacent to a first data line or a last data line among the data lines. The light-shielding patterns are a metal which is the same material as that of the data lines.

[0041] In further still another aspect of the present invention, an LCD panel includes: first and second substrates; a plurality of gate and data lines arranged on the first substrate to define a plurality of pixel regions, the gate lines crossing the data lines; a plurality of pixel electrodes, wherein one pixel electrode is in each pixel region; and a black matrix pattern formed on the second substrate to shield portions other than the pixel electrodes from light, wherein a first gate line among the gate lines has a greater width than the other gate lines, one of a first data line and a last data line among the data lines has a width greater than the other data lines, and the black matrix pattern corresponding to the first gate line, the first data line or the last data line has a width greater than the black matrix pattern corresponding to the other portions.

[0042] A plurality of thin film transistors are further provided in a crossing portion of the respective gate line and the respective data line.

[0043] The pixel electrodes adjacent to the first data line and/or the last data line have smaller area than the other pixel electrodes.

[0044] The pixel electrodes adjacent to the first data line and the last data line have an aperture ratio reduced by 10~15% of aperture ratios of the other pixel electrodes.

[0045] In the LCD panel of the present invention, to remove relatively high luminance caused because a region where a pixel electrode is not formed has higher transmittivity than that of a region where a pixel electrode is formed, an aperture ratio in a region of the pixel electrode adjacent to where the pixel electrode is not formed is reduced so that even luminance distribution can be obtained.

[0046] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0047] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0048] FIG. 1 is a plan view illustrating a related art LCD panel;

[0049] FIG. 2 is a cross-sectional view illustrating a related art method for fabricating an LCD panel;

[0050] FIG. 3 is a plan view illustrating an LCD panel according to the first embodiment of the present invention;

[0051] FIG. 4 is a sectional view taken along line I-I' of FIG. 3;

[0052] FIG. 5 is a plan view illustrating an LCD panel according to the second embodiment of the present invention;

[0053] FIG. 6 is a sectional view taken along line II-II' of FIG. 5;

[0054] FIG. 7 is a plan view illustrating an LCD panel according to the third embodiment of the present invention;

[0055] FIG. 8 is a plan view illustrating an LCD panel according to the fourth embodiment of the present invention;

[0056] FIG. 9 is a sectional view taken along line III-III' of FIG. 8;

[0057] FIG. 10 is a plan view illustrating an LCD panel according to the fifth embodiment of the present invention; and

[0058] FIG. 11 is a sectional view taken along line IV-IV' of FIG. 10.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0059] Reference will now be made in detail to the illustrated embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0060] FIG. 3 is a plan view illustrating an LCD panel according to the first embodiment of the present invention. FIG. 4 is a sectional view taken along line I-I' of FIG. 3, in which relatively high luminance is removed by varying a width of data lines.

[0061] As shown in FIG. 3, a plurality of gate lines G1, G2, . . . , Gn are arranged in one direction and a plurality of data lines D1, D2, . . . , Dn are arranged to cross the gate lines G1, G2, . . . , Gn to define a plurality of pixel regions.

[0062] A plurality of TFTs are formed at each crossing point between the respective gate line and the respective data line. A plurality of pixel electrodes 37 are formed so that each pixel electrode is connected with a drain electrode of each respective TFT.

[0063] At least one of the first data line D1 and the last data line Dn has a portion that extends into the pixel region toward the pixel electrode 37. The other data lines D2, D3, . . . , Dn-1 do not have such a portion. Therefore, the pixel electrodes 37a adjacent to the one of the first data line D1 and the last data line Dn have a smaller area than the pixel electrodes 37 adjacent the remaining data lines D2, . . . , Dn-1. The smaller area of the pixel electrode 37a means reduction of an aperture ratio.

[0064] In FIG. 3, a shaded region indicates an oblique region where no pixel electrodes 37 and 37a are formed. Luminance is higher in the oblique region than in the regions where the pixel electrode is formed. For this reason, there is an uneven luminance distribution over the whole LCD panel.

[0065] To obtain even luminance distribution, a method is provided for reducing aperture ratio in a pixel electrode region adjacent to the oblique region. To this end, as shown in FIG. 3, portions of the first data line D1 and the last data line Dn are made to be wider than the other data lines D2, D3, . . . , Dn-1, so that the aperture ratio in a corresponding region is reduced. At this time, the reduced aperture ratio is within the range of about 10~15% lower than the aperture ratio of the other pixel electrode regions.

[0066] FIG. 4 is a sectional view taken along line I-I' of FIG. 3. Referring to FIG. 4, the gate insulating film 31 is formed on the first substrate 31. The first data line D1 and the last data line Dn have the greater widths than the other data lines D2, D3, . . . , Dn-1 on the gate insulating film 32.

[0067] At this time, although not shown, a gate electrode of the TFT is formed on the first substrate 31. A semiconductor layer is formed on the gate insulating film 32 and is used as a channel of the TFT. Source and drain electrodes are formed on the semiconductor layer by the same process as the process for forming the data lines.

[0068] A passivation film 33 is formed on the entire surface including the data lines D1, D2, . . . , Dn. Pixel electrodes 37 and 37a are formed on the passivation film 33. At this time, an area of the pixel electrode adjacent to the first data line D1 and the last data line Dn is smaller than areas of the other pixel electrodes because the area of the pixel electrode adjacent to the first data line D1 is by the area of the extended portion of the first data line.

[0069] The pixel electrode includes a transparent material such as ITO. The data line includes a metal material such as

Al, Cr, Mo, Ta, and Al alloy. Accordingly, the pixel electrode 37a adjacent to the first data line D1, and the last data line Dn have less area than the other pixel electrodes 37 and the data lines D1 and Dn have larger widths, so that transmittivity of light irradiated from a back light (not shown) is reduced to reduce the aperture ratio.

[0070] Accordingly, relatively high luminance in the region where the pixel electrode is not formed is compensated by reducing the aperture ratio around the region, so that even luminance distribution can be obtained over the LCD panel as a whole.

[0071] Meanwhile, FIG. 5 is a plan view illustrating an LCD panel according to the second embodiment of the present invention. FIG. 6 is a sectional view taken along line II-II' of FIG. 5.

[0072] In the LCD panel according to the second embodiment of the present invention, as shown in FIG. 5, the width of the first gate line that does not drive a pixel electrode is controlled to remove relatively high luminance in the region adjacent to the first data line, as indicated by the shading in FIG. 5 (oblique region). The width of the first gate line G1 is greater than the width of the other gate lines G2, G3, . . . , Gn. Thus, the aperture ratio is reduced because of the decrease in area of the pixel region that is adjacent to the first gate line G1. At this time, the width of the gate line G1 is controlled so that the aperture ratio is reduced by the range of about 10~15%. In FIG. 5, the width a of the first gate line G1 is greater than the width of a' of the other gate lines G2, . . . , Gn, i.e., $a > a'$, and the width b of the pixel region adjacent to the first gate line G1 is less than the width b' of the other pixel regions, i.e. $b < b'$.

[0073] That is, a plurality of the gate lines G1, G2, . . . , Gn are formed on the first substrate 31, and a gate insulating film 32 is formed on the entire surface including the gate lines. The data line D1 is formed to cross the gate lines.

[0074] The first gate line G01 of the gate lines G1, G2, . . . , Gn is patterned to have a greater width than widths of the other gate lines G2, G3, . . . , Gn.

[0075] Accordingly, the pixel electrode 37 has a relatively small area as compared to the other pixel regions because the width of the first gate line G1 is greater than the width of the other gate lines G2, . . . , Gn. Thus, the aperture ratio is reduced by the decreased area of the pixel electrode.

[0076] As described above, in FIG. 3 and FIG. 4, to remove relatively high luminance occurring before the first data line and after the last data line, the first and last data lines D1 and Dn are patterned to have greater widths than the other data lines. In FIG. 5 and FIG. 6, to remove relatively high luminance occurring above the first gate line, the first gate line is patterned to have a greater width than the other gate lines.

[0077] Therefore, in the case where an LCD panel is formed based on FIG. 3 and FIG. 4, relatively high luminance occurring at the front end of the first gate and data lines and at the rear end of the last data line can be removed.

[0078] FIG. 7 is a plan view illustrating an LCD panel according to the third embodiment of the present invention.

[0079] In the LCD panel according to the third embodiment of the present invention, as shown in FIG. 7, relatively

high luminance occurring along the periphery of the LCD panel is removed by increasing the width of the first gate line and at the same time increasing the widths of the first data line D1 and the last data line Dn.

[0080] As described above, the aperture ratio of the pixel region adjacent to the first data line D1 and the last data line Dn is reduced by increasing the widths of the first data line D1 and the last data line Dn. At the same time, the aperture ratio of the pixel region adjacent to the first gate line G1 is reduced by increasing the width of the first gate line G1. Thus, relatively high luminance occurring in the oblique region (indicated by shading in FIG. 7) is removed.

[0081] While relatively high luminance has been removed by controlling the widths of the gate line and the data line, the relatively high luminance may be removed by controlling the width of a black matrix pattern formed on a second substrate.

[0082] FIG. 8 is a plan view illustrating an LCD panel according to the fourth embodiment of the present invention.

[0083] In the LCD panel according to the fourth embodiment of the present invention, as shown in FIG. 8, the black matrix pattern 41 on the second substrate 31a, which corresponds to the first gate line G1 formed on the first substrate 31, the first data line D1 and the last data line Dn, is patterned to be wider than the other regions. Thus, the aperture ratio of the pixel region adjacent to the first gate line G1, the first data line D1 and the last data line Dn is reduced. The width C of portions of the black matrix over the first and last data lines D1 and Dn is greater than the width C' of other portions of the black matrix over the other data lines. (see $C > C'$ in the drawing). The width D of a portion of the black matrix over the first gate line G1 is greater than the width D' of portions of the black matrix over the other gate lines G2 . . . Gn, i.e. $D > D'$. Thus the reduction in aperture ratio is within the range of about 10~15%.

[0084] In other words, as shown in FIG. 9, the black matrix pattern 41 on the second substrate 31a corresponding to the first data line D1 and the last data line Dn is patterned to be wider than the other regions.

[0085] As described above, in this embodiment the width of the black matrix pattern 41 formed on the second substrate 31a is controlled, while the widths of the gate and data lines are maintained as they are. Thus, the aperture ratio of the pixel electrode region adjacent to a region where the pixel electrode is not formed, is reduced, thereby removing relatively high luminance occurring in the region where the pixel electrode is not formed.

[0086] In FIG. 9 reference numeral "42," which is not described, denotes a color filter pattern that displays colors. Reference numeral "43" denotes a common electrode for applying a voltage to a liquid crystal layer 44 together with the pixel electrode 37.

[0087] Meanwhile, in addition to the method for controlling the width of the black matrix pattern, a light-shielding pattern that can reduce the aperture ratio may be formed in the pixel region adjacent to the region where the relatively high luminance occurs.

[0088] FIG. 10 is a plan view illustrating an LCD panel according to the fifth embodiment of the present invention. FIG. 11 is a sectional view taken along line IV-IV' of FIG. 10.

[0089] In other words, in the LCD panel according to the fifth embodiment of the present invention, as shown in **FIG. 10** and **FIG. 11**, a plurality of gate lines **G1**, **G2**, . . . , **Gn** are arranged to cross a plurality of data lines **D1**, **D2**, . . . , **Dn** so that a plurality of pixel regions are defined. A thin film transistor (TFT) is formed at each crossing point of the respective gate line and the respective data line. A light-shielding pattern **51** is formed in the pixel region adjacent to the first gate line **G1**, the first data line **D1** and the last data line **Dn**. A pixel electrode **37** is formed in each pixel region.

[0090] In other words, the light-shielding pattern **51** is formed in the pixel region adjacent to the region where relatively high luminance occurs, so that the aperture ratio is reduced by about 10~15%. As a result, an even LCD panel having no relatively high luminance can be obtained.

[0091] The light-shielding pattern **51** is formed of the same material as that of the gate line when the gate line is formed. Alternatively, the light-shielding pattern **51** may be formed of the same material as that of the data line when the data line is formed.

[0092] As described above, the LCD panel of the present invention has the following advantages.

[0093] The relatively high luminance occurring in the region where the pixel electrode is not formed is removed by reducing the aperture ratio of the pixel region adjacent to the high luminance region, which results in the same transmittivity over the LCD panel as a whole. As a result, even luminance distribution having no relatively high luminance can be obtained, thereby providing an LCD panel having high picture quality.

[0094] The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.

What is claimed is:

1. A liquid crystal display (LCD) panel comprising:

a first substrate provided with a plurality of gate and data lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement;

a second substrate provided with a black matrix layer to shield portions other than the pixel regions from light; and

a liquid crystal layer injected between the first and second substrates, wherein the pixel regions in a peripheral portion of the matrix arrangement has an aperture ratio lower than that of the pixel regions in other portions of the matrix arrangement.

2. The liquid crystal display panel of claim 1, wherein a first gate line among the gate lines has a greater width than widths of the other gate lines so as to allow the pixel regions in the peripheral portion to obtain an aperture ratio lower than that of the pixel regions in the other portions.

3. The liquid crystal display panel of claim 1, wherein a first data line or a last data line among the data lines has a greater width than widths of the other data lines so as to

allow the pixel regions in the peripheral portion to obtain an aperture ratio lower than that of the pixel regions in the other portions.

4. The liquid crystal display panel of claim 1, wherein the black matrix layer corresponding to at least one of a first gate line, a first data line and a last data line has a greater width than widths of the black matrix layer corresponding to the other portions so as to allow the pixel regions in the peripheral portion to obtain an aperture ratio lower than that of the pixel regions in the other portions.

5. The liquid crystal display panel of claim 1, further comprising a light-shielding pattern in the pixel regions at the peripheral portion so as to allow the pixel regions at the peripheral portion to obtain an aperture ratio lower than that of the pixel regions at the other portions.

6. The liquid crystal display panel of claim 1, wherein an aperture ratio of the pixel regions in the peripheral portion is about 10~15% lower than aperture ratios of the pixel regions at the other portions.

7. An liquid crystal display panel comprising:

a plurality of gate lines arranged in one direction at constant intervals;

a plurality of data lines arranged at constant intervals to be substantially perpendicular to the gate lines to define a plurality of pixel regions in a matrix arrangement; and

a plurality of pixel electrodes, wherein one pixel electrode is in each pixel region, wherein the pixel electrodes at a peripheral portion of the matrix arrangement are narrower than the pixel electrodes at other portions of the matrix arrangement.

8. The liquid crystal display panel of claim 7, wherein a gate line that does not drive the pixel electrode among the gate lines has a greater width than widths of other gate lines.

9. The liquid crystal display panel of claim 7, wherein at least one of a first data line and a last data line among the data lines has a greater width than widths of other data lines.

10. The liquid crystal display panel of claim 7, wherein area of the pixel electrodes adjacent to at least one of a first data line and a last data line is less than areas of the pixel electrodes at the other portions.

11. An liquid crystal display panel, comprising:

a first substrate provided with a plurality of gate and data lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement;

a second substrate provided with a black matrix layer to shield portions other than the pixel regions from light; and

a liquid crystal display layer injected between the first and second substrates, wherein portions of the black matrix layer corresponding to at least one of a first data line and a last data line among the data lines has a greater width than portions of the black matrix layer corresponding to other data lines.

12. The liquid crystal display panel of claim 11, wherein a portion of the black matrix layer corresponding to a first gate line among the gate lines has a greater width than portions of a the black matrix layer corresponding to other gate lines.

13. An liquid crystal display panel comprising:

a plurality of gate lines arranged in one direction at constant intervals;

a plurality of data lines arranged at constant intervals to be substantially perpendicular to the gate lines to define a plurality of pixel regions in a matrix arrangement; and

a plurality of light-shielding patterns in at least one of the pixel regions at a surrounding portion among the pixel regions.

14. The liquid crystal display panel of claim 13, wherein the light-shielding patterns are in the pixel regions adjacent to at least one of the a first data line and a last data line among the data lines.

15. The liquid crystal display panel of claim 13, wherein the light-shielding patterns are metal.

16. The liquid crystal display panel of claim 15, wherein the metal is the same material as that of the data lines.

17. An liquid crystal display panel, comprising:

first and second substrates;

a plurality of gate and data lines arranged on the first substrate to define a plurality of pixel regions, the gate lines crossing the data lines;

a plurality of pixel electrodes, wherein at least one pixel electrode is in each pixel region; and

a black matrix pattern formed on the second substrate to shield portions other than the pixel electrodes from light,

wherein width of a first gate line among the gate lines is greater than widths of other gate lines, width of one of a first data line and a last data line among the data lines is greater than widths of other data lines, and width of portions the black matrix pattern corresponding to one of the first gate line, the first data line and the last data line is greater than widths of portions of the black matrix pattern not corresponding to the one of the first gate line, the first data line, and the last data line.

18. The liquid crystal display panel of claim 17, further comprising a plurality of thin film transistors in a crossing portion of a respective gate line and a respective data line.

19. The liquid crystal display panel of claim 17, wherein area of the pixel electrodes adjacent to at least one of the first data line and the last data line is less than areas of other pixel electrodes.

20. The liquid crystal display panel of claim 17, wherein aperture ratio the pixel electrodes adjacent to at least one of the first data line and the last data line is about 10~15% lower than aperture ratios of other pixel electrodes.

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专利名称(译)	液晶显示面板		
公开(公告)号	US20020080309A1	公开(公告)日	2002-06-27
申请号	US10/025904	申请日	2001-12-26
[标]申请(专利权)人(译)	邦永IK KWAK董杨 朴成IL		
申请(专利权)人(译)	邦永IK KWAK董杨 朴成IL		
当前申请(专利权)人(译)	邦永IK KWAK董杨 朴成IL		
[标]发明人	BANG YONG IK KWAK DONG YEUNG PARK SUNG IL		
发明人	BANG, YONG IK KWAK, DONG YEUNG PARK, SUNG IL		
IPC分类号	G02F1/133 G02F1/1335 G02F1/1362 G02F1/1343		
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优先权	1020000080214 2000-12-22 KR		
其他公开文献	US6900860		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种具有高图像质量的均匀亮度的液晶显示 (LCD) 面板。 LCD 面板包括设置有多条栅极线和数据线的第一基板, 栅极线布置成与数据线交叉以限定矩阵排列的多个像素区域; 第二基板, 设置有黑矩阵层, 以遮挡除像素区域以外的部分光; 注入第一和第二基板之间的液晶层, 其中周围部分的像素区域的开口率低于其他部分的像素区域的开口率。

