US007714963B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.: US 7,714,963 B2**
(45) **Date of Patent: May 11, 2010**

(54) **TRANSFLECTIVE LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME**

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(73) Assignee: **LG Display Co., Ltd.**, Seoul (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 993 days.

(21) Appl. No.: **11/372,081**

(22) Filed: **Mar. 10, 2006**

(65) **Prior Publication Data**

US 2007/0058116 A1 Mar. 15, 2007

(30) **Foreign Application Priority Data**

Sep. 9, 2005 (KR) 10-2005-0084196

(51) **Int. Cl.**
G02F 1/1335 (2006.01)

(52) **U.S. Cl.** **349/114**

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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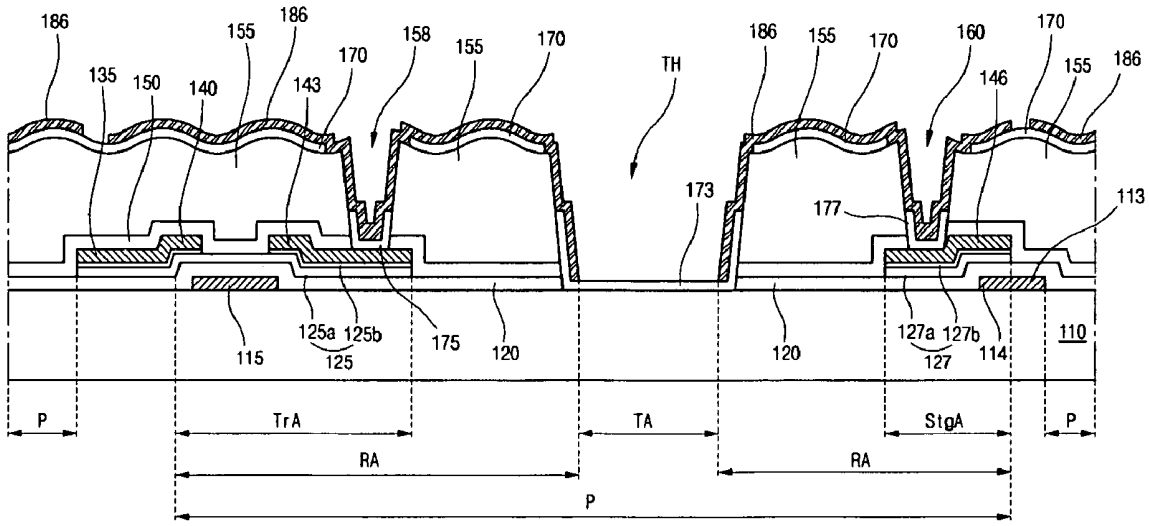
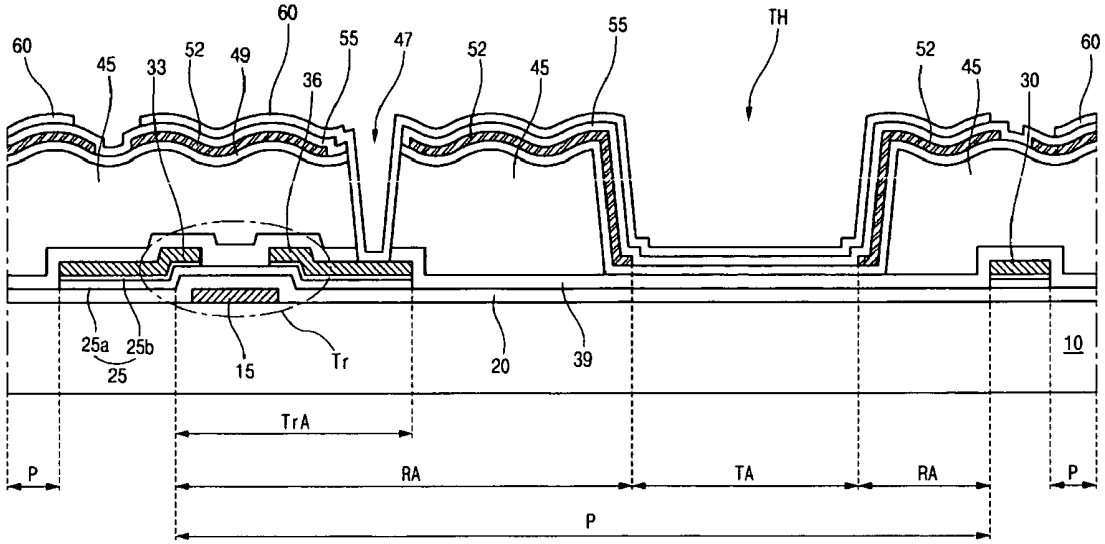
Primary Examiner—Timothy Rude
(74) *Attorney, Agent, or Firm*—Holland & Knight LLP

(57) **ABSTRACT**

An array substrate for a transflective liquid crystal display device includes: a substrate; a gate line and a data line on the substrate, the gate line and the data line crossing each other to define a pixel region including a transmissive area and a reflective area surrounding the transmissive area; a thin film transistor having a gate insulating layer, the thin film transistor electrically connected to the gate line and the data line; a first passivation layer having a drain contact hole exposing a drain electrode of the thin film transistor and a through hole exposing the substrate in the transmissive area; a pixel electrode on the first passivation layer, the pixel electrode contacting the substrate in the transmissive area through the through hole; and a reflective plate on the pixel electrode, the reflective plate being electrically connected to the drain electrode through the drain contact hole and to the pixel electrode.

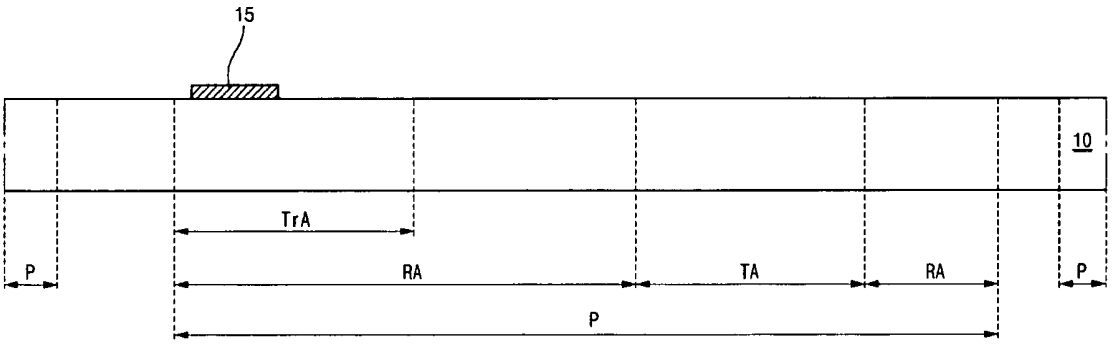
12 Claims, 21 Drawing Sheets





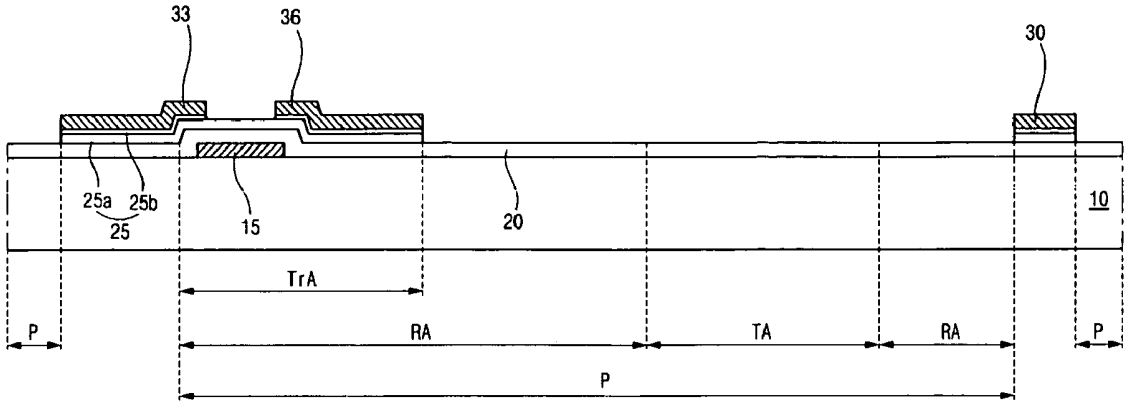
(related art)

FIG. 1



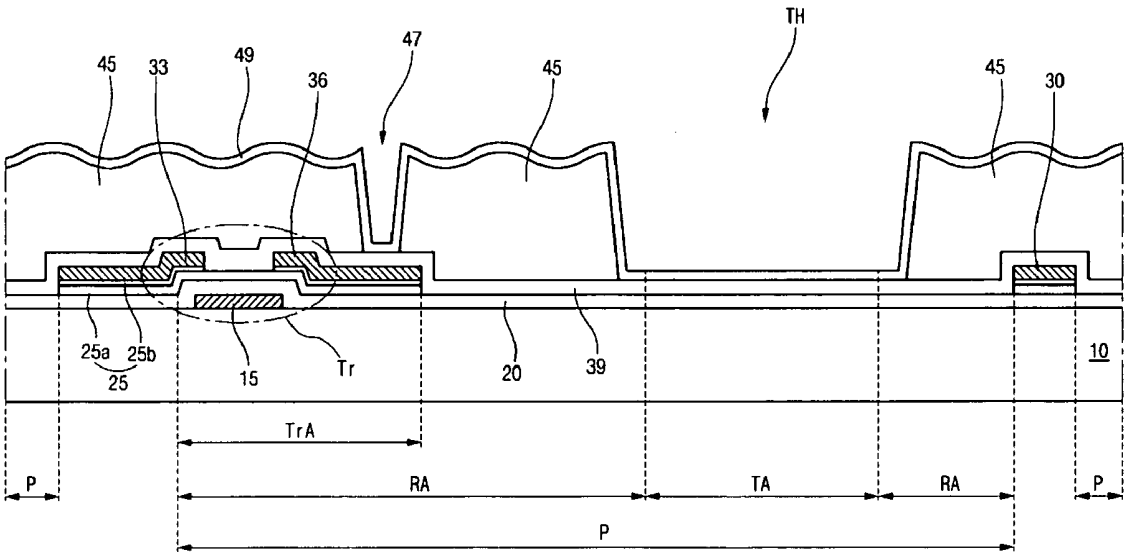
(related art)

FIG. 2A



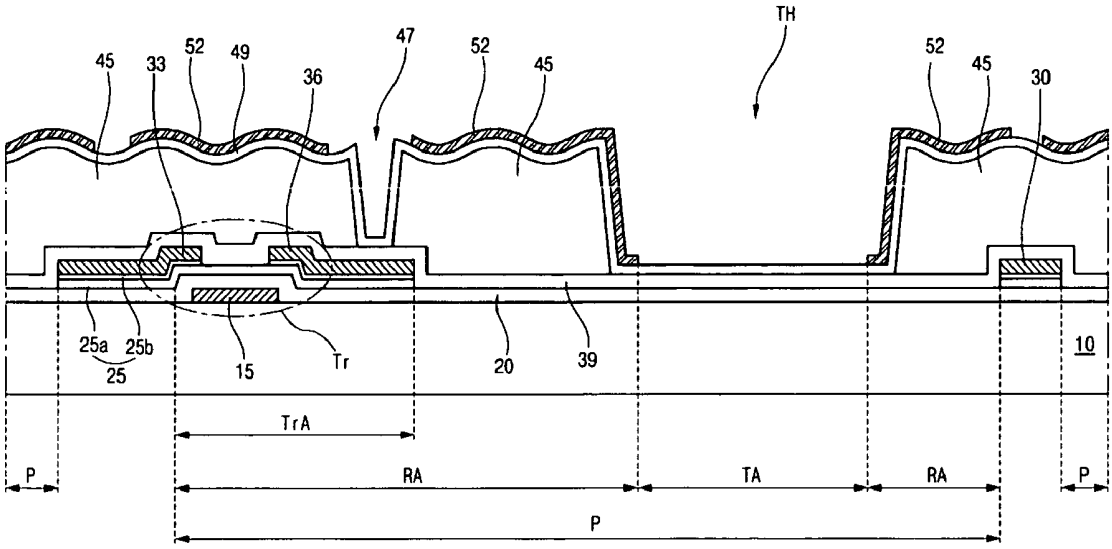
(related art)

FIG. 2B



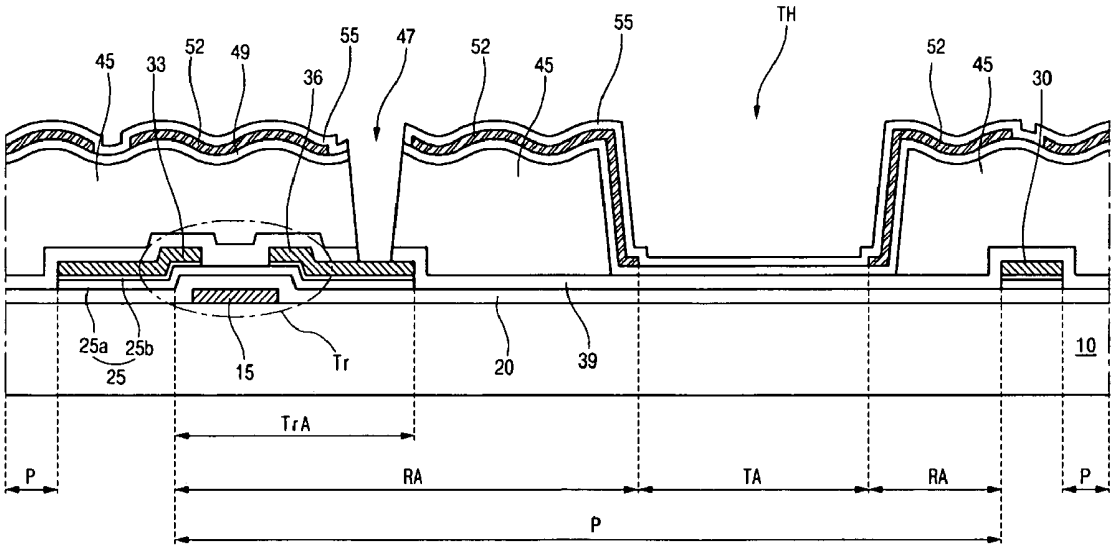
(related art)

FIG. 2C



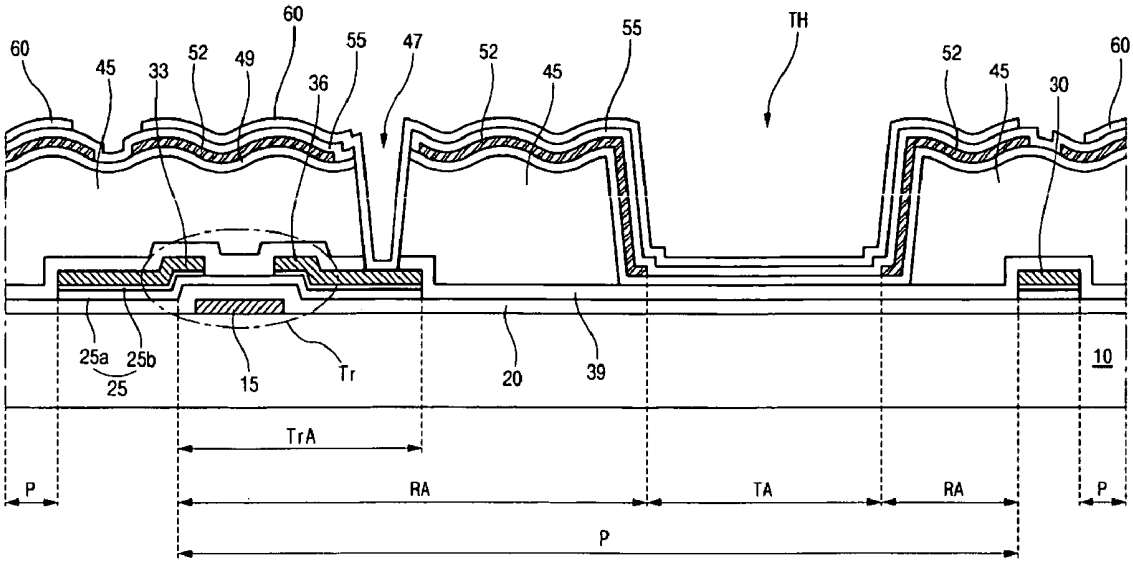
(related art)

FIG. 2D



(related art)

FIG. 2E



(related art)

FIG. 2F

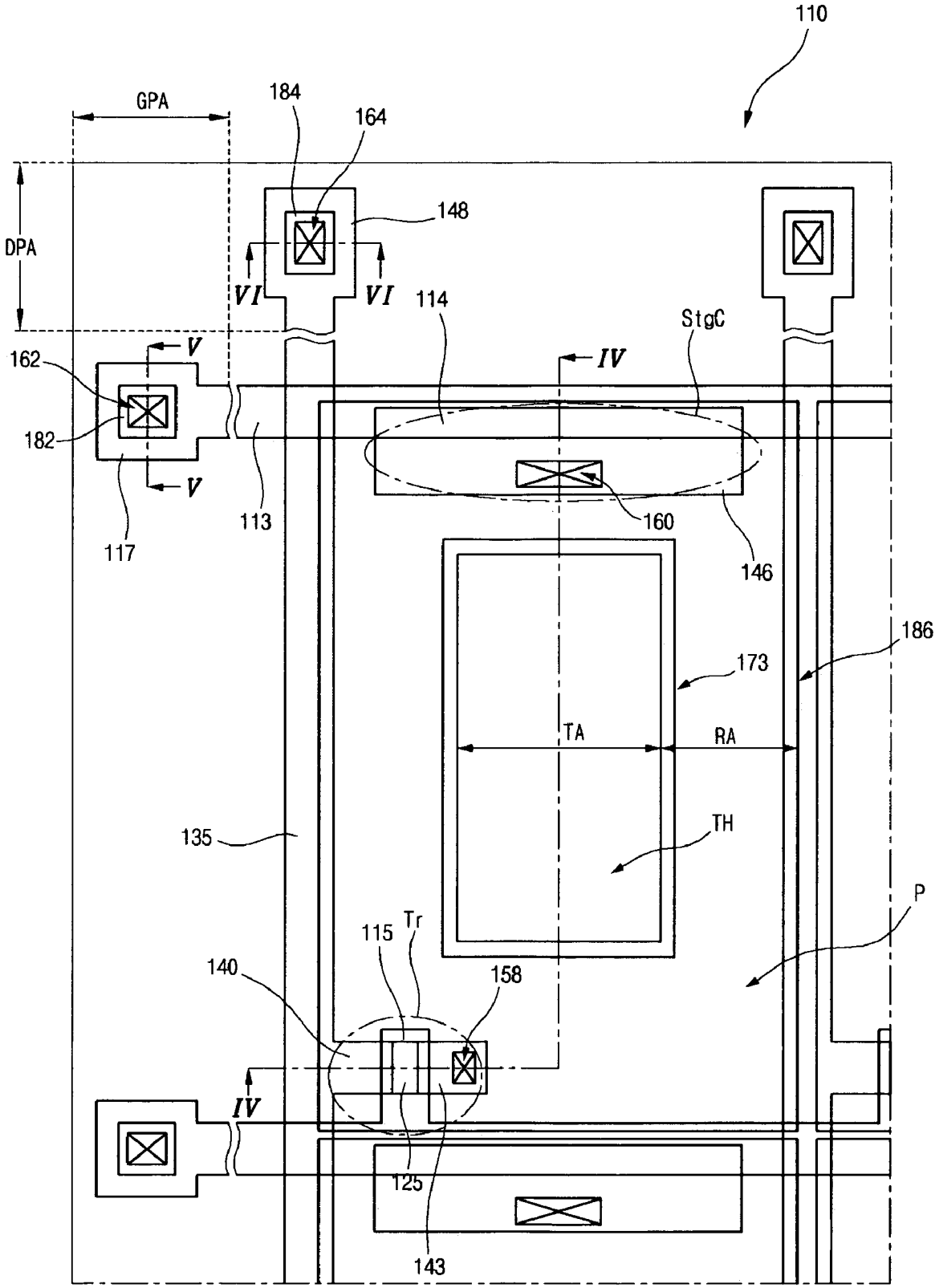

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FIG. 3

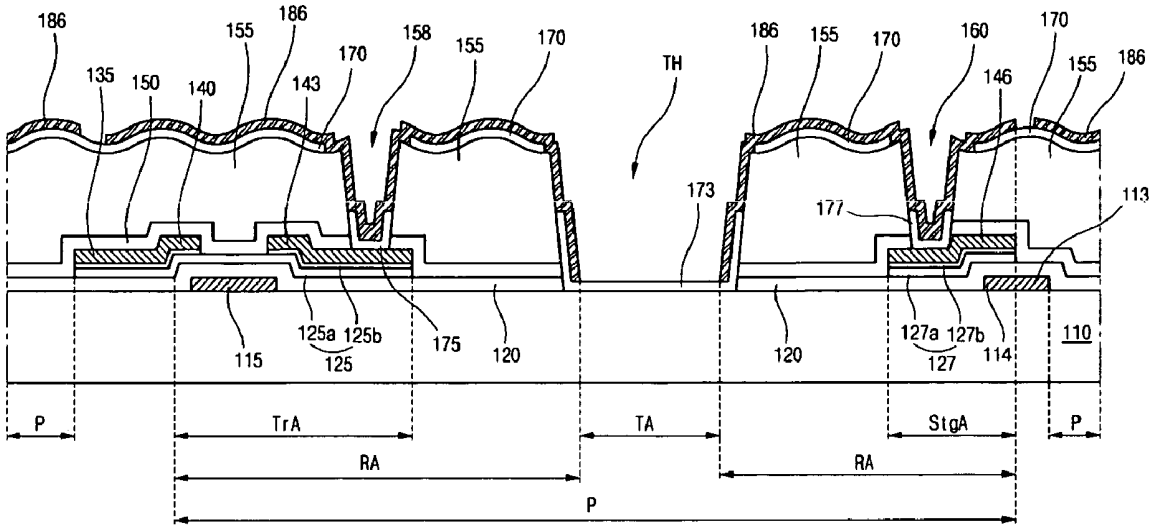
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FIG. 4

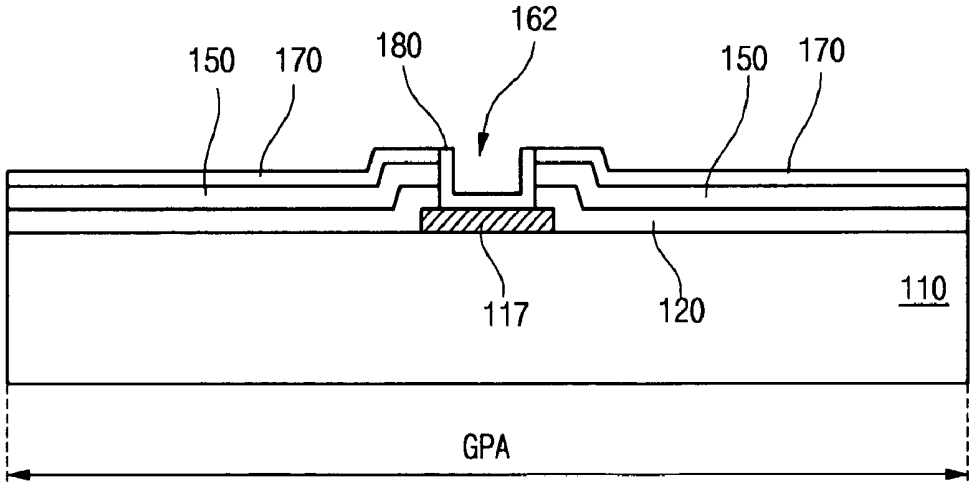
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FIG. 5

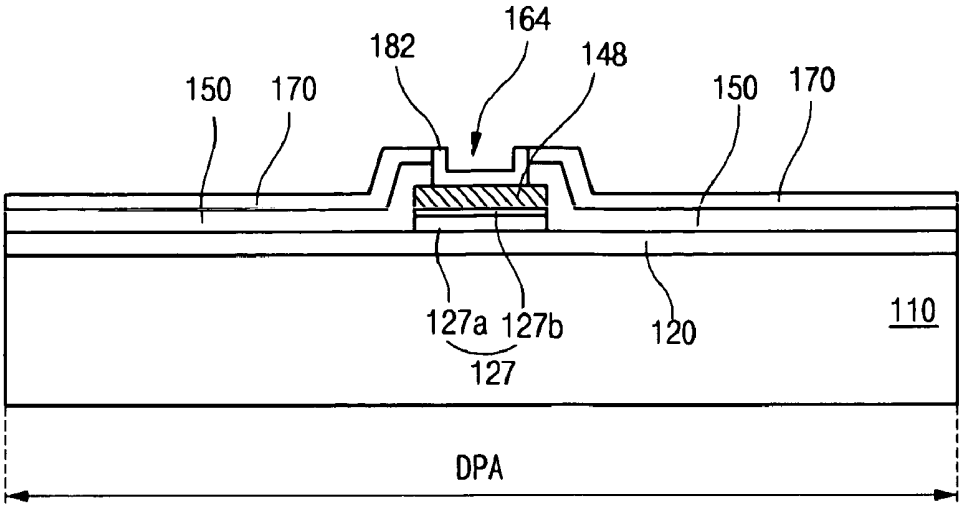
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FIG. 6

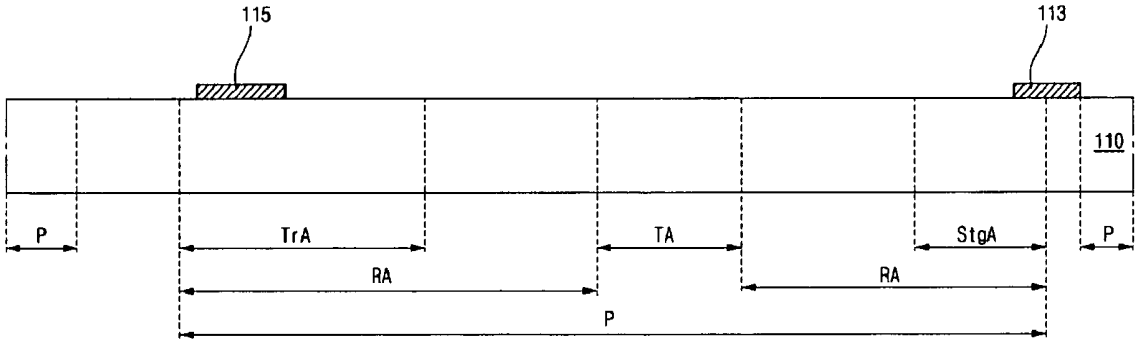
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FIG. 7A

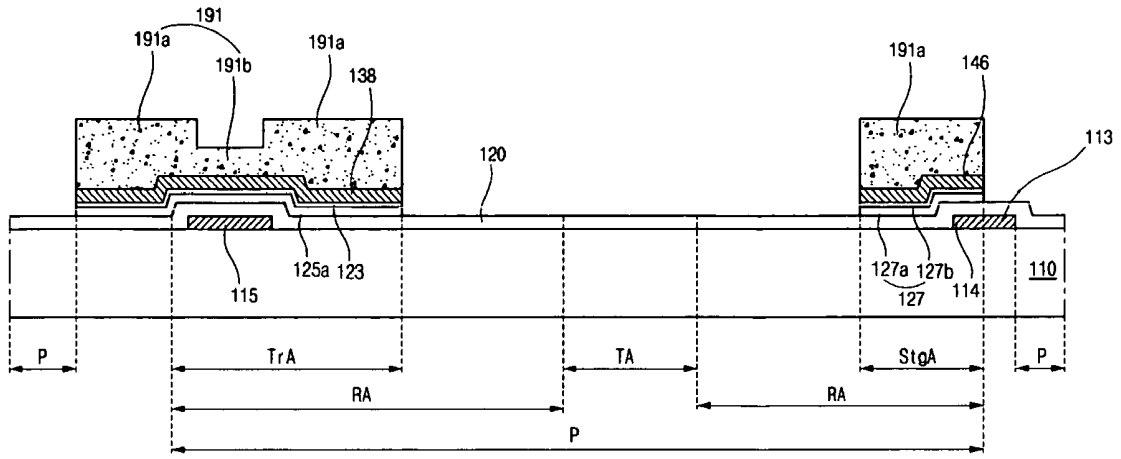

FIG. 7B

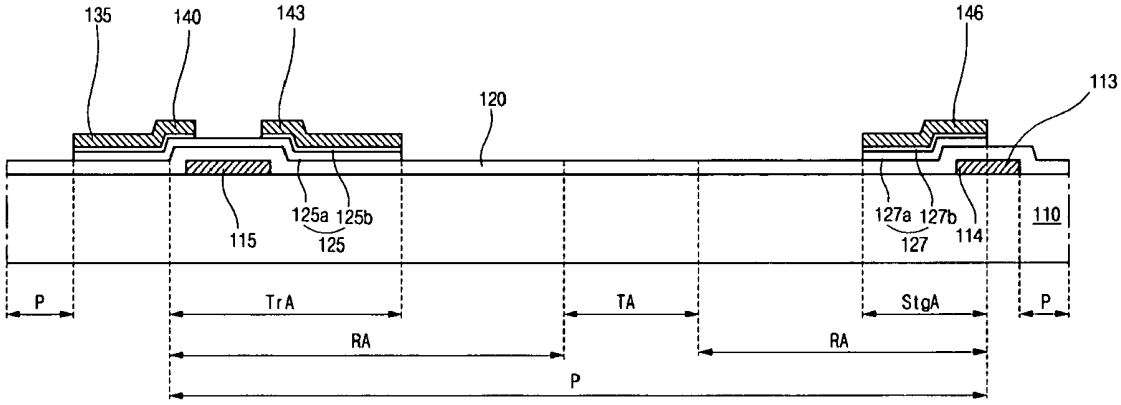

FIG. 7C

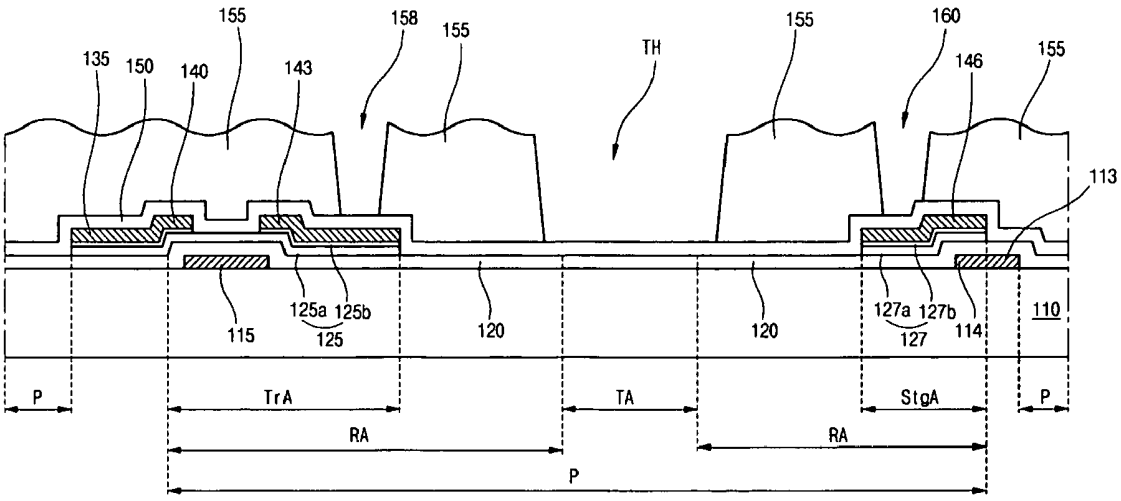

FIG. 7D

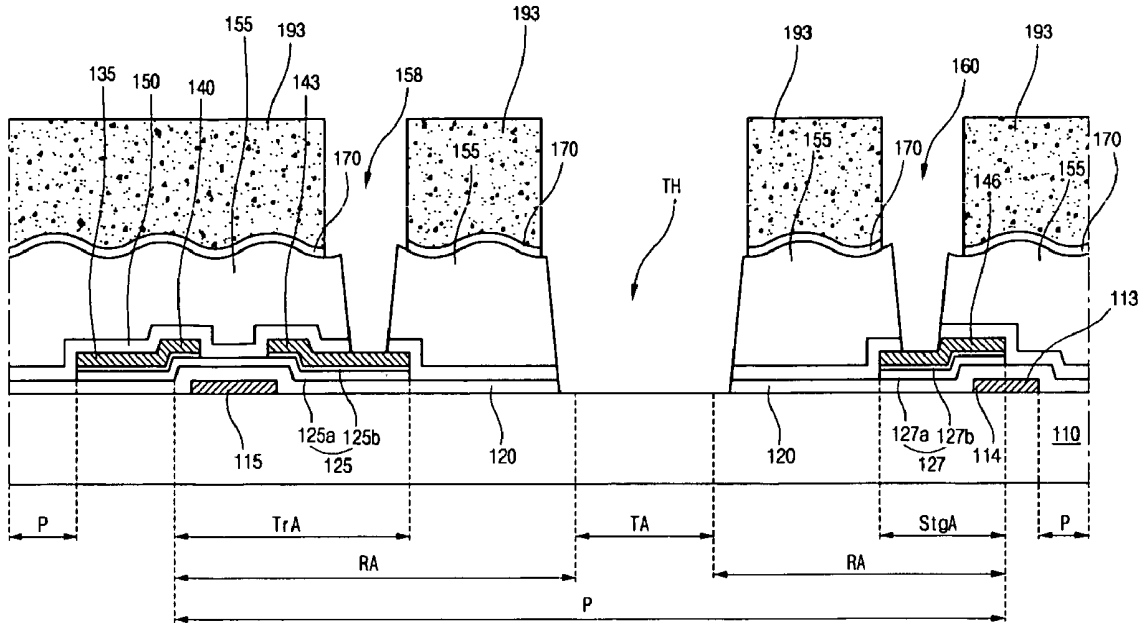
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FIG. 7E

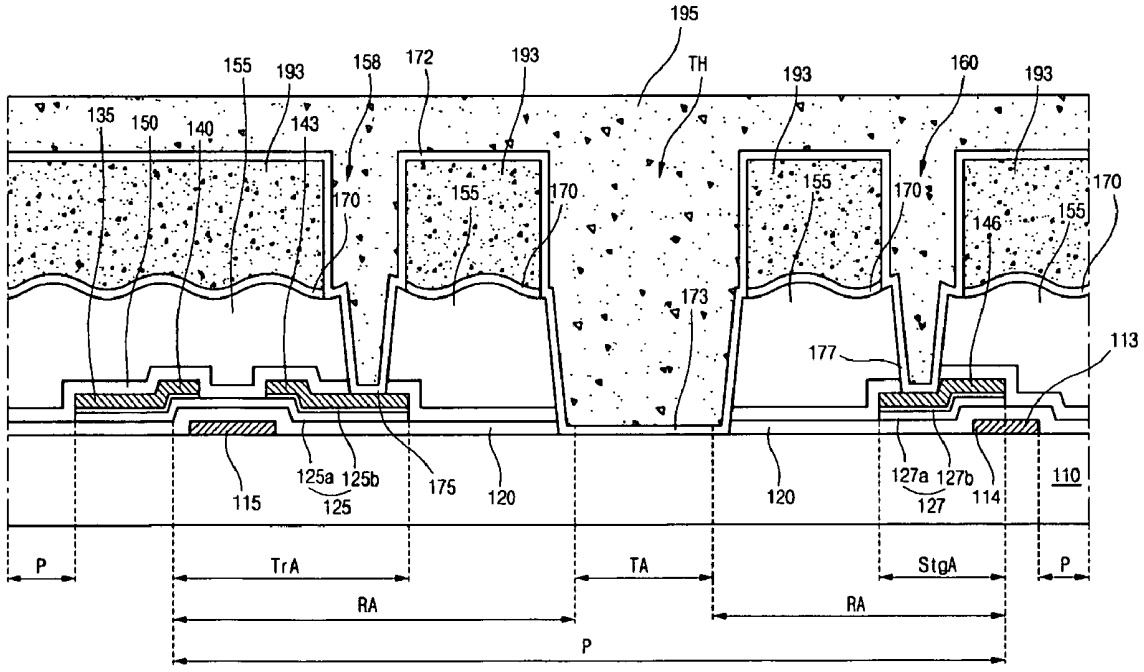
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FIG. 7F

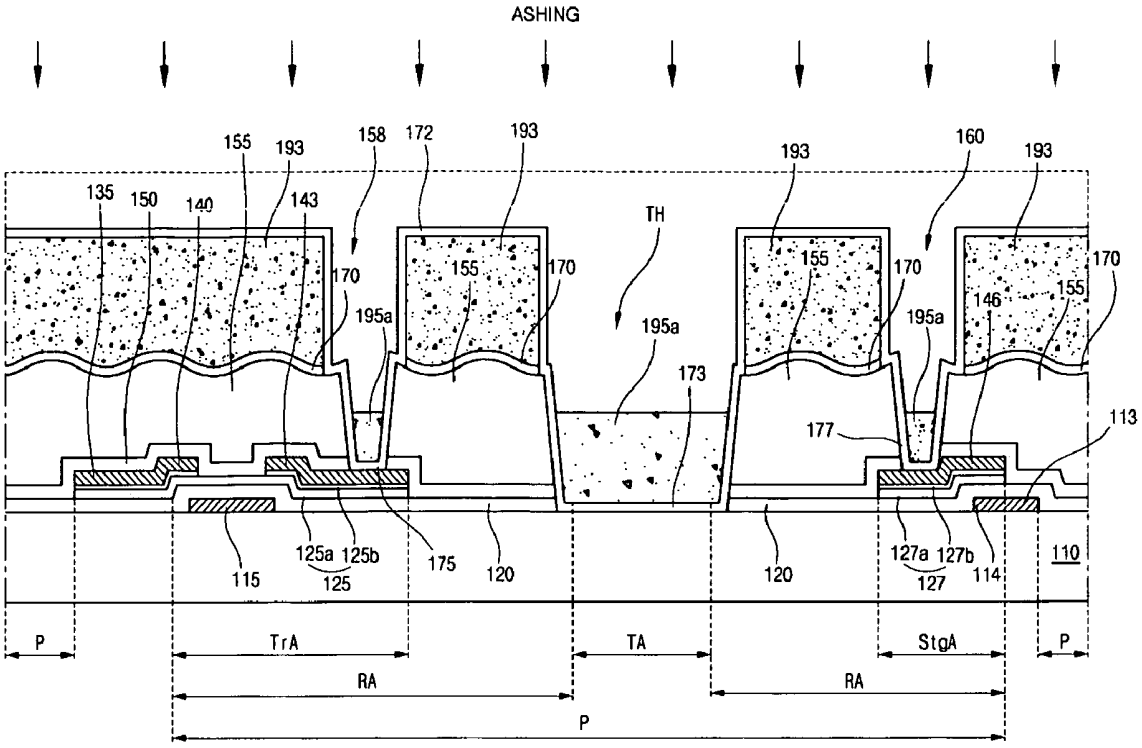
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FIG. 7G

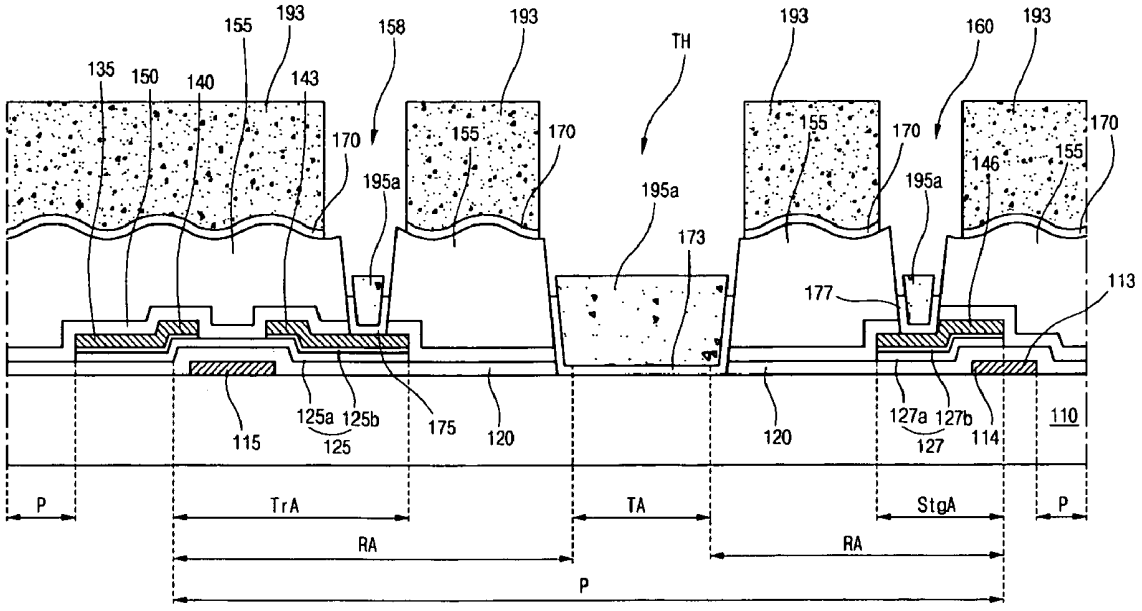
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FIG. 7H

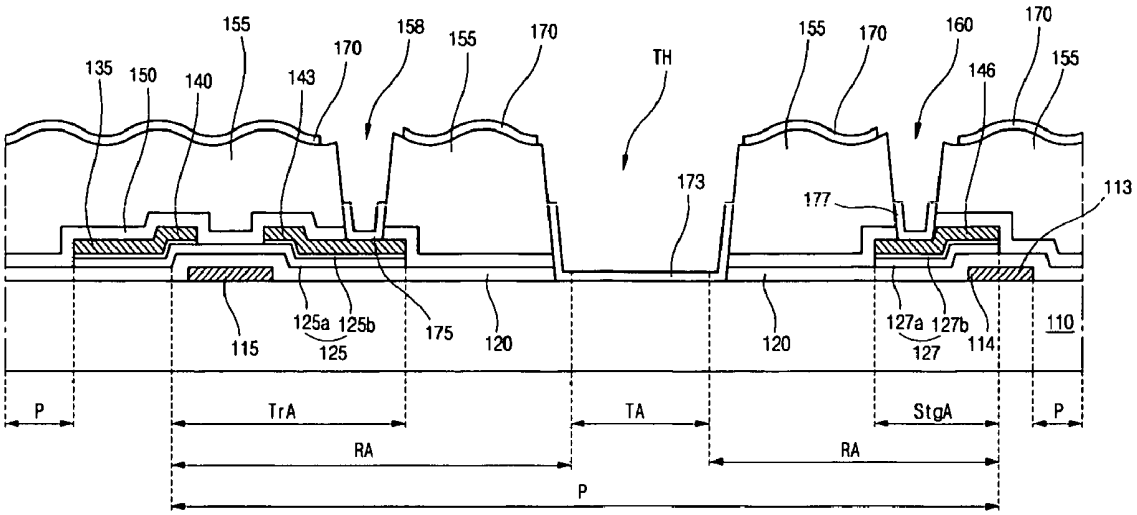
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FIG. 7I

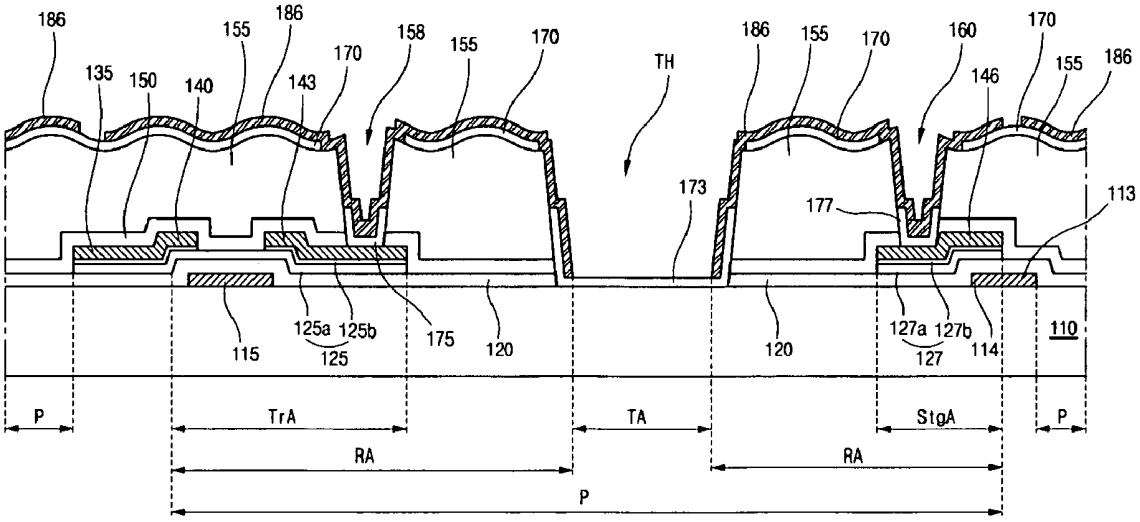
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FIG. 7J

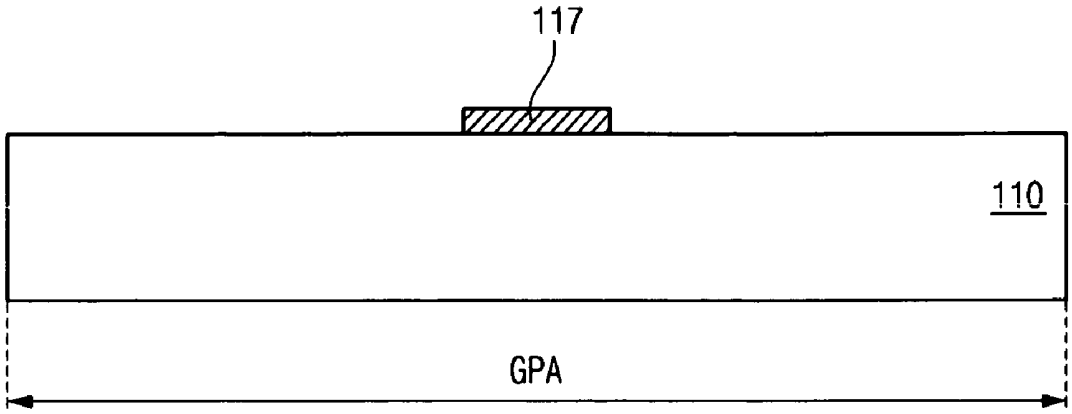


FIG. 8A

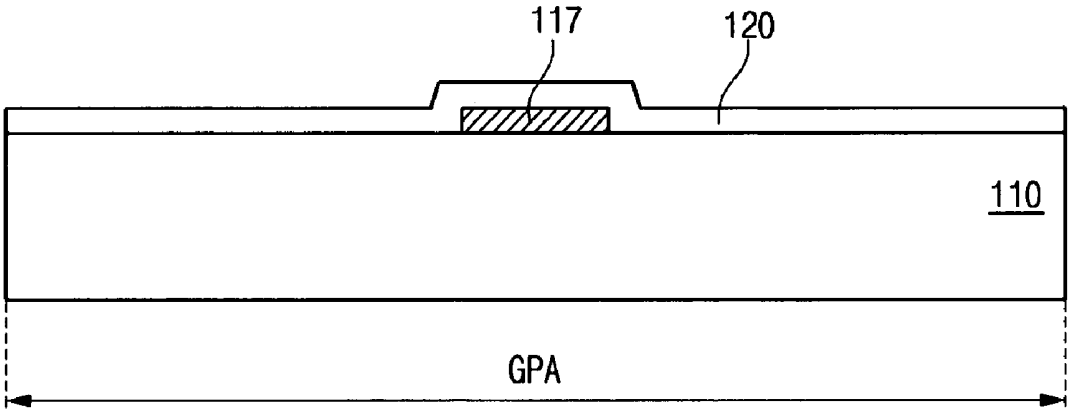


FIG. 8B

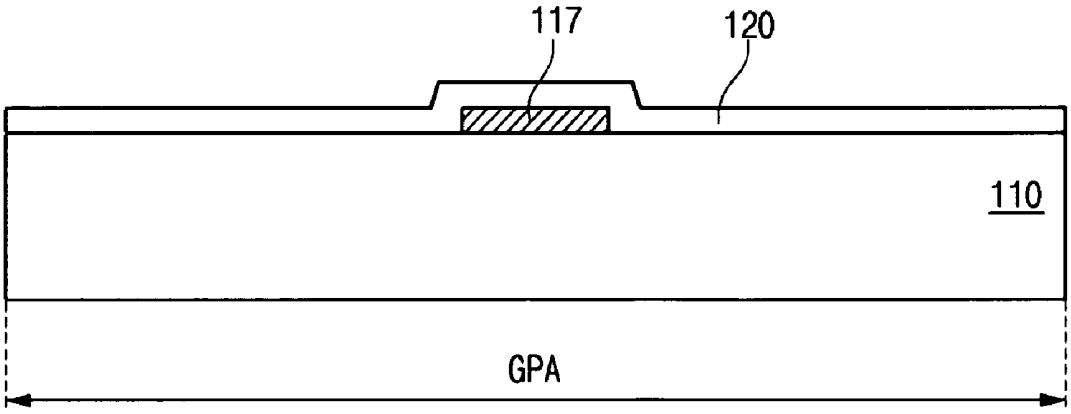
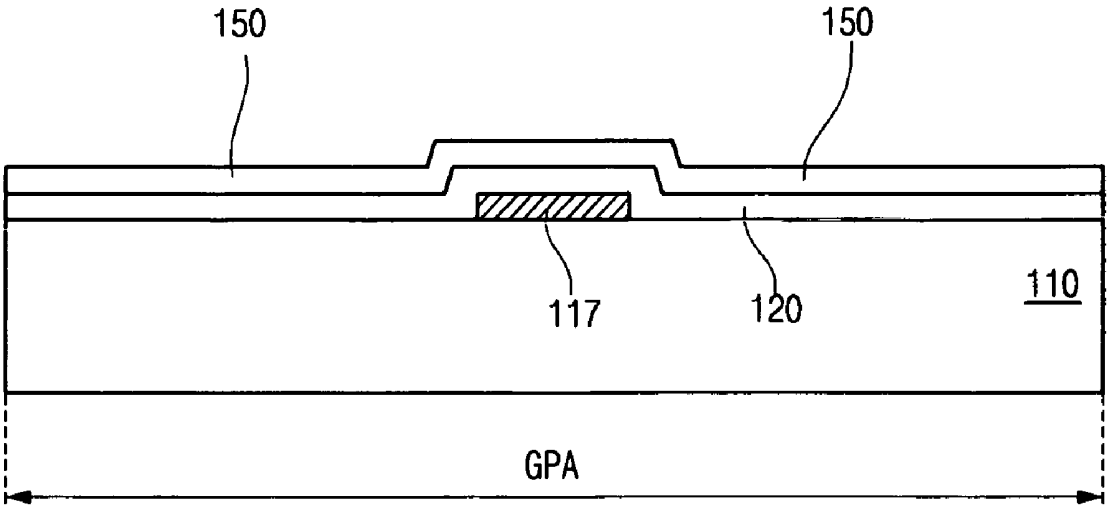


FIG. 8C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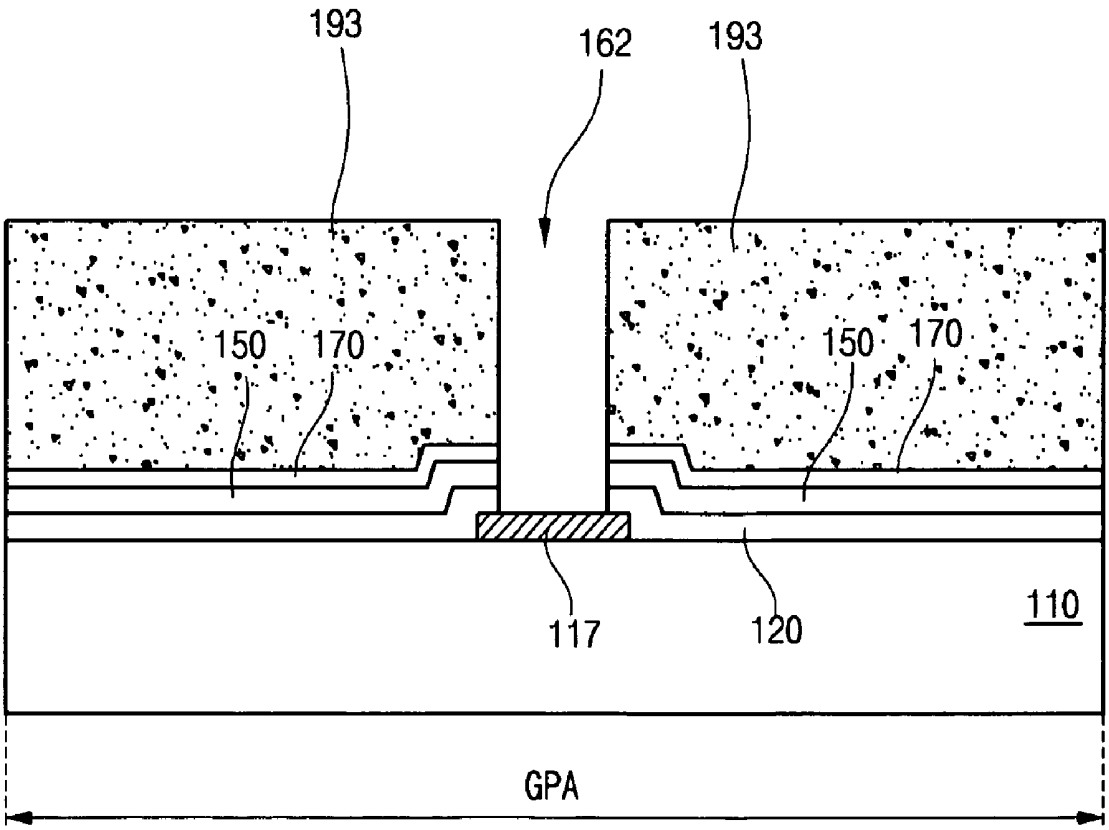
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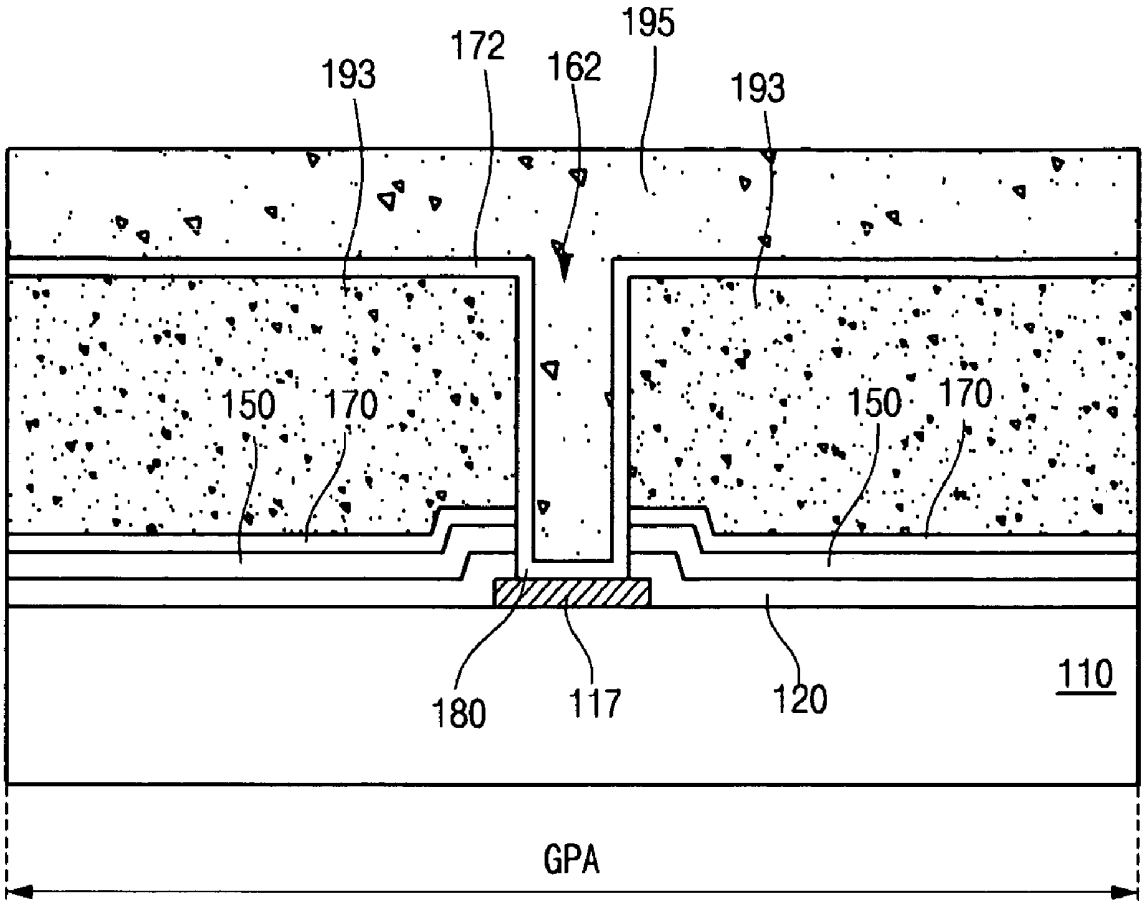

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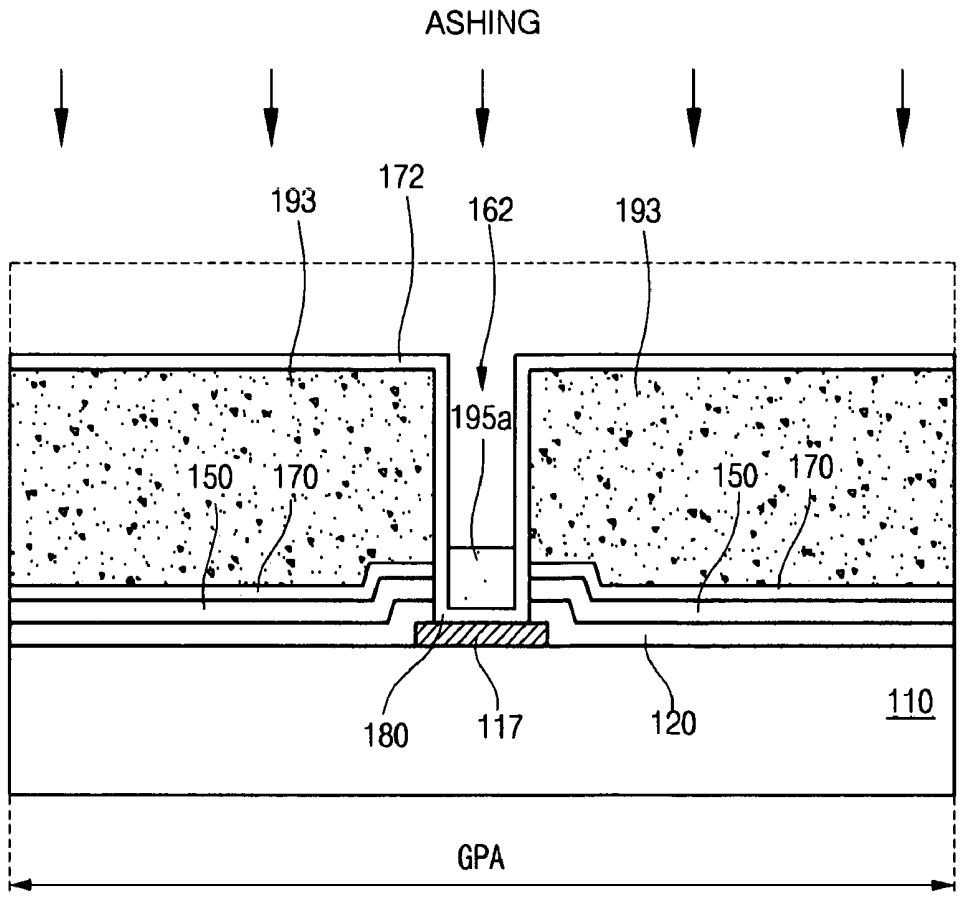
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FIG. 8G

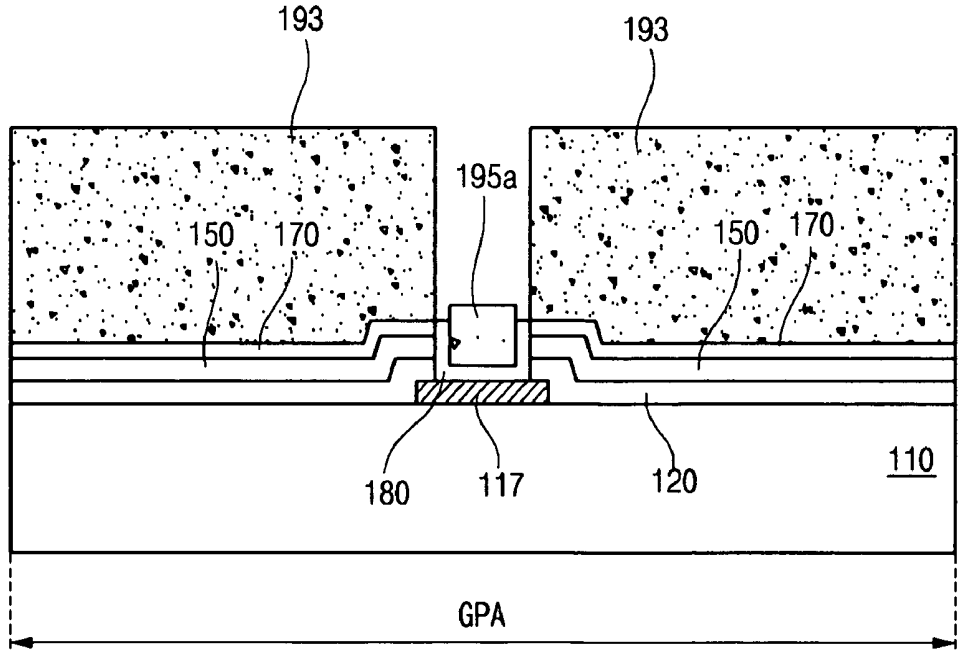
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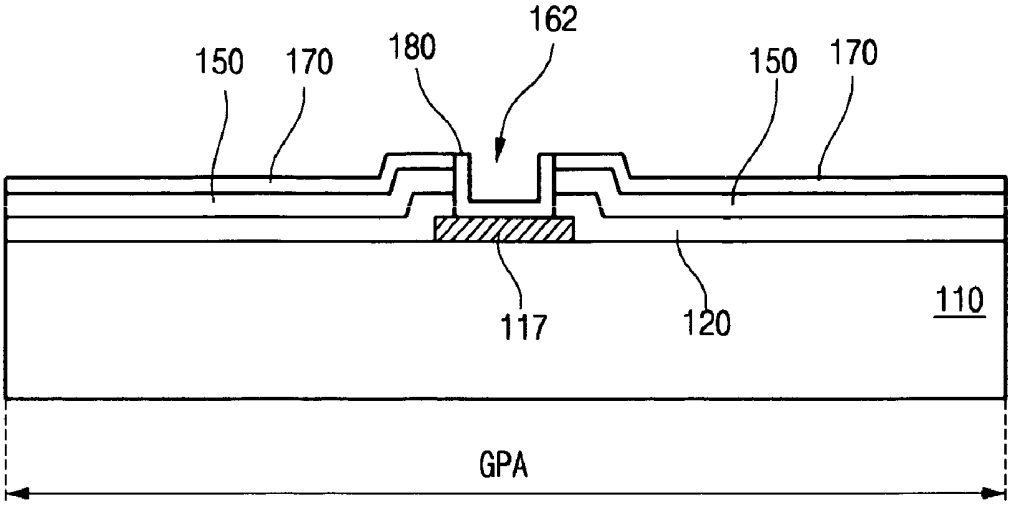
FIG. 8H



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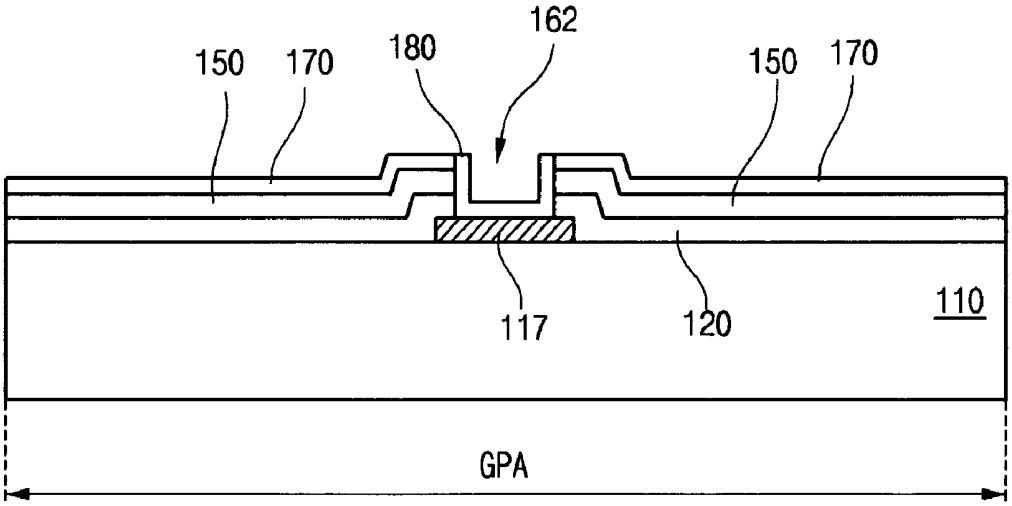

FIG. 8J

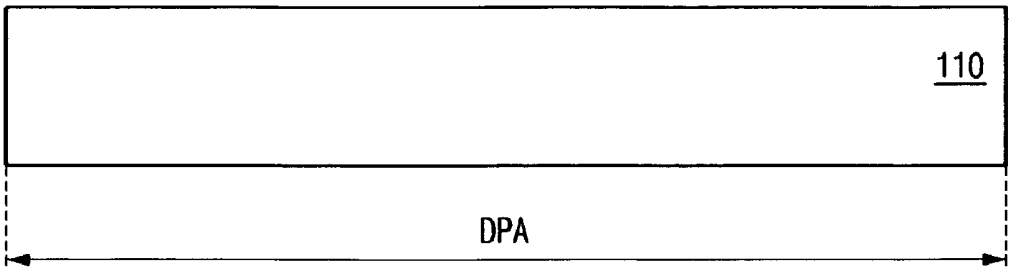

FIG. 9A

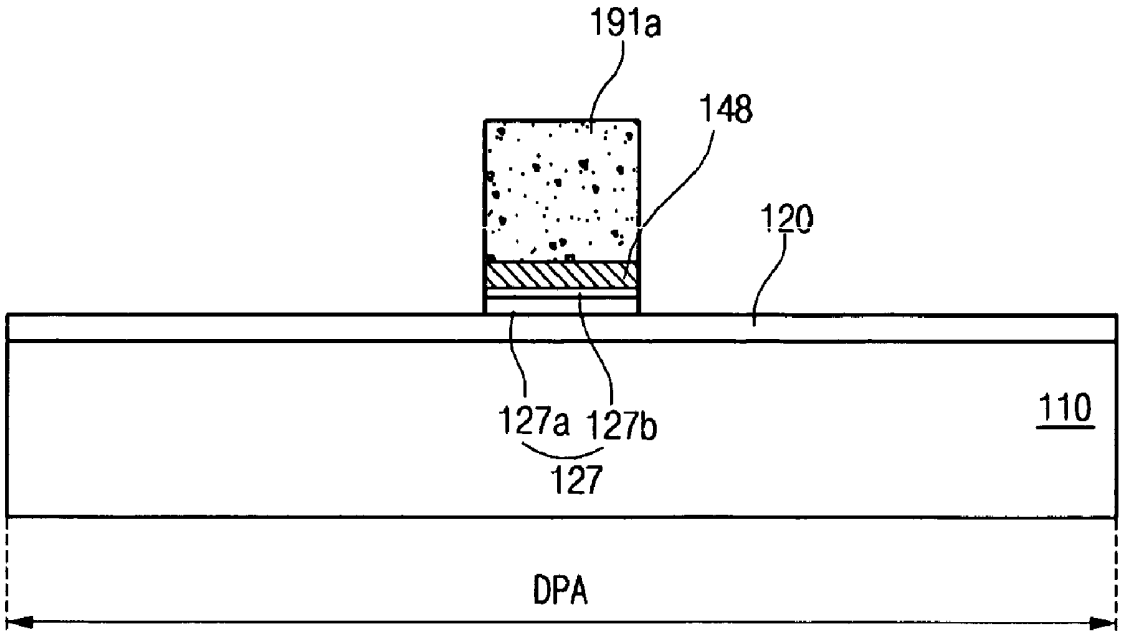
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FIG. 9B

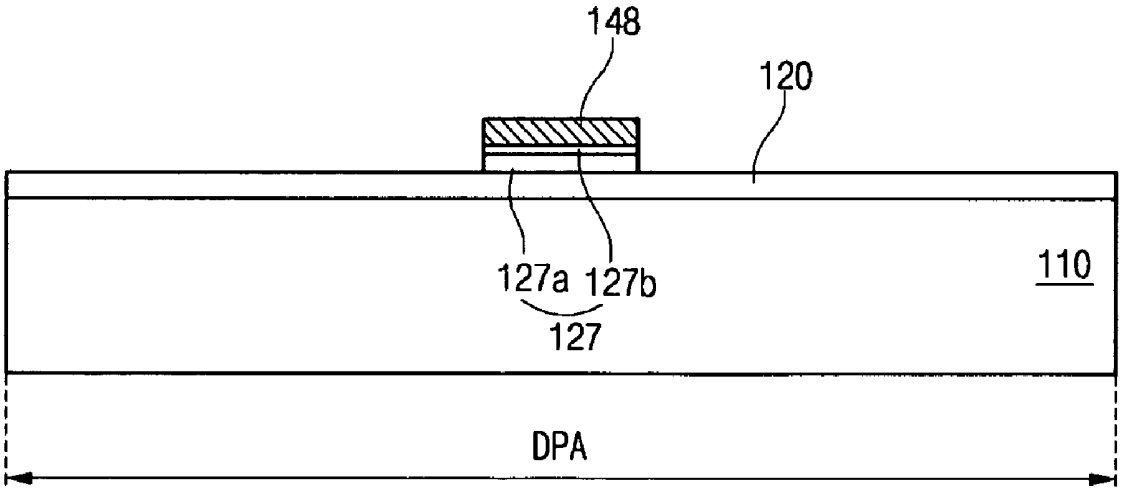
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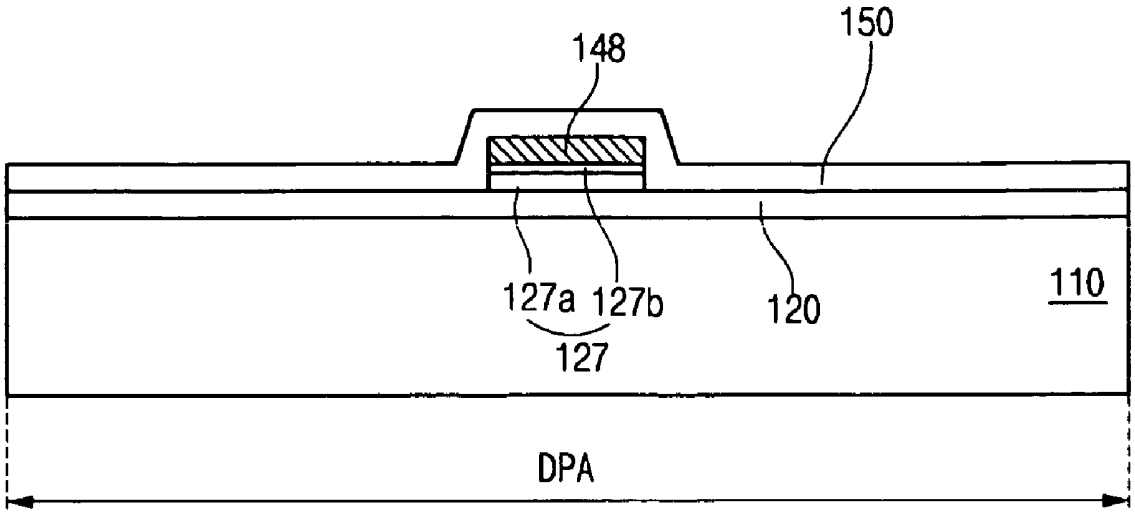
FIG. 9C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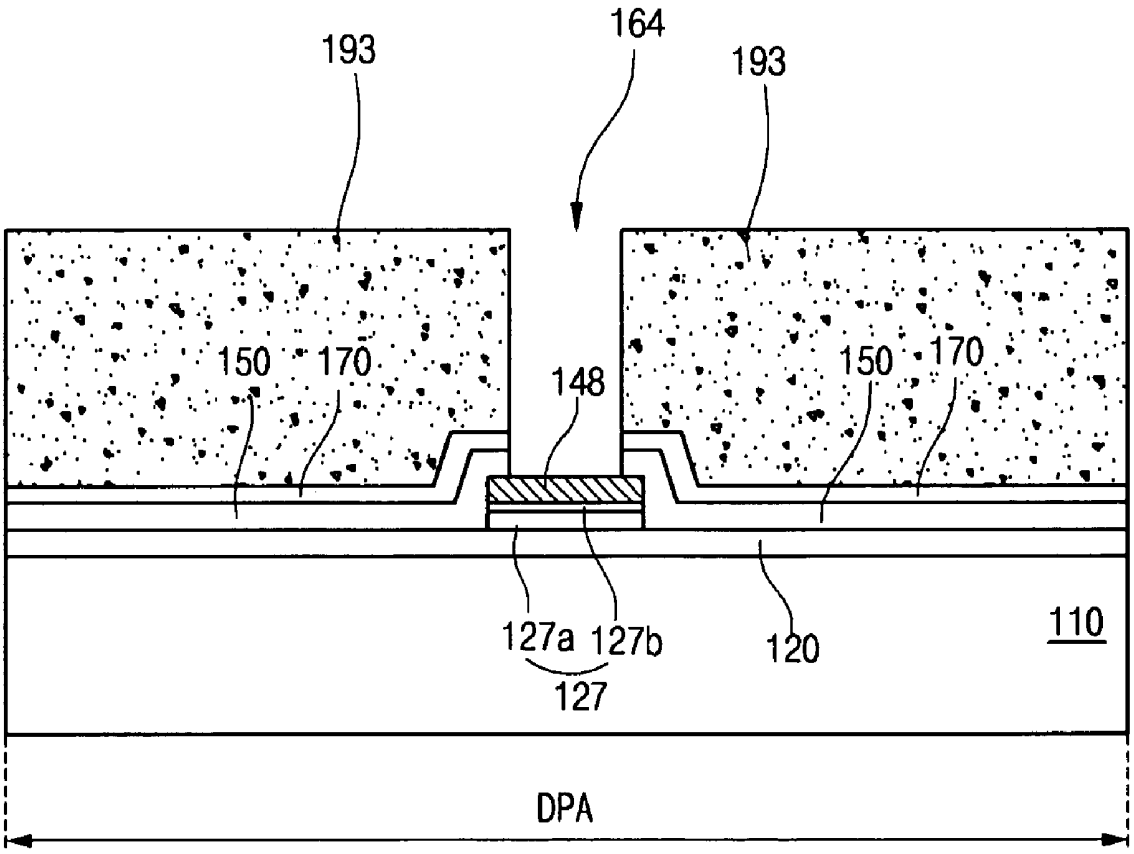
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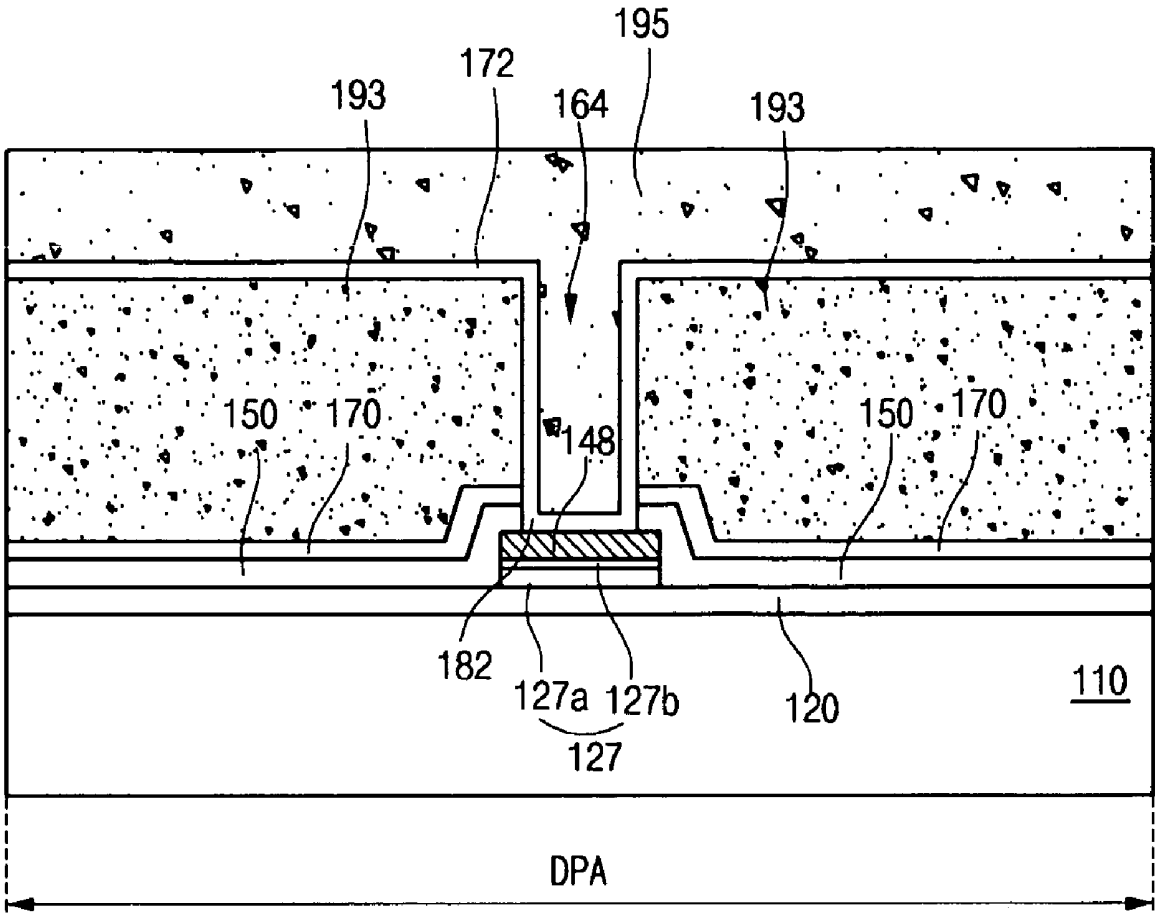
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FIG. 9F

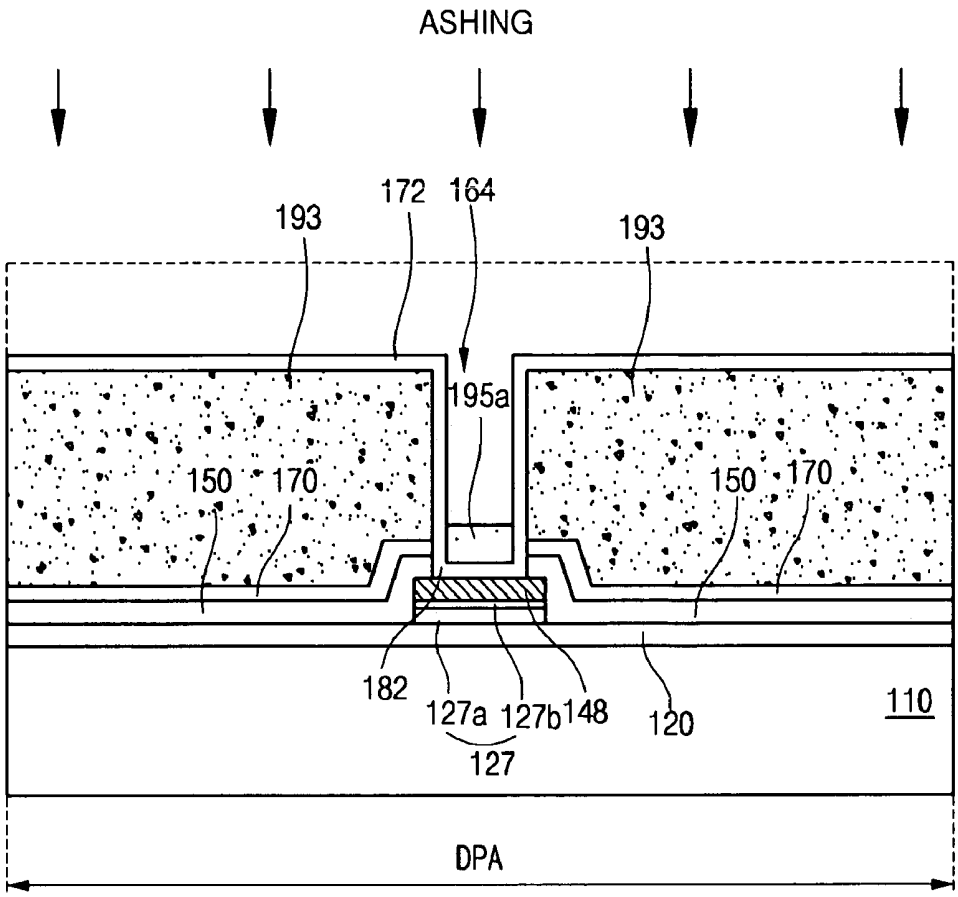
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FIG. 9G

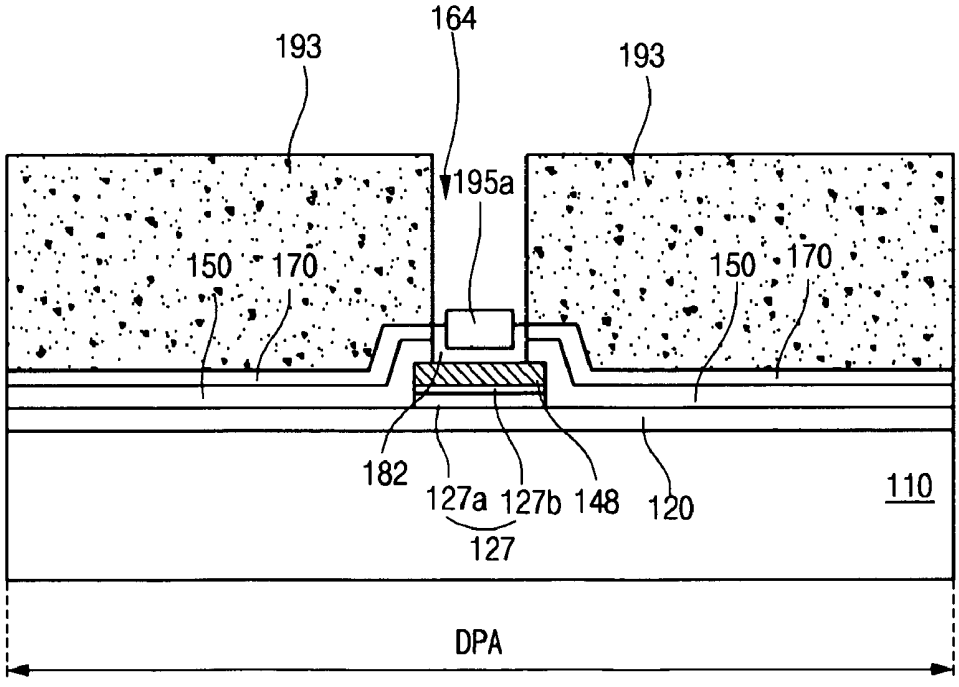
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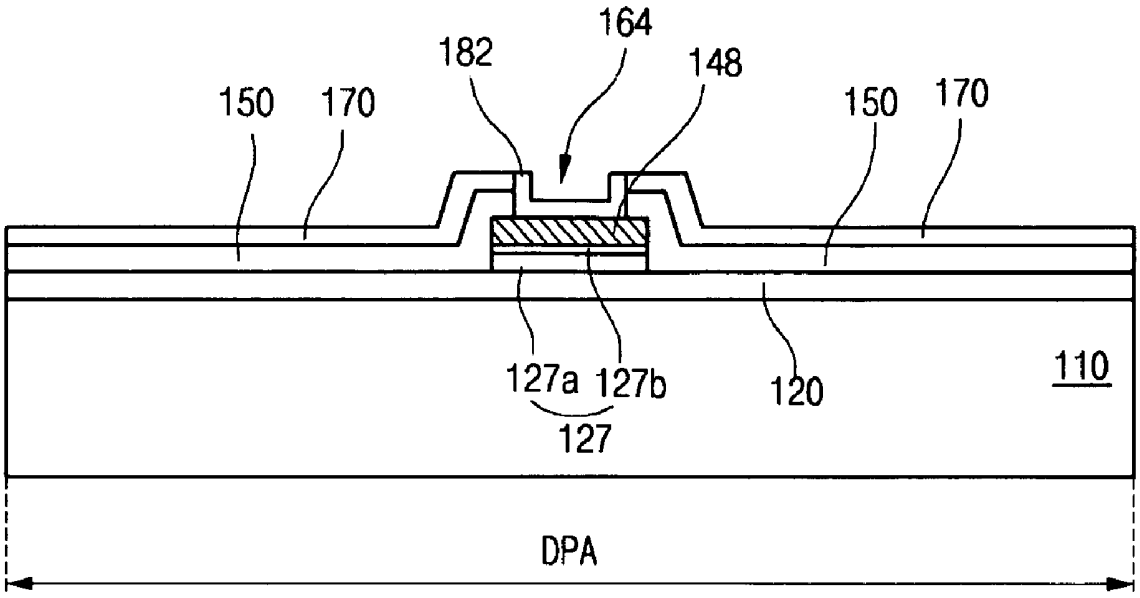
FIG. 9H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DPA

FIG. 9I

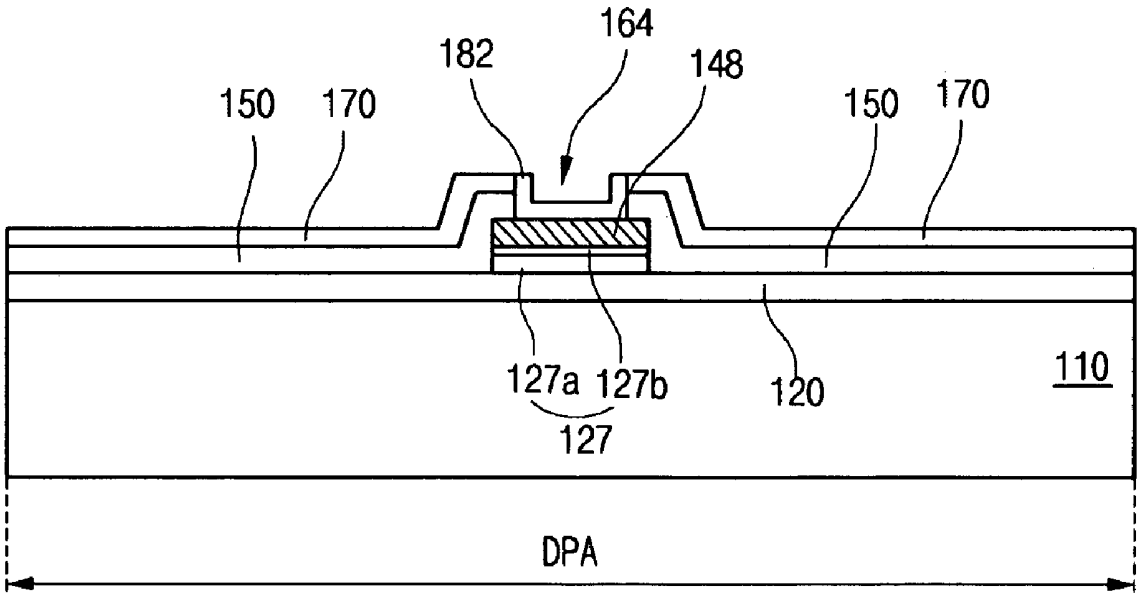
164
182
148
150
170
150
170
127a
127b
127
120
110
DPA

FIG. 9J

TRANSFLECTIVE LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME

This application claims the benefit of Korean Patent Application No. 2005-0084196, filed on Sep. 9, 2005, which is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a liquid crystal display (LCD) device and a method of fabricating a liquid crystal display device, and more particularly, to an array substrate for a transflective liquid crystal display device and a method of fabricating the same.

2. Discussion of the Related Art

As the information age advances, display devices for displaying information are actively being developed. More particularly, flat panel display (FPD) devices having a thin profile, light weight and low power consumption are actively being pursued. FPD devices can be classified as either an emissive type or a non-emissive type depending on their light emission capability. In an emissive type FPD device, an image is displayed using light that emanates from the FPD device. In a non-emissive type FPD device, an image is displayed using light from an external source that reflects and/or transmits through the FPD. For example, a plasma display panel (PDP) device is a field emission display (FED) device. In another example, an electroluminescent display (ELD) device is an emissive type FPD device. Unlike a PDP and an ELD, a liquid crystal display (LCD) device is a non-emissive type FPD device that uses a backlight as a light source.

Among the various types of FPD devices, liquid crystal display (LCD) devices are widely used as monitors for notebook computers and desktop computers because of their high resolution, color rendering capability and superiority in displaying moving images. The LCD device displays images by controlling a transmittance of light through the device. More particularly, liquid crystal molecules of a liquid crystal interposed between two substrates facing each other control light transmission in response to an electric field generated between electrodes on one of the substrates.

Because the LCD device does not emit light, the LCD device needs to be used with a separate light source. Thus, a backlight is disposed on the rear surface on a liquid crystal panel of the LCD device, and images are displayed with the light emitted from the backlight and transmitted through the liquid crystal panel. Accordingly, the above-mentioned LCD device is referred to as a transmission type LCD device. The transmission type LCD device can display bright images in a dark environment due to the use of a separate light source, such as a backlight, but may cause a large power consumption because of the use of the backlight.

To solve the problem of large power consumption, a reflection type LCD device has been developed. The reflection type LCD device controls a transmittance of light by reflecting the outside natural light or artificial light through a liquid crystal layer. In a reflection type LCD device, a pixel electrode on a lower substrate is formed of a conductive material having a relatively high reflectance and a common electrode on an upper substrate is formed of a transparent conductive material. Although the reflection type LCD device may have lower power consumption than the transmission type LCD device, it may have low brightness when the outside light is insufficient or weak.

To solve both the problems of large power consumption and low brightness, a transflective LCD device combining the capabilities of a transmission type LCD device and reflection type LCD device has been suggested. The transflective LCD device can select a transmission mode using a backlight while in an indoor environment or a circumstance having no external light source, and a reflection mode using an external light source in an environment where the external light source exists.

FIG. **1** is a cross-sectional view of an array substrate for a transflective LCD device according to the related art. In FIG. **1**, a substrate **10** includes a pixel region "P" defined by a crossing of a gate line (not shown) and a data line **30**. The pixel region "P" includes a reflective area "RA" and a transmissive area "TA." The reflective area "RA" includes a transistor area "TrA."

A thin film transistor (TFT) "Tr," including a gate electrode **15**, a gate insulating layer **20**, a semiconductor layer **25**, a source electrode **33** and a drain electrode **36**, is formed on the substrate **10** in the transistor area "TrA." The semiconductor layer **25** includes an active layer **25***a* and an ohmic contact layer **25***b*. A first passivation layer **39** of an inorganic insulating material is formed on the TFT "Tr" and a second passivation layer **45** of an organic insulating material is formed on the first passivation layer **39**. Subsequently, a through hole "TH" is formed in the second passivation layer **45** within the transmissive area "TA." Further, the second passivation layer **45** includes a drain contact hole **47** exposing the drain electrode **36** and an uneven top surface. A third passivation layer **49** of an inorganic insulating material is formed on the second passivation layer **45** and has the drain contact hole **47** exposing the drain electrode **36**. A reflective plate **52** of a reflective metallic material layer is formed on the third passivation layer **49**. The reflective plates **52** in the adjacent pixel region "P" are separated from each other. A fourth passivation layer **55** of an inorganic insulating material is formed on the reflective plate **52**, and a pixel electrode **60** is formed on the fourth passivation layer **55**. The pixel electrode **60** is connected to the drain electrode **36** through the drain contact hole **47**. As a result, a gate insulating layer **20** of the thin film transistor (TFT) "Tr," the first passivation layer **39**, the third passivation layer **49**, the fourth passivation layer **55** and the pixel electrode **60** are sequentially formed on the substrate **10** in the transmissive area "TA."

FIGS. **2**A to **2**F are cross-sectional views showing a fabrication process of an array substrate for a transflective LCD device according to the related art. As shown in FIG. **2**A, after a first metal layer (not shown) of a first metallic material is deposited on a substrate **10**, a gate electrode **15** and a gate line (not shown) are formed by patterning the first metal layer through a first mask process including a coating step for a photoresist (PR), an exposure step using a mask, a developing step of the PR and an etching step of the first metal layer. The substrate **10** includes a pixel region "P" divided into a transmissive area "TA" and a reflective area "RA." The reflective area "RA" includes a transistor area "TrA."

As shown in FIG. **2**B, a gate insulating layer **20** is formed on the gate electrode **15** and the gate line. An intrinsic amorphous silicon layer (not shown), a doped amorphous silicon layer (not shown) and a second metal layer (not shown) are sequentially deposited on the gate insulating layer **20**. Then, a data line **30**, a semiconductor layer **25**, including an active layer **25***a* and an ohmic contact layer **25***b*, a source electrode **33** and a drain electrode **36**, are formed by patterning the second metal layer, the doped amorphous silicon layer and the intrinsic amorphous silicon layer through a second mask process.

As shown in FIG. 2C, a first passivation layer **39** is formed on the source electrode **33**, the drain electrode **36** and the data line **30** by depositing an inorganic insulating material. After coating an organic insulating material on the first passivation layer **39**, a second passivation layer **45** is formed by patterning the coated organic insulating material through a third mask process. The second passivation layer **45** has an uneven top surface, and includes a drain contact hole **47** and a through hole "TH." The drain contact hole exposes the first passivation layer **39** on the drain electrode **36** and the through hole "TH" exposes the first passivation layer **39** in the transmissive area "TA." In addition, a third passivation layer **49** is formed on the second passivation layer **39** by depositing an inorganic insulating material.

As shown in FIG. 2D, after a third metal layer (not shown) having a relatively high reflectance is deposited on the third passivation layer **49**, a reflective plate **52** is formed in the reflective area "RA" of the pixel region "P" by patterning the third metal layer through a fourth mask process. Since the third metal layer corresponding to the drain contact hole **47** and the through hole "TH" is removed, the third passivation layer **49** corresponding to the drain contact hole **47** and the through hole "TH" is exposed through the reflective plate **52**.

As shown in FIG. 2E, after an inorganic insulating material is deposited on the reflective plate **52**, a fourth passivation layer **55** is formed by patterning the deposited inorganic insulating material through a fifth mask process. Since the fourth passivation layer **55**, the third passivation layer **49** and the first passivation layer **39** corresponding to the drain contact hole **47** are removed, the drain electrode **36** is exposed through the drain contact hole **47**.

As shown in FIG. 2F, after a transparent conductive material is deposited on the fourth passivation layer **55**. Then, a pixel electrode **60** is formed in the pixel region "P" by patterning the deposited transparent conductive material through a sixth mask process. Thus, the pixel electrode **60** is connected to the drain electrode **36** through the drain contact hole **47**.

As described above, an array substrate for a transflective LCD device according to the related art is fabricated through a six-mask process. Each mask process includes several steps, such as coating PR, exposure of the PR using a mask, a developing the PR, etching using the developed PR and stripping the developed PR. Accordingly, mask processes are expensive in terms of both fabrication time and material cost. In addition, each mask process introduces an additional probability of yield reduction.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a transflective LCD device and a method of fabricating the same that substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide an array substrate for a transflective LCD device that is fabricated through a five-mask process, and a method of fabricating the same.

Another object of the present invention is to provide an array substrate for a transflective LCD device having an improved production efficiency, and a method of fabricating the same.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. These and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for a transflective liquid crystal display device includes: a substrate; a gate line and a data line on the substrate, the gate line and the data line crossing each other to define a pixel region including a transmissive area and a reflective area surrounding the transmissive area; a thin film transistor electrically connected to the gate line and the data line; a first passivation layer on the thin film transistor, the first passivation layer having a drain contact hole exposing a drain electrode of the thin film transistor and a through hole exposing the substrate in the transmissive area; a pixel electrode on the first passivation layer, the pixel electrode contacting the substrate in the transmissive area through the through hole; a reflective plate on the pixel electrode, the reflective plate being electrically connected to the drain electrode through the drain contact hole and contacting the pixel electrode.

In another aspect, a method of fabricating an array substrate for a transflective liquid crystal display device includes: forming a gate line and a data line on a substrate, the gate line and the data line crossing each other to define a pixel region including a transmissive area and a reflective area surrounding the transmissive area; forming a gate insulating layer between the gate line and the data line; forming a thin film transistor connected to the gate line and the data line; forming a first passivation layer on the thin film transistor, the first passivation layer having a drain contact hole exposing a drain electrode of the thin film transistor and a through hole exposing the gate insulating layer on the substrate in the transmissive area; forming a second passivation layer on the first passivation layer; forming a first photoresist pattern on the second passivation layer, the first photoresist pattern exposing the drain contact hole and the through hole; etching the second passivation layer and the gate insulating layer using the first photoresist pattern as an etch mask such that the drain electrode is exposed through the drain contact hole and the substrate is exposed through the through hole; forming a transparent conductive material layer on the first photoresist pattern; forming a first photoresist layer on the transparent conductive material layer; anisotropically removing the first photoresist layer to form a second photoresist pattern on the transparent conductive material layer in the drain contact hole and the through hole; etching the transparent conductive material layer using the second photoresist pattern as an etch mask to form a drain terminal in the drain contact hole and a pixel electrode in the through hole; removing the first and second photoresist patterns; and forming a reflective plate on the drain terminal and the pixel electrode, the reflective plate contacting the drain terminal and the pixel electrode.

In another aspect, an array substrate for a transflective liquid crystal display device includes: a substrate; a gate line and a data line on the substrate, the gate line and the data line crossing each other to define a pixel region including a transmissive area and a reflective area surrounding the transmissive area; a thin film transistor electrically connected to the gate line and the data line; a first passivation layer on the thin film transistor, the first passivation layer having a drain contact hole exposing a drain electrode of the thin film transistor and a through hole exposing the substrate in the transmissive area; a pixel electrode contacting the substrate in the transmissive area and a first sidewall of the through hole; a drain terminal contacting the drain electrode and a second sidewall of the drain contact hole; and a reflective plate on the first

passivation layer, the reflective plate contacting the pixel electrode on the first sidewall of the through hole and covering the drain terminal.

In another aspect, a method of fabricating an array substrate for a transflective liquid crystal display device includes: forming a gate line and a data line on a substrate, the gate line and the data line crossing each other to define a pixel region including a transmissive area and a reflective area surrounding the transmissive area; forming a gate insulating layer between the gate line and the data line; forming a thin film transistor connected to the gate line and the data line; forming a first passivation layer on the thin film transistor, the first passivation layer having a drain contact hole exposing a drain electrode of the thin film transistor and a through hole exposing the gate insulating layer on the substrate in the transmissive area; forming a second passivation layer on the first passivation layer; forming a first photoresist pattern on the second passivation layer, the first photoresist pattern exposing the drain contact hole and the through hole; etching the second passivation layer and the gate insulating layer using the first photoresist pattern as an etch mask such that the drain electrode is exposed through the drain contact hole and the substrate is exposed through the through hole; forming a transparent conductive material layer on the first photoresist pattern and on the second passivation layer; changing the crystalline state of the transparent conductive material layer such that the crystalline state of first portions of the transparent conductive material layer on the first passivation layer are different than second portions of the transparent conductive material layer over the first passivation layer; forming a first photoresist layer on the transparent conductive material layer; anisotropically removing the first photoresist layer to form a second photoresist pattern on the transparent conductive material layer in the drain contact hole and the through hole; selectively etching the second portions of the transparent conductive material layer to form a drain terminal in the drain contact hole and a pixel electrode in the through hole; removing the first and second photoresist patterns; and forming a reflective plate on the drain terminal and the pixel electrode, the reflective plate contacting the drain terminal and the pixel electrode.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

FIG. **1** is a cross-sectional view of an array substrate for a transflective LCD device according to the related art.

FIGS. **2**A to **2**F are cross-sectional views showing a fabrication process of an array substrate for a transflective LCD device according to the related art.

FIG. **3** is a plane view of an array substrate for a transflective LCD device according to an embodiment of the present invention.

FIG. **4** is a cross-sectional view along line "IV-IV" of FIG. **3**.

FIG. **5** is a cross-sectional view along line "V-V" of FIG. **3**.

FIG. **6** is a cross-sectional view along line "VI-VI" of FIG. **3**.

FIGS. **7**A to **7**J are cross-sectional views, which along line "IV-IV" of FIG. **3**, showing a fabricating process of an array substrate for a transflective LCD device according to an embodiment of the present invention.

FIGS. **8**A to **8**J are cross-sectional views, which are along line "V-V" of FIG. **3**, showing a fabricating process of an array substrate for a transflective LCD device according to an embodiment of the present invention.

FIGS. **9**A to **9**J are cross-sectional views, which are along line "VI-VI" of FIG. **3**, showing a fabricating process of an array substrate for a transflective LCD device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, similar reference numbers will be used to refer to the same or similar parts.

FIG. **3** is a plan view of an array substrate for a transflective LCD device according to an embodiment of the present invention. As shown in FIG. **3**, a gate line **113** and a data line **135** are formed on a substrate **110**. The gate line **113** and the data line **135** cross each other, to thereby define a pixel region "P." A thin film transistor (TFT) "Tr," as a switching element, is electrically connected to the gate line **113** and the data line **135**. The TFT "Tr" includes a gate electrode **115**, a gate insulating layer (not shown), a semiconductor layer **125**, a source electrode **140** and a drain electrode **143**. The semiconductor layer **125** has an active layer and an ohmic contact layer. A gate pad **117** is formed at one end of the gate line **113**, and a data pad **148** is formed at one end of the data line **135**. Although not shown in FIG. **3**, an external driving circuit contacts the gate pad **117** and the data pad **148**, and supplies a gate signal and a data signal through the gate pad **117** and the data pad **148**, respectively.

The pixel region "P" includes a transmissive area "TA" at a central portion thereof and a reflective area "RA" surrounding the transmissive area "TA." A second passivation layer (not shown) of an organic insulating material has a through hole (TH) corresponding to the transmissive area "TA," and a reflective plate **186** is formed to correspond to the reflective area "RA." The second passivation layer has an uneven top surface to prevent a mirror reflection at the reflective plate **186**. The reflective plate **186** is electrically connected to the drain electrode **143** of the TFT "Tr" through a drain contact hole **158**. A pixel electrode **173** of a transparent conductive material is formed in the transmissive area "TA." Thus, the pixel electrode is formed at a bottom and a sidewall of the through hole "TH," and contacts the reflective plate **186** at edge portions.

A storage capacitor "StgC" is formed in a boundary of the pixel region "P." The storage capacitor "StgC" includes a first storage electrode **114** of a portion of the gate line **113**, a dielectric layer (not shown) of the gate insulating layer on the first storage electrode **114** and a second storage electrode **146** on the dielectric layer over the first storage electrode **114**. The second storage electrode **146** is electrically connected to the reflective plate **186** through a storage contact hole **160**.

In this embodiment, the storage capacitor "StgC" has a storage-on-gate structure where the gate line **113** is used as the first storage electrode **114**, more particularly, a storage-on-previous gate structure where an n^{th} pixel region uses a $(n-1)^{th}$ gate line as a first storage capacitor. In another embodiment, however, a storage capacitor can have a storage-on-common structure, where a common line parallel to the

gate line is used as a first storage electrode, and a metal pattern overlapping the common line and connected to a pixel electrode through a contact hole is used as a second storage electrode.

FIG. **4** is a cross-sectional view along line "IV-IV" of FIG. **3**, and FIG. **5** is a cross-sectional view along line "V-V" of FIG. **3**. In addition, FIG. **6** is a cross-sectional view along line "VI-VI" of FIG. **3**. As shown in FIGS. **4** to **6**, a substrate **110** has a pixel region "P" defined by a crossing of a gate line **113** and a data line **135**. A gate pad area "GPA" is at one end of the gate line **113** and a data pad area "DPA" is at one end of the data line **135**. A gate pad **117** is formed in the gate pad area "GPA" and a data pad **148** is formed in the data pad area "DPA." The pixel region "P" includes a transmissive area "TA" corresponding to a through hole "TH" and a reflective area "RA" corresponding to a reflective plate **186**. A transistor area "TrA" where a thin film transistor (TFT) "Tr" is formed and a storage capacitor area "StgA" where a storage capacitor "StgC" is formed can be defined in the reflective area "RA."

The gate line **113** is formed on the substrate **110** and a gate electrode **115** extending from the gate line **113** is formed in the transistor area "TrA" of the reflective area "RA." A gate insulating layer **120** is formed on the gate electrode **115**, and a semiconductor layer **125** is formed on the gate insulating layer **120**. The semiconductor layer **125** can include an active layer **125***a*, such as intrinsic amorphous silicon, and an ohmic contact layer **125***b*, such as, impurity-doped amorphous silicon. The ohmic contact layer **125***b* is separated into two portions so as to expose the active layer **125***a* between the two portions. Source and drain electrodes **140** and **143** are formed on the ohmic contact layer **125***b*. The gate electrode **115**, the semiconductor layer **125**, the source electrode **140** and the drain electrode **143** constitute the thin film transistor (TFT) "Tr" as a switching element. The data line **135** crossing the gate line **113** to define the pixel region "P" is formed on the gate insulating layer **120**. The data line **135** is connected to the source electrode **140** of the TFT "Tr."

The gate pad **117** is formed in the gate pad area "GPA" for connection to one end of the gate line **113** and the data pad **148** is formed in the data pad area "DPA" for connection to one end of the data line **135**. In the storage area "StgA," a second storage electrode **146** having an island shape is formed over the gate insulating layer **120** on the gate line **113**. The second storage electrode **146** can be formed of the same material as the source and drain electrodes **140** and **143**.

A first passivation layer **150** of an inorganic insulating material is formed on the TFT "Tr," and a second passivation layer **155** of an organic insulating material is formed on the first passivation layer **150** corresponding to the reflective area "RA." The second passivation layer **155** has an uneven top surface contour that is like the top surface of the reflective plate **186**, which is subsequently formed over the second passivation layer **155**. A portion of the second passivation layer **155** corresponding to the transmissive area "TA" is removed to form the through hole "TH" exposing the substrate **110**. In addition, portions of the second passivation layer **155** corresponding to the gate pad area "GPA" and the data pad area "DPA" are removed to expose the gate pad **117** and the data pad **148**. The second passivation layer **155** has a drain contact hole **158** exposing the drain electrode **143** and a storage contact hole **160** exposing the second storage electrode **146** formed by removing portions of the second passivation layer **155**.

A third passivation layer **170** of an inorganic insulating material is formed on the second passivation layer **155**. Portions of the third passivation layer **170** corresponding to the through hole "TH," the drain contact hole **158** and the storage contact hole **160** are removed. In addition, portions of the third passivation layer **170** corresponding to the gate pad **117** and the data pad **148** are removed to form a gate pad contact hole **162** and a data pad contact hole **164**, respectively. As a result, the through hole "TH" is formed through the third passivation layer **170**, the second passivation layer **155**, the first passivation layer **150** and the gate insulating layer **120** in the transmissive area "TA" to expose the substrate **110**. The drain contact hole **158** is formed through the third passivation layer **170**, the second passivation layer **155** and the first passivation layer **150** in the transistor area "TrA" to expose the drain electrode **143**. The storage contact hole **160** is formed through the third passivation layer **170**, the second passivation layer **155** and the first passivation layer **150** in the storage area "StgA" to expose the second storage electrode **146**. In addition, the gate pad contact hole is formed through the third passivation layer **170**, the first passivation layer **150** and the gate insulating layer **120** in the gate pad area "GPA" to expose the gate pad **117**, and the data pad contact hole **164** is formed through the third passivation layer **170** and the first passivation layer **150** in the data pad area "DPA" to expose the data pad **148**.

A pixel electrode **173** of a transparent conductive material is formed on the bottom and sidewall of the through hole "TH." Accordingly, the pixel electrode **173** contacts the substrate **110** in the transmissive area "TA." Similarly, a drain terminal **175** of a transparent conductive material is formed in the bottom and sidewall of the drain contact hole **158** to contact the drain electrode **143**, and the storage terminal **177** of a transparent conductive material is formed on bottom and sidewall of the storage contact hole **160** to contact the second storage electrode **146**. In addition, a gate pad terminal **180** is formed on the bottom and sidewall of the gate pad contact hole **162** to contact the gate pad **117**, and a data pad terminal **182** of a transparent conductive material is formed on the bottom and sidewall of the data pad contact hole **164** to contact the data pad **148**.

A reflective plate **186** of a metallic material having a relatively high reflectance is formed on the third passivation layer **170** in the reflective area "RA." The reflective plate **186** is connected to the pixel electrode **173**, the drain terminal **175** and the storage terminal **177**. The reflective plate **186** contacts the pixel electrode on the sidewall of the through hole "TH." In addition, the reflective plate **186** contacts the drain terminal **175** on the bottom and the sidewall of the drain contact hole **158**, and contacts the storage terminal **177** on the bottom and the sidewall of the storage contact hole **160**. The reflective plate **186** is independently formed in each pixel region "P" and functions as a reflective electrode because the reflective plate **186** is electrically connected to the drain electrode **143**.

FIGS. **7**A to **7**J, **8**A to **8**J, and **9**A to **9**J are cross-sectional views showing a fabricating process of an array substrate for a transflective LCD device according to an embodiment of the present invention. FIGS. **7**A to **7**J are along line "IV-IV" of FIG. **3**. In addition, FIGS. **8**A to **8**J are along line "V-V" of FIG. **3**, and FIGS. **9**A to **9**J are along a line "VI-VI" of FIG. **3**.

In FIGS. **7**A, **8**A and **9**A, after a first metal layer (not shown) is formed on a substrate **110**, the first metal layer is patterned through a first mask process to form a gate line **113**, a gate electrode **115** extending from the gate line **113** in a transistor area "TrA" of a pixel region "P" and a gate pad **117** at one end of the gate line **113**. In the first mask process, a first photoresist (PR) layer (not shown) can be formed on the first metal layer and can be exposed through a first mask (not shown) having a transmissive region and a blocking region. The exposed first PR layer is developed to form a first PR

pattern, and the first metal layer is etched using the first PR pattern as an etch mask to form the gate line **113**, the gate electrode **115** and the gate pad **117**.

In FIGS. **7**B, **8**B and **9**B, a gate insulating layer **120** is formed on the gate line **113**, the gate electrode **115** and the gate pad **117** by depositing an inorganic insulating material, such as silicon oxide (SiO_2) and silicon nitride (SiN_x). An intrinsic amorphous silicon layer (not shown), an impurity-doped amorphous silicon layer (not shown) and a second metal layer are sequentially formed on the gate insulating layer **120**. Through a second mask process, the second metal layer is patterned to form a source electrode **140**, a drain electrode **143**, a data line **135** and a data pad **148**, and the impurity-doped amorphous silicon layer and the intrinsic amorphous silicon layer are patterned to form a semiconductor layer **125** including an active layer **125***a* and an ohmic contact layer **125***b*. In the second mask process, a second PR layer (not shown) can be formed on the second metal layer, and can be exposed through a second mask (not shown) having a transmissive region, a blocking region and a half-transmissive region such that a transmittance of the half-transmissive region is greater than a transmittance of the blocking region and smaller than a transmittance of the transmissive region. Since the half-transmissive region of the second mask can be obtained from a slit pattern or a half-tone pattern, an exposure step using the second mask is referred to as a diffraction exposure or a half-tone exposure. The exposed second PR layer is developed to form a second PR pattern **191** corresponding to the transistor area "TrA," the storage area "StgA" and the data pad area "DPA."

The second PR pattern **191** includes a first portion **191***a* having a first thickness and a second portion **191***b* having a second thickness smaller than the first thickness. The first portion **191***a* of the second PR pattern **191** corresponds to a portion where the second metal layer, the impurity-doped amorphous silicon layer and the intrinsic amorphous silicon layer remain in a subsequent process, and the second portion **191***b* of the second PR layer **191** corresponds to another portion where the second metal layer is removed and the impurity-doped amorphous silicon layer and the intrinsic amorphous silicon layer remain in a subsequent process. In the transistor area "TrA," for example, the first portion **191***a* of the second PR layer **191** corresponds to a portion for source and drain electrodes and the second portion **191***b* of the second PR layer corresponds to another portion for a channel region. Accordingly, the first portion **191***a* of the second PR layer **191** corresponds to a data line, a source electrode, a drain electrode, a second storage electrode and a data pad of a subsequent process, while the second portion **191***b* of the second PR layer **191** corresponds to the channel region between the source and drain electrodes.

The second metal layer, the impurity-doped amorphous silicon layer and the intrinsic amorphous silicon layer are etched using the second PR pattern **191** having the first and second portions **191***a* and **191***b* as an etch mask to form a source-drain pattern **138**, an impurity-doped amorphous silicon pattern **123** under the source-drain pattern **138** and an active layer **125***a* under the impurity-doped amorphous silicon pattern **123** in the transistor area "TrA." At the same time, a data line **135** crossing the gate line **113**, a data pad **148** at one end of the data line **135** and a second storage electrode **146** overlapping the gate line **113** are formed by etching the second metal layer, the impurity-doped amorphous silicon layer and the intrinsic amorphous silicon layer. A portion of the gate line **113** overlapping the second storage electrode **146** in the storage area "StgA" functions as a first storage electrode **114**. Here, a storage impurity-doped amorphous silicon pattern **127***a* and a storage intrinsic amorphous silicon pattern **127***b* having the same shape as the second storage electrode **146** are formed under the second storage electrode **146**. Similarly, a data impurity-doped amorphous silicon pattern and a data intrinsic amorphous silicon pattern having the same shape as the data line **135** are formed under the data line **135**.

In FIGS. **7**C, **8**C and **9**C, the second portion **191***b* (of FIG. **7**B) of the second PR pattern **191** are removed by an ashing step to expose a portion of the source-drain pattern **138** (of FIG. **7**B). Since the first portion **191***a* (of FIGS. **7**B and **9**B) of the second PR pattern **191** has the first thickness greater than the second thickness, the first portion **191***a* of the second PR pattern **191** remains even after the second portion **191***b* of the second PR pattern **191** is removed. The remaining first portion (not shown) of the second PR pattern can have a thickness corresponding to a difference between the first and second thicknesses.

The portion of the source-drain pattern **138** (of FIG. **7**B) exposed through the remaining first portion of the second PR pattern **191** and the impurity-doped amorphous silicon pattern **123** (of FIG. **7**B) under the exposed portion of the source-drain electrode **138** are etched using the remaining first portion of the second PR pattern **191** as an etch mask to form a source electrode **140**, a drain electrode **143** and an ohmic contact layer **125***b* under the source and drain electrodes **140** and **143**. The source and drain electrodes **140** and **143** are spaced apart from each other and on opposite sides of the gate electrode **115** in the transistor area "TrA," and the ohmic contact layer **125***b* has the same shape as the source and drain electrodes **140** and **143**. After the source electrode **140**, the drain electrode **143** and the ohmic contact layer **125***b* are formed, the remaining first portion of the second PR pattern **191** is removed by a stripping step.

As shown in FIGS. **7**D, **8**D and **9**D, a first passivation layer **150** of an inorganic insulating material, such as silicon oxide (SiO_2) or silicon nitride (SiN_x), is formed on the data line **135**, the source electrode **140**, the drain electrode **143** and the second storage electrode **146**. When the active layer **125***a* contacts a second passivation layer **155** of an organic material in a subsequent process, the active layer **125***a* can be degraded by contamination that causes deterioration of the TFT "Tr." To prevent such contamination, the first passivation layer **150** prevents a contact between the active layer **125***a* and the second passivation layer **155**. In an alternative embodiment, the first passivation layer **150** can be omitted when possible degradation of the active layer **125***a* is negligible.

The second passivation layer **155** is formed on the first passivation layer **150** through a third mask process. An organic insulating material layer having a photosensitivity is formed on the first passivation layer **150**, and is exposed through a third mask (not shown) having a transmissive region, a blocking region and a half-transmissive region such that a transmittance of the half-transmissive region is greater than a transmittance of the blocking region and smaller than a transmittance of the transmissive region. For example, when the organic insulating material layer has a positive type photosensitivity, the third mask can be aligned such that transmissive regions correspond to the transmissive area "TA," the gate pad area "GPA," the data pad area "DPA," the drain contact hole **158** and the storage contact hole **160**, and alternating blocking and half-transmissive regions correspond to the reflective area "RA." In the alternative, when the organic insulating material layer has a negative type photosensitivity, the third mask can be aligned such that blocking regions correspond to the transmissive area "TA," the gate pad area "GPA," the data pad area "DPA," the drain contact hole **158**

and the storage contact hole **160**, and alternating transmissive region and the half-transmissive region correspond to the reflective area "RA."

The organic insulating material layer is exposed through the third mask and the exposed organic insulating material layer is developed to form the through hole "TH" exposing the first passivation layer **150** in the transmissive area "TA," the drain contact hole **158** exposing the first passivation layer **150** on the drain electrode **143**, and the storage contact hole **160** exposing the first passivation layer **150** on the second storage electrode **146**. The second passivation layer can nave an uneven top surface due to the half-transmissive region of the third mask. The round shape of the uneven top surface of the second passivation layer **155** can be obtained by an additional heat treatment step.

As shown in FIGS. **7**E, **8**E and **9**E, a third passivation layer **170** of an inorganic insulating material, such as silicon oxide (SiO_2) or silicon nitride (SiN_x), is formed on the second passivation layer **155** through a fourth mask process. A third PR layer (not shown) is formed on the third passivation layer **170** and is exposed through a fourth mask (not shown) having a transmissive region and a blocking region. The exposed third PR layer is developed to form a third PR pattern **193** exposing portions corresponding to the drain contact hole **158**, the storage contact hole **160**, the through hole "TH," the gate pad area "GPA" and the data pad area "DPA." In the alternative, the third passivation layer **170** can be omitted.

The third passivation layer **170**, the first passivation layer **150** and the gate insulating layer **120** are sequentially etched using the third PR pattern **193** as an etch mask to complete the drain contact hole **158** exposing the drain electrode **143**, the storage contact hole **160** exposing the second storage electrode **146**, the through hole "TH" exposing the substrate **110**, the gate pad contact hole **162** exposing the gate pad **117** and the data pad contact hole exposing the data pad **148**. As a result, the through hole "TH" is formed through the gate insulating layer **120**, the first passivation layer **150**, the second passivation layer **155** and the third passivation layer **170**, and the gate pad contact hole **162** is formed through the gate insulating layer **120**, the first passivation layer **150** and the third passivation layer **170**. In addition, the drain contact hole **158** and the storage contact hole **160** are formed through the first, second and third passivation layers **150**, **155** and **170**. The data pad contact hole **164** is formed through the first passivation layer **150** and third passivation layer **170**.

As shown in FIGS. **7**F, **8**F and **9**F, a transparent conductive material layer **172** is formed on the third PR pattern **193**. Accordingly, the transparent conductive material layer **172** is formed on bottoms and sidewalls of the drain contact hole **158**, the storage contact hole **160**, the through hole "TH," the gate pad contact hole **162** and the data pad contact hole **164**. A fourth PR layer **195** is formed on the transparent conductive material layer **172**. Since the fourth PR layer **195** is formed by coating method having an excellent step coverage property, the drain contact hole **158**, the storage contact hole **160**, the through hole "TH," the gate pad contact hole **162** and the data pad contact hole **164** are filled up with the fourth PR layer **195** having a flat top surface.

As shown in FIGS. **7**G, **8**G and **9**G, the fourth PR layer **195** is removed by an ashing method having an anisotropic property. Accordingly, the fourth PR layer **195** is equally removed along a downward direction to expose the transparent conductive material layer **172** except on the bottoms and the sidewalls of the drain contact hole **158**, the storage contact hole **160**, the through hole "TH," the gate pad contact hole **162** and the data pad contact hole **164**. Since the transparent conductive material layer **172** is not removed by the ashing method, the ashing method for the fourth PR layer **195** can be continuously performed even after the fourth PR layer **195** in the reflective area "RA" is removed. As a result, a fourth PR pattern **195***a* remains on the bottoms and the sidewalls of the drain contact hole **158**, the storage contact hole **160**, the through hole "TH," the gate pad contact hole **162** and the data pad contact hole **164**. The fourth PR pattern **195***a* can have a top surface height smaller than a top surface height of the second passivation layer **155** by controlling time period, or type and amount of gas for the ashing method. Since a thickness of the fourth PR layer **195** in the reflective area "RA" is much smaller than a thickness of the fourth PR layer **195** in each holes **158**, **160**, "TH," **162** and **164** due to the third PR pattern **193** and the second passivation layer **155**, the fourth PR pattern **195***a* remains more stably.

As shown in FIGS. **7**H, **8**H and **9**H, the transparent conductive material layer **172** (of FIGS. **7**G, **8**G and **9**G) is etched using the fourth PR pattern **195***a* as an etch mask to form a pixel electrode **173**, a drain terminal **175**, a storage terminal **177**, a gate pad terminal **180** and a data pad terminal **182**. More particularly, the transparent conductive material layer **172** can be selectively etched leaving the pixel electrode **173** based upon the transparent conductive layer **172** on the third PR pattern **193** having a different crystalline state than the pixel electrode **173**. The difference in crystalline states can be done by a laser process or ultraviolet treatment after forming the transparent conductive layer **172** or, in the alternative, by a laser or thermal process after forming the fourth PR pattern **195***a*.

The pixel electrode **173** contacts the substrate in the through hole "TH." In addition, the drain terminal **175** and the storage terminal contact the drain electrode **143** in the drain contact hole **158** and the second storage electrode **146** in the storage contact hole **160**, respectively. Further, the gate pad terminal **180** and the data pad terminal **182** contact the gate pad **117** in the gate pad contact hole **162** and the data pad **148** in the data pad contact hole **164**, respectively.

As shown in FIGS. **71**, **81** and **91**, the third and fourth PR patterns **193** and **195***a* (of FIGS. **7**H, **8**H and **9**H) are removed by a stripping method to expose the third passivation layer **170**, the pixel electrode **173**, the drain terminal **175**, the storage terminal **177**, the gate pad terminal **180** and the data pad terminal **182**.

As shown in FIGS. **7**J, **8**J and **9**J, a reflective plate **186** is formed on the third passivation layer **170** through a fifth mask process. In the fifth mask process, a third metal layer (not shown) is formed on the third passivation layer **170**, the pixel electrode **173**, the drain terminal **175**, the storage terminal **177**, the gate pad terminal **180** and the data pad terminal **182**, and a fifth PR layer (not shown) is formed on the third metal layer. A metallic material, such as aluminum (Al) or aluminum (Al) alloy, having a high reflectance can be used for the third metal layer. The fifth PR layer is exposed through a fifth mask (not shown) having a transmissive region and a blocking region to form a fifth PR pattern (not shown). The third metal layer is etched using the fifth PR pattern as an etch mask to form the reflective plate **186**. The reflective plate **186** contacts the pixel electrode **173** on the sidewall of the through hole "TH," and contacts the drain terminal **175** on the bottoms and the sidewalls of the drain contact hole **158** and the storage terminal **177** on the bottoms and the sidewalls of the storage contact hole **160**. As a result, the reflective plate **186** is electrically connected to the drain electrode **143**, the second storage electrode **146** and the pixel electrode **173**. Thus, the reflective plate **186** functions as an electrode for driving a liquid crystal layer of a transflective LCD device in a subsequent process. Since the reflective plate **186** and the pixel

electrode **173** contact each other on the sidewall of the through hole "TH," it is preferable that the through hole "TH" has a slanted sidewall for more reliable contact.

In embodiments of the present invention, since an array substrate for a transflective LCD device is fabricated through a five-mask process, production yield is improved and fabrication cost is reduced. In addition, since a reflective plate having an uneven top surface is formed at a top of the array substrate, a mirror reflection is prevented and a reflection efficiency is maximized.

It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An array substrate for a transflective liquid crystal display

device, comprising: a substrate; a gate line and a data line on the substrate, the gate line and the data line crossing each other to define a pixel region including a transmissive area and a reflective area surrounding the transmissive area;

a thin film transistor having a gate insulating layer, the thin film transistor electrically connected to the gate line and the data line

a first passivation layer on the thin film transistor, the first passivation layer having a drain contact hole exposing a drain electrode of the thin film transistor and a through hole exposing the substrate in the transmissive area;

a second passivation layer of an inorganic insulating material between the thin film transistor and the first passivation layer, wherein the second passivation layer has the drain contact hole exposing the drain electrode;

a third passivation layer of an inorganic insulating material between the first passivation layer and the reflective plate, wherein the third passivation layer has the drain contact hole exposing the drain electrode;

a pixel electrode on the first passivation layer, the pixel electrode contacting the substrate in the transmissive area through the through hole;

a reflective plate on the pixel electrode, the reflective plate being electrically connected to the drain electrode through the drain contact hole and to the pixel electrode; and

a drain terminal of a transparent conductive material positioned between the reflective plate and the drain electrode,

wherein the drain terminal is formed of the same layer as the pixel electrode and patterned apart from the pixel electrode, and

wherein the reflective plate is electrically connected to the drain electrode through the drain terminal.

2. The array substrate according to claim **1**, further comprising a storage capacitor electrically connected to the reflective plate, wherein the storage capacitor includes a first storage electrode that is a portion of the gate line, a portion of the gate insulating layer on the first storage electrode and a second storage electrode on the gate insulating layer.

3. The array substrate according to claim **2**, wherein the first passivation layer has a storage contact hole exposing the second storage electrode, and the reflective plate is electrically connected to the second storage electrode through the storage contact hole.

4. The array substrate according to claim **3**, further comprising a storage terminal of a transparent conductive material between the reflective plate and the second storage electrode.

5. The array substrate according to claim **4**, wherein the storage terminal is formed of the same layer as the pixel electrode.

6. The array substrate according to claim **1**, wherein the pixel electrode is formed on a bottom and a sidewall of the through hole, and wherein the reflective plate electrically contacts the pixel electrode on the sidewall of the through hole and exposes the pixel electrode on the bottom of the through hole.

7. The array substrate according to claim **1**, further comprising a gate pad at one end of the gate line and a data pad at one end of the data line.

8. The array substrate according to claim **7**, further comprising a gate pad terminal on the gate pad and a data pad terminal on the data pad, wherein the gate pad terminal and the data pad terminal are formed of a transparent conductive material.

9. The array substrate according to claim **8**, wherein gate pad terminal and the data pad terminal is formed of the same layer as the pixel electrode.

10. The array substrate according to claim **1**, wherein the first passivation layer is formed of an organic insulating material and has an uneven top surface.

11. The array substrate according to claim **10**, wherein the reflective plate has an embossed shape corresponding to the uneven top surface of the first passivation layer.

12. The array substrate according to claim **1**, wherein the thin film transistor includes a gate electrode, a gate insulating layer on the gate electrode, an active layer on the gate insulating layer over the gate electrode, an ohmic contact layer on the active layer, a source electrode on the ohmic contact layer, the drain electrode spaced apart from the source electrode.

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摘要(译)

一种半透半反液晶显示装置用阵列基板，包括：基板;栅极线和数据线在基板上，栅极线和数据线彼此交叉以限定像素区域，该像素区域包括透射区域和围绕透射区域的反射区域;薄膜晶体管，具有栅极绝缘层，薄膜晶体管电连接到栅极线和数据线;第一钝化层，具有暴露薄膜晶体管的漏极的漏极接触孔和在透射区域中暴露衬底的通孔;第一钝化层上的像素电极，像素电极通过通孔与透射区域中的基板接触;在像素电极上的反射板上，反射板通过漏极接触孔与像素电极电连接到漏极。