



US 20110037688A1

(19) **United States**

(12) **Patent Application Publication**  
**Chiang et al.**

(10) **Pub. No.: US 2011/0037688 A1**

(43) **Pub. Date: Feb. 17, 2011**

(54) **LIQUID CRYSTAL DISPLAY AND OPERATION METHOD THEREOF**

(30) **Foreign Application Priority Data**

Aug. 25, 2006 (TW) ..... 95131463

(75) Inventors: **Min-Feng Chiang**, Hsin-Chu (TW); **Hsueh-Ying Huang**, Hsin-Chu (TW); **Ming-Sheng Lai**, Hsin-Chu (TW)

**Publication Classification**

(51) **Int. Cl.**  
**G09G 3/36** (2006.01)

Correspondence Address:  
**THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP**  
**600 GALLERIA PARKWAY, S.E., STE 1500**  
**ATLANTA, GA 30339-5994 (US)**

(52) **U.S. Cl.** ..... **345/98**

(73) Assignee: **AU Optronics Corporation**, Hsin-Chu (TW)

(57) **ABSTRACT**

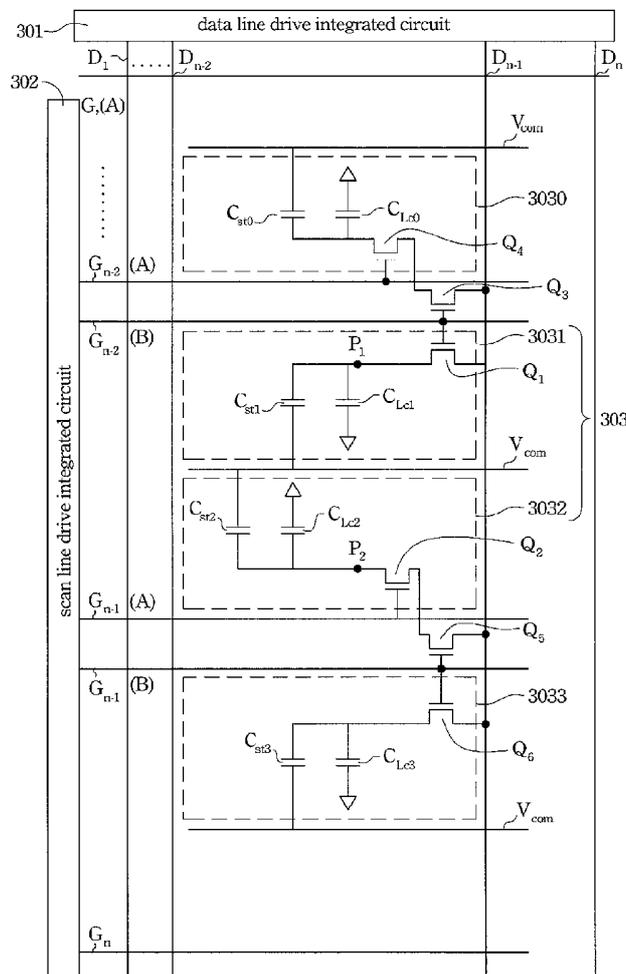
(21) Appl. No.: **12/912,230**

A pixel unit in the present invention is divided into two sub-pixels. Each sub-pixel includes a thin film transistor, a liquid crystal capacitor and a storage capacitor. The two transistors respectively located in different sub-pixels are connected to different scan lines. One of the two transistors is connected to the data line through another transistor. Therefore, two different pixel voltages are formed in a pixel.

(22) Filed: **Oct. 26, 2010**

**Related U.S. Application Data**

(63) Continuation of application No. 11/745,663, filed on May 8, 2007, now Pat. No. 7,852,302.



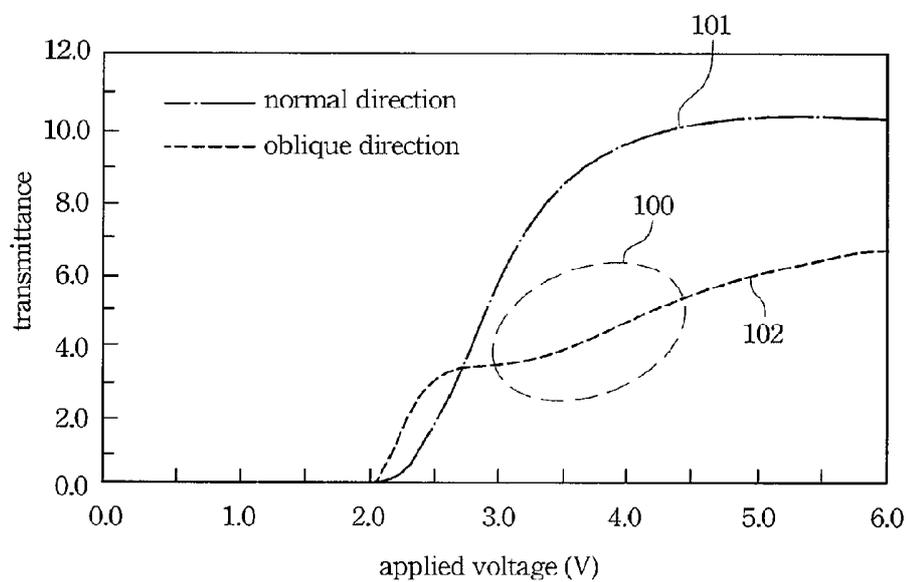


Fig. 1  
(PRIOR ART)

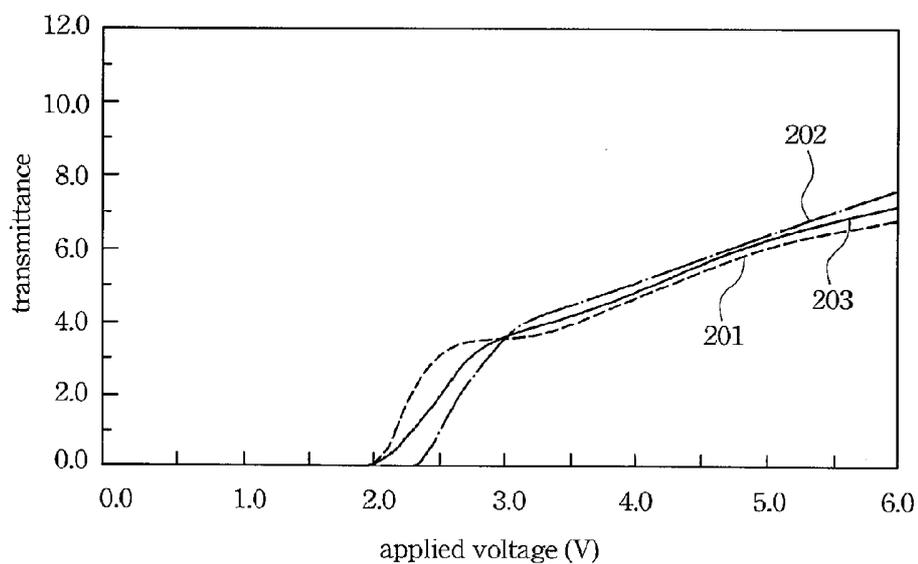


Fig. 2  
(PRIOR ART)

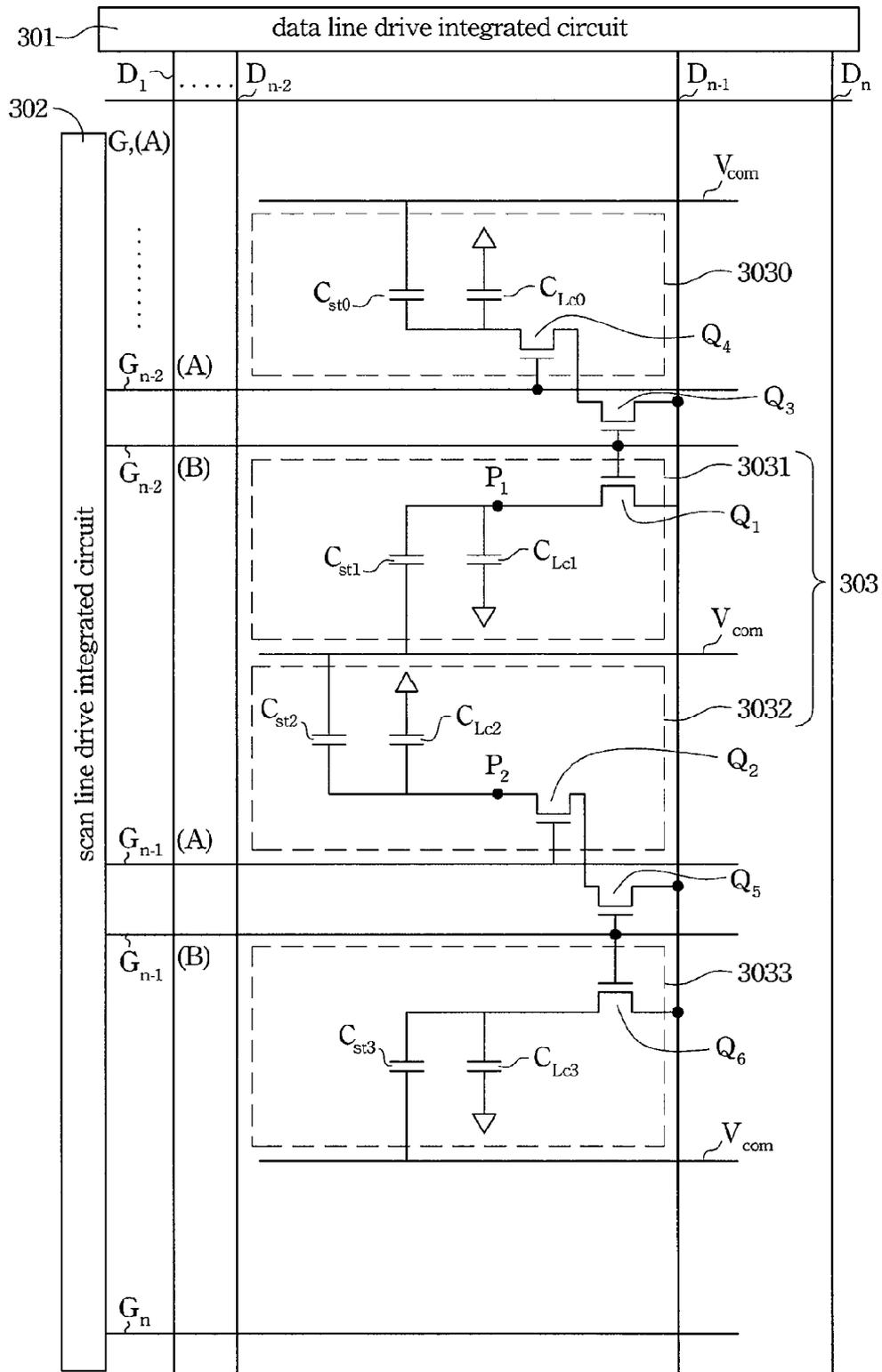


Fig. 3A



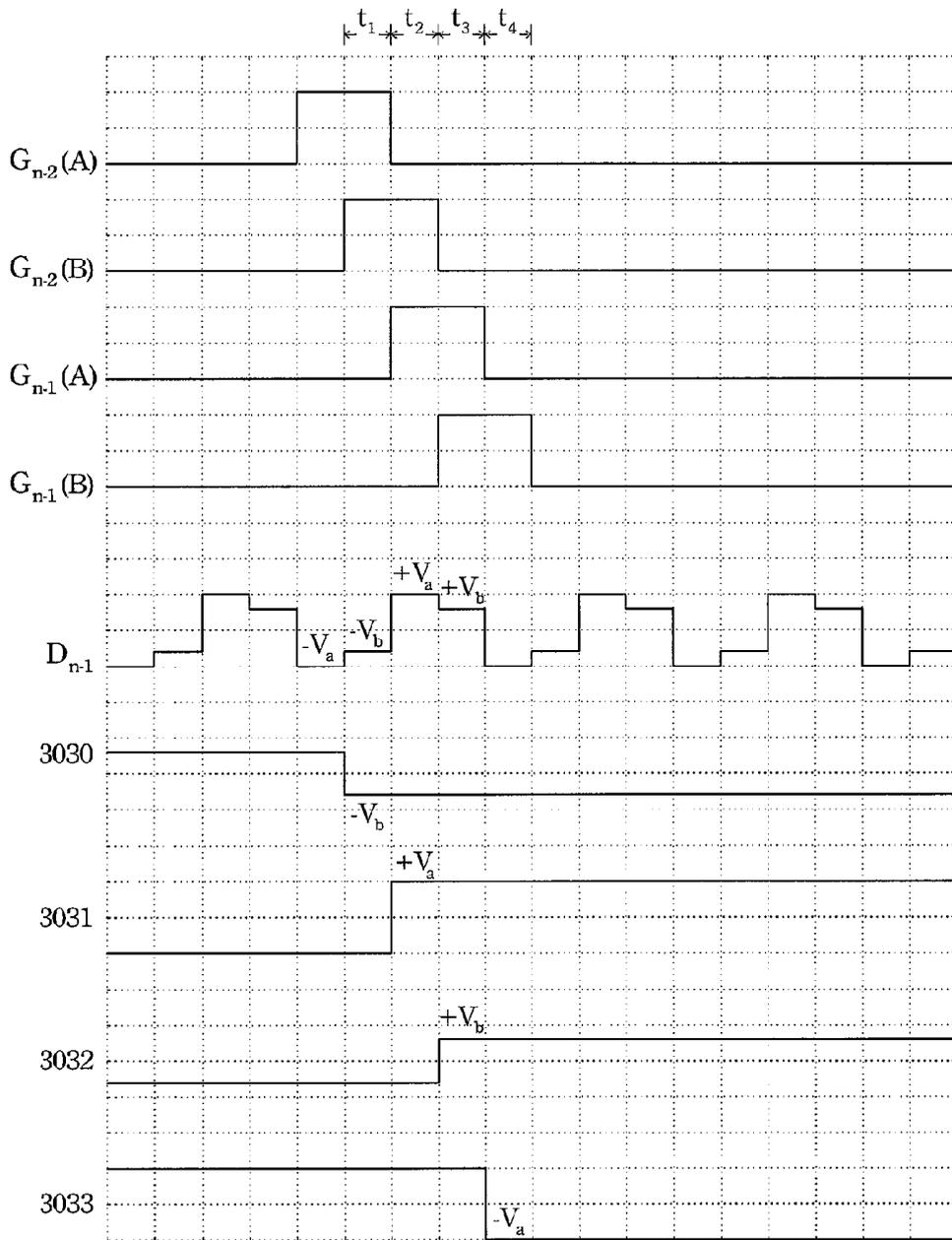


Fig. 4A

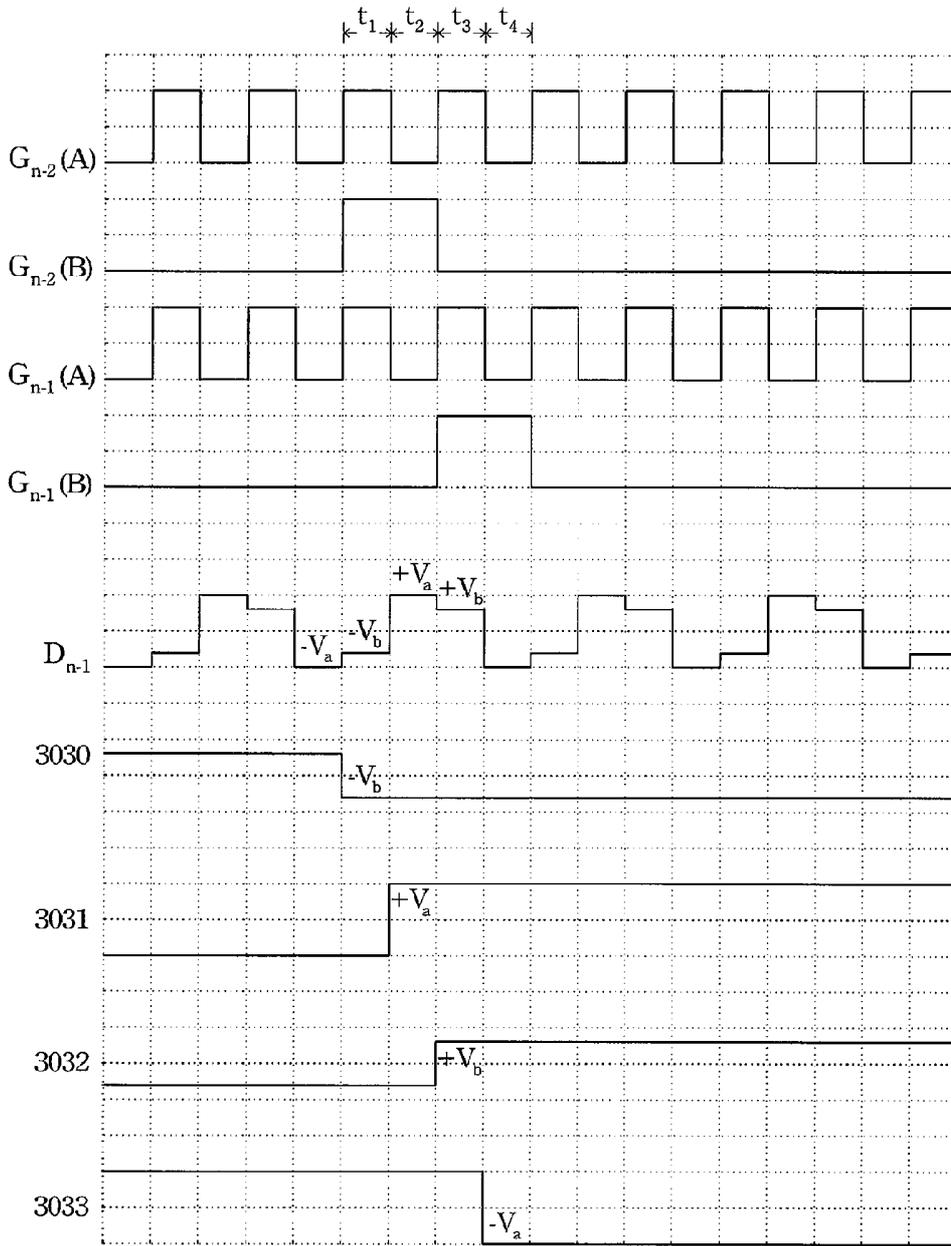


Fig. 4B

## LIQUID CRYSTAL DISPLAY AND OPERATION METHOD THEREOF

### RELATED APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 11/745,663, filed May 08, 2007, which claims priority to Taiwan Patent Application Ser. No. 95131463, filed Aug. 25, 2006, which is herein incorporated by reference.

### FIELD OF THE INVENTION

[0002] The present invention relates to a liquid crystal display, and more particularly to a liquid crystal display with improved view angles.

### BACKGROUND OF THE INVENTION

[0003] Liquid crystal displays have been used in various electronic devices. A Multi-Domain Vertically Aligned Mode (MVA mode) liquid crystal display is developed by Fujitsu in 1997 to provide a wider viewing range. In the MVA mode, a 160 degree view angle and a high response speed may be realized. However, when a user looks at this LCD from the oblique direction, the skin color of Asian people (light orange or pink) appears bluish or whitish from an oblique viewing direction. Such a phenomenon is called color shift.

[0004] The transmittance-voltage (T-V) characteristic of the MVA mode liquid crystal display is shown in FIG. 1. The vertical axis is the transmittance rate. The horizontal axis is the applied voltage. When the applied voltage is increased, the transmittance rate curve **101** in the normal direction is also increased. The transmittance changes monotonically as the applied voltage increases. In the oblique direction, the transmittance rate curve **102** winds and the various gray scales become the same. However, in the region **100**, when the applied voltage is increased, the transmittance rate curve **102** is not increased. That is the reason to cause the color shift.

[0005] A method is provided to improve the foregoing problem. According to the method, a pixel unit is divided into two sub pixels. The two sub pixels may generate two different T-V characteristics. By combining the two different T-V characteristics, a monotonic T-V characteristic can be realized. The line **201** in FIG. 2 shows the T-V characteristic of a sub-pixel. The line **202** in FIG. 2 shows the T-V characteristic of another sub-pixel. By combining the two different T-V characteristics of line **201** and line **202**, a monotonic T-V characteristic can be realized, as shown by the line **203** in FIG. 2.

[0006] Therefore, a pixel unit with two sub pixels and drive method thereof are required.

### SUMMARY OF THE INVENTION

[0007] One object of the present invention is to provide a liquid crystal display with a wide view angle.

[0008] Another object of the present invention is to provide a pixel with two sub pixels.

[0009] One aspect of the present invention is directed to a liquid crystal display with a plurality of pixel unit that may be drove by a drive wave to form two different pixel electrode voltages in a pixel unit.

[0010] Another aspect of the present invention is directed to a method for driving a liquid crystal display with a plurality of pixel unit, wherein each pixel unit has two sub pixels.

[0011] Accordingly, the present invention provides a liquid crystal display, comprising: a plurality of data lines; a plurality of scan lines crossing said data lines, wherein said scan lines are grouped into a first group and a second group and are alternatively arranged, adjacent data lines and adjacent scan lines define a pixel; a plurality of common electrodes respectively located in corresponding pixels to divide pixels to first sub-pixels and second sub-pixels; a plurality of switching devices formed in the locations of the scan lines crossing the data lines, wherein part of the switching devices connected with the second group's scan line are connected to the first group's scan line and the other switching devices connected with the second group's scan line are located in corresponding first sub-pixels, and wherein the switching devices connected with the first group's scan line are located in corresponding second sub-pixels and are coupled to corresponding data line through the switching devices connected with the second group's scan line; and a plurality pixel electrodes connected to the switching devices respectively.

[0012] According to an embodiment, the liquid crystal display further comprises a data line drive integrated circuit for driving said data lines.

[0013] According to an embodiment, the liquid crystal display further comprises a scan line drive integrated circuit for driving said scan lines.

[0014] Accordingly, the present invention provides a liquid crystal display, comprising: a plurality of data lines; a plurality of scan lines crossing the data lines, wherein adjacent first and second data lines and adjacent first and second scan lines define a pixel, wherein each pixel comprises: a first pixel electrode; a second pixel electrode; a common electrode, wherein the common electrode and the first pixel electrode define a first sub-pixel and the common electrode and the second pixel electrode define a second sub-pixel; a first transistor located in the first sub-pixel, a gate electrode of the first transistor is connected to the first scan line, a first source/drain electrode of the first transistor is connected to the first data line and a second source/drain electrode of the first transistor is connected to the first pixel electrode; a second transistor located in the second sub-pixel, a gate electrode and a first source/drain electrode of the first transistor is connected to the second scan line and a second source/drain electrode of the first transistor is connected to the second pixel electrode; and a third transistor located between two adjacent pixel, a gate electrode of the third transistor is connected to the first scan line, a second source/drain electrode of the third transistor is connected to the second scan line and a first source/drain electrode of the third transistor is connected to the first data line, wherein the second transistor is coupled to the first data line through the third transistor.

[0015] According to an embodiment, the common electrode and corresponding pixel electrode form storage capacitor.

[0016] According to an embodiment, the embodiment provides a drive method for driving a liquid crystal display disclosed in the above, the method comprises: providing a first signal to the first scan line; providing a second signal to the second scan line, wherein a time difference exists between the first signal and the second signal; and providing two-step signals to the data lines sequentially, the two-step signal includes a first voltage signal and a second voltage signal, wherein the first voltage signal is written to the first sub-pixel through the first transistor when the first scan line is driven by the first signal, and the second voltage signal is written to the

second sub-pixel through the second transistor and the third transistor when the first scan line is not driven and the second scan line is driven by the second signal and adjacent pixel's first scan line is driven by the first signal.

**[0017]** According to an embodiment, the time difference is equal to half width of the first signal.

**[0018]** According to an embodiment, the first signal and the second signal are pulse signals.

**[0019]** According to an embodiment, the first signal is a pulse signal and the second signal is a clock signal.

**[0020]** According to an embodiment, further comprises the second scan line is driven by pulse signal when the first scan line is driven by pulse signal.

**[0021]** According to an embodiment, further comprises the second scan line is driven by clock signal when the first scan line is driven by pulse signal.

**[0022]** Accordingly, a pixel unit in the present invention is divided into two sub-pixels. Each sub-pixel includes a thin film transistor, a liquid crystal capacitor and a storage capacitor. The two transistors respectively located in different sub-pixels are connected to different scan lines. One of the two transistors is connected to the data line through another transistor. Therefore, two different pixel voltages are formed in a pixel.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0023]** The foregoing aspects and many of the attendant advantages of this invention are more readily appreciated and better understood by referencing the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

**[0024]** FIG. 1 and FIG. 2 illustrate the transmittance-voltage (T-V) characteristic of MVA mode liquid crystal display;

**[0025]** FIG. 3A illustrates a top view of a liquid crystal display according to the first embodiment of the present invention.

**[0026]** FIG. 3B illustrates an enlarged schematic diagram of a pixel unit according to an embodiment of the present invention.

**[0027]** FIG. 4A illustrates a drive waveform and the corresponding electric voltage of four adjacent sub pixels according to an embodiment of the present invention.

**[0028]** FIG. 4B illustrates a drive waveform and the corresponding electric voltage of four adjacent sub pixels according to another embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

**[0029]** FIG. 3A illustrates a top view of a liquid crystal display according to the first embodiment of the present invention. The Liquid crystal display is composed of data lines  $D_1, D_2, D_3, \dots, D_n$ , the scan lines  $G_1(A), G_2(A), G_3(A), \dots, G_n(A)$  of group A and the scan lines  $G_2(B), G_3(B), \dots, G_{n-1}(B)$  of group B. These scan lines are arranged in parallel to each other. Moreover, the scan lines of group A and the scan lines of group B are alternatively formed over a substrate (not shown in this figure).

**[0030]** The data lines and the scan lines are perpendicular to each other. Adjacent two data lines and adjacent two scan lines respectively belong to the group A and group B define a pixel unit. Each pixel includes a common electrode  $V_{com}$  parallel to the scan line. According to the present invention, two transistors are connected to the scan line of group B

located between adjacent two pixels to control the data of the data line to transfer to the corresponding pixel.

**[0031]** According to the present invention, a pixel includes two sub-pixels. Each sub-pixel includes a storage capacitor, a liquid crystal capacitor and a thin film transistor. The storage capacitor is composed of the pixel electrode and the common electrode. The liquid crystal capacitor is composed of the pixel electrode and the conductive electrode in the upper substrate (not shown in figure). The thin film transistor is formed in the location that the data line crosses the scan line. According to the present invention, the transistors located in adjacent two sub-pixels are connected to adjacent two scan lines that belong to the group A and group B respectively. These two scan lines are connected together through a transistor that is controlled by this scan line of group B. A data line drive integrated circuit **301** is used to control the data lines  $D_1, D_2, D_3, \dots, D_n$ . A scan line drive integrated circuit **302** is used to control the scan lines  $G_1(A), G_2(A), G_3(A), \dots, G_n(A)$  of group A and the scan lines  $G_2(B), G_3(B), \dots, G_{n-1}(B)$  of group B.

**[0032]** The storage capacitors and the liquid crystal capacitors in the sub pixels described in the following are indicated by different symbols. These symbols are not related to their capacitance.

**[0033]** FIG. 3B illustrates an enlarged diagram of a pixel. The pixel **303** is defined by the data lines  $D_{n-2}, D_{n-1}$  and the scan lines  $G_{n-2}(B), G_{n-1}(A)$ . A common electrode  $V_{com}$  parallel to the scan line is arranged between the scan line  $G_{n-2}(B)$  and the scan line  $G_{n-1}(A)$ . The pixel **303** is divided into two sub-pixels. The sub-pixel **3031** is located between the scan line  $G_{n-2}(B)$  and the common electrode  $V_{com}$ . The sub pixel **3032** is located between the scan line  $G_{n-1}(A)$  and the common electrode  $V_{com}$ .

**[0034]** The sub-pixel **3031** includes a transistor  $Q_1$ . According to the transistor  $Q_1$ , the gate electrode is connected to the scan line  $G_{n-2}(B)$ , the first source/drain electrode is connected to the data line  $D_{n-1}$  and the second source/drain electrode is connected to the pixel electrode  $P_1$ . The storage capacitor  $C_{st1}$  is composed of the pixel electrode  $P_1$  and the common electrode  $V_{com}$ . The liquid crystal capacitor  $C_{LC1}$  is composed of the pixel electrode  $P_1$  and the conductive electrode in the upper substrate (not shown in figure).

**[0035]** The sub-pixel **3032** also includes a transistor  $Q_2$ . According to the transistor  $Q_2$ , the gate electrode is connected to the scan line  $G_{n-1}(A)$ , the first source/drain electrode is connected to the data line  $D_{n-1}$  through another transistor  $Q_5$  and the second source/drain electrode is connected to the pixel electrode  $P_2$ . The storage capacitor  $C_{st2}$  is composed of the pixel electrode  $P_2$  and the common electrode  $V_{com}$ . The liquid crystal capacitor  $C_{LC2}$  is composed of the pixel electrode  $P_2$  and the conductive electrode in the upper substrate (not shown in figure). In addition, according to the transistor  $Q_5$ , the gate electrode is connected to the scan line  $G_{n-1}(B)$ , the first source/drain electrode is connected to the data line  $D_{n-1}$ . The adjacent two scan lines, such as the scan line  $G_{n-1}(A)$  and  $G_{n-1}(B)$ , are connected together through the transistor  $Q_5$ .

**[0036]** The transistors  $Q_1, Q_2$  and  $Q_5$  act as switches. When a scan voltage is applied to the gate electrode of a transistor, the data voltage in the data line is transferred to the second source/drain electrode and is written into the corresponding storage capacitor and the liquid crystal capacitor. In this invention, the transistor  $Q_2$  is not directly connected to the data line  $D_{n-1}$ . This transistor  $Q_2$  is connected to the data line

$D_{n-1}$  through the transistor  $Q_5$ . In other words, the transistor  $Q_2$  and the transistor  $Q_5$  together control the sub-pixel **3032** whether or not to display the data in the data line. Therefore, when a data is written into the storage capacitor  $C_{st2}$  and the liquid crystal capacitor  $C_{LC2}$ , the transistor  $Q_2$  and the transistor  $Q_5$  have to be conducted together. Accordingly, in the present invention, a voltage waveform in the scan line is used to control the transistors  $Q_1$ ,  $Q_2$  and  $Q_5$  to co-operates with the voltage waveform in the data line to make the two sub-pixels **3031** and **3032** have different pixel voltages.

**[0037]** FIG. 4A illustrates a drive waveform and the corresponding electric voltage of four adjacent sub pixels according to an embodiment of the present invention. The drive signal of each scan line is pulse. When scanning, drive signal is sequentially transferred to these scan lines. The time difference between the two drive signals transferred to adjacent scan lines respectively is half period of the pulse. In other words, the two drive signals transferred to adjacent scan lines respectively partially overlap. Therefore, in the time period of the two drive signals overlapping, the transistors connected with the two scan lines are turned on together.

**[0038]** In this embodiment, the drive waveform of the data line is a two steps drive waveform. The positive part of this drive waveform includes two drive voltage  $V_a$  and  $V_b$ . The negative part of this drive waveform also includes two drive voltage  $-V_a$  and  $-V_b$ . The absolute value of the drive voltage  $V_a$  is larger than the absolute value of the drive voltage  $V_b$ .

**[0039]** Please refer to the FIG. 3A and FIG. 4A. During the time segment  $t_1$ , the voltage state of both the scan line  $G_{n-2}(A)$  and  $G_{n-2}(B)$  are in a high level state. The voltage state of both the scan line  $G_{n-1}(A)$  and  $G_{n-1}(B)$  are in a low level state. Therefore, the transistors  $Q_1$ ,  $Q_3$  and  $Q_4$  are turned on and the transistors  $Q_2$ ,  $Q_5$  and  $Q_6$  are turned off. In this case, the voltage  $-V_b$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitors  $C_{LC0}$  and the storage capacitors  $C_{st0}$  through the transistors  $Q_3$  and  $Q_4$ . At this time, the sub-pixel **3030** may present the pixel voltage,  $-V_b$ . Moreover, the voltage  $-V_b$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitors  $C_{LC1}$  and the storage capacitors  $C_{st1}$  through the transistor  $Q_1$ . At this time, the sub-pixel **3031** may also present the pixel voltage,  $-V_b$ . The transistors  $Q_2$ ,  $Q_5$  and  $Q_6$  are turned off. Therefore, the pixel voltage of the sub-pixels **3032** and **3033** is not changed. In this embodiment, the sub-pixel **3032** presents the pixel voltage,  $-V_b$ . The sub-pixel **3033** presents the pixel voltage,  $-V_b$ .

**[0040]** During the time segment  $t_2$ , the voltage state of both the scan line  $G_{n-2}(B)$  and  $G_{n-1}(A)$  are in a high level state. The voltage state of both the scan line  $G_{n-2}(A)$  and  $G_{n-1}(B)$  are in a low level state. Therefore, the transistors  $Q_1$ ,  $Q_2$  and  $Q_3$  are turned on and the transistors  $Q_4$ ,  $Q_5$  and  $Q_6$  are turned off. In this case, the voltage  $+V_a$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitor  $C_{LC1}$  and the storage capacitor  $C_{st1}$  through the transistor  $Q_1$ . At this time, the sub-pixel **3031** may present the pixel voltage,  $+V_a$ . The transistors  $Q_4$ ,  $Q_5$  and  $Q_6$  are turned off. Therefore, the liquid crystal capacitors  $C_{LC0}$ ,  $C_{LC2}$  and  $C_{LC3}$  and the storage capacitors  $C_{st0}$ ,  $C_{st2}$  and  $C_{st3}$  coupling with the transistors  $Q_4$ ,  $Q_5$  and  $Q_6$  respectively are not charged by the voltage  $+V_a$ . At this time, the sub-pixel **3030**, the sub-pixel **3032** and the sub-pixel **3033** still present the pixel voltage of the previous state. In other words, the sub-pixel **3030** presents the pixel voltage,  $-V_b$ . The sub-pixel **3032** presents the pixel voltage,  $-V_b$ . The sub-pixel **3033** presents the pixel voltage,  $+V_a$ .

**[0041]** During the time segment  $t_3$ , the voltage state of both the scan line  $G_{n-1}(A)$  and  $G_{n-1}(B)$  are in a high level state. The voltage state of both the scan line  $G_{n-2}(A)$  and  $G_{n-2}(B)$  are in a low level state. Therefore, the transistors  $Q_2$ ,  $Q_5$  and  $Q_6$  are turned on and the transistors  $Q_1$ ,  $Q_3$  and  $Q_4$  are turned off. In this case, the voltage  $+V_b$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitor  $C_{LC2}$  and the storage capacitor  $C_{st2}$  through the transistors  $Q_2$  and  $Q_5$ . At this time, the sub-pixel **3032** may present the pixel voltage,  $+V_b$ . On the other hand, the voltage  $+V_b$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitor  $C_{LC3}$  and the storage capacitor  $C_{st3}$  through the transistor  $Q_6$ . At this time, the sub-pixel **3033** may present the pixel voltage,  $+V_b$ . Because the transistors  $Q_3$  and  $Q_4$  are turned off, the liquid crystal capacitor  $C_{LC0}$  and the storage capacitor  $C_{st0}$  are not charged by the voltage  $+V_b$ . At this time, the sub-pixel **3030** still presents the pixel voltage,  $-V_b$ . On the other hand, because the transistor  $Q_1$  is turned off, the liquid crystal capacitors  $C_{LC1}$  and the storage capacitors  $C_{st1}$  are not charged by the voltage  $+V_b$ . At this time, the sub-pixel **3031** still present the pixel voltage,  $+V_a$ .

**[0042]** During the time segment  $t_4$ , the voltage state of the scan line  $G_{n-1}(B)$  is in a high level state. The voltage state of both the scan line  $G_{n-1}(A)$ ,  $G_{n-2}(A)$  and  $G_{n-2}(B)$  are in a low level state. Therefore, the transistors  $Q_5$  and  $Q_6$  are turned on and the transistors  $Q_1$ ,  $Q_2$ ,  $Q_3$  and  $Q_4$  are turned off. In this case, the voltage  $-V_b$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitor  $C_{LC3}$  and the storage capacitor  $C_{st3}$  through the transistor  $Q_6$ . At this time, the sub-pixel **3033** may present the pixel voltage,  $-V_b$ . Because the transistors  $Q_3$  and  $Q_4$  are turned off, the liquid crystal capacitor  $C_{LC0}$  and the storage capacitor  $C_{st0}$  are not charged by the voltage  $-V_b$ . At this time, the sub-pixel **3030** still presents a pixel voltage,  $-V_b$ . Because the transistor  $Q_1$  is turned off, the liquid crystal capacitors  $C_{LC1}$  and the storage capacitors  $C_{st1}$  are not charged by the voltage  $-V_b$ . At this time, the sub-pixel **3031** still presents the pixel voltage,  $+V_a$ . Because the transistor  $Q_2$  is turned off, the liquid crystal capacitors  $C_{LC2}$  and the storage capacitors  $C_{st2}$  are not charged by the voltage  $-V_b$ . At this time, the sub-pixel **3032** still presents the pixel voltage,  $+V_b$ . Accordingly, from the time segment  $t_1$  to  $t_4$ , at least two pixel voltages,  $V_b$  and  $+V_a$ , are presented in the pixel **303** together. Different pixel voltage may present different optical characteristics. Therefore, the color shift phenomenon may be eased by combining the two pixel voltages in a pixel.

**[0043]** FIG. 4B illustrates a drive waveform and the corresponding electric voltage of four adjacent sub pixels according to another embodiment of the present invention. The drive signal transferred in the scan line of the group A is a clock signal. The drive signal transferred in the scan line of the group B is pulse signal. When scanning, pulse signal is sequentially transferred to these scan lines of the group B. The pulse width is equal to the period the clock signal. In other words, the two drive signals, the clock signal and the pulse signal, transferred to adjacent scan lines respectively partially overlap. Therefore, in the time period of the two drive signals overlapping, the transistors connected with the two scan lines are turned on together.

**[0044]** In this embodiment, the drive waveform of the data line is a two steps drive waveform. The positive part of this drive waveform includes two drive voltage  $V_a$  and  $V_b$ . The negative part of this drive waveform also includes two drive voltage  $-V_a$  and  $-V_b$ . The absolute value of the drive voltage  $V_a$  is larger than the absolute value of the drive voltage  $V_b$ .

**[0045]** Please refer to the FIG. 3A and FIG. 4B. During the time segment  $t_1$ , the voltage state of the scan line  $G_{n-1}(A)$ ,  $G_{n-2}(A)$  and  $G_{n-2}(B)$  are in a high level state. The voltage state of the scan line  $G_{n-1}(B)$  is in a low level state. Therefore, the transistors  $Q_1$ ,  $Q_2$ ,  $Q_3$  and  $Q_4$  are turned on and the transistors  $Q_5$  and  $Q_6$  are turned off. In this case, the voltage  $-Vb$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitors  $C_{LC0}$  and the storage capacitors  $C_{st0}$  through the transistors  $Q_3$  and  $Q_4$ . At this time, the sub-pixel **3030** may present the pixel voltage,  $-Vb$ . Moreover, the voltage  $-Vb$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitors  $C_{LC1}$  and the storage capacitors  $C_{st1}$  through the transistor  $Q_1$ . At this time, the sub-pixel **3031** may also present the pixel voltage,  $-Vb$ . The transistors  $Q_5$  and  $Q_6$  are turned off. The transistor  $Q_2$  is connected to the data line  $D_{n-1}$  through the transistors  $Q_5$ . Therefore, the liquid crystal capacitor  $C_{LC2}$  and the storage capacitor  $C_{st2}$  are not charged by the voltage  $-Vb$ . On the other hand, because the transistor  $Q_6$  is turned off, the liquid crystal capacitors  $C_{LC3}$  and the storage capacitors  $C_{st3}$  are not charged by the voltage  $-Vb$ . Therefore, the sub-pixel **3032** and the sub-pixel **3033** still present the pixel voltage of the previous state. In this embodiment, the sub-pixel **3032** presents the pixel voltage,  $-Vb$ . The sub-pixel **3033** presents the pixel voltage,  $Va$ .

**[0046]** During the time segment  $t_2$ , the voltage state of both the scan line  $G_{n-2}(B)$  is in a high level state. The voltage state of the scan lines  $G_{n-1}(A)$ ,  $G_{n-2}(A)$  and  $G_{n-1}(B)$  are in a low level state. Therefore, the transistors  $Q_1$  and  $Q_3$  are turned on and the transistors  $Q_2$ ,  $Q_4$ ,  $Q_5$  and  $Q_6$  are turned off. In this case, the voltage  $+Va$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitor  $C_{LC1}$  and the storage capacitor  $C_{st1}$  through the transistor  $Q_1$ . At this time, the sub-pixel **3031** may present the pixel voltage,  $+Va$ . On the other hand, because the transistor  $Q_4$  is turned off, the liquid crystal capacitor  $C_{LC0}$  and the storage capacitor  $C_{st0}$  are not charged by the voltage  $+Va$ . At this time, the sub-pixel **3030** still presents the previous pixel voltage state,  $-Vb$ . Because the transistor  $Q_1$  and  $Q_5$  are turned off, the liquid crystal capacitors  $C_{LC2}$  and the storage capacitors  $C_{st2}$  are not charged by the voltage  $+Va$ . At this time, the sub-pixel **3032** still present the previous pixel voltage state,  $-Vb$ . Because the transistor  $Q_6$  is turned off, the liquid crystal capacitors  $C_{LC3}$  and the storage capacitors  $C_{st3}$  are not charged by the voltage  $+Va$ . At this time, the sub-pixel **3033** still present the previous pixel voltage state,  $+Va$ .

**[0047]** During the time segment  $t_3$ , the voltage state of the scan line  $G_{n-1}(A)$ ,  $G_{n-2}(A)$  and  $G_{n-1}(B)$  are in a high level state. The voltage state of the scan line  $G_{n-2}(B)$  is in a low level state. Therefore, the transistors  $Q_2$ ,  $Q_4$ ,  $Q_5$  and  $Q_6$  are turned on and the transistors  $Q_1$ ,  $Q_3$  and are turned off. In this case, the voltage  $+Vb$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitor  $C_{LC2}$  and the storage capacitor  $C_{st2}$  through the transistors  $Q_2$  and  $Q_5$ . At this time, the sub-pixel **3032** may present the pixel voltage,  $+Vb$ . On the other hand, the voltage  $+Vb$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitor  $C_{LC3}$  and the storage capacitor  $C_{st3}$  through the transistor  $Q_6$ . At this time, the sub-pixel **3033** may present the pixel voltage,  $+Vb$ . Because the transistors  $Q_3$  and  $Q_4$  are turned off, the liquid crystal capacitor  $C_{LC0}$  and the storage capacitor  $C_{st0}$  are not charged by the voltage  $+Vb$ . At this time, the sub-pixel **3030** still presents the pixel voltage,  $-Vb$ . On the other hand, because the transistor  $Q_1$  is turned off, the liquid crystal capacitors  $C_{LC1}$  and the storage capacitors  $C_{st1}$  are not charged by the voltage  $+Vb$ . At this time, the sub-pixel **3031** still present the pixel voltage,  $+Va$ .

**[0048]** During the time segment  $t_4$ , the voltage state of the scan line  $G_{n-1}(B)$  is in a high level state. The voltage state of both the scan line  $G_{n-1}(A)$ ,  $G_{n-2}(A)$  and  $G_{n-2}(B)$  are in a low level state. Therefore, the transistors  $Q_5$  and  $Q_6$  are turned on and the transistors  $Q_1$ ,  $Q_2$ ,  $Q_3$  and  $Q_4$  are turned off. In this case, the voltage  $-Vb$  in the data line  $D_{n-1}$  may charge the liquid crystal capacitor  $C_{LC3}$  and the storage capacitor  $C_{st3}$  through the transistor  $Q_6$ . At this time, the sub-pixel **3033** may present the pixel voltage,  $-Vb$ . Because the transistors  $Q_3$  and  $Q_4$  are turned off, the liquid crystal capacitor  $C_{LC0}$  and the storage capacitor  $C_{st0}$  are not charged by the voltage  $-Vb$ . At this time, the sub-pixel **3030** still presents the previous pixel voltage state,  $-Vb$ . Because the transistor  $Q_1$  is turned off, the liquid crystal capacitors  $C_{LC1}$  and the storage capacitors  $C_{st1}$  are not charged by the voltage  $-Vb$ . At this time, the sub-pixel **3031** still presents the previous pixel voltage state,  $+Va$ . Because the transistor  $Q_2$  is turned off, the liquid crystal capacitors  $C_{LC2}$  and the storage capacitors  $C_{st2}$  are not charged by the voltage  $-Vb$ . At this time, the sub-pixel **3032** still presents the previous pixel voltage state,  $+Vb$ .

**[0049]** Accordingly, from the time segment  $t_1$  to  $t_4$ , at least two pixel voltages,  $Vb$  and  $+Va$ , are presented in the pixel **303** together. Different pixel voltage may present different optical characteristics. Therefore, the color shift phenomenon may be eased by combining the two pixel voltages in a pixel.

**[0050]** Accordingly, a pixel unit in the present invention is divided into two sub-pixels. Each sub-pixel includes a thin film transistor, a liquid crystal capacitor and a storage capacitor. The two transistors in a pixel are connected to different scan lines. One of the two transistors is connected to the data line through another transistor. Therefore, two different pixel voltages are formed in a pixel. The color shift phenomenon may be eased by combining the two pixel voltages in a pixel.

**[0051]** As is understood by a person skilled in the art, the foregoing descriptions of the preferred embodiment of the present invention are an illustration of the present invention rather than a limitation thereof. Various modifications and similar arrangements are included within the spirit and scope of the appended claims. The scope of the claims should be accorded to the broadest interpretation so as to encompass all such modifications and similar structures. While a preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A liquid crystal display, comprising:

- a plurality of data lines;
- a plurality of scan lines crossing said data lines, wherein said scan lines are grouped into a first group and a second group, and scan lines of the first group and scan lines of the second group are alternatively arranged;
- a plurality of pixels defined by two neighboring data lines and two neighboring scan lines crossing the two neighboring data lines;
- a plurality of common electrodes disposed in corresponding pixels to define said pixels to include a plurality of first sub-pixels and a plurality of second sub-pixels;
- a plurality of switching devices respectively formed in the locations of said scan lines crossing said data lines, wherein each of the pixels includes three switching devices, a first switching device, a second switching device and a third switching device, wherein the first switching device and the second switching device are

- directly connected to a first data line and the third switching device are connected to the first data line through the first switching device, wherein the second switching device connected with the second group's scan line is located in corresponding first sub-pixel, and the third switching device connected with the first group's scan line is located in corresponding second sub-pixel; and
- a plurality of pixel electrodes electrically coupled to said switching devices respectively.
2. The liquid crystal display of claim 1, wherein said switching device is a transistor.
3. The liquid crystal display of claim 1, wherein said common electrodes and said pixel electrodes form storage capacitors.
4. A liquid crystal display, comprising:
- a plurality of data lines a plurality of scan lines crossing said data lines, wherein said scan lines are grouped into a first group and a second group, and scan lines of the first group and scan lines of the second group are alternately arranged;
- a plurality of pixels defined by two neighboring data lines and two neighboring scan lines crossing the two neighboring data lines;
- a plurality of first and second switching devices respectively formed in the locations of the second group's scan lines crossing said data lines, wherein the first switching devices and the second switching devices are directly connected to corresponding data lines, and the second switching devices are located in pixels that are defined by the second group's scan line;
- a plurality of third switching devices respectively formed in the locations of the first group's scan lines crossing said data lines, and the third switching devices are located in pixels that are defined by the first group's scan line and the third switching devices are coupled to corresponding data lines through the first switching devices; and
- a plurality of pixel electrodes electrically coupled to the second and third switching devices.
5. The liquid crystal display of claim 4, wherein said switching device is a transistor.
6. The liquid crystal display of claim 4, wherein said common electrodes and said pixel electrodes form storage capacitors.
7. A liquid crystal display, comprising:
- a plurality of data lines;
- a plurality of scan lines crossing said data lines;
- a plurality of pixels defined by two neighboring data lines and two neighboring scan lines crossing the two neighboring data lines, wherein each pixel comprises:
- a first pixel electrode;
- a second pixel electrode;
- a common electrode, wherein said common electrode and said first pixel electrode define a first sub-pixel and said common electrode and said second pixel electrode define a second sub-pixel;
- a first transistor located in said first sub-pixel, a gate electrode of said first transistor is connected to said first scan line, a first source/drain electrode of said first transistor is directly connected to said first data line and a second source/drain electrode of said first transistor is connected to said first pixel electrode, wherein the first pixel electrode receives a data signal from the first data line through the first transistor;
- a second transistor located in said second sub-pixel, a gate electrode is connected to said second scan line and a second source/drain electrode of said second transistor is connected to said second pixel electrode; and
- a third transistor located between two adjacent pixel, a gate electrode of said third transistor is connected to said first scan line, a second source/drain electrode of said third transistor is connected to a first source/drain electrode of said second transistor and a first source/drain electrode of said third transistor is directly connected to said first data line, wherein said second transistor is coupled to said first data line through said third transistor, wherein the second pixel electrode receives a data signal from the first data line through the second transistor and the third transistor.
8. The liquid crystal display of claim 7, wherein said common electrode and corresponding pixel electrode form storage capacitor.

\* \* \* \* \*

专利名称(译)	液晶显示器及其操作方法		
公开(公告)号	<a href="#">US20110037688A1</a>	公开(公告)日	2011-02-17
申请号	US12/912230	申请日	2010-10-26
[标]申请(专利权)人(译)	友达光电股份有限公司		
申请(专利权)人(译)	友达光电股份有限公司		
当前申请(专利权)人(译)	友达光电股份有限公司		
[标]发明人	CHIANG MIN FENG HUANG HSUEH YING LAI MING SHENG		
发明人	CHIANG, MIN-FENG HUANG, HSUEH-YING LAI, MING-SHENG		
IPC分类号	G09G3/36		
CPC分类号	G02F1/13624 G02F2001/134345 G09G3/3659 G09G2320/028 G09G2300/0447 G09G2310/0205 G09G2300/0443		
优先权	095131463 2006-08-25 TW		
其他公开文献	US8217879		
外部链接	<a href="#">Espacenet</a> <a href="#">USPTO</a>		

摘要(译)

本发明中的像素单元分为两个子像素。每个子像素包括薄膜晶体管，液晶电容器和存储电容器。分别位于不同子像素中的两个晶体管连接到不同的扫描线。两个晶体管中的一个通过另一个晶体管连接到数据线。因此，在像素中形成两个不同的像素电压。

