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(54) ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME

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(57) **ABSTRACT**

Array substrates for liquid crystal display (LCD) devices are formed on a substrate with first and second gate lines crossing a data line to define first and second pixel regions. A thin film transistor includes a source electrode and a drain electrode. A metal pattern overlaps a common line and makes up a portion of the drain electrode. A passivation layer is disposed on the source and drain electrodes and on the metal pattern. A first pixel electrode is connected to the metal pattern and a common electrode is connected to the common line. Various repair patterns are formed to define one or more repairing portions that enable connection of the drain electrode or metal pattern to a second pixel electrode of the second pixel region if the cut line is cut in the event the first pixel electrode fails to display an image.

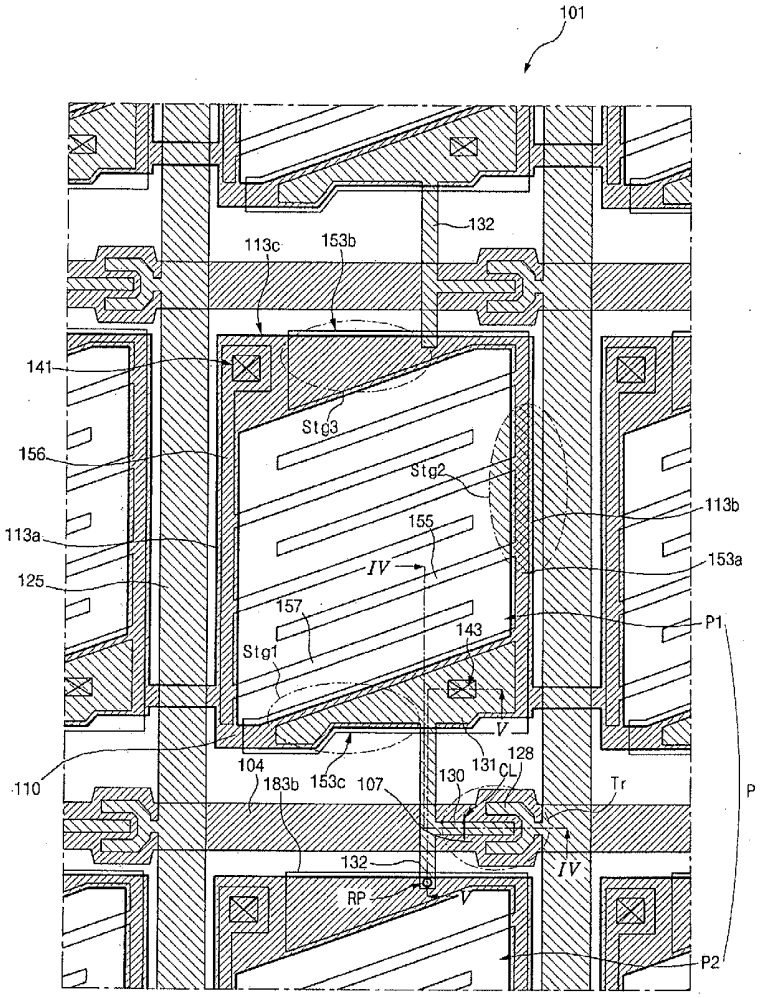


FIG. 1
RELATED ART

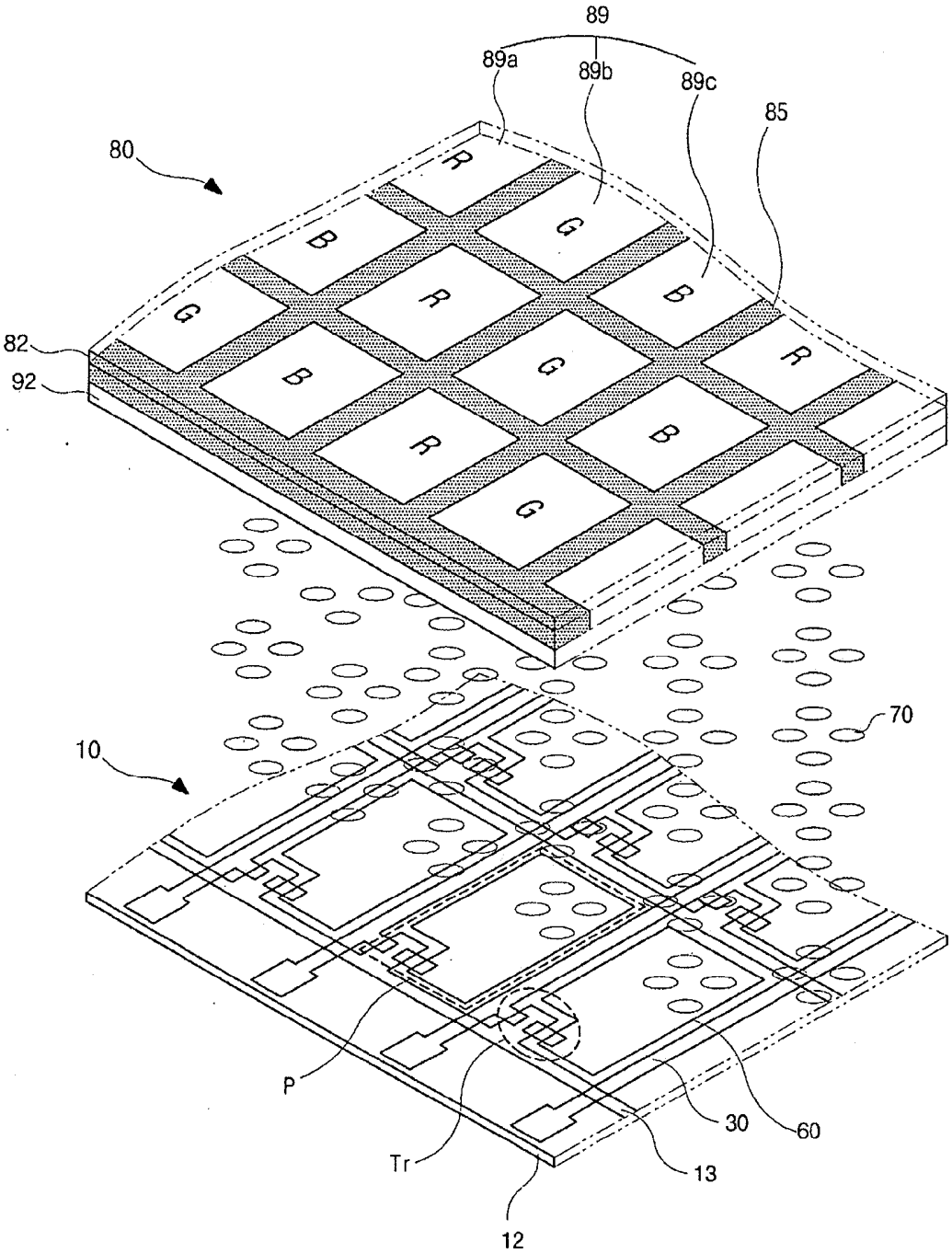


FIG. 2
RELATED ART

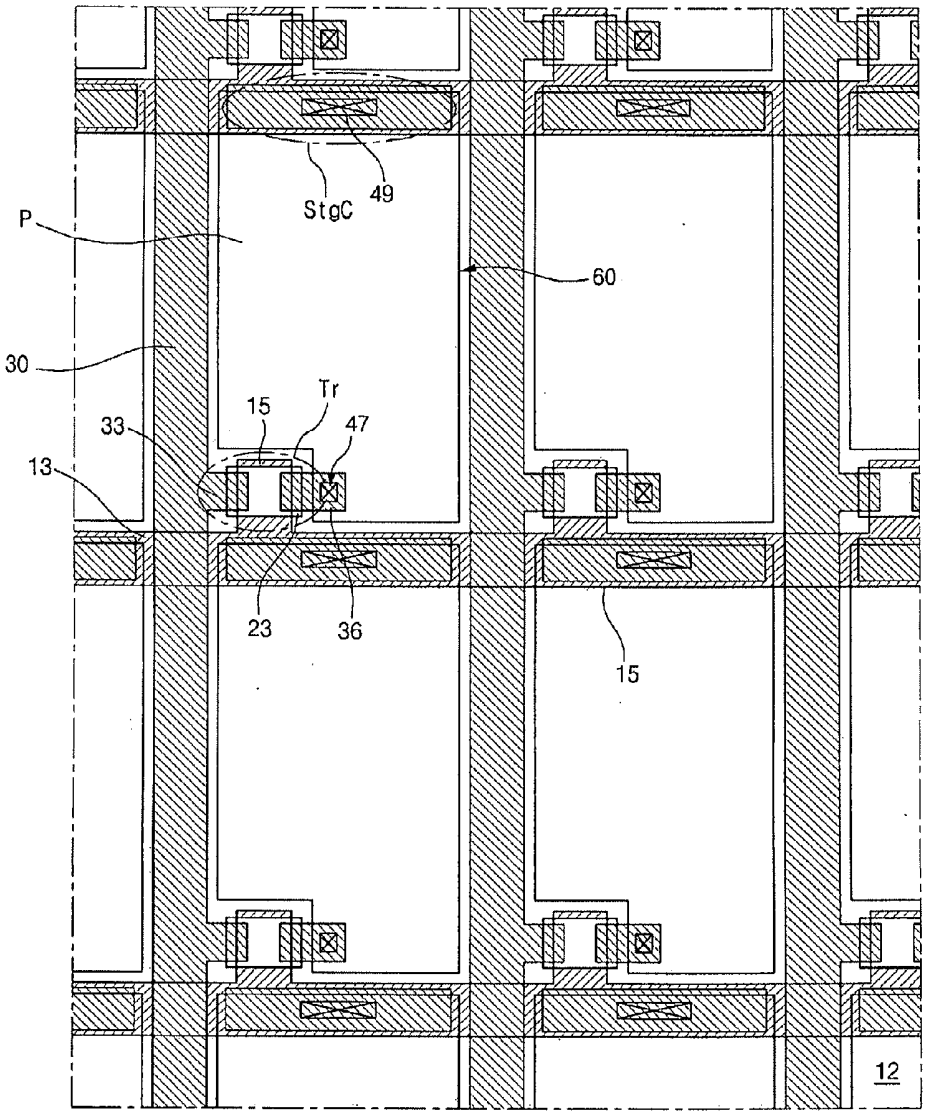


FIG. 3

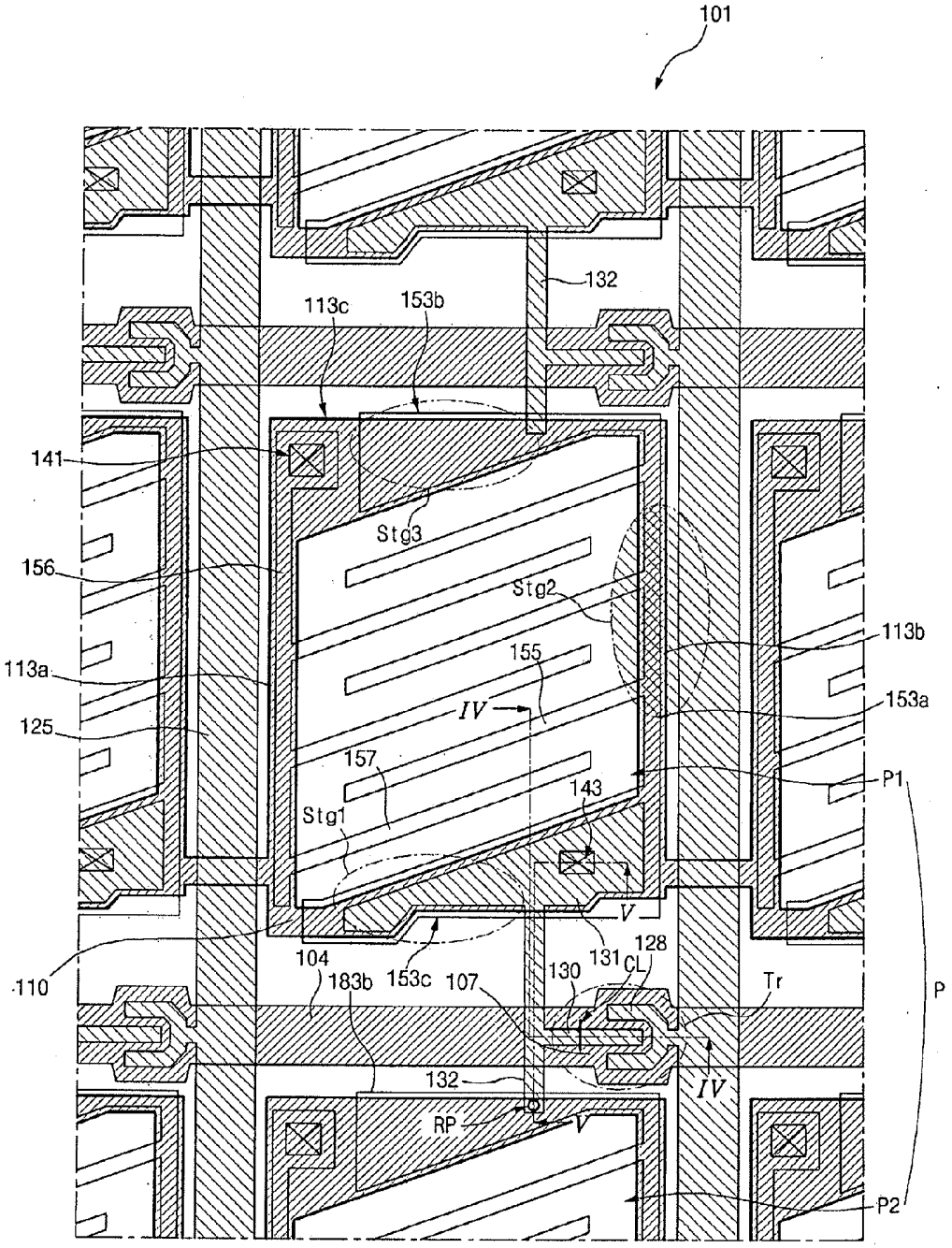

101
132
113c
153b
141
Stg3
156
Stg2
113b
113a
155
153a
125
IV
157
P1
143
Stg1
V
110
104
153c
131
128
CL
130
107
183b
Tr
P
132
IV
RP
V
P2

FIG. 4

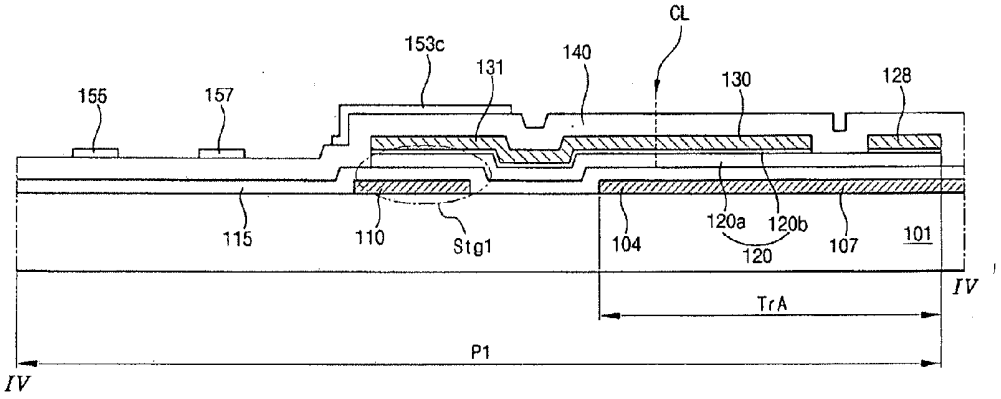

CL
153c
131
140
130
128
155
157
115
110
Stg1
104
120a
120b
120
107
101
IV
TrA
P1
IV

FIG. 5

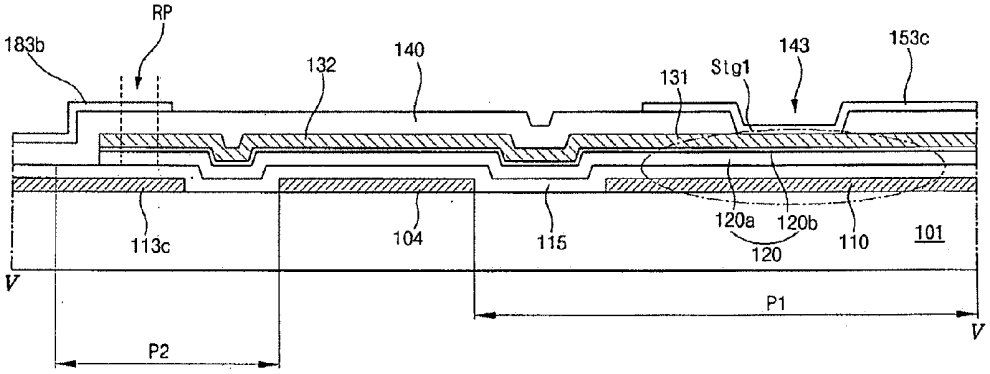

RP
183b
132
140
131
Stg1
143
153c
113c
104
115
120a
120b
120
110
101
V
P1
V
P2

FIG. 6

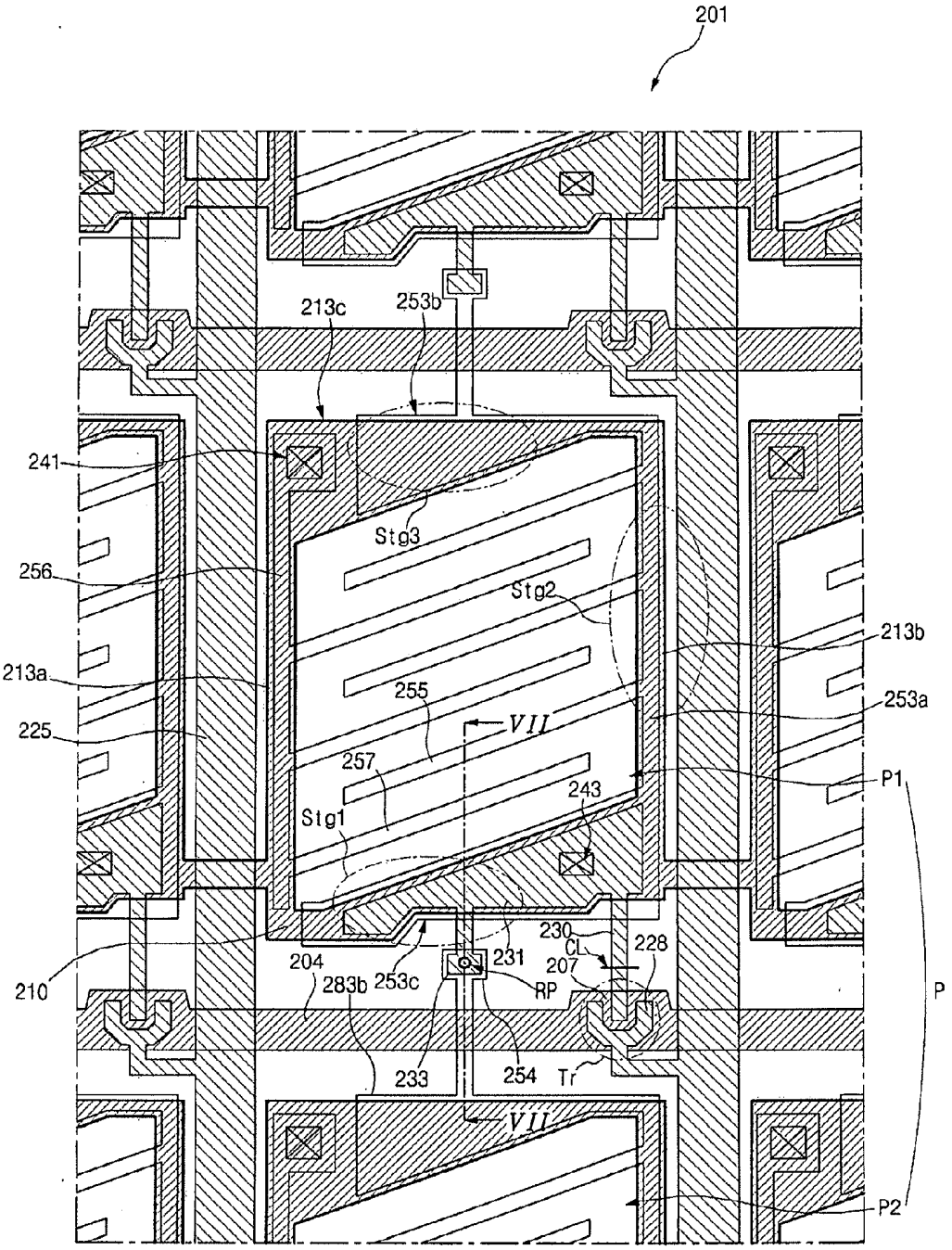

201
213c
253b
241
Stg3
256
Stg2
213b
213a
255
253a
225
VII
257
P1
243
Stg1
230
CL
228
210
204
231
207
283b
253c
RP
P
233
254
Tr
VII
P2

FIG. 7

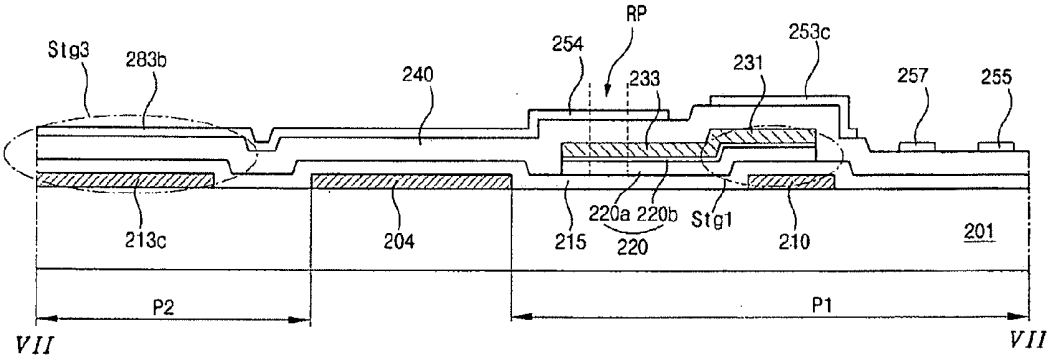

Stg3
283b
240
254
RP
233
231
253c
257
255
213c
204
215
220a 220b
220
Stg1
210
201
P2
P1
VII
VII

FIG. 8

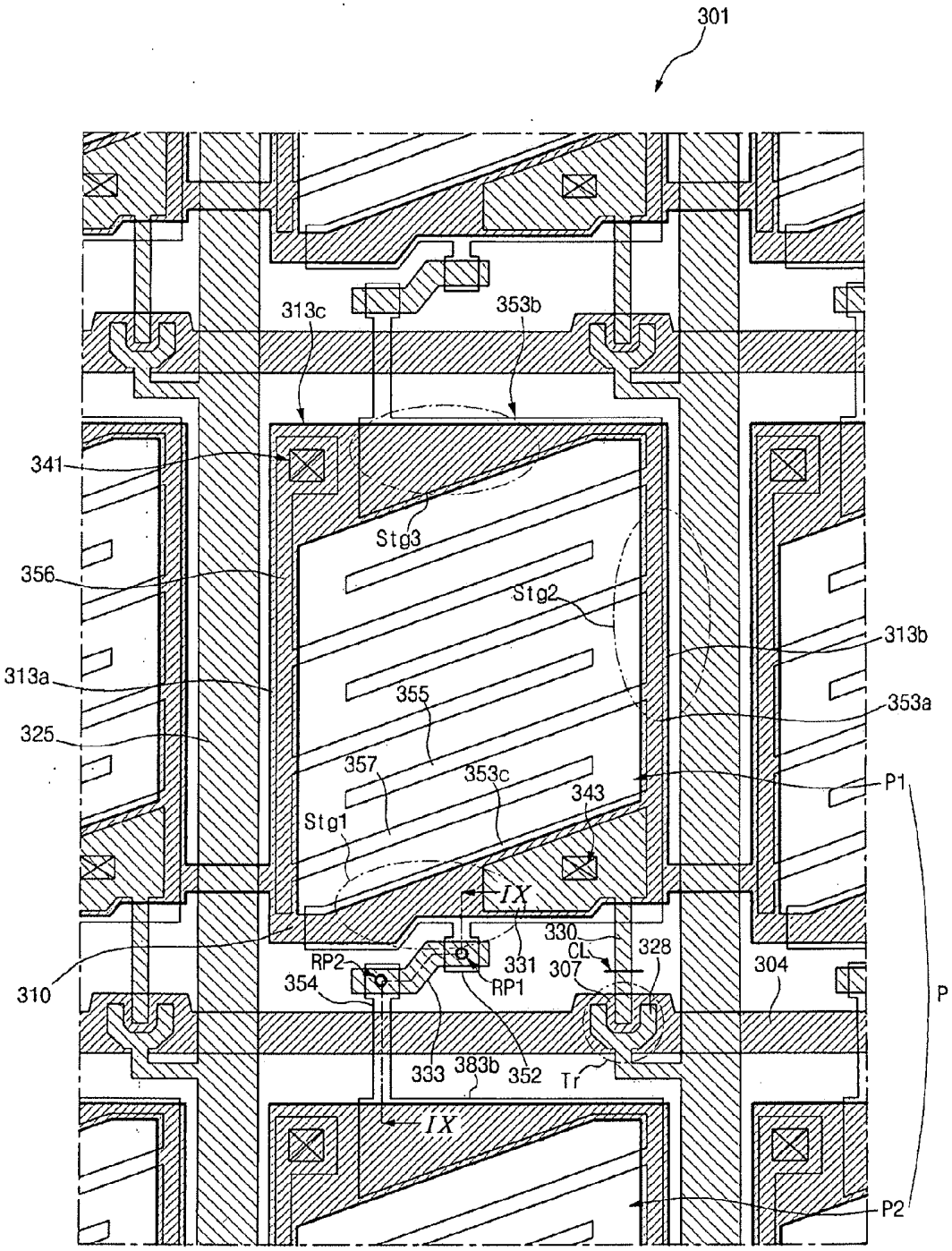
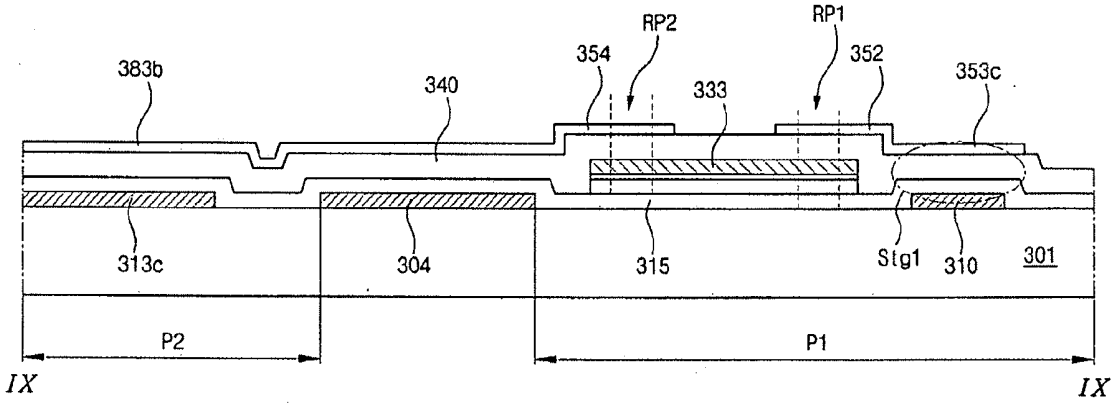

301
313c
353b
341
Stg3
356
Stg2
313b
313a
355
353a
325
357
353c
P1
343
Stg1
IX
330
CL
328
RP2
331
307
304
310
354
RP1
P
333
383b
352
Tr
IX
P2

FIG. 9


RP2
RP1
354
352
383b
340
333
353c
313c
304
315
Stg1
310
301
P2
P1
IX
IX

ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME

[0001] The present patent document is a divisional of U.S. patent application Ser. No. 11/824,041, filed Jun. 29, 2007, which claims priority to Korean Patent Application No. 2006-0137829 filed in Korea on Dec. 29, 2006, which are hereby incorporated by reference.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present disclosure relates to an array substrate for a liquid crystal display (LCD) device, and more particularly, to an array substrate for an LCD device having a repair pattern.

[0004] 2. Discussion of the Related Art

[0005] The conventional LCD devices use an optical anisotropic property and polarization properties of liquid crystal molecules to display images. The liquid crystal molecules have orientation characteristics of arrangement resulting from their long, thin shape. Thus, an arrangement direction of the liquid crystal molecules can be controlled by applying an electrical field to them. Accordingly, when the electric field is applied to them, polarization properties of light are changed according to the arrangement of the liquid crystal molecules such that the LCD devices display images.

[0006] The LCD device includes a first substrate, a second substrate, and a liquid crystal layer interposed therebetween. A common electrode and a pixel electrode are respectively formed on the first and second substrates. The first and second substrates may be referred to as a color substrate and an array substrate, respectively. The liquid crystal layer is driven by a vertical electric field induced between the common and pixel electrodes. LCD devices typically have excellent transmittance and aperture ratios.

[0007] Among the known types of LCD devices, active matrix LCD (AM-LCD) devices that have thin film transistors (TFTs) arranged in a matrix form are the subject of significant research and development because of their high resolution and superior ability in displaying moving images.

[0008] FIG. **1** is an exploded perspective view of a conventional liquid crystal panel of an LCD device. As shown in FIG. **1**, the liquid crystal panel includes an array substrate **10**, a color filter substrate **80**, and a liquid crystal layer **70**. The array substrate **10** and the color filter substrate **80** face each other. The liquid crystal layer **70** is interposed therebetween.

[0009] The array substrate **10** includes a first substrate **12**, a gate line **13**, a data line **30**, a thin film transistor (TFT) Tr, and a pixel electrode **60**. The gate and data lines **13** and **30** are formed on the first substrate **12** and cross each other to define a pixel region P. The TFT Tr is formed at a crossing portion of the gate and data lines **13** and **30**. The pixel electrode **60** is formed in the pixel region P and connected to the TFT Tr.

[0010] The color filter substrate **80** includes a second substrate **82**, a black matrix **85**, a color filter layer **89**, and a common electrode **92**. The black matrix **85** is formed on the second substrate **82** and has a lattice shape. The black matrix **85** corresponds to a non-display region of the first substrate **12**. The non-display region of the first substrate **12** also includes the gate and data lines **13** and **30** and the TFT Tr. The color filter layer **89** corresponds to the pixel region "P" and has one of red (R), green (G), and blue (B) colors **89***a*, **89***b*, and **89***c*. The common electrode **92** is formed on the black matrix **85** and the color filter layer **89**. The common electrode **92** generates an electric field with the pixel electrode **60** such that the liquid crystal layer **70** is driven by the electric field.

[0011] Though not shown, first and second polarization plates may be formed on an outer surface of the first and second substrates **12** and **82**. The first and second polarization plates respectively have first and second optical axes, and light parallel to each of the first and second optical axes can be passed through the first and second polarization plates, respectively. Moreover, a backlight assembly is formed on a rear side of the first substrate **12** to apply light into the liquid crystal panel.

[0012] FIG. **2** is a plane view showing an array substrate for an LCD device according to the related art. As shown in FIG. **2**, a plurality of gate lines **13** and a plurality of data lines **30** are formed on a first substrate **12**. The plurality of gate lines **13** and the plurality of data lines **30** cross each other such that a plurality of pixel regions P are defined. A gate pad (not shown) is formed at an end of each gate line **13**. Each gate line **13** is connected to a gate driving circuit (not shown) via the gate pad. A data pad (not shown) is formed at an end of each data line **30**. Each data line **30** is connected to a data driving circuit (not shown) via the data pad.

[0013] A thin film transistor (TFT) Tr is formed in each pixel region P. The TFT Tr is connected to the gate and data lines **13** and **30**. A gate electrode **15**, a semiconductor layer **23**, a source electrode **33** and a drain electrode **36** constitute the TFT Tr. The gate electrode **15** is connected to the gate line **13**, and the source electrode **33** is connected to the data line **30**. The drain electrode **36** is spaced apart from the source electrode **33**. A pixel electrode **60** is formed in each pixel region P. The pixel electrode **60** is connected to the drain electrode **36** through a drain contact hole **47**. Moreover, a storage capacitor StgC is formed over the gate line **13**. A storage pattern **15** overlaps the gate line **13** and is connected to the pixel electrode **60** through a storage contact hole **49**. The overlapped portion of the gate line **13** functions as a first electrode, and the storage pattern **15** functions as a second electrode. An insulating layer (not shown) interposed between the overlapped portion of the gate line **13** and the storage pattern **15** functions as a dielectric material. The first electrode, the second electrode, and the insulating layer constitute the storage capacitor StgC.

[0014] The array substrate is fabricated through complicated processes such that defects may arise during the processes. Static electricity may be generated during the process. Moreover, the TFT may be deteriorate due to impurities such that the TFT does not have its desired functions. In this case, the defects may be repaired by disconnecting the pixel electrode **60** and the drain electrode **36** in the pixel region P. As a result, the LCD device displays only white color in a normally white mode and black color in a normally black mode in the pixel region P having the pixel electrode **60** disconnected from the drain electrode **36**. In the normally white mode, white color is displayed in the pixel region P in which a signal is not applied. In contrast, in the normally black mode, black color is displayed in the pixel region in which a signal is not applied.

[0015] The LCD device may have tens of thousands to tens of millions of the pixel regions P depending on size or resolution of the liquid crystal panel. If the LCD devices are considered acceptable for sale only when all pixel regions P function well, production yield becomes too low. Accord-

ingly, although some pixel regions P do not display desired images, the LCD devices are treated as acceptable for sale and considered to be without defect. A method of repairing by disconnecting the pixel electrode **60** from the drain electrode **36** in some pixel regions P may not affect quality of the displaying images.

[0016] However, there are some problems. When the LCD device has the normally black mode and displays bright images, the repaired pixel region P in which black color is normally displayed may be conspicuous. In contrast, when the LCD device has the normally white mode and displays dark images, the repaired pixel region in which white color is normally displayed may be conspicuous.

BRIEF SUMMARY

[0017] Accordingly, the present disclosure is directed to an array substrate, and method of fabrication, for an in-plane switching mode liquid crystal device (IPS-LCD) that provides one or more advantages over the related art when repairing an LCD device in which the desired image of one or more of pixel regions P is not displayed.

[0018] In a first aspect, an array substrate for a liquid crystal display device includes: first and second gate lines on a substrate; a data line crossing the first and second gate lines to define first and second pixel regions, respectively; a first thin film transistor connected to the first gate line and the data line; first and second pixel electrodes in the first and second pixel regions, respectively, the first pixel electrode connected to the first thin film transistor; and a first repair pattern crossing over the first gate line, the first repair pattern electrically connected to one of the first thin film transistor and the second pixel electrode.

[0019] In a second aspect, an array substrate for a liquid crystal display (LCD) device includes: first and second gate lines crossing a data line on a substrate to define first and second pixel regions; a thin film transistor (TFT) including a source electrode that extends from the data line, a drain electrode spaced apart from the source electrode, a semiconductor layer on an insulating layer positioned between the gate electrode and the source and drain electrodes; a metal pattern on the semiconductor layer that overlaps a common line and makes up a portion of the drain electrode; a passivation layer disposed on the source and drain electrodes and on the metal pattern; a first pixel electrode on the passivation layer and connected to the metal pattern; a common electrode on the passivation layer and connected to the common line; and a repair pattern on the semiconductor layer connected to the drain electrode at one end thereof and overlapping under a second pixel electrode of the second pixel region at another end thereof to define a repairing portion.

[0020] In a third aspect, an array substrate for a liquid crystal display (LCD) device includes: first and second gate lines crossing a data line on a substrate to define first and second pixel regions; a thin film transistor (TFT) including a source electrode that extends from the data line, a drain electrode spaced apart from the source electrode, a semiconductor layer on an insulating layer positioned between the gate electrode and the source and drain electrodes; a first metal pattern on the semiconductor layer that extends from the drain electrode and overlaps a common line; a second metal pattern that extends from the first metal pattern towards the second pixel region; a passivation layer disposed on the source and drain electrodes and on the first and second metal patterns; a common electrode on the passivation layer and connected to the common line; a first pixel electrode on the passivation layer and connected to the first metal pattern; and a repair pattern on the passivation layer that extends from a second pixel electrode of the second pixel region at one end thereof and overlaps the second metal pattern at another end thereof to define a repairing portion.

[0021] In a fourth aspect, an array substrate for a liquid crystal display (LCD) device includes: first and second gate lines crossing a data line on a substrate to define first and second pixel regions; a thin film transistor (TFT) including a source electrode that extends from the data line, a drain electrode spaced apart from the source electrode, a semiconductor layer on an insulating layer positioned between the gate electrode and the source and drain electrodes; a metal pattern on the semiconductor layer that overlaps a common line and makes up a portion of the drain electrode; a passivation layer disposed on the source and drain electrodes and on the metal pattern; a common electrode on the passivation layer and connected to the common line; a first pixel electrode on the passivation layer and connected to the metal pattern, wherein the first pixel electrode includes a protrusion that extends towards the second pixel region; a first repair pattern on the passivation layer that extends from a second pixel electrode of the second pixel region; and a second repair pattern on the semiconductor layer that overlaps under the protrusion at one end thereof to define a first repairing portion and overlaps under the first repair pattern at the other end thereof to define a second repairing portion.

[0022] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the disclosure as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings, which are included to provide a further understanding of the disclosure, and are incorporated in and constitute a part of this specification, illustrate embodiments of the disclosure and together with the description serve to explain the principles thereof.

[0024] FIG. **1** is an exploded perspective view of a conventional liquid crystal panel of an LCD device.

[0025] FIG. **2** is a plane view showing an array substrate for an LCD device according to the related art.

[0026] FIG. **3** is a plane view showing an array substrate for an in-plane switching mode liquid crystal device (IPS-LCD) according to a first embodiment of the present disclosure.

[0027] FIG. **4** is a cross-sectional view taken along the line IV-IV of FIG. **3**.

[0028] FIG. **5** is a cross-sectional view taken along the line V-V of FIG. **3**.

[0029] FIG. **6** is a plane view showing an array substrate for an IPS-LCD device according to a second embodiment of the present disclosure.

[0030] FIG. **7** is a cross-sectional view taken along the line VII-VII of FIG. **6**.

[0031] FIG. **8** is a plane view showing an array substrate for an IPS-LCD device according to a third embodiment of the present disclosure.

[0032] FIG. **9** is a cross-sectional view taken along the line IX-IX of FIG. **8**.

DETAILED DESCRIPTION OF THE DRAWINGS AND THE PRESENTLY PREFERRED EMBODIMENTS

[0033] An array substrate for an LCD device has a repair pattern. When defects are generated in a pixel region, a pixel

electrode in the pixel region can be electrically connected to another pixel electrode in another pixel region by the repair pattern. Although the disclosure teaches with respect to an array substrate for an in-plane switching mode liquid crystal device (IPS-LCD) where a pixel electrode and a common electrode are formed in the same substrate so as to have a wide viewing angle, the present disclosure can be equally applied to an array substrate for a twisted nematic (TN) mode LCD device (TN-LCD).

[0034] FIG. **3** is a plane view showing an array substrate **101** for an IPS-LCD device according to a first embodiment of the present disclosure. FIG. **4** is a cross-sectional view taken along the line IV-IV of FIG. **3**. FIG. **5** is a cross-sectional view taken along the line V-V of FIG. **3**. FIGS. **3** through **5** will jointly be referred to for the following discussion.

[0035] A plurality of pixel regions P are defined in the substrate **101**. Because each of the plurality of pixel regions P has the same structure, two adjacent pixel regions will be illustrated for discussion. The array substrate **101** includes a first gate line **104** and a data line **125** formed thereon. Although not shown in FIG. **3**, a second gate line is formed on the substrate **101** to be parallel to and spaced apart from the first gate line **104**. The first gate line **104** and the second gate line cross the data line **125** to define first and second pixel regions P**1** and P**2**, respectively. The first and second pixel regions P**1** and P**2**, which have the same structure, constitute a plurality of pixel regions P of the substrate **101**. A common line **110**, which is substantially parallel to and spaced apart from the first gate line **104**, is formed on the substrate **101**.

[0036] First and second common electrode connecting patterns **113***a* and **113***b* respectively extend from both ends of the common line **110** and are formed in the first pixel region P**1**. The first and second common electrode connecting patterns **113***a* and **113***b* are parallel to the data line **125**. Moreover, a third common electrode connecting pattern **113***c* joins the first and second common electrode connecting patterns **113***a* and **113***b* and is formed in the pixel region P. Namely, one end of each of the first and second common electrode connecting patterns **113***a* and **113***b* is connected to the common line **110**, and the other end of each of the first and second common electrode connecting patterns **113***a* and **113***b* are connected to the third common electrode connecting pattern **113***c*. As a result, the common line **110** and the first to third common electrode connecting patterns **113***a* to **113***c* form a square or rectangular shape in the first pixel region P**1**.

[0037] The common line **110** and the third common electrode connecting pattern **113***c* have both wider and narrower portions in FIG. **3**. The common line **110** and the third common electrode connecting pattern **113***c*, however, may have other shapes. The wider portion of the common line **110** is connected to the second common electrode connecting pattern **113***b*, and the narrower portion of the common line **110** is connected to the first common electrode connecting pattern **113***a*. In contrast, the wider portion of the third common electrode connecting pattern **113***c* is connected to the first common electrode connecting pattern **113***a*, and the narrower portion of the third common electrode connecting pattern **113***c* is connected to the second common electrode connecting pattern **113***b*.

[0038] A source electrode **128** extends from the data line **125** and a drain electrode **130** is spaced apart from the source electrode **128**, and overlaps the first gate line **104**. The overlapped portion of the first gate line **104** with the source and drain electrodes **128** and **130** is defined as a gate electrode **107**. A gate insulating layer **115** is formed on the gate electrode **107**, and a semiconductor layer **120** is formed on the gate insulating layer **115**. The source and drain electrodes **128** and **130** are formed on the semiconductor layer **120**. The drain electrode **130** may be parallel to the first gate line **104**. The source electrode **128** may have a "U" shape, and the drain electrode **130** is disposed in the "U" shape. The gate electrode **107**, the gate insulating layer **115**, the semiconductor layer **120**, the source electrode **128**, and the drain electrode **130** constitute a first thin film transistor (TFT) Tr. The first TFT Tr is connected to the first gate line **104** and the data line **125**. Although not shown in FIGS. **3** through **5**, a second TFT in the second pixel region P is connected to the second gate line and the data line **125**.

[0039] A first pixel electrode including first, second, and third pixel patterns **153***a*, **153***b* and **153***c* and a plurality of fourth pixel patterns **155** is formed in the first pixel region P**1**. The first, second and third pixel patterns **153***a*, **153***b* and **153***c* and the plurality of fourth pixel patterns **155** are electrically connected to the first TFT Tr. The first pixel pattern **153***a* combines one end of the plurality of fourth pixel patterns **155**. The second and third pixel patterns **153***b* and **153***c* extend from respective ends of the first pixel pattern **153***a*. The second and third pixel patterns **153***b* and **153***c* have wider and narrower portions in FIG. **3**. However, the second and third pixel patterns **153***b* and **153***c* may have other shapes. The narrower portion of the second pixel pattern **153***b* is adjacent to the first pixel pattern **153***a* than the wider portion of the second pixel patterns **153***b*. In contrast, the wider portion of the third pixel pattern **153***c* is adjacent to the first pixel pattern **153***a* than the narrower portion of the third pixel patterns **153***c*. Namely, the second and third pixel patterns **153***b* and **153***c* have substantially the same shape as the third common electrode connecting pattern **113***c* and the common line **110**, respectively. The plurality of fourth pixel patterns **155**, the second pixel pattern **153***b* and the third pixel pattern **153***c* are substantially parallel to each other and form an angle with respect to the first pixel pattern **153***a*.

[0040] The plurality of fourth pixel patterns **155** are spaced apart from each other. The plurality of fourth pixel patterns **155** may include a transparent conductive material, such as indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

[0041] The third pixel pattern **153***c* is connected to a metal pattern **131**, which makes up a portion of the drain electrode **130**, through a drain contact hole **143**. The metal pattern **131** extends from the drain electrode **130** of the TFT Tr. Signals are applied to the plurality of fourth pixel patterns **155** via the drain electrode **130**, the metal pattern **131**, the third pixel pattern **153***c* and the first pixel pattern **153***a*.

[0042] The metal pattern **131** overlaps the common line **110**. The overlapped portion of the common line **110**, the metal pattern **131** connected to the third pixel pattern **153***c*, and a gate insulating layer **115** interposed therebetween constitute a first storage capacitor Stg**1**. The second common electrode connecting pattern **113***b* overlaps the first pixel pattern **153***a*. The overlapped portion of the second common electrode connecting pattern **113***b*, the overlapped portion of the first pixel pattern **153***a*, and the intervening gate insulating layer **115** and an intervening passivation layer **140** interposed therebetween, constitute a second storage capacitor Stg**2**. Moreover, the third common electrode connecting pattern **113***c* overlaps the second pixel pattern **153***b*. The overlapped portion of the third common electrode connecting pattern

113*c*, the overlapped portion of the second pixel pattern **153***b*, and the intervening gate insulating and passivation layers **115**, **140** interposed therebetween, constitute a third storage capacitor Stg**3**.

[0043] A common electrode, including a first common pattern **156** and a plurality of second common patterns **157**, is formed in the first pixel region P**1**. The first common pattern **156** overlaps the first common electrode connecting pattern **113***a*. The first common pattern **156** is connected to the first common electrode connecting pattern **113***a* through a common contact hole **141** and includes a transparent conductive material, such as ITO and IZO. The plurality of second common patterns **157** extend from the first common pattern **156** and are spaced apart form each other. The plurality of second common patterns **157** are alternately arranged with and parallel to the plurality of fourth pixel patterns **155**. The plurality of second common patterns **157** and the plurality of fourth pixel patterns **155** may be formed of the same layer and the same transparent conductive material. The plurality of second common patterns **157** and the plurality of fourth pixel patterns **155** are formed at angles with respect to the first gate line **104** in FIG. **3**. However, the plurality of second common patterns **157** and the plurality of fourth pixel patterns **155** may be parallel to the first gate line **104** in another embodiment. Alternately, the plurality of second common patterns **157** and the plurality of fourth pixel patterns **155** may be classified into two groups having varying angles to form two domains in the first pixel region P**1**. A viewing angle is improved by a multiple-domain structure.

[0044] Moreover, a repair pattern **132** is formed on the substrate **101**. The plurality of pixel regions includes the first pixel region P**1** and the second pixel region P**2** vertically adjacent to each other. The repair pattern **132** crosses over the first gate line **104** and electrically connects to the drain electrode **130** of the first TFT Tr. Accordingly, the repair pattern **132** extends from the drain electrode **130** in the first pixel region P**1** to a second pixel pattern **183***b* of a second pixel electrode in the second pixel region P**2** to overlap the second pixel pattern **183***b* in the second pixel region P**2**. The repair pattern **132** may be formed of the same layer and the same material as the drain electrode **130**. Because the passivation layer **140** is formed between the repair pattern **132** and the second pixel pattern **183***b* of the second pixel electrode in the second pixel region P**2**, the repair pattern **132** and the second pixel pattern **183***b* of the second pixel electrode are electrically disconnected from each other before repairing. The overlapped portion of the repair pattern **132** and the second pixel pattern **183***b* of the second pixel electrode in the second pixel region P**2** is defined as a repairing portion RP.

[0045] When the first TFT Tr in the first pixel region P**1** does not function due to impurities, the drain electrode **130** is cut along a cutting line CL such that the first pixel electrode, including the first, second, and third pixel patterns **153***a*, **153***b* and **153***c* and the plurality of fourth pixel patterns **155**, is disconnected from the first TFT Tr in the first pixel region P**1**. Next, the repair pattern **132** is connected to the second pixel pattern **183***b* of the second pixel electrode in the second pixel region P**2** by a repairing method. For example, laser beam may be irradiated into a repairing portion RP to connect the repair pattern **132** and the second pixel pattern **183***b* of the second pixel electrode in the second pixel region P**2**.

[0046] As a result, the first pixel electrode in the first pixel region P**1** is electrically connected to the second TFT (not shown) in the second pixel region P**2** through the second pixel electrode in the second pixel region P**2**, the repair pattern **132** and the drain electrode **130** in the first pixel region P**1**. Signals applied to the second pixel electrode in the second pixel region P**2** can be applied to the first pixel electrode in the first pixel region P**1** such that images displayed in the first pixel region P**1** has the same gray level as images displayed in the second pixel region P**2**. Accordingly, the above-mentioned problems in the related art can be overcome.

[0047] With further reference to FIGS. **4** and **5**, a region where the first TFT Tr is formed is defined as a switching region TrA. The first gate line **104** is formed on the substrate **101**; the gate electrode **107** is connected to the first gate line **104** as formed in the switching region TrA of the first pixel region P**1**. The common line **110** is spaced apart from the first gate line **104** and is formed in the first pixel region P**1** on the substrate **101**. FIG. **5** shows the third common electrode connecting pattern **113***c* formed in the second pixel region P**2**. In the second pixel region P**2**, the third common electrode connecting pattern **113***c* is connected to the common line through the first and second common electrode connecting patterns (structures not shown). The first and second common electrode connecting patterns may be formed of the same layer and the same material as the third common electrode connecting pattern **113***c* in the second pixel region P**2**.

[0048] The gate insulating layer **115** is formed on the substrate **101** including the first gate line **104**, the gate electrode **107**, the common line **110**, and the third common electrode connecting patterns **113***c* of the second pixel region P**2**. The gate insulating layer **115** may include an inorganic insulating material. The semiconductor layer **120**, including an active layer **120***a* of intrinsic amorphous silicon and an ohmic contact layer **120***b* of impurity-doped amorphous silicon, is formed on the gate insulating layer **115**. The ohmic contact layer **120***b* is formed on the active layer **120***a*. The source and drain electrodes **128** and **130** are formed on the semiconductor layer **120** in a spaced-apart relationship. Moreover, the repair pattern **132** is formed on the gate insulating layer **115**. The repair pattern **132** crosses over the first gate line **104** and is electrically connected to the drain electrode **130**. Accordingly, the repair pattern **132** extends from the drain electrode **130** in the first pixel region P**1** to the second pixel region P**2**. The repair pattern **132** may be formed of the same layer and the same material as the drain electrode **130**. The data line **125** (of FIG. **3**) crosses the first gate line **104** and the second gate line (not shown) such that the first and second pixel regions P**1** and P**2** are defined. The data line **125** (of FIG. **3**) is connected to the source electrode **128**.

[0049] The metal pattern **131** extending from the drain electrode **130** is formed on the gate insulating layer **115** and overlaps the common line **110**. As mentioned above, the overlapped portion of the common line **110** as a first electrode, the metal pattern **131** as a second electrode, and the gate insulating layer **115** therebetween as a dielectric material, constitute the first storage capacitor Stg**1**.

[0050] The semiconductor layer **120** is disposed under and has substantially the same shape as the data line **125** (of FIG. **3**), the repair pattern **132**, and the metal pattern **131**. This is because the semiconductor layer **120**, the data line **125** (of FIG. **3**), the repair pattern **132**, and the metal pattern **131** are patterned at the same time using a single mask process. If the semiconductor layer **120** is patterned by a different mask process than that of the data line **125**, then the repair pattern

132, the metal pattern **131**, and the semiconductor layer **120** would not lie under the data line **125**, the repair pattern **132**, and the metal pattern **131**.

[0051] The passivation layer **140** is formed on the source electrode **128**, the drain electrode **130**, the repair pattern **132**, and the metal pattern **131**. The passivation layer **140** is patterned to form the drain contact hole **143** and the common contact hole **141** (of FIG. **3**). The drain contact hole **143** and the common contact hole **141** respectively expose the metal pattern **131** and the first common electrode connecting pattern **113***a* (of FIG. **3**).

[0052] The second pixel pattern **153***b*, the third pixel pattern **153***c*, the plurality of fourth pixel patterns **155**, and the plurality of second common patterns **157** are formed of a transparent conductive material on the passivation layer **140**. Moreover, the first pixel pattern **153***a* (of FIG. **3**) and the first common pattern **156** (of FIG. **3**) are formed on the passivation layer **140**.

[0053] The first pixel pattern **153***a* overlaps the second common electrode connecting pattern **113***b*, and the second and third pixel patterns **153***b* and **153***c* extend from respective ends of the first pixel pattern **153***a*. The second and third pixel patterns **153***b* and **153***c* overlap the third common electrode connecting pattern **113***c* and the common line **110**, respectively. Moreover, the second pixel pattern **183***b* of the second pixel electrode in the second pixel region P**2** overlaps the repair pattern **132** extending from the drain electrode **130** in the first pixel region P**1**. The plurality of fourth pixel patterns **155** extend from the first pixel pattern **153***a*. The second pixel pattern **153***b* and the third pixel pattern **153***c*, and the plurality of fourth pixel patterns **155** are substantially parallel to the each other and angled toward the first pixel pattern **153***a*. The third pixel pattern **153***c* is connected to the metal pattern **131** through the drain contact hole **143**.

[0054] The first common pattern **156** (of FIG. **3**) is connected to the first common connecting pattern **113***a* through the common contact hole **141** and also overlaps the first common connecting pattern **113***a*. The plurality of second common patterns **157** extend from and are angled toward the first common pattern **156**. The plurality of second common patterns **157** are alternately arranged with, and parallel to, the plurality of fourth pixel patterns **155**.

[0055] When the first TFT Tr in the first pixel region P**1** does not function, the plurality of fourth pixel patterns **155** in the first pixel region P**1** are electrically disconnected from the first TFT Tr in the first pixel region P**1** and are electrically connected to the second TFT in the second pixel region P**2** by repairing. Namely, the drain electrode **130** of the first TFT Tr in the first pixel region P**1** is cut along the cutting line CL, and a laser beam may be irradiated into the repairing portion RP such that the repair pattern **132** is connected to the second pixel pattern **183***b* of the second pixel electrode in the second pixel region P**2**. As a result, the first pixel electrode in the first pixel region P**1** receives the same signals as the second pixel electrode in the second pixel electrode P**2**.

[0056] FIG. **6** is a plane view showing an array substrate for an IPS-LCD device according to a second embodiment of the present disclosure. In the second embodiment, the drain electrode is parallel to the data line. Similar elements as the elements explained in FIGS. **3** to **5** are not explained.

[0057] As shown in FIG. **6**, the first gate line **204** and the second gate line (not shown) cross the data line **225** to define the first and second pixel regions P**1** and P**2**, respectively. The source electrode **228** extends from the data line **225** and has a "U" shape. The drain electrode **230** in the first pixel region P**1** is parallel to the data line **225** and disposed within the "U" shape source electrode **228**. The source and drain electrodes **228** and **230** overlap the gate line **204**. The overlapped portion of the gate line **204** is defined as the gate electrode **207**. A first metal pattern **231** in the first pixel region P**1** extends from the drain electrode **230**, and a second metal pattern **233** extends from the first metal pattern **231** to be parallel to the drain electrode **230**. The first and second metal patterns **231** and **233** make up portions of the drain electrode **230** of the first TFT Tr. A repair pattern **254** is formed on a passivation layer (not shown). A repair pattern **254** may cross over the first gate line **204** and is electrically connected to a second pixel pattern **283***b* of a second pixel electrode in the second pixel region P**2**. One of skill in the art will appreciate that the repair pattern **254** may stop short of crossing the first gate line **204**, and that the second metal pattern **233** may extend to cross over the first gate line **204** to overlap with the repair pattern **254**.

[0058] In sum, the repair pattern **254** extends from the second pixel pattern **283***b* in the second pixel region P**2** to the first pixel region P**1** and overlaps the second metal pattern **233** that makes up a portion of the drain electrode **230** in the first pixel region P**1**. The repairing portion RP is disposed in the overlapped portion of the repair pattern **254** and the second metal pattern **233**.

[0059] FIG. **7** is a cross-sectional view taken along the line VII-VII of FIG. **6**. As shown in FIG. **7**, the first gate line **204**, a common line **210** and a third common electrode connecting pattern **213***c* are formed on the substrate **201**. A gate insulating layer **215** is formed on the first gate line **204**, the common line **210**, and the third common electrode connecting pattern **213***c*. A semiconductor layer **220**, including an active layer **220***a* and an ohmic contact layer **220***b*, is formed on the gate insulating layer **215**. The first metal pattern **231** extending from the drain electrode **230** (of FIG. **6**) is disposed on the semiconductor layer **220** and overlaps the common line **210**. The overlapped portion of the common line **210**, the first metal pattern **231**, and the gate insulating layer **215** therebetween constitute the first storage capacitor Stg**1**. The second metal pattern **233** that extends from the first metal pattern **231** is formed on the gate insulating layer **215**. A passivation layer **240** is formed on the first and second metal patterns **231** and **233**. A plurality of fourth pixel patterns **255**, a plurality of second common patterns **257**, the second pixel pattern **283***b* of the second electrode, and the repair pattern **254** are formed on the passivation layer **240**.

[0060] In FIG. **7**, the plurality of fourth pixel patterns **255** and the plurality of second common patterns **257** are formed in the first pixel region P**1**. In the second pixel region P**2**, the second pixel pattern **283***b* of the second pixel electrode overlaps the third common electrode connecting pattern **213***c* in the second pixel region P**2**. The overlapped third common electrode connecting pattern **213***c*, the second pixel pattern **283***b* of the second pixel electrode, and the gate insulating and passivation layers **215** and **240** interposed therebetween, constitute the third storage capacitor Stg**3**. The repair pattern **254** extends from the second pixel pattern **283***b* of the second pixel electrode in the second pixel region P**2** into the first pixel region P**1** to overlap the second metal pattern **233** that makes up a portion of the drain electrode **230**. Because the passivation layer **240** is interposed between the repair pattern **254** and the second metal pattern **233**, the repair pattern **254** and the second metal pattern **233** are not electrically connected to each other before repairing.

[0061] When the first TFT Tr in the first pixel region P**1** does not function, the drain electrode **230** in the first pixel region P**1** is cut along the cutting line CL to disconnect the first pixel electrode in the first pixel region P**1** from the first TFT Tr in the first pixel region P**1**. And then, the repair pattern **254** and the second metal pattern **233** are connected by irradiating a laser beam into the repairing portion RP to connect the first pixel electrode in the first pixel region P**1** to the second pixel electrode in the second pixel region P**2**. Pixel regions P**1** and P**2** are connected through connecting together the second pixel pattern **283***b* in the second pixel region P**2**, the repair pattern **254**, and the drain electrode **230** in the first pixel region P**1**. As a result, signals applied to the second pixel electrodes in the second pixel region P**2** are applied to the first pixel electrode in the first pixel region P**1**. And images displayed in the first pixel region P**1** have the same gray level as the images displayed in the second pixel region P**2**.

[0062] FIG. **8** is a plane view showing an array substrate for an IPS-LCD device according to a third embodiment of the present disclosure, and FIG. **9** is a cross-sectional view taken along the line IX-IX of FIG. **8**. Elements in the third embodiment except for a repair pattern are substantially the same as those in the second embodiment such that the same elements are not explained.

[0063] Over a substrate **301**, a first gate line **304** and the second gate line (not shown) crosses a data line **325** to define first and second pixel regions P**1** and P**2**, respectively. A common line **310** is spaced apart from the first gate line **304**. A source electrode **328** extends from the data line **325** and may have a "U" shape. A drain electrode **330** is disposed within the "U" shape source electrode **328**, yet spaced apart from the source electrode **328**. The drain electrode **330** is substantially parallel to a data line **325**.

[0064] A metal pattern **331**, which makes up a portion of the drain electrode **330**, extends from the drain electrode **330** and overlaps a common line **310**. First and second repair patterns **354** and **333** are formed over the substrate **301**. The first pixel electrode in the first pixel region P**1** includes a protruding portion **352**. The protruding portion **352** extends from a third pixel pattern **353***c* in the first pixel region P**1** and overlaps one end of the second repair pattern **333**. The first repair pattern **354** crosses over the first gate line **304** and electrically connects to a second pixel pattern **383***b* of a second pixel electrode in the second pixel region P**2**. Accordingly, the first repair pattern **354** extends from the second pixel pattern **383***b* of the second pixel electrode in the second pixel region P**2** to the first pixel region P**1** and overlaps the other end of the second repair pattern **333**.

[0065] The second repair pattern **333** may be disposed between the first gate line **304** and the common line **310** in the first pixel region P**1**. One of skill in the art will appreciate that the second repair pattern **33** may be disposed between the second pixel pattern **383***b* and the first gate line **304**, wherein the first repair pattern **354** does not cross the first gate line **304**. The second repair pattern **333** is formed of the same layer and the same material as the drain electrode **330** and the metal pattern **331**. However, the second repair pattern **333** is separated from the drain electrode **330** and the metal pattern **331** and has an island shape.

[0066] The second repair pattern **333** is formed on a gate insulating layer **315** and disposed between the first gate line **304** and the common line **310**. A passivation layer **340** is formed on the second repair pattern **333**. The protruding portion **352** is formed on the passivation layer **340** and extends from the third pixel pattern **353***c* in the first pixel region P**1** to overlap one end of the second repair pattern **333**. The first repair pattern **354** is formed on the passivation layer **340** and extends from the second pixel pattern **383***b* of the second pixel electrode in the second pixel region P**2** to overlap the other end of the second repair pattern **333**. The overlapped portion of the protruding portion **352** and the second repair pattern **333** is defined as a first repairing portion RP**1**, and the overlapped portion of the first repair pattern **354** and the second repair pattern **333** is defined as a second repairing portion RP**2**. Since the passivation layer **340** is interposed between the second repair pattern **333** and the protruding portion **352** and between the second repair pattern **333** and the first repair pattern **354**, the protruding portion **352** of the first pixel electrode and the first repair pattern **354** are electrically disconnected from the second repair pattern **333**.

[0067] When the first TFT Tr in the first pixel region P**1** does not function, the drain electrode **330** in the first pixel region P**1** is cut along the cutting line CL to disconnect the first pixel electrode in the first pixel region P**1** from the first TFT Tr in the first pixel region P**1**. And then, the protruding portion **352** of the first pixel electrode in the first pixel region P**1** and the second repair pattern **333** are electrically connected by irradiating a laser beam into the first repairing portion RP**1**, and the first and second repair patterns **354** and **333** are electrically connected by irradiating a laser beam into the second repairing portion RP**2**. Accordingly, the protruding portion **352** of the first pixel electrode in the first pixel region P**1** and the first repair pattern **354** are electrically connected to each other via the second repair pattern **333**. As a result, the second pixel electrode in the first pixel region P**1** is connected to the second pixel electrode in the second pixel region P**2** through the first repair pattern **354**, the second repair pattern **333**, and the protruding portion **352**. Accordingly, the first pixel electrode in the first pixel region P**1** begins to receive the same signals as the second pixel electrode in the second pixel region P**2** after repair.

[0068] A method of fabricating an array substrate for an IPS-LCD device according to the first embodiment is briefly explained. First, a first metallic material layer is formed on the substrate. Then, the first metallic material layer is patterned using a mask process to form the first and second gate lines, the gate electrode, the common line and the first to third common electrode connecting patterns. The mask process includes a step of forming a photoresist (PR) layer, a step of exposing the PR layer using a mask, a step of developing the PR layer to form PR patterns, and a step of removing the first metallic layer exposed between the PR patterns. As mentioned above, the common line is spaced apart from the first gate line. The first and second common electrode connecting patterns extend from respective ends of the common line. The third common electrode connecting pattern combines the first and second common electrode connecting patterns. Namely, the common line and the first to third common electrode connecting patterns form a square or rectangular shape.

[0069] Next, the gate insulating layer is formed on the first and second gate lines, the gate electrode, the common line and the first to third common electrode connecting patterns by depositing an inorganic insulating material, such as silicon oxide and silicon nitride.

[0070] Next, an amorphous silicon layer, an impurity-doped amorphous silicon layer and a second metallic material layer are sequentially formed on the gate insulating layer. The amorphous silicon layer, the impurity-doped amorphous sili-

con layer and the second metallic material layer may be patterned using one of a diffractive mask process or a half-tone mask process to form the data line, the source electrode, the drain electrode, the active layer and the ohmic contact layer. The data line crosses the first and second gate lines to define the first and second pixel regions. The source electrode extends from the data line and is spaced apart from the drain electrode. The source and drain electrodes overlap the gate electrode. The drain electrode is parallel to the first gate line. The semiconductor layer, including the active layer and the ohmic contact layer, is disposed under the source electrode, the drain electrode, and the data line.

[0071] At the same time, the repair pattern crosses the first gate line and is electrically connected to the drain electrode of the first thin film transistor. The repair pattern extends from the drain electrode in the first pixel region into the second pixel region to overlap the third common electrode connecting pattern of the second pixel electrode. Moreover, the metal pattern that makes up a portion of the drain electrode extends from the drain electrode in the first pixel region and overlaps the common line. The repair pattern and the metal pattern may oppositely extend.

[0072] Next, the passivation layer is formed on the data line, the source and drain electrodes, the repair pattern and the metal pattern. The passivation layer is patterned to form the drain contact hole and the common contact hole. The drain contact hole and the common contact hole respectively expose the metal pattern and the first common electrode connecting pattern.

[0073] Next, a transparent conductive material layer is formed on the passivation layer. The transparent conductive material layer is patterned to form the first to third pixel patterns, the plurality of fourth pixel patterns, the first common pattern and the plurality of second common patterns. The first pixel pattern overlaps the second common electrode pattern such that the first pixel pattern is substantially parallel to the data line. The second pixel pattern extends from one end of the first pixel pattern and overlaps the third common connecting pattern and the repair pattern. The third pixel pattern extends from the other of the one end of the first pixel pattern and overlaps the metal pattern to be connected to the metal pattern through the drain contact hole. The plurality of fourth pixel patterns extend from the first pixel pattern and are substantially parallel to the second and third pixel patterns. The first common pattern overlaps the first common connecting pattern to be connected to the first common connecting pattern through the common contact hole. The plurality of fourth pixel patterns are disposed between the second and third pixel patterns. The plurality of second common patterns extend from the first common pattern and are alternately arranged with the plurality of fourth pixel patterns.

[0074] In the second embodiment, the drain electrode is parallel to the data line instead of the first gate line. Moreover, the second metal pattern extends from the first metal pattern, and the repair pattern extends form the second pixel pattern to overlap the second metal pattern. In the third embodiment, the second repair pattern is disposed between the common line and the first gate line. The second repair pattern is formed of the same layer and the same material as the drain electrode and the metal pattern. However, the second repair pattern has an island shape and is electrically disconnected from both the drain electrode and the metal pattern. The first repair pattern extends from the third pixel pattern to overlap one end of the second repair pattern. The protruding portion of the second pixel electrode extends from the second pixel pattern to overlap the other end of the second repair pattern.

[0075] When the TFT in one pixel region is broken or non-functional, the pixel electrode connected to the broken TFT is capable of being connected to the available adjacent TFT. Accordingly, display quality of the LCD device is improved.

[0076] It will be apparent to those skilled in the art that various modifications and variations can be made in the organic electroluminescent device and fabricating method thereof of the present disclosure without departing from the spirit or scope of the disclosure. Thus, it is intended that the present disclosure cover the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents.

1. An array substrate for a liquid crystal display device, comprising:

first and second gate lines on a substrate;

a data line crossing the first and second gate lines to define first and second pixel regions, respectively;

a first thin film transistor connected to the first gate line and the data line;

first and second pixel electrodes in the first and second pixel regions, respectively, the first pixel electrode connected to the first thin film transistor; and

a first repair pattern crossing over the first gate line, the first repair pattern electrically connected to one of the first thin film transistor and the second pixel electrode.

2. The substrate according to claim **1**, wherein the first thin film transistor includes a gate electrode, a semiconductor layer, a source electrode and a drain electrode, and the first pixel electrode is connected to the drain electrode.

3. The substrate according to claim **2**, wherein the first repair pattern is electrically connected to the drain electrode and overlaps the second pixel electrode.

4. The substrate according to claim **3**, wherein the first repair pattern is formed of the same layer and the same material as the drain electrode.

5. The substrate according to claim **2**, wherein the first repair pattern is electrically connected to the second pixel electrode and overlaps the drain electrode.

6. The substrate according to claim **5**, wherein the first repair pattern is formed of the same layer and the same material as the second pixel electrode.

7. The substrate according to claim **2**, further comprising a second repair pattern overlapping the first repair pattern and the first pixel electrode.

8. The substrate according to claim **7**, wherein the first repair pattern is electrically connected to the second pixel electrode.

9. The substrate according to claim **8**, wherein the first repair pattern is formed of the same layer and the same material as the second pixel electrode.

10. The substrate according to claim **7**, wherein the second repair pattern has an island shape in the first pixel region.

11. The substrate according to claim **10**, wherein the second repair pattern is formed of the same material and the same material as the drain electrode.

12. The substrate according to claim **1**, wherein each of the first and second pixel electrode includes first to third pixel patterns and a plurality of fourth pixel patterns, the first pixel pattern combining the plurality of fourth pixel patterns, the second and third pixel patterns extending from respective

ends of the first pixel pattern, the plurality of fourth pixel patterns spaced apart from each other.

13. The substrate according to claim **12**, further comprising:

a common line and first to third common electrode connecting patterns in the first pixel, the common line parallel to and spaced apart from the first gate line, the first and second common electrode connecting patterns extending from both ends of the common line, the third common electrode connecting pattern combining the first and second common electrode connecting patterns; and

a common electrode in the first pixel region, the common electrode including a first common pattern and a plurality of second common patterns extending from the first common pattern,

wherein the plurality of second common patterns are alternately arranged with the plurality of fourth pixel patterns.

14. The substrate according to claim **13**, wherein the common electrode is connected to the first common electrode connecting pattern.

15. The substrate according to claim **13**, further comprising:

a gate insulating layer on the common line;

a metal pattern on the gate insulating layer, the metal pattern overlapping the common line; and

a passivation layer on the metal pattern,

wherein the third pixel pattern is connected to the metal pattern, and the common line, the metal pattern constitute a first storage capacitor with the gate insulating layer therebetween.

16. The substrate according to claim **15**, wherein the gate insulating layer and the passivation layer are disposed between the second common electrode connecting pattern and the first pixel pattern, and wherein the second common electrode connecting pattern and the first pixel pattern constitute a second storage capacitor with the gate insulating layer and the passivation layer interposed therebetween.

17. The substrate according to claim **16**, wherein the gate insulating layer and the passivation layer are disposed between the third common electrode connecting pattern and the second pixel pattern, and wherein the third common electrode connecting pattern and the second pixel pattern constitute a third storage capacitor with the gate insulating layer and the passivation layer interposed therebetween.

* * * * *

专利名称(译)	用于液晶显示装置的阵列基板及其制造方法		
公开(公告)号	US20100289978A1	公开(公告)日	2010-11-18
申请号	US12/845573	申请日	2010-07-28
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	CHOI IL MAN KIM TAE HYEUNG LEE MIN JIC		
发明人	CHOI, IL-MAN KIM, TAE-HYEUNG LEE, MIN-JIC		
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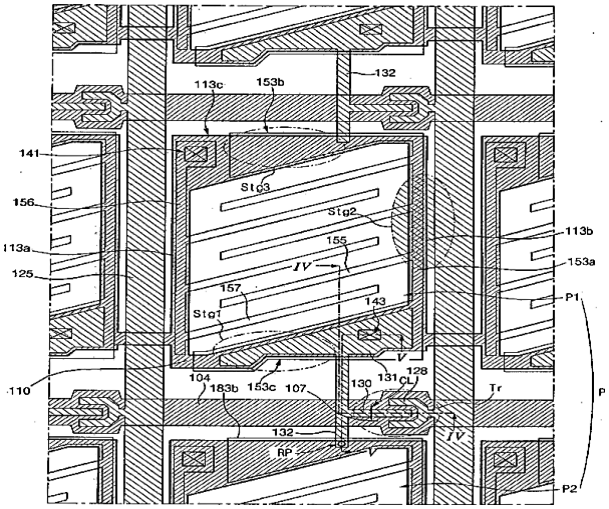
摘要(译)

用于液晶显示（LCD）器件的阵列基板形成在基板上，第一和第二栅极线与数据线交叉以限定第一和第二像素区域。薄膜晶体管包括源电极和漏电极。金属图案与公共线重叠并构成漏电极的一部分。钝化层设置在源极和漏极上以及金属图案上。第一像素电极连接到金属图案，公共电极连接到公共线。形成各种修复图案以限定一个或多个修复部分，如果在第一像素电极未能显示图像的情况下切割切割线，则能够将漏电极或金属图案连接到第二像素区域的第二像素电极。