US 20090295703A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2009/0295703 A1**

(43) **Pub. Date: Dec. 3, 2009**

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(54) **LIQUID CRYSTAL DISPLAY PANEL AND DRIVING METHOD THEREOF**

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(21) Appl. No.: **12/407,972**

(22) Filed: **Mar. 20, 2009**

(30) **Foreign Application Priority Data**

May 30, 2008 (TW) 97120266

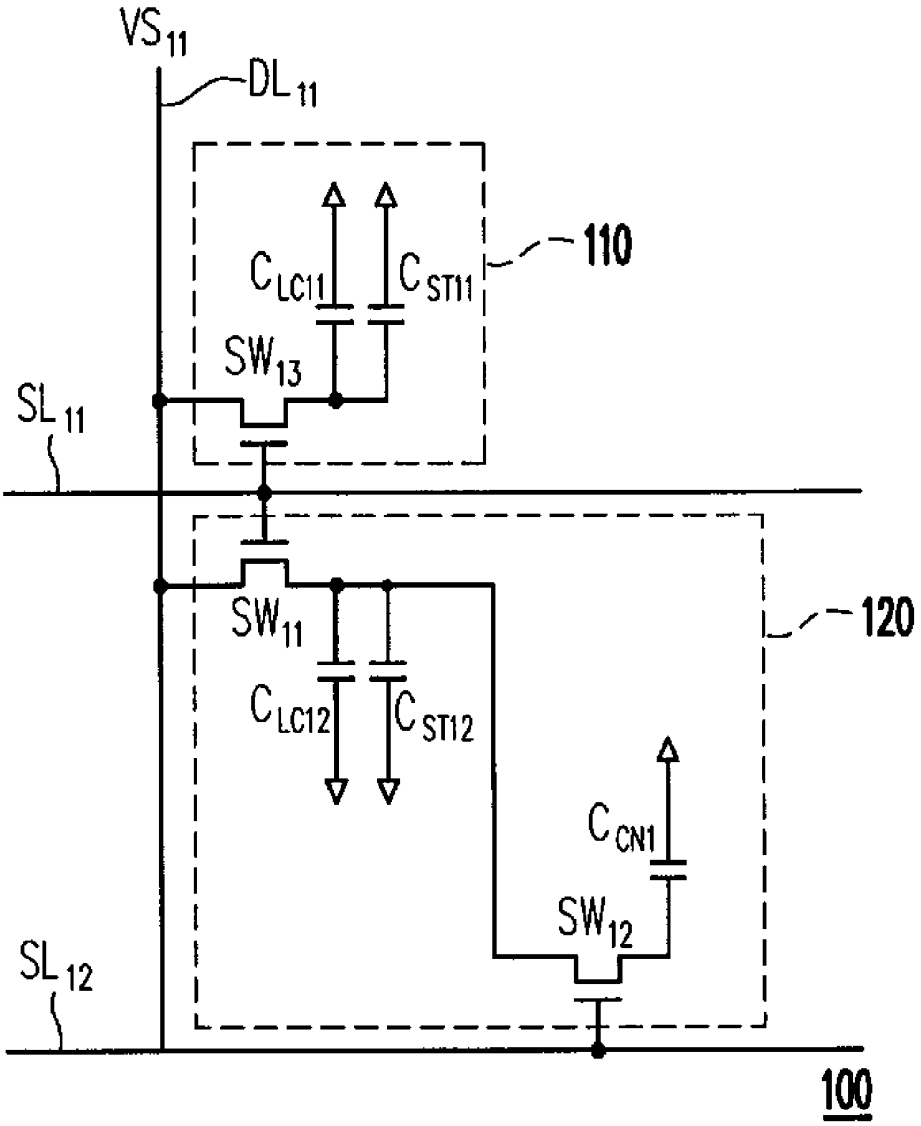
Publication Classification

(51) **Int. Cl.**
G09G 3/36 (2006.01)

(52) **U.S. Cl.** **345/94**; 345/98

(57) **ABSTRACT**

A liquid crystal display panel includes a plurality of pixels and each of the pixels includes a first sub-pixel and a second sub-pixel. The first sub-pixel and the second sub-pixel individually load a source voltage according to a first gate pulse and a second gate pulse, respectively. The second sub-pixel includes a first storage capacitor and a first compensation capacitor. The first compensation capacitor charges or discharges to a predetermined voltage before performing charge neutralization with the first storage capacitor according to a second gate pulse.



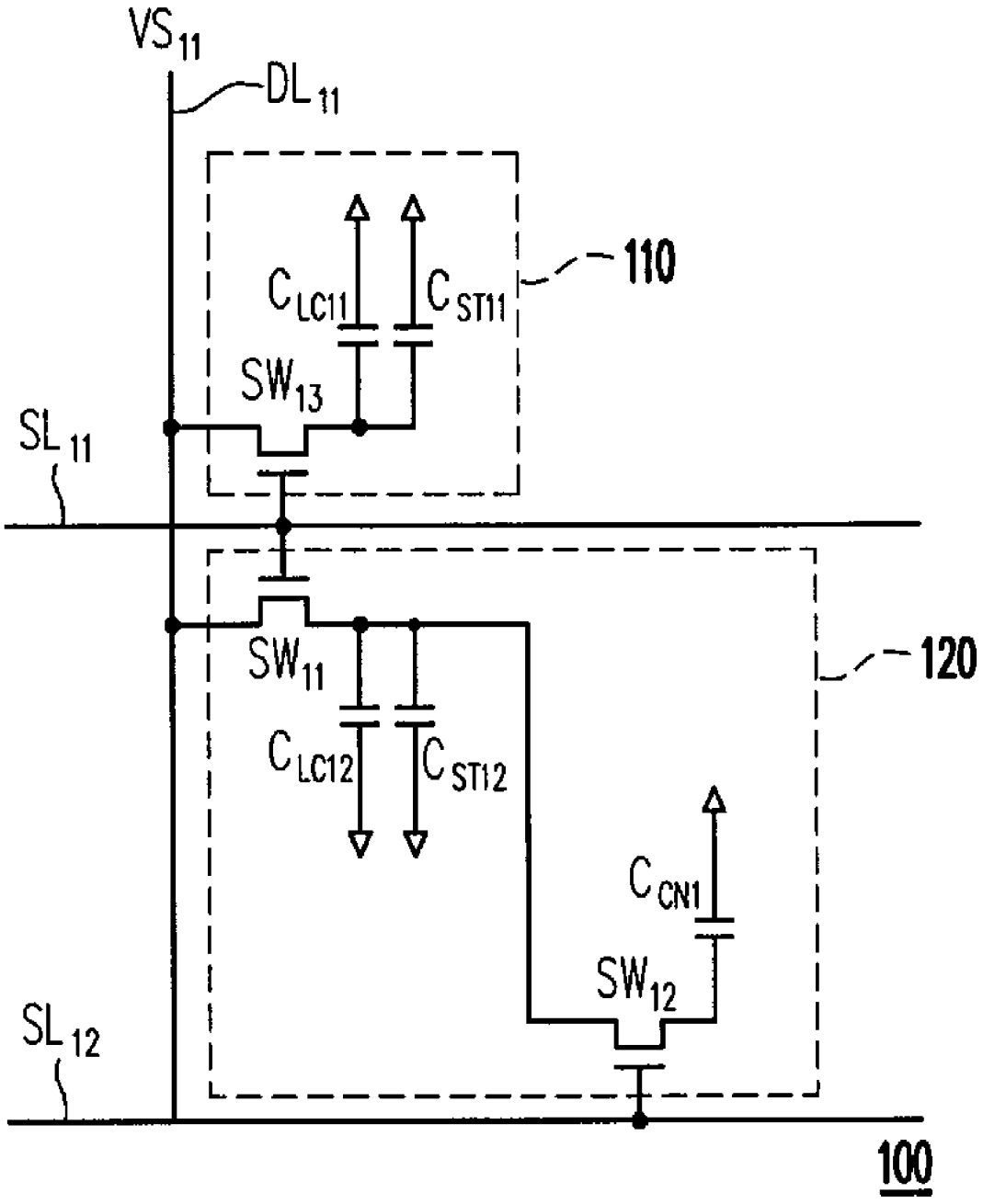

VS11
DL11
110
CLC11
CST11
SW13
SL11
120
SW11
CLC12
CST12
CCN1
SW12
SL12
100

FIG. 1

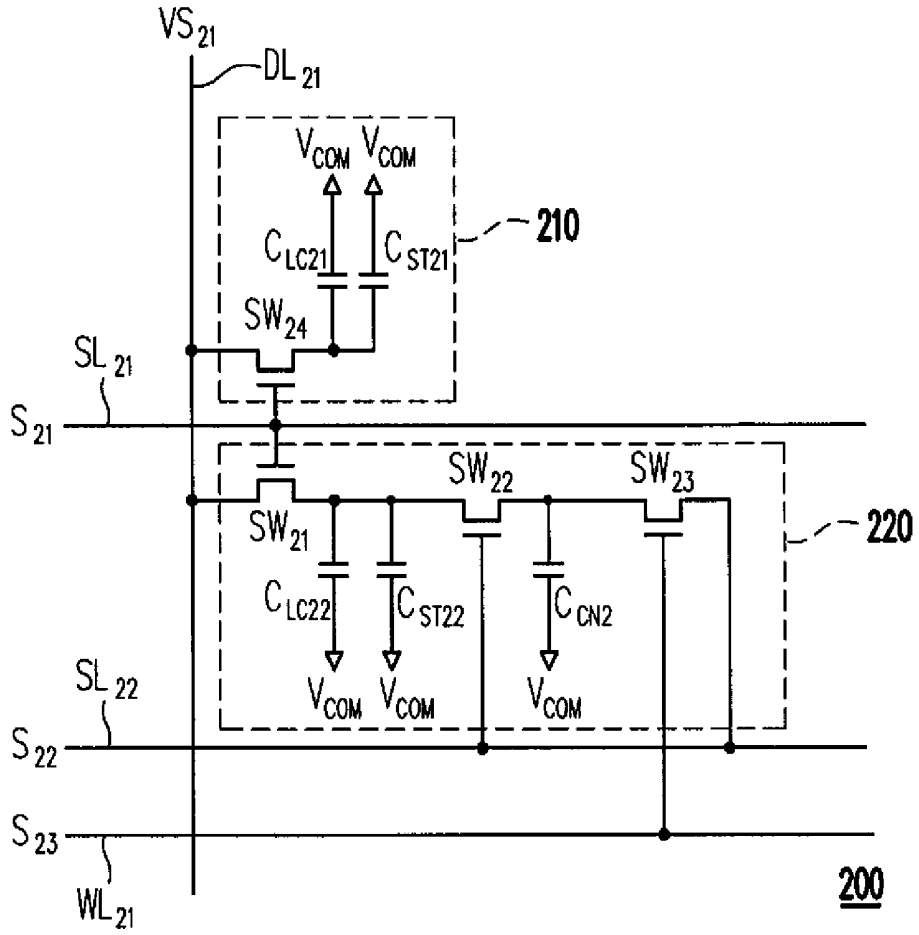

VS21
DL21
VCOM VCOM
210
CLC21
CST21
SW24
SL21
S21
SW22
SW23
220
SW21
CLC22
CST22
CCN2
VCOM VCOM VCOM
SL22
S22
S23
WL21
200

FIG. 2A

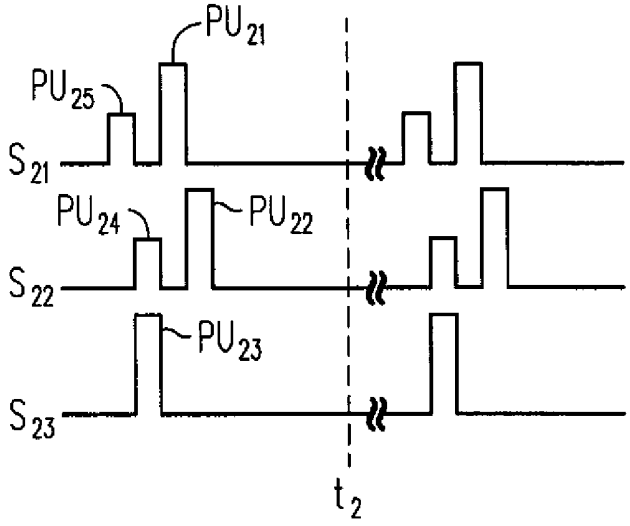

PU21
PU25
S21
PU24
PU22
S22
PU23
S23
t2

FIG. 2B

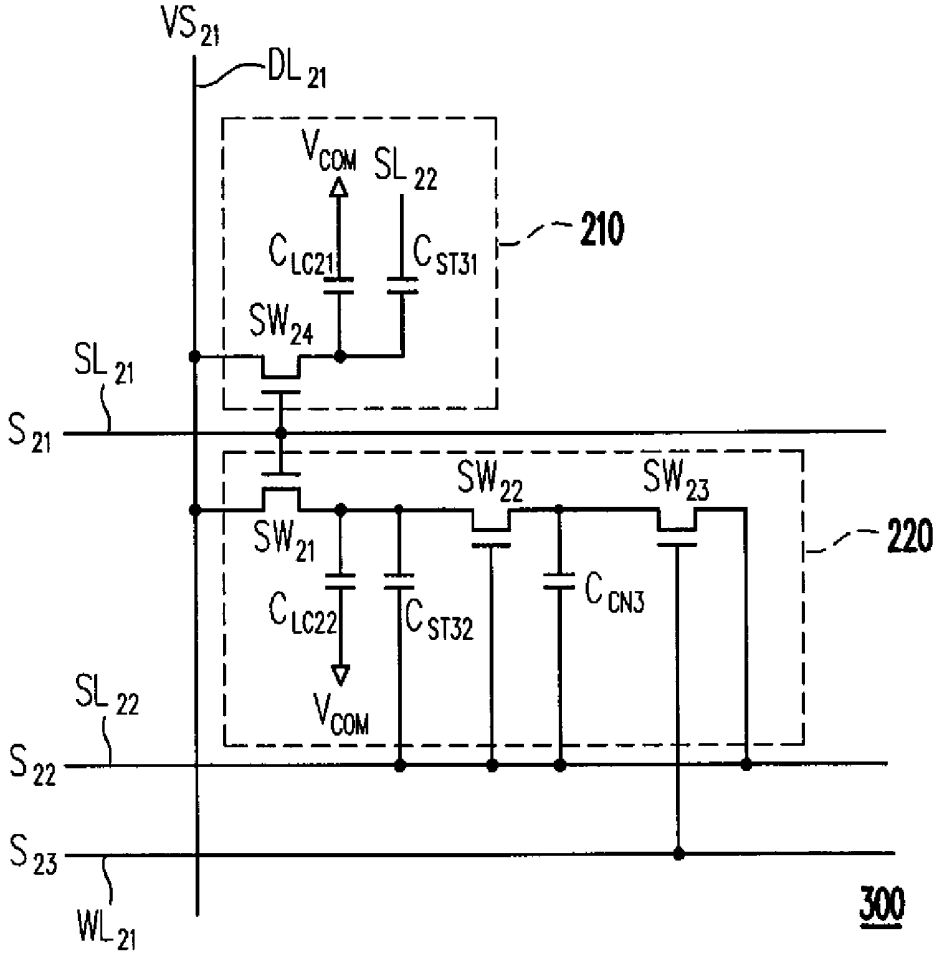

VS21
DL21
VCOM
SL22
CLC21
CST31
210
SW24
SL21
S21
SW22
SW23
SW21
220
CLC22
CST32
CCN3
VCOM
SL22
S22
S23
WL21
300

FIG. 3A

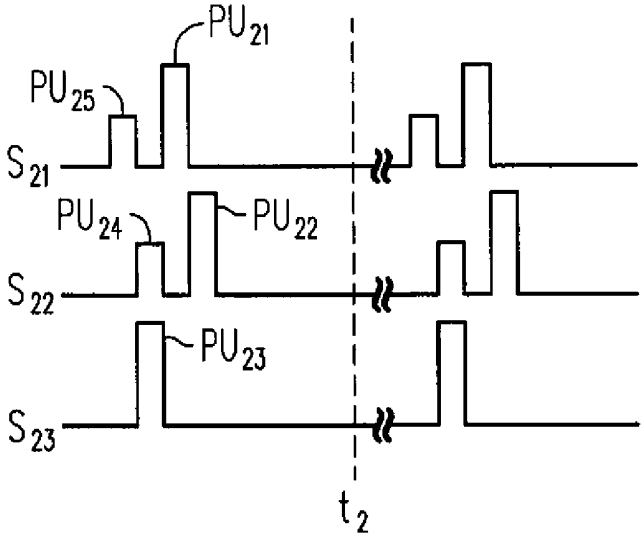

PU21
PU25
S21
PU24
PU22
S22
PU23
S23
t2

FIG. 3B

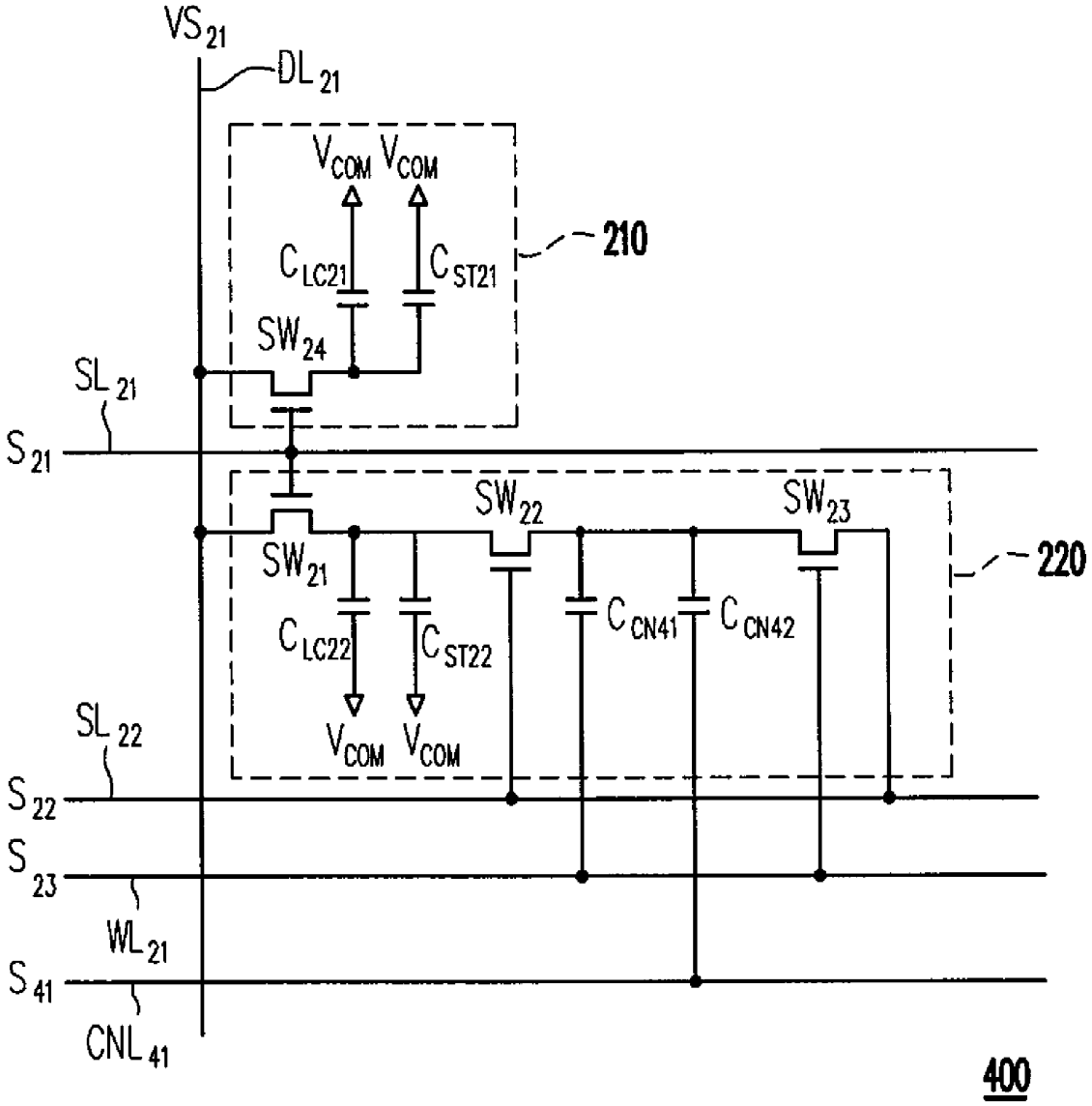

VS21
DL21
VCOM VCOM
CLC21
CST21
210
SW24
SL21
S21
SW22
SW23
SW21
220
CLC22
CST22
CCN41
CCN42
VCOM VCOM
SL22
S22
S23
WL21
S41
CNL41
400

FIG. 4A

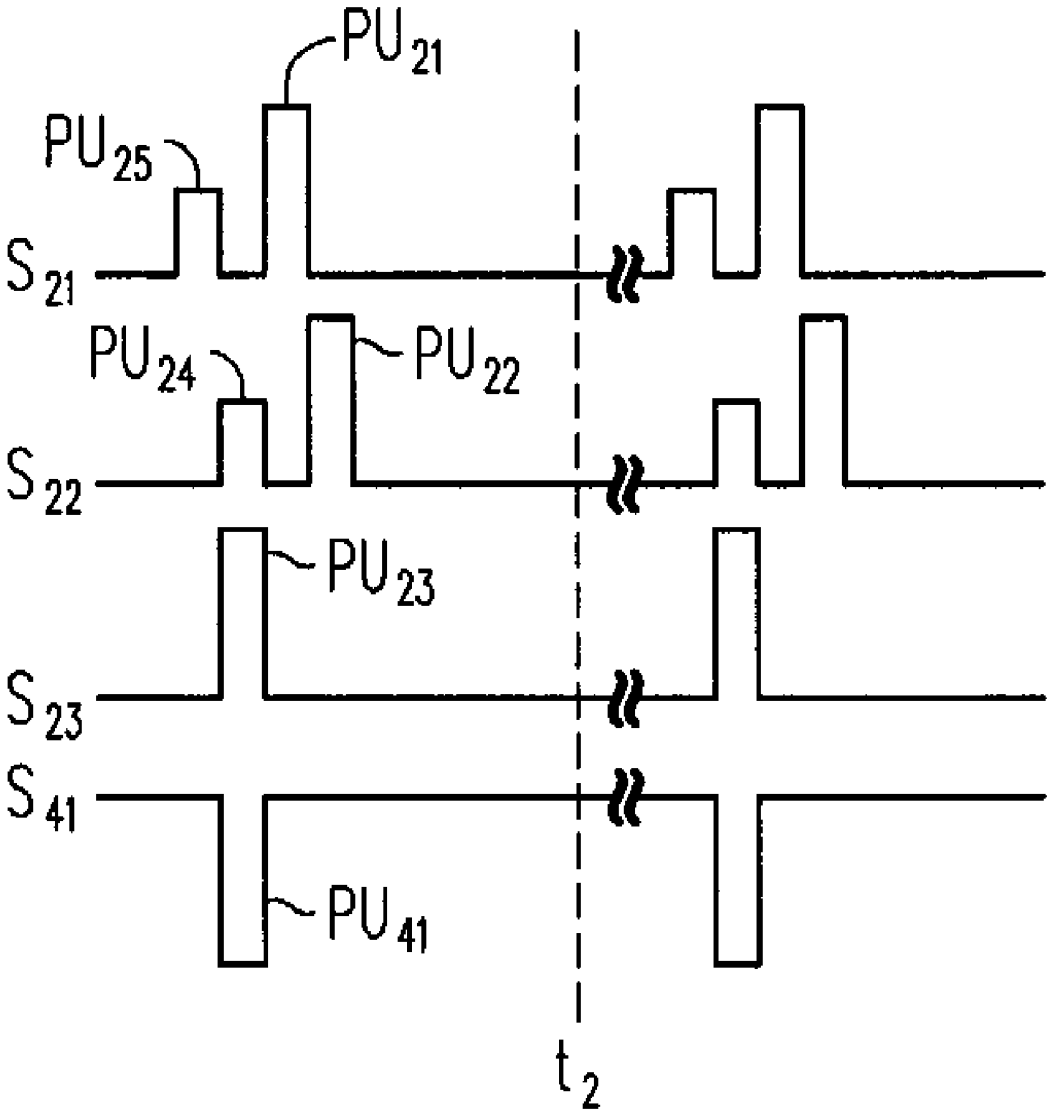


FIG. 4B

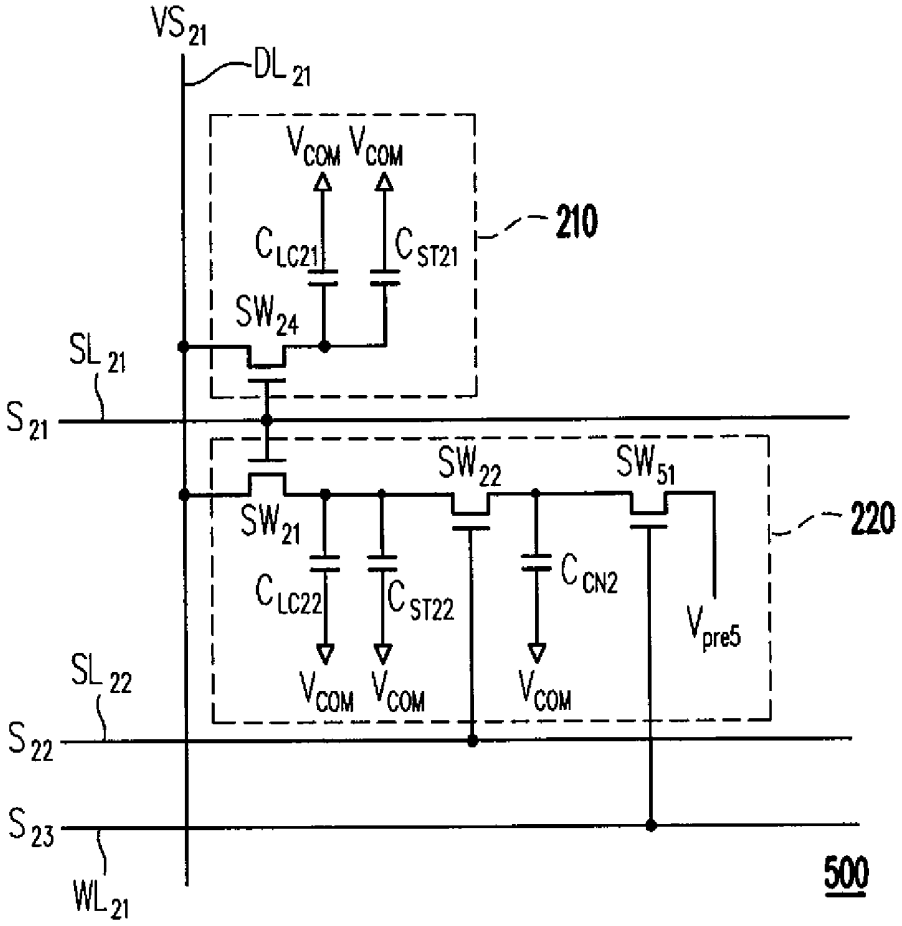

VS21
DL21
VCOM VCOM
CLC21
CST21
210
SW24
SL21
S21
SW22
SW51
SW21
220
CLC22
CST22
CCN2
Vpre5
VCOM VCOM VCOM
SL22
S22
S23
WL21
500

FIG. 5A

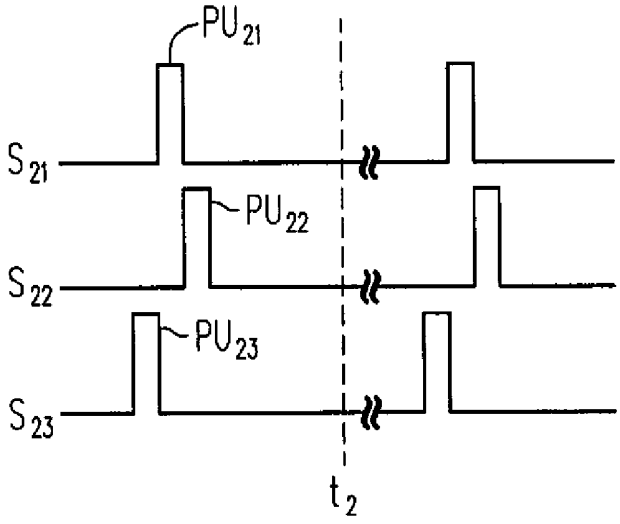

PU21
S21
PU22
S22
PU23
S23
t2

FIG. 5B

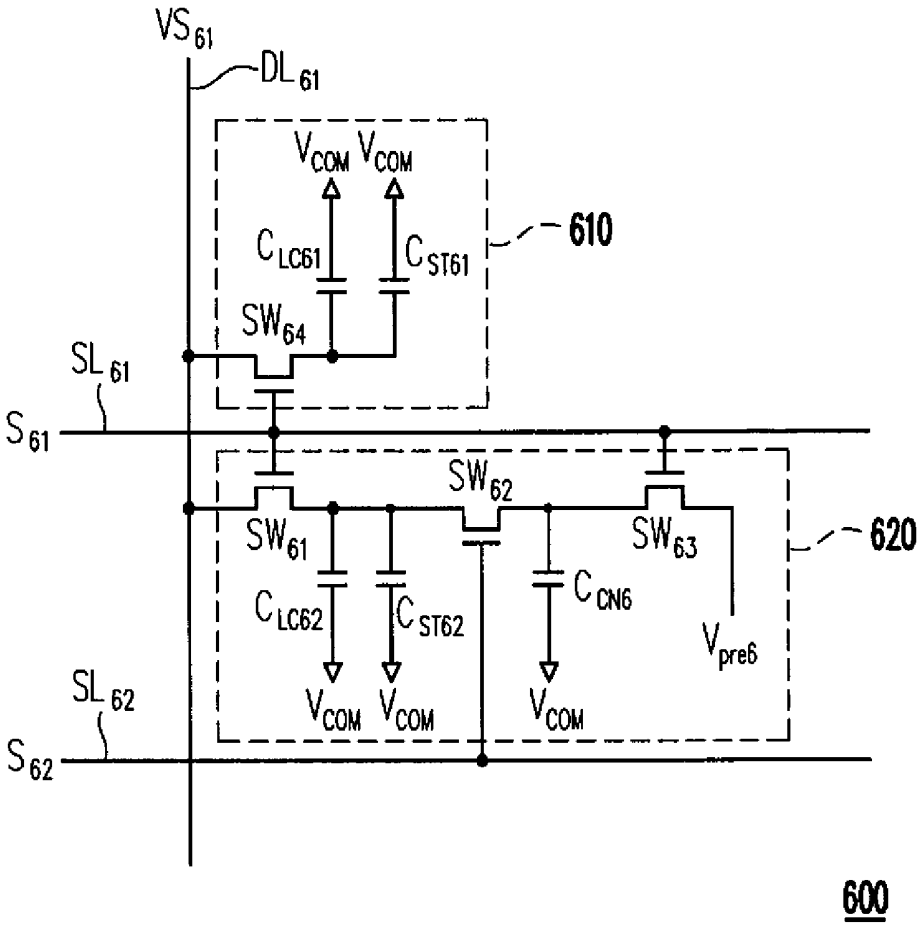

VS61
DL61
VCOM VCOM
CLC61
CST61
610
SW64
SL61
S61
SW62
SW61
SW63
620
CLC62
CST62
CCN6
Vpre6
VCOM VCOM VCOM
SL62
S62
600

FIG. 6A

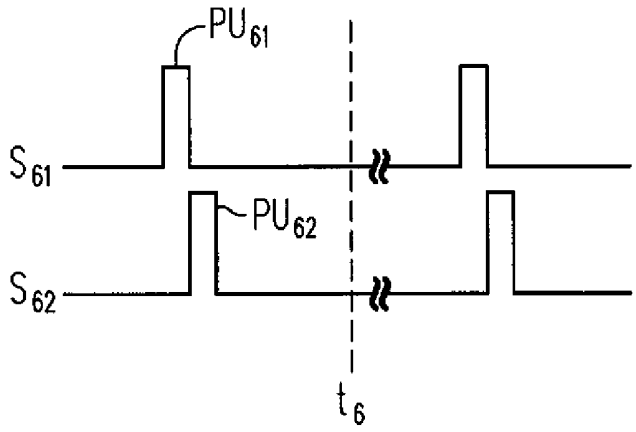

PU61
S61
PU62
S62
t6

FIG. 6B

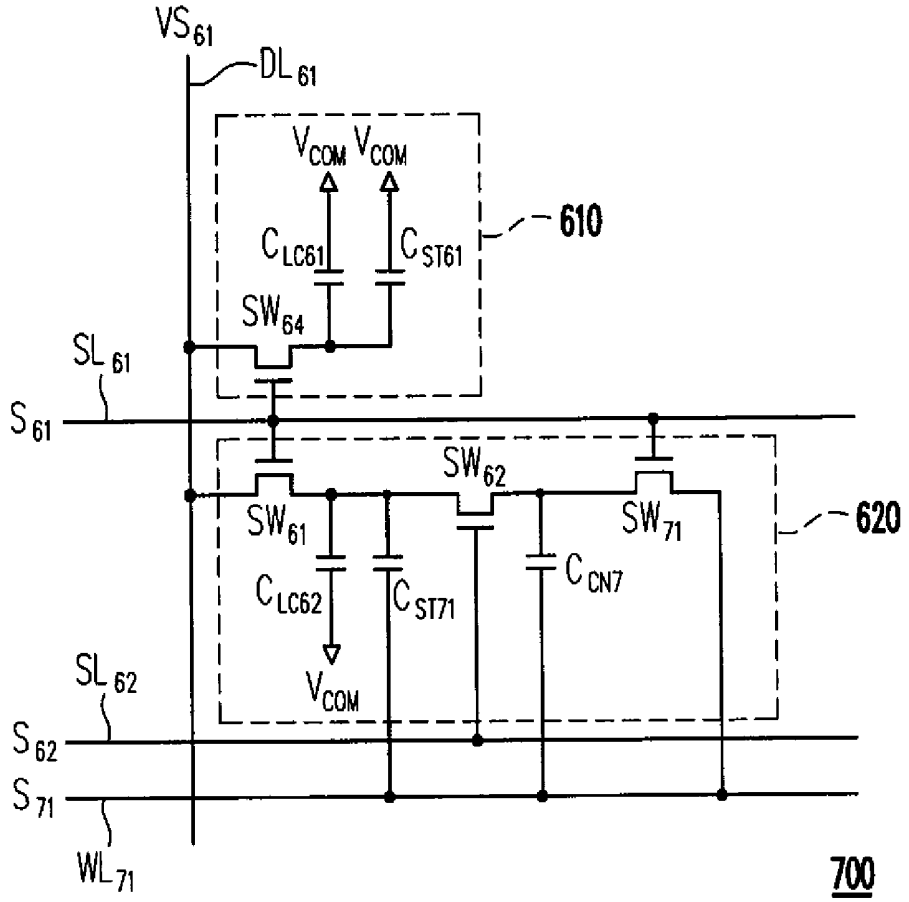

VS61
DL61
VCOM VCOM
610
CLC61
CST61
SW64
SL61
S61
SW62
SW61
SW71
620
CLC62
CST71
CCN7
VCOM
SL62
S62
S71
WL71
700

FIG. 7A

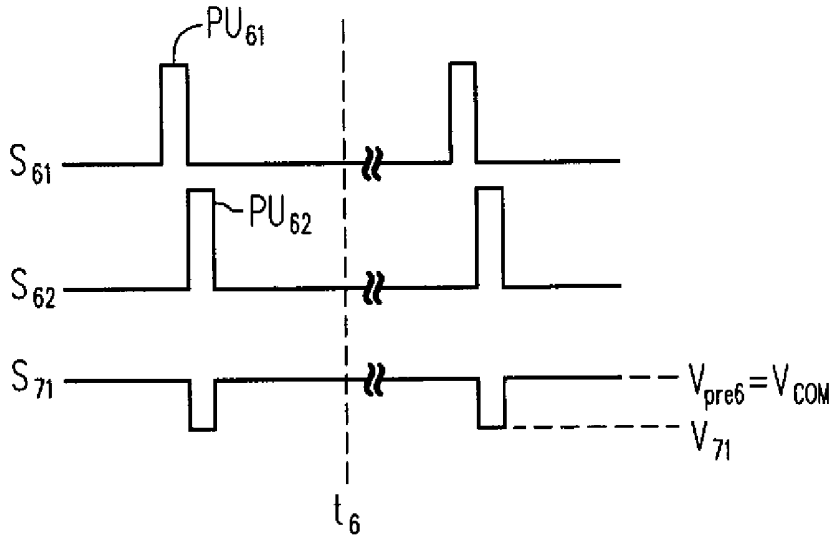

PU61
S61
PU62
S62
S71
Vpre6=VCOM
V71
t6

FIG. 7B

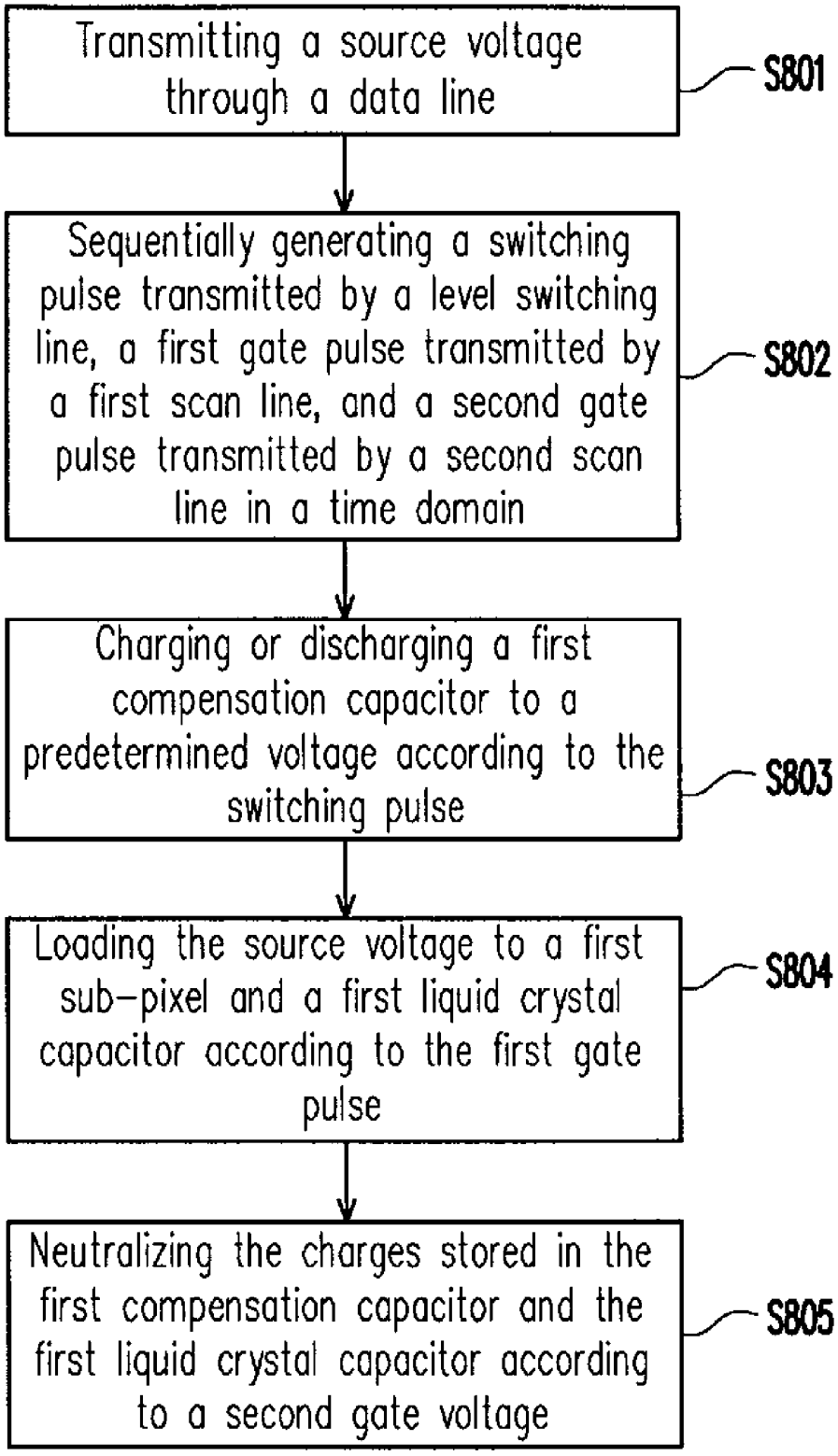

Transmitting a source voltage through a data line
S801
Sequentially generating a switching pulse transmitted by a level switching line, a first gate pulse transmitted by a first scan line, and a second gate pulse transmitted by a second scan line in a time domain
S802
Charging or discharging a first compensation capacitor to a predetermined voltage according to the switching pulse
S803
Loading the source voltage to a first sub-pixel and a first liquid crystal capacitor according to the first gate pulse
S804
Neutralizing the charges stored in the first compensation capacitor and the first liquid crystal capacitor according to a second gate voltage
S805

FIG. 8

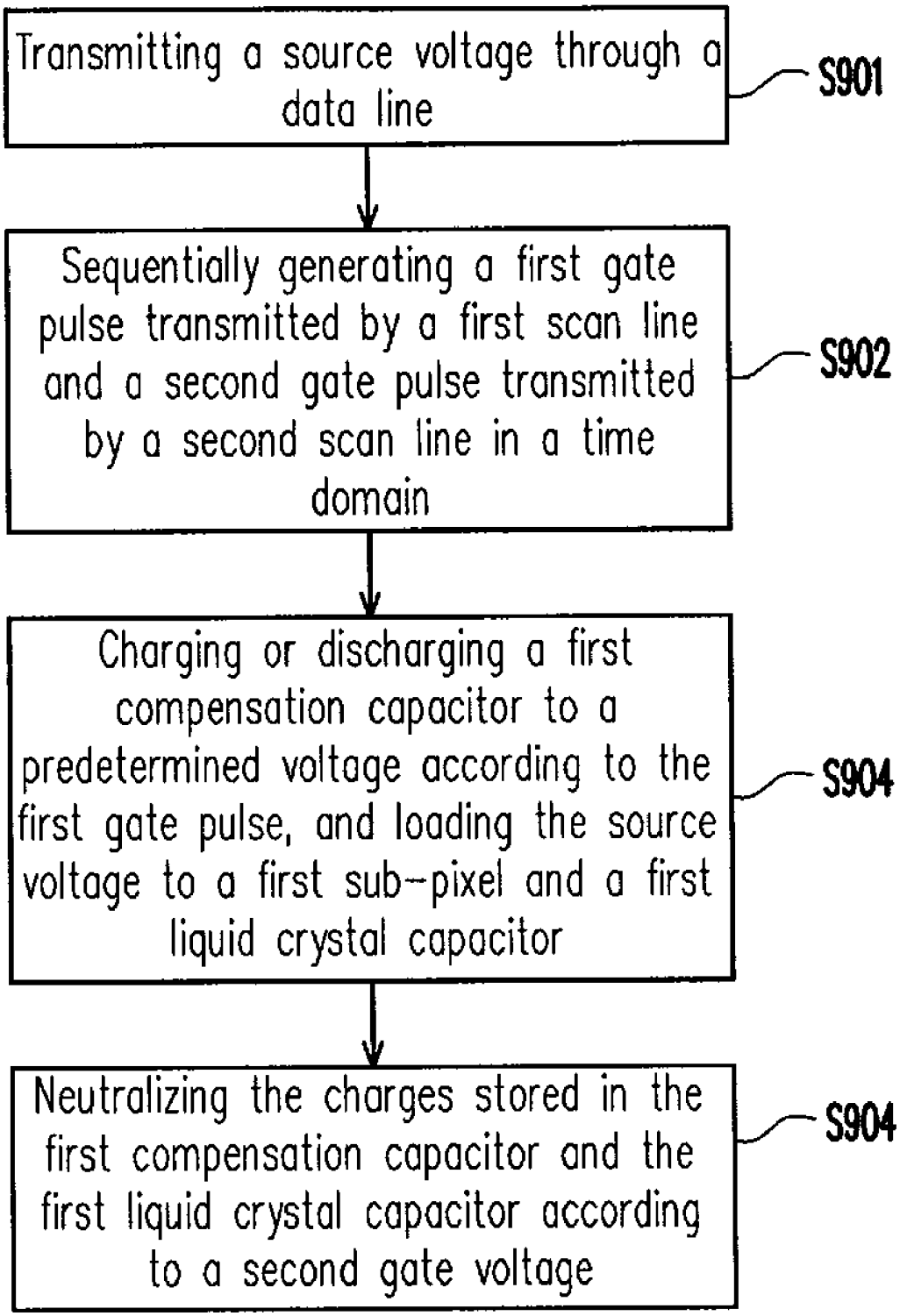

Transmitting a source voltage through a data line
S901
Sequentially generating a first gate pulse transmitted by a first scan line and a second gate pulse transmitted by a second scan line in a time domain
S902
Charging or discharging a first compensation capacitor to a predetermined voltage according to the first gate pulse, and loading the source voltage to a first sub-pixel and a first liquid crystal capacitor
S904
Neutralizing the charges stored in the first compensation capacitor and the first liquid crystal capacitor according to a second gate voltage
S904

FIG. 9

LIQUID CRYSTAL DISPLAY PANEL AND DRIVING METHOD THEREOF

[0001] This application claims the benefit of Taiwan application Serial No. 97120266, filed May 30, 2008, the entire disclosure of which is incorporated herein by reference.

BACKGROUND

[0002] The disclosure relates to a liquid crystal display panel and a method of driving such panel which in one or more embodiments are capable of eliminating residual images and/or non-uniform images.

[0003] A multi-domain vertical alignment liquid crystal display (MVA-$_{LC}$D) is capable of satisfying the requirement of wide viewing angle because the alignment protrusions or slits formed on the color filter substrate or the display device array substrate can cause liquid crystal molecules to be arranged in multiple directions to form multiple different alignment domains. However, it is inevitable that the transmittance-level curve of the MVA-LCD has different curvatures when the viewing angles are changed. The brightness displayed by the MVA-LCD varies as the viewing angle alters, which leads to the problems such as color shift, color washout, and so forth. At present, a structure as described below has been provided to solve the problems of color shift and color washout.

[0004] FIG. **1** is a circuit diagram of a pixel known to the inventor(s). Referring to FIG. **1**, a pixel **100** includes a first sub-pixel **110** and a second sub-pixel **120**. In the first sub-pixel **110**, a switch SW_{13} is conducted (turned-on) according to a gate pulse transmitted via a scan line SL_{11}. A source voltage VS_{11} transmitted via a data line DL_{11} is stored in a storage capacitor C_{ST11} and a liquid crystal capacitor C_{LC11}. In the meantime, a switch SW_{11} is also conducted, and the source voltage VS_{11} is stored in a storage capacitor C_{ST12} and a liquid crystal capacitor C_{LC12} of the second sub-pixel **120**.

[0005] After the first sub-pixel **110** and the second sub-pixel **120** store the source voltage VS_{11}, a switch SW_{12} is conducted according to a gate pulse transmitted via a scan line SL_{12}. Further, the charges in the liquid crystal capacitor C_{LC12}, the storage capacitor C_{ST12}, and a compensation capacitor C_{CN1} are neutralized. Accordingly, the pixel **100** mixes colors of the sub-pixels based on different transmittance variations of the two sub-pixels **110** and **120**, so as to equate the transmittance variations at a side viewing angle and at a front viewing angle, and thereby solving the problems of color shift and color washout.

[0006] In the known technology, however, the charge in the compensation capacitor C_{CN1} is varied whenever the compensation capacitor C_{CN1} performs the charge neutralization. In other words, the quantum of charge in the compensation capacitor C_{CN1} changes as the pixel **100** switches the gray scale of the displayed image. Under such a circumstance, the pixel **100** cannot predict the charge in the compensation capacitor C_{CN1}. When the pixel **100** displays an image, gray scale voltage levels may be inconsistent and result in the problems of residual image and non-uniform image.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1** is a circuit diagram of a known pixel.

[0008] FIG. **2**A is a circuit diagram of a pixel according to an embodiment.

[0009] FIG. **2**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **2**A.

[0010] FIG. **3**A is a circuit diagram of a pixel according to another embodiment.

[0011] FIG. **3**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **3**A.

[0012] FIG. **4**A is a circuit diagram of a pixel according to a further embodiment.

[0013] FIG. **4**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **4**A.

[0014] FIG. **5**A is a circuit diagram of a pixel according to still another embodiment.

[0015] FIG. **5**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **5**A.

[0016] FIG. **6**A is a circuit diagram of a pixel according to yet another embodiment.

[0017] FIG. **6**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **6**A.

[0018] FIG. **7**A is a circuit diagram of a pixel according to a still further embodiment.

[0019] FIG. **7**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **7**A.

[0020] FIG. **8** is a flowchart illustrating a driving method of a liquid crystal display panel according to an embodiment.

[0021] FIG. **9** is a flowchart illustrating a driving method of a liquid crystal display panel according to another embodiment.

DETAILED DESCRIPTION OF EMBODIMENTS

[0022] In the following detailed description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding. It will be apparent, however, that further embodiments may be practiced without these specific details. In other instances, well-known structures and devices are schematically shown in order to simplify the drawings.

[0023] In addition, the liquid crystal display panels in the embodiments comprise a plurality of pixels. For clarity and simplicity, only one of the pixels is illustrated as an example for explanation. In the following paragraphs, elements having identical or similar functions and structures are assigned with the same reference numbers and terms for consistency.

[0024] FIG. **2**A is a circuit diagram of a pixel according to an embodiment. With reference to FIG. **2**A, a pixel **200** includes a first sub-pixel **210** and a second sub-pixel **220**. Herein, the first sub-pixel **210** is coupled to a data line DL_{21} and a scan line SL_{21}. The second sub-pixel **220** is coupled to the data line DL_{21}, the scan line SL_{21}, a scan line SL_{22}, and a level switching line WL_{21}. In this embodiment, the scan line SL_{22} and a scan line SL_{23} are respectively connected to structures identical to the first sub-pixel **210** and the second sub-pixel **220** as well. For simplicity, these structures are not shown in the drawings.

[0025] Furthermore, the first sub-pixel **210** comprises a switch SW_{24}, a storage capacitor C_{ST21}, and a liquid crystal capacitor C_{LC21}. Herein, a first end of the switch SW_{24}, such as a drain, is coupled to the data line DL_{21}, and a control end of the switch SW_{24}, such as a gate, is coupled to the scan line SL_{21}. A first end of the liquid crystal capacitor C_{LC21} is coupled to a second end, such as a source, of the switch SW_{24}, and a second end of the liquid crystal capacitor C_{LC21} is coupled to a common voltage V_{COM}. The storage capacitor C_{ST21} and the liquid crystal capacitor C_{LC21} are connected in parallel.

[0026] Moreover, the second sub-pixel **220** comprises a switch SW_{21}, a switch SW_{22}, a switch SW_{23}, a storage capacitor C_{ST22}, a compensation capacitor C_{CN2}, and a liquid crystal capacitor C_{LC22}. A first end of the switch SW_{21}, such as a drain, is coupled to the data line DL_{21}, and a control end of the switch SW_{21}, such as a gate, is coupled to the scan line SL_{21}. A first end of the liquid crystal capacitor C_{LC22} is coupled to a second end, such as a source, of the switch SW_{21}, and a second end of the liquid crystal capacitor C_{LC22} is coupled to the common voltage V_{COM}. The storage capacitor C_{ST22} and the liquid crystal capacitor C_{LC22} are connected in parallel. Additionally, a first end of the switch SW_{22} is coupled to a first end of the storage capacitor C_{ST22}, and a control end of the switch SW_{22} is coupled to the scan line SL_{22}. A first end of the compensation capacitor C_{CN2} is coupled to a second end of the switch SW_{22}, and a second end of the compensation capacitor C_{CN2} is coupled to the common voltage V_{com}. A first end of the switch SW_{23} is coupled to the first end of the compensation capacitor C_{CN2}, and a control end of the switch SW_{23} is coupled to the level switching line WL_{21}. Further, a second end of the switch SW_{23} is coupled to the scan line SL_{22}.

[0027] FIG. **2**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **2**A. wherein S_{21} represents a signal transmitted via the scan line SL_{21}, S_{22} represents a signal transmitted via the scan line SL_{22}, S_{23} represents a signal transmitted via the level switching line WL_{21}, and VS_{21} represents a source voltage transmitted via the data line DL_{21}. The signal S_{21} comprises a gate pulse PU_{21} and a specific pulse PU_{25} as time changes. Similarly, the signal S_{22} comprises a gate pulse PU_{22} and a specific pulse PU_{24}, and the signal S_{23} comprises a switching pulse PU_{23}. In this embodiment, the specific pulse PU_{25} is equal to the specific pulse PU_{24}, and the gate pulse PU_{21} is equal to the gate pulse PU_{22}.

[0028] The specific pulse PU_{25} is transmitted to another pixel (not shown) of the scan line SL_{21}, and the operation mechanism thereof is the same as the operation mechanism of the specific pulse PU_{24} and the pixel **200**. Furthermore, in this specific embodiment, the switching pulse PU_{23}, the gate pulse PU_{21}, and the gate pulse PU_{22} are transmitted sequentially, and the specific pulse PU_{24} and the switching pulse PU_{23} are transmitted simultaneously.

[0029] Further, referring to FIG. **2**A and FIG. **2**B for the operation mechanism of the pixel **200**, the switch SW_{24} conducts the first end and the second end thereof according to the gate pulse PU_{21}. In the meantime, the data line DL_{21} and the storage capacitor Cs_{51} are electrically connected, so as to load the source voltage VS_{21} on the data line DL_{21} to the liquid crystal capacitor C_{LC21}. Because the liquid crystal capacitor C_{LC21} and the storage capacitor C_{ST21} are connected in parallel, the source voltage VS_{21} is stored in the storage capacitor C_{ST21} as well. Meanwhile, the switch SW_{21} also conducts the first end and the second end thereof according to the gate pulse PU_{21}. The source voltage VS_{21} is loaded to the liquid crystal capacitor C_{LC22} and the storage capacitor C_{ST22}.

[0030] Then, the switch SW_{22} conducts the first end and the second end thereof according to the gate pulse PU_{22}. At the same time, the charges in the liquid crystal capacitor C_{LC22}, the storage capacitor C_{ST22}, and the compensation capacitor C_{CN2} are neutralized. Thereby, the transmittance variations of the first sub-pixel **210** and the second sub-pixel **220** are differentiated. The pixel **200** mixes colors and/or gray levels of the sub pixels based on the different transmittance variations of the two sub-pixels and brings the transmittance at a side viewing angle close to that at a front viewing angle to overcome the problems of color shift and color washout.

[0031] It should be noted that the switch SW_{23} conducts the first end and the second end thereof according to the switching pulse PU_{23} before the compensation capacitor C_{CN2} performs charge neutralization. Simultaneously, the compensation capacitor C_{CN2} loads the specific pulse PU_{24} transmitted via the scan line SL_{22}. Because a voltage level of the specific pulse PU_{24} is maintained at a predetermined voltage, the compensation capacitor C_{CN2} is charged or discharged to the predetermined voltage correspondingly.

[0032] In other words, before the liquid crystal capacitor C_{LC22}, the storage capacitor C_{ST22}, and the compensation capacitor C_{CN2} perform charge neutralization, the compensation capacitor C_{CN2} charges or discharges to the predetermined voltage according to the switching pulse PU_{23}. Assume that the pixel **200** starts gray scale switching of the image at a timing t_2, then during the switching, the compensation capacitor C_{CN2} is still charging or discharging to the predetermined voltage based on the aforementioned waveform and then performs charge neutralization with the liquid crystal capacitor C_{LC22} and the storage capacitor C_{ST22}.

[0033] No matter how many times the pixel **200** switches the gray scale of the image, the quantum of charge in the compensation capacitor C_{CN2} remains a fixed value before charge neutralization is performed. The problems of residual image and non-uniform image, resulting from the uncertain charge of the compensation capacitor, are therefore overcome. It is noted that the predetermined voltage as described in this embodiment may be the common voltage V_{COM}. In other embodiments the predetermined voltage is varied to meet certain designs and requirements.

[0034] FIG. **3**A is a circuit diagram of a pixel **300** according to another embodiment, and FIG. **3**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **3**A. A storage capacitor C_{ST31} of the first sub-pixel **210** and a compensation capacitor C_{CN3} and a storage capacitor C_{ST32} of the second sub-pixel **220** differentiate the embodiments of FIGS. **3**A and **3**B from the embodiments of FIGS. **2**A and **2**B.

[0035] To be more specific, in the pixel **300**, a first end of the storage capacitor C_{ST31} is coupled to the second end of the switch SW_{24}, and a second end of the storage capacitor C_{ST31} is coupled to the scan line SL_{22}. In addition, a first end of the compensation capacitor C_{CN3} is coupled to the second end of the switch SW_{22}, and a second end of the compensation capacitor C_{CN3} is coupled to the scan line SL_{22}. Further, a first end of the storage capacitor C_{ST32} is coupled to the second end of the switch SW_{21}, and a second end of the storage capacitor C_{ST32} is coupled to the scan line SL_{22}. In this embodiment, the storage capacitors C_{ST31} and C_{ST32} and the compensation capacitor C_{CN3} share the scan line SL_{22}, so as to simplify the complexity of the wire layout in the pixel **300**.

[0036] Similar to the embodiment shown in FIG. **2**A, the switch SW_{23} conducts the first end and the second end thereof according to the switching pulse PU_{23} before the liquid crystal capacitor C_{LC22}, the storage capacitor C_{ST32}, and the compensation capacitor C_{CN3} performs the charge neutralization. In the meantime, the compensation capacitor C_{CN3} loads a specific pulse PU_{24} which has a voltage level maintained at the predetermined voltage. In other words, the quantum of charge in the compensation capacitor C_{CN3} is maintained at a fixed value before neutralization is performed, so as to solve

the problems of residual image and non-uniform image caused by the changeable charge of the compensation capacitor.

[0037] Further, FIG. **4**A is a circuit diagram of a pixel **400** according to another embodiment, and FIG. **4**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **4**A.

[0038] Compensation capacitors C_{CN41} and C_{CN42} and a level complementary line CNL_{41} of the second sub-pixel **220** are the main differences between the embodiments of FIGS. **4**A and **4**B and the foregoing embodiments.

[0039] Specifically, in the pixel **400**, a first end of the compensation capacitor C_{CN41} is coupled to the second end of the switch SW_{22}, and a second end of the compensation capacitor C_{CN41} is coupled to the level switching line WL_{21}. A first end of the compensation capacitor C_{CN42} is coupled to the first end of the compensation capacitor C_{CN41}, and a second end of the compensation capacitor C_{CN42} is coupled to the level complementary line CNL_{41}. As shown in FIG. **4**B, S_{41} represents a signal transmitted via the level complementary line CNL_{41}, and a voltage level of the signal S_{41} forms a complementary pulse PU_{41} as time changes. It should be noted that the complementary pulse PU_{41} is reverse to the switching pulse PU_{23}. Therefore, the complementary pulse PU_{41} loaded to the compensation capacitor C_{CN42} may compensate the capacitor coupling effects which the switching pulse PU_{23} causes to the compensation capacitor C_{CN41}.

[0040] In this embodiment, it should also be noted that the second end of the storage capacitor C_{ST21} may also be electrically connected to the level switching line WL_{21} or the level complementary line CNL_{41} in addition to the common voltage V_{COM}. Further, the level switching line WL_{21} and the level complementary line CNL_{41} transmit the switching pulse PU_{23} and the complementary pulse PU_{41} before the gate pulse PU_{21} is formed. In addition, when the gate pulse PU_{21} is formed, the signals S_{23} and S_{41} transmitted via the level switching line WL_{21} and the level complementary line CNL_{41}, respectively, will be restored to the common voltage V_{COM}. Hence, when the gate pulse PU_{21} is formed, the storage capacitor C_{ST21} loads the source voltage VS_{21} based on the common voltage V_{COM} notwithstanding whether the second end of the storage capacitor C_{ST21} is electrically connected to the level switching line WL_{21} or to the level complementary line CNL_{41}.

[0041] Similar to the above embodiments, the compensation capacitors C_{CN41} and C_{CN42} perform charge neutralization with the liquid crystal capacitor C_{LC22} and the storage capacitor C_{ST22}. Before performing the charge neutralization, the compensation capacitors C_{CN41} and C_{CN42} load the specific pulse PU_{24} which has voltage level maintained at the predetermined voltage. Accordingly, the pixel **400** is able to solve the problems of residual image and non-uniform image, resulting from the changeable charge of the compensation capacitor.

[0042] FIG. **5**A is a circuit diagram of a pixel **500** according to another embodiment, and FIG. **5**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **5**A.

[0043] A switch SW_{51} of the second sub-pixel **220** differentiates the embodiments of FIG. **5**A and FIG. **5**B from the foregoing embodiments.

[0044] Specifically, in the pixel **500**, a first end of the switch SW_{51} is coupled to the first end of the compensation capacitor C_{CN2}, and a second end of the switch SW_{51} is coupled to a predetermined voltage V_{pre5}. Furthermore, a control end of the switch SW_{51} is coupled to the level switching line WL_{21}. Herein, the switch SW_{51} conducts the first end and the second end thereof according to the switching pulse PU_{23}, so as to charge or discharge the compensation capacitor C_{CN2} to the predetermined voltage V_{pre5}. Thereby, the quantum of charge of the compensation capacitor C_{CN2} is maintained at a fixed value before charge neutralization is performed.

[0045] It is noted that, because the second end of the switch SW_{51} is directly coupled to a constant voltage source (the predetermined voltage V_{pre5}) as shown in FIG. **5**B, each of the signals S_{21} and S_{22} transmitted via the scan lines SL_{21} and SL_{22} merely comprises one gate pulse. That is to say, the pixel **500** may adopt a driving waveform similar to the pixel **100** (shown in FIG. **1**) for displaying images. In addition, similar to the above embodiments, the compensation capacitor C_{CN2} charges or discharges to the predetermined voltage according to the switching pulse PU_{23} before performing charge neutralization. Therefore, the pixel **500** is able to solve the problems of residual image and non-uniform image which results from the changeable charge of the compensation capacitor.

[0046] FIG. **6**A is a circuit diagram of a pixel **600** according to yet another embodiment. Referring to FIG. **6**A, the pixel **600** comprises a first sub-pixel **610** and a second sub-pixel **620**. Herein, the first sub-pixel **610** is coupled to a data line DL_{61} and a scan line SL_{61}. The second sub-pixel **620** is coupled to the data line DL_{61} and scan lines SL_{61}~SL_{62}.

[0047] Further, the first sub-pixel **610** comprises a switch SW_{64}, a storage capacitor C_{ST61}, and a liquid crystal capacitor C_{LC61}. Herein, a first end of the switch SW_{64} is coupled to the data line DL_{61} and a control end of the switch SW_{64} is coupled to the scan line SL_{61}. A first end of the liquid crystal capacitor C_{LC61} is coupled to the second end of the switch SW_{64}, and a second end of the liquid crystal capacitor C_{LC61} is coupled to the common voltage V_{COM}. The storage capacitor C_{ST61} and the liquid crystal capacitor C_{LC61} are connected in parallel.

[0048] In addition, the second sub-pixel **620** comprises switches SW_{61}~SW_{63}, a storage capacitor C_{ST62}, a compensation capacitor C_{CN}**6**, and a liquid crystal capacitor C_{LC62}. Herein, a first end of the switch SW_{61} is coupled to the data line DL_{61} and a control end of the switch SW_{61} is coupled to the scan line SL_{61}. A first end of the liquid crystal capacitor C_{LC62} is coupled to a second end of the switch SW_{61}, and a second end of the liquid crystal capacitor C_{LC62} is coupled to the common voltage V_{COM}. The storage capacitor C_{ST62} and the liquid crystal capacitor C_{LC62} are connected in parallel.

[0049] Moreover, a first end of the switch SW_{62} is coupled to a first end of the storage capacitor C_{ST62}, and a control end of the switch SW_{62} is coupled to the scan line SL_{62}. A first end of the compensation capacitor C_{CN6} is coupled to a second end of the switch SW_{62}, and a second end of the compensation capacitor C_{CN6} is coupled to the common voltage V_{COM}. A first end of the switch SW_{63} is coupled to the first end of the compensation capacitor C_{CN6}, and a control end of the switch SW_{63} is coupled to the scan line SL_{61}. Further, a second end of the switch SW_{63} is coupled to a predetermined voltage V_{pre6}. It should be noted that the predetermined voltage V_{pre6} as described in this embodiment may be the common voltage V_{COM}. However, in other embodiments, the predetermined voltage is varied to meet certain designs and requirements.

[0050] FIG. **6**B is a waveform-timing diagram for illustrating the operation of the fifth embodiment, wherein S_{61} represents a signal transmitted via the scan line SL_{61}, S_{62} represents a signal transmitted via the scan line SL_{62}, and VS_{61}

represents a source voltage transmitted via the data line DL_{61}. In addition, a voltage level of the signal S_{61} forms a gate pulse PU_{61} as time changes. Similarly, the signal S_{62} comprises a gate pulse PU_{62} and the specific pulse PU_{24}. The gate pulse PU_{61} and the gate pulse PU_{62} are sequentially delivered.

[0051] Further, referring to FIG. **6**A and FIG. **6**B for the operation mechanism of the pixel **600**, the switch SW_{64} conducts the first end and the second end thereof according to the gate pulse PU_{61}. In the meantime, the liquid crystal capacitor C_{LC61} loads a source voltage VS_{61} from the data line DL_{61}. The source voltage VS_{61} is also stored in the storage capacitor C_{ST61}. Similar to the above, the switch SW_{61} also conducts the first end and the second end thereof according to the gate pulse PU_{61}. Accordingly, the liquid crystal capacitor C_{LC62} also loads the source voltage VS_{21}, and the storage capacitor C_{ST62} also stores the source voltage VS_{21}.

[0052] Furthermore, the switch SW_{63} also conducts the first end and the second end thereof according to the gate pulse PU_{61}. Due to the conduction of the switch SW_{63}, the compensation capacitor C_{CN6} charges or discharges to the predetermined voltage V_{pre6}. Then, when the switch SW_{62} conducts the first end and the second end thereof according to the gate pulse PU_{62}, the liquid crystal capacitor C_{LC62}, the storage capacitor C_{ST62}, and the compensation capacitor C_{CN6} perform charge neutralization. As a consequence, the transmittance variations of the first sub-pixel **610** and the second sub-pixel **620** are differentiated. The pixel **600** mixes colors and/or gray levels of the sub-pixels based on the different transmittance variations of the two sub-pixels, and thereby equates the transmittance variations at a side viewing angle and at a front viewing angle.

[0053] It should be noted that, provided the pixel **600** starts gray scale switching of the image at a timing t_6, during the switching, the compensation capacitor C_{CN6} is still charging or discharging to the predetermined voltage V_{pre6} based on the aforementioned waveform and then perform charge neutralization with the liquid crystal capacitor C_{LC62} and the storage capacitor C_{ST62}. In other words, no matter how many times the pixel **600** switches the gray scale of the image, the quantum of charge in the compensation capacitor C_{CN6} remains a fixed value before charge neutralization is performed. The problems of residual image and non-uniform image, resulting from an uncertain charge of the compensation capacitor, are therefore overcome.

[0054] FIG. **7**A is a circuit diagram of a pixel **700** according to another embodiment, and FIG. **7**B is a waveform-timing diagram for illustrating the operation of the embodiment of FIG. **7**A.

[0055] The main differences between the embodiments of FIGS. **7**A and **7**B and the embodiments of FIGS. **6**A and **6**B are a storage capacitor C_{ST71}, a compensation capacitor C_{CN7}, a switch SW_{71}, and a level switching line WL_{71} of the second sub-pixel **620**.

[0056] To be more specific, in the pixel **700**, a first end of the storage capacitor C_{ST71} is coupled to the first end of the switch SW_{62}, and a second end of the storage capacitor C_{ST71} is coupled to the level switching line WL_{71}. A first end of the compensation capacitor C_{CN7} is coupled to the second end of the switch SW_{62}, and a second end of the compensation capacitor C_{CN7} is coupled to the level switching line WL_{71}. Moreover, a first end of the switch SW_{71} is coupled to the first end of the compensation capacitor C_{CN7}, and a control end of the switch SW_{71} is coupled to the scan line SL_{61}. Further, a second end of the switch SW_{71} is coupled to the level switching line WL_{71}.

[0057] In addition, as shown in FIG. **7**B, S_{71} represents a signal transmitted via the level switching line WL_{71}, and a voltage level of the signal S_{71} is switched from the predetermined voltage V_{pre6} to a compensation voltage V_{71} according to the gate pulse PU_{62}. It is noted that the compensation voltage V_{71} is smaller than the predetermined voltage V_{pre6}, and the predetermined voltage V_{pre6} is equal to the common voltage V_{COM} of the liquid crystal display panel.

[0058] Because the voltage level of the signal S_{71} is maintained at the predetermined voltage V_{pre6}, when the switch SW_{71} conducts the first end and the second end thereof according to the gate pulse PU_{61}, the compensation capacitor C_{CN7} charges or discharges to the predetermined voltage V_{pre6}. Then, the voltage level of the signal S_{71} is switched from the predetermined voltage V_{pre6} to the compensation voltage V_7, according to the gate pulse PU_{62}, so that while the switch SW_{62} is switched according to the gate pulse PU_{62}, the feed-through voltages formed from the switch SW_{62} to the storage capacitor C_{ST71} and the compensation capacitor C_{CN7} may be neutralized. Thus, the charges in the compensation capacitor C_{CN7} and the storage capacitor C_{ST71} are not changed when the switch SW_{62} functions. Problems such as non-uniform image or flicker are therefore reduced.

[0059] Furthermore, similar to the embodiments of FIGS. **6***a*-**6**B, the liquid crystal capacitor C_{LC62}, the storage capacitor C_{ST71}, and the compensation capacitor C_{CN7} perform the charge neutralization due to the conduction of the switch SW_{62}. As mentioned above, the quantum of charge of the compensation capacitor C_{CN7} is maintained at a fixed value before charge neutralization is performed. Hence, the pixel **700** mixes colors and/or gray levels of the sub-pixels based on the different transmittance variations of the two sub-pixels, and thereby equates the transmittance variations at a side viewing angle and at a front viewing angle.

[0060] FIG. **8** is a flowchart illustrating a driving method of a liquid crystal display panel according to an embodiment. Referring to FIG. **8**, the driving method of liquid crystal display panel in this embodiment comprises the following steps. First, a source voltage is transmitted through a data line (Step S**801**). Then, in Step S**802**, a switching pulse transmitted via a level switching line, a first gate pulse transmitted via a first scan line, and a second gate pulse transmitted via a second scan line are sequentially generated.

[0061] Next, in Step S**803**, a first compensation capacitor is charged or discharged to a predetermined voltage according to the switching pulse. Thereafter, in Step S**804**, the source voltage is loaded to a first sub-pixel and a first liquid crystal capacitor according to the first gate pulse. Finally, in Step S**805**, the charges stored in the first compensation capacitor and the first liquid crystal capacitor are neutralized according to a second gate voltage.

[0062] In this embodiment, Step S**805**, in which the first compensation capacitor is charged or discharged to the predetermined voltage according to the switching pulse, further comprises the following steps. First, a specific pulse is transmitted through the second scan line. Then, the specific pulse is loaded to the first compensation capacitor according to the switching pulse, wherein a voltage level of the specific pulse is maintained at the predetermined voltage.

[0063] The foregoing driving method corresponds to the embodiments discussed with respect to FIGS. **2**A-**5**B.

Another driving method corresponding to the embodiments discussed with respect to FIGS. **6**A-**7**B will be further provided in the following paragraphs.

[0064] FIG. **9** is a flowchart illustrating a driving method of a liquid crystal display panel according to another embodiment. First, a source voltage is transmitted through a data line (Step S**901**). Next, in Step S**902**, a first gate pulse transmitted via a first scan line and a second gate pulse transmitted via a second scan line are generated sequentially.

[0065] Further, in Step S**903**, a first compensation capacitor is charged or discharged to a predetermined voltage according to the first gate pulse, and the source voltage is loaded to a first sub-pixel and a first liquid crystal capacitor. Finally, in Step S**904**, the charges stored in the first compensation capacitor and the first liquid crystal capacitor are neutralized according to a second gate voltage.

[0066] It should be noted that the aforementioned predetermined voltage is equal to the common voltage of the liquid crystal display panel in some embodiments, and the predetermined voltage may be varied in other embodiments to certain requirements.

[0067] In one or more embodiments, the charge neutralization is performed by the compensation capacitor and the storage capacitor to equate the transmittance variations at a side viewing angle and at a front viewing angle. Moreover, the quantum of charge of the compensation capacitor is maintained at a fixed value before the charge neutralization is performed. Thus, the problems of residual image and non-uniform image caused by the uncertain charge of the compensation capacitor can be solved.

What is claimed is:

1. A liquid crystal display panel comprising a plurality of pixels each comprising:

a first sub-pixel, coupled to a data line and a first scan line, for receiving a source voltage transmitted via the data line according to a first gate pulse transmitted via the first scan line; and

a second sub-pixel, coupled at least to the data line, the first scan line, and a second scan line for receiving the source voltage according to the first gate pulse, wherein the second sub-pixel comprises:

a first liquid crystal capacitor, for loading the source voltage; and

a first compensation capacitor coupled to be charged or discharged to a predetermined voltage before performing charge neutralization with the first liquid crystal capacitor according to a second gate pulse transmitted via the second scan line.

2. The liquid crystal display panel as claimed in claim **1**, wherein the second sub-pixel is further coupled to a level switching line and the first compensation capacitor is coupled to be charged or discharged to the predetermined voltage according to a switching pulse transmitted via the level switching line.

3. The liquid crystal display panel as claimed in claim **2**, wherein the second sub-pixel further comprises:

a switch which is coupled between the first compensation capacitor and a source of the predetermined voltage, and has a control terminal coupled to the level switching line for connecting the first compensation capacitor to the source of the predetermined voltage in response to the switching pulse transmitted via the level switching line.

4. The liquid crystal display panel as claimed in claim **3**, wherein the source of the predetermined voltage comprises a specific pulse transmitted via the second scan line prior to the second gate pulse.

5. The liquid crystal display panel as claimed in claim **3**, wherein the source of the predetermined voltage comprises a constant voltage source.

6. The liquid crystal display panel as claimed in claim **2**, wherein the second sub-pixel further comprises:

a first switch, having a first end coupled to the data line, a second end coupled to a first end of the first liquid crystal capacitor, and a control end coupled to the first scan line, wherein the first end and the second end of the first switch are connected in response to the first gate pulse;

a second switch, having a first end coupled to the first end of the first liquid crystal capacitor, a second end coupled to a first end of the first compensation capacitor, and a control end coupled to the second scan line, wherein the first end and the second end of the second switch are connected in response to the second gate pulse;

a third switch, having a first end coupled to the first end of the first compensation capacitor, a second end coupled to the second scan line, and a control end coupled to the level switching line, wherein the first end and the second end of the third switch are connected in response to the switching pulse, so as to load a specific pulse of the predetermined voltage from the second scan line into the first compensation capacitor.

7. The liquid crystal display panel as claimed in claim **6**, wherein the second sub-pixel further comprises:

a first storage capacitor having a first end connected to the first end of the first liquid crystal capacitor,

wherein a second end of the first liquid storage capacitor and a second end of the first compensation capacitor are commonly coupled.

8. The liquid crystal display panel as claimed in claim **7**, wherein the second ends of the first liquid storage capacitor and the first compensation capacitor are commonly coupled to a common voltage of the liquid crystal display panel.

9. The liquid crystal display panel as claimed in claim **7**, wherein the second ends of the first liquid storage capacitor and the first compensation capacitor are commonly coupled to the second scan line.

10. The liquid crystal display panel as claimed in claim **6**, wherein the second sub-pixel further comprises:

a second compensation capacitor having a first end coupled to the first end of the first compensation capacitor and a second end coupled to a level complementary line,

wherein a second end of the first compensation capacitor is coupled to the level switching line.

11. The liquid crystal display panel as claimed in claim **10**, wherein,

a signal transmitted via the level complementary line is a reverse of a signal transmitted via the level switching line; and

the second sub-pixel further comprises a first storage capacitor connected in parallel to the first liquid crystal capacitor, wherein a second end of the first liquid crystal capacitor is coupled to a common voltage of the liquid crystal display panel.

12. The liquid crystal display panel as claimed in claim **1**, wherein the predetermined voltage is equal to a common voltage of the liquid crystal display panel.

13. A liquid crystal display comprising the liquid crystal display panel as claimed in claim **1**.

14. The liquid crystal display panel as claimed in claim **1**, wherein:

the first compensation capacitor is coupled to be charged or discharged to the predetermined voltage according to the first gate pulse.

15. The liquid crystal display panel as claimed in claim **14**, wherein the second sub-pixel further comprises:

a switch which is coupled between the first compensation capacitor and a source of the predetermined voltage, and has a control terminal coupled to the first scan line for connecting the first compensation capacitor to the source of the predetermined voltage in response to the first gate pulse transmitted via the first scan line.

16. The liquid crystal display panel as claimed in claim **15**, wherein the second sub-pixel further comprises:

a first switch, having a first end coupled to the data line, a second end coupled to a first end of the first liquid crystal capacitor, and a control end coupled to the first scan line, wherein the first end and the second end of the first switch are connected in response to the first gate pulse;

a second switch, having a first end coupled to the first end of the first liquid crystal capacitor, a second end coupled to a first end of the first compensation capacitor, and a control end coupled to the second scan line, wherein the first end and the second end of the second switch are connected in response to the second gate pulse;

a third switch, having a first end coupled to the first end of the first compensation capacitor, a second end coupled to the predetermined voltage, and a control end coupled to the first scan line, wherein the first end and the second end of the third switch are connected in response to the first gate pulse; and

a first storage capacitor having a first end connected to the first end of the first liquid crystal capacitor, wherein a second end of the first storage capacitor and a second end of the first compensation capacitor are commonly coupled.

17. The liquid crystal display panel as claimed in claim **16**, wherein:

the second end of the third switch is coupled to a level switching line, and

a voltage level of a signal transmitted via the level switching line is switched from the predetermined voltage to a compensation voltage according to the second gate pulse, and the compensation voltage is smaller than the predetermined voltage.

18. A method of driving a liquid crystal display panel, wherein the liquid crystal display panel comprises a plurality of pixels each comprising a first sub-pixel and a second sub-pixel, wherein the second sub-pixel comprises a first liquid crystal capacitor and a first compensation capacitor, the first sub-pixel is coupled to a data line and a first scan line, the second sub-pixel is coupled at least to the data line, the first scan line, and a second scan line, said method comprising:

transmitting a source voltage through the data line to be loaded into the first and second sub-pixels in response to a first gate pulse transmitted via the first scan line, and a second gate pulse transmitted via the second scan line, respectively;

charging or discharging the first compensation capacitor to a predetermined voltage; and

after the first compensation capacitor has been charged or discharged to the predetermined voltage, neutralizing charges stored in the first compensation capacitor and the first liquid crystal capacitor according to the second gate pulse.

19. The method as claimed in claim **18**, wherein the second sub-pixel is further coupled to a level switching line and the first compensation capacitor is charged or discharged to the predetermined voltage according to a switching pulse transmitted via the level switching line.

20. The method as claimed in claim **18**, wherein the first compensation capacitor is charged or discharged to the predetermined voltage according to the first gate pulse.

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专利名称(译)	液晶显示面板及其驱动方法		
公开(公告)号	US20090295703A1	公开(公告)日	2009-12-03
申请号	US12/407972	申请日	2009-03-20
[标]申请(专利权)人(译)	群创光电股份有限公司		
申请(专利权)人(译)	奇美电子股份有限公司.		
当前申请(专利权)人(译)	群创光电		
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IPC分类号	G09G3/36		
CPC分类号	G09G3/3659 G09G3/3677 G09G2300/0443 G09G2320/028 G09G2300/0852 G09G2310/0251 G09G2320/0233 G09G2300/0842		
优先权	097120266 2008-05-30 TW		
外部链接	Espacenet USPTO		

摘要(译)

液晶显示面板包括多个像素，并且每个像素包括第一子像素和第二子像素。第一子像素和第二子像素分别根据第一栅极脉冲和第二栅极脉冲分别加载源极电压。第二子像素包括第一存储电容器和第一补偿电容器。在根据第二栅极脉冲利用第一存储电容器执行电荷中和之前，第一补偿电容器充电或放电到预定电压。