US 20020126246A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0126246 A1

Oh et al. (43) Pub. Date: Sep. 12, 2002

(54) IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

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(21) Appl. No.: 09/846,324

(22) Filed: May 2, 2001

Related U.S. Application Data

(63) Continuation of application No. 09/079,895, filed on May 15, 1998, now Pat. No. 6,281,957.

(30) Foreign Application Priority Data

May 19, 1997 (KR) 1997-19201

Publication Classification

(51) Int. Cl.[7] G02F 1/1343

(52) U.S. Cl. 349/141

(57) ABSTRACT

An in-plane switching mode liquid crystal display device includes first and second substrates and a plurality of gate and data bus lines defining pixel regions and arranged perpendicularly and/or horizontally on the first substrate. A common line is formed with the gate bus line, and a plurality of thin film transistors are formed at respective crossing areas of the gate and data bus lines. A plurality of gate electrodes are connected to the gate bus lines, and a gate insulator having a contact hole on the gate electrodes. A transparent first metal layer including a plurality of first electrodes is on the gate insulator. A passivation layer having a contact hole is on the first metal layer. A transparent second metal layer including a plurality of second electrodes is on the passivation layer. A black matrix for preventing light from leaking around the thin film transistor, the gate bus line, and data bus line is on the second substrate. A color filter layer is on the second substrate, and a liquid crystal layer is between the first and second substrates.

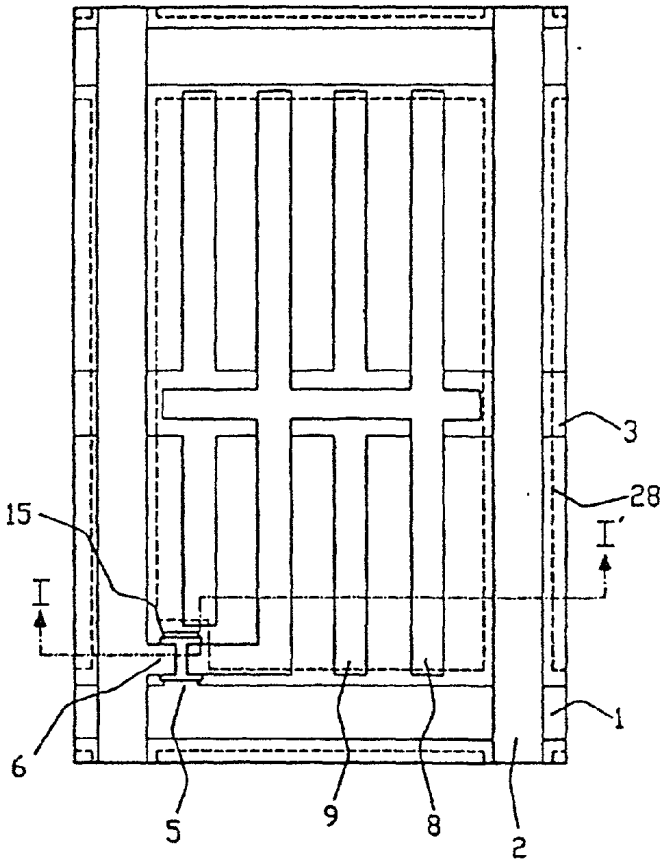


FIG. 1A
PRIOR ART

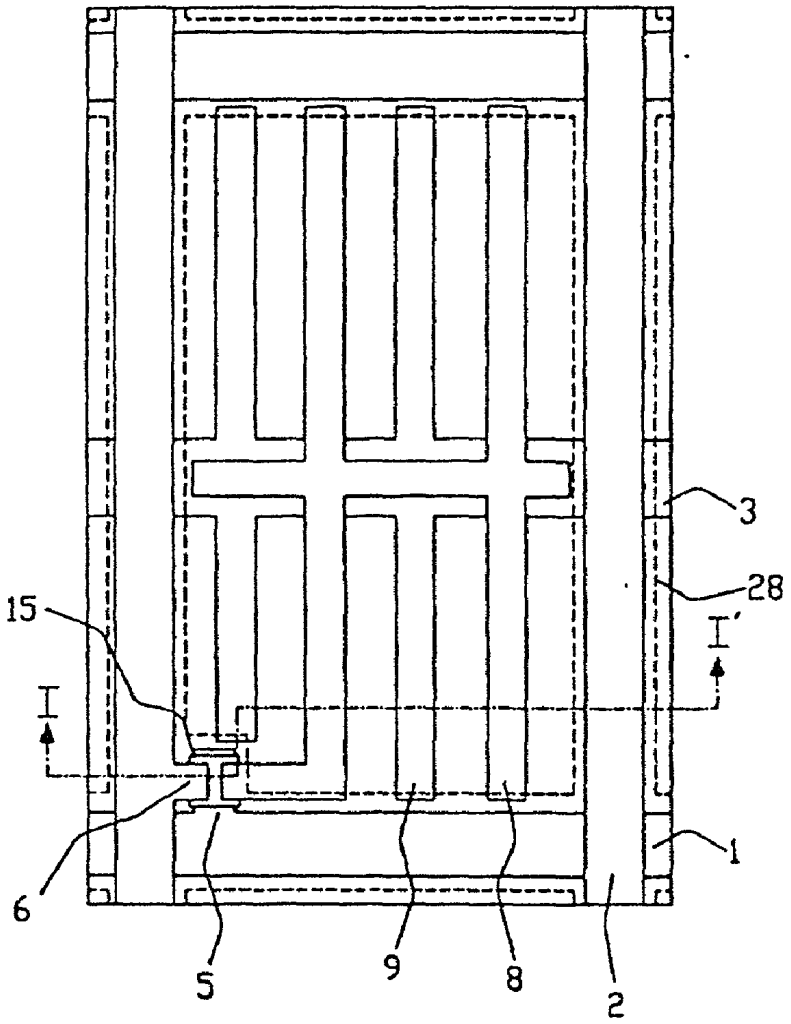


FIG. 1B
PRIOR ART

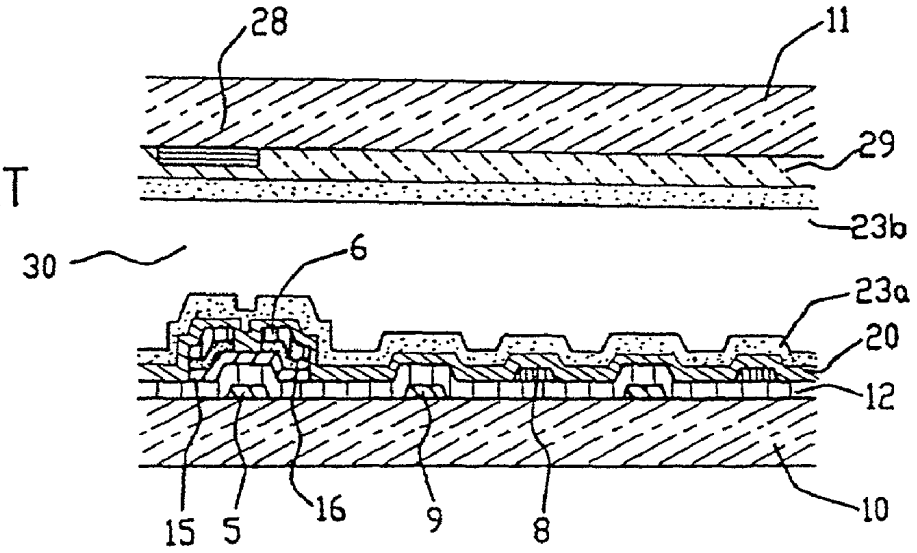


FIG. 2A

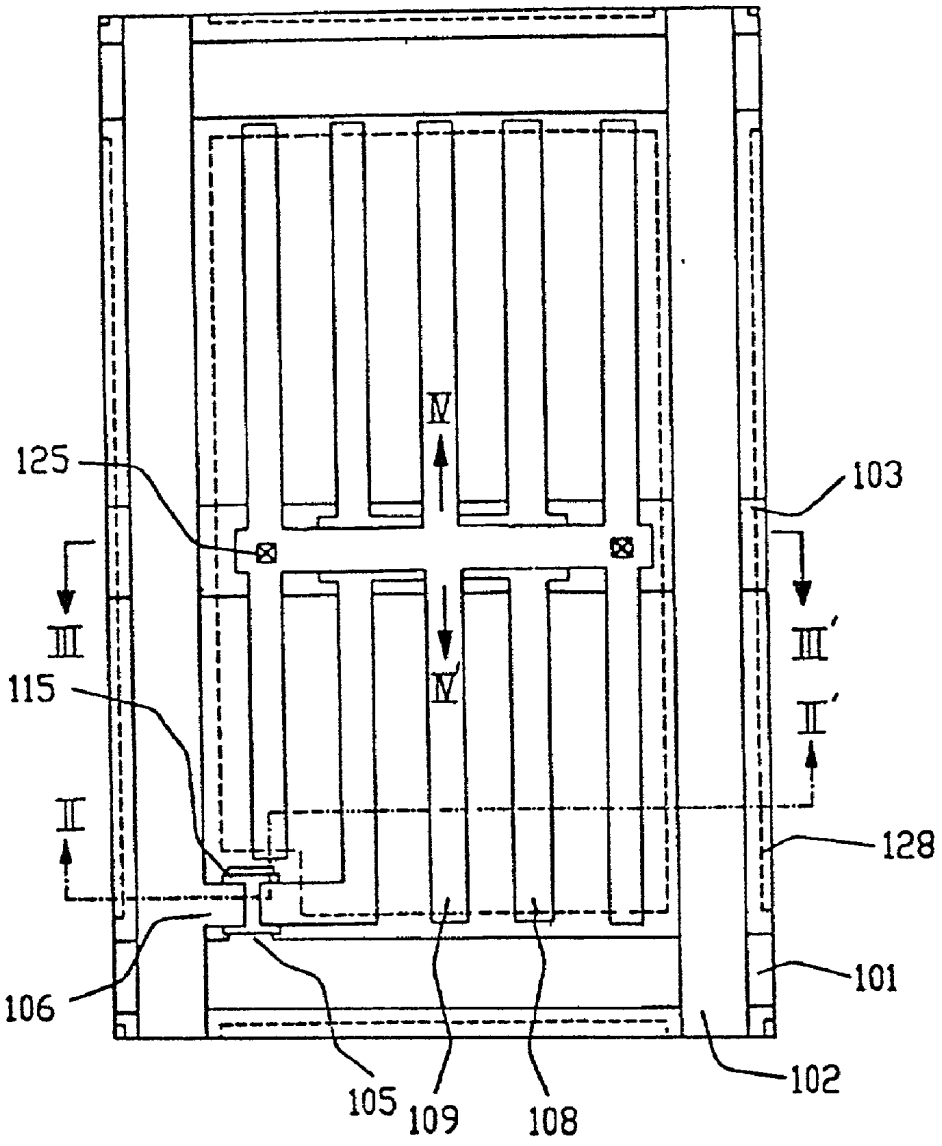

125
103
Ⅳ
Ⅲ
Ⅲ′
115
Ⅳ′
Ⅱ′
Ⅱ
128
106
101
105
109
108
102

FIG. 2B

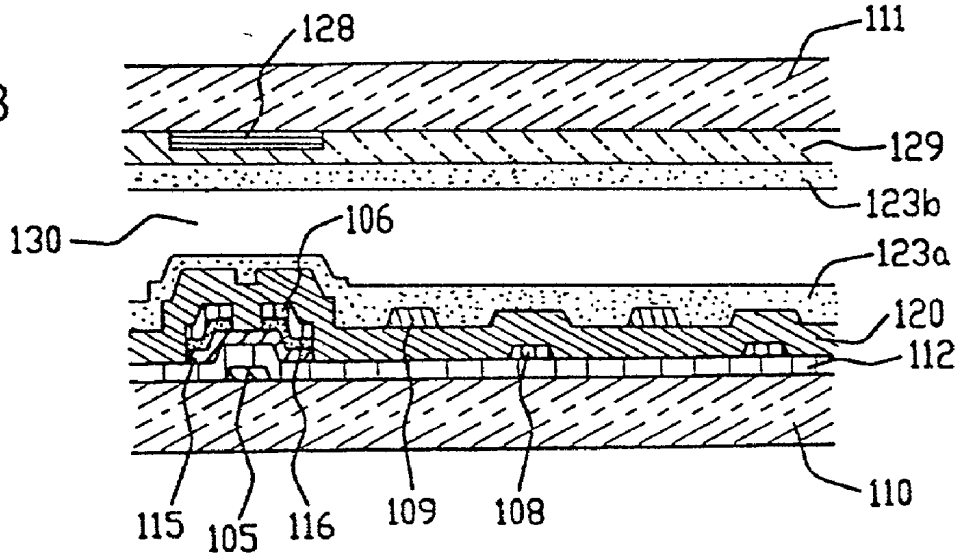

128
111
129
123b
130
106
123a
120
112
115
105
116
109
108
110

FIG. 2C

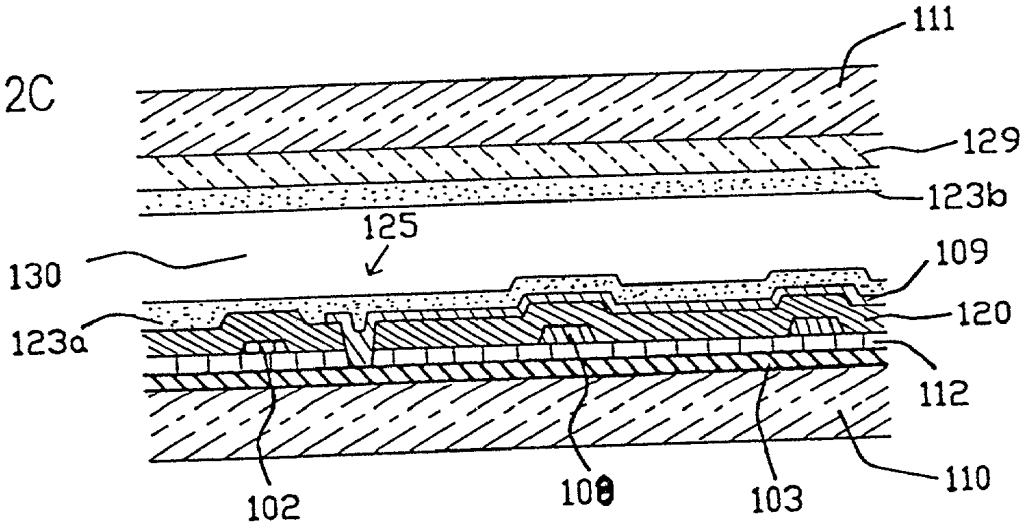

111
129
123b
125
130
109
123a
120
112
110
102
108
103

FIG. 2D

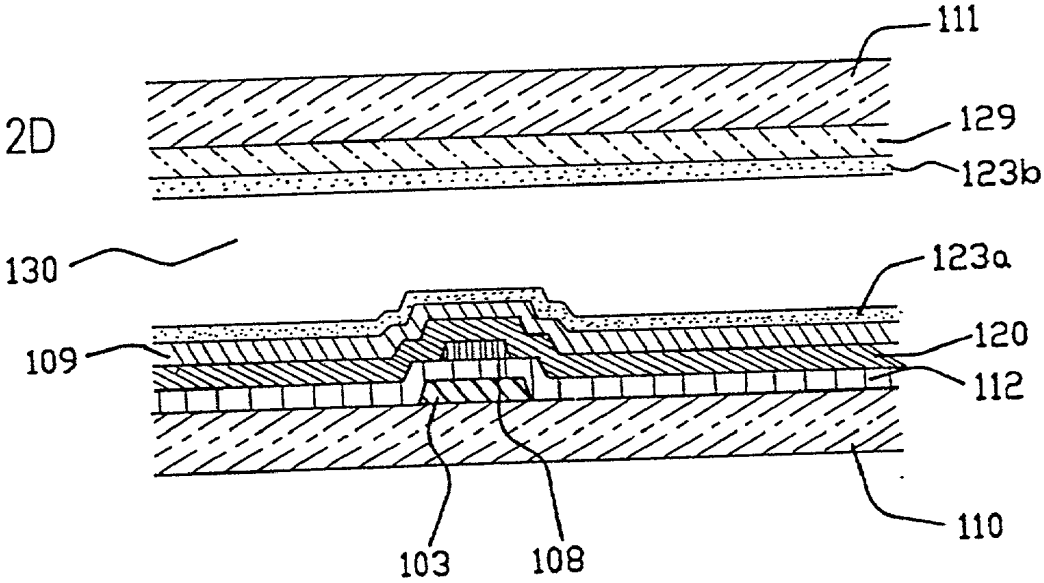

111
129
123b
130
123a
109
120
112
110
103
108

FIG. 3A

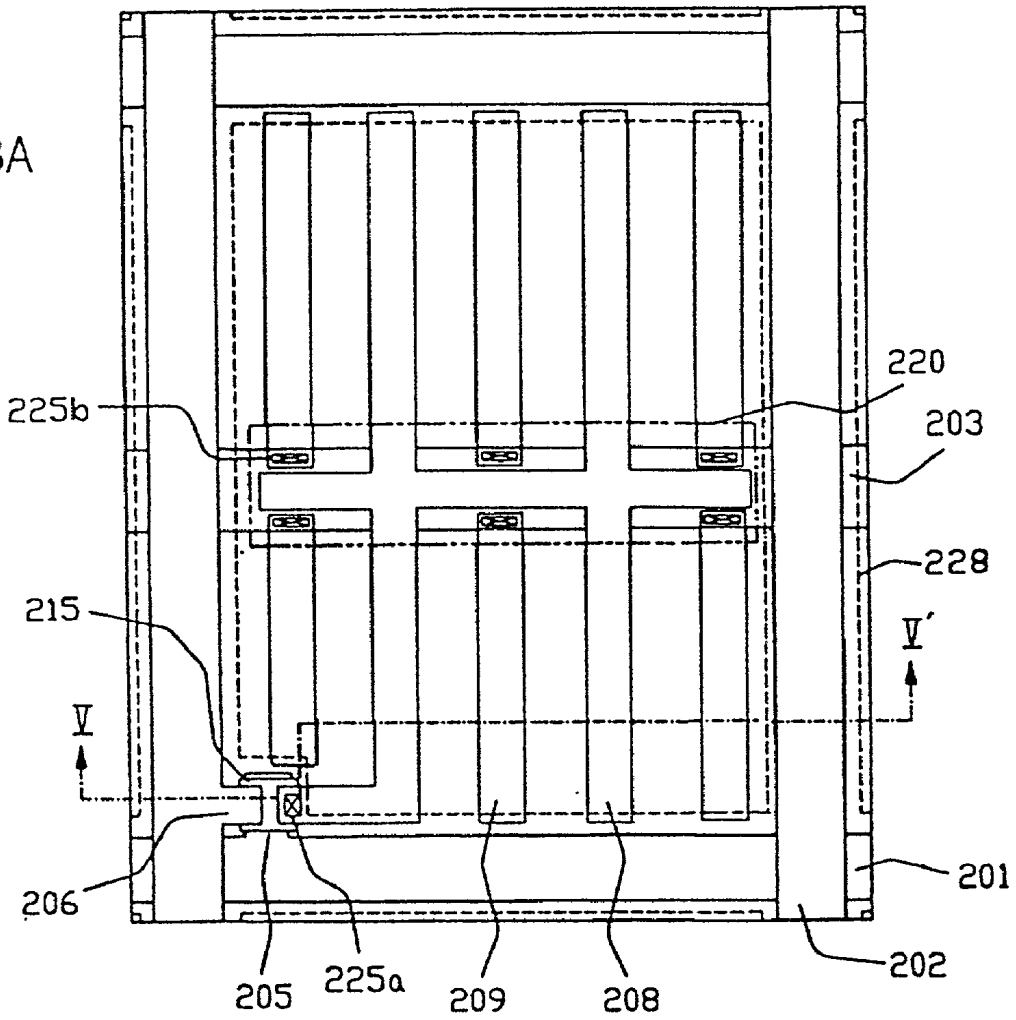
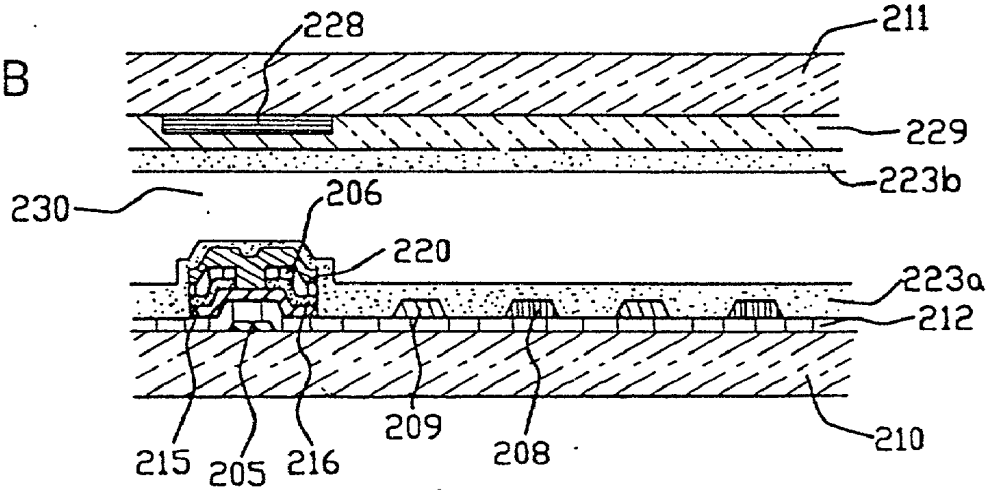

220
225b
203
228
215
V'
V
206
201
205
225a
209
208
202

FIG. 3B


228
211
229
223b
230
206
220
223a
212
215
205
216
209
208
210

IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

[0001] This application claims the benefit of Korean Application No. 1997-19201, filed on May 19, 1997, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display device, and more particularly, to a wide viewing angle in-plane switching mode liquid crystal display device.

[0004] 2. Discussion of the Related Art

[0005] Twisted nematic liquid crystal display devices(hereinafter TN LCDs) having high image quality and low consumption electric power are widely applied to flat panel display devices. TN LCDs, however, have a narrow viewing angle due to refractive anisotropy of liquid crystal molecules. This is because prior to applying voltage, liquid crystal molecules are horizontally aligned relative to the substrate but become nearly vertically aligned relative to the substrate when voltage is applied to a liquid crystal panel.

[0006] Recently, in-plane switching mode liquid crystal display devices(hereinafter IPS-LCDs) have been widely studied in which viewing angle characteristic is improved and the liquid crystal molecules are nearly horizontally aligned.

[0007] **FIG. 1A** is a plan view of a unit pixel of a conventional IPS-LCD. As shown in the drawing, a unit pixel region is defined by a gate bus line **1** and a data bus line **2** in which the lines are arranged perpendicularly and/or horizontally in a matrix on a first substrate **10**. A common line **3** is arranged parallel to the gate bus line **1** in the pixel region. A thin film transistor(TFT) is formed of a crossing area of the data bus line **2** and the gate bus line **1**. As shown in **FIG. 1B** which is a sectional view taken along line I-I' of **FIG. 1A**, the TFT includes a gate electrode **5**, a gate insulator **12**, a semiconductor layer **15**, a channel layer **16**, and source/drain electrode **6**. The gate electrode **5** is connected to the gate bus line **1**, and the source/drain electrode **6** is connected to the data bus line **2**. The gate insulator **12** is formed on the entire surface of the first substrate **10**.

[0008] A common electrode **9** and a data electrode **8** are formed in the pixel region. The common electrode **9** is formed with the gate electrode **5** and connected to the common line **3**. The data electrode **8** is formed with the source/drain electrode **6** and electrically connected to the source/drain electrode **6**. Further, a passivation layer **20** and a first alignment layer **23***a* are deposited on the entire surface of the first substrate **10**.

[0009] On a second substrate **11**, a black matrix **28** is formed to prevent a light leakage which may be generated around TFT, the gate bus line **1**, and the data bus line **2**. A color filter layer **29**, and a second alignment layer **23***b* are formed on the black matrix **28** in sequence. Also, a liquid crystal layer **30** is formed between the first and second substrates **10**, **11**. When voltage is not applied to LCD having the above structure, liquid crystal molecules in the liquid crystal layer **30** are aligned according to alignment directions of the first and second alignment layers **23***a*, **23***b*, but when voltage is applied between the common electrode **9** and the data electrode **8**, the liquid crystal molecules are vertically aligned to extending directions of the common and data electrode. As in the foregoing, since liquid crystal molecules in the liquid crystal layer **30** are switched on the same plane at all times, a grey inversion is not created in the viewing angle directions of up and down direction, and right and left direction.

[0010] However, in the conventional LCD having the above structure, an aperature ratio is less than desired because the data electrode and the common electrode are opaque. Also, since a short by coupling the common electrode and said gate bus line in the manufacturing process of the LCD is often generated, the yield goes downed. Further, for the gate insulator and the passivation layer between the data electrode and the common electrode, a high driving voltage for switching liquid crystal molecules is required.

SUMMARY OF THE INVENTION

[0011] Accordingly, the present invention is directed to an plane switchin mode liquid crystal display device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0012] An object of the present invention is to provide an LCD having a high aperature ratio.

[0013] Another object of the present invention is to increase the yield of an LCD.

[0014] Additional features and advantages of the present invention will be set forth in the description which follows, and will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure and process particularly pointed out in the written description as well as in the appended claims.

[0015] To achieve these an other advantages, and in accordance with the purpose of the present invention, as embodied and broadly described, in a first aspect of the present invention there is provided an in-plane switching mode liquid crystal display device comprising first and second substrates; a plurality of gate and data bus lines defining pixel regions and arranged on said first substrate; a common line formed with said gate bus line; a plurality of thin film transistors formed at respective crossing areas of said gate and data bus lines, gate electrodes of said transistors being connected to said gate bus lines, respectively; a gate insulator having a contact hole on said gate electrodes; a transparent first metal layer including a plurality of first electrodes on said gate insulator; a passivation layer having a contact hole on said transparent first metal layer; and a transparent second metal layer including a plurality of second electrodes on said passivation layer, said second electrodes producing plane electric fields together with said first electrodes.

[0016] In another aspect of the present invention, an in-plane switching mode liquid crystal display device comprises first and second substrates; a plurality of gate and data bus lines defining pixel regions and arranged on said first substrate; a common line formed with said gate bus line; a plurality of thin film transistors formed at respective crossing areas of said gate and data bus lines, gate electrodes of said transistors being connected to said gate bus lines, respectively; a gate insulator having a contact hole on said

gate electrodes; a transparent first metal layer including a plurality of first electrodes and a transparent second metal layer including a plurality of second electrodes on said gate insulator, said second electrodes producing plane electric fields together with said first electrodes on said gate insulator; and a passivation layer on said common line and said thin film transistors.

[0017] In anther aspect of the present invention, a method of forming an in-plane switching mode liquid crystal display device comprises the steps of forming first and second substrates; forming a plurality of gate and data bus lines defining pixel regions and arranged on said first substrate; forming a common line formed with said gate bus line; forming a plurality of thin film transistors formed at respective crossing areas of said gate and data bus lines, gate electrodes of said transistors being connected to said gate bus lines, respectively; forming a gate insulator having a contact hole on said gate electrodes; forming a transparent first metal layer including a plurality of first electrodes on said gate insulator; forming passivation layer having a contact hole on said transparent first metal layer; and forming transparent second metal layer including a plurality of second electrodes on said passivation layer, said second electrodes producing plane electric fields together with said first electrodes.

[0018] In a further aspect of the present invention, a method of forming an in-plane switching mode liquid crystal display device comprises the steps of forming first and second substrates; forming a plurality of gate and data bus lines defining pixel regions and arranged on said first substrate; forming a common line formed with said gate bus line; forming a plurality of thin film transistors formed at respective crossing areas of said gate and data bus lines, gate electrodes of said transistors being connected to said gate bus lines, respectively; forming a gate insulator having a contact hole on said gate electrodes; forming a transparent first metal layer including a plurality of first electrodes and a transparent second metal layer including a plurality of second electrodes on said gate insulator, said second electrodes producing plane electric fields together with said first electrodes on said gate insulator; and forming a passivation layer on said common line and said thin film transistors.

[0019] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0021] In the drawings:

[0022] **FIG. 1A** is a plan view of a unit pixel of a conventional in-plane switching mode LCD;

[0023] **FIG. 1B** is a sectional view taken along line I-I' of **FIG. 1A**;

[0024] **FIG. 2A** is a plan view of a unit pixel of an LCD according to a first embodiment of the present invention;

[0025] **FIG. 2B** is a sectional view taken along line II-II' of **FIG. 2A**;

[0026] **FIG. 2C** is a sectional view taken along line III-III' of **FIG. 2A**;

[0027] **FIG. 2D** is a sectional view taken along line IV-IV' of **FIG. 2A**;

[0028] **FIG. 3A** is a plan view of a unit pixel of an LCD according to a second embodiment of the present invention; and

[0029] **FIG. 3B** is a sectional view taken along line V-V' of **FIG. 3A**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] The present invention preferably comprises first and second substrates, data and gate bus lines defining pixel region on the first substrate in which the lines are arranged perpendicularly and/or horizontally in a matrix, common lines formed parallel to the gate bus lines in the pixel region, TFTs at respective crossing areas of the data bus lines and the gate bus lines in the pixel region, at least one transparent data electrode in the pixel region, a passivation layer having contact holes on the data electrode, at least one transparent common electrode parallel to the data bus lines and coupled to the common line on the passivation layer, a first alignment layer with a fixed alignment direction deposited on the passivation layer, black matrixes over the second substrate to prevent a light leakage which may be generated around TFTs, the gate bus lines, and the data bus lines, a color filter layer on the black matrix and the second substrate, a second alignment layer on the color filter layer, and a liquid crystal layer between the first and second substrates.

[0031] The transparent common electrode is coupled to the common line through the contact hole, and the data electrode is coupled to the source/drain electrode of the TFT. Although the common line and common electrode are formed in different planes in one embodiment of the present invention, the common line may be formed with the common electrode in a single process using the same material in another embodiment of the present invention. When the transparent common and data electrodes are formed on the gate insulator at the same time, the common line is formed with the gate bus line in a single process using the same material and coupled to the common electrodes on the gate insulator through contact holes. Transparent conductive sections on the gate pad and the data pad connect the gate and data bus lines to an outer driving circuit. The transparent conductive sections are preferably formed with the transparent common or data electrodes at the same time.

[0032] Further, the storage capacitor according to the present invention is preferably formed by the common bus line, the data electrode over the common bus line, and the common electrode over the data electrode.

[0033] **FIG. 2A** is a plan view of a unit pixel of a LCD according to a first embodiment of the present invention, and **FIG. 2B** is a sectional view taken along line II-II' of **FIG. 2A**. As shown in **FIGS. 2A and 2B**, gate and data bus lines **101**, **102** defining a pixel region are arranged perpendicularly and/or horizontally in a matrix on the first substrate **110**. A common line **103** is formed parallel to the gate bus

line **101**. A TFT is formed at a crossing area of the data bus line **102** and the gate bus line **101** in the pixel region.

[**0034**] As shown in **FIG. 2**B, the TFT preferably comprises a gate electrode **105**, a gate insulator **112** on the gate electrode **105**, a semiconductor layer **115** on the gate insulator **112**, a channel layer **116** on the semiconductor layer **115**, and source/drain electrode **106** on the channel layer **116**. The gate insulator **112** is preferably deposited on the entire surface of the substrate **110**.

[**0035**] The gate electrode **105** and the gate bus line **101** are preferably formed by sputtering and photoetching a metal such as Al, Mo, or Al alloy in a single process on a surface of the substrate. At this time, it is possible to form an anodic oxidation layer by anodizing the gate bus line **101** and the gate electrode **105** to improve the insulating characteristic. The gate insulator **112** preferably including an inorganic material such as SiNx or SiOx is formed by a PCVD (plasma chemical vapor deposition) method.

[**0036**] The semiconductor layer **115** is preferably formed by depositing and etching an amorphous silicon, for example, by the PCVD method, and the channel layer **116** is formed by depositing a doped amorphous silicon (n+ a-Si). The source/drain electrode **106** is preferably formed with the data electrode **108** at the same time by depositing and etching a metal such as Al, Cr, Ti, Al alloy by a sputtering method. At this time, it is possible to form each the semiconductor layer **115**, the channel layer **116**, and the source/drain electrode **106** by different processes. Also, it is possible that the semiconductor layer **115** and the channel layer **116** are formed by etching the a-Si layer and the n^+a-Si layer after continually depositing the a-Si layer and the n^+a-Si layer on the gate insulator **112**. Furthermore, an etch stopper may be formed on the semiconductor layer **115** to prevent the channel region from being undesirably etched.

[**0037**] The common electrode **109** is formed on a passivation layer **120** including an inorganic material such as SiNx or SiOx, or organic material such as BCB (benzocyclobutene) by depositing and etching a transparent metal such as ITO (indium tin oxide) by using a sputtering method. Further, the first alignment layer **123***a* is formed on the passivation layer **120** and the common electrode **109**.

[**0038**] On the second substrate **111**, black matrix **128** for preventing a light leakage which may be generated around TFTs, the gate bus lines **101**, and the data bus lines **102**, a color filter layer **129**, and a second alignment layer **123***b* is formed on the second substrate. A color filter layer **129**, and a second alignment layer **123***b* are formed on the black matrix **128** in sequence. A liquid crystal layer **130** is formed between the first and second substrates. Further, an overcoat layer (not illustrated) may be formed on said color filter layer **129**.

[**0039**] **FIG. 2C** is a sectional view taken along line III-III' of **FIG. 2**A, and **FIG. 2D** is a sectional view taken along line IV-IV' of **FIG. 2A**. As shown in **FIGS. 2C and 2D**, the common electrode **109** connected to the common line **103** through a contact hole **125**. In this case, a storage capacitor is formed by the common line **103** and the data electrode **108**, and another storage capacitor is formed by the data electrode **108** and the common electrode **109**. As a result, the aperture ratio is increased by the amount of decrease in the width of the common line **103**.

[**0040**] **FIG. 3A** is a plan view of a unit pixel of a LCD according to a second embodiment of the present invention, and **FIG. 3B** is a sectional view taken along the V-V' of **FIG. 3A**.

[**0041**] A difference between the second embodiment and the first embodiment is that in the second embodiment, transparent common electrodes **209** and transparent data electrodes **208** are formed on a gate insulator **212**, thereby improving the aperture ratio. As shown in **FIG. 3A, a** passivation layer **220** including an inorganic material such as SiNx or SiOx, or organic material such as BCB is formed around a common line **203**. Each of the common electrodes **209** is connected to the common line **203** through a contact hole **225***b*. As shown in **FIG. 3**B, since the passivation layer **220** also formed in the TFT region as well as around the common lain **203**, the data electrode **208** is connected to a source/drain electrode **206** through a contact hole **225***a*.

[**0042**] In accordance with the embodiments of the present invention, since the transparent common electrode and the transparent data electrode are formed on the gate insulator at the same time, aperature ratio is increased and a plane electric field is achieved. Further, since a strong plane electric field is applied onto the liquid crystal layer where the passivation in the pixel region is removed, it is possible to obtain an improved viewing angle and prevent a break down of the moving image by making the liquid crystal molecules to switch fast.

[**0043**] While the invention on has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An in-plane switching mode liquid crystal display device comprising:

first and second substrates;

a plurality of gate and data bus lines defining pixel regions and arranged on said first substrate;

a common line formed with said gate bus line;

a plurality of thin film transistors formed at respective crossing areas of said gate and data bus lines, gate electrodes of said transistors being connected to said gate bus lines, respectively;

a gate insulator having a contact hole on said gate electrodes;

a transparent first metal layer including a plurality of first electrodes on said gate insulator;

a passivation layer having a contact hole on said transparent first metal layer; and

a transparent second metal layer including a plurality of second electrodes on said passivation layer, said second electrodes producing plane electric fields together with said first electrodes.

2. The in-plane switching mode liquid crystal display device according to claim 1, wherein said common line and

said transparent first metal layer form a first storage capacitor, and said transparent first metal layer and said transparent second metal layer form a second storage capacitor.

3. The in-plane switching mode liquid crystal display device according to claim 1, wherein each of said thin film transistors comprises a semi-conductor layer on said gate insulator, a channel layer on said semiconductor layer, and source and drain electrodes on said channel layer, one of said source and drain electrodes being connected to said data bus lines.

4. The in-plane switching mode liquid crystal display device according to claim 1, wherein said transparent first electrodes include data electrodes and said transparent second electrodes include common electrodes.

5. The in-plane switching mode liquid crystal display device according to claim 1, wherein said transparent first and second metal layers include indium tin oxide.

6. The in-plane switching mode liquid crystal display device according to claim 1, further comprising a first alignment layer over said first substrate.

7. The in-plane switching mode liquid crystal display device according to claim 6, wherein said first alignment layer includes one of polyimide, polyamide, and photosensitive material.

8. The in-plane switching mode liquid crystal display device according to claim 7, wherein said photosensitive material is selected from the group consisting of polyvinylcinnamate and polysiloxanecinnamate.

9. The in-plane switching mode liquid crystal display device according to claim 1, further comprising:

a black matrix for preventing light from leaking around said thin film transistor, said gate bus line, and data bus line;

a color filter layer on said second substrate; and

a liquid crystal layer between said first and second substrates.

10. The in-plane switching mode liquid crystal display device according to claim 9, further comprising an overcoat layer on said color filter layer.

11. The in-plane switching mode liquid crystal display device according to claim 1, further comprising a second alignment layer on said second substrate.

12. The in-plane switching mode liquid crystal display device according to claim 11, wherein said second alignment layer includes one of polyimide, polyamide, and photosensitive material.

13. The in-plane switching mode liquid crystal display device according to claim 12, wherein said photosensitive material is selected from the group consisting of polyvinylcinnamate and polysiloxanecinnamate.

14. An in-plane switching mode liquid crystal display device comprising:

first and second substrates;

a plurality of gate and data bus lines defining pixel regions and arranged on said first substrate;

a common line formed with said gate bus line;

a plurality of thin film transistors formed at respective crossing areas of said gate and data bus lines, gate electrodes of said transistors being connected to said gate bus lines, respectively;

a gate insulator having a contact hole on said gate electrodes;

a transparent first metal layer including a plurality of first electrodes and a transparent second metal layer including a plurality of second electrodes on said gate insulator, said second electrodes producing plane electric fields together with said first electrodes on said gate insulator; and

a passivation layer on said common line and said thin film transistors.

15. The in-plane switching mode liquid crystal display device according to claim 14, wherein said common line and said transparent first metal layer form a first storage capacitor, and said transparent first metal layer and said transparent second metal layer form a second storage capacitor.

16. The in-plane switching mode liquid crystal display device according to claim 14, wherein each of said thin film transistors comprises a semiconductor layer on said gate insulator, a channel layer on said semiconductor layer, and source and drain electrodes on said channel layer one of said source and drain electrodes being connected to said data bus lines.

17. The in-plane switching mode liquid crystal display device according to claim 14, wherein said transparent first electrodes include data electrodes and said transparent second electrodes include common electrodes.

18. The in-plane switching mode liquid crystal display device according to claim 14, wherein said transparent first and second metal layers include indium tin oxide.

19. The in-plane switching mode liquid crystal display device according to claim 14, further comprising a first alignment layer over said first substrate.

20. The in-plane switching mode liquid crystal display device according to claim 19, wherein said first alignment layer includes one of polyimide, polyamide, and photosensitive material.

21. The in-plane switching mode liquid crystal display device according to claim 20, wherein said photosensitive material is selected from the group consisting of polyvinylcinnamate and polysiloxanecinnamate.

22. The in-plane switching mode liquid crystal display device according to claim 14, further comprising:

a black matrix for preventing light from leaking around said thin film transistor, said gate bus line, and data bus line;

a color filter layer on said second substrate; and

a liquid crystal layer between said first and second substrates.

23. The in-plane switching mode liquid crystal display device according to claim 22, further comprising an overcoat layer on said color filter layer.

24. The in-plane switching mode liquid crystal display device according to claim 14, further comprising a second alignment layer on said second substrate.

25. The in-plane switching mode liquid crystal display device according to claim 24, wherein said second alignment layer includes one of polyimide, polyamide, and photosensitive material.

26. The in-plane switching mode liquid crystal display device according to claim 25, wherein said photosensitive material is selected from the group consisting of polyvinylcinnamate and polysiloxanecinnamate.

27. The in-plane switching mode liquid display device according to claim 14, wherein said passivation layer is substantially only on the thin film transistors and the common line.

28. A method of forming an in-plane switching mode liquid crystal display device, the method comprising the steps of:

forming first and second substrates;

forming a plurality of gate and data bus lines defining pixel regions and arranged on said first substrate;

forming a common line formed with said gate bus line;

forming a plurality of thin film transistors formed at respective crossing areas of said gate and data bus lines, gate electrodes of said transistors being connected to said gate bus lines, respectively;

forming a gate insulator having a contact hole on said gate electrodes;

forming a transparent first metal layer including a plurality of first electrodes on said gate insulator;

forming passivation layer having a contact hole on said transparent first metal layer; and

forming transparent second metal layer including a plurality of second electrodes on said passivation layer, said second electrodes producing plane electric fields together with said first electrodes.

29. The method according to claim 28, wherein said common line and said transparent first metal layer form a first storage capacitor, and said transparent first metal layer and said transparent second metal layer form a second storage capacitor.

30. The method according to claim 28, wherein each of said thin film transistors comprises a semiconductor layer on said gate insulator, a channel layer on said semiconductor layer, and source and drain electrodes on said channel layer, one of said source and drain electrodes being connected to said data bus lines.

31. The method according to claim 28, wherein said transparent first electrodes include data electrodes and said transparent second electrodes include common electrodes.

32. The method according to claim 28, wherein said transparent first and second metal layers include indium tin oxide.

33. The method according to claim 28, further comprising the step of forming a first alignment layer over said first substrate.

34. The method according to claim 33, wherein said first alignment layer includes one of polyimide, polyamide, and photosensitive material.

35. The method according to claim 34, wherein said photosensitive material is selected from the group consisting of polyvinylcinnamate and polysiloxanecinnamate.

36. The method according to claim 1, further comprising the steps of:

forming a black matrix for preventing light from leaking around said thin film transistor, said gate bus line, and data bus line;

forming a color filter layer on said second substrate; and

forming a liquid crystal layer between said first and second substrates.

37. The method according to claim 36, further comprising the step of forming an overcoat layer on said color filter layer.

38. The method according to claim 28, further comprising the step of forming a second alignment layer on said second substrate.

39. The method according to claim 38, wherein said second alignment layer includes one of polyimide, polyamide, and photosensitive material.

40. The method according to claim 39, wherein said photosensitive material is selected from the group consisting of polyvinylcinnamate and polysiloxanecinnamate.

41. A method of forming an in-plane switching mode liquid crystal display device, the method comprising the steps of:

forming first and second substrates;

forming a plurality of gate and data bus lines defining pixel regions and arranged on said first substrate;

forming a common line formed with said gate bus line;

forming a plurality of thin film transistors formed at respective crossing areas of said gate and data bus lines, gate electrodes of said transistors being connected to said gate bus lines, respectively;

forming a gate insulator having a contact hole on said gate electrodes;

forming a transparent first metal layer including a plurality of first electrodes and a transparent second metal layer including a plurality of second electrodes on said gate insulator, said second electrodes producing plane electric fields together with said first electrodes on said gate insulator; and

forming a passivation layer on said common line and said thin film transistors.

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专利名称(译)	面内切换模式液晶显示装置		
公开(公告)号	US20020126246A1	公开(公告)日	2002-09-12
申请号	US09/846324	申请日	2001-05-02
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IPC分类号	G02F1/1343		
CPC分类号	G02F1/134363		
优先权	1019970019201 1997-05-19 KR		
其他公开文献	US6665036		
外部链接	Espacenet USPTO		

摘要(译)

面内切换模式液晶显示装置包括第一和第二基板以及限定像素区域并且在第一基板上垂直和/或水平布置的多个栅极和数据总线。与栅极总线形成公共线，并且在栅极线和数据总线的各个交叉区域处形成多个薄膜晶体管。多个栅电极连接到栅极总线，栅极绝缘体在栅电极上具有接触孔。包括多个第一电极的透明第一金属层位于栅极绝缘体上。具有接触孔的钝化层位于第一金属层上。包括多个第二电极的透明第二金属层位于钝化层上。用于防止光在薄膜晶体管，栅极总线和数据总线周围泄漏的黑矩阵在第二基板上。滤色器层位于第二基板上，液晶层位于第一和第二基板之间。