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(54) **LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF**

Publication Classification

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(57) **ABSTRACT**

A liquid crystal display includes m valid gate lines G1 to Gm arranged in a first direction with first constant intervals between gate lines, n valid data lines arranged in a second direction perpendicular to the valid gate lines with second constant intervals between data lines, and at least one dummy data line at a periphery of and in parallel with the n valid data lines. A method of driving a liquid crystal display is carried out by a general procedure of shorting the dummy data lines with a specific data line or by applying the same driving signals of a specific data line to the dummy data line.

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Dec. 27, 2000 (KR) 2000-83095

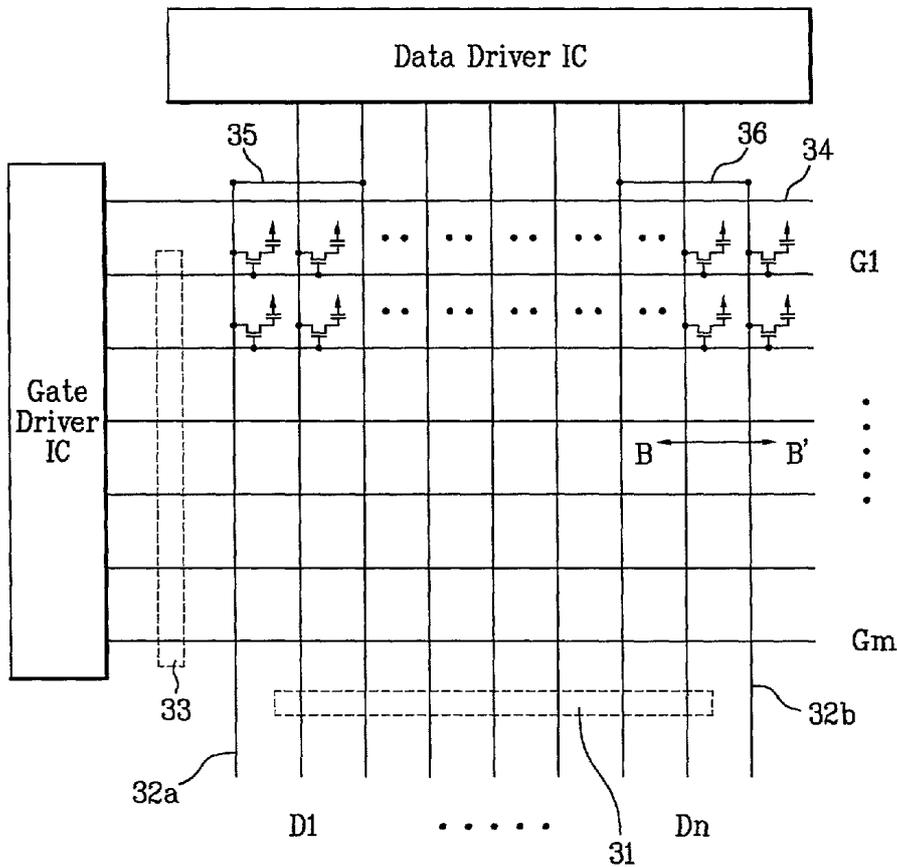


FIG. 1
Prior Art

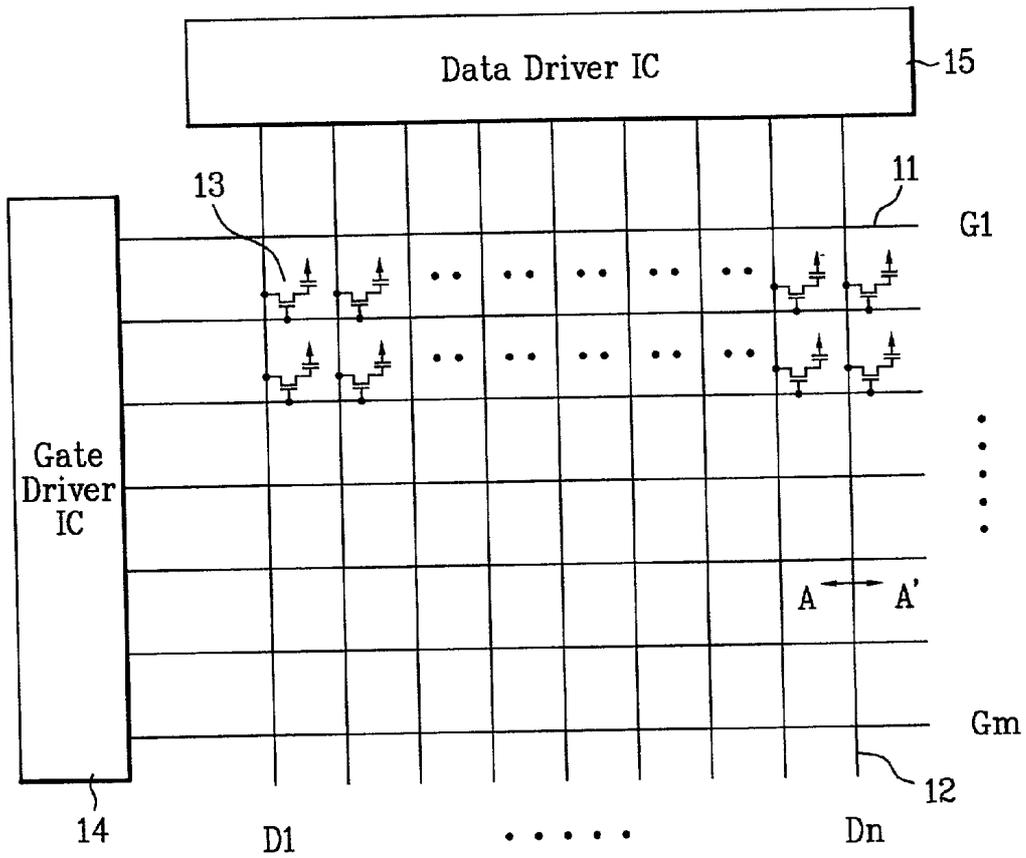


FIG. 2
Prior Art

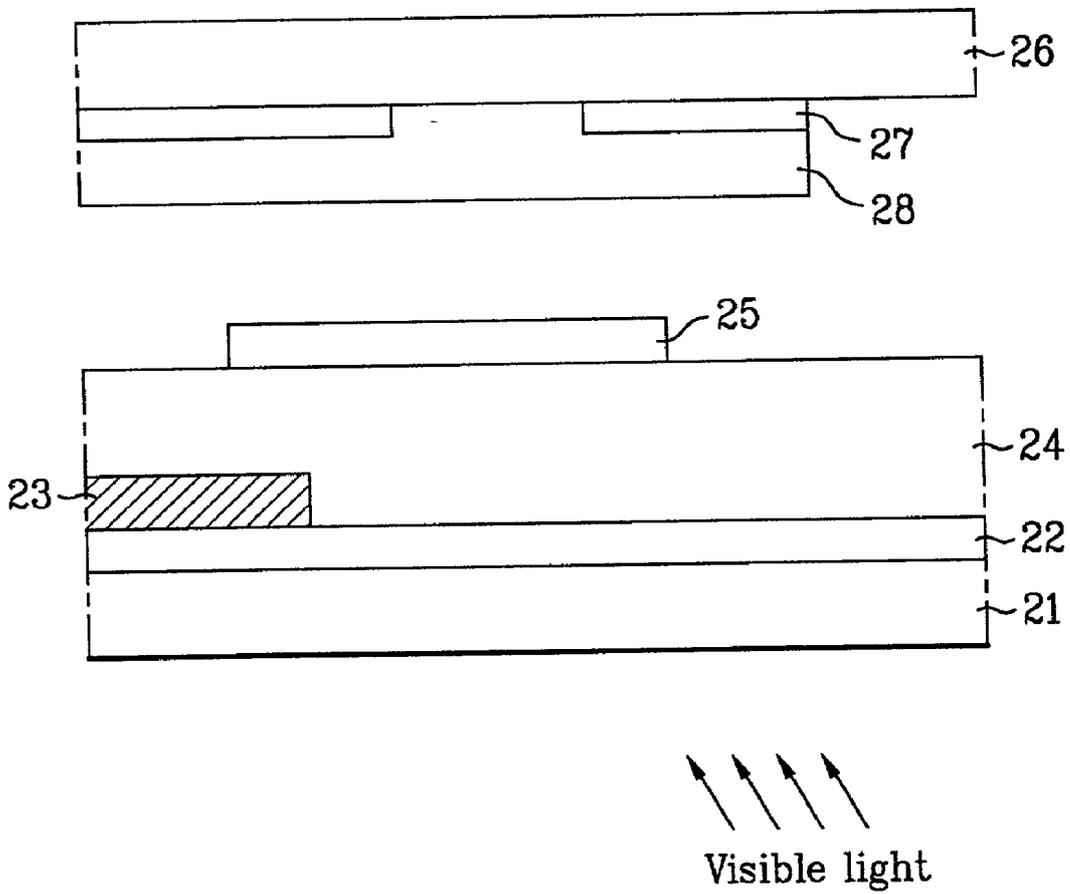


FIG. 3

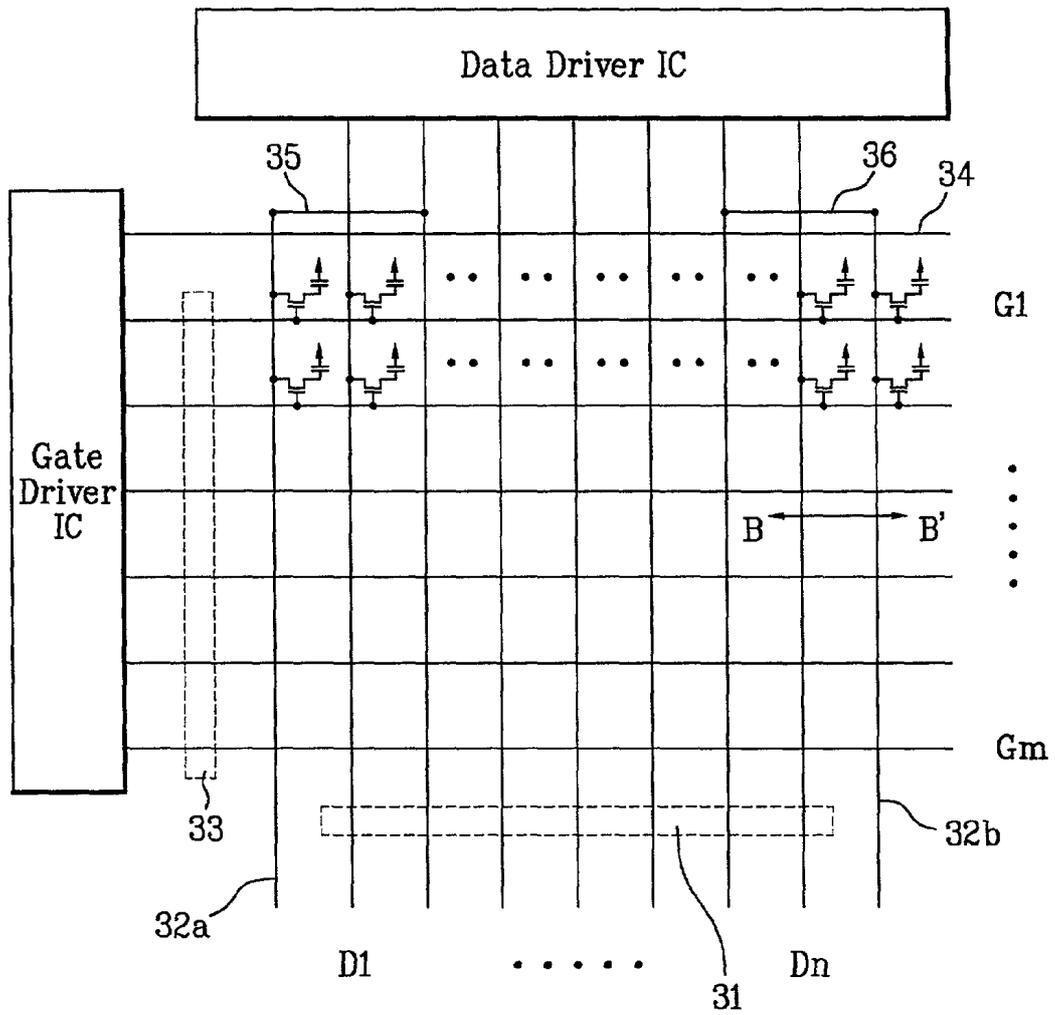


FIG. 4

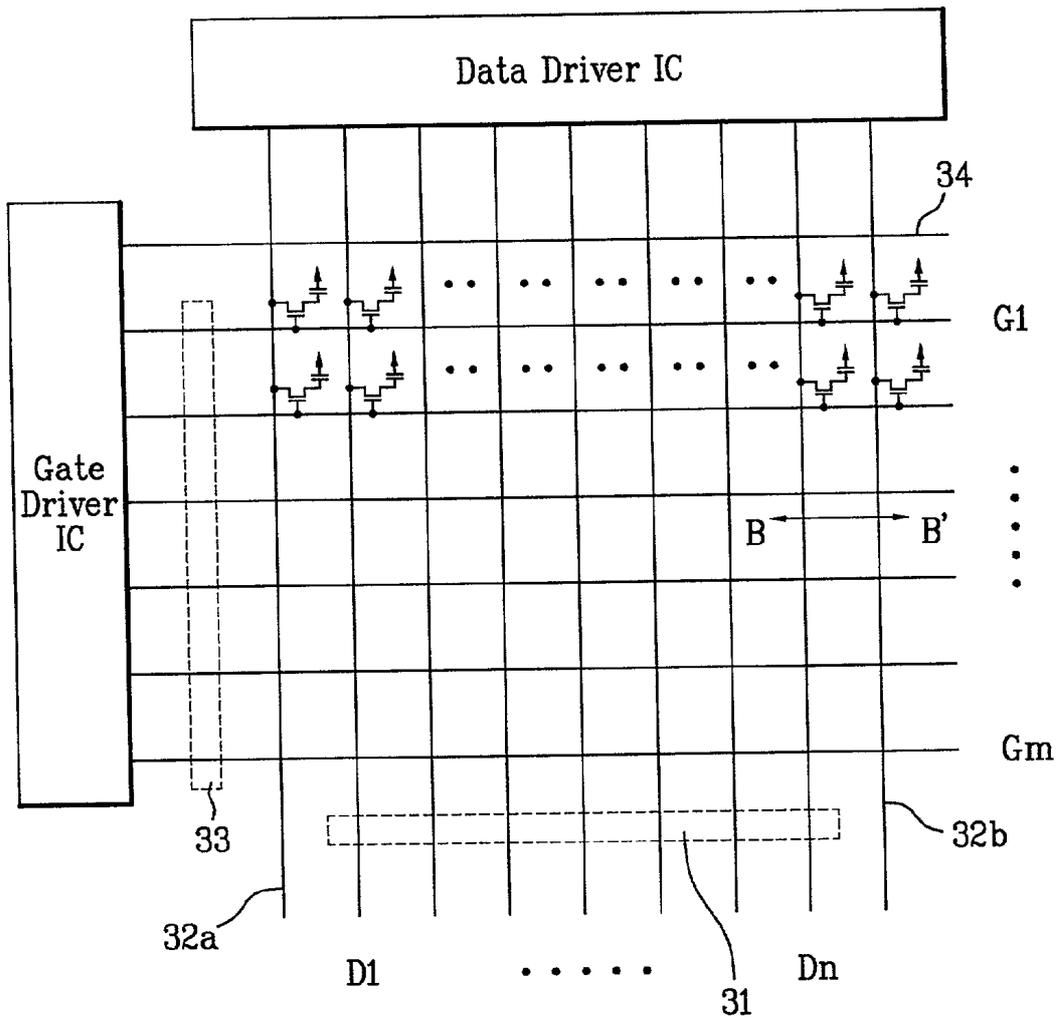


FIG. 5

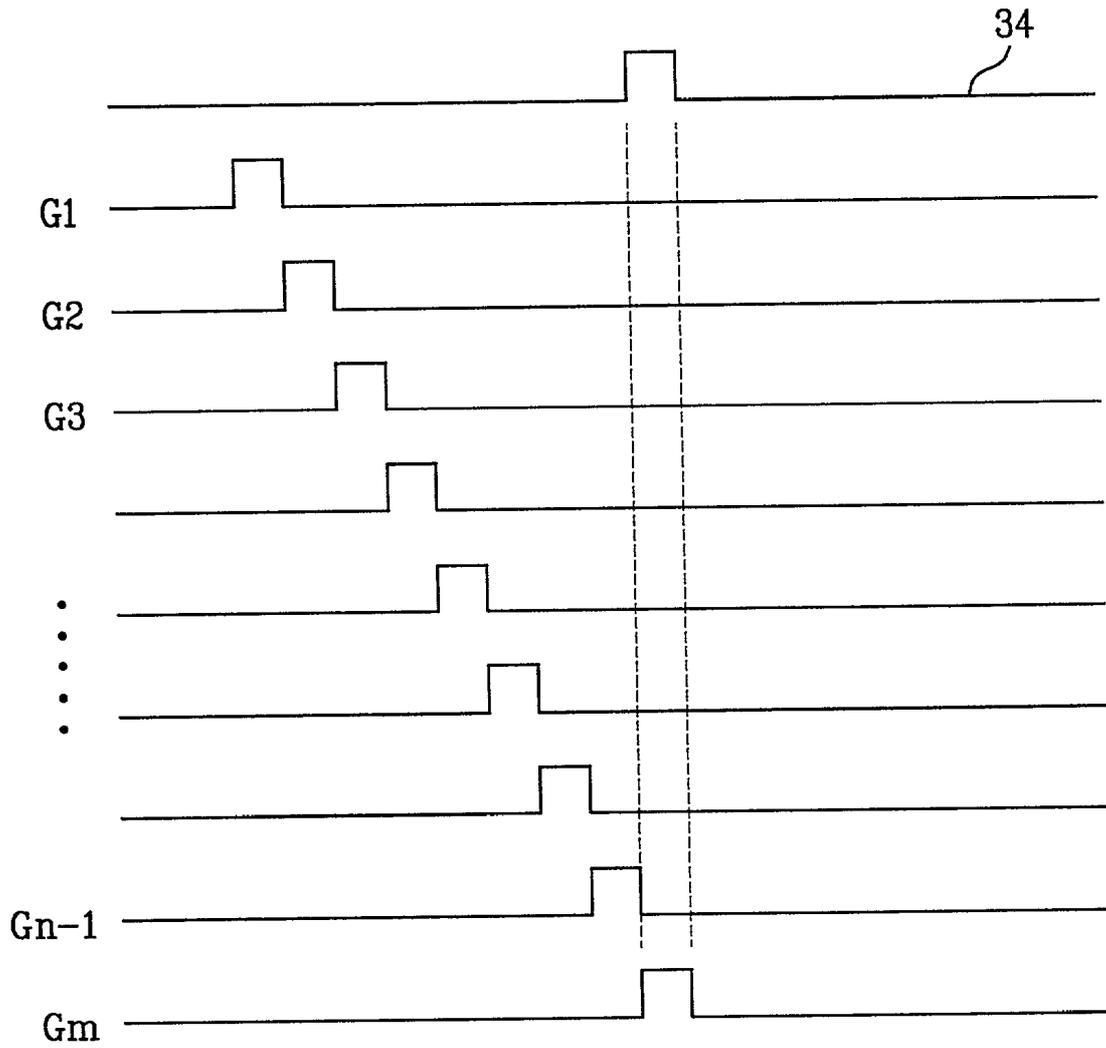


FIG. 6A

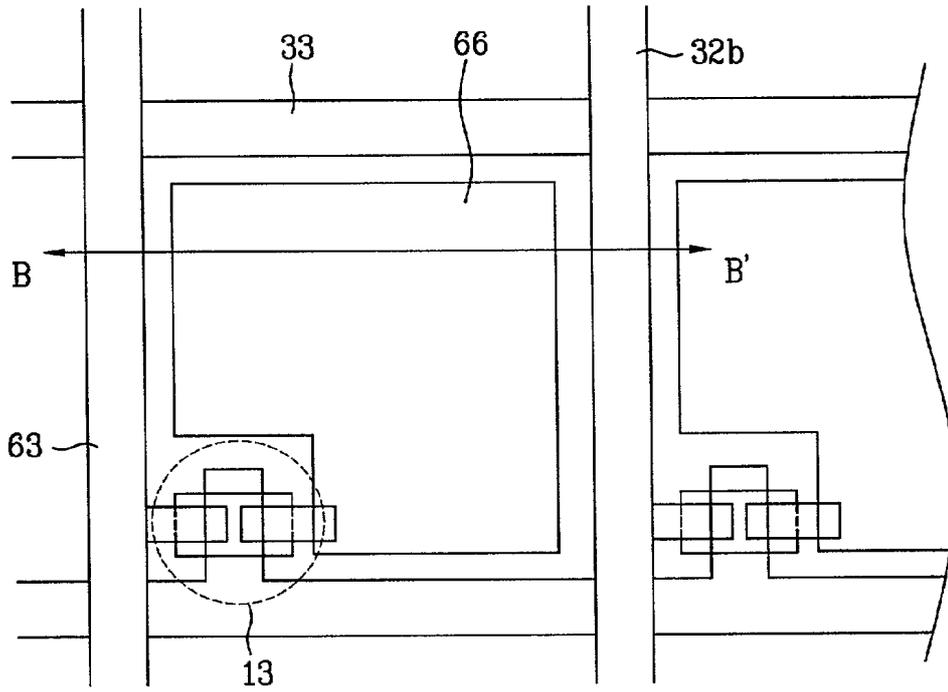
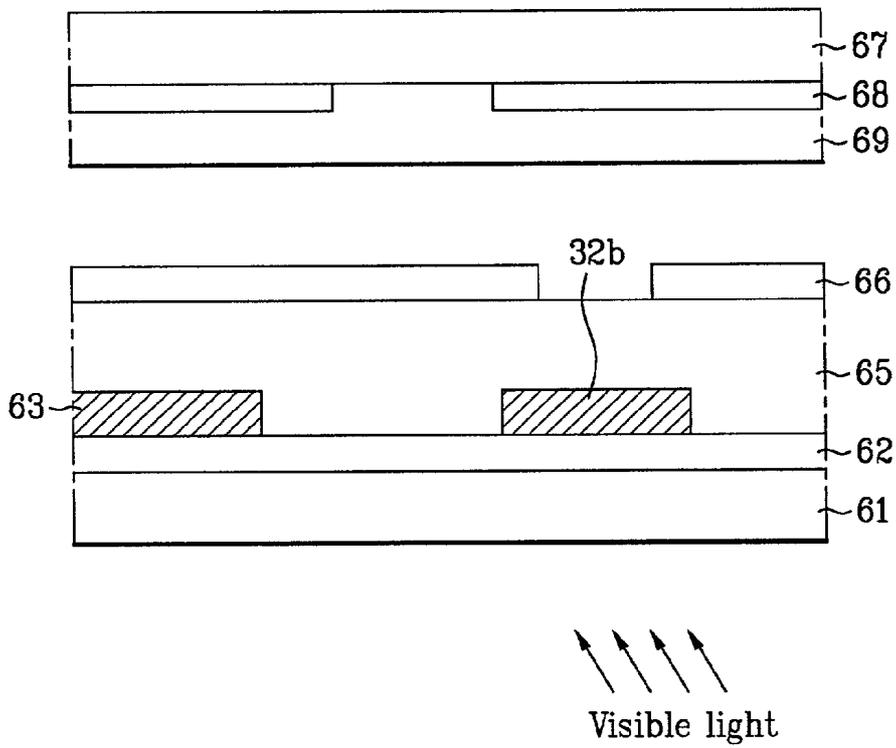


FIG. 6B



LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

[0001] This application claims the benefit of Korean Patent Application No. P2000-83095, filed on Dec. 27, 2000, the entirety of which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a displaying apparatus, and more particularly to a liquid crystal display and driving method thereof.

[0004] 2. Background of the Related Art

[0005] Generally, a liquid crystal display (LCD) includes a thin film transistor (TFT) liquid crystal display (TFT-LCD) panel, a backlight unit, and a driver. The TFT-LCD panel may have degradations as follows: first, degradation of characteristic values from standard design due to process deviations; second, degradation due to dust, poor cleaning at a film surface, and the like; and, third, degradation of characteristic variations due to static electricity and breakdown of thin film transistors or liquid crystal cells.

[0006] One of the degradations occurring in a TFT-LCD panel is the irregularity of combining a first substrate with an opposed second substrate, which results in reducing the sharpness of a displayed video or in leaking light when failing to meet the design margin.

[0007] Reference will now be made in detail to an LCD according to a related art, examples of which are illustrated in the accompanying drawings.

[0008] FIG. 1 shows a layout of an LCD according to a related art.

[0009] Referring to FIG. 1, a liquid crystal display generally comprises a number of 'm' gate lines G1 to Gm arranged in a first direction with a constant interval between the gate lines; a number of 'n' data lines D1 to Dn arranged in a second direction perpendicular to the respective gate lines G1 to Gm with a constant interval between the data lines; a plurality of pixel electrodes (not shown in the drawing) formed as a matrix in pixel areas defined by the crossing gate and data lines respectively; and a plurality of thin film transistors for applying data signals supplied through the respective data lines to the respective pixel electrodes by being switched according to signals of the gate lines.

[0010] Further, a pair of driver integrated circuits (ICs) 14 and 15 are installed at the sides of the gate and data lines, respectively, so as to supply gate and data driving signals thereto. Namely, a pair of pads (not shown in the drawing) are formed at the ends of the gate and data lines to which the driver ICs are connected.

[0011] FIG. 2 shows cross-sectional views of the LCD taken along a line I-I' in FIG. 1.

[0012] Referring to FIG. 2, a gate insulating layer 22 is formed on a first substrate 21. An nth data line 23 is patterned on the gate insulating layer 22. A passivation layer 24 made of an insulator is formed over an entire surface of the substrate including the nth data line 23. A transparent

conductive layer of indium tin oxide (ITO) 25 for applying a voltage to the liquid crystal display is patterned on the passivation layer 24.

[0013] A black matrix 27 having predetermined spaces therein, is formed on an upper insulating substrate 26. A color filter layer 28 fills the spaces in the black matrix 27.

[0014] Unfortunately, the LCD according to the related art has some problems as follows.

[0015] The degree of alignment for the TFT and color filter substrates depends on the alignment tolerance (or margin) for combining (or assembling) the upper and lower substrates. Such combining margin is determined by the design of the respective substrates, for which precision of about several micrometers is required. Light leakage occurs at both lateral sides of the panel when the alignment between two substrates is deviated from the combining margin, thereby failing to provide desirable driving characteristics.

[0016] Namely, as shown in FIG. 2, there is no structure to block the light leakage at the right side of the nth data line 23. Therefore, light leakage occurs due to the transmitting light reaching the color filter layer.

SUMMARY OF THE INVENTION

[0017] Accordingly, the present invention is directed to a liquid crystal display and driving method thereof that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0018] An advantage of the present invention is to provide the provision of a liquid crystal display and driving method thereof, in which additional dummy gate and data lines are formed to prevent light leakage at both lateral sides of the panel due to the combining irregularity of the panels.

[0019] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0020] To achieve these and other advantages, and in accordance with the purpose of the present invention as embodied and broadly described, a liquid crystal display according to the present invention includes m valid gate lines G1 to Gm arranged in a first direction with first constant intervals between the valid gate lines; n valid data lines arranged in a second direction perpendicular to the valid gate lines with second constant intervals between the valid data lines; and at least one dummy data line at a periphery of and in parallel with the n valid data lines.

[0021] In another aspect of the present invention, a liquid crystal display according to the present invention includes m valid gate lines G1 to Gm arranged in a first direction with first constant intervals between the valid gate lines; n valid data lines arranged in a second direction perpendicular to the valid gate lines with second constant intervals between the valid data lines; a dummy gate line in parallel with the valid gate lines at a periphery of the m valid gate lines; and at least a first and a second dummy data line at left and right sides of the n valid data lines.

[0022] In a further aspect of the present invention, a liquid crystal display in a TFT-LCD panel includes a first substrate on which a black matrix layer and a color filter layer are stacked sequentially on a first insulating substrate; a second substrate on which a gate electrode, a gate insulating layer, an active semiconductor layer, source and drain electrodes, and a passivation layer are stacked on a second insulating substrate, wherein the second substrate opposes the first substrate; and a liquid crystal layer between the first and second substrates, wherein the passivation layer is formed of an organic insulating material.

[0023] In another further aspect of the present invention, a method of driving a liquid crystal display including a valid data line area in which a plurality of data lines D1 to Dn are formed; areas of a first dummy data line and a second dummy data line formed at left and right sides of the valid data line area; a valid gate line area in which a plurality of gate lines G1 to Gm are formed; and a first dummy gate line formed at one side of the valid gate line area, includes applying a first same driving signal to the first dummy data line and a second data line D2 in a plurality of the data lines and a second same driving signal to the second dummy data line and (n-1)th data line Dn-1, and applying a pulse waveform synchronized to a waveform applied to the mth gate line Gm to the dummy data lines.

[0024] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0026] In the drawings:

[0027] FIG. 1 shows a layout of LCD according to a related art;

[0028] FIG. 2 shows a cross-sectional view of the LCD taken along a line I-I' in FIG. 1;

[0029] FIG. 3 shows a layout of a liquid crystal display according to a first embodiment of the present invention;

[0030] FIG. 4 shows a layout of a liquid crystal display according to a second embodiment of the present invention;

[0031] FIG. 5 shows a timing graph of gate driving signals in a liquid crystal display according to the present invention;

[0032] FIG. 6A shows a layout of a magnified area II-II' in FIG. 3; and

[0033] FIG. 6B shows a cross-sectional view the LCD taken along a line III-III' in FIG. 6A.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0034] Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Where possible,

the same reference numerals will be used to illustrate like elements throughout the specification.

[0035] In the present invention, it is intended that forming additional dummy gate and data lines prevents light leakage at both lateral sides of the panel due to the combining irregularity of the panels.

[0036] FIG. 3 shows a layout of a liquid crystal display according to a first embodiment of the present invention.

[0037] Referring to FIG. 3, a panel according to the present invention includes a valid data line area 31 in which a plurality of even-numbered and odd-numbered data lines D1' to Dn are separated from each other by a constant interval between data lines; a first dummy data line area 32a and a second dummy data line area 32b formed outside the valid data line area 31; a valid gate line area 33 where a plurality of gate lines G1 to Gm are formed in a direction crossing with the data lines with constant intervals between adjacent gate lines; and a first dummy gate line area 34 outside the valid gate line area 33.

[0038] In this case, the first dummy data line formed in the first dummy data line area 32a is connected with the second data line D2 in the valid data line area 31 through a first conductive line 35. The second dummy data line formed in the second dummy data line area 32b is connected with the (n-1)th data line Dn-1 in the valid data line area 31 through a second conductive line 36.

[0039] Therefore, the first dummy data line formed in the first dummy data line area 32a is supplied with the same data signal as applied to the second data line D2, while the second dummy data line in the second dummy data line area 32b is supplied with the same data signal as applied to the (n-1)th data line Dn-1.

[0040] The LCD according to the present invention is driven by the data inversion method. Thus, the first data line D1 is positive (+) and the second data line D2 is negative (-), thereby resulting in the alternation of (+) and (-) in a plurality of the data lines formed in the valid data line area 31.

[0041] Accordingly, the first dummy data line in the first dummy data line area 32a is driven in a manner opposite to that of the first data line D1, while the second dummy data line in the second dummy data line area 32b is driven in a manner opposite to that of the nth data line Dn.

[0042] The LCD having the above structure is driven in a manner as follows.

[0043] First, as shown in FIG. 3, the first dummy data line is connected to the second data line D2 through the first conductive line 35, and the second dummy data line is connected to the (n-1)th data line Dn-1 through the second conductive line 36. In this case, data signals are outputted from the driver by a general method.

[0044] Therefore, the effective width of the display is broadened by driving all the pixels of the display because the data lines including the first and second dummy data lines are driven in accordance with the alternating of (+) and (-).

[0045] FIG. 4 shows a layout of a liquid crystal display according to a second embodiment of the present invention.

[0046] Referring to FIG. 4, the structure of a panel in an LCD according to the second embodiment is the same as that of the panel of the first embodiment, except for the formation of the first and second conductive lines. In such a structure, a data driver circuit supplies video signals so that one signal is applied to the first dummy data line and the second data line D2, and another signal is applied to the second dummy data line and the (n-1)th data line. The first dummy data line and the second dummy data line are supplied with video signals having different polarities respectively. The data driver applies the same video signals to the second data line D2 and the first dummy data line and applies another identical video signal to the (n-1)th data line Dn-1 and the second dummy data line. A voltage difference between high and low levels, $\Delta V_{gh1}(=V_{gh}-V_{gl})$, applied to the first dummy gate line is equal to or higher than about 1V.

[0047] In this case, a gate driving signal for driving the first and second dummy data lines and the valid data line is explained in the following description.

[0048] FIG. 5 shows a timing graph of gate driving signals in a liquid crystal display according to the present invention.

[0049] Referring to FIG. 5, the time at which a driving signal is applied to the first dummy gate line 34 is synchronized with the time at which a driving signal is applied to the mth gate line Gm placed at the end of the panel.

[0050] Namely in the panel, when the driving signal is finally applied to the mth gate line Gm through a plurality of valid gate lines G1 to Gm from the first dummy gate line 34, the same signal is applied to the first dummy gate line 34.

[0051] FIG. 6A shows a layout of a magnified area II-II' in FIG. 3 and FIG. 4.

[0052] Referring to FIG. 6A, a pixel electrode 66 and a thin film transistor 13 are formed in a pixel area defined by an nth data line Dn 63, a second dummy data line 32b, and a pair of valid gate lines 33 crossing with the nth data line Dn and the second dummy data line 32b.

[0053] FIG. 6B shows a cross-sectional view the LCD taken along a line III-III' in FIG. 6A.

[0054] Referring to FIG. 6B, a gate insulating layer 62 is formed on an insulating substrate 61 as a lower substrate. The nth data line 63 and the second dummy data line 32b are formed on the gate insulating layer 62 a predetermined interval apart.

[0055] A passivation layer 65 is formed on the substrate including the data lines with an organic insulating material such as BCB (benzocyclobutene) or acrylate or an inorganic insulating material such as silicon nitride (SiN_x).

[0056] A transparent conductive layer 66 of ITO for applying voltage to the liquid crystal display is formed on the passivation layer 65.

[0057] A black matrix 68 having a space therein is patterned on the other insulating substrate 67 as an upper substrate. A color filter layer 69 is formed on the substrate 67 including the black matrix 68.

[0058] The second dummy data line 32b formed in the above structure prevents light transmission within a visible angle at the edge of the panel and drives the pixel at the

lateral sides of the second dummy data line, which also occurs in an area where the first dummy data line is formed.

[0059] Accordingly, the LCD according to the present invention prevents light leakage due to the combining irregularity by adding the dummy data lines and dummy gate lines, as well as substantially widening the display by driving the pixels next to the dummy data line when applying signals to the dummy data line.

[0060] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display comprising:

m valid gate lines GI to Gm arranged in a first direction with first constant intervals between the valid gate lines;

n valid data lines arranged in a second direction perpendicular to the valid gate lines with second constant intervals between the valid data lines; and

at least one dummy data line at a periphery of in parallel with the n valid data lines.

2. The liquid crystal display of claim 1, wherein the at least one dummy data line comprises:

a first dummy data line at a first side of the valid data lines; and

a second dummy data line at a second side of the valid data lines wherein the second side is opposite to the first side.

3. The liquid crystal display of claim 2, wherein the n valid data lines include even numbered data lines and odd numbered data lines, and wherein the first dummy data line is connected to one of the even-numbered data lines through a first conductive line and the second dummy data line is connected to one of the odd-numbered data lines through a second conductive line.

4. The liquid crystal display of claim 3, wherein the first dummy data line is connected to a second data line D2 and the second dummy data line is connected to an (n-1)th data line Dn-1.

5. A liquid crystal display comprising:

m valid gate lines G1 to Gm arranged in a first direction with first constant intervals;

n valid data lines arranged in a second direction perpendicular to the valid gate lines with second constant intervals between the valid data lines;

a dummy gate line in parallel with the valid gate lines at a periphery of the m valid gate lines; and

at least a first and a second dummy data line at a first side and a second side of the n valid data lines respectively.

6. The liquid crystal display of claim 5, wherein the n valid data lines include even-numbered data lines and odd-numbered data lines, and wherein the first dummy data line is connected to one of the even-numbered data lines through

a first conductive line and the second dummy data line is connected to one of the odd-numbered data lines through a second conductive line.

7. The liquid crystal display of claim 6, wherein the first dummy data line is connected to a second data line D2 and the second dummy data line is connected to an (n-1)th data line Dn-1.

8. The liquid crystal display of claim 2, the display further comprising a data driving circuit for applying video signals to a plurality of the data lines in an area of the valid data lines and the first and second dummy data lines.

9. The liquid crystal display of claim 5, the display further comprising a data driving circuit for applying video signals to a plurality of the data lines in an area of the valid data lines and the first and second dummy data lines.

10. The liquid crystal display of claim 2, wherein the first and second dummy data lines are supplied with video signals having different polarities, respectively.

11. The liquid crystal display of claim 5, wherein the first and second dummy data lines are supplied with video signals having different polarities, respectively.

12. The liquid crystal display of claim 5, wherein a pulse waveform synchronized to a waveform applied to the mth gate line Gm is applied to the dummy gate line.

13. The liquid crystal display of claim 8, wherein the data driver applies the same video signals to the second data line D2 and the first dummy data line and applies other identical video signals to the (n-1)th data line Dn-1 and the second dummy data line.

14. The liquid crystal display of claim 9, wherein the data driver applies the same video signals to the second data line D2 and the first dummy data line and applies other identical video signals to the (n-1)th data line Dn-1 and the second dummy data line.

15. The liquid crystal display of claim 2, wherein a voltage difference between high and low levels, $\Delta V_{gh1}(=V_{gh}-V_{g1})$, applied to the first dummy gate line is equal to or higher than 1V.

16. The liquid crystal display of claim 5, wherein a voltage difference between high and low levels, $\Delta V_{gh1}(=V_{gh}-V_{g1})$, applied to the first dummy gate line is equal to or higher than 1V.

17. A liquid crystal display in a TFT-LCD panel comprising:

a first substrate in which a black matrix layer and a color filter layer are stacked sequentially on a first insulating substrate;

a second substrate on which a gate electrode, a gate insulating layer, an active semiconductor layer, source and drain electrodes, and a passivation layer are stacked on a second insulating substrate, wherein the second substrate opposes the first substrate; and

a liquid crystal layer between the first and second substrates,

wherein the passivation layer is formed of an organic insulating material.

18. The liquid crystal display of claim 17, wherein the organic insulating material is one of BCB (benzocyclobutene) and acrylate.

19. The liquid crystal display of claim 17, wherein the passivation layer is formed of an inorganic insulating material.

20. The liquid crystal display of claim 19, wherein the inorganic insulating material is silicon nitride (SiN_x).

21. A method of driving a liquid crystal display,

the liquid crystal display including a valid data line area in which a plurality of data lines D1 to Dn are formed, areas of a first dummy data line and a second dummy data line formed at left and right sides of the valid data line area, a valid gate line area in which a plurality of gate lines G1 to Gm are formed, and a first dummy gate line formed at one side of the valid gate line area, the method comprising the steps of:

applying a first same driving signal to the first dummy data line and a second data line D2 and a second same driving signal to the second dummy data line and an (n-1)th data line Dn-1; and

applying a pulse waveform synchronized to a waveform applied to the mth gate line Gm to the dummy data lines.

22. The method of driving a liquid crystal display of claim 21, wherein an alternating signal that has one of positive (+) and negative (-) polarity is applied to each of a plurality of the data lines including the first and second dummy data lines.

23. The method of driving a liquid crystal display of claim 21, wherein the first and second dummy data lines are connected electrically to the second data line D2 and the (n-1)th data line, respectively.

24. The method of driving a liquid crystal display of claim 21, wherein a data driving circuit applies a first video signal to the first dummy data line and second data line and a second video signal to the second dummy data line and the (n-1)th data line.

25. The method of driving a liquid crystal display of claim 21, wherein the first and second dummy data lines are supplied with video signals having different polarities, respectively.

26. The method of driving a liquid crystal display of claim 21, wherein a pulse waveform synchronized to a waveform applied to the mth gate line Gm is applied to the dummy gate line.

27. The liquid crystal display of claim 21, wherein a voltage difference between high and low levels, $\Delta V_{gh1}(=V_{gh}-V_{g1})$, applied to the first dummy gate line is equal to or higher than 1V.

28. A liquid crystal display in a TFT-LCD panel comprising:

a valid data line area having a plurality of data lines D1 to Dn with a constant interval between adjacent data lines;

a first dummy data line area and a second dummy data line area formed outside the valid data line area;

a valid gate line area having a plurality of gate lines G1 to Gm formed in a direction crossing with the data lines with a constant interval between adjacent gate lines;

and a first dummy gate line area outside the valid gate line area.

29. The liquid crystal display of claim 28, wherein a first dummy data line formed in the first dummy data line area is connected with a second data line D2 in the valid data line area through a first conductive line, and a second dummy data line formed in the second dummy data line area is

connected with an (n-1)th data line D_{n-1} in the valid data line area through a second conductive line.

30. The liquid crystal display of claim 29, wherein the first dummy data line formed in the first dummy data line area is supplied with a same data signal as applied to the second data line D_2 , while the second dummy data line in the second dummy data line area is supplied with a same data signal as applied to the (n-1)th data line D_{n-1} .

31. The liquid crystal display of claim 29, the display further comprising a data driver circuit for applying video signals, wherein a first signal is applied to the first dummy data line and the second data line D_2 , and a second signal is applied to the second dummy data line and the (n-1)th data line.

32. The liquid crystal display of claim 29, wherein the time at which a driving signal is applied to the first dummy gate line is synchronized with the time at which a driving signal is applied to the mth gate line G_m .

33. A liquid crystal display comprising:

a pixel electrode and a thin film transistor formed in a pixel area defined by an nth data line D_n ;

a dummy data line; and

a pair of valid gate lines crossing with the nth data line D_n and the dummy data line.

34. A liquid crystal display comprising:

a gate insulating layer formed on a first insulating substrate;

a plurality of data lines D_1 through D_n , wherein nth data line and a dummy data line formed on the gate insulating layer a predetermined interval apart;

a passivation layer formed on the first insulating substrate including the data lines;

a transparent conductive layer for applying voltage to the liquid crystal display formed on the passivation layer;

a black matrix having a space therein patterned on a second insulating substrate; and

a color filter formed on the second insulating substrate including the black matrix.

35. The liquid crystal display of claim 34, wherein the organic insulating material is one of BCB (benzocyclobutene) and acrylate.

* * * * *

| | | | |
|----------------|--|---------|------------|
| 专利名称(译) | 液晶显示器及其驱动方法 | | |
| 公开(公告)号 | US20020080313A1 | 公开(公告)日 | 2002-06-27 |
| 申请号 | US10/017583 | 申请日 | 2001-12-18 |
| [标]申请(专利权)人(译) | LIM BYOUNG HO | | |
| 申请(专利权)人(译) | LIM BYOUNG HO | | |
| 当前申请(专利权)人(译) | LIM BYOUNG HO | | |
| [标]发明人 | LIM BYOUNG HO | | |
| 发明人 | LIM, BYOUNG HO | | |
| IPC分类号 | G02F1/133 G02F1/1335 G02F1/1345 G02F1/1362 G09G3/36 G02F1/1343 | | |
| CPC分类号 | G02F1/133512 G02F1/1345 G02F1/136286 G02F2001/133388 G09G2310/0232 G09G3/3648 G09G2300/0426 G09G2300/043 G02F2001/136272 | | |
| 优先权 | 1020000083095 2000-12-27 KR | | |
| 其他公开文献 | US6812908 | | |
| 外部链接 | Espacenet USPTO | | |

摘要(译)

液晶显示器包括沿第一方向排列的m条有效栅极线G1至Gm，栅极线之间具有第一恒定间隔，n条有效数据线沿垂直于有效栅极线的第二方向排列，数据线之间具有第二恒定间隔，并且至少一条虚拟数据线位于n条有效数据线的包围并与其并行。通过用特定数据线短接伪数据线或通过特定数据线的相同驱动信号施加到伪数据线的过程来执行驱动液晶显示器的方法。

