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(54) **ALTERNATIVE THIN FILM TRANSISTORS FOR LIQUID CRYSTAL DISPLAYS**

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G02F 1/1343 (2006.01)

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(58) **Field of Classification Search** 349/38–43, 349/139; 257/72, 59

See application file for complete search history.

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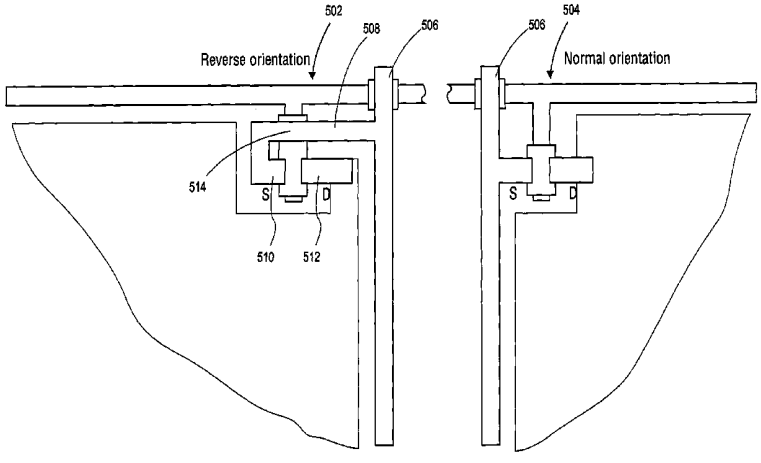
(57) **ABSTRACT**

Alternative thin film transistors for liquid crystal displays are disclosed. The alternative transistors can be used for panels of displays such as liquid crystal displays (LCDs), especially those having alternative pixel arrangements. These transistors can be oriented on a panel of an LCD using different, non-traditional configurations, while addressing misalignment and parasitic capacitance.

18 Claims, 8 Drawing Sheets



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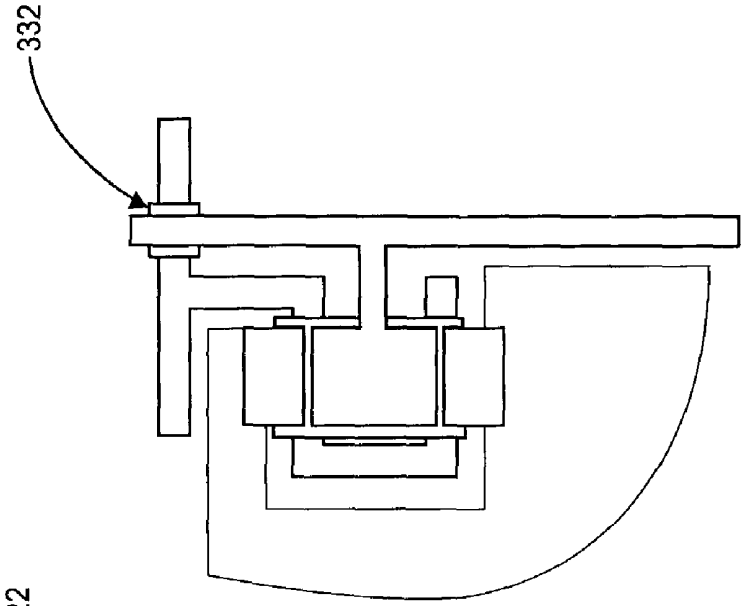

FIG. 3

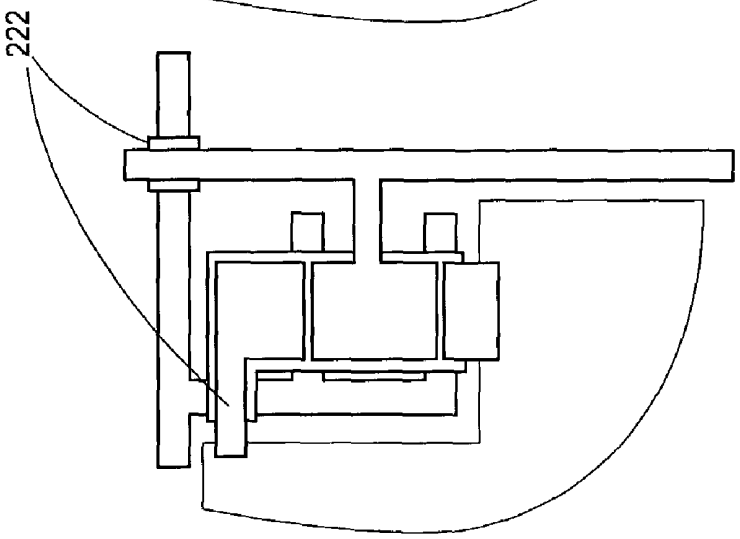

FIG. 2

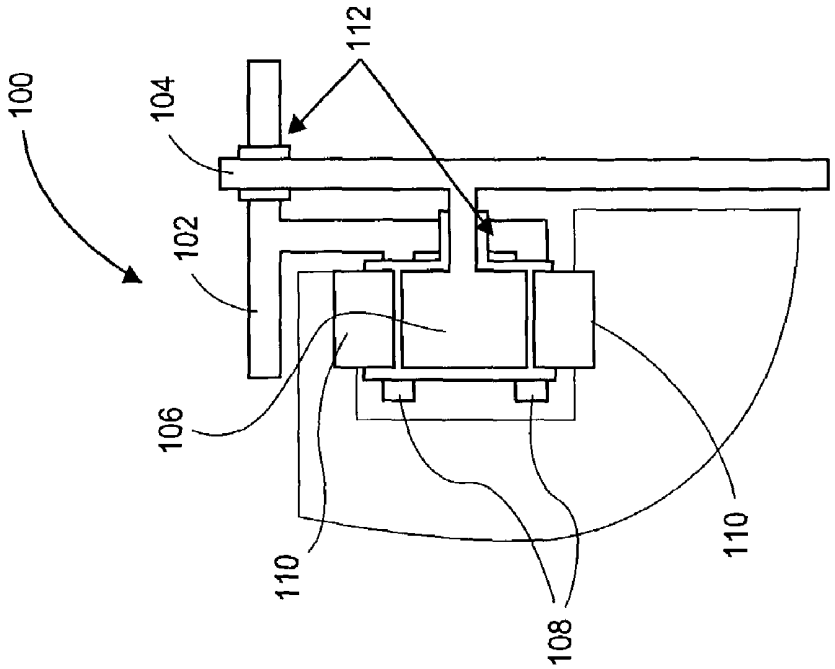

FIG. 1
(PRIOR ART)

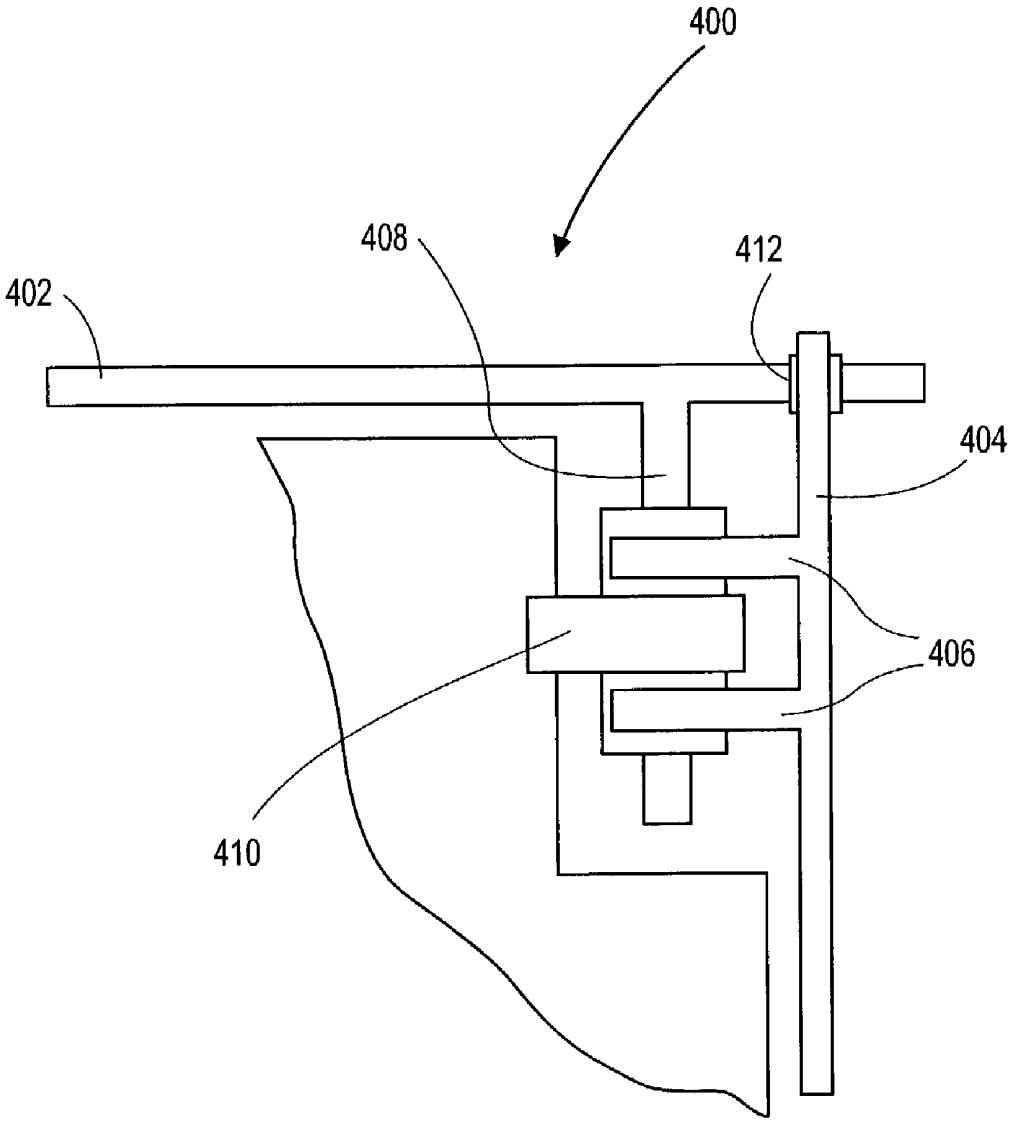

FIG. 4
(PRIOR ART)

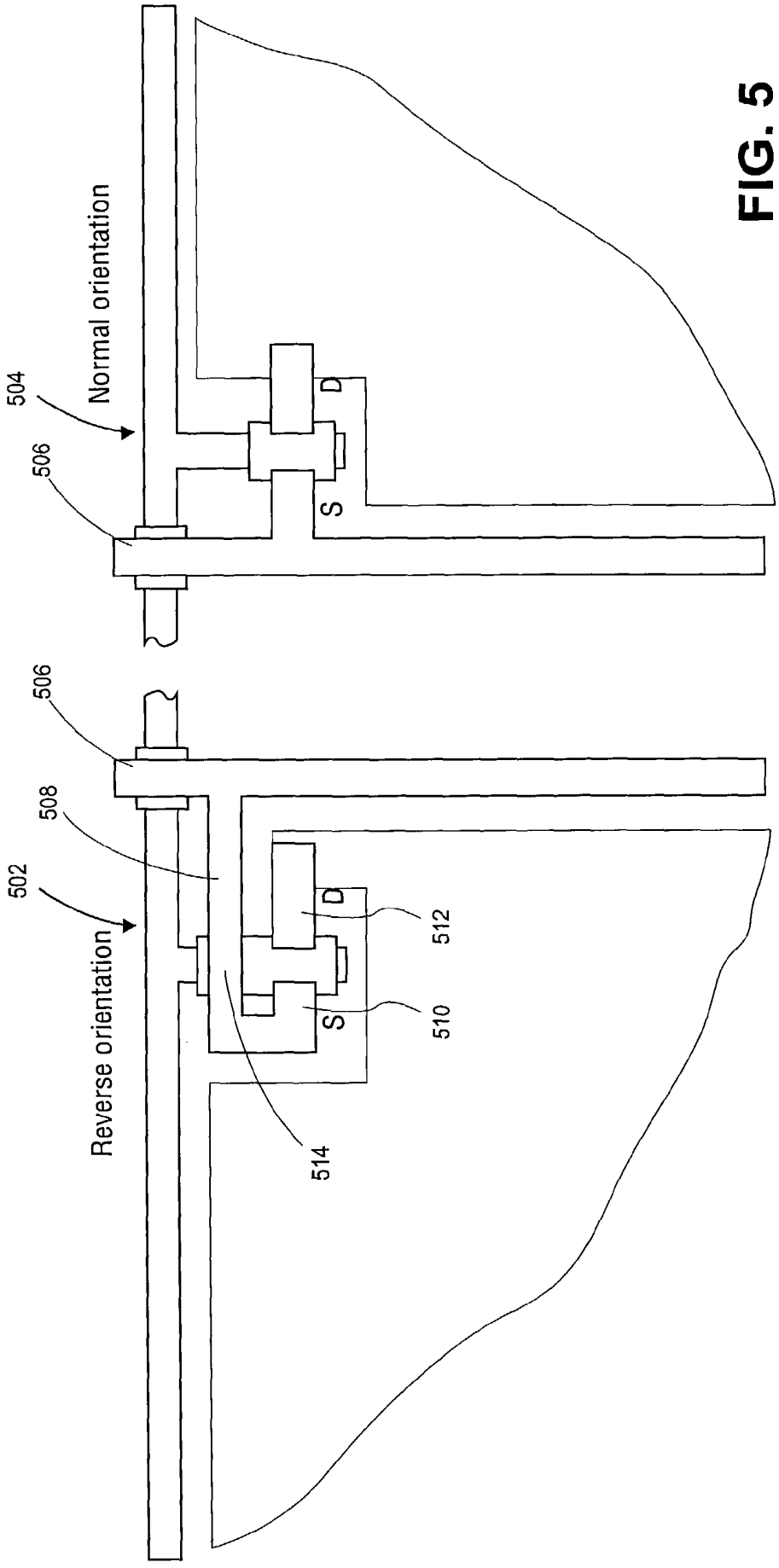
Normal orientation
504
506
D
S
506
508
502
Reverse orientation
D
S
512
510
514

FIG. 5

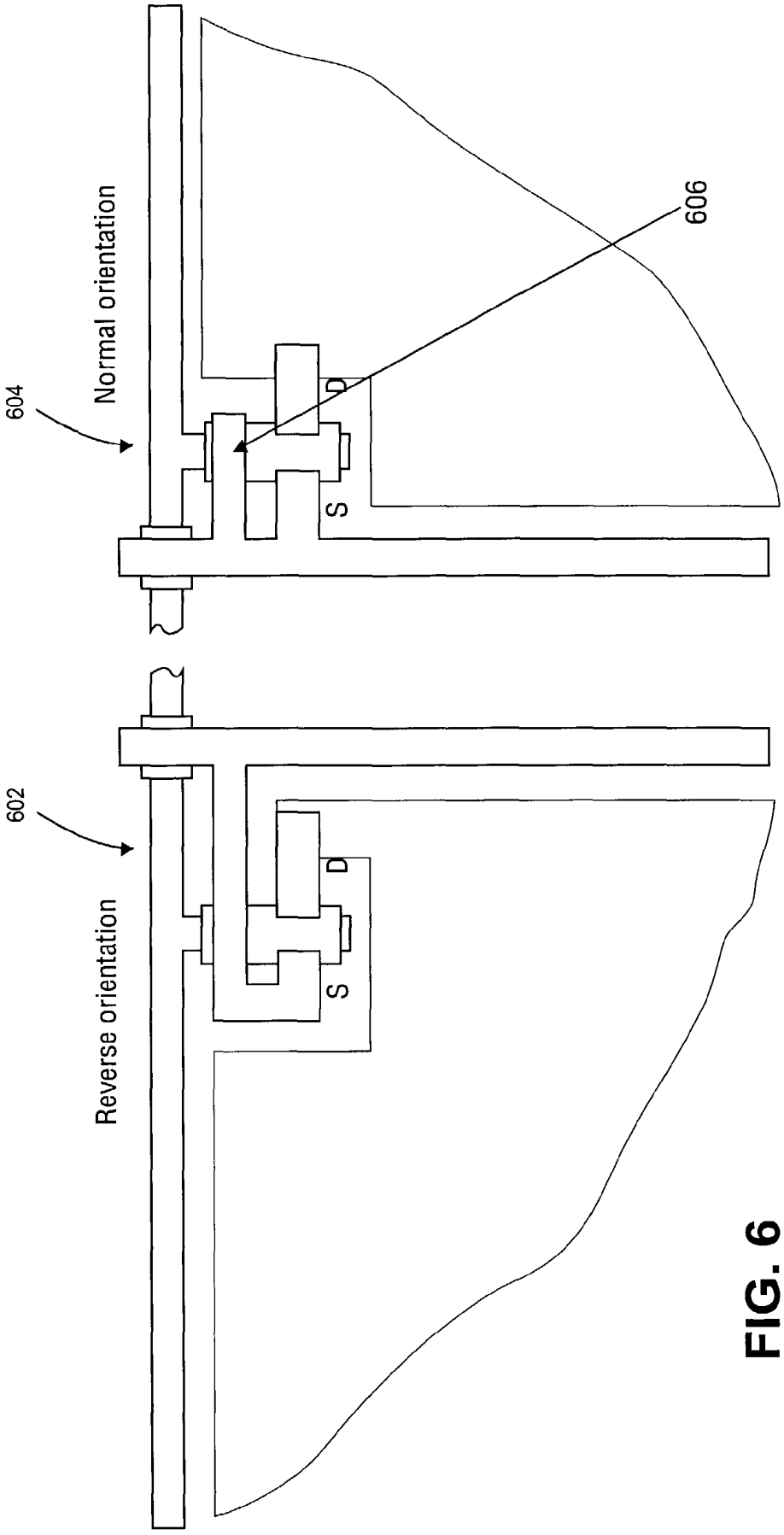

FIG. 6

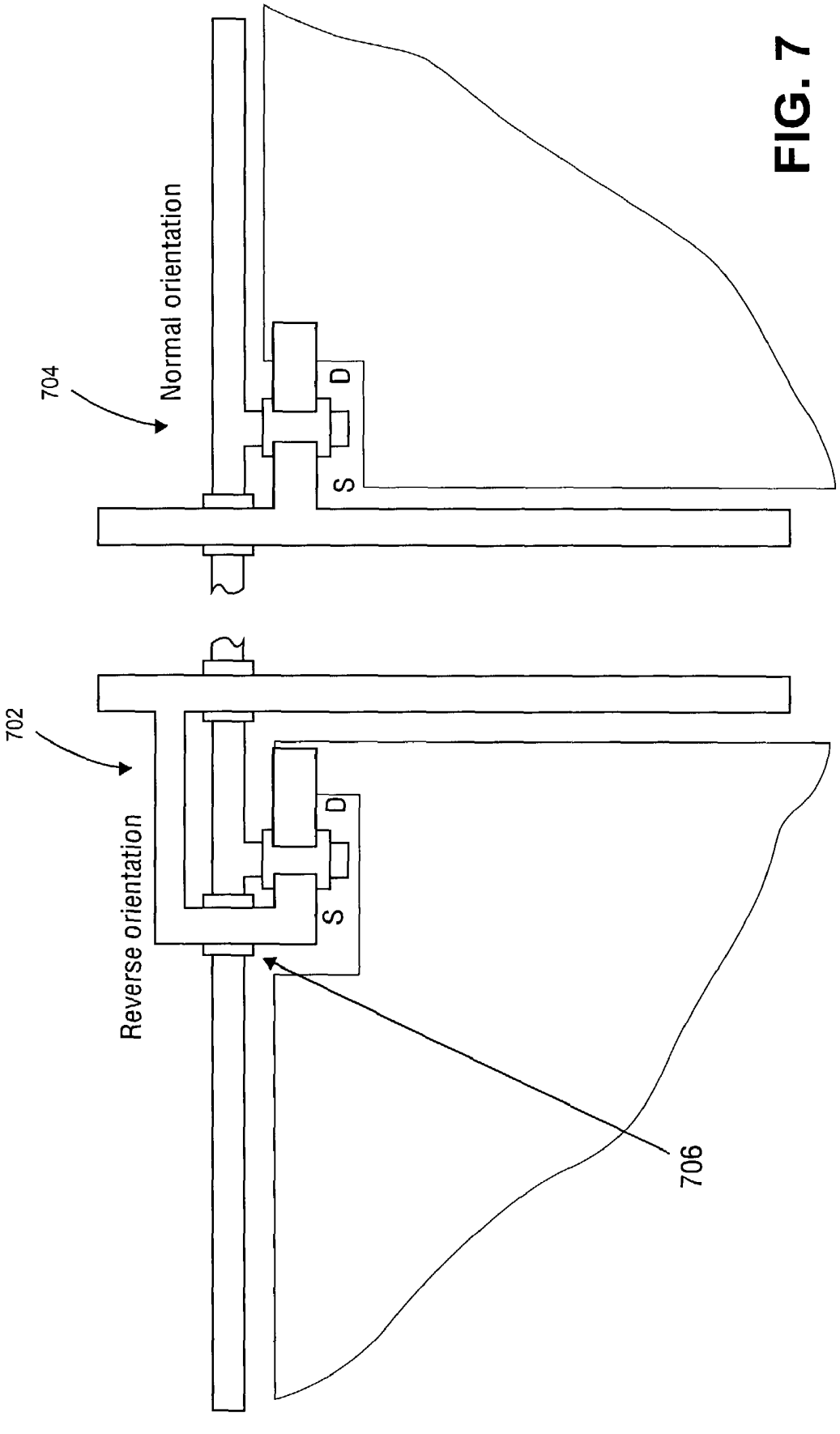

FIG. 7

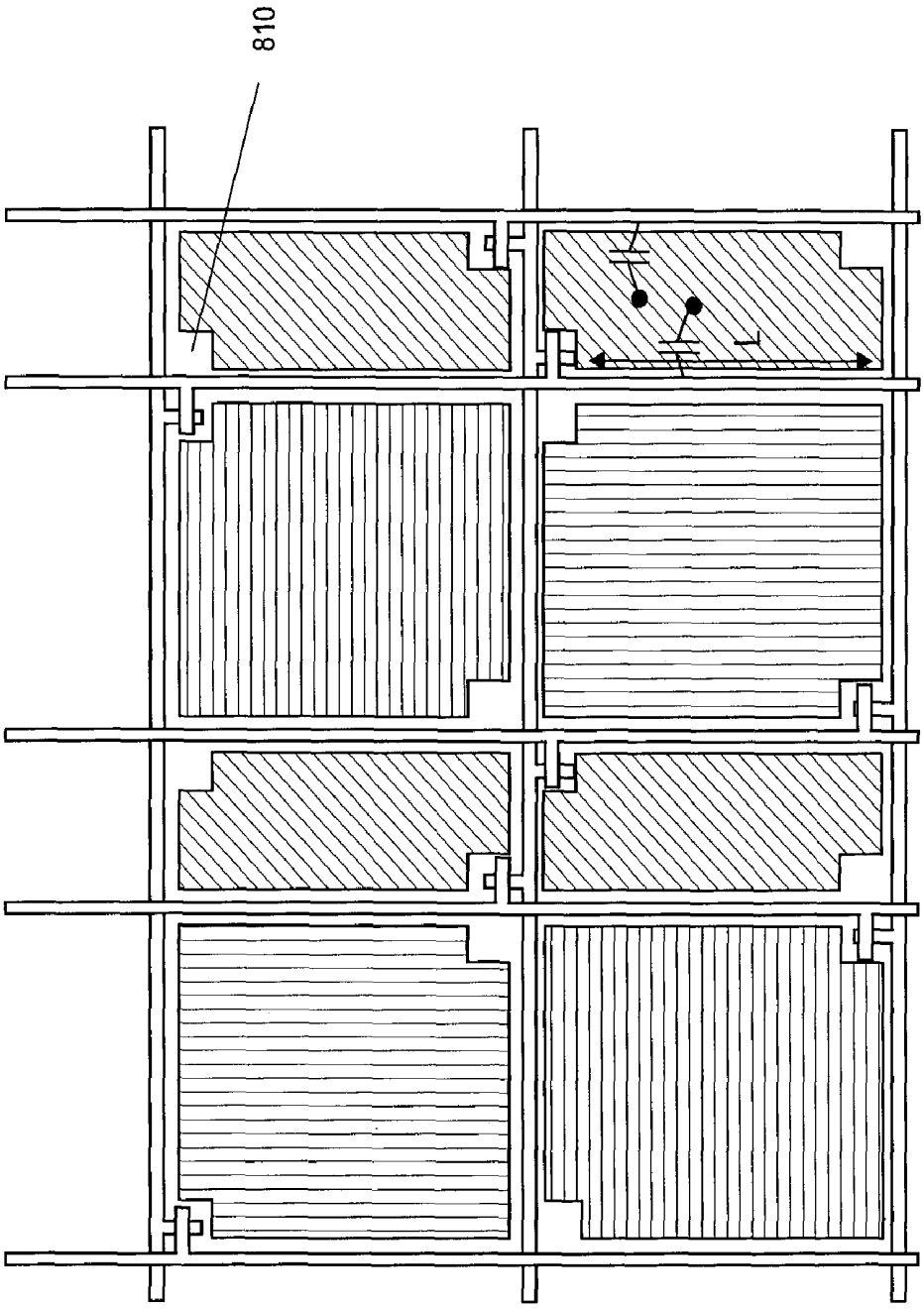

FIG. 8

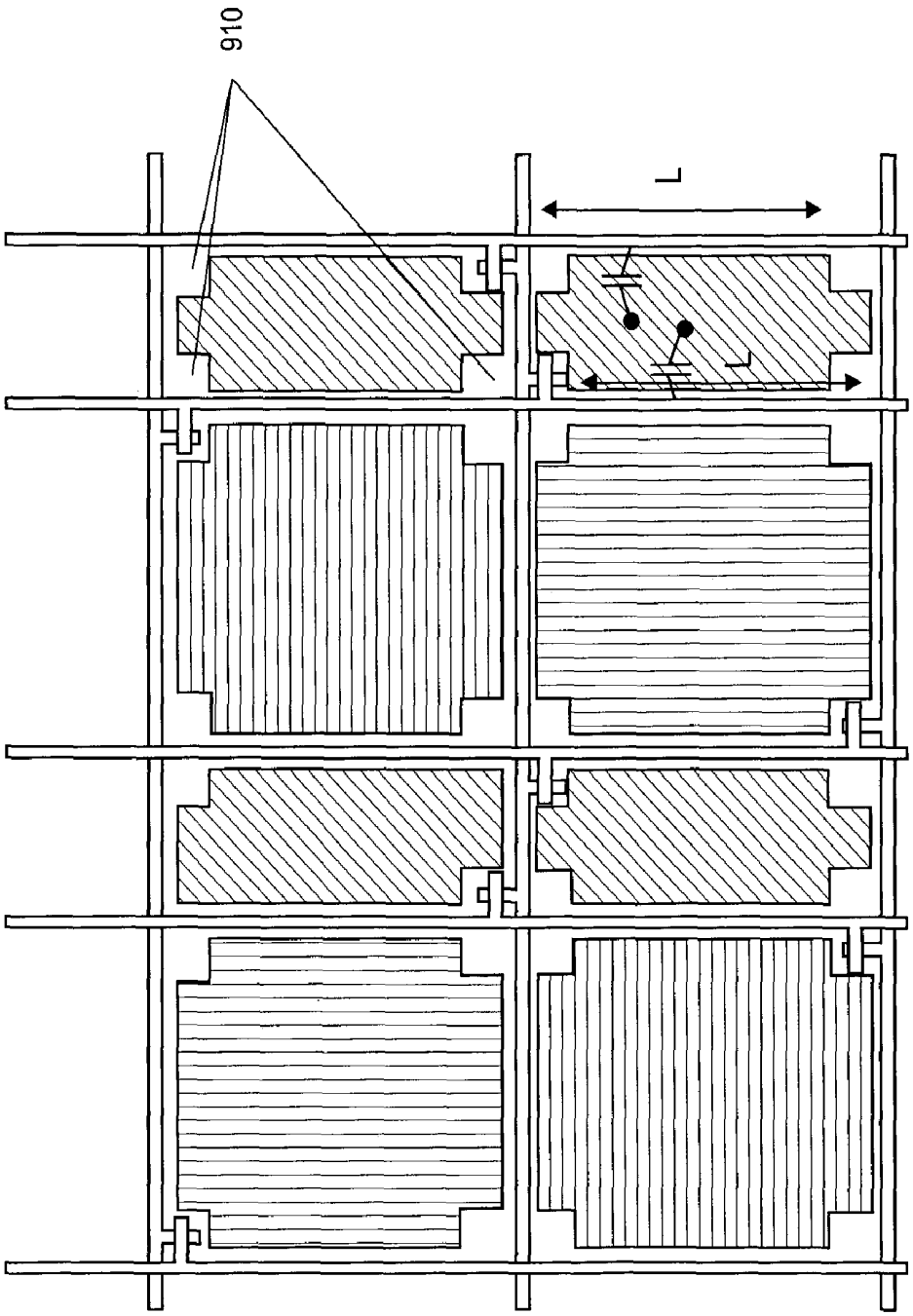

FIG. 9

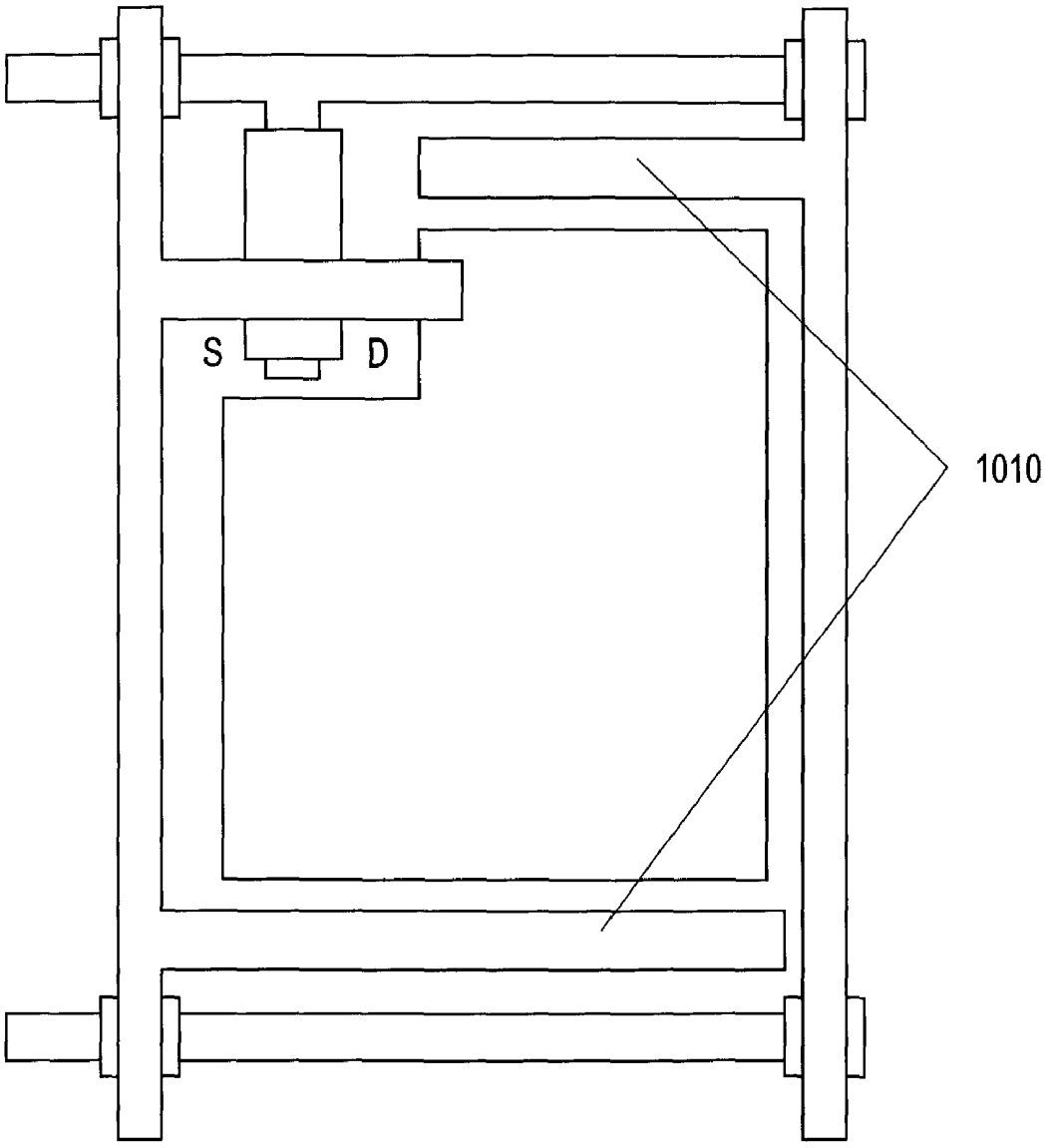

FIG. 10

ALTERNATIVE THIN FILM TRANSISTORS FOR LIQUID CRYSTAL DISPLAYS

BACKGROUND

Thin-film transistor (TFT) misalignment and parasitic capacitance can degrade the quality and performance of electronic devices such as liquid crystal displays (LCDs). One known attempt to correct for TFT misalignments and any associated increase in parasitic capacitance is found in U.S. Pat. No. 5,191,451 to Katayama et al ("the '451 patent"). FIG. **1** depicts the "double TFT" arrangement **100** of the '451 patent. Source line **104** connects to the TFT via source electrode **106**. Two gate electrodes **108** are connected to gate line **102**. Two drain electrodes **110** connect to the pixel and are formed such that the two gate electrodes **108** affect conduction from the source electrode to the drain electrodes when activated. It is noted that there are two crossover regions **112** that are connected to TFT may produce additional parasitic capacitance between the gate and the source. As discussed in the '451 patent, any vertical misalignment of the TFT placement is somewhat corrected by this double TFT arrangement as is discussed therein.

Another manner of reducing the ill effects of TFT misalignment is shown in U.S. Pat. No. 5,097,297 to Nakazawa ("the '297 patent"). FIG. **4** depicts a TFT **400** made in the manner taught in the '297 patent. As may be seen in FIG. **2**, gate line **402** delivers the gate signal to gate electrode **408**. Source line **404** sends image data to source electrodes **406**. When the gate electrode is activated, the image data is transferred to the pixel via the drain electrode **410**. It is noted that this TFT embodiment contains only one gate crossover **412** which aids in reducing parasitic capacitance.

Furthermore, prior LCDs use the same orientation to align transistor in the pixel area of the display. However, for alternative pixel arrangements, transistors may need to be located in unconventional locations of a pixel area, while addressing misalignment and parasitic capacitance.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in, and constitute a part of this specification illustrate exemplary implementations and embodiments of the invention and, together with the description, serve to explain principles of the invention.

FIG. **1** shows a prior art TFT having a double source/drain structure.

FIGS. **2** and **3** show alternative TFTs having a double source/drain structure.

FIG. **4** shows a prior art TFT with a double gate structure.

FIG. **5** show TFT structures in a reverse orientation and normal orientation, respectively.

FIG. **6** show TFT structures in a reverse orientation and normal orientation with an added gate crossover in the normal orientation to balance any parasitic capacitance found in the reverse orientation.

FIG. **7** show TFT structures in a reverse orientation and normal orientation with one fewer gate crossover in the reverse orientation to match any parasitic capacitance in the normal orientation.

FIG. **8** shows one novel pixel element design having a corner removed from the pixel to balance parasitic capacitances.

FIG. **9** shows yet another novel pixel element design having multiple corners

FIG. **10** shows yet another novel pixel structure in which at least one extra line is added to shield the pixel element from parasitic effects.

DETAILED DESCRIPTION

Reference will now be made in detail to implementations and embodiments, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

The following implementations and embodiments disclose alternative thin film transistors for liquid crystal displays are disclosed. The alternative transistors can be used for panels of displays such as liquid crystal displays (LCDs), especially those having alternative pixel arrangements. These transistors can be oriented on a panel of an LCD using different, non-traditional configurations, while addressing misalignment and parasitic capacitance.

FIGS. **2** and **3** provide different alternative embodiments to the prior art double TFT structure shown in FIG. **1**. These structures can provide reduced source to gate capacitance, which can cause crosstalk in certain images. However, the gate to drain crossover can lessen the damage to image quality. One advantage of the embodiment of FIG. **3** is that there is only one crossover **132** that may reduce parasitic capacitance.

Another set of TFT redesigns are shown in FIGS. **5** through **10** to handle the unevenness of parasitic capacitance that might be introduced by the above described TFT remapping. As TFTs are remapped on the panel, it is possible for some TFTs on the panel to be implemented in different corners or quadrants of a pixel area. For example, some TFTs may be constructed in the upper left hand corner of the pixel area, some in the upper right hand corner of the pixel area and so on. If all such TFTs were constructed the same way, then it would be likely that the source-drain orientation would be reversed for left hand corner and right hand corner implementation. Such non-uniformity of construction might introduce uneven parasitic capacitance in the case of a given TFT misalignment.

FIG. **5** is one embodiment of a TFT built with a reverse orientation **502** as compared with a TFT built with a typical orientation **1904**. For exemplary purposes, TFT **504** is constructed within the upper left hand corner of its associated pixel in the usual manner—i.e. without any crossovers to avoid any introduced parasitic capacitance. It is noted that the source (S) and drain (D) electrodes are placed in a left-to-right fashion. TFT **502** is shown constructed in the upper right hand corner of a pixel area in a reverse orientation—i.e. a crossover **514** from source line **1906** is constructed so that the source electrode **1910** and drain electrode **512** are also in left-to-right fashion. Thus, if there is a TFT misalignment in the horizontal direction, then TFTs **502** and **504** will receive the same amount of added parasitic capacitance—thus, keeping the panel's defects uniform. It will be appreciated that although TFT **502** and TFT **504** are depicted side-by-side and connected to the same column, this is primarily for explanatory purposes. It is unlikely that two adjoining subpixels would share the same column/data line—thus, TFT **504** and its associated pixel is provided to show the distinction between a normal TFT orientation and TFT **502** in a reverse orientation.

FIG. **6** shows another embodiment of TFTs **602** and **604**. As can be seen, a new crossover **606** is added to TFT **604** so as to balance the added parasitic capacitance via crossover **604**. FIG. **7** is yet another embodiment of TFTs **702** and **704**. As may be seen here, the gate electrode crossover **606** in FIG.

6 has been removed in favor of a gate line crossover **706** which may have a lesser impact on individual pixel elements.

FIGS. **8** and **9** are embodiments of pixel elements with corners **810** and **910** removed to match the one corner removed containing the TFT structure. These pixel elements as designed here may balance the parasitic capacitances than a normal pixel structure.

FIG. **10** is another embodiment of a pixel structure that employs at least one extra metal line **1010** that may help to shield the pixel element from the parasitic capacitances between the gate lines and the pixel element. Additionally, if a dot inversion scheme is employed, then the opposing polarities on both lines **1010** will also help to balance any parasitic capacitance between the source lines and the pixel elements.

Regarding the alternative TFT structures and pixel elements disclosed herein, standard LCD fabrication techniques can be implemented to form such structures. Moreover, the column, gate, and electrode lines can be formed of transparent material such as transparent conductive oxide so as not to degrade the optical qualities of the LCD.

What is claimed is:

1. A device comprising a plurality of first thin film transistors and a plurality of second thin film transistors, each of said first and said second thin film transistors comprising a source electrode, a gate electrode, and a drain electrode;

wherein at least one of said first thin film transistors comprises the source electrode, the gate electrode and the drain electrode being sequentially arranged along a normal orientation away from its corresponding data line,

at least one of said second thin film transistors comprises the drain electrode, the gate electrode and the source electrode being sequentially arranged along a reverse orientation away from its corresponding data line; and

wherein, in the second thin film transistor, (i) a crossover is formed by the data line corresponding to the second thin film transistor and the gate electrode of the second thin film transistor when the data line is connected to the source electrode of the second thin film transistor; or (ii) a first crossover is formed by the data line corresponding to the second thin film transistor and the gate line connected to the second thin film transistor when the data line is connected to the source electrode of the second thin film transistor, the first crossover being spaced apart from a second crossover where the gate line connected to the second thin film transistor crosses the data line corresponding to the second thin film transistor;

wherein said crossover in (i) or said first crossover in (ii) serve to effect substantially the same source electrode and drain electrode orientation as in said first thin film transistor;

wherein said first thin film transistors comprise a crossover to substantially balance any parasitic capacitance affected by said crossover in said second thin film transistor.

2. The device of claim **1** wherein any misalignment of thin film transistors are substantially the same for said first thin film transistors and said second thin film transistors.

3. The device of claim **1** wherein said device further comprises a plurality of pixel elements, each said pixel element connected to a thin film transistor wherein said thin film transistor comprises one of a group of thin film transistors, said group comprising said first thin film transistor and said second thin film transistor;

wherein further said pixel elements have a first corner and a second corner removed wherein further said second corner is placed where said thin film transistor connects with said pixel element.

4. The device of claim **1** wherein said data line corresponding to the first thin film transistor coincides with the data line corresponding to the second thin film transistor.

5. The device of claim **1** where the gate line connected to the second thin film transistor is also connected to the first thin film transistor.

6. A device comprising a plurality of first thin film transistors and a plurality of second thin film transistors, each of said first and said second thin film transistors comprising a source electrode, a gate electrode, and a drain electrode;

wherein at least one of said first thin film transistors comprises the source electrode, the gate electrode and the drain electrode being sequentially arranged along a normal orientation away from its corresponding data line,

at least one of said second thin film transistors comprises the drain electrode, the gate electrode and the source electrode being sequentially arranged along a reverse orientation away from its corresponding data line; and

wherein, in the second thin film transistor, (i) a crossover is formed by the data line corresponding to the second thin film transistor and the gate electrode of the second thin film transistor when the data line is connected to the source electrode of the second thin film transistor; or (ii) a first crossover is formed by the data line corresponding to the second thin film transistor and the gate line connected to the second thin film transistor when the data line is connected to the source electrode of the second thin film transistor, the first crossover being spaced apart from a second crossover where the gate line connected to the second thin film transistor crosses the data line corresponding to the second thin film transistor;

wherein said device further comprises a plurality of pixel elements, each said pixel element connected to a thin film transistor wherein said thin film transistor comprises one of a group of thin film transistors, said group comprising said first thin film transistor and said second thin film transistor;

wherein further said pixel elements have a first corner and a second corner removed wherein further said second corner is placed where said thin film transistor connects with said pixel element;

wherein said pixel element comprises a boundary contour and said boundary contour further comprises a first portion of said boundary contour where said first corner being removed comprises a shape substantially the shape of a second portion of said boundary contour comprising said second corner comprising said thin film transistor.

7. The device of claim **6** wherein said crossover in (i) or said first crossover in (ii) serve to effect substantially the same source electrode and drain electrode orientation as in said first thin film transistor.

8. A display panel with a first side and a second side opposite to the first side, the display panel comprising:

a plurality of source lines;

a plurality of gate lines;

a plurality of pixel elements;

a plurality of thin film transistors (TFTs) each of which connects a respective pixel elements to a respective source line, each TFT comprising: a gate electrode connected to a respective gate line; a source electrode connected to the respective source line; and a drain electrode connected to the respective pixel element;

wherein in top view, each gate electrode of each TFT connecting any one of said pixel elements to any one of said source lines comprises a portion positioned between the TFT's source and drain electrodes, said

portion comprising a first edge facing the drain electrode and the second edge facing the source electrode, wherein the first edge is on the first side of the second edge;

wherein at least one said gate electrode is on the first side of the respective source line, and at least one other said gate electrode is on the second side of the respective source line.

9. The display panel of claim **8** wherein at least one said TFT is on the first side of the respective source line, and at least one other said TFT is on the second side of the respective source line.

10. The display panel of claim **8** wherein in each TFT located on the second side of the respective source line, the source electrode crosses the gate electrode or the gate line.

11. The display panel of claim **9** wherein each TFT located on the first side of the respective source comprises a member extending from the respective source line and crossing the gate electrode to increase the parasitic capacitance between the respective source line and the gate electrode to improve the match between the parasitic capacitance of the TFTs located on the first side of the respective source lines and the TFTs located on the second side of the respective source lines.

12. The display panel of claim **8** wherein each pixel element comprises a first corner region on the first side of the pixel element and a second corner region on the second side of the pixel element;

wherein each TFT located on the first side of the respective source line is at least partially located in a cutout formed in the second corner region of the respective pixel element, and the respective pixel element also comprises a cutout in the second corner region, the cutout containing no part of any TFT connecting any one of said pixel elements to any one of said source lines;

wherein each TFT located on the second side of the respective source line is at least partially located in a cutout formed in the first corner region of the respective pixel element, and the respective pixel element also comprises a cutout in the first corner region, the cutout containing no part of any TFT connecting any one of said pixel elements to any one of said source lines.

13. A display panel with a first side and a second side opposite to the first side, the display panel comprising:

a plurality of source lines;

a plurality of gate lines;

a plurality of pixel elements;

a plurality of thin film transistors (TFTs) each of which connects a respective pixel elements to a respective source line, each TFT comprising: a gate electrode connected to a respective gate line; a source electrode connected to the respective source line; and a drain electrode connected to the respective pixel element;

wherein in top view, each drain electrode of each TFT connecting any one of said pixel elements to any one of said source lines is connected to the respective pixel element on the first side of the gate electrode;

wherein at least one said gate electrode is on the first side of the respective source line, and at least one other said gate electrode is on the second side of the respective source line.

14. The display panel of claim **13** wherein each drain electrode of each TFT connecting any one of said pixel elements to any one of said source lines is located on the first side of the gate electrode.

15. The display panel of claim **13** wherein at least one said TFT is on the first side of the respective source line, and at least one other said TFT is on the second side of the respective source line.

16. The display panel of claim **13** wherein in each TFT located on the second side of the respective source line, the source electrode crosses the gate electrode or the gate line.

17. The display panel of claim **16** wherein each TFT located on the first side of the respective source comprises a member extending from the respective source line and crossing the gate electrode to increase the parasitic capacitance between the respective source line and the gate electrode to improve the match between the parasitic capacitance of the TFTs located on the first side of the respective source lines and the TFTs located on the second side of the respective source lines.

18. The display panel of claim **13** wherein each pixel element comprises a first corner region on the first side of the pixel element and a second corner region on the second side of the pixel element;

wherein each TFT located on the first side of the respective source line is at least partially located in a cutout formed in the second corner region of the respective pixel element, and the respective pixel element also comprises a cutout in the second corner region, the cutout containing no part of any TFT connecting any one of said pixel elements to any one of said source lines;

wherein each TFT located on the second side of the respective source line is at least partially located in a cutout formed in the first corner region of the respective pixel element, and the respective pixel element also comprises a cutout in the first corner region, the cutout containing no part of any TFT connecting any one of said pixel elements to any one of said source lines.

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专利名称(译)	用于液晶显示器的替代薄膜晶体管		
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[标]申请(专利权)人(译)	ELLIOTT CANDICE HELLEN BROWN CREDELLE THOMAS LLOYD SCHLEGEL MATTHEW奥斯本		
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摘要(译)

公开了用于液晶显示器的替代薄膜晶体管。替代晶体管可用于诸如液晶显示器（LCD）的显示器面板，尤其是具有替代像素布置的那些。这些晶体管可以使用不同的非传统配置定向在LCD的面板上，同时解决未对准和寄生电容。