US006753935B2

(12) United States Patent
Wu

(10) **Patent No.: US 6,753,935 B2**
(45) **Date of Patent: Jun. 22, 2004**

(54) LIQUID CRYSTAL DISPLAY ELEMENT WITH A DEFECT REPAIRING FUNCTION

(75) Inventor: **Biing-Seng Wu**, Tainan Science-Based Industrial Park (TW)

(73) Assignee: **Chi Mei Optoelectronics Corp.**, Tainan (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) bydays.days.

(21) Appl. No.: **09/789,591**

(22) Filed: **Feb. 22, 2001**

(65) **Prior Publication Data**

US 2001/0028429 A1 Oct. 11, 2001

(30) **Foreign Application Priority Data**

Apr. 6, 2000 (TW) .... 89106351 A

(51) **Int. Cl.**^{7} **G02F 1/1333**; G01F 1/1339
(52) **U.S. Cl.** **349/54**; 349/139; 345/93
(58) **Field of Search** 349/54, 139

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,298,891 A	*	3/1994	Plus et al.	345/93
5,825,438 A	*	10/1998	Song et al.	349/54
6,191,832 B1	*	2/2001	Nakakura	349/54
2002/0024493 A1	*	2/2002	Ozawa et al.	

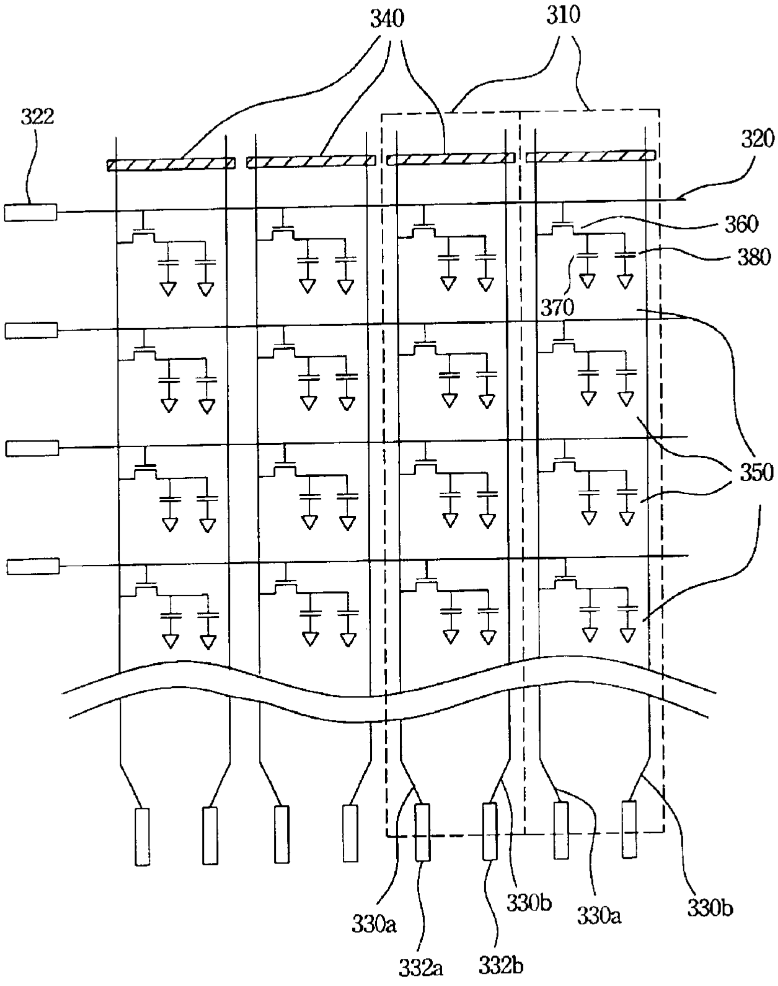
* cited by examiner

Primary Examiner—Julie-Huyen L. Ngo

(57) **ABSTRACT**

A liquid crystal display (LCD) element with a defect repairing function and a defect repairing method of the same. In an embodiment of the invention, a pixel is associated with a plurality of scan lines and a plurality of data lines. Along with separate spare lines, melting connection can be obtained to form a circuit path and to compensate for broken wires. A single pixel can also have a plurality of subpixels with spare conduction ports and meltable joints so that defective electrodes can be separated. The spare conduction ports can be melted and connected so that other subpixels support and compensate for the defective subpixel to minimize pixel signal loss.

11 Claims, 11 Drawing Sheets



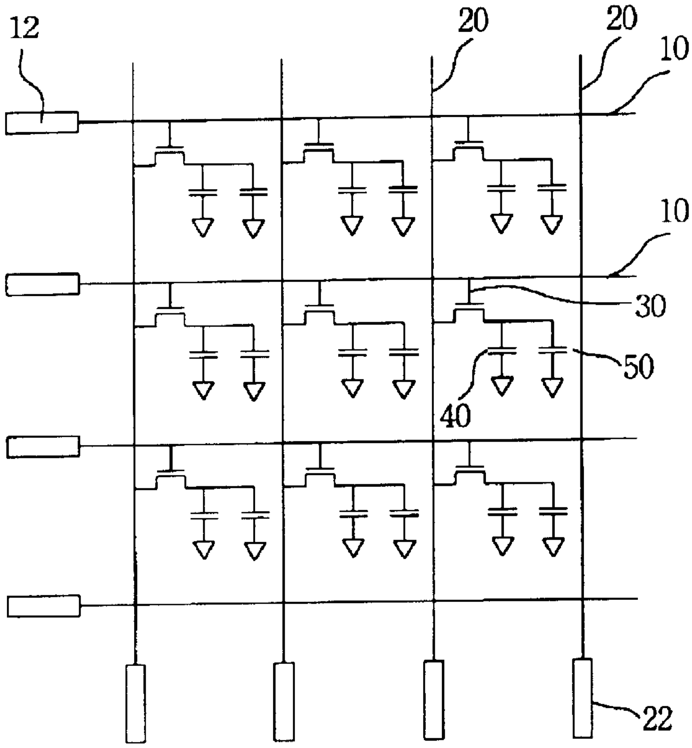


FIG. 1 A

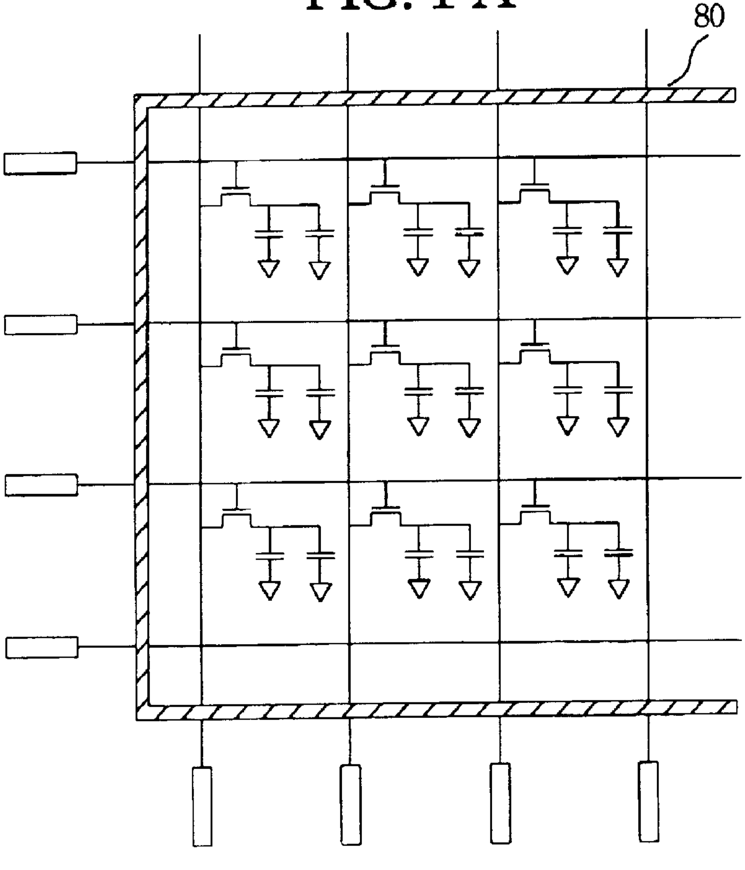


FIG. 2 A

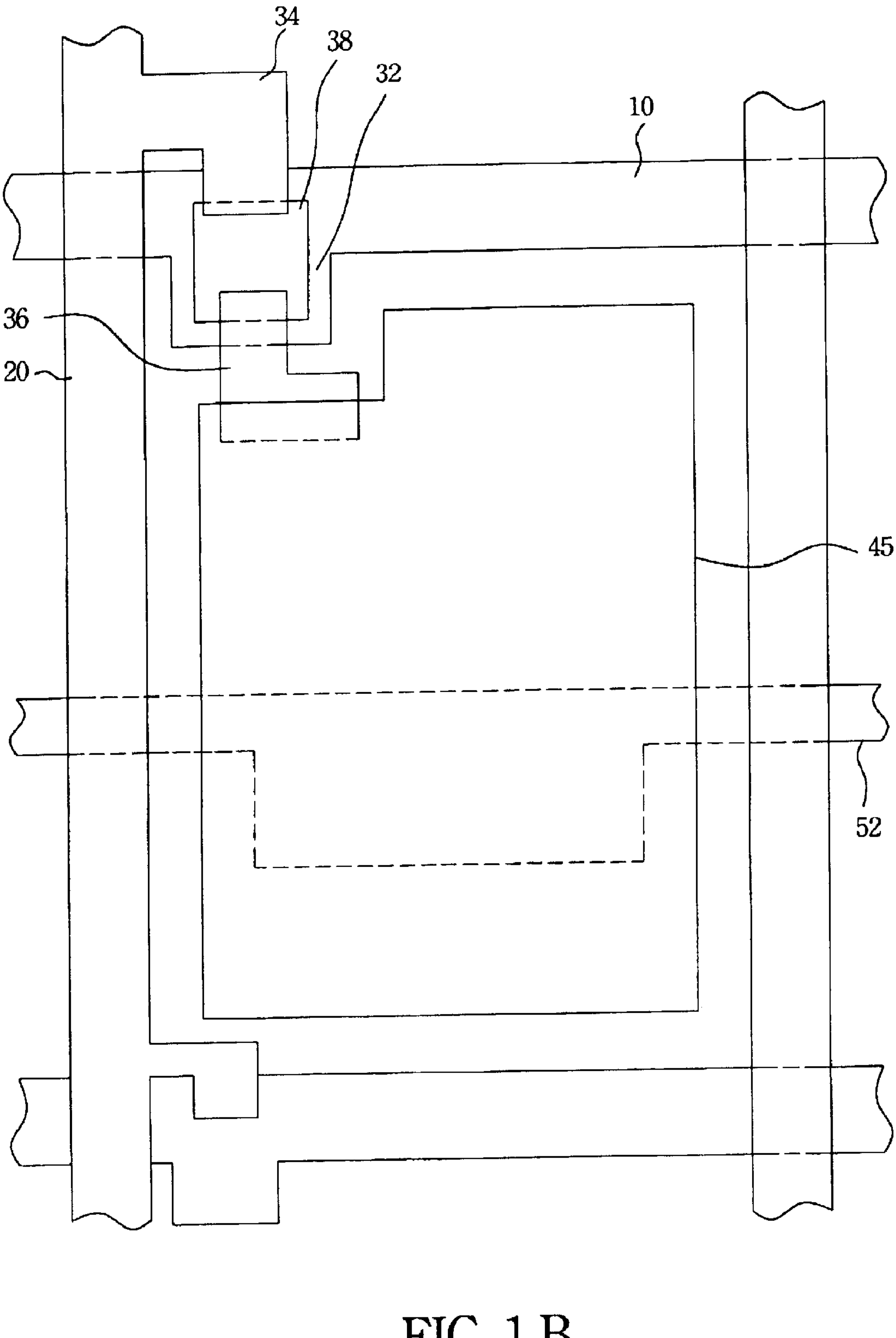


FIG. 1 B

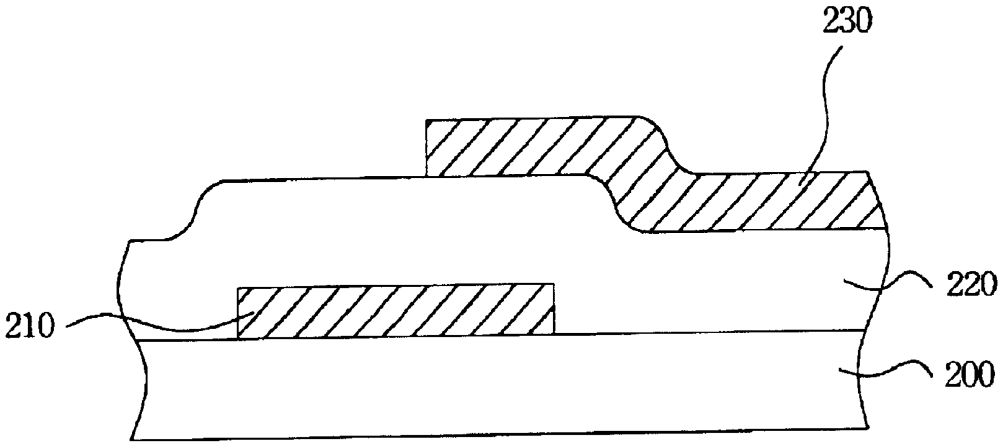


FIG. 2 B

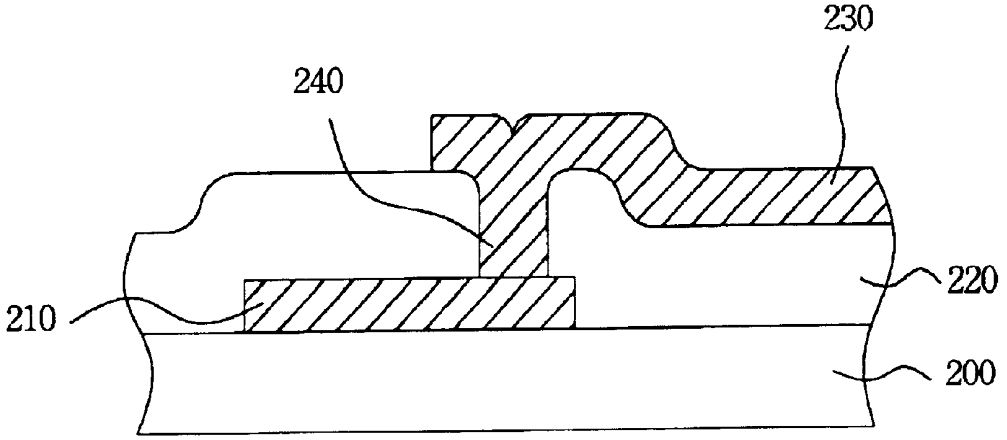


FIG. 2 C

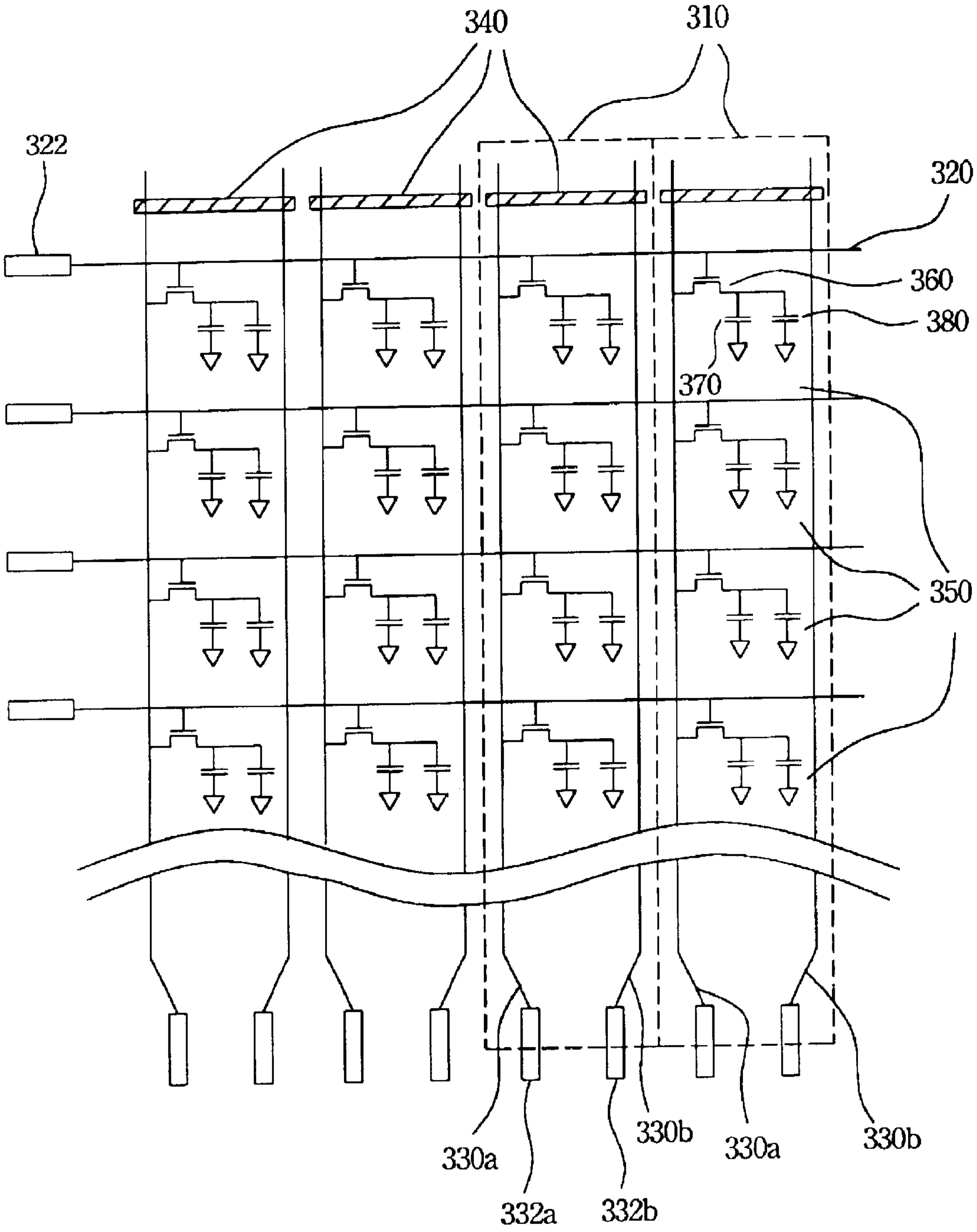


FIG. 3

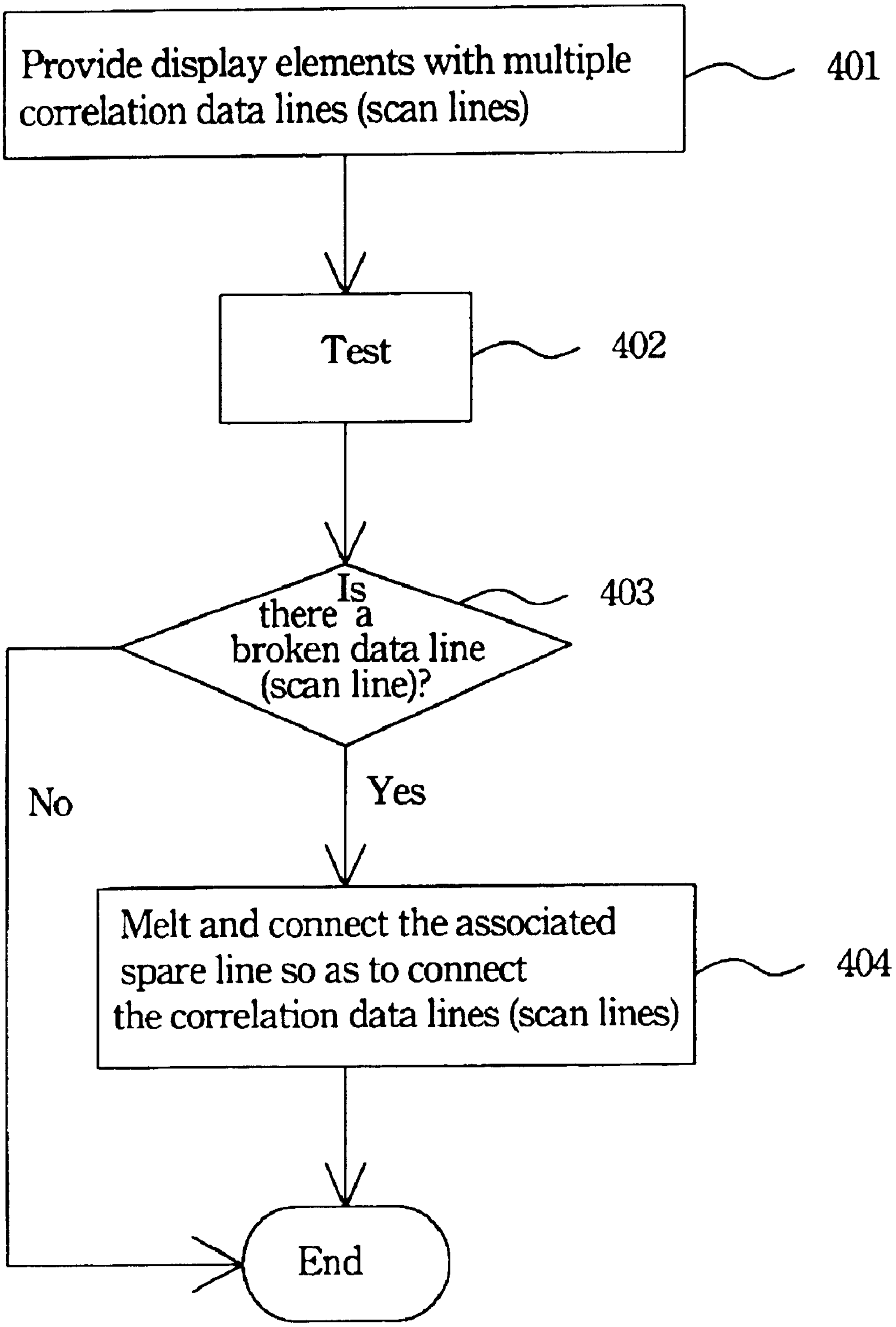

Provide display elements with multiple correlation data lines (scan lines)
401
Test
402
Is there a broken data line (scan line)?
403
No
Yes
Melt and connect the associated spare line so as to connect the correlation data lines (scan lines)
404
End

FIG. 4

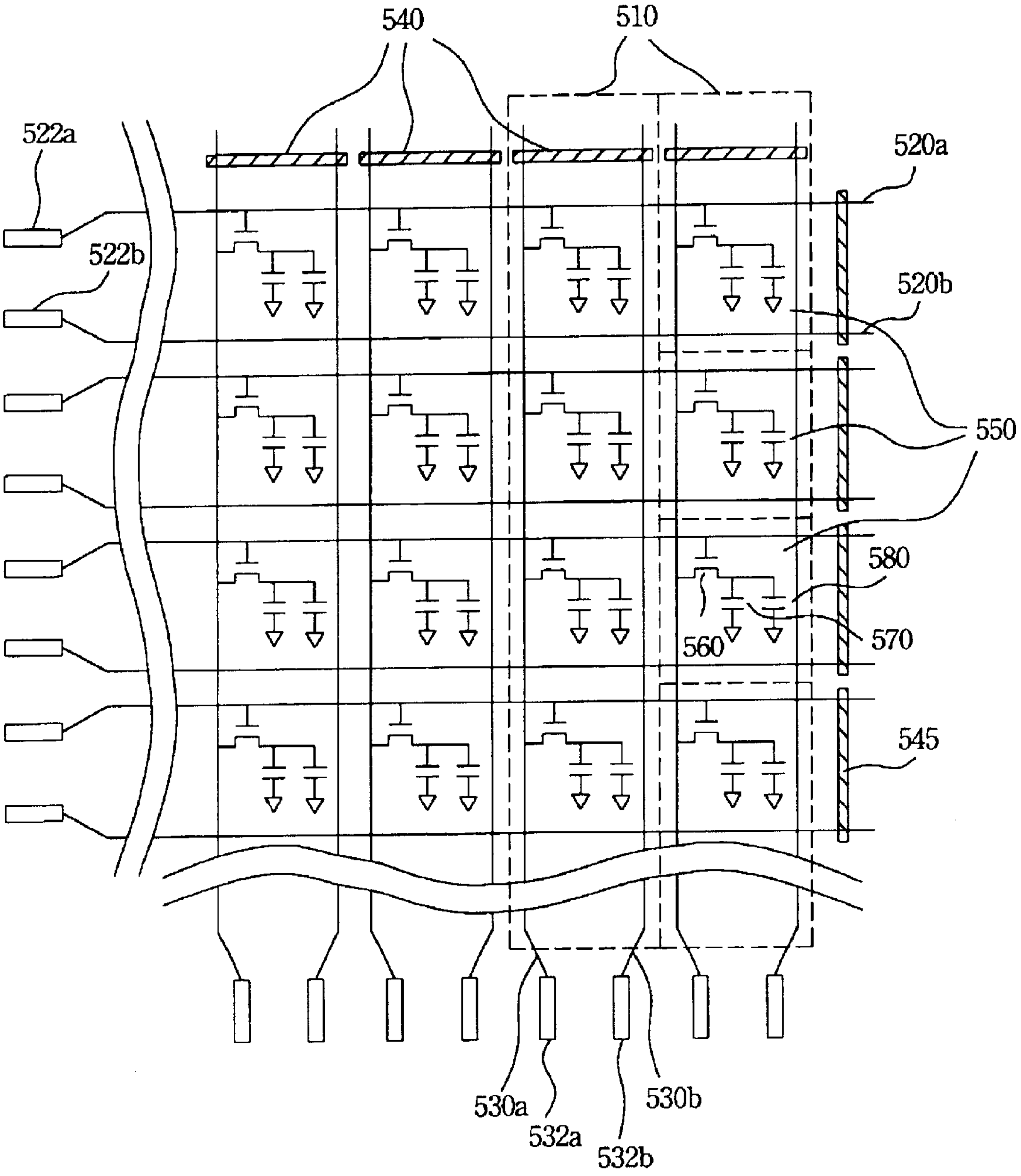

540
510
522a
520a
522b
520b
550
580
570
560
545
530a
532a
532b
530b

FIG. 5

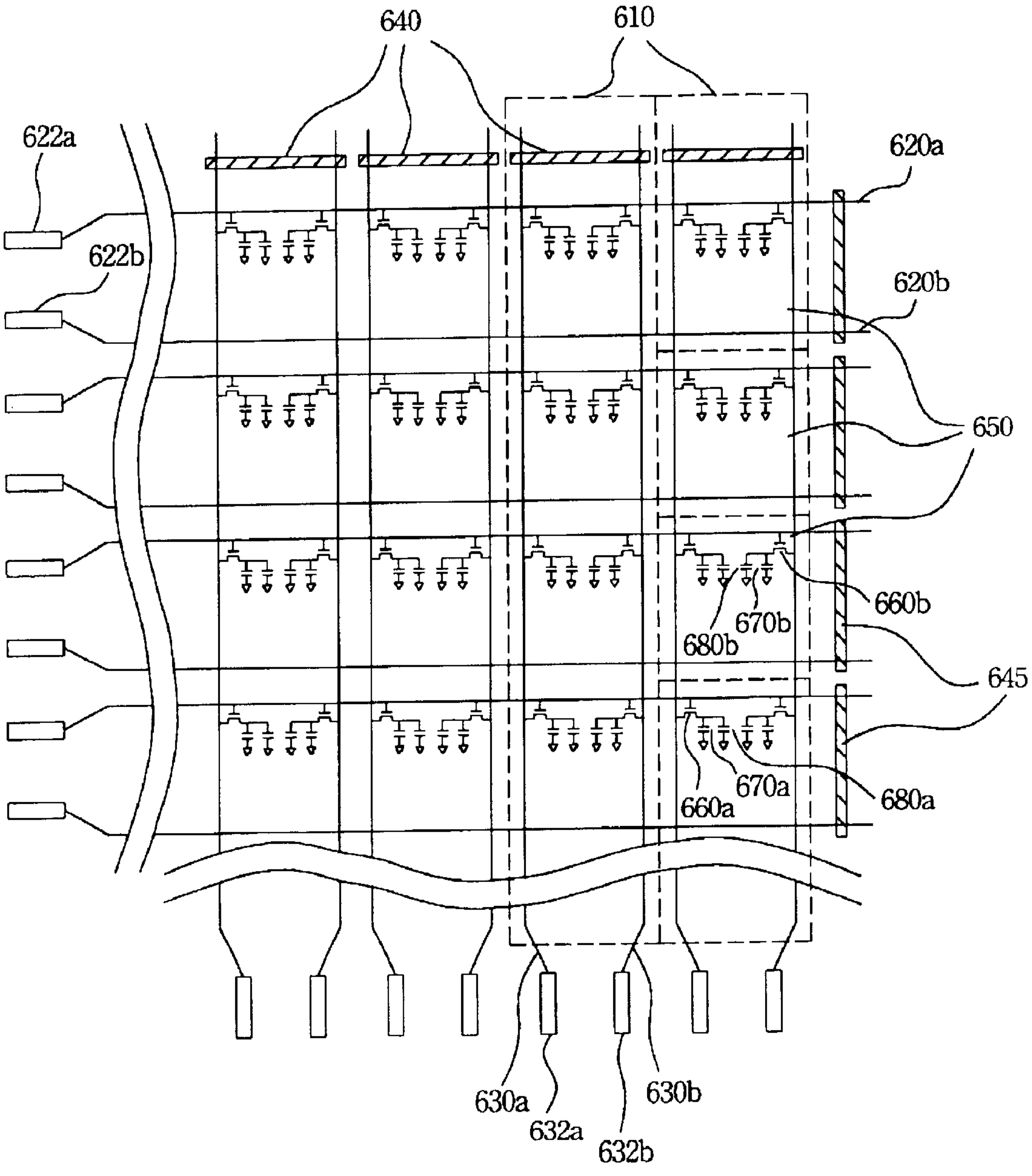

640
610
622a
622b
620a
620b
650
660b
670b
680b
645
670a
660a
680a
630a
632a
632b
630b

FIG. 6 A

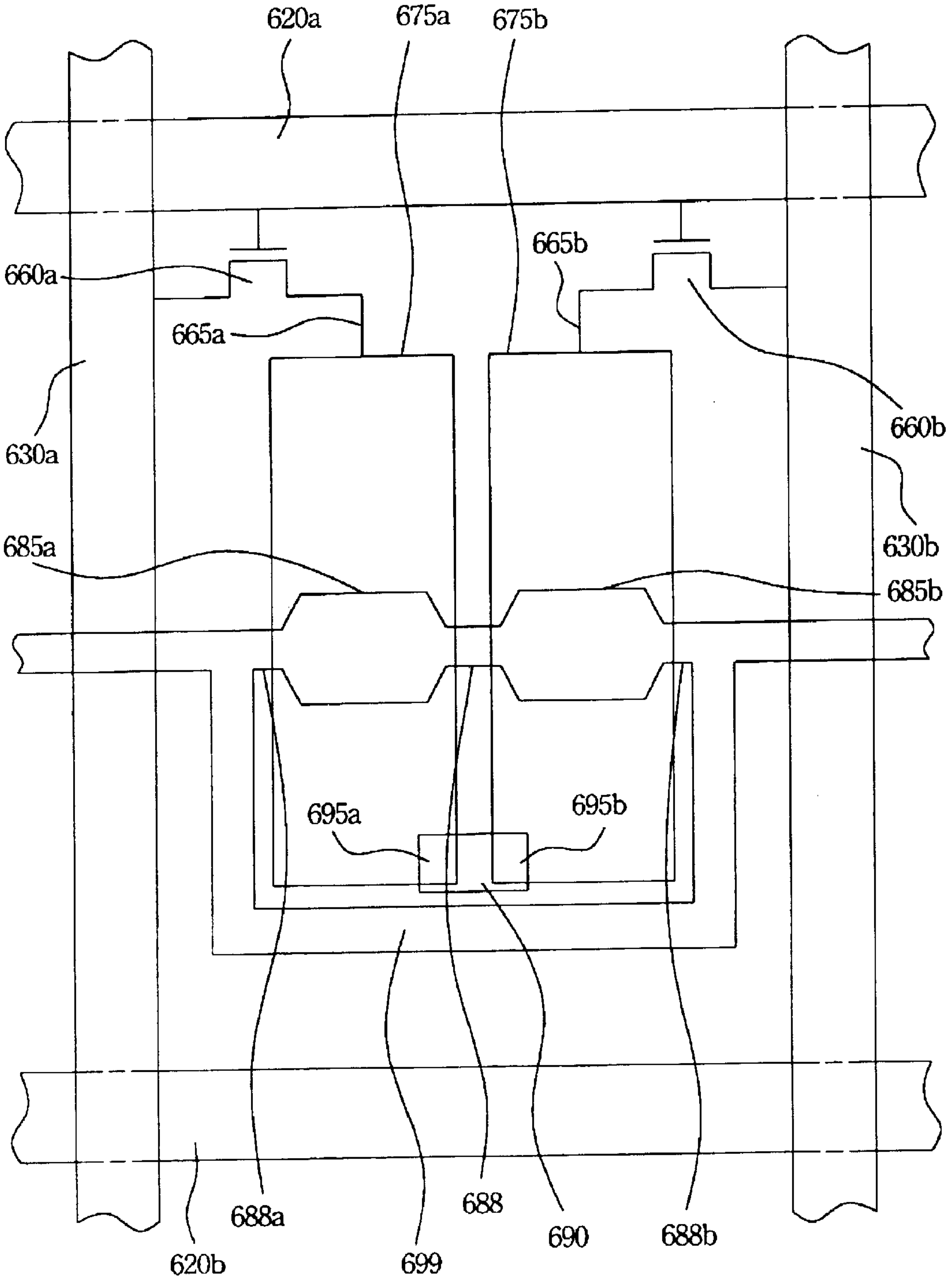

620a
675a
675b
665b
660a
665a
630a
660b
630b
685a
685b
695a
695b
688a
688
690
688b
620b
699

FIG. 6 B

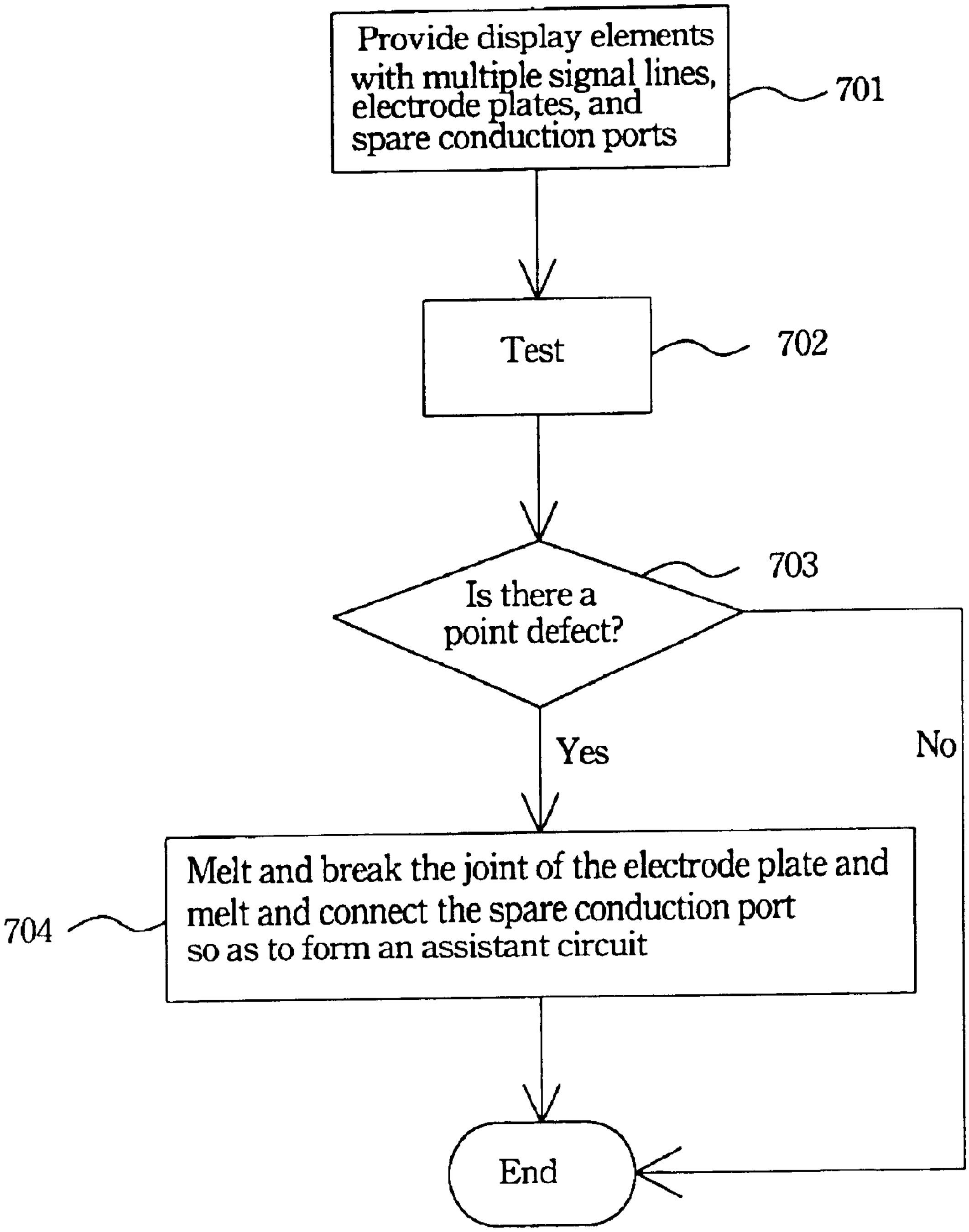

Provide display elements with multiple signal lines, electrode plates, and spare conduction ports
701
Test
702
703
Is there a point defect?
Yes
No
Melt and break the joint of the electrode plate and melt and connect the spare conduction port so as to form an assistant circuit
704
End

FIG. 7

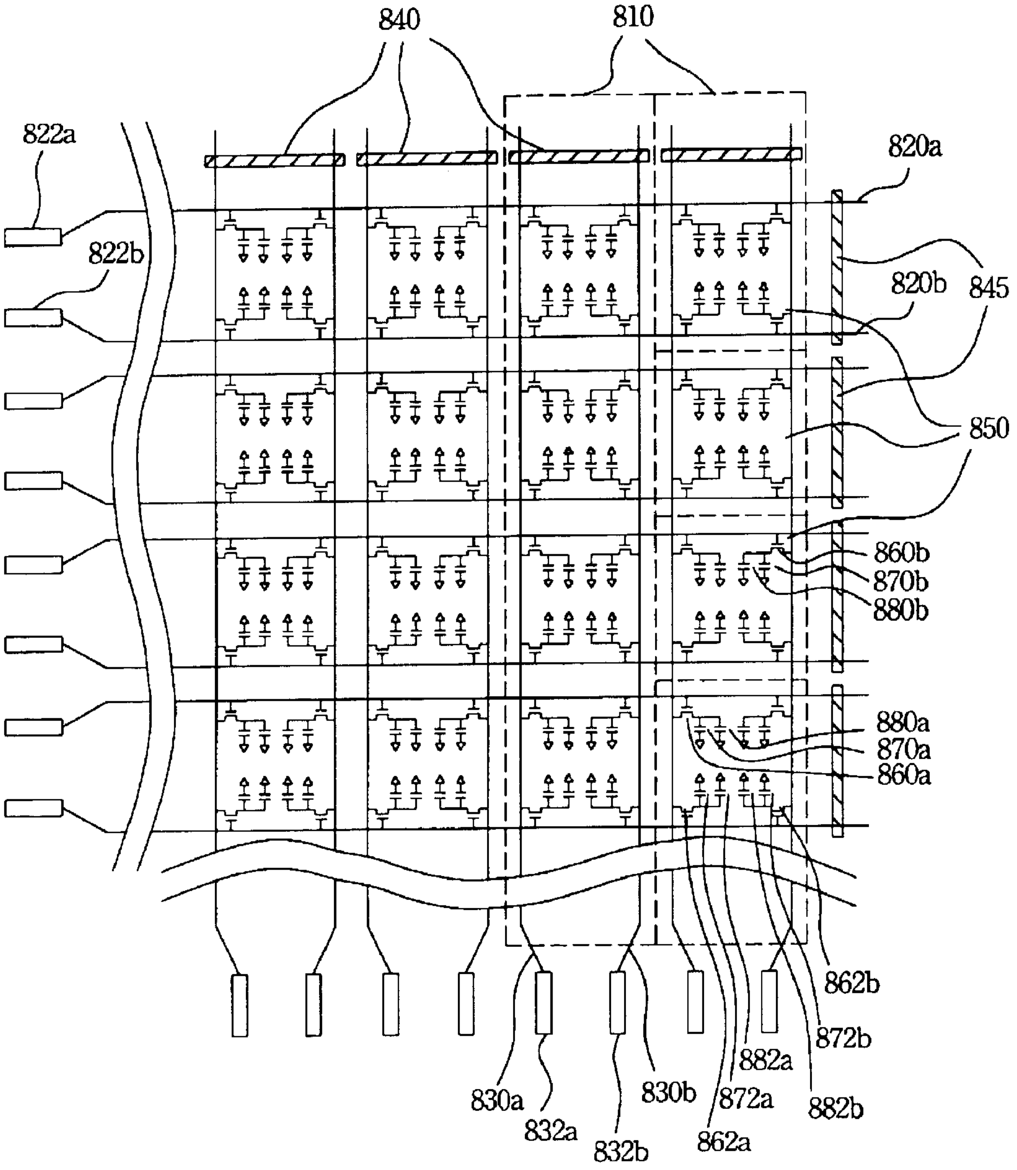

840
810
822a
820a
822b
820b
845
850
860b
870b
880b
880a
870a
860a
862b
872b
882a
830a
832a
830b
872a
882b
832b
862a

FIG. 8 A

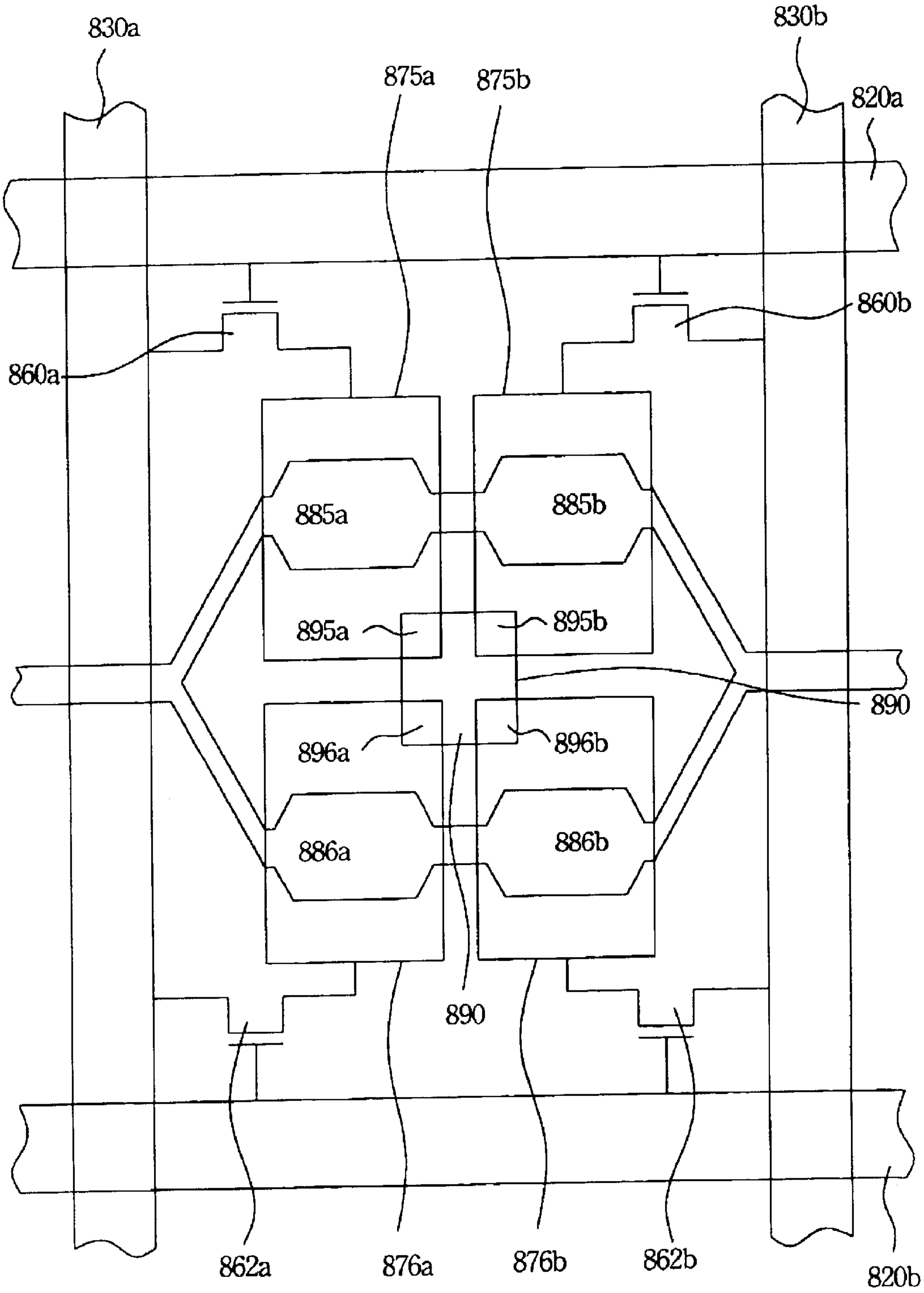

830a
875a
875b
830b
820a
860b
860a
885a
885b
895a
895b
890
896a
896b
886a
886b
890
862a
876a
876b
862b
820b

FIG. 8 B

LIQUID CRYSTAL DISPLAY ELEMENT WITH A DEFECT REPAIRING FUNCTION

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention relates to a liquid crystal display (LCD) element and, in particular, to an LCD element with a defect repairing function. The invention also discloses a defect repairing method.

2. Related Art

With the merits of small volume and light weight, liquid crystal display (LCD) holds the edge in the market of portable display devices and smallspace application displays. Among all, the thin film transistor liquid crystal display (TFT-LCD) is the most favorable device. The device is using the field effect transistors to control the voltage applied to the liquid crystal film layer so as to control the orientation of liquid crystal molecules, thus adjusting the penetration of light through the liquid crystal layer. With the utilization of filters, a screen is able to display various colors and brightness.

FIG. **1**A shows a standard circuit layout of a thin film transistor liquid crystal display (TFT-LCD) panel. A series of parallel scan lines **10** and a series of parallel data lines **20** are orthogonal to each other and not connected. They connect to a control electrode **12** and a control electrode **22**, respectively, and separate the display panel into an array composed of pixels. Each pixel in the array has a field effect transistor (FET) **30**, a liquid crystal capacitor **40** and a storage capacitor **50**. Each FET has a gate, a drain and a source, wherein the gate connects to the corresponding scan line, and the drain connects to the corresponding data line. The liquid crystal capacitor **40** and the storage capacitor **50** are connected in parallel between the drain of the FET **30** and the ground.

In the conventional LCD elements, a detailed standard layout of each pixel is shown in FIG. **1**B. The conduction areas **32**, **34**, **36** are the gate, source, and drain of the FET **30**, respectively. The area **38** is the semiconductor channel of the transistor **30**. The FET drain **36** connects to a transparent electrode plate **45**, which functions simultaneously as the electrodes for the liquid crystal capacitor **40** and the storage capacitor **50**. The transparent electrode plate **45** is usually made of indium tin oxide (ITO). A storage electrode plate **52** is installed underneath the transparent electrode plate **45** with a dielectric layer inserted between (not shown) so as to form a storage capacitor **50**. The liquid crystal capacitor **40** is formed above the transparent electrode plate **45**.

With the technology development of displays heading toward high screen quality and large sizes, manufacturers have to use narrower line width and smaller pixel sizes to make longer signal transmission lines (including scan lines and data lines) on the large-scale panels. Under this situation, such problems as uneven line width distribution and broken lines are likely to happen. It is also likely to have short circuits because of holes between separated electrodes, e.g., between the upper and lower electrode plates of the storage capacitor **50** (the transparent electrode plate **45** and the storage electrode plate **52**), between the FET gate **32** and the source and drain **34**, **36**, or between channels **38**. Broken signal lines will result in line defects since an entire row of pixels cannot receive control signals. Short circuits of electrode plates will cause point defects as the pixels cannot react to the voltage. Both of them have bad influence on the quality and the production yield of the display panels.

FIG. **2**A shows a pixel array circuit for repairing line defects in the prior art. The basic circuit layout is the same as in FIG. **1**A, except that the array border is surrounded with a spare line **80** over three sides. The spare line **80** is floating and striding over the data lines and scan lines, with a dielectric layer between. Its cross-sectional view is shown in FIG. **2**B. The conduction layer **210** on the substrate **200** representing the signal lines **10** on the lower layer, and the conduction layer **230** representing the spare line **80** on the upper layer are segregated by a dielectric layer **220** inserted between. When no defect is detected in the display panel, the spare line is maintained in the default configuration. However, when one of the data lines is detected to have a line defect, i.e., the data line is broken because of discontinuity, then the spare line overlapping on the defective data line is melted (usually using a high energy laser) so that the conductive material can pass through the dielectric isolation layer to form a contact window **240** with the conductive wire on the lower layer. When both ends of the defective data line are connected to the conduction layer **210** by melting, the spare line **80** can replace the broken data line and transmit control signals to transistors.

Nevertheless, this line defect repairing design still has its drawbacks. The spare line is so long and strides over so many data lines and scan lines that parasitic capacitance effect occurs during the control signal transmission. The signal received by the transistors will be decreased and seriously distorted, resulting in bad screen images. In addition, this surrounding spare line design cannot repair multiple defects, such as line defects indicated above. To further increase the product quality and manufacturing yield and to control production costs, it is crucial to develop a better defect repairing method.

SUMMARY OF THE INVENTION

In view of the foregoing bad defect repairing ability in conventional liquid crystal display (LCD) panel, it is an object of the invention to provide an LCD element with good defect repairing ability and the corresponding defect repairing method capable of repairing line defects and point defects due to broken circuits and short circuits, respectively.

To repair the line defects, the invention provides a circuit design of a single pixel having multiple scan lines and multiple data lines, with separate spare lines installed between. When a broken circuit occurs to any data line or scan line, the spare line is electrically welded to connect to the broken circuit, thereby forming the shortest connection path. This can minimize the signal attenuation due to long wiring and is suitable for multiple line defect repairs.

To repair point defects, the invention provides a circuit design of a single pixel having multiple subpixel electrodes, with spare conduction ports installed between. With the application of welding and connecting joints, the defective electrode can be readily separated once any subpixel has a defect. The spare conduction port for connection is melted for connection, and the resource of other subpixels will be used to support and compensate for the defective subpixel in an attempt to decrease the loss in screen image signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will make a specific demonstration in virtue of the detailed description along with the figures given below:

FIG. **1**A shows the array circuit layout of a conventional LCD element;

FIG. **1**B shows the pixel layout of a conventional LCD element;

FIG. **2**A shows the array circuit layout of a conventional LCD element that has spare data lines;

FIGS. **2**B and **2**C shows a schematic cross-sectional view of the spare data line configuration and welding in a conventional LCD element;

FIG. **3** is an array circuit layout of an LCD element with multiple data lines according to a first embodiment of the invention;

FIG. **4** is a flowchart showing the signal line defect test and repairing according to the first embodiment LCD element circuit;

FIG. **5** is an array circuit layout of an LCD element with multiple data lines and multiple scan lines according to a second embodiment of the invention;

FIG. **6**A is an array circuit layout of an LCD element with two subpixels according to a third embodiment of the invention;

FIG. **6**B is a pixel layout of the LCD element with two subpixels according to the third embodiment of the invention;

FIG. **7** is a flowchart showing the signal line defect test and repairing according to the third embodiment LCD element circuit;

FIG. **8**A is an array circuit layout of an LCD element with four subpixels according to a third embodiment of the invention; and

FIG. **8**B is a pixel layout of the LCD element with four subpixels according to the third embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a liquid crystal display (LCD) element with a defect repairing function. The invention also proposes a repairing method for line defects and point defects. As this invention adopts the design of multiple data lines and multiple scan lines assisted with the installation of spare lines, line defects due to broken circuits can be easily repaired. Furthermore, as each display pixel forms multiple subpixels by using multiple electrode plates and with the connection of multiple signal lines and the installation of spare conduction ports, point defects due to short circuits in pixel electrodes or control transistors can be repaired. So the present invention can greatly increase the quality and yield of the LCD elements. The invention utilizes many widely known circuit elements and manufacturing techniques in the prior art, such as field effect transistor (FET) manufacturing processes and wire melting and connecting technologies which will not be further described hereinafter.

With reference to FIG. **3**, the circuit adopts a multiple data line configuration that uses more than one data line to provide display control signals to the same pixel. In this embodiment, the LCD element is composed of a plurality of parallel optical display rows **310** and a plurality of scan lines **320** orthogonal to each optical display row **310**. One terminal of each scan line connects to a source pad **322***a*, **322***b* for signal input.

Each optical display row **310** has at least two correlation data lines **330***a*, **330***b* with one terminal connecting to source pads **332***a*, **332***b* for signal input, respectively. They are also orthogonal to the scan lines **320**. A spare line **340** is provided between the two correlation data lines **330***a*, **330***b*. The spare lines for different display rows are allocated separately without connection to each other. In a preferred embodiment, the spare line **340** is installed between the terminals of the correlation data lines **330***a*, **330***b* near the border of the display element. The spare line **340** of each optical display row **310** is floating above the two correlation data lines **330***a*, **330***b* so that it can be melted for connection. In this embodiment, the configuration can be achieved by overlapping and isolation, as shown in FIG. **2**B.

Each optical display row **310** is separated into a series of pixels **350** by orthogonal scan lines **320**. Each pixel **350** corresponds to a scan line **320** and two correlation data lines **330***a*, **330***b*. In the first embodiment, each pixel **350** comprises a field effect transistor (FET) **360**, a liquid crystal capacitor **370**, and a storage capacitor **380**. Each FET **360** has a gate, a drain, and a source, wherein the gate connects to the corresponding scan line **320** and the drain connects to either data line **330***a* or **330***b* in the same optical display row **310**. The liquid crystal capacitor **370** and the storage capacitor **380** are connected in parallel between the drain and ground of the FET **360**.

Using a circuit composed of the LCD element according to the first embodiment, the defects in the LCD element caused by broken data lines can be easily repaired. With reference to FIG. **4**, the display element mentioned in the first embodiment is provided in step **401**. The display element is provided with multiple correlation data lines **330***a* and **330***b* with spare lines **340** installed between. When the elementary manufacturing process for the display element is finished, all spare lines **340** and correlation data lines **330***a*, **330***b* are isolated from each other before defect tests and repairs.

Afterwards, each gate pad **322** and source pad **332***a*, **332***b* sends control signals to perform tests (step **402**) and (step **403**). If any line defect caused by broken data lines is found in the test process, repairing can be carried out immediately (step **404**). The repairing focuses on the broken data line. The intervening areas between the separated spare line **340** and the corresponding two correlation data lines **330***a*, **330***b* are welded so that the broken data line and the correlation data lines **330***a*, **330***b* are electrically connected through the spare line **340**. Therefore, the data line that has an open circuit with the source pads **332***a*, **332***b* due to broken lines will connect to the corresponding source pads **332***a*, **332***b* via the correlation data lines **330***a*, **330***b* and the spare line **340**. Once the defect is repaired, the source pads **332***a*, **332***b* of each set of correlation data lines in the display element are coupled to the same signal input terminal. Thus, the original broken data line will receive the same control signals of data line through the correlation data lines achieving predetermined display effects and the goals of repairing defects as well as increasing element quality and the manufacturing yield.

Referring to FIG. **5**, the configuration of multiple data lines and multiple scan lines is adopted in the second embodiment. More than one data line and more than one scan line provide display control signals to the same pixel. In the current embodiment, the LCD element is composed of a plurality of parallel optical display rows **510** and a plurality of pairs of correlation scan lines **520***a*, **520***b*, orthogonal to each optical display row **510**. One terminal of each scan line connects to a gate pad **522***a* or **522***b* as signal input terminal.

Each optical display row **510** contains at least two correlation data lines **530***a* and **530***b*, with the source pads **532***a* and **532***b* installed at the terminals thereof as signal input terminals. A data spare line **540** is disposed between two correlation data lines **530***a*, and **530***b*. In a preferred embodiment, the data spare line **540** is installed at the terminals of the two correlation data lines **530***a* **530***b* near the display element border. The data spare line **540** of each optical display row **510** is electrically floating over the terminals thereof so that it can be melted. This configuration can be achieved by the aforesaid overlapping and separating method. Furthermore, a scan spare line **545** is floating between each pair of correlation scan lines **520***a*, **520***b* near the terminals thereof. The data spare lines **540** between different optical display rows **510** and the scan spare lines **545** between different sets of correlation scan lines **520***a*, **520***b* are installed separately without connection to each other.

Each optical display row **510** is divided into a series of pixels **550** by orthogonal correlation scan lines **520***a* and **520***b*. Each pixel corresponds to a pair of correlation scan lines **520***a*, **520***b* and two correlation data lines **530***a*, **530***b*. In the second embodiment, each pixel **550** includes an FET **560**, a liquid crystal capacitor **570** and a storage capacitor **580**, similar to the first embodiment. Each FET **560** has a gate, a drain, and a source, wherein the gate connects to any of the corresponding scan lines **520***a*, **520***b*, the source connects to any of the data lines **530***a*, **530***b* in the same optical display row **510**. The liquid crystal capacitor **570** and the storage capacitor **580** are connected in parallel between the drain and the ground of the FET **560**.

Using a circuit composed of the LCD element in the second embodiment, defects caused by broken data lines or scan lines in the LCD element can be simultaneously repaired. All test and repairing procedures are the same as in FIG. **4** as long as the display elements mentioned in the second embodiment is provided and the repairing procedure for data lines is utilized identically to the broken scan lines. Before performing defect tests and repairing, all data spare lines **540** and correlation data lines **530***a*, **530***b*, as well as the scan spare lines **545** and correlation scan lines **520***a*, **520***b*, are isolated from one another. After the repairing is complete, the originally broken data line or scan line will connect to the associated data line or scan line through the spare line, respectively. The source pads of each set of the correlation data lines and the gate pads of each set of the correlation scan lines are then coupled to the same signal input terminal, respectively, to receive the same control signals, thus achieving expected display effects.

The repairing circuit and technologies for point defects is further described in the following embodiments. With reference to FIG. **6**A for the third embodiment of the disclosed LCD element, a two-subpixel configuration is adopted in addition to the multiple data lines and multiple scan lines. Two subpixel electrodes receive the same control signals and generate the same display signals to form a complete LCD pixel. In this embodiment, the LCD element is composed of a plurality of parallel optical display rows **610** and a plurality of pairs of correlation scan lines **620***a*, **620***b* that are orthogonal to each optical display row **610**. One terminal of each scan line **620***a*, **620***b* connects to gate pad **622***a* or **622***b* as signal input terminal.

Each optical display row **610** contains at least two correlation data lines **630***a*, **630***b*, with the source pads **632***a*, **632***b* installed at the terminals thereof as signal input terminals. The two correlation data lines **630***a*, **630***b* are also orthogonal to the scan lines **620***a*, **620***b*. A data spare line **640** is situated between the two correlation data lines **630***a*, **630***b*, preferably at the terminals thereof near the display element border. A scan spare line **645** between each pair of correlation scan lines **620***a*, **620***b* is also provided. The scan spare line **645** is also preferably installed at the terminals of the correlation scan lines **620***a*, **620***b* near the display element border. The data spare line **640** and the scan spare line **645** are electrically floating and can be welded. The data spare lines **640** between different optical display rows **610**, as well as the scan spare lines **645** between different sets of correlation scan lines **620***a*, **620***b*, are installed separately without connection to each other.

Each optical display row **610** is divided into a series of pixels **650** by orthogonal correlation scan lines **620***a*, **620***b*. Each pixel corresponds to a pair of correlation scan lines **620***a*, **620***b* and two correlation data lines **630***a*, **630***b*. In the third embodiment, each pixel **650** includes two FETs **660***a*, **660***b*, two liquid crystal capacitors **670***a*, **670***b*, and two storage capacitors **680***a*, **680***b*. The FET **660***a*, the liquid crystal capacitor **670***a*, and the storage capacitor **680***a* form one subpixel; the FET **660***b*, the liquid crystal capacitor **670***b*, and the storage capacitor **680***b* form another subpixel. Each FET **660***a*, **660***b* has a gate, a drain, and a source, wherein the two gates connect to any of the corresponding scan lines **620***a*, **620***b* respectively or together, the two sources connect to any of the correlation data lines **630***a*, **630***b* of the same optical display row **610** respectively or together. In the embodiment as shown in FIG. **6**A, the two gates connect to the same scan line **620***a*, the two sources connect to the different data lines **630***a* and **630***b*. The liquid crystal capacitor **670***a* and the storage capacitor **680***a* are connected in parallel between the drain and the ground of the FET **660***a*; the liquid crystal capacitor **670***b* and the storage capacitor **680***b* are connected in parallel between the drain and the ground of the FET **660***b*.

In other embodiments related to two-subpixel, each pixel can be associated with a single scan line and two correlation data lines or, alternatively, each pixel is associated with a single data line and two correlation scan lines. Each subpixel in the former case corresponds to a distinct data line and the same scan line. Each subpixel in the later case corresponds to a distinct scan line and the same data line.

Please refer to FIG. **6**B for a pixel layout of the disclosed LCD element in the third embodiment. Since the layout of the FETs **660***a*, **660***b* are not the feature of the invention, they are referred to as element symbols. The disclosed design of multiple data line and/or multiple scan line configuration or the multiple subpixel configuration described hereinafter, regardless of the deployment of FETs **660***a*, **660***b*, are within the scope of the present invention.

As shown in FIG. **6**B, the third embodiment of the pixel layout contains two transparent electrode plates **675***a*, **675***b*, respectively connecting to the drains of FETs **660***a*, **660***b*. The transparent electrode plate **675***a* serves as the electrode of the liquid crystal capacitor **670***a* and the storage capacitor **680***a*, and the transparent electrode plate **675***b* is used as the other electrode of the liquid crystal capacitor **670***b* and the storage capacitor **680***b*. A spare conduction port **690** is electrically floating over the two transparent electrode plates **675***a*, **675***b* with the overlapping areas **695***a*, **695***b*. In addition, the spare conduction ports **690** of different pixels are not connected to each other.

The liquid crystal pixel has an electrode plate **685***a*, **685***b* isolating from the transparent electrode plates **675***a*, **675***b* by a dielectric layer (not shown) to form storage capacitors **680***a*, **680***b*. Since each storage electrode plate **685***a*, **685***b* in all pixels need to ground, all the storage electrode plates are connected to each other through a conductive wire. In the same pixel, the storage electrode plates **685***a*, **685***b* are electrically connected to each other through a connection port **688**. Both ends of the storage electrode plates **685***a*, **685***b* are connected via a spare connection wire **699** to form an auxiliary pathway. The spare connection wire **699** and the storage electrode plates **685***a*, **685***b* are coupled through the connection ports **688***a*, **688***b*, respectively. In the above layout, the connection ports **688**, **688***a*, **688***b*, the joint **665***a* between the transparent electrode plate **675***a* and the drain of the FET **660***a*, and the joint **665***b* between the transparent electrode plate **675***b* and the drain of the FET **660***b* can all be welded.

Using a circuit composed of the LCD elements in the third embodiment, line defects of the LCD elements and points defects caused by FET failures or short circuits in the transparent electrode plates can be readily repaired. The repairing procedure for line defects is as shown in FIG. **4** and the related description. The procedure for the point defect tests and repairing of the transparent electrode plates is shown in FIG. **7**. In the course of repairing, the display elements mentioned in the third embodiment are provided (step **701**) at first. The display element has to include multiple subpixels, subpixel electrodes **675***a*, **675***b*, and spare conduction ports **690** provided in between. The spare conduction port **690** and the two electrode plates **675***a*, **675***b* are disconnected before the defect tests and repairing.

Afterwards, each gate pad **622***a*, **622***b* and source pad **632***a*, **632***b* inputs control signals to perform tests (step **702**) such that any failure in the electrode plate **675***a* or **675***b* (step **703**) can be diagnosed. If any point defect caused by electrode plate failure is found in the display element during the test process, repairs can be performed right away (step **704**). The repairing is performed on the pixel with failed electrode plate, and the failed portion needs to be isolated. When the FET fails, the joint **665***a* or **665***b* between the electrode plate **675***a*, **675***b* and the FET drain is cut. When a short circuit between the electrode plate **675***a*, **675***b* and the corresponding storage electrode plate **685***a*, **685***b* occurs, the corresponding connection port **688** and **688***a* or **688***b* is cut. If the problem is unable to locate, the failed electrode plate and the FET, and the storage electrode plate **685***a*, **685***b* and the ground terminal are disconnected simultaneously.

Once the failed portion of the pixel is isolated, the overlapping area between the spare conduction port **690** and the two electrode plates **675***a*, **675***b* is welded so that the two electrode plates **675***a* and **675***b* of the failed pixel are connected through the conduction port **690**, forming a new coupled circuit. Therefore, the originally failed electrode plate connects to another FET drain through the spare conduction port **690** and another electrode plate. After the defect is repaired, the source pads **632***a*, **632***b* of each set of correlation data lines in the display element are coupled to the same signal input terminal, the gate pads **622***a*, **622***b* of each set of correlation scan lines also are coupled to the same signal input terminal. In a regular pixel, two FETs are used to drive two liquid crystal capacitors and two storage capacitors. In the defect-repairing pixel, however, one FET is used to drive two liquid crystal capacitors and one storage capacitor. The originally failed electrode plate will be charged and driven by the corresponding FET of another electrode plate to a predetermined voltage through the connection of the spare conduction port **690**. By this method, it can attain the expected display effect and the goal of repairing defects and enhancing element quality and yield.

FIG. **8**A shows circuit configuration of the LCD element in the fourth embodiment. In addition to the above-mentioned multiple data lines and multiple scan lines, a four subpixel configuration is further adopted such that the four subpixel electrodes receive the same control signals and generate the same display signals, forming a complete LCD pixel. In this embodiment, the LCD element is composed of a plurality of parallel optical display row **810** and a plurality of correlation scan line pairs **820***a*, **820***b* disposed orthogonal to each optical display row **810**, respectively. The gate pads **822***a*, **822***b* are installed at the terminals of each scan line pair **820***a*, **820***b* as signal input terminals.

Each optical display row **810** contains at least two correlation data lines **830***a*, **830***b* with the source pads **832***a*, **832***b* installed at the terminals thereof as signal input terminals. The correlation data lines **830***a*, **830***b* are also orthogonal to the scan lines **820***a*, **820***b*. A data spare line **840** is provided between the two correlation data lines **830***a*, **830***b* whose location is preferably at the terminals of the two correlation data lines **830***a*, **830***b* near the display element border. A scan spare line **845** is also provided between each pair of the correlation scan lines **820***a*, **820***b*, which is also preferably installed at the terminals of the two correlation scan lines **820***a*, **820***b* near the display element border. Each data spare line **840** and the scan spare lines **845** are allocated separately without connection to each other.

Each optical display row **810** is separated into a series of pixels **850** by orthogonal correlation scan line pairs **820***a* and **820***b*. Each pixel corresponds to a pair of correlation scan lines **820***a*, **820***b* and two correlation data lines **830***a*, **830***b*. In the fourth embodiment, each pixel **850** has four FETs **860***a*, **860***b*, **862***a*, **862***b*, four liquid crystal capacitors **870***a*, **870***b*, **872***a*, **872***b*, and four storage capacitors **880***a*, **880***b*, **882***a*, **882***b*, totally forming four subpixels. Each FET has a gate, a drain, and a source, wherein the gates of the FETs **860***a*, **860***b* connect to the same scan lines **820***a*, and the gates of the FETs **862***a*, **862***b* connect to the same scan lines **820***b*. The sources of the FETs **860***a*, **862***a* connect to the same data line **830***a* of the optical display row **810**. The sources of the FETs **860***b*, **862***b* connect to the same data line **830***b* of the optical display row **810**. The liquid crystal capacitor **870***a* and the storage capacitor **880***a* are connected in parallel between the drain and the ground of the FET **860***a*; the liquid crystal capacitor **870***b* and the storage capacitor **880***b* in parallel between the drain and the ground of the FET **860***b*; the liquid crystal capacitor **872***b* and the storage capacitor **882***b* in parallel between the drain and the ground of the FET **862***b*; and the liquid crystal capacitor **872***b* and the storage capacitor **882***b* in parallel between the drain and the ground of the FET **862***b*.

With reference to FIG. **8**B, the FETs **860***a*, **860***b*, **862***a*, **862***b* are referred to by element symbols since they are not the features of the invention. The previously disclosed design of multiple data lines and/or multiple scan lines with multiple subpixels, despite of the deposition of the FETs **860***a*, **860***b*, **862***a*, **862***b*, are within the scope of the invention.

As shown in FIG. **8**B, the pixel layout has four transparent electrode plates **875***a*, **875***b*, **876***a*, **876***b* connecting to the drains of the FETs **860***a*, **860***b*, **862***a*, **862***b*, respectively. The transparent electrode plate **875***a* serves as the electrode of the liquid crystal capacitor **870***a* and the storage capacitor **880***a*; the transparent electrode plate **875***b* is used as the electrode of the liquid crystal capacitor **870***b* and the storage capacitor **880***b*; the transparent electrode plate **876***a* serves as the electrode of the liquid crystal capacitor **872***a* and the storage capacitor **882***a*; and the transparent electrode plate **876***b* is used as a electrode of the liquid crystal capacitor **872***b* and the storage capacitor **882***b*.

A spare conduction port **890** is partially overlapping and floating over the four transparent electrode plates **875***a*,

875*b*, **876***a*, **876***b*. The overlapping areas include **895***a*, **895***b*, **896***a* and **896***b*. Spare conduction ports **890** of different pixels are not connected.

The liquid crystal pixel has the storage electrode plates **885***a*, **885***b*, **886***a*, **886***b* overlapping-but isolated from the transparent electrode plates **875***a*, **875***b*, **876***a*, **876***b* by a dielectric layer (not shown), forming the storage capacitors **880***a*, **880***b*, **882***a*, **882***b*. Each storage electrode plate in all pixels is connected by a conductive wire and coupled to the ground. In the above layout, all connection ports among the storage electrode plates and the joints between the transparent electrode plates and the FET drains are meltable.

Using a circuit composed of the LCD elements in the fourth embodiment, repair line defects or point defects because of electrode plate short circuits or FET failure can be easily repaired. The line defect repairing procedure is shown in FIG. **4** and the related description, the point defect test and repairing procedure is shown in FIG. **7**. Before performing defect tests and repairing, the spare conduction port **890** and all electrode plates **875***a*, **875***b*, **876***a*, **876***b* are separated and not connected. When any electrode plate of the pixel is found to be defective, the electrode plate and the corresponding storage capacitor are separated from the corresponding transistor and ground, and the spare conduction port **890** and all the electrode plates **875***a*, **875***b*, **876***a*, **876***b* are melted and electrically connected. After repairing, the good pixel uses four FETs to drive four liquid crystal capacitors and four storage capacitors, whereas the repaired defective pixel uses three FETs to drive four liquid crystal capacitors and three storage capacitors. Through the spare conduction port **890**, the originally defective electrode plate is charged by the transistors of the other three electrode plates a predetermined voltage. This can then achieve expected display results, repair defects and increase the element quality and yield.

In summary, the invention uses a circuit design of a single pixel associated with multiple scan lines and multiple data lines for repairing line defects. Between the multiple scan lines and multiple data lines of the same pixel, a separated spare line is provided to melt and connect the data lines or scan lines of the broken circuit, forming the shortest connection path. This can minimize the transmission distance, stray capacitance, and signal attenuation. This method is also applicable to multiple line defect repairs. Furthermore, the invention provides a circuit design of a single pixel associated with a plurality of subpixels for repairing point defects. A spare conduction port is provided between the subpixel electrodes of the same pixel. Through the utilization of meltable joints and the connection with multiple signal lines, the defective electrode at any pixel can be isolated and the spare conduction port can be melted for connection. By exercising the resource of other subpixels to support and compensate the defective subpixel, the screen quality of the entire pixel can be maintained, thereby minimizing the loss in screen signals.

The scope of this invention is not limited to the above description with reference to specific embodiments. Various modifications of the disclosed embodiments, as well as alternative embodiments, will be apparent to persons skilled in the art. For example, one can use more than two correlation scan lines and/or data lines on the same pixel. One can also use a spare line to selectively connect all correlation scan lines or data lines. Alternatively, one can use dividable spare lines so that the correlation scan lines or data lines can be selectively connected to each other. The spare conduction port can have a similar design. A plurality of spare conduction ports can be selectively connected between the subpixel electrode plates. At this moment, each pixel electrode plate corresponds to at least one spare conduction port and each spare conduction port corresponds to at least two subpixel electrode plates. The correspondence of the spare lines can use the similar pattern. It is, therefore, contemplated that the appended claims will cover all modifications that fall within the true scope of the invention.

What is claimed is:

1. A method of repairing line defects in liquid crystal display (LCD) elements, said method comprising the steps of:

providing an LCD element, wherein the LCD element comprises a plurality of scan lines and a plurality of optical display rows orthogonal to said scan lines, each of the optical display rows comprising at least two data lines, at least one spare line and a plurality of display pixels, the spare line being adapted to selectively connect any of the data lines in the respective optical display row with another data line in the same optical display row, and the spare lines of the different optical display rows being disconnected from each other;

testing the data lines of the LCD element; and

when a line defect is detected on one of the data lines, connecting the defective data line to another data line in the same optical display row through the associated spare line;

wherein, in the providing step, the spare line is formed to overlap and be electrically isolated from the data lines of the associated optical display row.

2. The method of claim **1**, wherein the step of connecting the defective data line to said another data line in the same optical display row through the associated spare line is implemented by melting.

3. The method of claim **1**, wherein said two data lines of each of said optical display rows are electrically connected, in said connecting step, through the associated spare line only if one of said two data lines is found defective in said testing step.

4. A liquid crystal display (LCD) element with a defect repairing function, said LCD element comprising:

a plurality of parallel scan lines; and

a plurality of optical display rows disposed orthogonal to the plurality of scan lines;

wherein each of the optical display rows at least includes:

two data lines, orthogonal to the plurality of scan lines;

a spare line, installed between the two data lines of the optical display row for selectively connecting the two data lines, wherein the spare line is electrically isolated from and overlaps said two data lines; and

a plurality of display pixels, each display pixel corresponding to at least one of the scan lines and each of the scan lines corresponding to one of the display pixels;

wherein each of the display pixels includes:

at least one field effect transistor (FET) having a gate, a drain, and a source, said FET corresponding to one of the scan lines and one of the data lines, wherein the gate is connected to the corresponding scan line and the source is connected to the corresponding data line; and

at least one transparent electrode corresponding to the FET, and being connected to the drain of the corresponding FET; and

wherein the spare lines of different said optical display rows are disconnected from each other.

5. The LCD element of claim **4**, wherein the spare line is electrically connectable to the two data lines by welding said spare line to said two data lines.

6. A liquid crystal display (LCD) element, comprising:

a plurality of parallel scan lines; and

a plurality of optical display rows disposed orthogonal to the plurality of scan lines, wherein each of the optical display rows at least includes:

two data lines, orthogonal to the plurality of scan lines;

a spare line, installed between the two data lines of the optical display row for selectively connecting the two data lines, wherein the spare line is electrically isolated from and overlaps said two data lines; and

a plurality of display pixels, each display pixel corresponding to at least one of the scan lines, wherein each of the display pixels includes at least one field effect transistor (FET) and each said FET having a gate, a drain, and a source, said FET corresponding to one of the scan lines and one of the data lines, wherein the gate is connected to the corresponding scan line and the source is connected to the corresponding data line;

wherein the spare lines of different said optical display rows are disconnected from each other.

7. The LCD element of claim **6**, wherein one of said two data lines is defective and the spare line is electrically connected to the two data lines.

8. The LCD element of claim **6**, wherein the drain is connected to a liquid crystal capacitor.

9. The LCD element of claim **6**, wherein each display pixel corresponds to one of the scan lines, and each of the display pixels includes one said field effect transistor (FET).

10. The LCD element of claim **9**, wherein one of said two data lines is defective and the spare line is electrically connected to the two data lines.

11. The LCD element of claim **9**, wherein the drain is connected to a liquid crystal capacitor.

* * * * *

专利名称(译)	具有缺陷修复功能的液晶显示元件		
公开(公告)号	US6753935	公开(公告)日	2004-06-22
申请号	US09/789591	申请日	2001-02-22
[标]申请(专利权)人(译)	群创光电股份有限公司		
申请(专利权)人(译)	奇美电子股份有限公司.		
当前申请(专利权)人(译)	群创光电		
[标]发明人	WU BIING SENG		
发明人	WU, BIING-SENG		
IPC分类号	G02F1/13 G02F1/1343 G02F1/1362 G02F1/133 G09F9/00 G09G3/20 G09G3/36 G02F1/1333 G01F1/1339		
CPC分类号	G02F1/1309 G02F1/13624 G02F2001/134345 G02F2001/136263 G02F2001/136268 G02F2001/136272		
优先权	089106351 2000-04-06 TW		
其他公开文献	US20010028429A1		
外部链接	Espacenet USPTO		

摘要(译)

一种具有缺陷修复功能的液晶显示（LCD）元件及其缺陷修复方法。在本发明的实施例中，像素与多条扫描线和多条数据线相关联。与单独的备用线一起，可以获得熔化连接以形成电路路径并补偿断线。单个像素还可以具有多个子像素，这些子像素具有备用传导端口和可熔接头，从而可以分离有缺陷的电极。备用传导端口可以熔化并连接，使得其他子像素支持并补偿有缺陷的子像素，以最小化像素信号损失。