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(54) **LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURING THE SAME**

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(57) **ABSTRACT**

A liquid crystal display includes a first substrate including pixels, each having a transmissive area and a reflective area, a second substrate, and a liquid crystal layer disposed between the first and second substrates. Each of the pixels includes first and second thin film transistors which output a data signal in response to a first gate signal, a transmissive pixel electrode disposed in the transmissive area and electrically connected to the first thin film transistor to charge a first pixel voltage based on the data signal, a reflective pixel electrode disposed in the reflective area and electrically connected to the second thin film transistor to charge a second pixel voltage based on the data signal, and a voltage controller which controls the first pixel voltage and the second pixel voltage in response to a second gate signal, which is generated after the first gate signal.

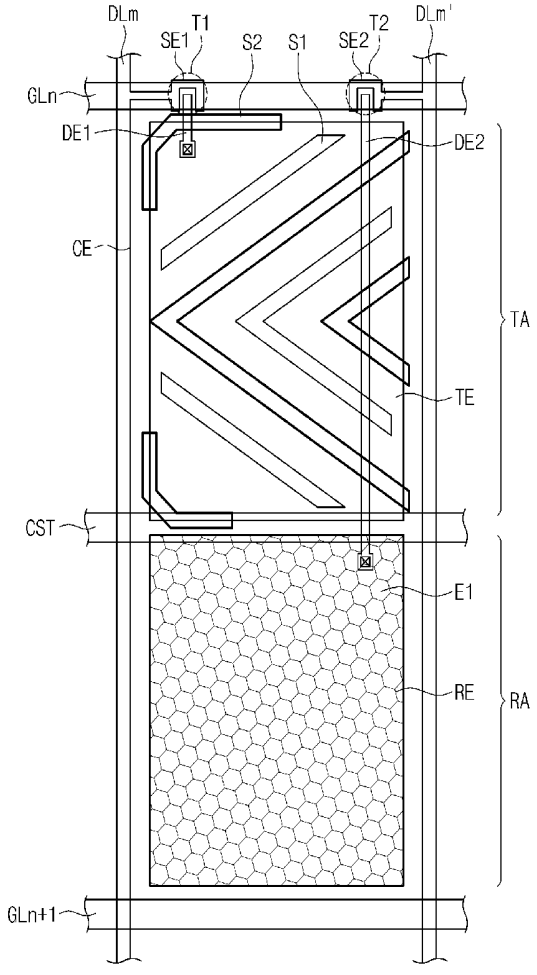
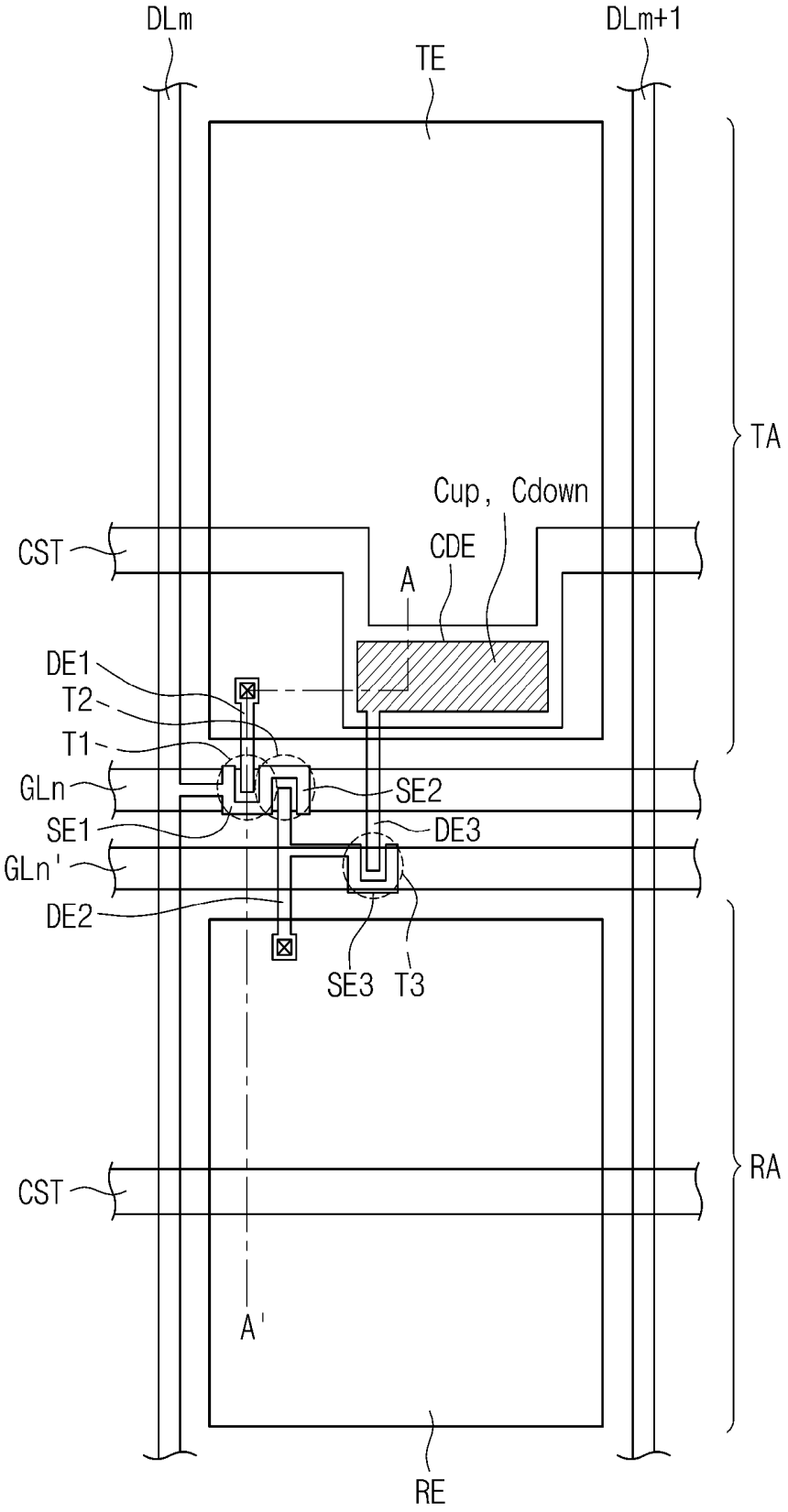


Fig. 1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DLm+1
TE
TA
Cup, Cdown
CST
CDE
A
DE1
T2
T1
GLn
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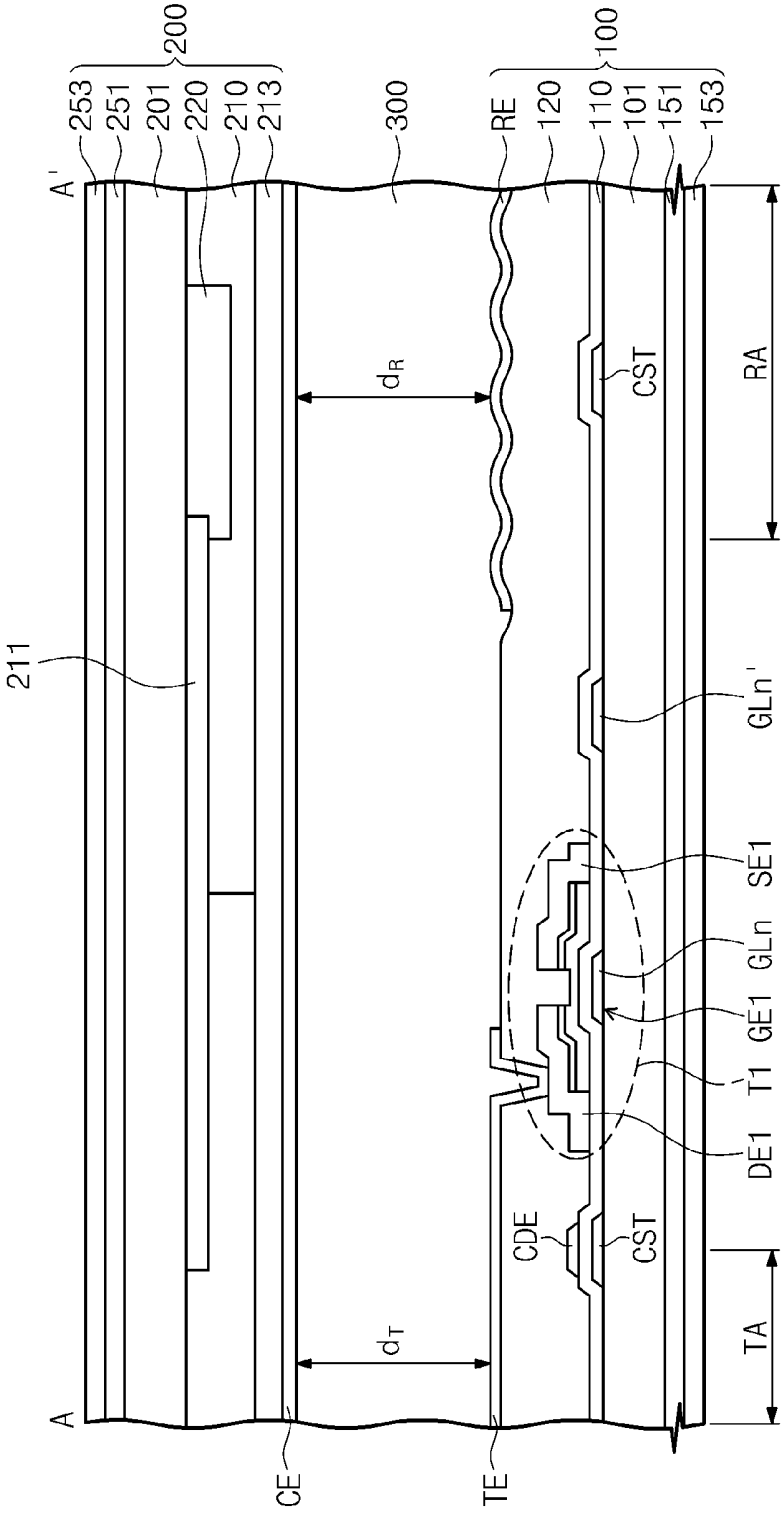
SE1
DE3
GLn'
DE2
SE3
T3
CST
RA
A'
RE

Fig. 2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253
251
201
220
210
213
300
RE
120
110
101
151
153
A'
A
211
d_R
d_T
CST
RA
GLn'
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GLn
GE1
T1
DE1
CDE
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CE
TE

Fig. 3

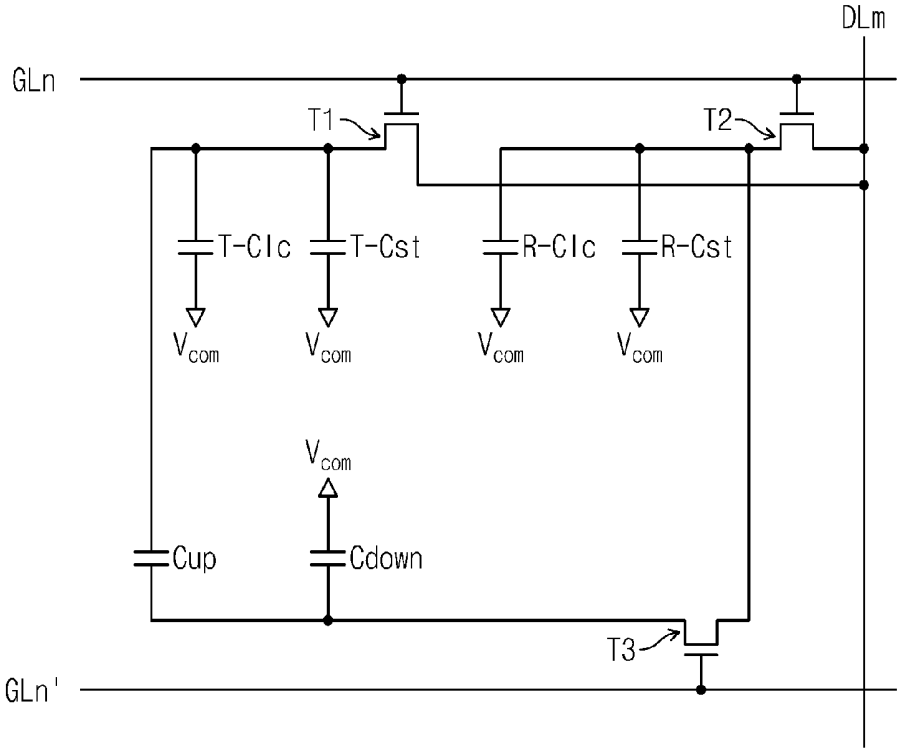

DLm
GLn
T1
T2
T-Clc
T-Cst
R-Clc
R-Cst
Vcom
Vcom
Vcom
Vcom
Vcom
Cup
Cdown
T3
GLn'

Fig. 4

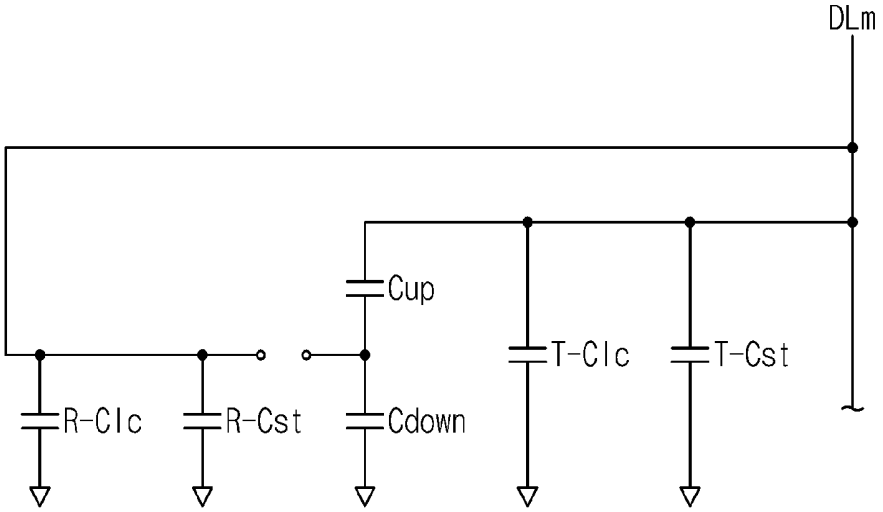

DLm
Cup
T-Clc
T-Cst
R-Clc
R-Cst
Cdown

Fig. 5

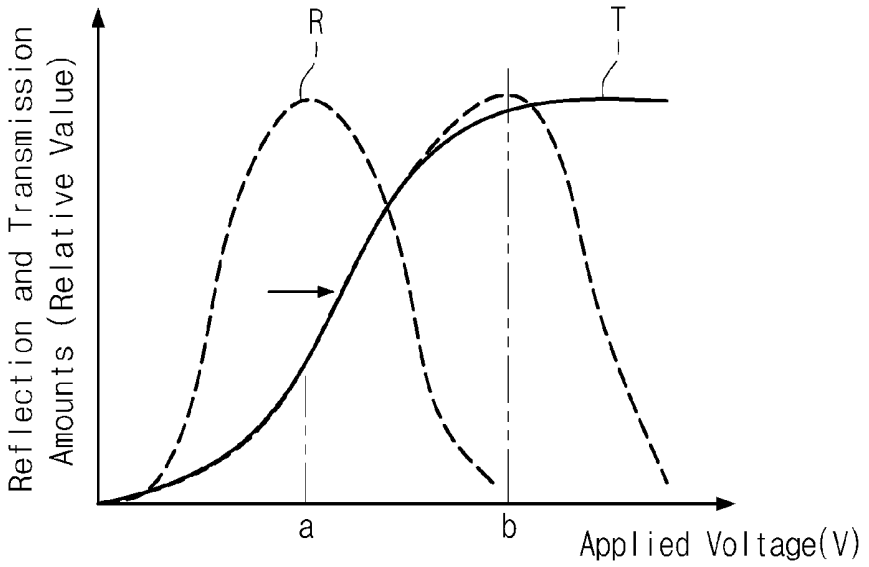
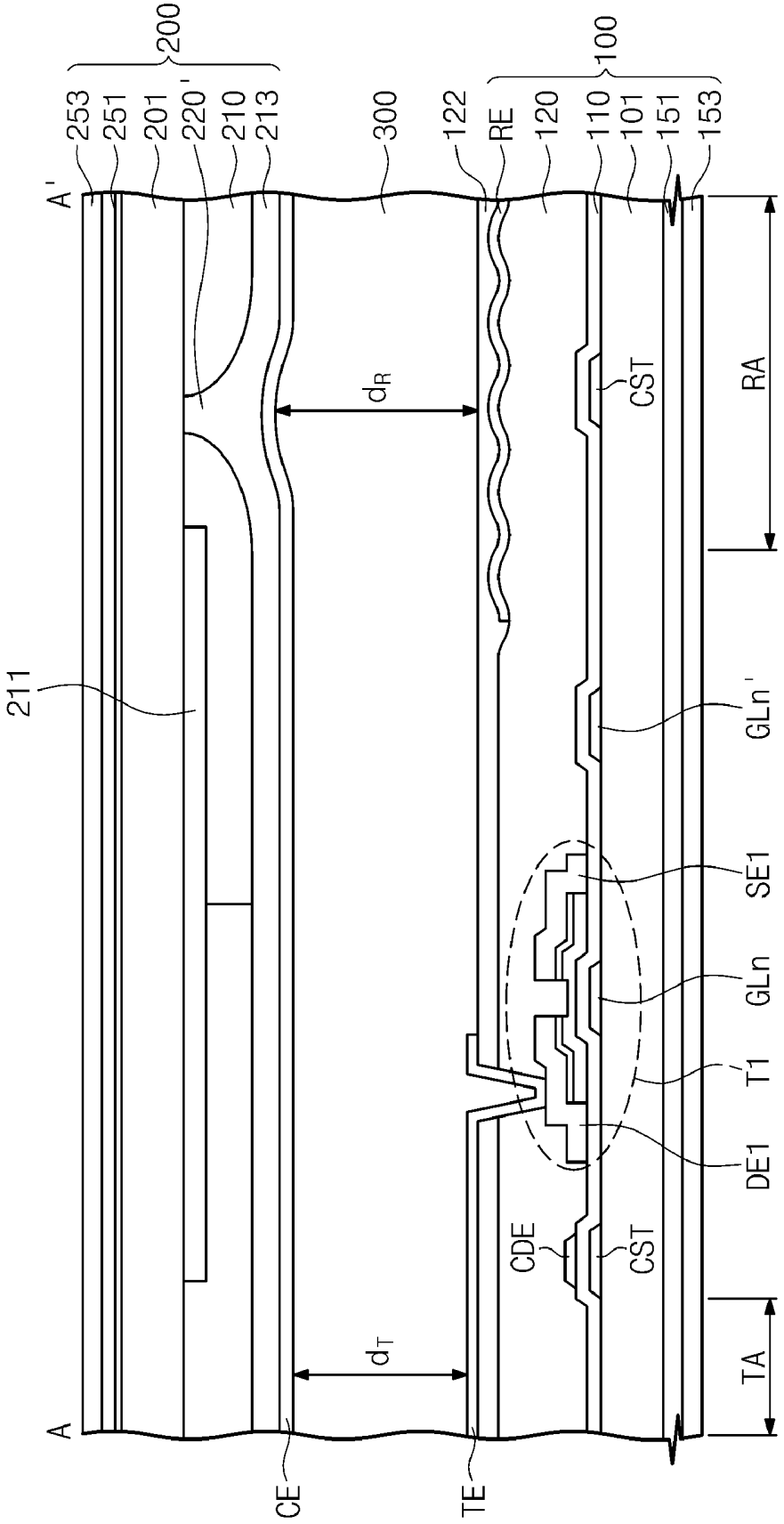

R
T
Reflection and Transmission Amounts (Relative Value)
a
b
Applied Voltage(V)

Fig. 6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100
253
251
201
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213
300
122
RE
120
110
101
151
153
A'
A
211
d_R
d_T
CST
RA
GLn'
SE1
GLn
T1
DE1
CDE
CST
TA
CE
TE

Fig. 7A

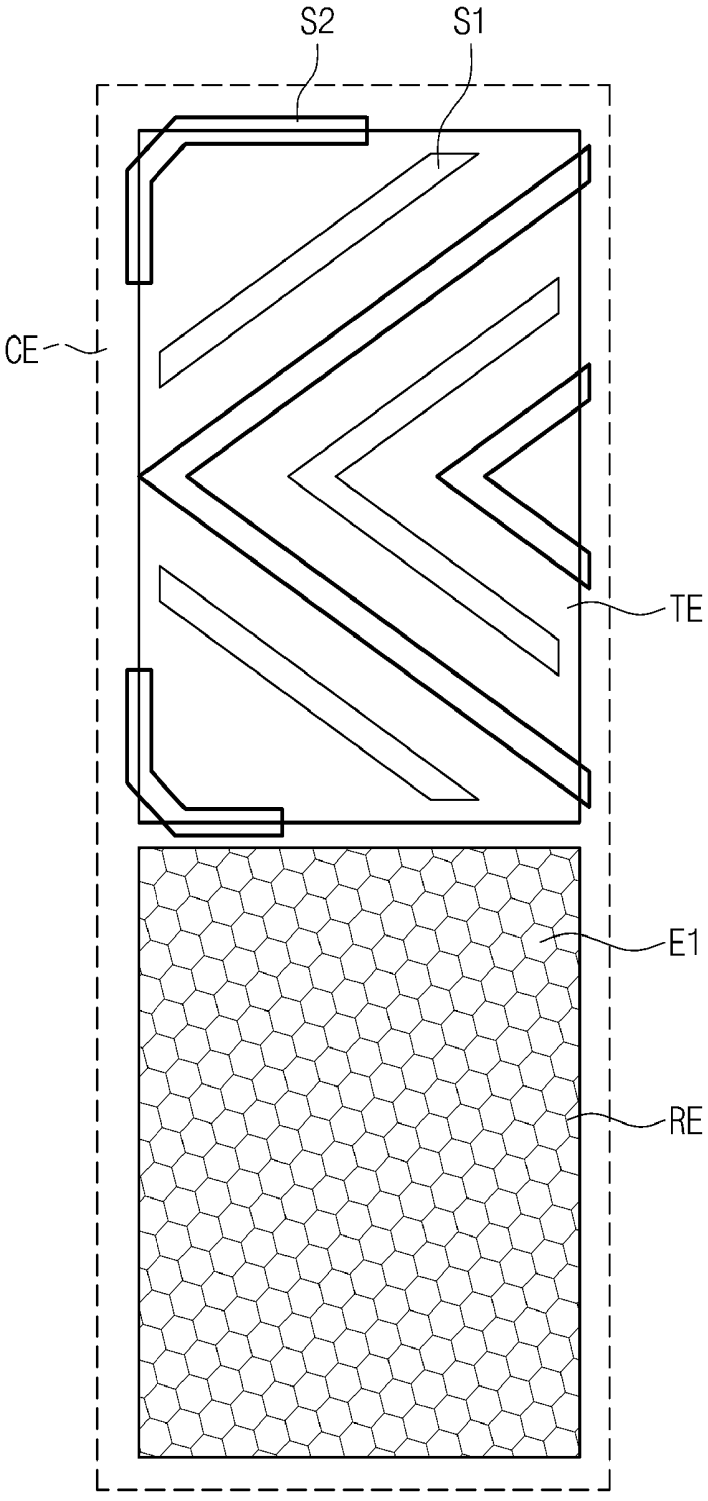


Fig. 7B

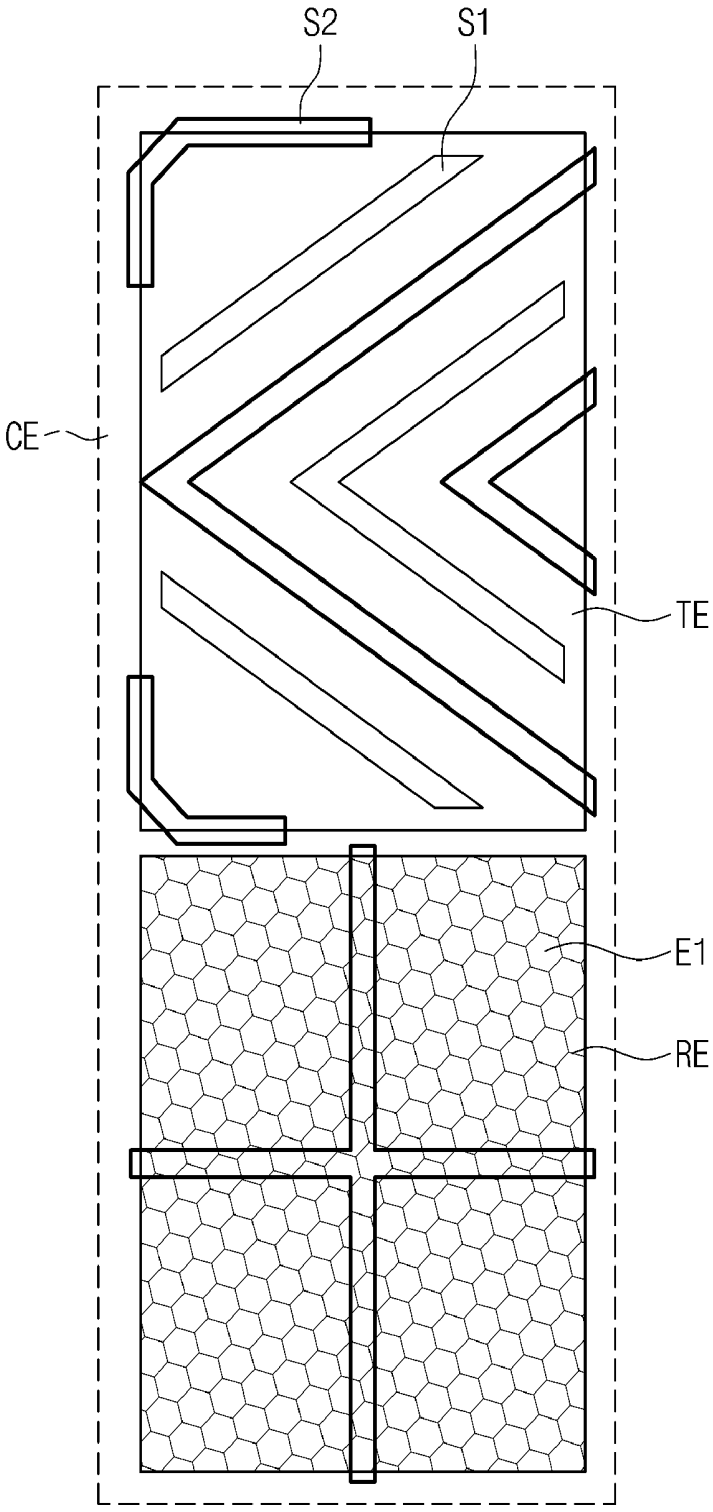


Fig. 7C

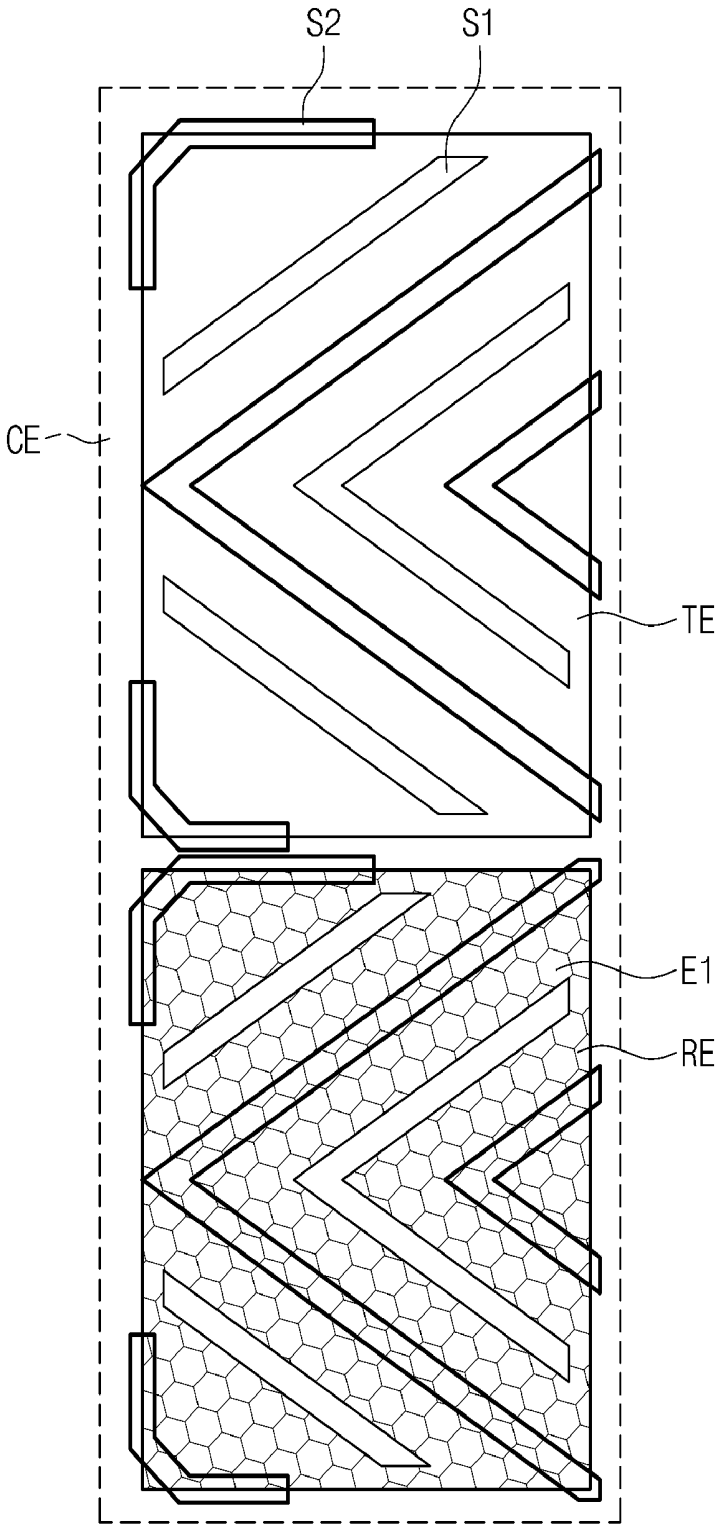


Fig. 7D

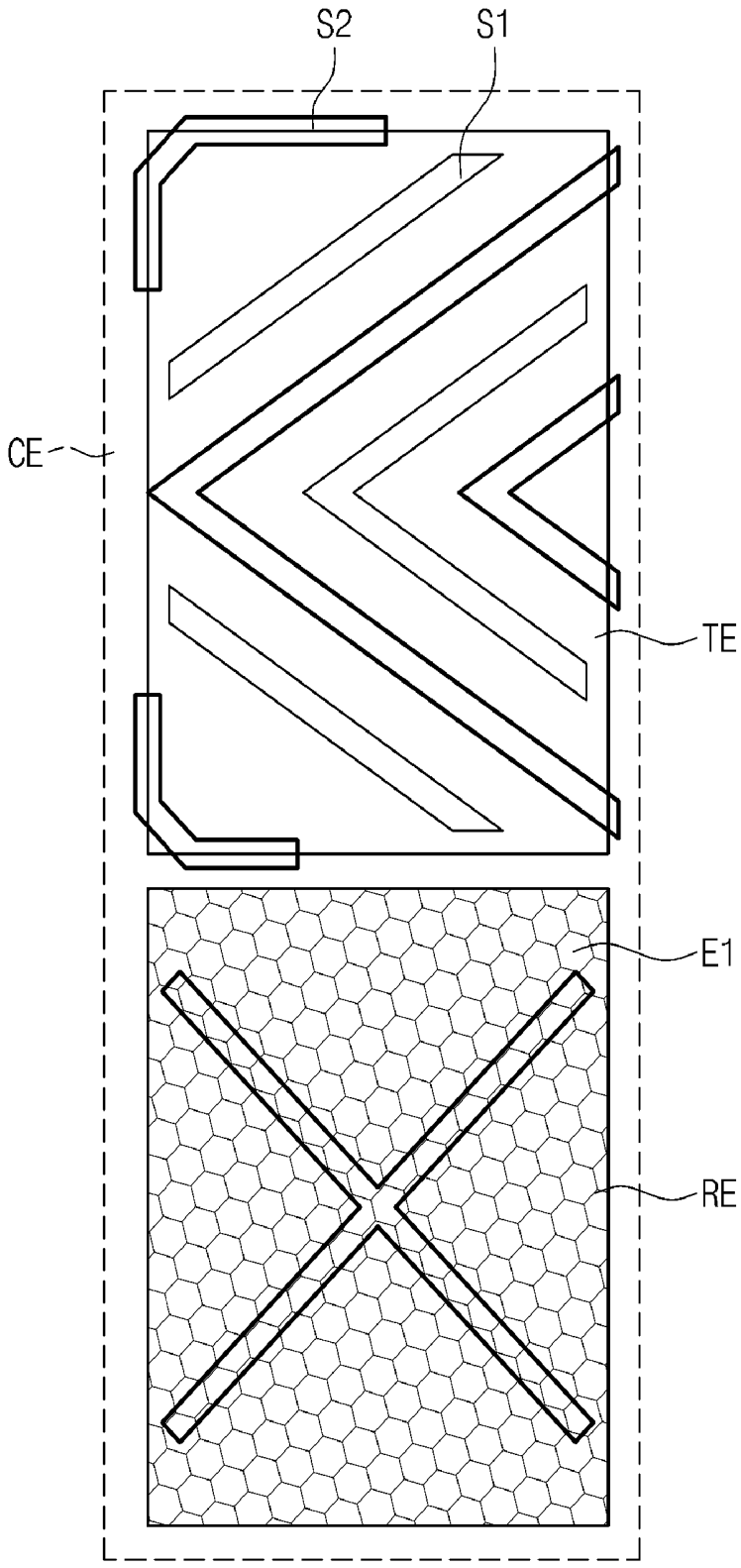


Fig. 7E

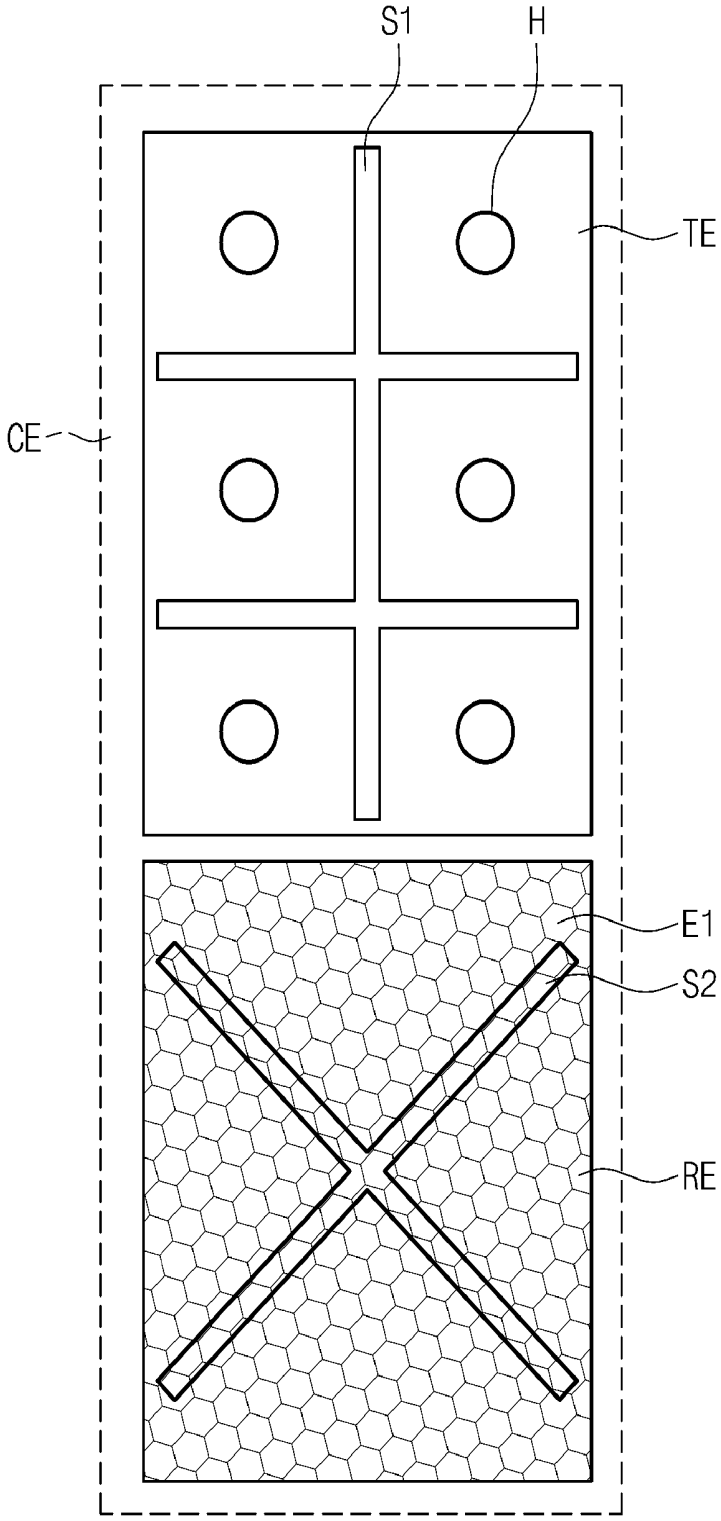
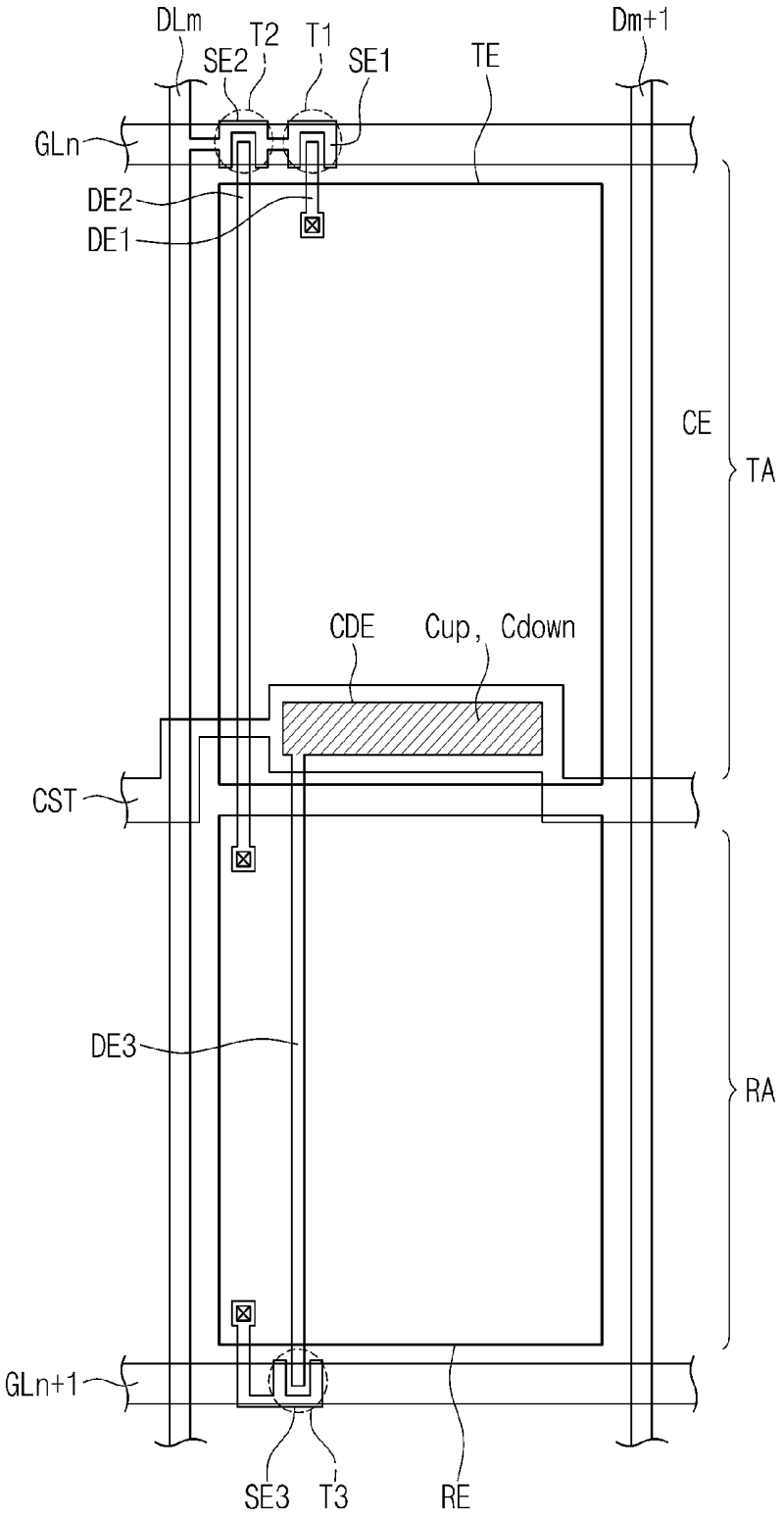


Fig. 8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T2
T1
SE2
SE1
TE
Dm+1
GLn
DE2
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CE
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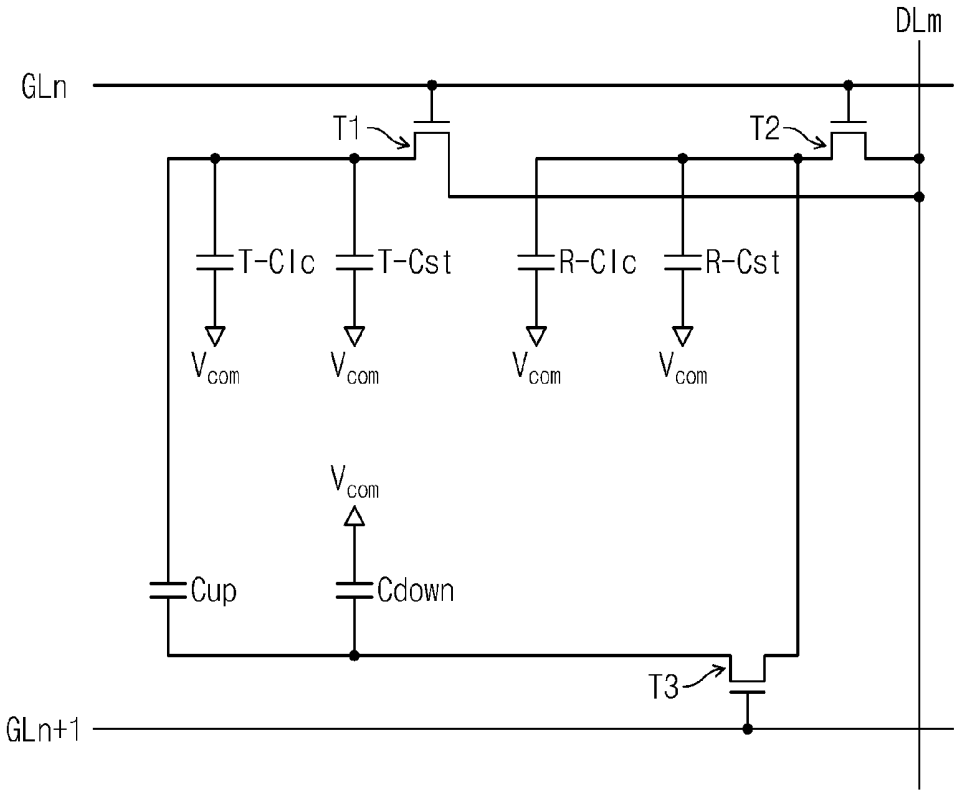
CDE
Cup, Cdown
CST
DE3
RA
GLn+1
SE3
T3
RE

Fig. 9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GLn
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T2
T-Clc
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Vcom
Vcom
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Vcom
Cup
Cdown
T3
GLn+1

Fig. 10

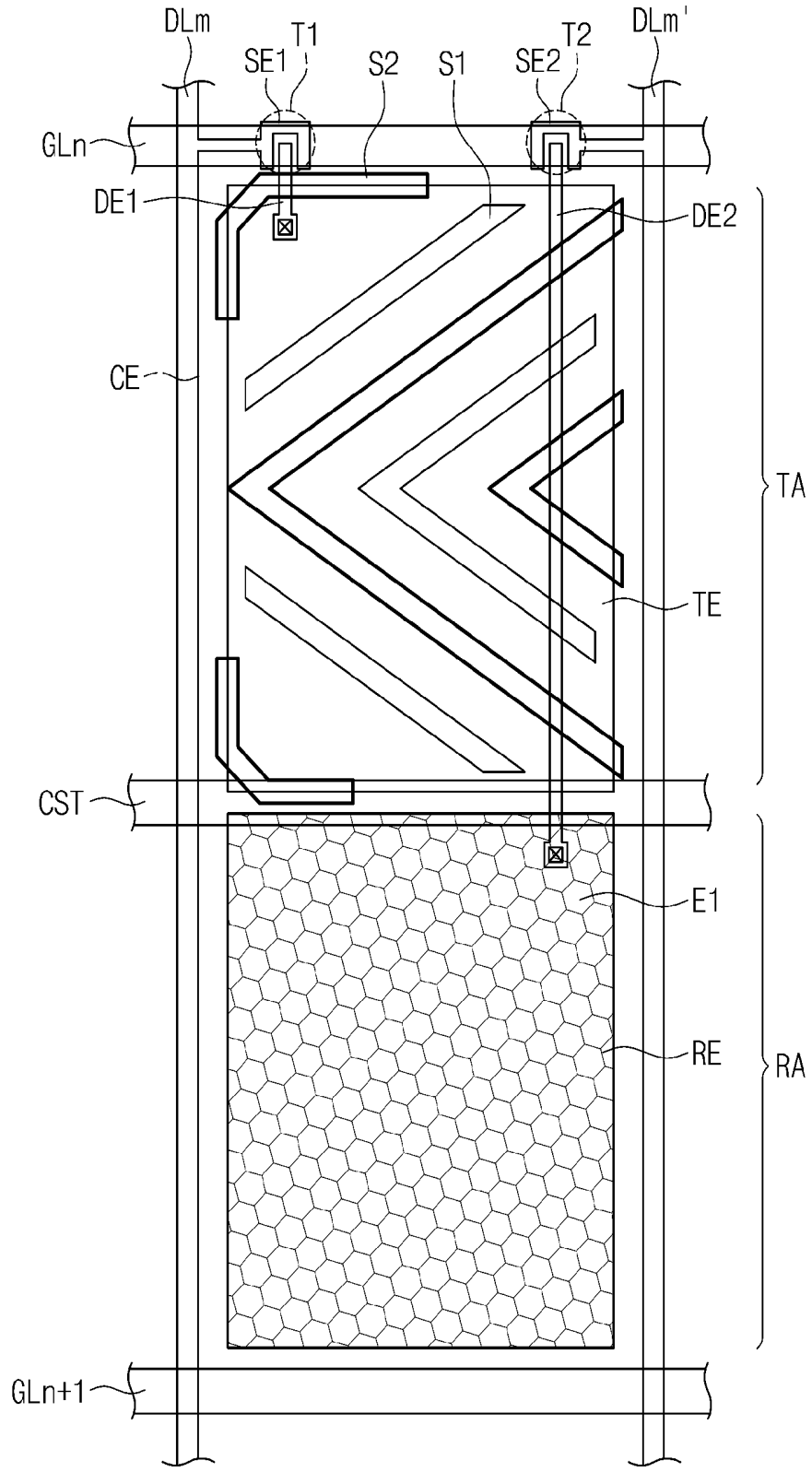
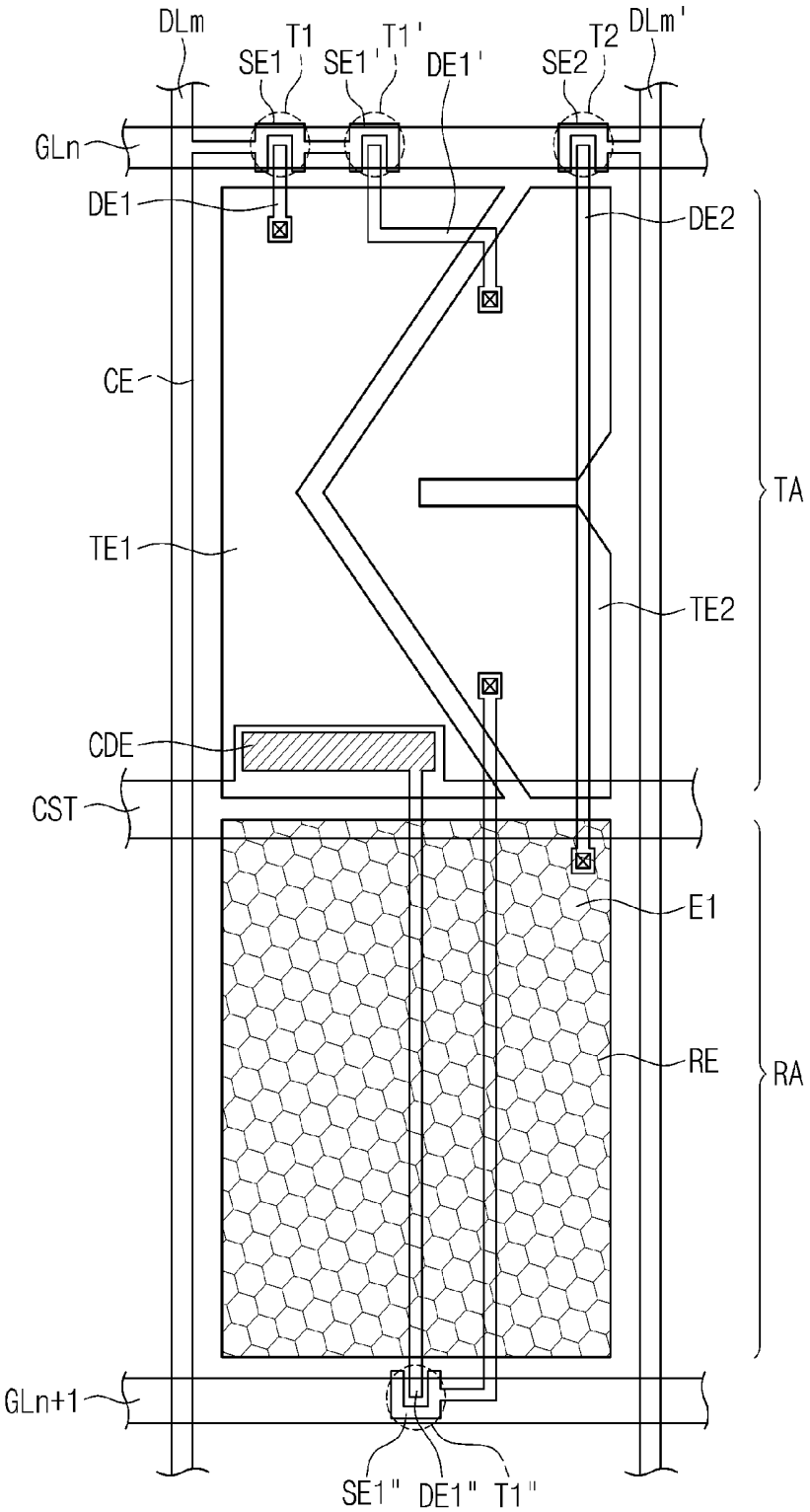


Fig. 11


DLm
T1
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DE1"
T1"

LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURING THE SAME

[0001] This application claims priority to Korean Patent Application No. 2009-59233, filed on Jun. 30, 2009, and all the benefits accruing therefrom under 35 U.S.C. §119, the content of which in its entirety is herein incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display and a method of manufacturing the liquid crystal display. More particularly, the present invention relates to a transflective liquid crystal display having a single cell gap and a method of manufacturing the liquid crystal display.

[0004] 2. Description of the Related Art

[0005] A liquid crystal display ("LCD") typically includes a liquid crystal layer disposed between two transparent substrates. To display a desired image, the LCD drives the liquid crystal layer to control a transmittance of light for each pixel.

[0006] In general, an LCD is classified as either a transmissive LCD, which displays an image using a backlight unit as a light source thereof, or a reflective LCD, which displays an image using natural light as a light source thereof, e.g., without requiring a backlight unit.

[0007] Compared to the reflective LCD, the transmissive LCD, which requires the backlight unit, has a high power consumption. Although it does not require a backlight, and thus consumes less power, the reflective LCD cannot display an image if there is insufficient ambient light.

[0008] In attempts to overcome the abovementioned problems with transmissive and reflective LCDs, a transflective LCD, which has both a reflective area and a transmissive area, has recently been suggested. Since the transflective LCD operates in both reflective and transmissive modes, depending on the environment or surroundings of the LCD, the transflective LCD has relatively low power consumption, and is also able to be used in places with low ambient light.

[0009] However, the transflective LCD typically has a single cell gap structure and, as a result, a gray-scale difference occurs in the reflective and transmissive areas due to a phase retardation difference therein, thereby causing deterioration of display quality of the LCD. In contrast, when the transflective LCD has a dual cell gap structure, in which a cell gap of the transmissive area is larger than a cell gap of the reflective area, a step difference occurs between the reflective and transmissive areas. As a result, it is difficult to control a liquid crystal director, due to the step difference, and defects in patterning occur in a manufacturing process, thereby causing deterioration of both the display quality and production efficiency of the LCD.

[0010] Accordingly, it is desired to develop a transflective LCD that overcomes at least the problems discussed above.

BRIEF SUMMARY OF THE INVENTION

[0011] An exemplary embodiment of the present invention provides a transflective liquid crystal display ("LCD") having a single cell gap structure and substantially improved display quality.

[0012] Another exemplary embodiment of the present invention provides a method of manufacturing the transflective LCD.

[0013] In an exemplary embodiment of the present invention, a liquid crystal display includes a first substrate including a plurality of pixels, each of which has a transmissive area and a reflective area, a second substrate opposite to the first substrate, and a liquid crystal layer disposed between the first substrate and the second substrate.

[0014] Each pixel includes a first thin film transistor and a second thin film transistor, a transmissive pixel electrode, a reflective pixel electrode and a voltage controller. The first and second thin film transistors output a data signal in response to a first gate signal. The transmissive pixel electrode is disposed in the transmissive area and is electrically connected to the first thin film transistor to charge a first pixel voltage based on the data signal. The reflective pixel electrode is disposed in the reflective area and is electrically connected to the second thin film transistor to charge a second pixel voltage based on the data signal. The voltage controller controls the first and second pixel voltages in response to a second gate signal generated after the first gate signal.

[0015] The transmissive area has a cell gap that is equal to or larger than a cell gap of the reflective area.

[0016] According to an exemplary embodiment, each pixel further comprises a first gate line which receives the first gate signal, a second gate line which receives the second gate signal, and a data line which receives the data signal.

[0017] The voltage controller includes a third thin film transistor, a charge dividing electrode and a storage line. The third thin film transistor includes a source electrode connected to a drain electrode of the second thin film transistor and outputs a voltage control signal in response to the second gate signal. The charge dividing electrode is connected to a drain electrode of the third thin film transistor and is charged with the voltage control signal. The storage line overlaps at least a portion of the charge dividing electrode to form a first capacitor which controls the first pixel voltage and the second pixel voltage.

[0018] The first gate line is connected to a first pixel of the pixels, the second gate line is connected to a second pixel, adjacent to the first pixel, of the pixels, and the voltage controller receives the second gate signal through the second gate line.

[0019] The voltage controller may include: a third thin film transistor including a source electrode connected to the reflective pixel electrode and which outputs a voltage control signal in response to the second gate signal; a charge dividing electrode connected to a drain electrode of the third thin film transistor and which is charged with the voltage control signal; and a storage line which overlaps at least a portion of the charge dividing electrode to form a first capacitor which controls the first pixel voltage and the second pixel voltage.

[0020] The second substrate may include: a color filter layer; and a transparent organic layer disposed in a first area of the color filter layer such that a thickness of the first area is less than a thickness of a second area, different from the first area, of the color filter layer.

[0021] The second substrate may include a color filter layer, and the color filter layer may include at least one penetrating hole formed therethrough at an area corresponding to the reflective area of a corresponding pixel of the pixels.

[0022] A cell gap of the area at which the penetrating hole is formed is greater than a cell gap of another area of the color filter layer.

[0023] The second substrate may include: a common electrode which forms an electric field with the transmissive pixel electrode and the reflective pixel electrode; and at least one dividing pattern disposed on at least one of the transmissive pixel electrode, the reflective pixel area and the common electrode. The at least one dividing pattern divides the liquid crystal layer into domains.

[0024] The reflective pixel electrode may include a concavo-convex portion.

[0025] The domains have different areas.

[0026] The liquid crystal display may further include: a first polarizer disposed on an outer surface of the first substrate; a second polarizer disposed on an outer surface of the second substrate; and at least one phase retardation film disposed at least one of between the first substrate and the first polarizer and between the second substrate and the second polarizer.

[0027] At least one of the first polarizer, the second polarizer and the at least one phase retardation film may include an anti-glare portion disposed thereon.

[0028] In another exemplary embodiment, a method of manufacturing a liquid crystal display is provided, the method including: forming a first substrate comprising pixels, each of which includes a transmissive area and a reflective area; forming a second substrate opposite to the first substrate; and forming a liquid crystal layer between the first substrate and the second substrate.

[0029] The forming the first substrate includes: forming a first thin film transistor, a second thin film transistor, and a third thin film transistor on a first insulating substrate disposed on the first substrate; forming a transmissive pixel electrode, connected to the first thin film transistor, in the transmissive area and; forming a reflective pixel electrode, connected to the second thin film transistor, in the reflective area; and forming a voltage controller overlapping at least a portion of the transmissive pixel electrode.

[0030] A cell gap of the transmissive area is greater than or equal to a cell gap of the reflective area.

[0031] The forming the first thin film transistor, the second thin film transistor and the third thin film transistor may include: forming a first gate line and a second gate line on the first substrate; forming a data line which crosses the first gate line and the second gate line on the first substrate; interposing a gate insulating layer between the data line and each of the first gate line and the second gate line; forming the first thin film transistor and the second thin film transistor connected to the first gate line and the data line, respectively; and forming the third thin film transistor connected to a drain electrode of the second thin film transistor and the second gate line.

[0032] The forming the voltage controller includes: forming a storage line, spaced apart from and insulated from the first gate line and the second gate line, on the first substrate; forming a charge dividing electrode, connected to the third thin film transistor and which overlaps at least a portion the storage line, on the first substrate; and interposing the gate insulating layer between the charge dividing electrode and the storage line.

[0033] The charge dividing electrode overlaps at least a portion of the transmissive pixel electrode, and a protective layer is interposed between the charge dividing electrode and the at least a portion of the transmissive pixel electrode.

[0034] The preparing the second substrate may include: forming a common electrode, configured to form an electric field with the transmissive pixel electrode and the reflective pixel electrode, on a second insulating layer; and forming at least one dividing pattern in the common electrode. The forming the first substrate may further include forming at least one dividing pattern in at least one of the transmissive pixel electrode and the reflective pixel electrode.

[0035] The forming the first thin film transistor, the second thin film transistor and the third thin film transistor may include: forming a first gate line and a second gate line on the first substrate; forming a data line which crosses the first gate line and the second gate line on the first substrate; interposing a gate insulating layer between the data line and both the first gate line and the second gate line; and connecting the first thin film transistor and the second thin film transistor to the first gate line and the data line; and connecting the third thin film transistor to the transmissive pixel electrode and the second gate line.

[0036] The forming the voltage controller includes: comprises forming a storage line, spaced apart from and insulated from the first gate line and the second gate line, on the first substrate; forming a charge dividing electrode, connected to the third thin film transistor and which overlaps at least a portion of the storage line, on the first substrate; and interposing the gate insulating layer between the charge dividing electrode and the storage line.

[0037] The charge dividing electrode overlaps at least a portion of the transmissive pixel electrode, and a protective layer is interposed between the charge dividing electrode and the at least a portion of the transmissive pixel electrode.

[0038] The forming the second substrate includes: forming a common electrode, configured to form an electric field with the transmissive pixel electrode and the reflective pixel electrode, on a second insulating layer; and forming at least one dividing pattern in the common electrode. The forming the first substrate may further include forming at least one dividing pattern in at least one of the transmissive pixel electrode and the reflective pixel electrode.

[0039] In yet another exemplary embodiment, a liquid crystal display includes: a first substrate comprising pixels, each of which includes a transmissive area and a reflective area; a second substrate facing the first substrate; and a liquid crystal layer disposed between the first substrate and the second substrate.

[0040] Each pixel includes: a first thin film transistor which outputs a first data signal in response to a gate signal; a second thin film transistor which outputs a second data signal in response to the gate signal; a transmissive pixel electrode disposed in the transmissive area and connected to the first thin film transistor, and which charges a first pixel voltage in response to the first data signal; and a reflective pixel electrode disposed in the reflective area and connected to the second thin film transistor and which charges a second pixel voltage in response to the second data signal.

[0041] The second substrate includes: a common electrode which forms an electric field with the transmissive pixel electrode and the reflective pixel electrode; and at least one dividing pattern disposed on at least one of the transmissive pixel electrode, the reflective pixel electrode and the common electrode to divide the liquid crystal layer into domains.

[0042] A cell gap of the transmissive area is greater than or equal to a cell gap of the reflective area.

[0043] The liquid crystal display may further include: a first sub-thin film transistor which outputs a first sub-data signal in response to the gate signal; and a voltage controller connected to the first sub-thin film transistor.

[0044] The transmissive pixel electrode includes: a first transmissive pixel electrode connected to a drain electrode of the first thin film transistor to charge a first transmissive pixel voltage; and a second transmissive pixel electrode spaced apart from the first transmissive pixel electrode and connected to the first sub-thin film transistor to charge a second transmissive pixel voltage. The voltage controller controls the first transmissive pixel voltage and the second transmissive pixel voltage in response to a next gate signal of a next pixel generated after the gate signal.

[0045] Thus, according to the exemplary embodiments described herein, a liquid crystal layer corresponding to a transmissive area is driven by a voltage different from a voltage used to drive a liquid crystal layer corresponding to a reflective area, and a phase retardation value of the reflective area is matched with a phase retardation value of the transmissive area. Thus, a gray-scale difference between the transmissive area and the reflective area is substantially reduced and deterioration of electro-optical characteristic of the liquid crystal layer is effectively prevented, thereby greatly improving a display quality of the liquid crystal display. In addition, the liquid crystal display according to an exemplary embodiment has a signal cell gap, and thus does not require the same patterning processes used to manufacture a liquid crystal display having a dual cell gap. As a result, a manufacturing process for the liquid crystal display is simplified, and manufacturing process defects are substantially reduced and/or effectively prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0046] The above and other aspects and features of the present invention will become more readily apparent by describing in further detail exemplary embodiments thereof with reference to the accompanying drawings, in which:

[0047] FIG. **1** is a plan view of an exemplary embodiment of a liquid crystal display ("LCD") according to the present invention;

[0048] FIG. **2** is a partial cross-sectional view taken along line A-A' of FIG. **1**;

[0049] FIG. **3** is an equivalent circuit diagram of a pixel of the liquid crystal display of FIG. **1**;

[0050] FIG. **4** is an equivalent circuit diagram of an n-th pixel when a gate signal is applied to an n-th gate line of the pixel of FIG. **3**;

[0051] FIG. **5** is a graph of reflection and transmission versus applied voltage illustrating an exemplary embodiment of a method of controlling a light transmission amount and a light reflection amount in the liquid crystal display of FIG. **1**;

[0052] FIG. **6** is a partial cross-sectional view of another exemplary embodiment of a liquid crystal display according to the present invention;

[0053] FIGS. **7**A through **7**E are plan views of additional exemplary embodiments of a liquid crystal display according to the present invention;

[0054] FIG. **8** is a plan view of yet another exemplary embodiment of a liquid crystal display according to the present invention;

[0055] FIG. **9** is an equivalent circuit diagram of a pixel of the liquid crystal display of FIG. **8**;

[0056] FIG. **10** is a plan view of still another exemplary embodiment of a liquid crystal display according to the present invention; and

[0057] FIG. **11** is a plan view of yet an additional exemplary embodiment of a liquid crystal display according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0058] The invention now will be described more fully hereinafter with reference to the accompanying drawings, in which various embodiments are shown. This invention may, however, be embodied in many different forms, and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

[0059] It will be understood that when an element is referred to as being "on" another element, it can be directly on the other element or intervening elements may be present therebetween. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0060] It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0061] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," or "includes" and/or "including" when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[0062] Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another element as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in one of the figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on "upper" sides of the other elements. The exemplary term "lower," can therefore, encompasses both an orientation of "lower" and "upper," depending on the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be ori-

ented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

[0063] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0064] Exemplary embodiments are described herein with reference to cross section illustrations that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments described herein should not be construed as limited to the particular shapes of regions as illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or nonlinear features. Moreover, sharp angles that are illustrated may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the present claims.

[0065] Hereinafter, exemplary embodiments of the present invention will be described in further detail with reference to the accompanying drawings.

[0066] FIG. **1** is a plan view of an exemplary embodiment of a liquid crystal display ("LCD") according to the present invention, and FIG. **2** is a partial cross-sectional view taken along line A-A' of FIG. **1**.

[0067] Referring to FIGS. **1** and **2**, a liquid crystal display includes a first substrate **100**, a second substrate **200** disposed opposite to, e.g., facing, the first substrate **100** and a liquid crystal layer **300** disposed between the first substrate **100** and the second substrate **200**.

[0068] The first substrate **100** includes a first insulating substrate **101** including pixels, each of which having a reflective area RA and a transmissive area TA. The first insulating substrate **101** includes N gate lines $GL_1, \ldots, GL_n, GL_{n+1}, \ldots, GL_N$, N sub-gate lines $GL_1', \ldots, GL_n', GL_{n+1}', \ldots, GL_N'$ disposed substantially parallel and correspondingly to the N gate lines, and M data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_M$ and each pixel includes one gate line GL of the N gate lines $GL_1, \ldots, GL_n, GL_{n+1}, \ldots, GL_N$, one sub-gate line GL' of the N sub-gate lines $GL_1', \ldots, GL_n', GL_{n+1}', \ldots, GL_N'$, and one data line DL of the M data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_M$. Hereinafter, for purposes of explanation, one pixel having an n-th gate line GL_n, an n-th sub-gate line GL_n' and an m-th data line DL_m will be described in further detail in conjunction with an (m+1)th data line DL_{m+1}, as shown in FIG. **1**, but it will be noted that alternative exemplary embodiments are not limited. In an exemplary embodiment, each pixel has substantially the same structure and function as the other pixels in the LCD.

[0069] Referring to FIGS. **1** and **2**, on the first substrate **100**, the pixel includes the n-th gate line GL_n the n-th sub-gate line GL_n', a first gate electrode GE**1** the n-th gate line GL_n, and a storage line CST disposed on the first insulating substrate **101**.

[0070] The first insulating substrate **101** is formed of a transparent material, such as glass, for example. The n-th gate line GL_n' is disposed on the first insulating substrate **101** and extends along a first direction (e.g., along a horizontal or row direction, as viewed in FIG. **1**). The n-th sub-gate line GL_n' is disposed substantially parallel to the n-th gate line GL_n and is spaced apart from the n-th gate line GL_n. The first gate electrode GE**1** may branch from the n-th gate line GL_n along a second direction, e.g., a horizontal or column direction (as viewed in FIG. **1**) substantially perpendicular to the first direction. However, in an exemplary embodiment, the first gate electrode GE**1** is disposed on at least a portion of the n-th gate line GL_n. The storage line CST is spaced apart from the n-th gate line GL_n and the n-th sub-gate line GL_n' and is disposed substantially parallel to the n-th gate line GL_n and the n-th sub-gate line GL_n'. In addition, a portion (not shown) of the storage line CST may extend along a different direction to overlap at least a portion of a data line DL of a corresponding pixel. The storage line CST may be disposed in each of the transmissive area TA and the reflective area RA.

[0071] The m-th data line DL_m, the first gate electrode G**1**, a first source electrode SE**1**, a first drain electrode DE**1**, a second source electrode SE**2**, a second drain electrode DE**2**, a third source electrode SE**3**, a third drain electrode DE**3** and a charge dividing electrode CDE are disposed on the first insulating substrate **101** on which the n-th gate line GL_n is disposed.

[0072] The m-th data line DL_m crosses the n-th gate line GL_n and extends along the second direction (substantially perpendicular to the first direction). An insulating layer **110** is interposed between the m-th data line DL_m and the n-th gate line GL_n, as shown in FIG. **2**. The first source electrode SE**1** and the second source electrode SE**2** branch from the m-th data line DL_m to partially overlap the n-th gate line GL_n. The first drain electrode DE**1** and the second drain electrode DE**2** are spaced apart from the first source electrode SE**1** and the second source electrode SE**2**, respectively, to partially overlap the n-th gate line GL_n. The third source electrode SE**3** branches from the second drain electrode DE**2** to partially overlap the n-th sub-gate line GL_n'. The third drain electrode DE**3** is spaced apart from the third source electrode SE**3** to partially overlap the n-th sub-gate line GL_n'. The charge dividing electrode CDE overlaps at least a portion of the storage line CST of the transmissive area TA.

[0073] A transmissive pixel electrode TE and a reflective pixel electrode RE are disposed on the first through third source electrodes SE**1**, SE**2** and SE**3**, respectively, and the first through third drain electrodes DE**1**, DE**2** and DE**3**, respectively, and a protective layer **120** is interposed therebetween. The transmissive pixel electrode TE, which includes a transparent conductive material, is disposed in the transmissive area TA and is connected to the first drain electrode DE**1** through a contact hole formed through the protective layer **120**. The reflective pixel electrode RE, which includes a non-transparent conductive material, is disposed in the reflective area RA and is connected to the second drain electrode DE**2** through a contact hole formed through the protective layer **120**. In an exemplary embodiment, the reflective pixel electrode RE may be disposed only with the non-transparent conductive material layer. Additionally, the reflective pixel electrode RE may be formed by forming the non-transparent conductive material layer on and/or under the transparent conductive material layer that forms the transmissive pixel electrode TE, and thereafter patterning the non-transparent

conductive material layer to form a multilayer structure. The reflective pixel electrode RE may be formed to have a concavo-convex portion on a surface thereof (as shown in FIG. **2**) such that the reflective pixel electrode RE has a high reflectance. The concavo-convex portion may be integrally formed with the reflective pixel electrode RE or, alternatively, may be formed by patterning the protective layer **120** under the reflective pixel electrode RE. When a width of one concavo-convex pattern of the concavo-convex portion is defined as a pitch thereof, the pitch may be about 4 micrometers (μm) to about 5 μm, and a distance between a most recessed portion and a most protruded portion (relative to a plane defined by an outer surface of the protective layer **120** or the reflective pixel electrode RE, as viewed along the vertical direction in FIG. **2**) may be about 0.5 μm to about 2.5 μm.

[0074] As described above, a portion of the n-th gate line GL_n, e.g., the first gate electrode GE**1**, the first source electrode SE**1** and the first drain electrode DE**1** form a first thin film transistor T**1**. Likewise, a portion of the n-th gate line GL_n, e.g., a second gate electrode (not shown), the second source electrode SE**2**, and the second drain electrode DE**2** form a second thin film transistor T**2**, and a portion of the n-th sub-gate line GL_n, e.g., a third gate electrode (not shown), the third source electrode SE**3**, and the third drain electrode DE**3** form a third thin film transistor T**3**. The third thin film transistor T**3**, the charge dividing electrode CDE connected to the third drain electrode DE**3** of the third thin film transistor T**3**, and the storage line CST form a voltage controller.

[0075] Referring still to FIGS. **1** and **2**, the second substrate **200** includes a second insulating substrate **201**. In addition, a transparent organic layer **220**, a light-blocking layer **211**, a color filter layer **210** and a common electrode CE are disposed on the second insulating substrate **201**.

[0076] The transparent organic layer **220** has a predetermined thickness in one area proximate to the second insulating substrate **201**. The light-blocking layer **211** prevents light from leaking and thus includes a non-transparent material that absorbs light. The color filter layer **210** covers the area in which the transparent organic layer **220** is disposed and a remaining area in which the transparent organic layer **220** is not disposed. The transparent organic layer **220** and the color filter layer **210** will be described in greater detail below.

[0077] The common electrode CE is disposed on the color filter layer **210** while an insulating layer **213** is disposed therebetween and forms an electric field with the transmissive pixel electrode TE and the reflective pixel electrode RE to drive the liquid crystal layer **300**.

[0078] A first polarizer **153** and a second polarizer **253** that has a polarizing axis substantially perpendicular to a polarizing axis of the first polarizer **153** are disposed on outer surfaces of the first insulating substrate **101** and the second insulating substrate **201**, respectively. A phase retardation film may be disposed between the first insulating substrate **101** and the first polarizer **153** and/or between the second insulating substrate **201** and the second polarizer **253**. For example, in the exemplary embodiment shown in FIG. **2**, a phase retardation film **151** and a phase retardation film **251** are disposed on surfaces of the first insulating substrate **101** and the second insulating substrate **201**, respectively, but alternative exemplary embodiments are not limited thereto. For example, in other exemplary embodiments, the phase retardation films **151** and/or **251** may be not be included on the first insulating substrate **101** and/or the second insulating substrate **201**, respectively, such as when since a phase retardation value is compensated by applying voltages having different voltage levels to the transmissive area TA and the reflective area RA, for example.

[0079] An anti-glare part (not shown) may be disposed on at least one surface of each of the first polarizer **153**, the second polarizer **253** and the phase retardation films **151** and **251** to prevent rainbow defects, such as when the concavo-convex portion of the reflective pixel electrode RE is disposed on the reflective pixel electrode RE itself, since the rainbow defects may occur due to reflected lights from the concavo-convex portion, which may interfere with each other.

[0080] In the anti-glare part, for example, non-conductive fine particles like silica or conductive fine particles like gold are unevenly dispersed, to substantially reduce interference between the reflected lights. The non-conductive fine particles or the conductive fine particles may have a diameter equal to or less than about 40 μm. The anti-glare part may have a haze value, which is defined as a percentage ratio of scattered light and total transmitted light, of about 5 percent (%) to about 70%.

[0081] In an exemplary embodiment, a distance between the first substrate **100** and the second substrate **200** in the transmissive area TA is substantially equal to a distance between the first substrate **100** and the second substrate **200** in the reflective area RA. Put another way, the transmissive area TA and the reflective area RA may have a single cell gap. More specifically, when the concavo-convex portion is disposed on the reflective pixel electrode RE (as shown in FIG. **2**) after performing a patterning process to form the concavo-convex portion, a cell gap d_R of the reflective are RA, in which the reflective pixel electrode RE is formed, may become slightly larger than a cell gap d_T of the transmissive area TA, in which the transmissive pixel electrode TE is formed. However, since the difference between the cell gaps d_R and d_T is small (relative to a value of the cell gaps d_R and d_T themselves, for example), the transmissive area TA and the reflective area RA effectively have a single cell gap.

[0082] FIG. **3** is an equivalent circuit diagram showing a pixel of the liquid crystal display of FIG. **1**, and FIG. **4** is an equivalent circuit diagram showing an n-th pixel when a gate signal is applied to the n-th gate line GL_n of the pixel FIG. **3**.

[0083] Hereinafter, an exemplary embodiment of a method of driving a liquid crystal display will be described in further detail with reference to FIGS. **1** through **4**.

[0084] A first liquid crystal capacitor T-Clc, a second liquid crystal capacitor R-Clc, a first storage capacitor T-Cst, and a second storage capacitor R-Cst are disposed in the pixel having the first and second thin film transistors T**1** and T**2**, respectively.

[0085] More particularly, the first thin film transistor T**1** includes the first gate electrode GE**1** connected to the n-th gate line GL_n, the first source electrode SE**1** connected to the m-th data line DL_m, and the first drain electrode DE**1** connected to the first liquid crystal capacitor T-Clc. The first liquid crystal capacitor T-Clc is formed by the transmissive pixel electrode TE connected to the first drain electrode DE**1**, the common electrode CE facing the transmissive pixel electrode TE and which receives a common voltage Vcom, and the liquid crystal layer **300** disposed between the transmissive pixel electrode TE and the common electrode CE. The first storage capacitor T-Cst is formed by the transmissive pixel electrode TE, the storage line CST to which the common voltage Vcom is applied, and the insulating layer **110** and the

protective layer **120**, which are interposed between the transmissive pixel electrode TE and the storage line CST.

[0086] The second thin film transistor T**2** includes a second gate electrode connected to the n-th gate line GL_n, the second source electrode SE**2** connected to the m-th data line DL_m, and the second drain electrode DE**2** connected to the second liquid crystal capacitor R-Clc. The second liquid crystal capacitor R-Clc is formed by the reflective pixel electrode RE connected to the second drain electrode DE**2**, the common electrode CE facing the reflective pixel electrode RE and which receives the common voltage Vcom, and the liquid crystal layer **300** disposed between the reflective pixel electrode RE and the common electrode CE. The second storage capacitor R-Cst is formed by the reflective pixel electrode RE, the storage line CST to which the common voltage Vcom is applied, and the insulating layer **110** and the protective layer **120**, which are interposed between the reflective pixel electrode RE and the storage line CST.

[0087] A gate signal is applied to the n-th gate line GL_n, and a data signal is applied to the m-th data line DL_m. When the first and second thin film transistors T**1** and T**2**, respectively, are turned on in response to the gate signal applied through the n-th gate line GL_n, the data signal is applied to the transmissive pixel electrode TE and the reflective pixel electrode RE through the first and second thin film transistors T**1** and T**2**.

[0088] Referring to FIGS. **3** and **4**, when the gate signal is applied to the n-th gate line GL_n, the first and second thin film transistors T**1** and T**2** are turned on. Thus, the data signal applied to the m-th data line DL_m is provided to the transmissive pixel electrode TE and the reflective pixel electrode RE of the first and second liquid crystal capacitors T-Clc and R-Clc through the first and second thin film transistors T**1** and T**2**, respectively. In this case, since the signals applied to the transmissive pixel electrode TE and the reflective pixel electrode RE of the first and second liquid crystal capacitors T-Clc and R-Clc are identical, the first and second liquid crystal capacitors T-Clc and R-Clc are charged with a first pixel voltage and a second pixel voltage, respectively, which have a same voltage level.

[0089] The pixel further includes the n-th sub-gate line GL_n' and the third thin film transistor T**3**, and the third thin film transistor T**3** controls a voltage level of the first and second pixel voltages charged in the transmissive pixel electrode TE and the reflective pixel electrode RE, respectively.

[0090] The third thin film transistor T**3** includes a third gate electrode connected to the n-th sub-gate line GL_n', the third source electrode SE**3** connected to the reflective pixel electrode RE and the third drain electrode DE**3** connected to a down-capacitor Cdown and an up-capacitor Cup.

[0091] As shown in FIG. **2**, the down-capacitor Cdown is formed by the storage line CST, the charge dividing electrode CDE connected to the third drain electrode DE**3** and which partially overlaps the storage line CST, and the insulating layer **110** interposed between the charge dividing electrode CDE and the storage line CST. The up-capacitor Cup is formed by the transmissive pixel electrode TE, the charge dividing electrode CDE that partially overlaps the transmissive pixel electrode TE, and the protective layer **120** interposed between the charge dividing electrode CDE and the transmissive pixel electrode TE.

[0092] The third thin film transistor T**3** is turned on in response to a gate signal applied to the n-th sub-gate line GL_n' to output a voltage control signal after the gate signal is applied to the n-th gate line GL_n. Thus, the reflective pixel electrode RE is electrically connected to the charge dividing electrode CDE by the third thin film transistor T**3**. Consequently, the voltage level of the first pixel voltage charged in the first liquid crystal capacitor T-Clc and the voltage level of the second pixel voltage charged in the second liquid crystal capacitor R-Clc is controlled by the up-capacitor Cup and the down-capacitor Cdown. Specifically, the voltage level of the first pixel voltage increases and the voltage level of the second pixel voltage decreases due to the up-capacitor Cup and the down-capacitor Cdown. An amount of increase and decrease in the first and second pixel voltages, respectively, depends capacitances of the up-capacitor Cup and the down-capacitor Cdown.

[0093] Thus, different voltages may be applied to the transmissive pixel electrode TE and the reflective pixel electrode RE by forming the voltage controller, as described above.

[0094] FIG. **5** is a graph of relative values of reflection transmission versus voltage, in volts (V), illustrating an exemplary embodiment of a method of controlling a light transmission amount and a light reflection amount according to applied voltages for a single cell gap in the liquid crystal display of FIG. **1**. In FIG. **5**, a structure in which the phase retardation films **151** and **251** are interposed between the first insulating substrate **101** and the first polarizer **153** and between the second insulating substrate **201** and the second polarizer **253**, respectively, will be described, but it will be noted that additional exemplary embodiments are not limited thereto. In an exemplary embodiment, each of the phase retardation films **151** and **251** serves as a compensation film having a wavelength λ, of about 550 nanometers (nm) and a retardation value Ro of λ/4 or, alternatively, λ/4+λ/2.

[0095] Referring to FIG. **5**, in an exemplary embodiment, the reflective area RA and the transmissive area TA are driven in normally-black mode, and a light reflection amount of the reflective area RA and the light transmission amount of the transmissive area TA have different values according to voltages applied to the reflective pixel electrode RE and the transmissive pixel electrode TE. As a result, a reflection curve R does not match a transmission curve T. For example, a first applied voltage value (a) when the light reflection amount is at maximum is less than an applied voltage value (b) when the light transmission amount is at maximum. Therefore, when the same voltages are applied to the reflective pixel electrode RE and the transmissive pixel electrode TE, it is difficult to match the gray-scale in the reflective area RA with the gray-scale in the transmissive area TA.

[0096] Thus, in an exemplary embodiment, the first pixel voltage and the second pixel voltage that are applied to the transmissive pixel electrode TE and the reflective pixel electrode RE, respectively, are controlled by the voltage controller, described in greater detail above, such that the reflection curve R is substantially identically matched to the transmission curve T, as shown by the right-shifted reflection curve R in FIG. **5**. Specifically, when the voltage controller lowers the voltage level of the second pixel voltage, the voltage level of a voltage applied to the liquid crystal layer **300** corresponding to the reflective area RA decreases, and the reflection curve R moves to the right, as shown in FIG. **5**. Therefore, the reflection curve R may be substantially identically matched to the transmission curve T, e.g., may be substantially the same as the transmission curve T. As a result, the gray-scale of the reflective area RA is substantially identically matched with the gray-scale of the transmission area RA by applying the

voltages having the same voltage level. It will be noted that other exemplary embodiments are not limited to the method of adjusting the transmission curve T as shown in FIG. **5**. Specifically, for example, the transmission curve T may be adjusted by decreasing the voltage level of the second pixel voltage or, alternatively, by increasing the voltage level of the first pixel voltage (not shown).

[0097] When the phase retardation film is not included, the gray-scale of the transmissive area TA may be matched with the gray-scale of the reflective area RA by controlling the first and second pixel voltages. Specifically, for example, when the phase retardation film is not included, the reflective area RA may be driven in normally-white mode and the transmissive area TA may be driven in normally-black mode. However, the gray-scale of the transmissive area TA is matched to the gray-scale of the reflective area RA by controlling the first and second pixel voltages applied to the transmissive area TA and the reflective area RA, respectively.

[0098] The first pixel voltage and the second pixel voltage may have different values, based on the cell gap difference (described above) between the reflective area RA and the transmissive area TA. For example, when the first pixel voltage is about 1 volt (V) and the cell gap d_R (FIG. **2**) of the reflective area RA is less than the cell gap d_T of the transmissive area TA, the second pixel voltage may be about 0.4 V to about 1 V. When the cell gap d_R of the reflective area RA is the same as the cell gap d_T of the transmissive area TA, the second pixel voltage may be about 0.3 V to about 0.8 V. In addition, when the cell gap d_R of the reflective area RA is larger than the cell gap d_T of the transmissive area TA, the second pixel voltage may be about 0.2 V to about 0.7 V.

[0099] That is, an alignment direction of liquid crystal molecules in the liquid crystal layer **300** is controlled according to voltages applied to the transmissive area TA and the reflective area RA. As a result, phase retardation values of light passing through the liquid crystal layer **300** corresponding to the transmissive area TA and the reflective area RA are effectively controlled to have a same value, thereby matching the gray-scale in the transmissive area TA with the gray-scale in the reflective area RA in an LCD having a signal cell gap. In addition, since the light provided to the reflective area RA successively travels through the second insulating substrate **201**, the color filter layer **210**, the insulating layer **213**, the common electrode CE, the liquid crystal layer **300**, the reflective pixel electrode RE, the liquid crystal layer **300**, the common electrode CE, the insulating layer **213**, the color filter layer **210**, and the second insulating substrate **201**, the light passes through the liquid crystal layer **300** and the color filter layer **210** two times. In contrast, the light provided to the transmissive area TA successively travels through the first insulating substrate **101**, the insulating layer **110**, the protective layer **120**, the transmissive pixel electrode TE, the liquid crystal layer **300**, the common electrode CE, the insulating layer **213**, the color filter layer **210**, and the second insulating substrate **201**, and thus the light passes through the liquid crystal layer **300** and the color filter layer **210** only one time. Therefore, when the light travels through the liquid crystal layer **300** and the color filter layer **210** two times, of which a light absorbance is relatively higher than other materials, parts of the light provided to the reflective area RA is absorbed by the liquid crystal layer **300** and the color filter layer **210**, so that the amount of the light exiting through the reflective area RA may decrease. Accordingly, a light amount difference may occur between the lights traveling through the reflective area RA and the transmissive area TA, and the gray-scales of the reflective and transmissive areas RA and TA are not matched with each other.

[0100] Thus, in an exemplary embodiment, the transparent organic layer **220** is disposed in an area of the color filter layer **210** corresponding to the reflective area RA, such that the light amount of the light traveling through the reflective area RA may increase and the difference in the light amount between the reflective and transmissive areas RA and TA may be minimized.

[0101] The transparent organic layer **220** has the predetermined thickness proximate to the area of the second insulating substrate **201**. The transparent organic layer **220** includes an organic material having a light absorbance less than that a light absorbance of the color filter layer **210**. The transparent organic layer **220** is disposed on the second insulating substrate **201** to correspond to the reflective area RA of the first substrate **100**.

[0102] The color filter layer **210** covers the area where the transparent organic layer **220** is disposed and a remaining area where the transparent organic layer **220** is not disposed. The color filter layer **210** is disposed on the second insulating substrate **201** and includes materials that produce red, blue, green and white colors, for example, to display colors during the light passing therethrough. In an exemplary embodiment, since the transparent organic layer **220** is formed to have the predetermined thickness in the area where the color filter layer **210** is disposed, a thickness of the color filter layer **210** in the area where the transparent organic layer **220** is disposed becomes thinner than a thickness of the color filter layer **210** in the remaining area where the transparent organic layer **220** is not disposed after forming the color filter layer **210**. The area where the color filter layer **210** has a relatively thin thickness has a light absorbance less than the area where the color filter layer **210** has a relatively thick thickness. Thus, the light traveling through the area has a higher light amount than that of the light traveling through the remaining area, to thereby compensate for the difference between the amount of light passing through the transmissive area TA, which has a relatively high light amount, and the amount of light passing through the reflective area RA, which has a relatively low light amount. Accordingly, the amounts of light in the reflective area RA and the transmissive area TA are uniform.

[0103] In an exemplary embodiment, the transparent organic layer **220** is disposed on the color filter layer **210** to improve the light amount of the reflective area RA, however, alternative exemplary embodiments are not limited thereto. For example, instead of forming the transparent organic layer **220** as described above, a penetrating hole **220'**, through which light easily passes, may be formed in the color filter layer **210**, as shown in FIG. **6**, which will now be described in further detail.

[0104] FIG. **6** is a partial cross-sectional view of an exemplary embodiment of a liquid crystal display according to the present invention. More particularly, FIG. **6** shows a color filter layer **210** through which the penetrating hole **220'** is formed. In FIG. **6**, the same reference characters denote the same or like components as described in greater detail above with reference to FIGS. **1** through **5**; accordingly, any repetitive detailed description thereof will hereinafter be simplified or omitted.

[0105] In an exemplary embodiment, the penetrating hole **220'**, which exposes at least a portion of a second insulating substrate **201**, is formed in a color filter layer **210** correspond-

ing to a reflective area RA, to improve a light amount of a light passing through the reflective area RA. In one or more exemplary embodiments, a plurality of the penetrating holes **220'** may be formed. Since the color filter layer **210** is not disposed in the area through which the penetrating hole **220'** is formed, the light directly passes through the penetrating hole **220'** without passing through the color filter layer **210**. Therefore, no light is absorbed by the color filter layer **210** and the light amount of the light increases. The penetrating hole **220'** is not disposed in a remaining area of the color filter layer **210** except for the area where the penetrating hole **220'** is formed of the color filter layer **210**, and the light passes through the remaining area of the color filter layer **210**, to thereby display colors. As a result, the light amount of the light may be improved without decreasing color reproducibility.

[0106] An insulating layer **213** is disposed on the color filter layer **210**, in which the penetrating hole **220'** is formed, and the color filter layer **210** is not disposed in the area in which the penetrating hole **220'** is formed. Thus, an upper surface of the insulating layer **213** has a substantially concave shape in the area in which the penetrating hole **220'** is formed. When the penetrating hole **220'** is formed in the color filter layer **210**, the cell gap d_R of the reflective area RA becomes greater than or equal to the cell gap d_T of the transmissive area TA since a cell gap of the area in which the penetrating hole **220'** is formed becomes larger than a cell gap of the remaining area.

[0107] In an exemplary embodiment, a planarization layer **122** is disposed on the reflective pixel electrode RE. The transmissive pixel electrode TE is disposed on the planarization layer **122**.

[0108] The planarization layer **122** is disposed in order to decrease a spot defect caused by the concavo-convex portion of the transmissive pixel electrode TE. The planarization layer planarizes a surface of the first substrate **100** and, as a result, liquid crystal molecules included in the liquid crystal layer **300** are effectively prevented from becoming misaligned due a height difference in the concavo-convex portion.

[0109] FIGS. **7**A through **7**E are plan views of additional exemplary embodiments of a liquid crystal display according to the present invention. In FIGS. **7**A through **7**E, the same reference characters denote the same or like components as described in greater detail above with reference to the previous drawings; accordingly, any repetitive detailed description thereof will hereinafter be simplified or omitted. Referring now to FIGS. **7**A through **7**E, a transmissive pixel electrode TE, a reflective pixel electrode RE and a common electrode CE will be described in further detail.

[0110] In an LCD according to one or more exemplary embodiments, at least one dividing pattern is formed on a transmissive pixel electrode TE, a reflective pixel electrode RE, and a common electrode CE to divide a liquid crystal layer **300** into a plurality of domains, to thereby substantially improve a viewing angle of the LCD. The domains may have the same area or, alternatively, different areas.

[0111] The dividing pattern is formed on at least one of the transmissive pixel electrode TE, the reflective pixel electrode RE and the common electrode CE, and the dividing pattern may have a slit shape (hereinafter, referred to as a slit portion) when viewed from above a plan view of the LCD, an embossed shape (hereinafter, referred to as an embossed portion) and/or a hole shape (hereinafter, referred to as a hole portion) to control a director of a liquid crystal, but exemplary embodiments are not limited thereto. In another exemplary embodiment, the embossed portion E**1** forms a pyramidal pattern or a hemispheric pattern.

[0112] Referring now to FIG. **7**A, in an exemplary embodiment, slit portions S**1** and S**2** are formed in the transmissive pixel electrode TE and the common electrode CE of the second substrate **200** corresponding to the transmissive pixel electrode TE as the dividing pattern. An embossed portion E**1** is formed in the reflective pixel electrode RE. In an exemplary embodiment, the embossed portion E**1** forms a close-packed hexagonal pattern, as shown in FIG. **7**A.

[0113] In alternative exemplary embodiments, the embossed portions E**1** and the slit portions S**1** and S**2** may be arranged differently than as shown in FIG. **7**A, e.g., the embossed portions E**1** and the slit portions S**1** and S**2** may be replaced with each other (e.g., swapped) and/or disposed in a same area. In addition, the slit portions S**1** and S**2** or the embossed portion E**1** may be formed by patterning at least one of the transmissive pixel electrode TE, the reflective pixel electrode RE, and the common electrode CE.

[0114] As shown in FIG. **7**B, in another exemplary embodiment, the slit portions S**1** and S**2** or the embossed portions E**1** are formed in the transmissive pixel electrode TE, the common electrode CE corresponding to the transmissive pixel electrode TE and the reflective pixel electrode RE.

[0115] As shown in FIG. **7**C, in yet another exemplary embodiment, the slit portions S**1** and S**2** or the embossed portions E**1** are formed in the transmissive pixel electrode TE, the reflective pixel electrode RE, and the common electrode CE that corresponds to the transmissive pixel electrode TE and the reflective pixel electrode RE.

[0116] As shown in FIG. **7**D, in another exemplary embodiment, the slit portions S**1** and S**2** or the embossed portions E**1** are formed in the transmissive pixel electrode TE and the common electrode CE corresponding to the transmissive pixel electrode TE and the reflective electrode RE.

[0117] As shown in FIG. **7**E, in another exemplary embodiment, the slit portions S**1** and S**2**, or the embossed portion E**1**, is formed through the transmissive pixel electrode TE, a hole portion H is formed in the common electrode CE corresponding to the transmissive pixel electrode TE, and the slit portions S**1** and S**2** or the embossed portions E**1** are formed through the common electrode CE corresponding to the reflective pixel electrode RE.

[0118] Referring now to FIGS. **7**A through **7**E, the dividing pattern formed in the transmissive pixel electrode TE and the reflective pixel electrode RE may be in the form of the slit portions S**1** and S**2**. Moreover, the dividing pattern formed in the common electrode CE may be prepared in the form of the slit portions S**1** and S**2**, as shown in FIGS. **7**A through **7**D, or in the form of the hole portion H, as shown in FIG. **7**E. In still another exemplary embodiment, the dividing pattern, which is formed through the transmissive pixel electrode TE and the reflective pixel electrode RE, may be the form of the embossed portions E**1** instead of the slit portions S**1** and S**2** or the hole portions H.

[0119] When the dividing pattern is in the form of the slit portions S**1** and S**2** in the transmissive pixel electrode TE, the reflective pixel electrode RE, and the common electrode CE, the slit portions S**2** formed in the common electrode CE are arranged substantially parallel to the slit portions S**1** of the transmissive pixel electrode or the reflective pixel electrode RE and positioned at an area corresponding to between the slit portions S**1** of the transmissive pixel electrode TE or the

reflective pixel electrode RE. The slit portions **S1** of the transmissive pixel electrode TE and the common electrode CE are inclined with respect to the n-th gate line GL_n or the m-th data line DL_m and are symmetrical with respect to each other with reference to an imaginary line parallel to the n-th gate line GL_n, and the slit portions **S2** of the transmissive pixel electrode TE and the common electrode CE is formed to be inclined to the n-th gate line GL_n or the m-th data line DL_m and is formed to be symmetrical with respect to each other with reference to an imaginary line parallel to the n-th gate line GL_n. As shown in FIG. **7**E, when the slit portion **S1** is disposed in the transmissive pixel electrode TE and the hole portion H is disposed in the common electrode CE, the slit portion **S1** of the transmissive pixel electrode TE may be disposed in substantially parallel to the n-th gate line GL_n and the m-th data line DL_m to form a plurality of domains, and the hole portion H may be formed at a position corresponding to a center portion of each domain. In another exemplary embodiment, the hole portion H formed at the center portion of each domain may be replaced with the embossing portions E**1**.

[0120] A concavo-convex portion is disposed on the reflective pixel electrode RE, and a pretilt angle of the liquid crystal molecules of the liquid crystal layer is controlled by the concavo-convex portion, so that the reflective pixel electrode RE of an LCD according to an exemplary embodiment may not need the slit portions **S1** and **S2**.

[0121] Liquid crystal molecules not shown) of the liquid crystal layer **300** (FIG. **2**) adjacent to the slit portions **S1** and **S2** may be tilted at a predetermined angle by the slit portions **S1** and **S2** of the transmissive pixel electrode TE and the common electrode CE, thereby substantially improving the viewing angle of the LCD according to an exemplary embodiment.

[0122] FIG. **8** is a plan view of yet another exemplary embodiment of an LCD according to the present invention, and FIG. **9** is an equivalent circuit diagram of a pixel of the LCD of FIG. **8**. In FIGS. **8** and **9**, a voltage controller is configured to have a circuit configuration different from in the additional exemplary embodiments of the voltage controller of described in greater detail above. In addition, the same reference characters have been used to refer to the same or like components throughout the drawings, and thus any repetitive detailed description will hereinafter be simplified or omitted.

[0123] Referring to FIGS. **2**, **8** and **9**, a voltage controller according to an exemplary embodiment includes a third thin film transistor T**3** having a source electrode SE**3** connected to a transmissive pixel electrode TE.

[0124] As shown in FIG. **8**, n+p gate lines $GL_1, \ldots, GL_n, GL_{n+1}, \ldots, GL_{(n+p)-1}, GL_{n+p}$ and m+q data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_{(m+q)-1}, DL_{m+q}$ are disposed on a first insulating substrate **101** (FIG. **2**), and each pixel includes one gate line GL of the n+p gate lines $GL_1, \ldots, GL_n, GL_{n+1}, \ldots, GL_{(n+p)-1}, GL_{n+p}$ and one data line DL of the m+q data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_{(m+q)-1}, DL_{m+q}$. In FIG. **8**, for purposes of description, a pixel including an n-th gate line GL_n, an (n+1)th gate line GL_{n+1}, and m-th data line DL_m is shown and will be described in further detail, but exemplary embodiments are not limited thereto. In an exemplary embodiment, each pixel has substantially the same structure and function.

[0125] In the first substrate **100**, the pixel including the n-th gate line GL_n, a gate electrode of the n-th gate line GL_n (not specifically labeled in FIG. **8**), and a storage line CST is disposed on the first insulating substrate **101** (FIG. **2**).

[0126] The n-th gate line GL_n, extends along a first direction on the first insulating substrate **101**. The (n+1)th gate line GL_{n+1} is spaced apart from the n-th gate line GL_n disposed substantially parallel to the n-th gate line GL_n to apply a gate signal to a next pixel, e.g., an (n+1)th pixel. The gate electrode may branch from the n-th gate line GL_n, or (n+1)th gate line GL_{n+1}, or may be disposed on at least a portion of the n-th gate line GL_n or (n+1)th gate line GL_{n+1}. The storage line CST is disposed between the n-th gate line GL_n, and the (n+1)th gate line GL_{n+1} substantially parallel to the n-th gate line GL_n, and the (n+1)th gate line GL_{n+1}. The storage line CST is spaced apart from the n-th gate line GL_n, and the (n+1)th gate line GL_{n+1}. The storage line CST may extend along a different direction from the first direction, e.g., in a second direction substantially perpendicular to the first direction. The storage line CST is disposed in a portion of an area of the transmissive area TA and the reflective area RA.

[0127] The m-th data line DL_m, a first source electrode SE**1**, a first drain electrode DE**1**, a second source electrode SE**2**, a second drain electrode DE**2**, a third source electrode SE**3**, a third drain electrode DE**3**, and a charge dividing electrode CDE are arranged on the first insulating substrate **101** on which the n-th gate line GL_n is formed. Since the first and second source electrodes SE**1** and SE**2** are connected to the m-th data line DL_m.

[0128] The m-th data line DL_m crosses the n-th gate line GL_n and the (n+1)th gate line GL_{n+1} and includes an insulating layer **110** disposed therebetween, and extends along the second direction. The first source electrode SE**1** and the second source electrode SE**2** branch from the m-th data line DL_m to partially overlap the n-th gate line GL_n. The first drain electrode DE**1** and the second drain electrode DE**2** are spaced apart from the first source electrode SE**1** and the second source electrode SE**2**, respectively, to partially overlap the n-th gate line GL_n. The third source electrode SE**3** partially overlaps the (n+1)th gate line GL_{n+1} and is connected to a reflective pixel electrode RE that will be described later. The third drain electrode DE**3** is spaced apart from the third source electrode SE**3** to partially overlap the (n+1)th gate line GL_{n+1}. The charge dividing electrode CDE overlaps the storage line CST of the transmissive area TA.

[0129] A transmissive pixel electrode TE and a reflective pixel electrode RE are disposed on the first through third source electrodes SE**1**, SE**2** and SE**3**, respectively, and the first through third drain electrodes DE**1**, DE**2** and DE**3**, respectively, while the protective layer **120** is disposed therebetween. The transmissive pixel electrode TE is disposed in the transmissive area TA and connected to the first drain electrode DE**1** through a contact hole formed in the protective layer **120**. The reflective pixel electrode RE is disposed in the reflective area RA and is connected to the second drain electrode DE**2** and the third source electrode SE**3** through a contact hole formed in the protective layer **120**. A first thin film transistor T**1** is formed by a portion of the n-th gate line GL_n, the first source electrode SE**1** and the first drain electrode DE**1**, a second thin film transistor T**2** is formed by a portion of the n-th gate line GLn, the second source electrode SE**2** and the second drain electrode DE**2**, while a third thin film transistor T**3** is formed by a portion of the (n+1)th gate line GLn+1, the third source electrode SE**3** and the third drain electrode DE**3**. The third thin film transistor T**3**, the charge

dividing electrode CDE connected to the drain electrode DE3 of the third thin film transistor T3, and the storage line CST form the voltage controller.

[0130] Referring now to FIG. **9**, when a gate signal is applied to the n-th gate line GL_n, the first thin film transistor T1 and the second thin film transistor T2 are turned on. Thus, a data signal applied to the m-th data line DL_m is provided to the transmissive pixel electrode TE of a first liquid crystal capacitor T-Clc and the reflective pixel electrode RE of a second liquid crystal capacitor R-Clc through the first thin film transistor T1 and the second thin film transistor T2. Since the signal applied to the transmissive pixel electrode TE of the first liquid crystal capacitor T-Clc is the same as the signal applied to the reflective pixel electrode RE of the second liquid crystal capacitor R-Clc, the first and second liquid crystal capacitors T-Clc and R-Clc are charged with a first pixel voltage and a second pixel voltage having the same voltage level.

[0131] The third thin film transistor T3 controls voltage levels of the first and second pixel voltages charged in the transmissive pixel electrode TE and the reflective pixel electrode RE, respectively. The third thin film transistor T3 includes a third gate electrode connected to the n-th gate line GL_{n+1}, the third source electrode SE3 connected to the reflective pixel electrode RE, and the third drain electrode DE3 connected to a down-capacitor Cdown and an up-capacitor Cup.

[0132] The down-capacitor Cdown is formed by the storage line CST, the charge dividing electrode CDE partially overlapped with the storage line CST and connected to the third drain electrode DE3, and the insulating layer **110** interposed between the charge dividing electrode CDE and the storage line CST. The up-capacitor Cup is formed by the transmissive pixel electrode TE, the charge dividing electrode CDE partially overlapped with the transmissive pixel electrode TE, and the protective layer **120** interposed between the charge dividing electrode CDE and the transmissive pixel electrode TE.

[0133] The third thin film transistor T3 is turned on in response to a gate signal applied to the (n+1)th gate line GL_{n+1} to output a voltage control signal after the gate signal is applied to the n-th gate line GL_n. Then, the reflective pixel electrode RE is electrically connected to the charge dividing electrode CDE by the third thin film transistor T3. Therefore, the voltage levels of the first pixel voltage charged in the first liquid crystal capacitor T-Clc and the second pixel voltage charged in the second liquid crystal capacitor R-Clc are controlled by the up-capacitor Cup and the down-capacitor Cdown. More particularly, the voltage level of the first pixel voltage increases and the voltage level of the second pixel voltage decreases by the up-capacitor Cup and the down-capacitor Cdown. An increase and decrease in the first and second pixel voltages, respectively, depends on capacitances of the up-capacitor Cup and the down-capacitor Cdown.

[0134] FIG. **10** is a plan view of yet another exemplary embodiment of an LCD according to the present invention. In an exemplary embodiment shown in FIG. **10**, different data signals are applied to each of the transmissive pixel electrode TE and the reflective pixel electrode PE such that different voltages are applied thereto. In addition, in an exemplary embodiment, a liquid crystal layer **300** (FIG. **2**) interposed between a first substrate **100** and a second substrate **200** is divided into a plurality of areas.

[0135] Hereinafter, only different elements from those of the additional exemplary embodiments described in greater detail above will be described with reference to FIGS. **1** and **10**. In addition, the same reference characters in FIG. **10** denote the same or like elements in the previously-described exemplary embodiments, and thus any repetitive detailed description thereof will be omitted.

[0136] The first substrate **100** includes a first insulating substrate **101** on which pixels, each having a reflective area RA and a transmissive area TA, are disposed. In an exemplary embodiment, n+p gate lines $GL_1, \ldots, GL_n, GL_{n+1}, \ldots, GL_{(n+p)-1}, GL_{n+p}$, m+q data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_{(m+q)-1}, DL_{m+q}$, and m'+q sub-data lines $DL_1', \ldots, DL_m', DL_{m+1}', \ldots, DL_{(m'+q)-1}, DL_{m'+q}$, which are disposed substantially parallel to and spaced apart from the m+q data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_{(m+q)-1}, DL_{m+q}$ are disposed on the first insulating substrate **101**. Each pixel includes one gate line GL of the n+p gate lines $GL_1, \ldots, GL_n, GL_{n+1}, \ldots, GL_{(n+p)-1}, GL_{n+p}$, one data line DL of the m+q data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_{(m+q)-1}, DL_{m+q}$ and one sub-data line DL' of the sub-data lines $DL_1', \ldots, DL_m', DL_{m+1}', \ldots, DL_{(m'+q)-1}, DL_{m'+q}$. In FIGS. **10** and **11**, for purposes of description, a pixel including the n-th gate line GLn, the m-th data line DLm, and the m-th sub-data line DL_m' is shown and will be described in greater detail herein, but alternative exemplary embodiments are not limited thereto. In an exemplary embodiment, each pixel has substantially the same structure and function.

[0137] The n-th gate line GL_n extends in a first direction on the first insulating substrate **101**. The m-th data line DL_m, the m-th sub-data line DL_m', a first source electrode SE1, a first drain electrode DE1, a second source electrode SE2, a second drain electrode DE2, and a storage line CST are disposed on the first insulating substrate **101** on which the n-th gate line GL_n is disposed.

[0138] The m-th data line DL_m and the m-th sub-data line DL_m' extend in a second direction, substantially perpendicular to the first direction, to cross the n-th gate line GL_n and having an insulating layer **110** disposed therebetween.

[0139] The first source electrode SE1 and the second source electrode SE2 branch from the m-th data line DL_m and the m-th sub-data line DL_m', respectively, to partially overlap the n-th gate line GL_n. The first drain electrode DE1 and the second drain electrode DE2 are spaced apart from the first source electrode SE1 and the second source electrode SE2, respectively, to partially overlap the n-th gate line GL_n.

[0140] A transmissive pixel electrode TE and a reflective pixel electrode RE are disposed on the first source electrode SE1 and the second source electrode SE2 and the first drain electrode DE1 and the second drain electrode DE2, while a protective layer **120** is disposed therebetween. The transmissive pixel electrode TE is disposed in the transmissive area TA, has a transparent conductive material, and is connected to the first drain electrode DE1 through a contact hole formed through the protective layer **120**. The reflective pixel electrode RE is disposed in the reflective area RA, has a non-transparent conductive material, and is connected to the second drain electrode DE2 through a contact hole formed through the protective layer **120**.

[0141] The reflective pixel electrode RE may have a concavo-convex portion disposed on a surface thereof to increase a reflectance of the same. The concavo-convex portion may be integrally formed with the reflective pixel electrode RE

and/or may be formed by patterning the protective layer **120** disposed under the reflective pixel electrode RE.

[0142] A second substrate **200** includes a second insulating substrate **201**, and a transparent organic layer **220**, a light-blocking layer **211**, a color filter layer **210** and a common electrode CE are disposed on the second insulating substrate **201**.

[0143] At least one dividing pattern is formed in one of the transmissive pixel electrode TE, the reflective pixel electrode RE and the common electrode CE to divide a liquid crystal layer **300** into domains. Each domain may have a same area or a different area. The dividing pattern is formed to have a slit shape (hereinafter, referred to as slit portions S**1** and S**2**) to control an alignment direction of the liquid crystal layer **300**. In an exemplary embodiment, the slit portions S**1** and S**2** are formed in the transmissive pixel electrode TE and the common electrode CE; however it will be noted that alternative exemplary embodiments are not limited thereto or thereby. For example, the slit portions S**1** and S**2** may be disposed in the reflective pixel electrode RE. In addition, the dividing pattern may have an embossed shape and/or a hole shape.

[0144] Thus, in an exemplary embodiment, a portion of the n-th gate line GL_n, the first source electrode SE**1**, and the first drain electrode DE**1** form a first thin film transistor T**1**, and a portion of the n-th gate line GL_n, a second source electrode SE**2**, and a second drain electrode DE**2** form a second thin film transistor T**2**.

[0145] Referring to FIG. **10**, when a gate signal is applied to the n-th gate line GL_n, the first thin film transistor T**1** and the second thin film transistor T**2** are turned on in response to the gate signal to output a first data signal and a second data signal, respectively. Thus, the first data signal applied to the m-th data line DL_m is applied to the transmissive pixel electrode TE through the first thin film transistor T**1** to charge the transmissive pixel electrode TE, and the second data signal applied to the m-th sub-data line DL_m' is applied to the reflective pixel electrode RE through the second thin film transistor T**2** to charge the reflective pixel electrode RE. In this case, since the m-th data line DL_m and the m-th sub-data line DL_m' may apply different data signals from each other, a first pixel voltage and a second pixel voltage having different voltage levels may be applied to the transmissive pixel electrode TE and the reflective pixel electrode RE, respectively.

[0146] As described above, since different voltages are applied to the transmissive pixel electrode TE and the reflective pixel electrode RE, alignment angles of liquid crystal molecules included in the liquid crystal layer **300** corresponding to the transmissive area TA and the reflective area RA are controlled differently from one another. As a result, a phase retardation value of light passing through the liquid crystal layer **300** of the transmissive pixel electrode TE may be substantially the same as a phase retardation value of light passing through the liquid crystal layer **300** of the reflective pixel electrode RE. Accordingly, a gray-scale of the transmissive area TA is matched with a gray-scale of the reflective area RA in an LCD having a signal cell gap. In addition, the dividing pattern is disposed in the transmissive pixel electrode TE and the reflective pixel electrode RE to form the domains, thereby substantially improving a side visibility and greatly widening a viewing angle of the LCD.

[0147] FIG. **11** is a plan view of still another exemplary embodiment of an LCD according to the present invention. In an exemplary embodiment, different data signals are applied to a transmissive pixel electrode TE and a reflective pixel electrode RE to provide different voltages to the transmissive pixel electrode TE and the reflective pixel electrode RE, thereby providing a transflective LCD with a single cell gap. In addition, in an exemplary embodiment, the transmissive pixel electrode TE may be divided into two areas, to which different pixel voltages are applied, and a liquid crystal layer **300** interposed between a first substrate **100** and a second substrate **200** is divided into a plurality of domains.

[0148] Hereinafter, only different elements from those of previously-described additional exemplary embodiments will be described in further detail with reference to FIGS. **1** and **11**. In addition, the same reference characters in FIG. **10** denote the same or like elements in the previous drawings, and thus any repetitive detailed description thereof will be omitted.

[0149] A first substrate **100** includes a first insulating substrate **101** on pixels, each having a reflective area RA and a transmissive area TA, are formed. n+p gate lines $GL_1, \ldots, GL_n, GL_{n+1}, \ldots, GL_{(n+p)-1}, GL_{n+p}$, m+q data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_{(m+q)-1}, DL_{m+q}$ and m'+q sub-data lines $DL_1', \ldots, DL_m', DL_{m+1}', \ldots, DL_{(m'+q)-1}, DL_{m+q}$ that are substantially parallel to and spaced apart from the M data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_{(m+q)-1}, DL_{m+q}$ are disposed on the first insulating substrate **101**. Each pixel includes one gate line GL of the n+p gate lines $GL_1, \ldots, GL_n, GL_{n+1}, \ldots, GL_{(n+p)-1}, GL_{n+p}$, one data line DL of the m+q data lines $DL_1, \ldots, DL_m, DL_{m+1}, \ldots, DL_{(m+q)-1}, DL_{m+q}$, and one sub-data line DL' of the m'+q sub-data lines $DL_1', \ldots, DL_m', DL_{m+1}', \ldots, DL_{(m'+q)-1}, DL_{m'+q}$. In FIG. **11**, for purposes of description, a pixel including the n-th gate line GL_n, the m-th data line DL_m, and the m-th sub-data line DL_m' has been illustrated with the (n+1)th gate line GL_{n+1} of a next pixel adjacent to the pixel, but alternative exemplary embodiments are not limited thereto. In an exemplary embodiment, each pixel has substantially the same structure and function.

[0150] The n-th gate line GL_n, extends along a first direction on the first insulating substrate **101**. The m-th data line DL_m, the m-th sub-data line DL_m', a first source electrode SE**1**, a first drain electrode DE**1**, a first sub-source electrode SE**1'**, a first sub-drain electrode DE**1'**, a second sub-source electrode SE**1"**, a second sub-drain electrode DE**1"**, a second source electrode SE**2**, a second drain electrode DE**2**, and a charge dividing electrode CDE are disposed on the first insulating substrate **101** on which the n-th gate line GL_n is disposed.

[0151] A storage line CST is arranged substantially parallel to the n-th gate line GL_n and the (n+1)th gate line GL_{n+1}, positioned between the n-th gate line GL_n and the (n+1)th gate line GL_{n+1}, and spaced apart from the n-th gate line GL_n and the (n+1)th gate line GL_{n+1}. A portion of the storage line CST may branch therefrom along a second direction substantially perpendicular to the first direction. The storage line CST may be disposed in both areas of the transmissive area TA and the reflective area RA.

[0152] The first source electrode SE**1** and the first sub-source electrode SE**1'** branch from the m-th data line DL_m to partially overlap the n-th gate line GL_n. The second source electrode SE**2** branches from the m-th sub-data line DL_m' to partially overlap the n-th gate line GL_n.

[0153] The first drain electrode DE**1** and the first sub-drain electrode DE**1'** are spaced apart from the first source electrode SE**1** and the first sub-source electrode SE**1'** to partially overlap the n-th gate line GL_n. The second drain electrode DE**2** is

spaced apart from the second source electrode SE2 to partially overlap the n-th gate line GL_n.

[0154] A transmissive pixel electrode TE and a reflective pixel electrode RE are disposed on the first source electrode SE1, the first sub-source electrode SE1' and the second source electrode SE2 and the first drain electrode DE1, the first sub-drain electrode DE1' and the second drain electrode DE2, and a protective layer **120** is disposed therebetween. The transmissive pixel electrode TE is disposed in the transmissive area TA, includes a transparent conductive material, and the transmissive pixel electrode TE further includes a first transmissive pixel electrode TE1 and a second transmissive pixel electrode TE2 spaced apart from and insulated from the first transmissive pixel electrode TE1. The first transmissive pixel electrode TE1 is connected to the first drain electrode DE1 through a contact hole formed through the protective layer **120**. The second transmissive pixel electrode TE2 is connected to the first sub-drain electrode DE1' through a contact hole formed in the protective layer **120**.

[0155] The second sub-source electrode SE1" is connected to the second transmissive pixel electrode TE2 through a contact hole and partially overlaps with the (n+1)th gate line GL_{n+1}. The second sub-drain electrode DE1" is spaced apart from the second sub-source electrode SE1" to partially overlap the (n+1)th gate line GL_{n+1}.

[0156] The charge dividing electrode CDE is connected to the second sub-drain electrode DE1" and partially overlaps the first transmissive pixel electrode TE1 and the storage line CST. The charge dividing electrode CDE forms a down-capacitor Cdown with the storage line CST with an insulating layer **110** disposed therebetween, and forms an up-capacitor Cup with the first transmissive pixel electrode TE1 with the insulating layer **110** disposed therebetween.

[0157] A second substrate **200** includes a second insulating substrate **201**, and a transparent organic layer **220**, a light-blocking layer **211**, a color filter layer **210** and a common electrode CE are disposed on the second insulating substrate **201**.

[0158] At least one dividing pattern is formed in at least one of the first transmissive pixel electrode TE1, the second transmissive pixel electrode TE2, the reflective pixel electrode RE and the common electrode CE to divide the liquid crystal layer **300** into domains. The domains may be divided into the same area or different areas. The dividing pattern is formed in at least one of the first transmissive pixel electrode TE1, the second transmissive pixel electrode TE2, the reflective pixel electrode RE and the common electrode CE, and the dividing pattern may have a slit shape (hereinafter referred to as a slit portion), an embossed shape (hereinafter referred to as an embossed portion), or a hole shape (hereinafter referred to as a hole portion). In an exemplary embodiment, a structure in which the slit portion is disposed in the transmissive pixel electrode TE, has been shown and will be described in further detail; however it will be noted that alternative exemplary embodiments are not be limited thereto or thereby. For example, the slit portion may be formed in the reflective pixel electrode RE or the common electrode, and the dividing pattern may be replaced by an embossed portion or a hole portion.

[0159] In an exemplary embodiment, a portion of the n-th gate line GL_n, the first source electrode SE1, and the first drain electrode DE1 form a first thin film transistor T1. A portion of the n-th gate line GL_n, the first sub-source electrode SE1', and the first sub-drain electrode DE1' form a first sub-thin film transistor T1'. A portion of the (n+1)th gate line GL_{n+1}, the second sub-source electrode SE1", and the second sub-drain electrode DE1" form a second sub-thin film transistor T1". A portion of the n-th gate line GL_n, the second source electrode SE2, and the second drain electrode DE2 form a second thin film transistor T2.

[0160] Referring to FIG. **11**, when a gate signal is applied to the n-th gate line GL_n, the first thin film transistor T1 and the second thin film transistor T2 are turned on in response to the gate signal to output a first data signal and a second data signal, respectively. Then, the first data signal applied to the m-th data line DL_m is provided to the transmissive pixel electrode TE through the first thin film transistor T1 and charged in the transmissive pixel electrode TE, and the second data signal applied to the m-th sub-data line DL_m' is provided to the reflective pixel electrode RE through the second thin film transistor T2 and charged in the reflective pixel electrode RE. Since the m-th data line DL_m and the m-th sub-data line DL_m' may transmit different data signals, a first pixel voltage and a second pixel voltage having different voltage levels may be applied to the transmissive pixel electrode TE and the reflective pixel electrode RE, respectively.

[0161] When the gate signal is applied, the first thin film transistor T1 and the first sub-thin film transistor T1' are turned on in response to the gate signal to output the first data signal and a first sub-data signal, respectively. Accordingly, the first data signal and the first auxiliary data signal are applied to the first transmissive pixel electrode TE1 and the second transmissive pixel electrode TE2, respectively, and are thereafter charged into the first transmissive pixel electrode TE1 and the second transmissive pixel electrode TE2, respectively. The signals applied to the first transmissive pixel electrode TE1 and the second transmissive pixel electrode TE2 are substantially identical, and thus a first liquid crystal capacitor and a second liquid crystal capacitor corresponding to the first transmissive pixel electrode TE1 and the second transmissive pixel electrode TE2, respectively, are charged with a first transmissive pixel voltage and a second transmissive pixel voltage having the same voltage level.

[0162] The second sub-thin film transistor T1" is turned on in response to a gate signal applied to the (n+1)th gate line GL_{n+1} to output a voltage control signal after the gate signal is applied to the n-th gate line GL_n. Thus, the second transmissive pixel electrode TE2 is electrically connected to the charge dividing electrode CDE by the second sub-thin film transistor T1". Then, the voltage levels of the first transmissive pixel voltage charged in the first liquid crystal capacitor and the second transmissive pixel voltage charged in the second liquid crystal capacitor may be controlled by the up-capacitor Cup and the down-capacitor Cdown. More particularly, the voltage level of the first transmissive pixel voltage increases by the up-capacitor Cup, and the voltage level of the second transmissive pixel voltage decreases by the down-capacitor Cdown.

[0163] An increase and a decrease in the first and second transmissive pixel voltages depend on capacitances of the up-capacitor Cup and the down-capacitor Cdown. Therefore, different voltages may be applied to the first transmissive pixel electrode TE1 and the second transmissive pixel electrode TE2 by forming a voltage controller.

[0164] As described herein, a signal cell gap LCD is achieved by dividing a transmissive pixel electrode TE into first and second transmissive pixel electrodes TE1 and TE2, respectively, and applying different pixel voltages to the first

and second transmissive pixel electrodes TE1 and TE2. In addition, liquid crystal molecules may be aligned at different angles from each other, to thereby substantially improve side visibility and provide a wide viewing angle.

[0165] Thus, since the different pixel voltages are applied to the transmissive pixel electrode TE and the reflective pixel electrode RE, the liquid crystal molecules included in the liquid crystal layer **300** corresponding to the transmissive area TA and the reflective area RA are controlled to have different alignment angles from each other. As a result, a phase retardation value of light traveling through the liquid crystal layer **300** corresponding to the transmissive pixel electrode TE has substantially the same phase retardation value of light traveling through the liquid crystal layer **300** corresponding to the reflective pixel electrode RE, and a gray-scale of the transmissive area TA is thereby matched with a gray-scale of the reflective area RA in an LCD with a signal cell gap. In one or more exemplary embodiments, a next gate line for the next pixel may be used instead of forming the sub-gate lines for corresponding pixels.

[0166] The present invention should not be construed as being limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the present invention to those skilled in the art.

[0167] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit or scope of the present invention as defined by the following claims.

What is claimed is:

1. A liquid crystal display comprising:

a first substrate including pixels, each of which includes a transmissive area and a reflective area;

a second substrate disposed opposite the first substrate; and

a liquid crystal layer disposed between the first substrate and the second substrate,

wherein each of the pixels comprises:

a first thin film transistor and a second thin film transistor which both output a data signal in response to a first gate signal;

a transmissive pixel electrode disposed in the transmissive area and electrically connected to the first thin film transistor to charge a first pixel voltage based on the data signal;

a reflective pixel electrode disposed in the reflective area and electrically connected to the second thin film transistor to charge a second pixel voltage based on the data signal; and

a voltage controller which controls the first pixel voltage and the second pixel voltage in response to a second gate signal,

wherein the second gate signal is generated after the first gate signal.

2. The liquid crystal display of claim **1**, wherein a cell gap of the transmissive area is greater than or equal to a cell gap of the reflective area.

3. The liquid crystal display of claim **1**, further comprising:

a first gate line which receives the first gate signal;

a second gate line which receives the second gate signal; and

a data line which receives the data signal.

4. The liquid crystal display of claim **1**, wherein the voltage controller comprises:

a third thin film transistor including a source electrode connected to a drain electrode of the second thin film transistor and which outputs a voltage control signal in response to the second gate signal;

a charge dividing electrode connected to a drain electrode of the third thin film transistor and which is charged with the voltage control signal; and

a storage line which overlaps at least a portion of the charge dividing electrode to form a first capacitor which controls the first pixel voltage and the second pixel voltage.

5. The liquid crystal display of claim **3**, wherein

the first gate line is connected to a first pixel of the pixels, the second gate line is connected to a second pixel, adjacent to the first pixel, of the pixels, and

the voltage controller receives the second gate signal through the second gate line.

6. The liquid crystal display of claim **1**, wherein the voltage controller comprises:

a third thin film transistor including a source electrode connected to the reflective pixel electrode and which outputs a voltage control signal in response to the second gate signal;

a charge dividing electrode connected to a drain electrode of the third thin film transistor and which is charged with the voltage control signal; and

a storage line which overlaps at least a portion of the charge dividing electrode to form a first capacitor which controls the first pixel voltage and the second pixel voltage.

7. The liquid crystal display of claim **1**, wherein the second substrate comprises:

a color filter layer; and

a transparent organic layer disposed in a first area of the color filter layer such that a thickness of the first area is less than a thickness of a second area, different from the first area, of the color filter layer.

8. The liquid crystal display of claim **1**, wherein

the second substrate comprises a color filter layer, and

the color filter layer includes at least one penetrating hole formed therethrough at an area corresponding to the reflective area of a corresponding pixel of the pixels.

9. The liquid crystal display of claim **8**, wherein a cell gap of the area at which the penetrating hole is formed is greater than a cell gap of another area of the color filter layer.

10. The liquid crystal display of claim **1**, wherein the second substrate comprises:

a common electrode which forms an electric field with the transmissive pixel electrode and the reflective pixel electrode; and

at least one dividing pattern disposed on at least one of the transmissive pixel electrode, the reflective pixel area and the common electrode, wherein the at least one dividing pattern divides the liquid crystal layer into domains.

11. The liquid crystal display of claim **1**, wherein the reflective pixel electrode comprises a concavo-convex portion.

12. The liquid crystal display of claim **10**, wherein the domains have different areas.

13. The liquid crystal display of claim **1**, further comprising:

a first polarizer disposed on an outer surface of the first substrate;

a second polarizer disposed on an outer surface of the second substrate; and

at least one phase retardation film disposed at least one of between the first substrate and the first polarizer and between the second substrate and the second polarizer.

14. The liquid crystal display of claim **13**, wherein at least one of the first polarizer, the second polarizer and the at least one phase retardation film comprises an anti-glare portion disposed thereon.

15. A method of manufacturing a liquid crystal display, the method comprising:

forming a first substrate comprising pixels, each of which includes a transmissive area and a reflective area;

forming a second substrate opposite to the first substrate; and

forming a liquid crystal layer between the first substrate and the second substrate,

wherein the forming the first substrate comprises:

forming a first thin film transistor, a second thin film transistor, and a third thin film transistor on a first insulating substrate disposed on the first substrate;

forming a transmissive pixel electrode, connected to the first thin film transistor, in the transmissive area and;

forming a reflective pixel electrode, connected to the second thin film transistor, in the reflective area; and

forming a voltage controller overlapping at least a portion of the transmissive pixel electrode.

16. The method of claim **15**, wherein a cell gap of the transmissive area is greater than or equal to a cell gap of the reflective area.

17. The method of claim **16**, wherein the forming the first thin film transistor, the second thin film transistor and the third thin film transistor comprises:

forming a first gate line and a second gate line on the first substrate;

forming a data line which crosses the first gate line and the second gate line on the first substrate;

interposing a gate insulating layer between the data line and each of the first gate line and the second gate line;

forming the first thin film transistor and the second thin film transistor connected to the first gate line and the data line, respectively; and

forming the third thin film transistor connected to a drain electrode of the second thin film transistor and the second gate line.

18. The method of claim **17**, wherein the forming the voltage controller comprises:

forming a storage line, spaced apart from and insulated from the first gate line and the second gate line, on the first substrate;

forming a charge dividing electrode, connected to the third thin film transistor and which overlaps at least a portion the storage line, on the first substrate; and

interposing the gate insulating layer between the charge dividing electrode and the storage line.

19. The method of claim **18**, wherein

the charge dividing electrode overlaps at least a portion of the transmissive pixel electrode, and

a protective layer is interposed between the charge dividing electrode and the at least a portion of the transmissive pixel electrode.

20. The method of claim **15**, wherein the preparing the second substrate comprises:

forming a common electrode, configured to form an electric field with the transmissive pixel electrode and the reflective pixel electrode, on a second insulating layer; and

forming at least one dividing pattern in the common electrode,

wherein the forming the first substrate further comprises forming at least one dividing pattern in at least one of the transmissive pixel electrode and the reflective pixel electrode.

21. The method of claim **15**, wherein the forming the first thin film transistor, the second thin film transistor and the third thin film transistor comprises:

forming a first gate line and a second gate line on the first substrate;

forming a data line which crosses the first gate line and the second gate line on the first substrate;

interposing a gate insulating layer between the data line and both the first gate line and the second gate line; and

connecting the first thin film transistor and the second thin film transistor to the first gate line and the data line; and

connecting the third thin film transistor to the transmissive pixel electrode and the second gate line.

22. The method of claim **21**, wherein the forming the voltage controller comprises:

forming a storage line, spaced apart from and insulated from the first gate line and the second gate line, on the first substrate;

forming a charge dividing electrode, connected to the third thin film transistor and which overlaps at least a portion of the storage line, on the first substrate; and

interposing the gate insulating layer between the charge dividing electrode and the storage line.

23. The method of claim **22**, wherein

the charge dividing electrode overlaps at least a portion of the transmissive pixel electrode, and

a protective layer is interposed between the charge dividing electrode and the at least a portion of the transmissive pixel electrode.

24. The method of claim **15**, wherein the forming the second substrate comprises:

forming a common electrode, configured to form an electric field with the transmissive pixel electrode and the reflective pixel electrode, on a second insulating layer; and

forming at least one dividing pattern in the common electrode,

wherein the forming the first substrate further comprises forming at least one dividing pattern in at least one of the transmissive pixel electrode and the reflective pixel electrode.

25. A liquid crystal display comprising:

a first substrate comprising pixels, each of which includes a transmissive area and a reflective area;

a second substrate facing the first substrate; and

a liquid crystal layer disposed between the first substrate and the second substrate,

wherein

each pixel comprises:

a first thin film transistor which outputs a first data signal in response to a gate signal;

a second thin film transistor which outputs a second data signal in response to the gate signal;

a transmissive pixel electrode disposed in the transmissive area and connected to the first thin film transistor, and which charges a first pixel voltage in response to the first data signal; and

a reflective pixel electrode disposed in the reflective area and connected to the second thin film transistor and which charges a second pixel voltage in response to the second data signal, and

the second substrate comprises:

a common electrode which forms an electric field with the transmissive pixel electrode and the reflective pixel electrode; and

at least one dividing pattern disposed on at least one of the transmissive pixel electrode, the reflective pixel electrode and the common electrode to divide the liquid crystal layer into domains.

26. The liquid crystal display of claim **25**, wherein a cell gap of the transmissive area is greater than or equal to a cell gap of the reflective area.

27. The liquid crystal display of claim **25**, further comprising:

a first sub-thin film transistor which outputs a first sub-data signal in response to the gate signal; and

a voltage controller connected to the first sub-thin film transistor,

wherein the transmissive pixel electrode comprises:

a first transmissive pixel electrode connected to a drain electrode of the first thin film transistor to charge a first transmissive pixel voltage; and

a second transmissive pixel electrode spaced apart from the first transmissive pixel electrode and connected to the first sub-thin film transistor to charge a second transmissive pixel voltage,

wherein the voltage controller controls the first transmissive pixel voltage and the second transmissive pixel voltage in response to a next gate signal of a next pixel generated after the gate signal.

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专利名称(译)	液晶显示器及其制造方法		
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申请号	US12/620801	申请日	2009-11-18
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	JEONG YOUN HAK YEOM JOOSEOK OH KEUNCHAN LEE HEEHWAN LYU JAEJIN		
发明人	JEONG, YOUN HAK YEOM, JOOSEOK OH, KEUNCHAN LEE, HEEHWAN LYU, JAEJIN		
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摘要(译)

一种液晶显示器，包括：第一基板，包括像素，每个像素具有透射区域和反射区域;第二基板;以及液晶层，设置在第一基板和第二基板之间。每个像素包括响应于第一栅极信号输出数据信号的第一和第二薄膜晶体管，设置在透射区域中并且电连接到第一薄膜晶体管以基于第一薄膜晶体管充电第一像素电压的透射像素电极。数据信号，设置在反射区域中并且电连接到第二薄膜晶体管以基于数据信号对第二像素电压充电的反射像素电极，以及控制第一像素电压和第二像素电压的电压控制器响应于在第一栅极信号之后产生的第二栅极信号。