



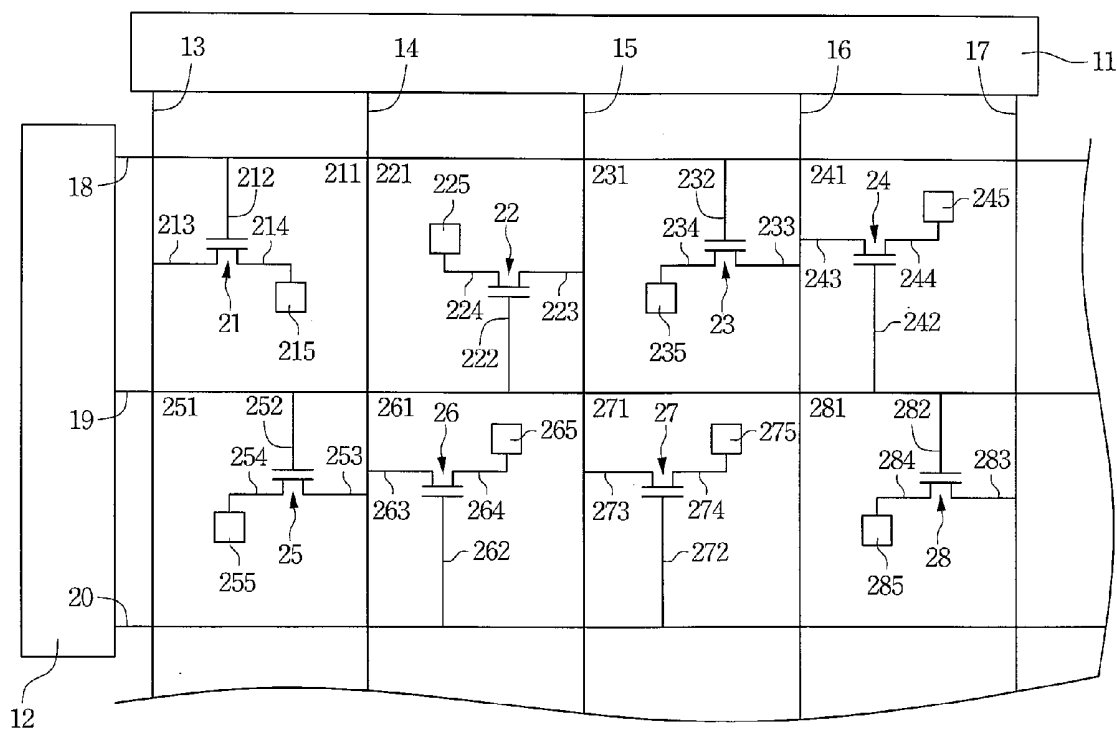
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(19) **United States**(12) **Patent Application Publication**
Liu et al.(10) **Pub. No.: US 2009/0109357 A1**(43) **Pub. Date: Apr. 30, 2009**(54) **LIQUID CRYSTAL DISPLAY DEVICE AND
METHOD FOR DRIVING THE SAME**(30) **Foreign Application Priority Data**

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Chi-Wen Chen, Hsin-Chu (TW)****Publication Classification**(51) **Int. Cl.**
G09G 3/36 (2006.01)
G02F 1/133 (2006.01)(52) **U.S. Cl.** **349/37; 349/48**(57) **ABSTRACT**

A method for driving a liquid crystal display device includes the following steps. A driving circuit and a display unit are provided, the driving circuit comprising a plurality of data lines for transferring data voltages to drive the display unit, wherein each adjacent two of the data lines are supplied with voltages of opposite polarities, and all the data lines in one frame period are supplied with voltages of the same polarity. Two adjacent pixel areas are combined to form one pixel unit, wherein the two adjacent pixel areas are supplied with the same polarity, and the adjacent two pixel units are supplied with opposite polarities.

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CORPORATION, Hsin-Chu (TW)**(21) Appl. No.: **12/104,863**(22) Filed: **Apr. 17, 2008**

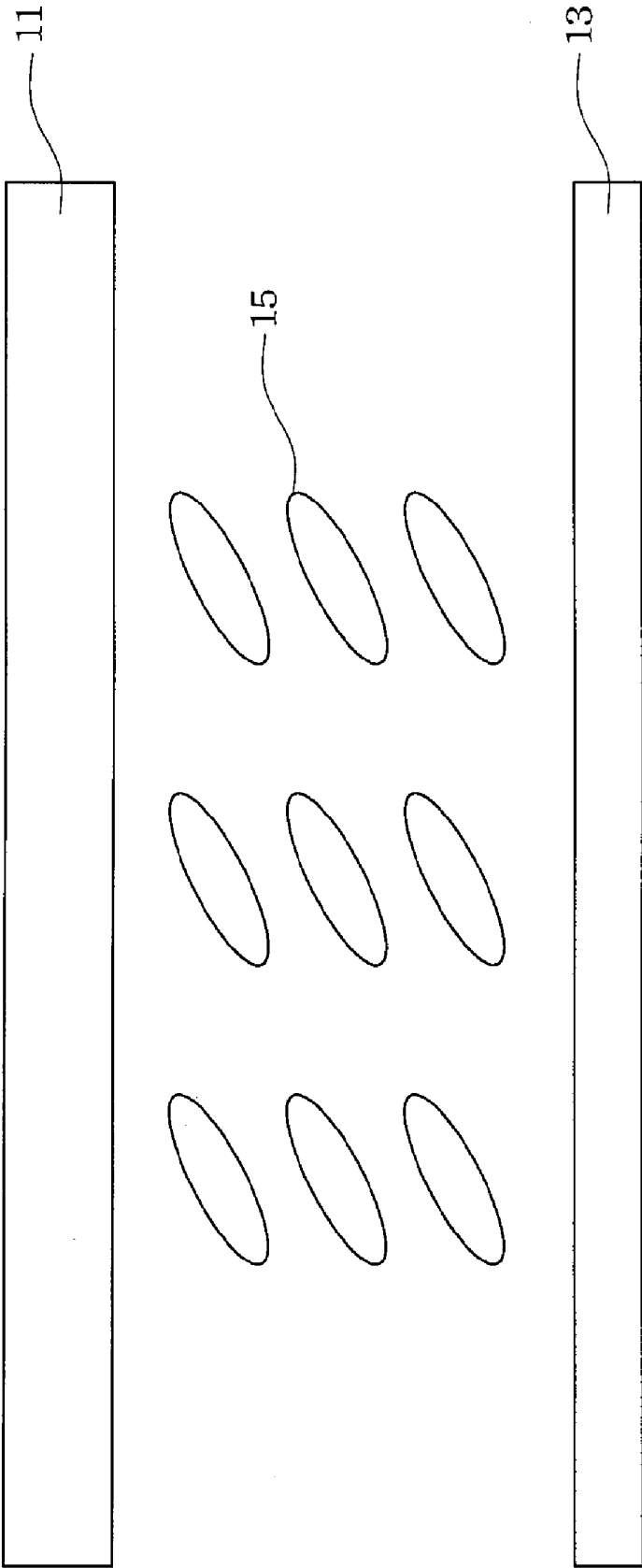


Fig. 1

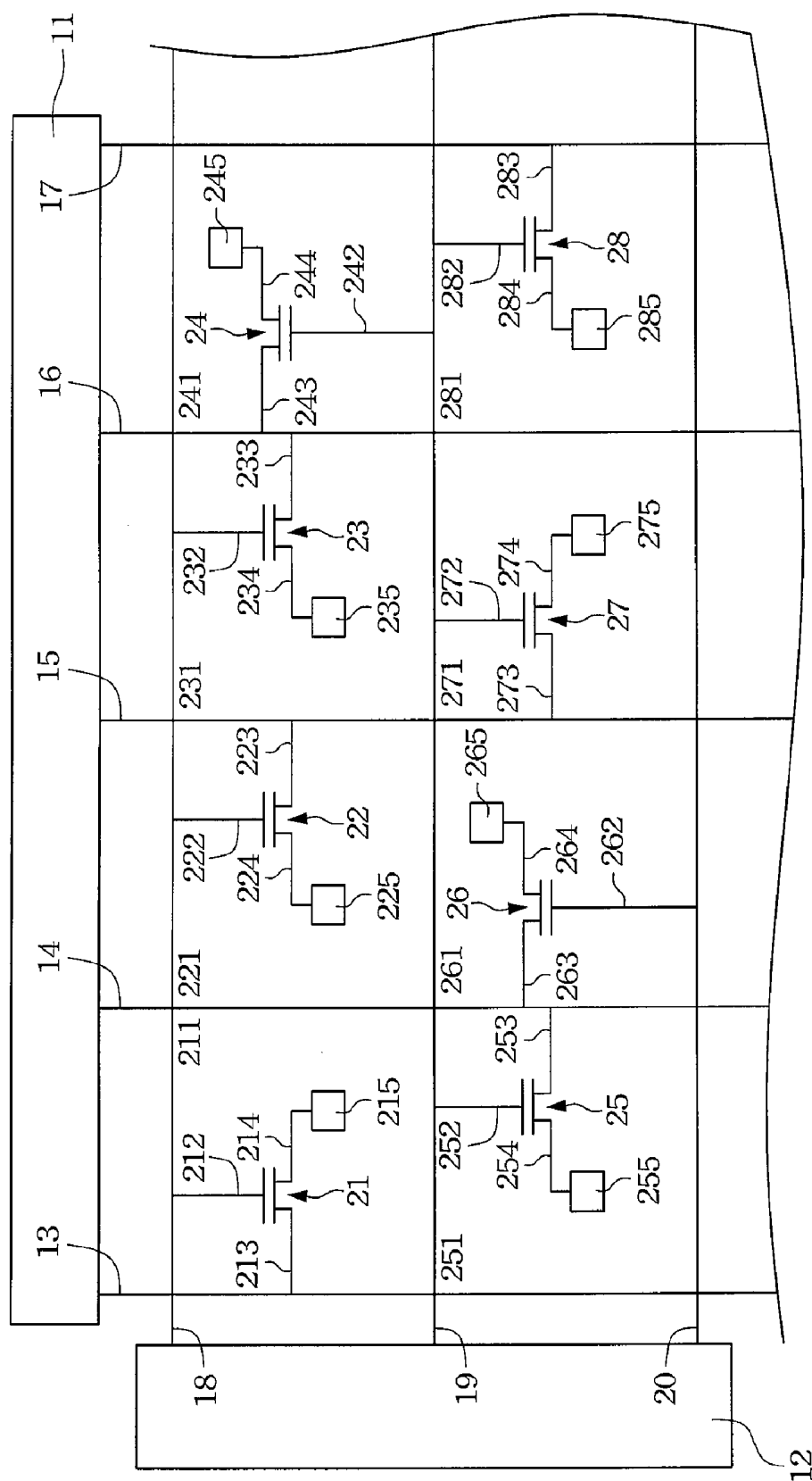


Fig. 2

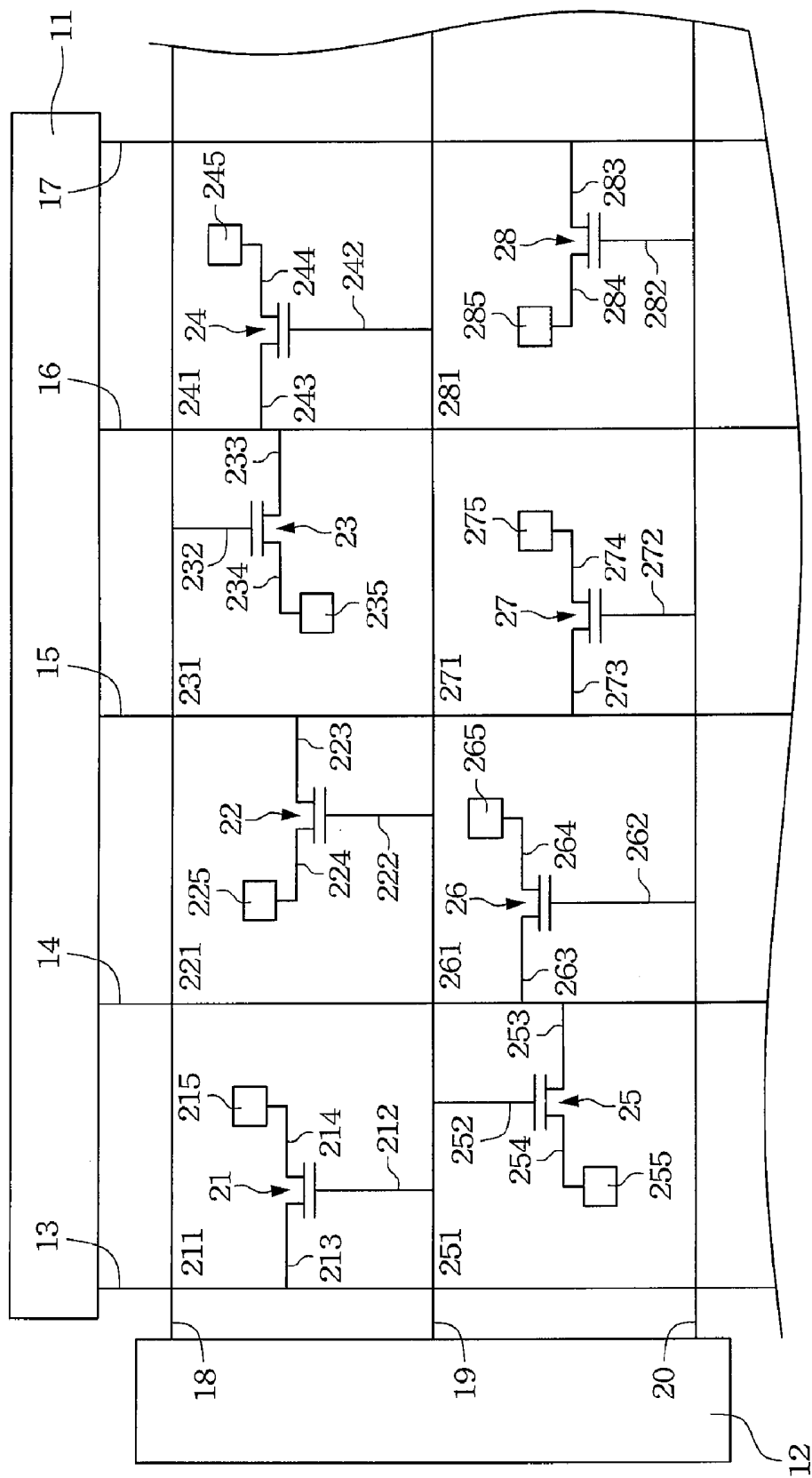


Fig. 3

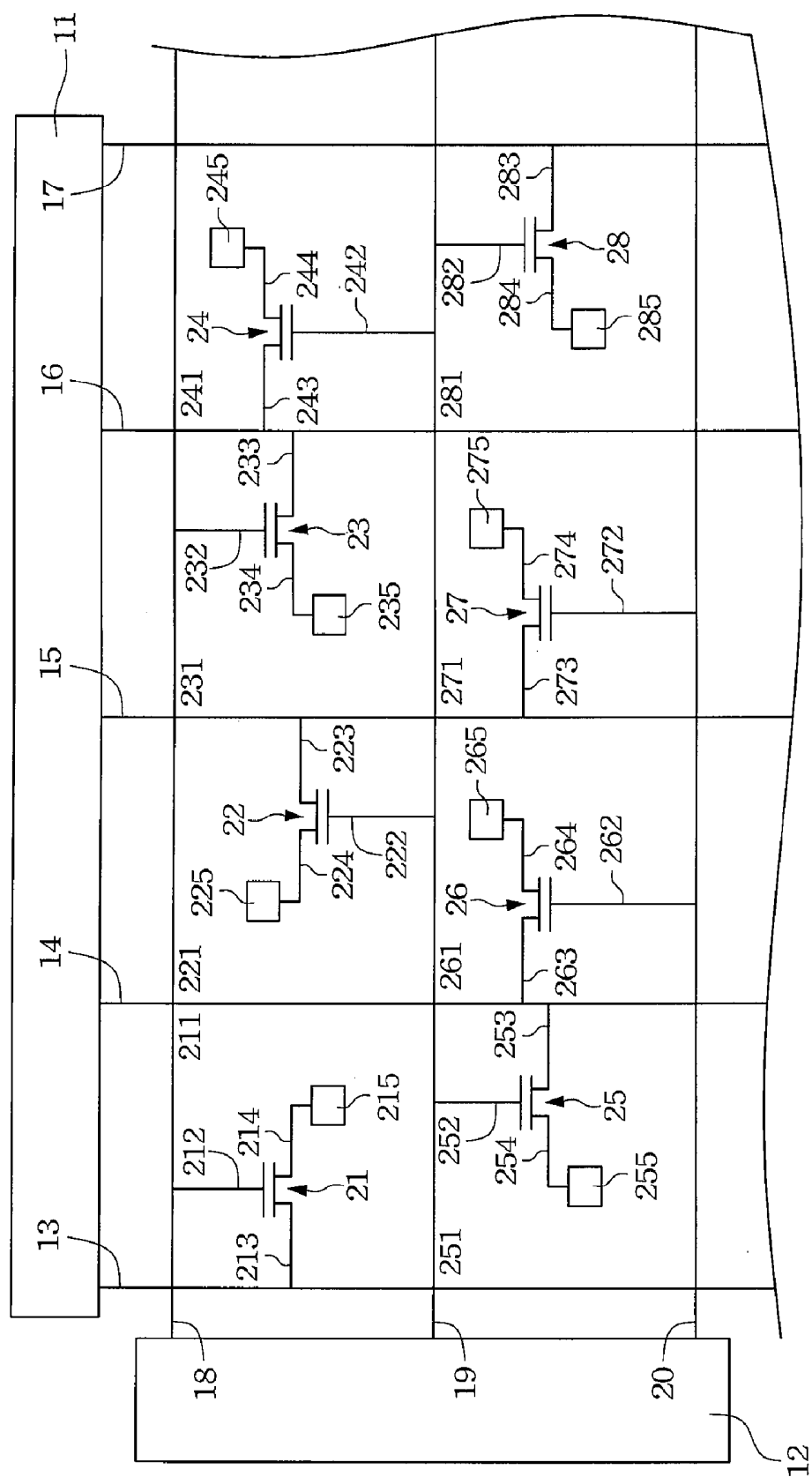


Fig. 4

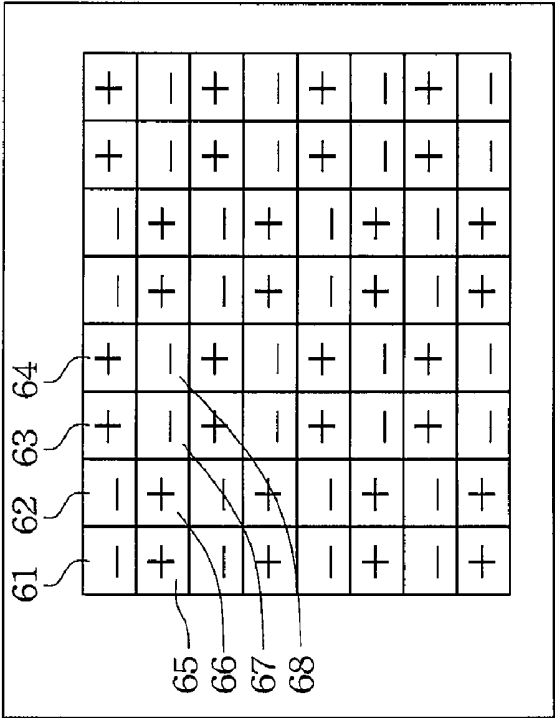


Fig. 5A

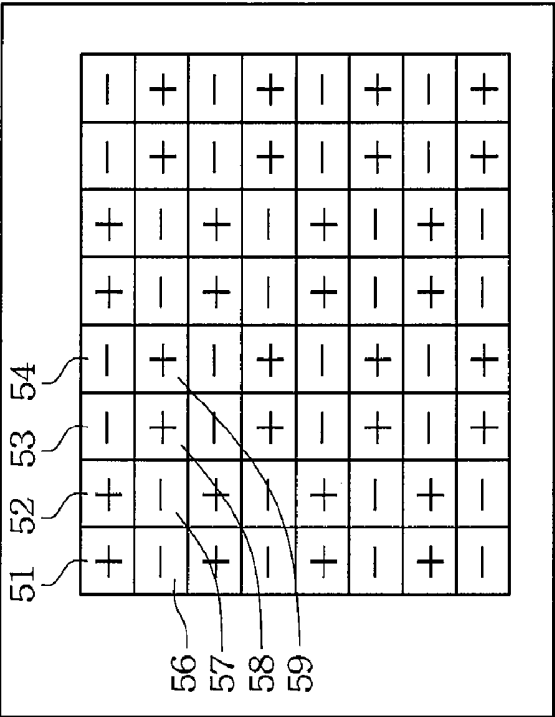


Fig. 5B

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING THE SAME

RELATED APPLICATIONS

[0001] This application claims priority to Taiwan Patent Application Serial Number 96140852, filed Oct. 30, 2007, which is herein incorporated by reference.

BACKGROUND

[0002] 1. Field of Invention

[0003] The present invention relates to a liquid crystal display device. More particularly, the present invention relates to a pixel structure and its driving method of a liquid crystal display device.

[0004] 2. Description of Related Art

[0005] During driving a liquid crystal display device, a driving voltage cannot be fixed at a voltage value, otherwise characteristics of crystal molecules might be damaged by a long-period driving. Therefore, every now and then, the driving voltage must be altered to avoid such damages upon the crystal molecules.

[0006] In order to solve this issue, driving phases for the liquid crystal display device are divided into two types: positive polarity and negative polarity. When a pixel electrode is supplied with a higher voltage than a common electrode is supplied with, the pixel is positively polarized. When a pixel electrode is supplied with a lower voltage than a common electrode is supplied with, the pixel is negatively polarized. When a voltage difference between the pixel electrode and the common electrode is the same, the same grayness would be presented by the pixel.

[0007] Several conventional polarity inversions between positive polarity and negative polarity are listed as follows: frame inversion, row inversion, column inversion and dot inversion.

[0008] When a frame refreshes, flickers are generated by the liquid crystal display device and make human eyes uncomfortable. The flickers are most-frequently generated when the frame inversion is applied in the liquid crystal display device. Other inversion ways may produce the flickers, but not as frequent as the frame inversion does.

[0009] Another issue of the liquid crystal display device is "cross talk", which means adjacent pixels interfere with each other, thereby displaying incorrect information. Dot inversion is the best way to reduce cross talk, but also consumes more power than the other inversion ways. How to reduce "cross talk", "flicker" and consume less power in a liquid crystal display device is an urgent issue for those persons skilled in the art.

[0010] For the foregoing reasons, there is a need for an improved pixel structure and its driving method of a liquid crystal display device.

SUMMARY

[0011] It is therefore an objective of the present invention to provide a pixel structure and its driving method of a liquid crystal display device.

[0012] In accordance with the foregoing and other objectives of the present invention, a method for driving a liquid crystal display device includes the following steps. A driving circuit and a display unit are provided, the driving circuit comprising a plurality of data lines for transferring data voltages to drive the display unit, wherein each adjacent two of

the data lines are supplied with voltages of opposite polarities, and all the data lines in one frame period are supplied with voltages of the same polarity. Two adjacent pixel areas are combined to form one pixel unit, wherein the two adjacent pixel areas are supplied with the same polarity, and the adjacent two pixel units are supplied with opposite polarities.

[0013] In accordance with the foregoing and other objectives of the present invention, a liquid crystal display device comprises a plurality of data lines, a plurality of scan lines, a transistor, a first pixel unit and a second pixel unit. The data lines are substantially in parallel with one another. The scan lines are perpendicularly crossed the data lines, one pixel area is defined as an overlapped area of the area between the two adjacent data lines and the area between the two adjacent scan lines, whereby a plurality of pixel areas are formed among the data lines and the scan lines. The transistor comprises a gate electrode, a source electrode and a drain electrode. The transistor is disposed within each of the pixel areas and electrically connected to the data lines and the scan lines. The first pixel unit includes adjacent two of the pixel areas and the two transistors, wherein the drain electrodes of the two transistors are respectively connected to different two of the data lines. The second pixel unit includes adjacent two of the pixel areas and the two transistors, wherein the drain electrodes of the two transistors are respectively connected to one of the data lines, the second pixel unit is immediately adjacent to the first pixel unit.

[0014] In accordance with the foregoing and other objectives of the present invention, a liquid crystal display device includes the following components. A plurality of data lines includes a first data line, a second data line, a third data line, a fourth data line and fifth data line, which are serially arranged and substantially in parallel with one another. A plurality of scan lines are perpendicularly crossed the data lines. One pixel area is defined as an overlapped area of the area between the two adjacent data lines and the area between the two adjacent scan lines, whereby a plurality of pixel areas are formed among the data lines and the scan lines, and the scan lines comprises a first scan line, a second scan line and a third scan line. Each of a plurality of crystal capacitors is disposed within each pixel area. Each of transistors includes a gate electrode, a source electrode and a drain electrode, and the transistor is electrically connected to one of the data lines, one of crystal capacitors and one of the scan lines. The transistors includes as follows:

[0015] A first transistor includes its drain electrode electrically connected to the first data line and its gate electrode electrically connected to the first scan line or the second scan line;

[0016] A second transistor includes its drain electrode electrically connected to the third data line and its gate electrode electrically connected to the first scan line or the second scan line;

[0017] A third transistor includes its drain electrode electrically connected to the fourth data line and its gate electrode electrically connected to the first scan line or the second scan line;

[0018] A fourth transistor includes its drain electrode electrically connected to the fifth data line and its gate electrode electrically connected to the first scan line or the second scan line;

[0019] A fifth transistor includes its drain electrode electrically connected to the second data line and its gate electrode electrically connected to the second scan line or the third scan line;

[0020] A sixth transistor includes its drain electrode electrically connected to the second data line and its gate electrode electrically connected to the second scan line or the third scan line;

[0021] A seventh transistor includes its drain electrode electrically connected to the third data line and its gate electrode electrically connected to the second scan line or the third scan line; and

[0022] An eighth transistor includes its drain electrode electrically connected to the fifth data line and its gate electrode electrically connected to the second scan line or the third scan line.

[0023] It is to be understood that both the foregoing general description and the following detailed description are by examples, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0025] FIG. 1 illustrates a cross-sectional view of a pixel structure according to one embodiment of this invention;

[0026] FIG. 2 illustrates a pixel structure according to a first embodiment of this invention;

[0027] FIG. 3 illustrates a pixel structure according to a second embodiment of this invention;

[0028] FIG. 4 illustrates a pixel structure according to a third embodiment of this invention;

[0029] FIG. 5A illustrates a polarity distribution of a first frame based upon the pixel structure and its driving method according to one embodiment of this invention; and

[0030] FIG. 5B illustrates a polarity distribution of a second frame based upon the pixel structure and its driving method according to one embodiment of this invention.

DESCRIPTION OF THE EMBODIMENTS

[0031] Reference will now be made in detail to the present embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0032] FIG. 1 illustrates a cross-sectional view of a pixel structure according to one embodiment of this invention. A plurality of crystal molecules 15 are disposed between a pixel electrode 11 and a common electrode 13. A driving circuit (not illustrated in FIG. 1) supplies the pixel electrode 11 with an electrical voltage while a power supply (not illustrated in FIG. 1) supplies the common electrode 13 with an electrical voltage, thereby driving the crystal molecules 15 to rotate according to an electrical field so as to affect the light transmission rate thereof.

[0033] FIG. 2 illustrates a pixel structure according to a first embodiment of this invention. A data driving circuit 11 sup-

plies data voltages via those data lines (13, 14 . . . 17) while a scan driving circuit 12 supplies scan voltages via those scan lines (18, 19, 20).

[0034] A pixel area 211 is defined as an overlapped area of the area between the two adjacent data lines (13, 14) and the area between the two adjacent scan lines (18, 19). Other pixel areas (221, 231, 241 . . .) are then defined by the same ways. The pixel area 211 includes a transistor 21 and a crystal capacitor 215, which contains the crystal molecules 15 as illustrated in FIG. 1.

[0035] In the first embodiment of this invention, only 8 (2×4) pixels are illustrated as those 8 pixels as an unit will be repeated in a display unit. There are eight pixel areas: a first pixel area 211, a second pixel area 221, a third pixel area 231, a fourth pixel area 241, a fifth pixel area 251, a sixth pixel area 261, a seventh area 271 and an eighth area 281. Five data lines (13, 14, 15, 16, 17) and three scan lines (18, 19, 20) are used to define those eight pixel areas, where the data lines are electrically connected to drain electrodes of transistors within each pixel, and the scan lines are electrically connected to gate electrodes of transistors within each pixel. The electrical connection details of each transistor in the first embodiment are described as follows:

[0036] In the pixel area 211, a transistor 21 has a drain electrode 213 electrically connected to a first data line 13, a source electrode 214 electrically connected to a first crystal capacitor 215 and a gate electrode 212 electrically connected to a first scan line 18.

[0037] In the pixel area 221, a transistor 22 has a drain electrode 223 electrically connected to a third data line 15, a source electrode 224 electrically connected to a second crystal capacitor 225 and a gate electrode 222 electrically connected to a first scan line 18.

[0038] In the pixel area 231, a transistor 23 has a drain electrode 233 electrically connected to a fourth data line 16, a source electrode 234 electrically connected to a third crystal capacitor 235 and a gate electrode 232 electrically connected to a first scan line 18.

[0039] In the pixel area 241, a transistor 24 has a drain electrode 243 electrically connected to a fourth data line 16, a source electrode 244 electrically connected to a fourth crystal capacitor 245 and a gate electrode 242 electrically connected to a second scan line 19.

[0040] In the pixel area 251, a transistor 25 has a drain electrode 253 electrically connected to a second data line 14, a source electrode 254 electrically connected to a fifth crystal capacitor 255 and a gate electrode 252 electrically connected to a second scan line 19.

[0041] In the pixel area 261, a transistor 26 has a drain electrode 263 electrically connected to a second data line 14, a source electrode 264 electrically connected to a sixth crystal capacitor 265 and a gate electrode 262 electrically connected to a third scan line 20.

[0042] In the pixel area 271, a transistor 27 has a drain electrode 273 electrically connected to a third data line 15, a source electrode 274 electrically connected to a seventh crystal capacitor 275 and a gate electrode 272 electrically connected to a second scan line 19.

[0043] In the pixel area 281, a transistor 28 has a drain electrode 283 electrically connected to a fifth data line 17, a source electrode 284 electrically connected to an eighth crystal capacitor 285 and a gate electrode 282 electrically connected to a second scan line 19.

[0044] Given the first embodiment of the pixel structure, the first crystal capacitor 215, the second crystal capacitor 225, the seventh crystal capacitor 275 and the eighth crystal capacitor 285 can be operated with the same polarity while the third crystal capacitor 235, the fourth crystal capacitor 245, the fifth crystal capacitor 255 and the sixth crystal capacitor 265 can also be operated with the same polarity. For example (as illustrated in FIG. 5A), a first frame is achieved by supplying pixel areas (51, 52, 58, 59) with positive polarity and supplying pixel areas (53, 54, 56, 57) with negative polarity.

[0045] For the next frame (a second frame), the first crystal capacitor 215, the second crystal capacitor 225, the seventh crystal capacitor 275 and the eighth crystal capacitor 285 can be operated with the same polarity but opposite to the first frame while the third crystal capacitor 235, the fourth crystal capacitor 245, the fifth crystal capacitor 255 and the sixth crystal capacitor 265 can also be operated with the same polarity but opposite to the first frame. For example (as illustrated in FIG. 5B), the second frame is achieved by supplying pixel areas (61, 62, 67, 68) with negative polarity and supplying pixel areas (63, 64, 65, 66) with positive polarity.

[0046] By combining two pixel areas as a pixel unit, adjacent two pixel units can be operated with opposite polarities, thereby reducing "cross talk" using column inversion to drive the pixel structure. Besides, using column inversion to drive the pixel structure has advantages of lower power consumptions and lessened flickers, thereby improving display quality.

[0047] In a conventional LCD device, for example, 16 transistors are respectively connected to one scan line while the 16 transistors are respectively connected to 16 data lines. In embodiments of this invention, for example, gate electrodes of 16 transistors are respectively connected to one of several scan lines while 17 data lines supply data voltages to 16 crystal capacitors. One more data line is used compared to the conventional LCD device. In another embodiment of this invention, a LCD device has 8 transistors, which are electrically connected to one of the data lines while 9 scan lines are electrically connected to gate electrodes of the 8 transistors. One more scan line is used compared to the conventional LCD device.

[0048] FIG. 3 illustrates a pixel structure according to a second embodiment of this invention. Compared to the first embodiment, gate electrodes of transistors (21, 22, 27, 28) are respectively electrically connected a different scan line. The electrical connection details of each transistor in the second embodiment are described as follows:

[0049] In the pixel area 211, a transistor 21 has a drain electrode 213 electrically connected to a first data line 13, a source electrode 214 electrically connected to a first crystal capacitor 215 and a gate electrode 212 electrically connected to a second scan line 19.

[0050] In the pixel area 221, a transistor 22 has a drain electrode 223 electrically connected to a third data line 15, a source electrode 224 electrically connected to a second crystal capacitor 225 and a gate electrode 222 electrically connected to a second scan line 19.

[0051] In the pixel area 231, a transistor 23 has a drain electrode 233 electrically connected to a fourth data line 16, a source electrode 234 electrically connected to a third crystal capacitor 235 and a gate electrode 232 electrically connected to a first scan line 18.

[0052] In the pixel area 241, a transistor 24 has a drain electrode 243 electrically connected to a fourth data line 16, a source electrode 244 electrically connected to a fourth crystal capacitor 245 and a gate electrode 242 electrically connected to a second scan line 19.

[0053] In the pixel area 251, a transistor 25 has a drain electrode 253 electrically connected to a second data line 14, a source electrode 254 electrically connected to a fifth crystal capacitor 255 and a gate electrode 252 electrically connected to a second scan line 19.

[0054] In the pixel area 261, a transistor 26 has a drain electrode 263 electrically connected to a second data line 14, a source electrode 264 electrically connected to a sixth crystal capacitor 265 and a gate electrode 262 electrically connected to a third scan line 20.

[0055] In the pixel area 271, a transistor 27 has a drain electrode 273 electrically connected to a third data line 15, a source electrode 274 electrically connected to a seventh crystal capacitor 275 and a gate electrode 272 electrically connected to a third scan line 20.

[0056] In the pixel area 281, a transistor 28 has a drain electrode 283 electrically connected to a fifth data line 17, a source electrode 284 electrically connected to an eighth crystal capacitor 285 and a gate electrode 282 electrically connected to a third scan line 20.

[0057] As the crystal capacitor's polarity inversion is subject to data voltages, data lines connection in this embodiment is the same as the first embodiment, thereby producing the results as illustrated FIG. 5A and FIG. 5B. Using column inversion to drive the pixel structure has advantages of lower power consumptions and lessened flickers, thereby improving display quality.

[0058] FIG. 4 illustrates a pixel structure according to a third embodiment of this invention. Compared to the first embodiment, gate electrodes of transistors (22, 27) are respectively electrically connected with a different scan line. The electrical connection details of each transistor in the third embodiment are described as follows:

[0059] In the pixel area 211, a transistor 21 has a drain electrode 213 electrically connected to a first data line 13, a source electrode 214 electrically connected to a first crystal capacitor 215 and a gate electrode 212 electrically connected to a first scan line 18.

[0060] In the pixel area 221, a transistor 22 has a drain electrode 223 electrically connected to a third data line 15, a source electrode 224 electrically connected to a second crystal capacitor 225 and a gate electrode 222 electrically connected to a second scan line 19.

[0061] In the pixel area 231, a transistor 23 has a drain electrode 233 electrically connected to a fourth data line 16, a source electrode 234 electrically connected to a third crystal capacitor 235 and a gate electrode 232 electrically connected to a first scan line 18.

[0062] In the pixel area 241, a transistor 24 has a drain electrode 243 electrically connected to a fourth data line 16, a source electrode 244 electrically connected to a fourth crystal capacitor 245 and a gate electrode 242 electrically connected to a second scan line 19.

[0063] In the pixel area 251, a transistor 25 has a drain electrode 253 electrically connected to a second data line 14, a source electrode 254 electrically connected to a fifth crystal capacitor 255 and a gate electrode 252 electrically connected to a second scan line 19.

[0064] In the pixel area 261, a transistor 26 has a drain electrode 263 electrically connected to a second data line 14, a source electrode 264 electrically connected to a sixth crystal capacitor 265 and a gate electrode 262 electrically connected to a third scan line 20.

[0065] In the pixel area 271, a transistor 27 has a drain electrode 273 electrically connected to a third data line 15, a source electrode 274 electrically connected to a seventh crystal capacitor 275 and a gate electrode 272 electrically connected to a third scan line 20.

[0066] In the pixel area 281, a transistor 28 has a drain electrode 283 electrically connected to a fifth data line 17, a source electrode 284 electrically connected to an eighth crystal capacitor 285 and a gate electrode 282 electrically connected to a second scan line 19.

[0067] As the crystal capacitor's polarity inversion is subject to data voltages, data lines connection in this embodiment is the same as the first embodiment, thereby producing the results as illustrated FIG. 5A and FIG. 5B. Using column inversion to drive the pixel structure has advantages of lower power consumptions and lessened flickers, thereby improving display quality.

[0068] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A method for driving a liquid crystal display device, comprising:

providing a driving circuit and a display unit, the driving circuit comprising a plurality of data lines for transferring data voltages to drive the display unit, wherein each adjacent two of the data lines are supplied with voltages of opposite, and all the data lines within one frame period are supplied with voltages of the same polarity; and

combining two adjacent pixel areas to form one pixel unit, wherein the two adjacent pixel areas are supplied with the same polarity, and the adjacent two pixel units are supplied with opposite polarities.

2. The method for driving a liquid crystal display device of claim 1, wherein the driving circuit further comprises a plurality of scan lines for transferring scan voltages to drive the display unit.

3. The method for driving a liquid crystal display device of claim 2, wherein each of the pixel areas is an overlapped area of the area between the two adjacent data lines and the area between the two adjacent scan lines.

4. The method for driving a liquid crystal display device of claim 2, wherein each of the pixel areas comprises a crystal capacitor containing crystal molecules, switching the voltage polarity of the data voltages inverses each crystal molecule of the crystal capacitor.

5. The method for driving a liquid crystal display device of claim 4, further comprising a step of providing a common electrode electrically connected to an electrode of the crystal capacitor, and the driving circuit being electrically connected to the other electrode of the crystal capacitor.

6. The method for driving a liquid crystal display device of claim 5, wherein when the driving circuit provides a higher voltage than the common electrode does, the crystal capacitor is positively polarized.

7. The method for driving a liquid crystal display device of claim 5, wherein when the driving circuit provides a lower voltage than the common electrode does, the crystal capacitor is negatively polarized.

8. A liquid crystal display device comprising:

a plurality of data lines, being substantially in parallel with one another;

a plurality of scan lines being perpendicularly crossed the data lines, one pixel areas being defined as an overlapped area of the area between the two adjacent data lines and the area between the two adjacent scan lines, whereby a plurality of pixel areas are formed among the data lines and the scan lines;

a transistor comprising a gate electrode, a source electrode and a drain electrode, the transistor being disposed within each of the pixel areas and electrically connected to the data lines and the scan lines;

a first pixel unit, comprising adjacent two of the pixel areas and the two transistors, wherein the drain electrodes of the two transistors are respectively connected to different two of the data lines; and

a second pixel unit, comprising adjacent two of the pixel areas and the two transistors, wherein the drain electrodes of the two transistors are respectively connected to one of the data lines, the second pixel unit is immediately adjacent to the first pixel unit.

9. The liquid crystal display device of claim 8, wherein:

the data lines comprising a first data line, a second data line, a third data line, a fourth data line and fifth data line, serially arranged; and

the scan lines comprising a first scan line and a second scan line.

10. The liquid crystal display device of claim 9, wherein the first pixel unit comprising:

a first transistor, comprising its drain electrode electrically connected to the first data line and its gate electrode electrically connected to the first scan line or the second scan line; and

a second transistor, comprising its drain electrode electrically connected to the third data line and its gate electrode electrically connected to the first scan line or the second scan line, wherein the second transistor is immediately adjacent to the first transistor.

11. The liquid crystal display device of claim 9, wherein the second pixel unit comprising:

a third transistor, comprising its gate electrode electrically connected to the first scan line or the second scan line; and

a fourth transistor, comprising its gate electrode electrically connected to the first scan line or the second scan line, wherein both drain electrodes of the third transistor and the fourth transistor are electrically connected to the fourth data line.

12. The liquid crystal display device of claim 9, wherein the second pixel unit comprising:

a fifth transistor and a sixth transistor comprising their drain electrodes electrically connected to the second data line.

13. The liquid crystal display device of claim 9, wherein the first pixel unit comprising:

- a seventh transistor, comprising its drain electrode electrically connected to the third data line; and
- an eighth transistor, comprising its drain electrode electrically connected to the fifth data line, wherein the eighth transistor is immediately adjacent to the seventh transistor.

14. A liquid crystal display device comprising:

a plurality of data lines comprising a first data line, a second data line, a third data line, a fourth data line and fifth data line, being serially arranged and substantially in parallel with one another;

a plurality of scan lines being perpendicularly crossed the data lines, one pixel areas being defined as an overlapped area of the area between the two adjacent data lines and the area between the two adjacent scan lines, whereby a plurality of pixel areas are formed among the data lines and the scan lines, and the scan lines comprises a first scan line, a second scan line and a third scan line;

a plurality of crystal capacitors, each of the crystal capacitors being disposed within each of the pixel areas; and

a plurality of transistors, each of the transistors comprising a gate electrode, a source electrode and a drain electrode, the transistor being electrically connected to one of the data lines, one of crystal capacitors and one of the scan lines,

wherein the transistors comprising:

- a first transistor, comprising its drain electrode electrically connected to the first data line and its gate electrode electrically connected to the first scan line or the second scan line;

a second transistor, comprising its drain electrode electrically connected to the third data line and its gate electrode electrically connected to the first scan line or the second scan line;

a third transistor, comprising its drain electrode electrically connected to the fourth data line and its gate electrode electrically connected to the first scan line or the second scan line;

a fourth transistor, comprising its drain electrode electrically connected to the fourth data line and its gate electrode electrically connected to the first scan line or the second scan line;

a fifth transistor, comprising its drain electrode electrically connected to the second data line and its gate electrode electrically connected to the second scan line or the third scan line;

a sixth transistor, comprising its drain electrode electrically connected to the second data line and its gate electrode electrically connected to the second scan line or the third scan line;

a seventh transistor, comprising its drain electrode electrically connected to the third data line and its gate electrode electrically connected to the second scan line or the third scan line; and

an eighth transistor, comprising its drain electrode electrically connected to the fifth data line and its gate electrode electrically connected to the second scan line or the third scan line.

* * * * *

专利名称(译)	液晶显示装置及其驱动方法		
公开(公告)号	US20090109357A1	公开(公告)日	2009-04-30
申请号	US12/104863	申请日	2008-04-17
[标]申请(专利权)人(译)	友达光电股份有限公司		
申请(专利权)人(译)	友达光电股份有限公司		
当前申请(专利权)人(译)	友达光电股份有限公司		
[标]发明人	LIU CHUN HSIN FU LI MIN CHEN CHI WEN		
发明人	LIU, CHUN-HSIN FU, LI-MIN CHEN, CHI-WEN		
IPC分类号	G09G3/36 G02F1/133		
CPC分类号	G09G3/3614 G09G3/3648 G09G2320/0247 G09G2320/0219 G09G2320/0204		
优先权	096140852 2007-10-30 TW		
其他公开文献	US8497830		
外部链接	Espacenet USPTO		

摘要(译)

一种驱动液晶显示装置的方法，包括以下步骤。提供一种驱动电路和显示单元，该驱动电路包括多条数据线，用于传输数据电压以驱动显示单元，其中每条相邻的两条数据线被提供相反极性的电压，以及所有数据线在一个帧周期中提供相同极性的电压。组合两个相邻的像素区域以形成一个像素单元，其中两个相邻的像素区域被提供相同的极性，并且相邻的两个像素单元被提供相反的极性。

