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(54) **THIN FILM TRANSISTOR ARRAY PANEL FOR LIQUID CRYSTAL DISPLAY HAVING PIXEL ELECTRODE**

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(57) **ABSTRACT**

A TFT array panel includes an insulating substrate, a gate line and a storage electrode line formed thereon. The gate line and the storage electrode line are covered with a gate insulating layer, and a semiconductor island is formed on the gate insulating layer. A pair of ohmic contacts are formed on the semiconductor island, and a data line and a drain electrode are formed thereon. The data line and the drain electrode are covered with a passivation layer having a contact hole exposing the drain electrode. A pixel electrode is formed on the passivation layer and connected to the drain electrode through the contact hole. The TFT array panel is covered with an alignment layer rubbed approximately in a direction from the upper left corner to the lower right corner of the TFT array panel or the pixel electrodes. The pixel electrode has approximately a rectangular shape and overlaps the gate line and the data line. The pixel electrode has an expansion located near the upper left corner of the pixel electrode to increase the width of the corresponding overlapping area between the pixel electrode and the gate line and/or the data line.

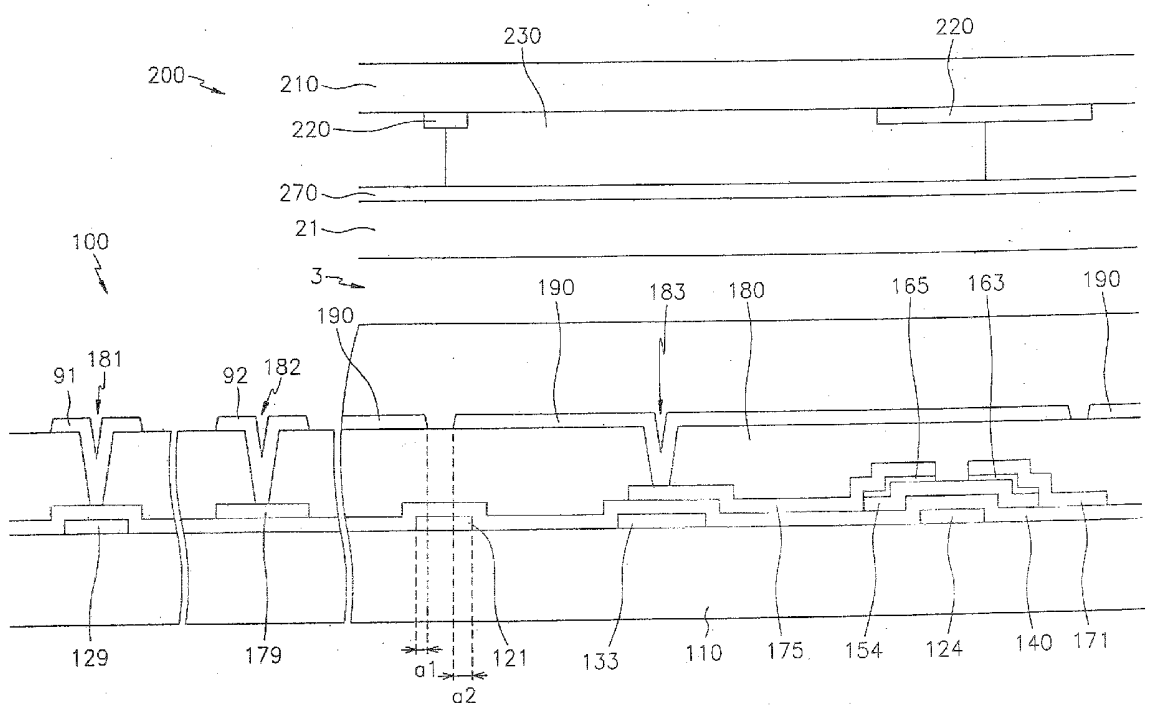


FIG.1

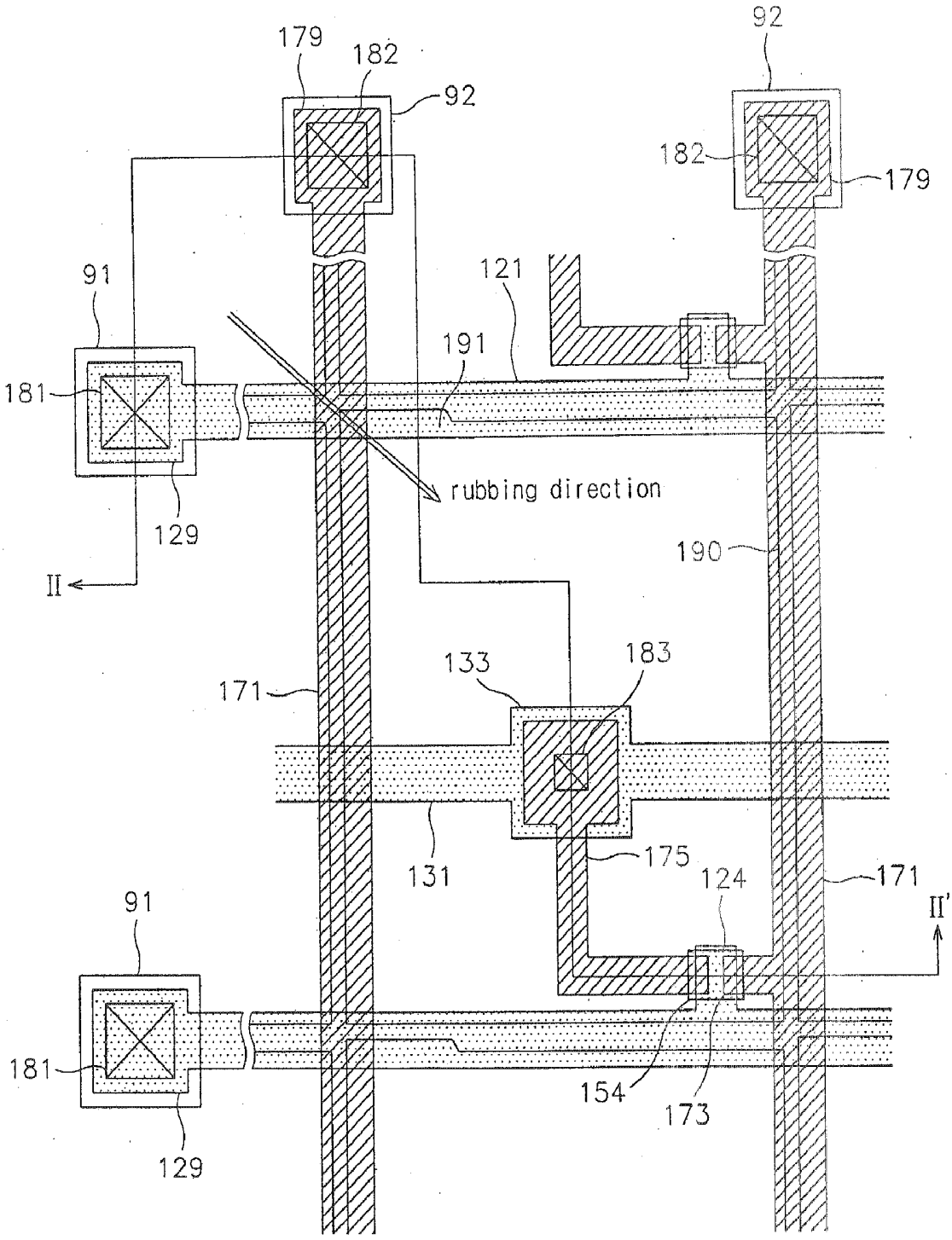

179
182
92
92
182
179
91
121
191
181
rubbing direction
129
190
II
133
183
171
175
131
124
171
II'
91
181
154
173
129

FIG. 2

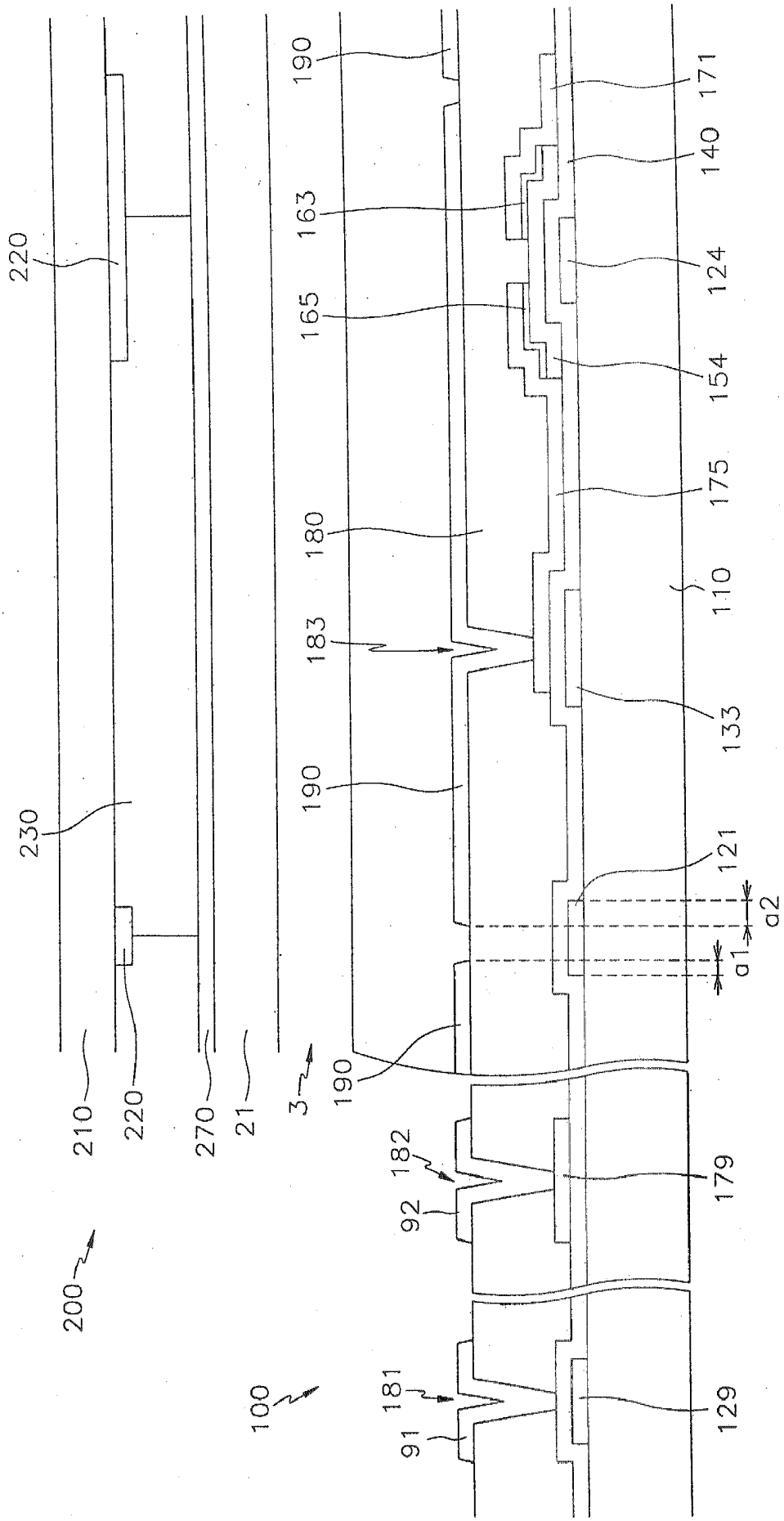

220
230
210
220
270
21
3
190
183
180
165
163
190
190
171
140
124
154
175
110
133
121
a2
a1
182
92
179
181
91
129
200
100

FIG.3

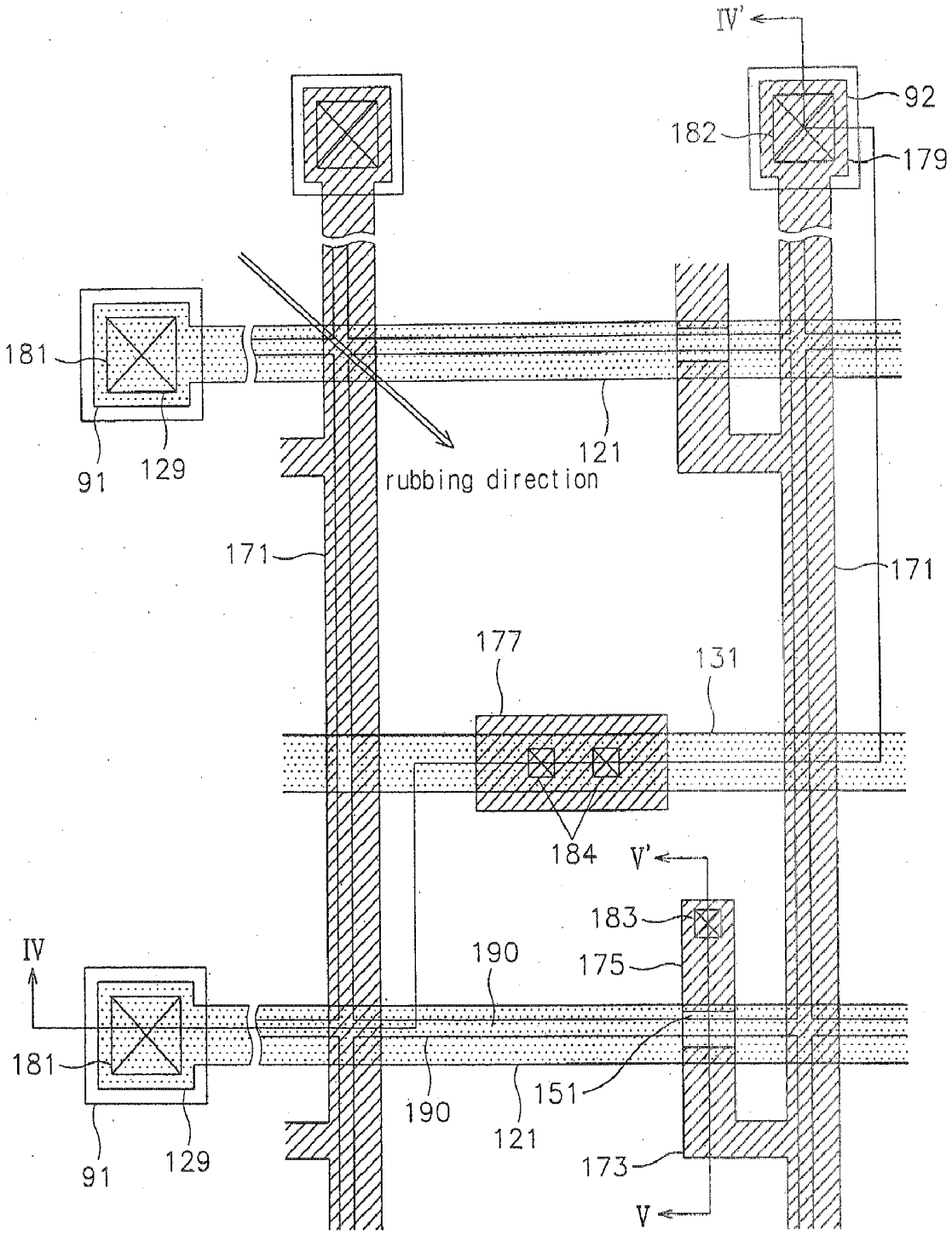
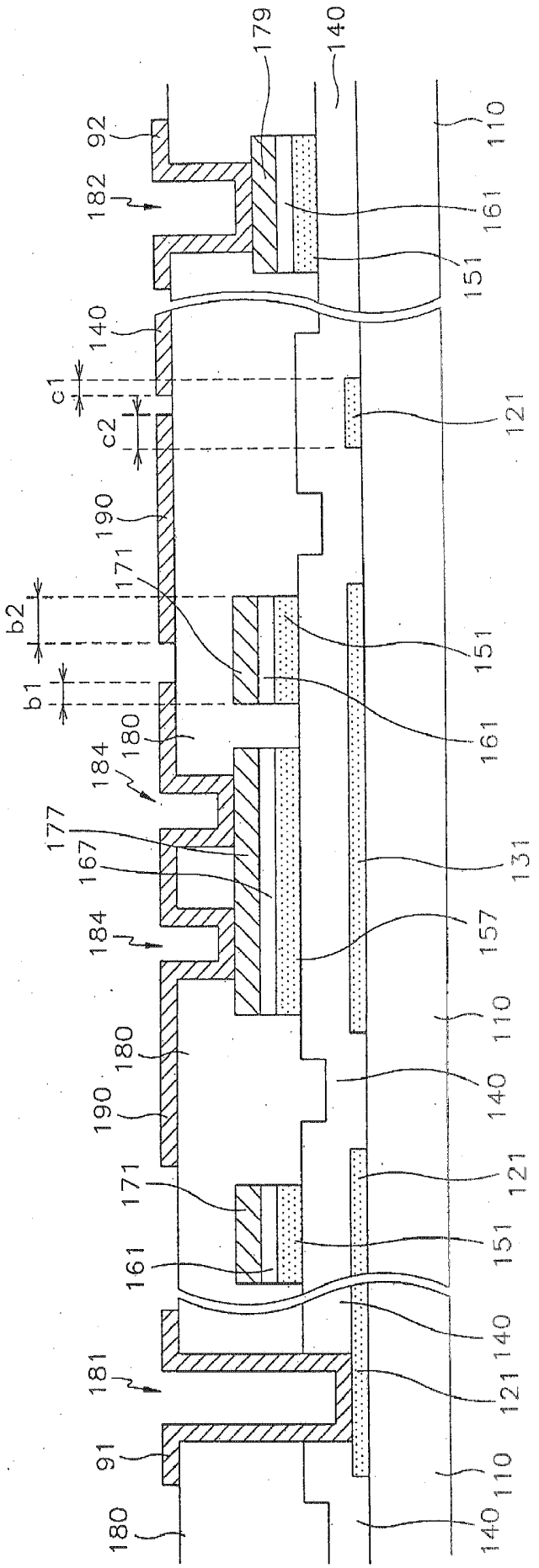

IV'
92
182
179
181
91
129
121
rubbing direction
171
171
177
131
184
V'
183
IV
190
175
181
190
151
121
91
129
173
V

FIG. 4


179
140
92
110
182
161
151
140
c1
c2
121
190
171
b2
151
b1
161
180
184
177
167
131
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121
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151
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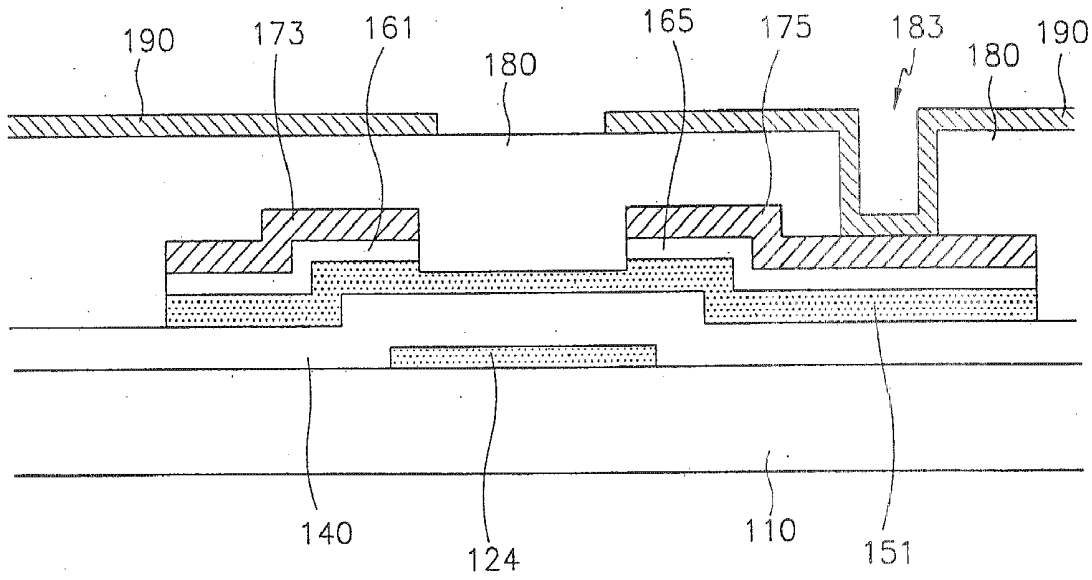
121
91
110
180
140

FIG.5



THIN FILM TRANSISTOR ARRAY PANEL FOR LIQUID CRYSTAL DISPLAY HAVING PIXEL ELECTRODE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a Divisional of U.S. application Ser. No. 10/317,591, filled on Dec. 12, 2002, which claims priority to Korean Application No. 2002-31098 filed on Jun. 3, 2002, which are all hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] (a) Field of the Invention

[0003] The present invention relates to a thin film transistor array panel for a liquid crystal display including a pixel electrode.

[0004] (b) Description of the Related Art

[0005] A liquid crystal display ("LCD") is one of the most widely used flat panel displays. An LCD includes two panels having field-generating electrodes and a liquid crystal layer interposed therebetween and controls the transmittance of light passing through the liquid crystal layer fly realigning liquid crystal molecules in the liquid crystal layer with voltages applied to the electrodes.

[0006] One of the most commonly used LCDs provides a plurality of planar field-generating electrodes on one panel with switching elements switching the voltages applied to the electrodes and one large planar field-generating electrode on the other panel, which is applied with a fixed voltage or two swinging voltages. Thin film transistors ("TFTs") are usually used as the switching elements, and the panel including the TFTs is called the "TFT array panel."

[0007] The planar field-generating electrodes provided on respective panels generate electric field perpendicular to the panels. Some of the electric field lose that perpendicularity near the edges of the electrodes.

[0008] A typical LCD further includes an alignment layer for determining initial alignments of the liquid crystal molecules. One type of the alignment layer forces the director of the liquid crystal material to be parallel to the surface of the alignment layer (which is called homogeneous alignment), while another type forces the director to be normal to the surface (which is called hemeotropic alignment). A proper surface treatment of the alignment layer such as rubbing and light exposure controls the tilt directions of the liquid crystal molecules. For example, the rubbing in a direction enforces the major axes of the liquid crystal molecules to tilt in that direction.

[0009] The combination of the irregularity of the electric field near the edges of the field-generating electrodes and the compulsive alignment of the liquid crystal molecules using the surface treatment of the alignment layer may result in loss of control for the liquid crystal molecules. This effect is called disclination, which causes light leakage.

SUMMARY OF THE INVENTION

[0010] A thin film transistor array panel for a liquid crystal display is provided, which includes: a substrate; a plurality of signal lines provided on the substrate and including a gate line and a data line insulated from each other; a switching element electrically connected to the gate line and the data line; a pixel electrode electrically connected to the switching element and overlapping at least one of the signal lines via an insulator to form at least one overlapping area; and a rubbed alignment layer covering the pixel electrode, wherein at least one portion of the at least one overlapping area near a starting position of rubbing of the alignment layer is wider than other portions of the at least one overlapping area.

[0011] According to an embodiment of the present invention, the pixel electrode has an expansion forming the at least one portion of the at least one overlapping area.

[0012] According to another embodiment of the present invention, the pixel electrode has a plurality of major edges, and at least one of the major edges proceeds into the at least one of the gate line and the data line more deeply than other major edges to form the at least one portion of the at least one overlapping area.

[0013] The switching element preferably includes a semiconductor layer electrically connected to the gate line and the pixel electrode, and the semiconductor layer extends along the data line. The switching element further includes an ohmic contact interposed between the semiconductor layer and the data line.

[0014] According to an embodiment of the present invention, the thin film transistor array panel further includes: a storage electrode separated from the signal lines; id a storage conductor electrically connected to the pixel electrode and overlapping the storage electrode via an insulating layer. The storage conductor is directly connected to the thin film transistor.

[0015] It is preferable that the pixel electrode is located on the insulator, and the thin film transistor is located under the insulator.

[0016] Another thin film transistor array panel for a liquid crystal display is provided, which includes: a substrate; a plurality of signal lines provided on the substrate and including a gate line and a data line; a gate insulating layer interposed between the gate line and the data line; a switching element electrically connected to the gate line and the data line; a pixel electrode electrically connected to the switching element; and a passivation layer interposed between the pixel electrode and the data line and between the pixel electrode and the gate line, wherein the pixel electrode overlaps at least one of the signal lines to form at least one overlapping area and includes an expansion providing larger width of a portion of the at least one overlapping area than other portions of the at least one overlapping area.

[0017] The at least one of the signal lines preferably includes the gate line.

[0018] According to an embodiment of the present invention, the pixel electrode has substantially a rectangular shape with four major edges including first two major edges substantially parallel to the gate line and second two major edges substantially parallel to the data line, and a portion of the first two major edges form the expansion.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

[0020] FIG. **1** is a layout view of an exemplary TFT array panel for an LCD according to an embodiment of the present invention;

[0021] FIG. **2** is a sectional view of the TFT array panel shown in FIG. **1** taken along the line II-II';

[0022] FIG. **3** is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention; and

[0023] FIGS. **4** and **5** are sectional views of the TFT array panel shown in FIG. **3** taken along the lines IV-IV' and V-V', respectively.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0024] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown.

[0025] In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly f-n the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements, present.

[0026] FIG. **1** is a layout view of an exemplary TFT array panel according to an embodiment of the present invention, and FIG. **2** is a sectional view of an exemplary LCD including the TFT array panel shown in FIG. **1** taken along the line II-II'.

[0027] As shown in FIG. **2**, an LCD according to an embodiment of the present invention includes a lower panel ("TFT array panel") **100**, an upper panel ("color filter panel") **200** and a liquid crystal layer **3** interposed therebetween.

[0028] The color filter panel **200** includes an insulating substrate **210**, a black matrix **220**, a plurality of color filters **230** and a reference electrode **270** formed in sequence. In addition, an alignment layer **21** is provided on the reference electrode **270**.

[0029] As shown in FIGS. **1** and **2**, the TFT array panel **100** includes a plurality of gate lines **121** and a plurality of storage electrode lines **131** extending substantially in a transverse direction formed on an insulating substrate **110**. The gate lines **121** and the storage electrode lines **131** include either a single layer preferably made of material with low resistivity such as silver, silver alloy, aluminum and aluminum alloy, or multiple layers including such a single layer and a layer preferably made of material with good physical and electrical contact characteristics, such as Cr, Ti and Ta. A plurality of branches of each gate line **121** form gate electrodes **124** of TFT's, and portions of storage electrode lines **131** expand upward and downward to form storage electrodes **133**. A predetermined voltage such as a reference voltage or a common electrode voltage (referred to as "a common voltage" hereinafter) is applied to the storage electrode lines **131** from an external source. The common voltage is also applied to the reference electrode **270** of the color filter panel **200**.

[0030] The gate lines **121** and the storage electrode lines **131** are covered by a gate insulating layer **140** preferably made of silicon nitride.

[0031] A plurality of semiconductor islands **154** preferably made of polysilicon or hydrogenated amorphous silicon are formed on the gate insulating layer **140** opposite the gate electrodes **124**, and a plurality of pairs of ohmic contacts **163** and **165** preferably made of silicide or n+ hydrogenated amorphous silicon heavily doped with n type impurity are formed on the semiconductor islands **154**. One of each pair of ohmic contacts **163** and **165** is separated from and disposed opposite to the other of the pair with respect to a corresponding one of the gate electrodes **124**.

[0032] A plurality of data lines **171** and a plurality of drain electrodes **175** of the TFTs are formed on the ohmic contacts **163** and **165** and the gate insulating layer **140**. The data lines **171** and the drain electrodes **175** preferably include Cr, Mo, Mo alloy, Al, Al alloy, Ta and Ti, and may have a double-layered structure including a low-resistivity metal layer and a good-contact metal layer exhibiting good contact characteristic with another material such as, IZO (indium zinc oxide). Examples of the double-layered structure are an Al (or Al alloy) layer End a Cr layer; and an Al (or Al alloy) layer and a Mo (or Mo alloy) layer.

[0033] The data lines **171** extend substantially in a longitudinal direction an intersect the gate lines **121**, and a plurality of branches of each data line **171** form source electrodes **173** of the TFTs. Each source electrode extending to one **163** of the corresponding pair of the ohmic contacts **163** and **165** is separated from and opposite the corresponding one of the drain electrodes **175**, which is located at least in part on the other **165** of the pair of the ohmic contacts **163** and **165** with respect to corresponding one of the gate electrodes **124**. The drain electrodes **175** extend onto the storage electrodes **133** to overlap.

[0034] The ohmic contacts **163** and **165** interposed between the semiconductor islands **154** and the data lines **171** and the drain electrodes **175** reduce the contact resistance therebetween.

[0035] A passivation layer **180** preferably made of silicon nitride, silicon oxide, low-permittivity insulating material such as SiO:C and SiO:F obtained by chemical vapor deposition or low-permittivity organic insulating material is formed on the data lines **171** and portions of the semiconductor islands **154**, which are not covered by the data lines **171** and the drain electrodes **175**.

[0036] The passivation layer **180** has a plurality of contact holes **182** and **183** exposing end portions **179** of the data lines **171** and the drain electrodes **175**, and the passivation layer **180** and the gate insulating layer **140** has a plurality of contact holes **181** exposing end portions **129** of the gate lines

121. Contact holes 181 and 182 are provided for electrical connection between the signal lines 121 and 171 and respective driving circuits therefor.

[0037] A plurality of pixel electrodes 190 preferably made of transparent conductive material such as indium zinc oxide ("IZO") and indium tin oxide ("ITO") are formed on the passivation layer 180. Each pixel electrode 190 is electrically connected to respective one of the drain electrodes 175 through the corresponding contact hole 183.

[0038] Each pixel electrode 190 applied with voltages from the data lines 171 generate electric fields in cooperation with a corresponding reference electrode provided on the other panel, and the variation of the applied voltage changes the orientations of liquid crystal molecules in a liquid crystal layer between the two field-generating electrodes, the pixel electrode 190 and the reference electrode. In view of electrical circuits, each pair of the pixel electrode 190 and the reference electrode form a capacitor with liquid crystal dielectric far storing electrical charges. The storage capacitance due to the overlap of the drain electrodes 175 and the storage electrodes 133 enhances the charge storing capacity of the liquid crystal capacitors.

[0039] Furthermore, a plurality of contact assistants 91 and 92 preferably made of the same material as the pixel electrodes 190 are formed on the passivation layer 180. The contact assistants 91 and 92 are connected to the exposed end portions 129 and 179 of the gate and the data lines 121 and 171 through the contact holes 181 and 182, respectively. One skilled in the art can readily appreciate that the contact assistants 91 and 92 are not required but are preferred elements used to protect the exposed portions 129 and 179 of the gate and the data lines 121 and 171, respectively, and to complement the adhesiveness of the TFT array panel and the driving circuits.

[0040] An alignment layer 11 is formed on the TFT array panel 100. As indicated by an arrow in FIG. 1, the alignment layer 21 is rubbed obliquely, preferably, about a direction from the upper left corner to the lower right corner of the TFT array panel 100 or the pixel electrodes 190.

[0041] As shown in FIG. 1, the pixel electrodes 190 overlap the gate lines 121 and the data lines 171 to increase aperture ratio, and it is preferably adapted for low-permittivity passivation. The pixel electrode 190 is substantially rectangular in shape with two major edges substantially parallel to the gate lines 121 and the other two edges substantially parallel to the data lines 171. The upper one of the two gate-parallel edges has an expansion 191 located near the upper left corner of the pixel electrode 190 to increase the width of the corresponding overlapping area between the pixel electrode 190 and the gate line 121 and/or the data line 171. In addition, the left one of the two data-parallel edges of the pixel electrode proceeds into the data line 171 more deeply than the right one to increase the width of the left overlapping area.

[0042] The orientation of the liquid crystal molecules in the liquid crystal layer 3 near the rubbing-starting corner of the pixel electrode 190 is distorted since the tilt direction of the liquid crystal molecules due to the rubbing makes a large angle with the field direction of the fringe field due to the discontinuity of the pixel electrode 190. Since the overlapping area between the pixel electrode 190 and the signal lines 121 and 171 is light-blocked by the signal lines 121 and 171, the increased overlapping area near the rubbing-starting corner means that the distorted area (or the disclination area) is sufficiently blocked by the signal lines 121 and 171.

[0043] A TFT array panel for an LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. 3-5.

[0044] FIG. 3 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention, and FIGS. 4 and 5 are sectional views of the TFT array panel shown in FIG. 3 taken along the lines IV-VI' and V-V', respective y.

[0045] As shown in FIGS. 3-5, a TFT array panel of an LCD according to this embodiment is almost the same as that of an LCD shown in FIGS. 1 and 2.

[0046] Different from the TFT array panel shown in FIGS. 1 and 2, a plurality of pixel electrodes 190 have no expansion for increasing the corresponding overlapping area. Instead, the upper one of two gate-parallel edges of the pixel electrode 190 proceeds in to the gate line 121 more deeply than the lower one to increase the width of the upper overlapping area.

[0047] Furthermore, a plurality of storage conductors 177 overlapping a plurality of storage electrode lines 131 are spaced apart from a plurality of drain electrodes 175. A plurality of contact holes 184 for exposing the storage conductors 177 are also provided to electrically connect the storage conductors 177 to the appropriate pixel electrodes 190.

[0048] In addition, a plurality of gate electrodes 124 of TFTs are parts of respective gate lines 121 rather than their branches.

[0049] Furthermore, there are provided a plurality of semiconductor stripes and islands 151 and 157 under respective plurality of data lines 171, a plurality of drain electrodes 175 and the storage conductors 177. Each semiconductor stripe 151 extends onto the gate electrodes 124 along a plurality of source electrodes 173 and a plurality of drain electrodes 175 to form channels of the TFTs. A plurality of ohmic contacts 161, 165 and 167 are provided between the semiconductor stripes and islands 151 and 157 and the data lines 171, the drain electrodes 175 and the storage conductors 177.

[0050] The semiconductor stripes 151 have similar planar shapes as the data lines 171 and the drain electrodes 175 except for channels of the TFTs. For example, although the data lines 171 are disconnected from the drain electrodes 175 on the channels of the TFTs, the semiconductor stripes 151 run continuously to form channels of the TFTs. The semiconductor islands 157 have similar planar shapes as the storage conductors 177. The ohmic contacts 161, 165 and 167 have similar planar shapes as the data lines 171, the drain electrodes 175 and the storage conductors 177.

[0051] While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

What is claimed is:

1. A thin film transistor array panel for a liquid crystal display, comprising:

a substrate;

a plurality of signal lines provided on the substrate and including a gate line and a data line;

a gate insulating layer interposed between the gate line and the data line;

a switching element electrically connected to the gate line and the data line;

a pixel electrode electrically connected to the switching element; and

a passivation layer interposed between the pixel electrode and the data line and between the pixel electrode and the gate line, wherein the pixel electrode overlaps at least one of the signal lines to form at least one overlapping area and includes an expansion providing larger width of a portion of the at least one overlapping area than other portions of the at least one overlapping area

2. The thin film transistor array panel of claim 1, wherein the at least one of the signal lines includes the gate line.

3. The thin film transistor array panel of claim 1, wherein the pixel electrode has substantially a rectangular shape with four major edges including first two major edges substantially parallel to the gate line and second two major edges substantially parallel to the data line, and a portion of the first two major edges form the expansion.

4. The thin film transistor array panel of claim 1, wherein the switching element comprises a semiconductor layer electrically connected to the gate line and the pixel electrode, and the semiconductor layer extends along the data line.

5. The thin film transistor array panel of claim 4, wherein the switching element further comprises an ohmic contact interposed between the semiconductor layer and the data line.

6. The thin film transistor array panel of claim 1, further comprising:

a storage electrode separated from the signal lines; and

a storage conductor electrically connected to the pixel electrode and located opposite the storage electrode with respect to the gate insulating layer to overlap the storage electrode.

7. The thin film transistor array panel of claim 6, wherein the storage conductor is directly connected to the thin film transistor.

8. The thin film transistor array panel of claim 1, wherein the pixel electrode is located on the passivation layer and the thin film transistor is located under the passivation layer.

9. The thin film transistor array panel of claim 1, further comprising a plurality of storage electrodes provided on the substrate, wherein the plurality of storage electrodes are commonly connected to each other and overlap the pixel electrode for forming a storage capacitance with the pixel electrode.

10. The thin film transistor array panel of claim 9, further comprising:

at least one drain electrode overlapping at least one storage electrode of the plurality of storage electrodes, wherein the passivation layer is formed over the at least one drain electrode and under the pixel electrode, the passivation layer including at least one contact hole for exposing a portion of the at least one drain electrode, wherein the pixel electrode is electrically connected to the at least one drain electrode through the at least one contact hole.

11. The thin film transistor array panel of claim 1, further comprising:

a plurality of storage electrode lines formed on the substrate; and

a plurality of storage conductors overlapping the plurality of storage electrode lines, wherein the passivation layer is formed over at least one storage conductor of the plurality of storage conductors and under the pixel electrode, the passivation layer including at least one contact hole for exposing a portion of the at least one storage conductor, wherein the pixel electrode is electrically connected to the at least one storage conductor through the at least one contact hole.

12. The thin film transistor array panel of claim 11, wherein the plurality of storage electrodes extend from the plurality of storage electrode lines.

13. The thin film transistor array panel of claim 11, further comprising an ohmic contact formed between the at least one storage conductor and at least one storage electrode line.

14. The thin film transistor array panel of claim 11, further comprising a semiconductor island formed between the at least one storage conductor and at least one storage electrode line.

15. The thin film transistor array panel of claim 1, further comprising:

a storage electrode separated from the signal lines; and

a storage conductor electrically connected to the pixel electrode and overlapping the storage electrode via the gate insulating layer.

16. The thin film transistor array panel of claim 15, wherein the storage conductor is directly connected to the thin film transistor.

* * * * *

专利名称(译)	用于液晶显示器的薄膜晶体管阵列面板，具有像素电极		
公开(公告)号	US20070046569A1	公开(公告)日	2007-03-01
申请号	US11/551450	申请日	2006-10-20
[标]申请(专利权)人(译)	金东GYU 香港香植 KIM JANG SOO		
申请(专利权)人(译)	金东GYU 香港香植 金章洙		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	KIM DONG GYU KONG HYANG SHIK KIM JANG SOO		
发明人	KIM, DONG-GYU KONG, HYANG-SHIK KIM, JANG-SOO		
IPC分类号	G09G3/04 G02F1/136 G02F1/1337 G02F1/1343 G02F1/1362		
CPC分类号	G02F1/1337 G02F1/133784 G02F2201/123 G02F1/136213 G02F1/136227 G02F1/134336		
优先权	1020020031098 2002-06-03 KR		
其他公开文献	US7289171		
外部链接	Espacenet USPTO		

摘要(译)

TFT阵列面板包括绝缘基板，栅极线和形成在其上的存储电极线。栅极线和存储电极线覆盖有栅极绝缘层，并且半导体岛形成在栅极绝缘层上。在半导体岛上形成一对欧姆接触，并在其上形成数据线和漏电极。数据线和漏电极覆盖有钝化层，该钝化层具有暴露漏电极的接触孔。像素电极形成在钝化层上并通过接触孔连接到漏电极。 TFT阵列面板覆盖有大致在TFT阵列面板的左上角到右下角或像素电极的方向上摩擦的对准层。像素电极具有近似矩形的形状并且与栅极线和数据线重叠。像素电极具有位于像素电极的左上角附近的扩展，以增加像素电极与栅极线和/或数据线之间的对应重叠区域的宽度。