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(54) **THIN FILM TRANSISTOR ARRAY PANEL
AND LIQUID CRYSTAL DISPLAY
INCLUDING THE SAME**

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(57) **ABSTRACT**

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A liquid crystal display is provided, which includes a plurality of pixels including first and second thin film transistors, and a pixel electrode connected to the first and second thin film transistors, a first gate line transmitting a first gate signal and connected to the first thin film transistor, a second gate line transmitting a second gate signal and connected to the second thin film transistor, and a data line transmitting a data signal and connected to the first thin film transistor. The second thin film transistor receives a uniform voltage and transmits the uniform voltage to the pixel electrode according to the second gate signal.

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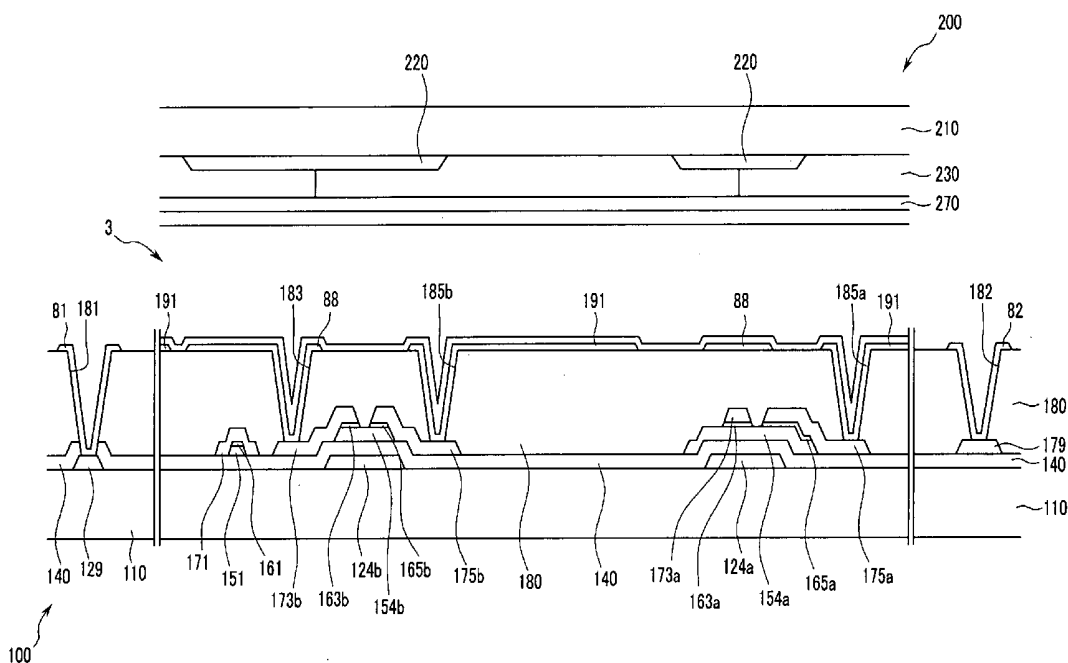


FIG. 1

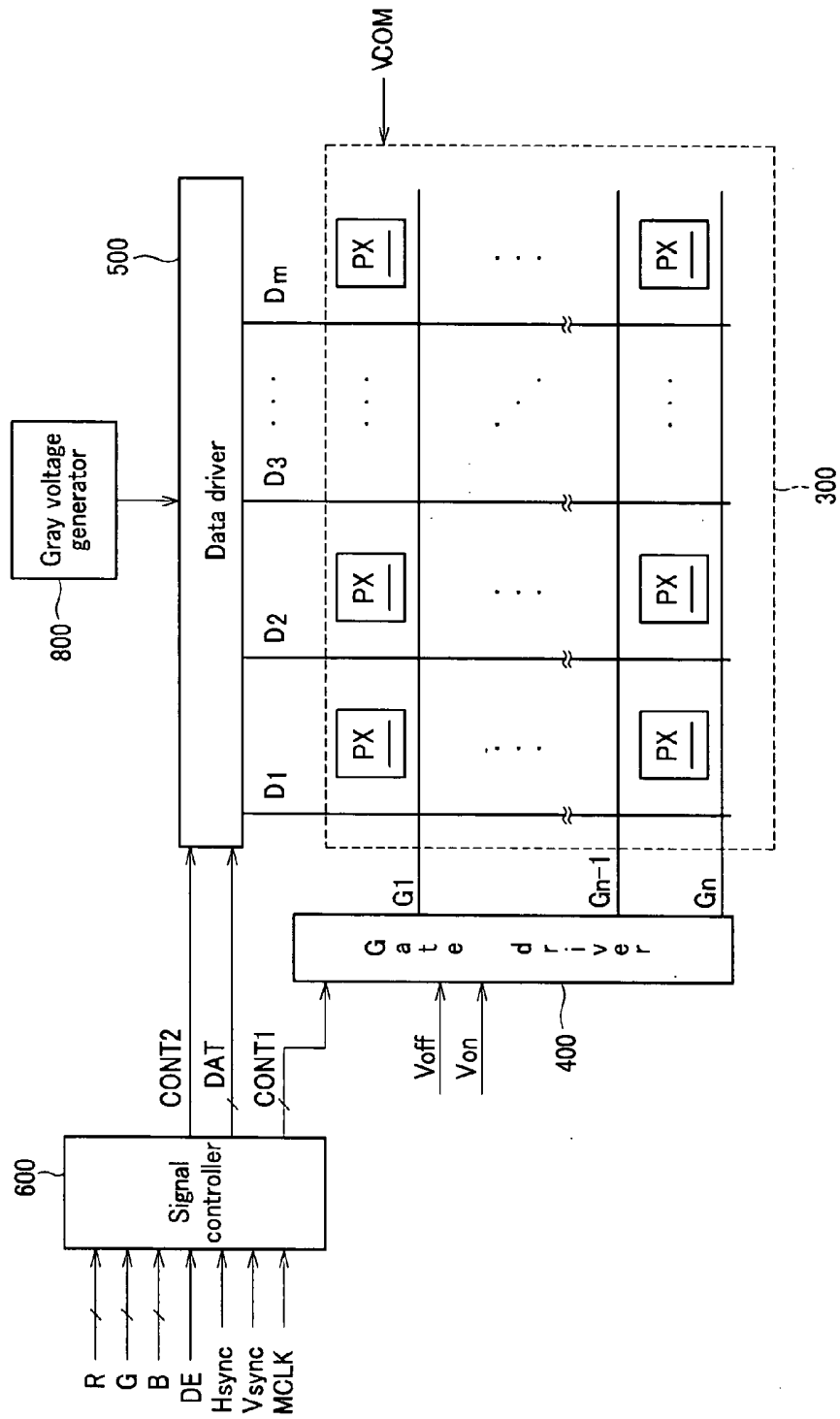


FIG.2

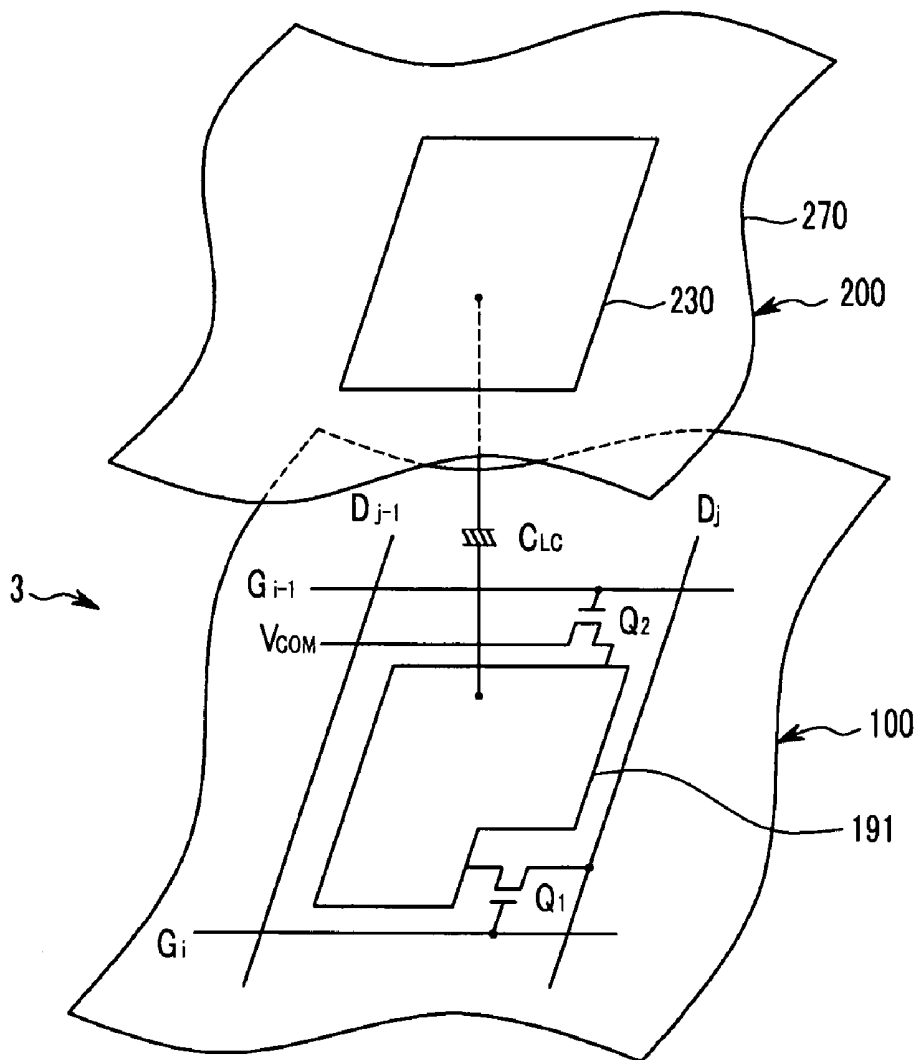


FIG.3

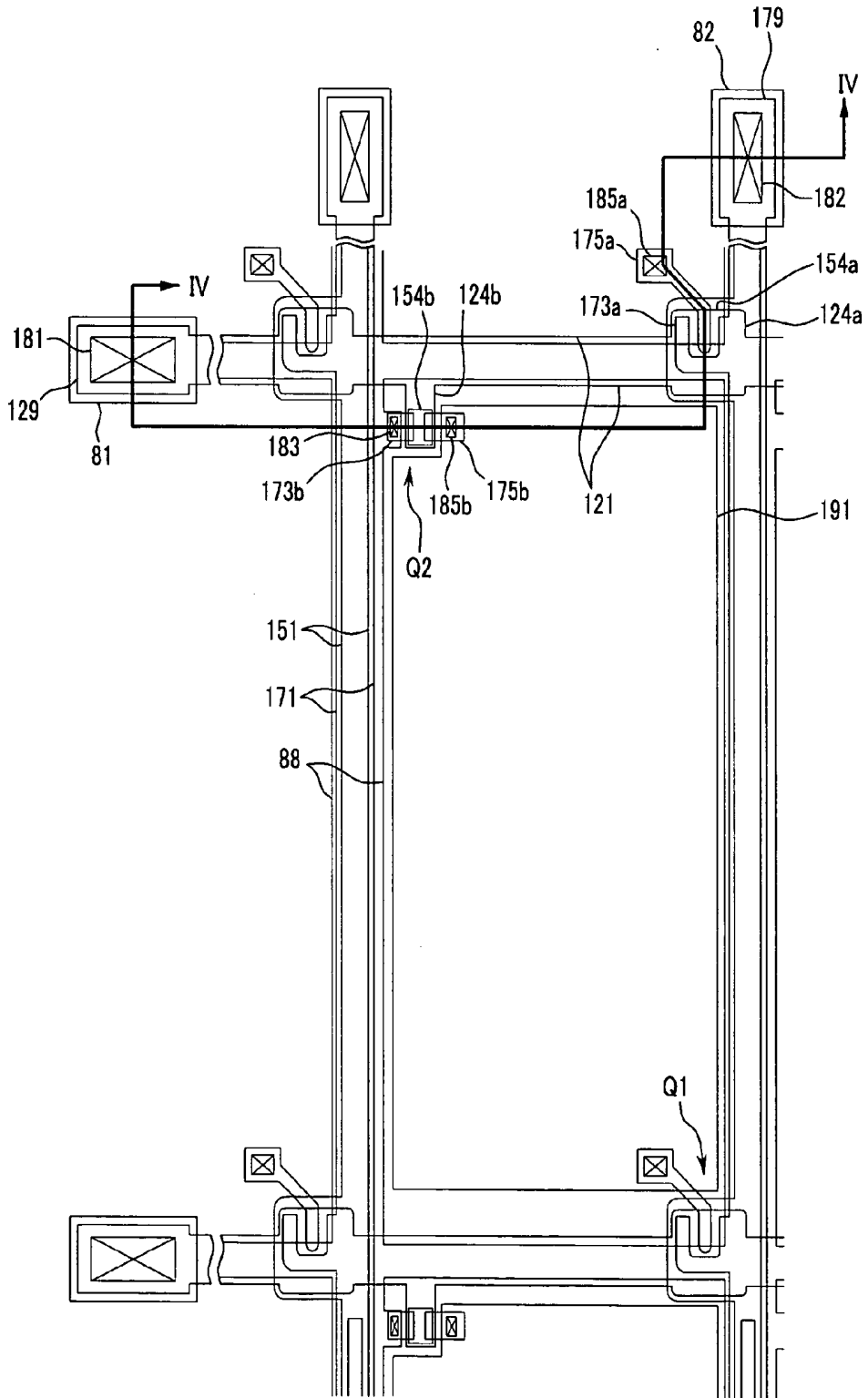


FIG.5

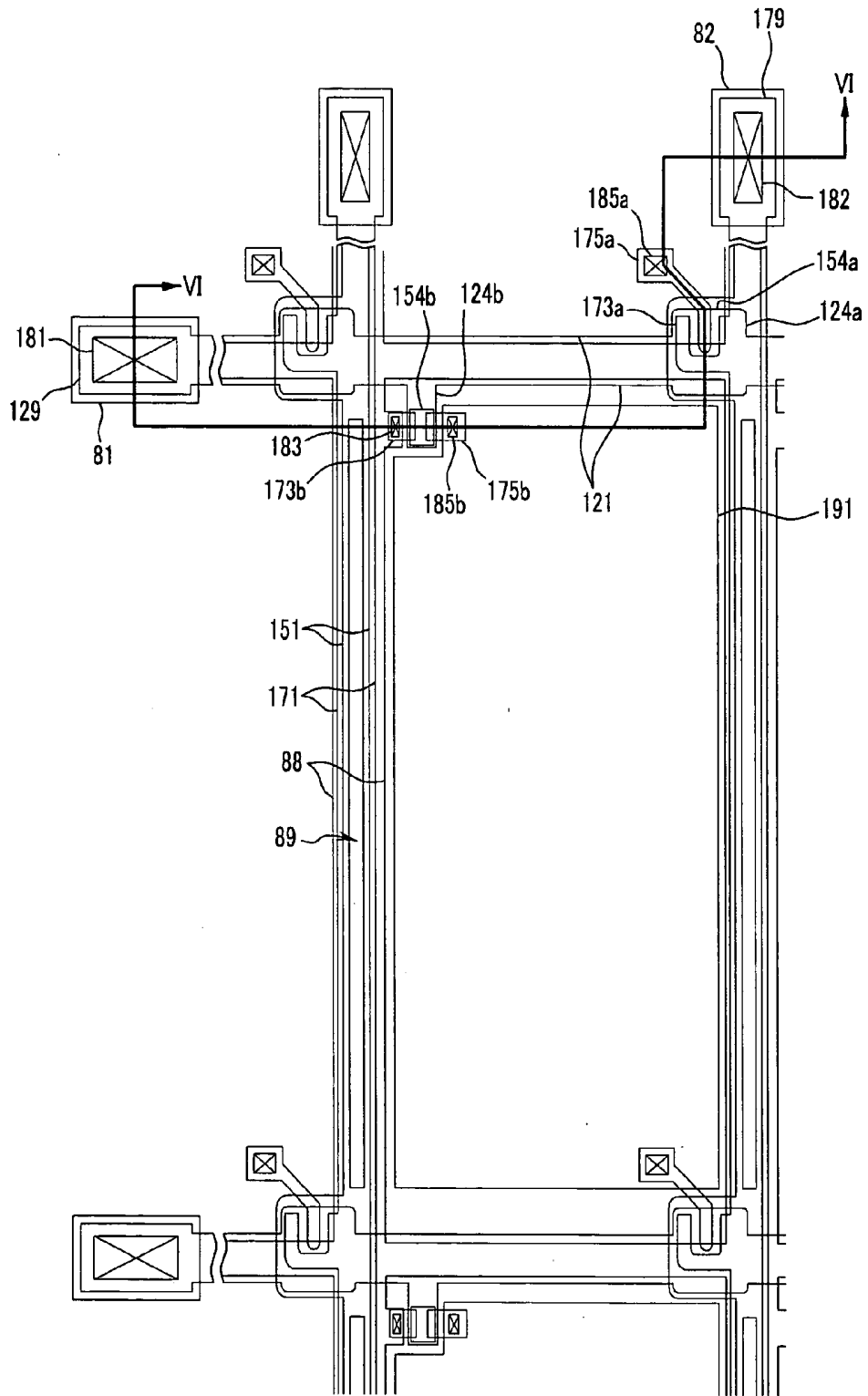


FIG. 7

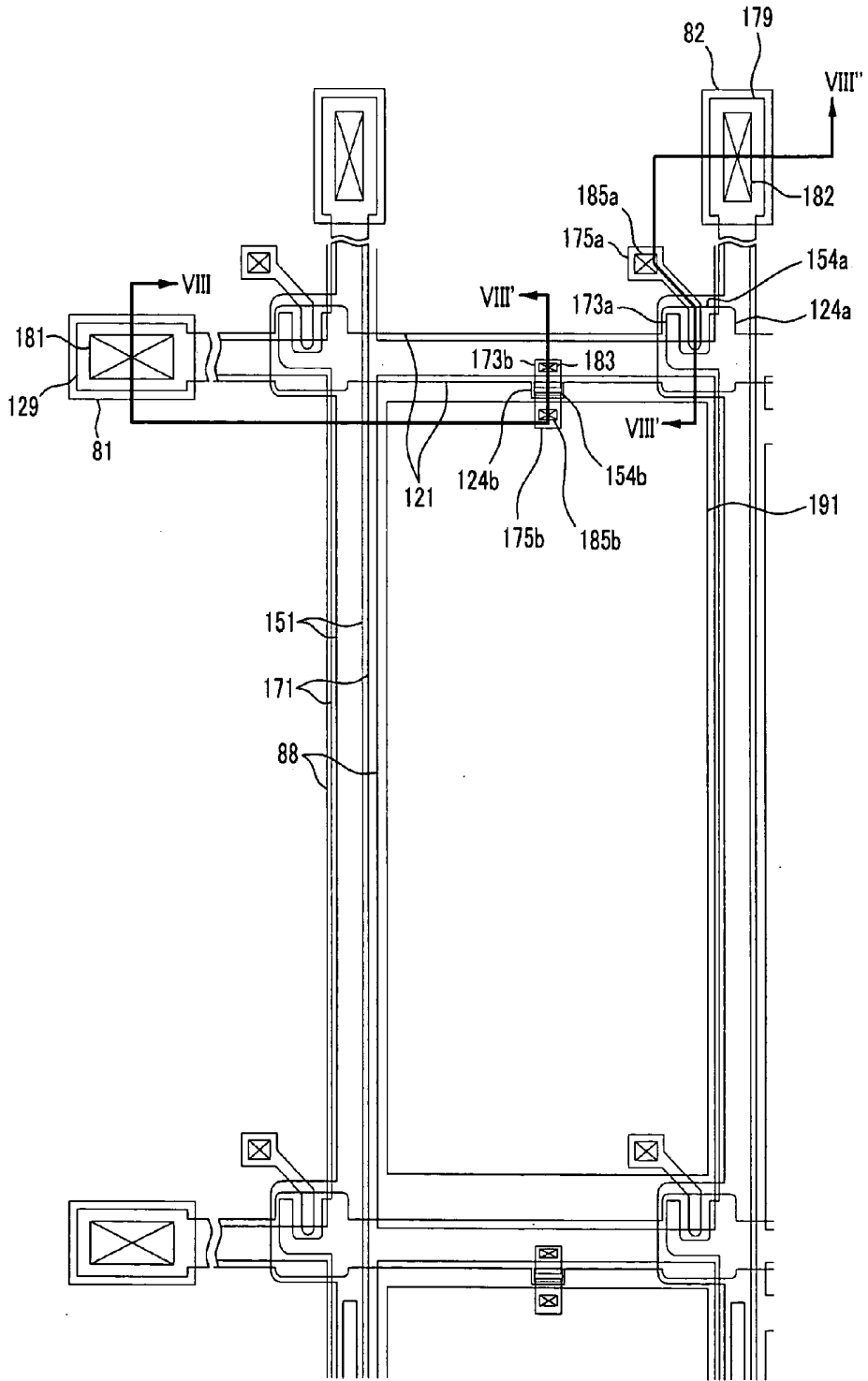


FIG. 8

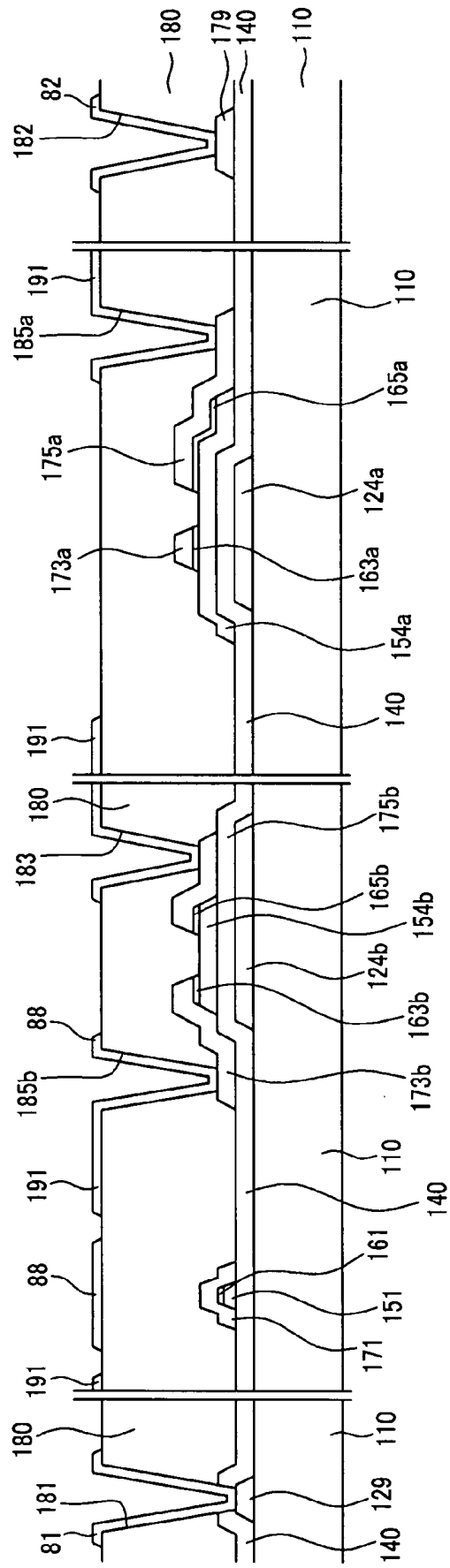


FIG. 9

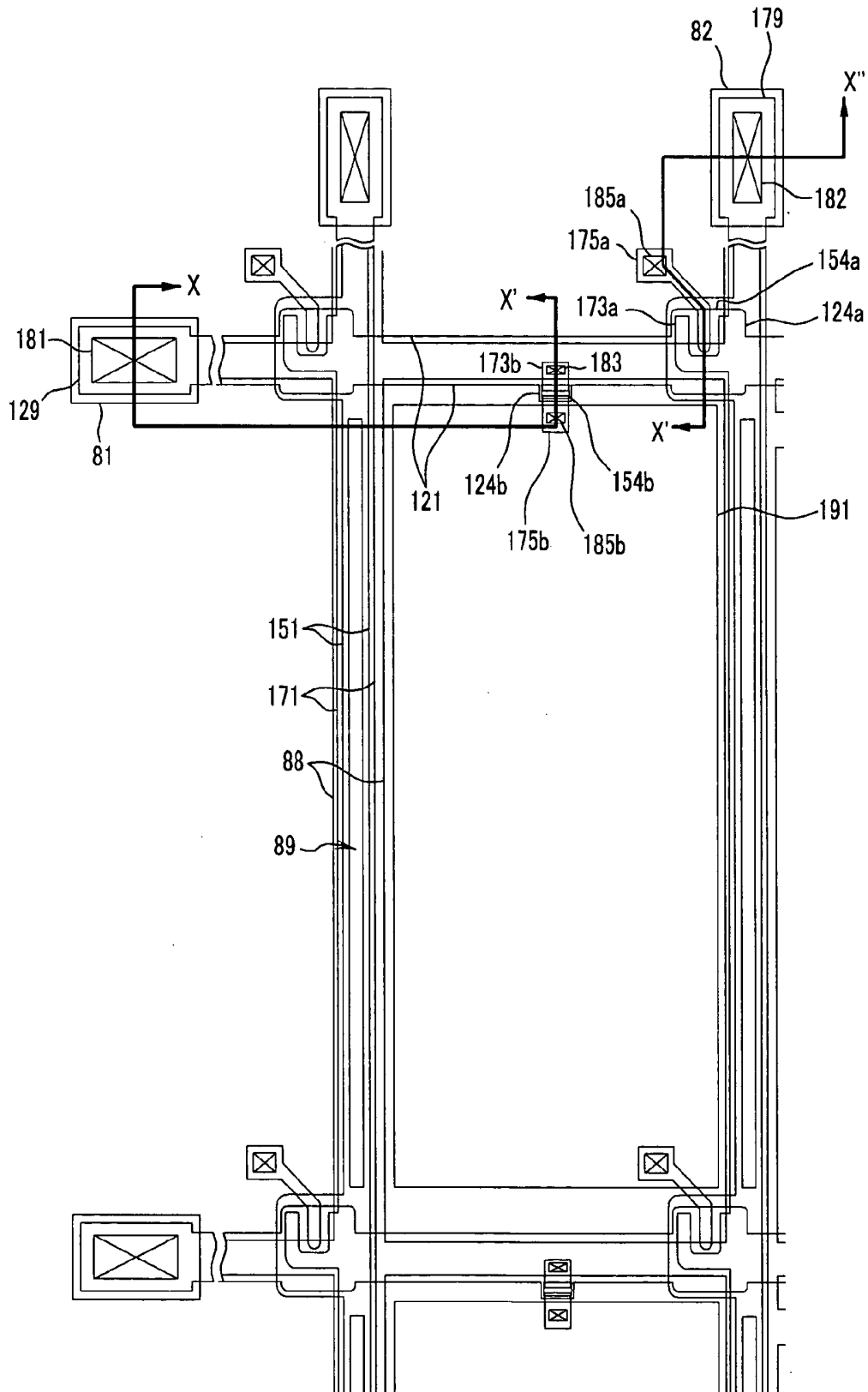


FIG. 10

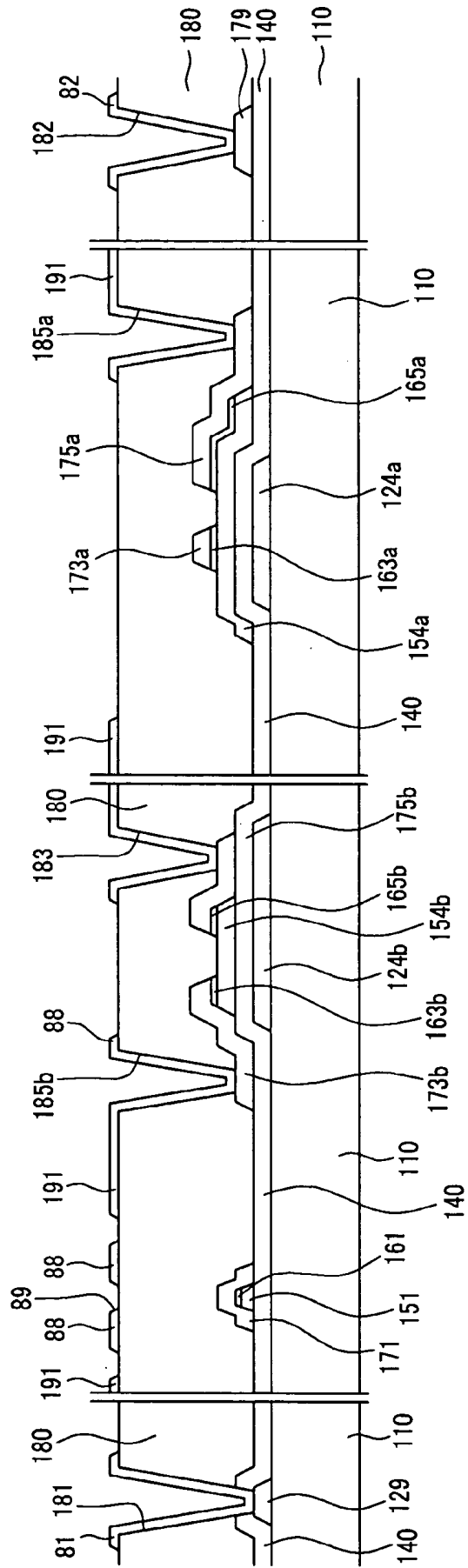


FIG. 11

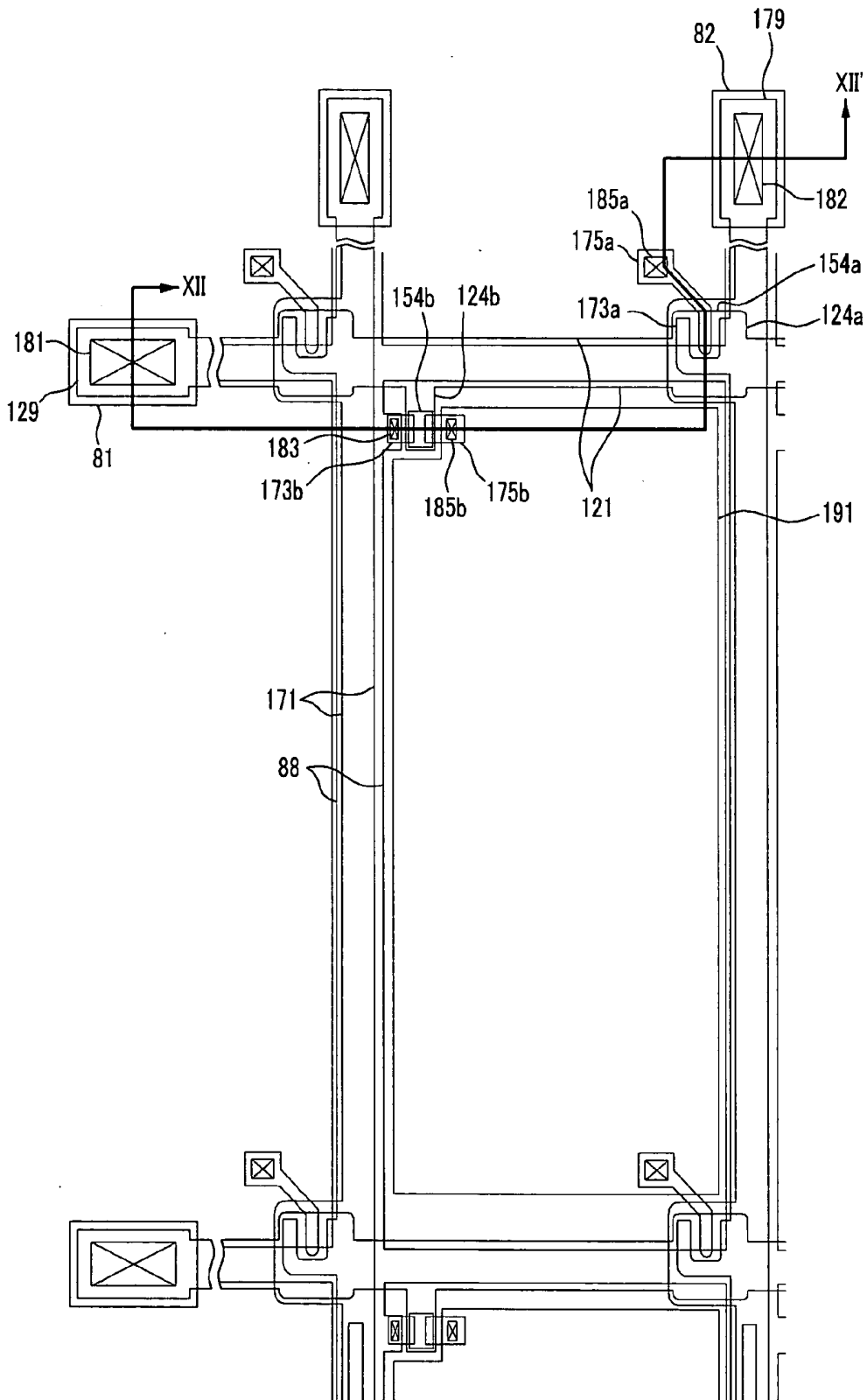
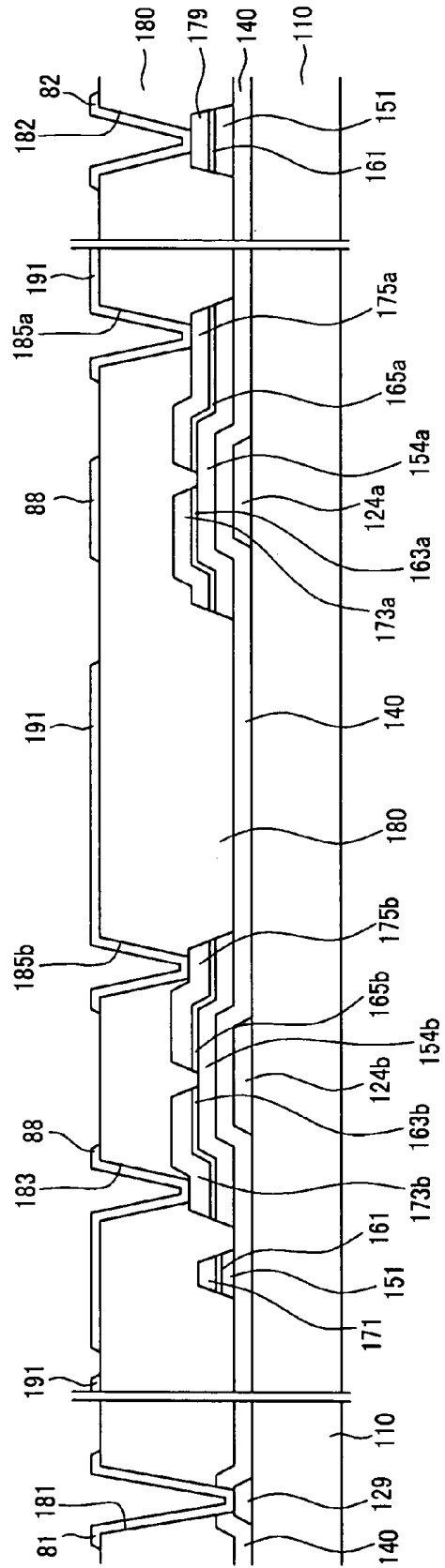


FIG. 12



**THIN FILM TRANSISTOR ARRAY PANEL AND
LIQUID CRYSTAL DISPLAY INCLUDING THE
SAME**

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to a thin film transistor array panel and a liquid crystal display including the same.

[0003] (b) Description of Related Art

[0004] Liquid crystal displays (LCDs) are widely used flat panel displays. An LCD includes two panels comprising field-generating electrodes, with a liquid crystal (LC) layer interposed between the two panels.

[0005] The LCD displays images by applying voltages to the field-generating electrodes to generate an electric field in the LC layer. The electric field determines orientations of LC molecules in the LC layer to adjust polarization of incident light.

[0006] LCDs may include field-generating electrodes on the respective panels. A type of LCD including field-generating electrodes on respective panels includes a plurality of pixel electrodes arranged in a matrix at one panel and a common electrode on the other panel. The common electrode covers an entire surface of the panel. The image display of the LCD is accomplished by applying individual voltages to respective pixel electrodes.

[0007] The common electrode, the pixel electrode, and the LC layer form a liquid crystal capacitor, and each pixel includes a switching element connected to the liquid crystal capacitor as well as the liquid crystal capacitor.

[0008] Currently, the driving speed of the LCD is being increased to improve the image quality of moving pictures, but it is difficult to charge the liquid crystal capacitor sufficiently when the speed is significantly increased. Therefore, the previous data voltage is pre-charged in the liquid crystal capacitor before it receives its data voltage.

[0009] However, the pre-charging generates a shadow phenomenon because the amounts of the pre-capacitance of each pixel are changed depending on the previous data voltage.

SUMMARY OF THE INVENTION

[0010] A liquid crystal display is provided, which includes a plurality of pixels including first and second thin film transistors and a pixel electrode connected to the first and second thin film transistors, a first gate line transmitting a first gate signal and connected to the first thin film transistor, a second gate line transmitting a second gate signal and connected to the second thin film transistor, and a data line transmitting a data signal and connected to the first thin film transistor, wherein the second thin film transistor receives a uniform voltage and transmits the uniform voltage to the pixel electrode according to the second gate signal.

[0011] The second thin film transistor may be turned on more quickly than the first thin film transistor.

[0012] The liquid crystal display may further include a common electrode facing the pixel electrode, and a liquid crystal layer formed between the common electrode and the pixel electrode.

[0013] The uniform voltage is the voltage supplied to the common electrode.

[0014] A thin film transistor array panel is provided, which includes a gate line formed on an insulating substrate, a data line intersecting the gate line, a shielding electrode formed on the data line, a first thin film transistor connected to the gate line and the data line, a second thin film transistor connected to the gate line and the shielding electrode, a pixel electrode connected to the first and second thin film transistors, and a passivation layer formed between the shielding electrode and the pixel electrode, and the data line.

[0015] The shielding electrode may have an opening extended along the data line.

[0016] The first thin film transistor may include a first gate electrode connected to the gate line, a first semiconductor overlapping the first gate electrode, a first source electrode connected to the data line and overlapping the first semiconductor, and a first drain electrode overlapping the first semiconductor and connected to the pixel electrode.

[0017] The second thin film transistor may include a second gate electrode connected to the gate line, a second semiconductor overlapping the second gate electrode, a second source electrode connected to the shielding electrode and overlapping the second semiconductor, and a second drain electrode overlapping the second semiconductor and connected to the pixel electrode.

[0018] The shielding electrode may include a protrusion extended to the second semiconductor, wherein the second source electrode is connected to the protrusion.

[0019] The shielding electrode may have a connection connecting the adjacent shielding electrode to each other, and it at least overlaps the gate line.

[0020] The second source electrode may be disposed on the gate line and be connected to the connection on the gate line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The present invention will become more apparent by describing preferred embodiments thereof in detail with reference to the accompanying drawings in which:

[0022] **FIG. 1** is a block diagram of a display device according to an embodiment of the present invention;

[0023] **FIG. 2** is an equivalent circuit diagram of a pixel of an LCD as an example of the display device according to an embodiment of the present invention;

[0024] **FIG. 3** is a layout view of a lower panel for an LCD according to an embodiment of the present invention;

[0025] **FIG. 4** is a sectional view of the LCD including an upper panel shown in **FIG. 3** taken along the line IV-IV;

[0026] **FIG. 5** is a layout view of a thin film transistor array panel for an LCD according to another embodiment of the present invention;

[0027] **FIG. 6** is a sectional view of the thin film transistor array panel shown in **FIG. 5** taken along the line VI-VI;

[0028] **FIG. 7** is a layout view of a thin film transistor array panel for an LCD according to another embodiment of the present invention;

[0029] FIG. 8 is a sectional view of the thin film transistor array panel shown in FIG. 7 taken along the line VIII-VIII;

[0030] FIG. 9 is a layout view of a thin film transistor array panel for an LCD according to another embodiment of the present invention;

[0031] FIG. 10 is a sectional view of the thin film transistor array panel shown in FIG. 9 taken along the lines X-X'-X'';

[0032] FIG. 11 is a layout view of a thin film transistor array panel for an LCD according to another embodiment of the present invention; and

[0033] FIG. 12 is a sectional view of the thin film transistor array panel shown in FIG. 11 taken along the lines XII-XII.

DETAILED DESCRIPTION OF EMBODIMENTS

[0034] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

[0035] In the drawings, the thickness of layers, films, and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0036] Referring to FIGS. 1 and 2, a liquid crystal display according to an embodiment of the present invention will be described in detail.

[0037] FIG. 1 is a block diagram of a display device according to an embodiment of the present invention, and FIG. 2 is an equivalent circuit diagram of a pixel of an LCD as an example of the display device according to an embodiment of the present invention.

[0038] Referring to FIG. 1, a display device according to the present embodiment includes a liquid crystal panel assembly 300, a gate driver 400 and a data driver 500 that are connected to the liquid crystal panel assembly 300, a gray voltage generator 800 connected to the data driver 500, and a signal controller 600 controlling the above elements.

[0039] Referring to FIG. 1, the liquid crystal panel assembly 300 includes a plurality of display signal lines G1-Gn and D1-Dm, and a plurality of pixels PX connected thereto. The pixels PX are arranged substantially in a matrix.

[0040] In the structural view shown in FIG. 2, the liquid crystal panel assembly 300 includes a lower panel 100, an upper panel 200, and an LC layer 3 interposed therebetween.

[0041] The display signal lines G1-Gn and D1-Dm include a plurality of gate lines G1-Gn transmitting gate signals (also referred to as "scanning signals") and a plurality of data lines D1-Dm transmitting data signals. The gate lines G1-Gn extend substantially in a row direction and are substantially parallel to each other, while the data lines

D1-Dm extend substantially in a column direction and are substantially parallel to each other.

[0042] Referring to FIG. 2, each pixel PX defined by the 'i'th gate line and the 'j'th data line of a liquid crystal display includes a main switching element Q1 and a sub switching element Q2, which are connected to the signal lines Gi and Dj, and an LC (liquid crystal) capacitor C_{LC}. The display signal lines Gi and Dj are provided on the lower panel 100. If necessary, the storage capacitor (not shown) may be added.

[0043] Each of the main and sub switching elements Q1 and Q2 such as a TFT is provided on the lower panel 100, and the main switching element Q1 has three terminals: a control terminal connected to the gate line Gi; an input terminal connected to the data line Dj; and an output terminal connected to the LC capacitor C_{LC}. The sub switching element Q2 has three terminals: a control terminal connected to the previous gate line Gi-1; an input terminal connected to the common voltage Vcom; and an output terminal connected to the LC capacitor C_{LC}.

[0044] The LC capacitor C_{LC} includes a pixel electrode 191 provided on the lower panel 100 and a common electrode 270 provided on the upper panel 200, as the two capacitor terminals. The LC layer 3 disposed between the two electrodes 191 and 270 functions as a dielectric for the LC capacitor C_{LC}. The pixel electrodes 191 are connected to the main and sub switching elements Q1 and Q2. The common electrode 270 is supplied with a common voltage Vcom and covers the entire surface of the upper panel 200. In other embodiments, the common electrode 270 may be provided on the lower panel 100, and both electrodes 191 and 270 may be provided in the shape of a bar or stripe.

[0045] For color displays, each pixel PX uniquely represents one of three primary colors (i.e., spatial division), or each pixel PX sequentially represents all three primary colors in turn (i.e., time division), such that a spatial or temporal sum of the three primary colors is recognized as a desired color. FIG. 2 shows an example of the spatial division type of color display in which each pixel is provided with a color filter 230 representing one of the primary colors, e.g., red, green, or blue, in an area of the upper panel 200 facing a pixel electrode 191. Alternatively, the color filter 230 may be provided on or under the pixel electrode 191 on the lower panel 100.

[0046] A pair of polarizers (not shown) for polarizing the light are attached on the outer surfaces of the panels 100 and 200 of the panel assembly 300.

[0047] The LCD may further include at least one retardation film (not shown) for compensating the retardation of the LC layer 3.

[0048] Referring back to FIG. 1, the gray voltage generator 800 generates two sets of a plurality of gray voltages related to the transmittance of the pixels PX. The gray voltages in one set have a positive polarity with respect to the common voltage Vcom, while those in the other set have a negative polarity with respect to the common voltage Vcom.

[0049] The gate driver 400 is connected to the gate lines G1-Gn of the liquid crystal panel assembly 300, and synthesizes the gate-on voltage Von and the gate-off voltage

Voff from an external device to generate gate signals for application to the gate lines G1-Gn. The gate driver 400 may be mounted on the liquid crystal panel assembly 300, and may comprise a plurality of IC (integrated circuit) chips. Each IC chip of the gate driver 400 is respectively connected to the gate lines G1-Gn and includes a plurality of thin film transistors.

[0050] The data driver 500 is connected to the data lines D1-Dm of the liquid crystal panel assembly 300 and applies data voltages, which are selected from the gray voltages supplied from the gray voltage generator 800, to the data lines D1-Dm. The data driver 500 may also be mounted on the panel assembly 300 and may also comprise a plurality of IC chips.

[0051] The IC chips of the drivers 400 and 500 may be mounted on flexible printed circuit (FPC) films as a TCP (tape carrier package), and are attached to the liquid crystal panel assembly 300. Alternatively, the drivers 400 and 500 may be integrated into the liquid crystal panel assembly 300 along with the display signal lines G1-Gn and D1-Dm and the TFT switching elements Q1 and Q2.

[0052] The IC chips of the drivers 400 and 500, or the flexible printed circuit (FPC) films, are located at a peripheral area of the liquid crystal panel assembly 300.

[0053] The signal controller 600 generates control signals for controlling the drivers 400 and 500 and provides the corresponding control signals for the drivers 400 and 500.

[0054] Now, the operation of the LCD will be described in detail.

[0055] The signal controller 600 is supplied with image signals R, G, and B and input control signals for controlling the display thereof, such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a main clock signal MCLK, and a data enable signal DE, from an external graphic controller (not shown). After generating gate control signals CONT1 and data control signals CONT2 and processing the image signals R, G, and B to be suitable for the operation of the panel assembly 300 on the basis of the input control signals, the signal controller 600 provides the gate control signals CONT1 for the gate driver 400, and the processed image data DAT and the data control signals CONT2 for the data driver 500.

[0056] The gate control signals CONT1 include a scanning start signal STV for instructing the gate driver 400 to start scanning, and at least one clock signal for controlling the output time of the gate-on voltage Von. The gate control signals CONT1 may further include an output enable signal OE for defining the duration of the gate-on voltage Von.

[0057] The data control signals CONT2 include a horizontal synchronization start signal STH for informing the data driver 500 of start of data transmission for image data DAT of a group of pixels, a load signal LOAD for instructing the data driver 500 to apply the data voltages to the data lines D1-Dm, and a data clock signal HCLK. The data control signal CONT2 may further include an inversion signal RVS for reversing the polarity of the data voltages (with respect to the common voltage Vcom).

[0058] The data driver 500 receives a packet of the image data DAT for a pixel row from the signal controller 600, and converts the image data DAT into the analogue data voltages

selected from the gray voltages supplied from the gray voltage generator 800 in response to the data control signals CONT2 from the signal controller 600.

[0059] In response to the gate control signals CONT1 from the signal controller 600, the gate driver 400 applies the gate-on voltage Von to the gate line G1-Gn. Each of the gate lines G1-Gn are connected to the main switching elements Q1 of the corresponding pixel row and to the sub switching elements Q2 of the following pixel row, thereby simultaneously turning on the main and the sub switching elements Q1 and Q2 connected thereto. Accordingly, the data voltage applied to the data lines D1-Dm is supplied to the pixels of one row through the main switching element Q1, while the common voltage as a pre-charging voltage is supplied to the pixels of the following row through the sub switching element Q2.

[0060] The difference between the data voltage and the common voltage Vcom is represented as a voltage across the LC capacitor C_{LC}, which is referred to as a pixel voltage. The LC molecules in the LC capacitor C_{LC} have orientations depending on the magnitude of the pixel voltage, and the molecular orientations determine the polarization of light passing through the LC layer 3. The polarizer(s) converts light polarization into light transmittance.

[0061] The row pixel applied by the common voltage through the sub switching element Q2 receives the corresponding data voltage through the main switching element Q1 after the 1 horizontal period (1 H).

[0062] By repeating this procedure by a unit of the horizontal period (which is indicated by 1 H and is equal to one period of the horizontal synchronization signal Hsync and the data enable signal DE), all gate lines G1-Gn are sequentially supplied with the gate-on voltage Von during a frame, thereby applying the data voltages to all pixels. When the next frame starts after finishing one frame, the inversion control signal RVS applied to the data driver 500 is controlled such that the polarity of the data voltages is reversed (which is called "frame inversion"). The inversion control signal RVS may also be controlled such that the polarity of the data voltages flowing in a data line in one frame are reversed (for example, line inversion and dot inversion), or the polarity of the data voltages in one packet are reversed (for example, column inversion and dot inversion).

[0063] As above-described, the common voltage as a pre-charging voltage is supplied to all pixels with the same voltage, and accordingly the charging ratio thereof may be uniform.

[0064] The liquid crystal panel assembly of an LCD according to one embodiment of the present invention will now be described in detail with reference to FIGS. 3 and 4 as well as FIGS. 1 and 2.

[0065] FIG. 3 is a layout view of a lower panel of the liquid crystal panel assembly shown in FIGS. 1 and 2 according to an embodiment of the present invention, and FIG. 4 is a sectional view of the liquid crystal panel assembly including the lower panel in FIG. 3 taken along the lines IV-IV.

[0066] The common electrode panel 200 will now be described in detail.

[0067] A light blocking member **220** referred to as a black matrix for preventing light leakage is formed on an insulating substrate **210** made of a material such as transparent glass or plastic. The light blocking member **220** may be a single layer made of chromium or a double layer made of chromium and chromium nitride, and may be made of organic material including a black pigment.

[0068] A plurality of color filters **230** are also formed on the substrate **210**, and they are disposed substantially in the areas enclosed by the light blocking member **220**. The color filters **230** may extend substantially along the longitudinal direction, and the edge of the adjacent color filters **230** may overlap each other.

[0069] A common electrode **270** is formed on the color filters **230**. The common electrode **270** is preferably made of transparent conductive material such as ITO and IZO.

[0070] An overcoat (not shown) may be added between the color filters **230** and the common electrode **270** to prevent the color filters **230** from being exposed or to provide a flat surface.

[0071] The TFT array panel **100** will now be described in detail.

[0072] A plurality of gate lines **121** are formed on an insulating substrate **110**. The gate lines **121** are for transmitting gate signals, and they extend substantially in a transverse direction and are separated from each other. Each gate line **121** includes a plurality of projections forming a plurality of first and second gate electrodes **124a** and **124b** respectively protruding downward and upward, and an end portion **129** having a large area for contact with another layer or an external device. The end portions **129** might not be provided when a gate driving circuit (not shown) is integrated on the substrate **110** such that the gate lines **121** are in direct contact with the gate driving circuit.

[0073] The gate lines **121** are preferably made of an Al-containing metal such as Al and an Al alloy, a Ag-containing metal such as Ag and a Ag alloy, a Cu-containing metal such as Cu and a Cu alloy, a Mo-containing metal such as Mo and a Mo alloy, Cr, Ta, or Ti. However, they may have a multi-layered structure including two conductive films (not shown) having different physical characteristics. One of the two films is preferably made of a low resistivity metal including an Al-containing metal, a Ag-containing metal, and a Cu-containing metal for reducing signal delay or voltage drop. The other film is preferably made of a material such as a Mo-containing metal, Cr, Ta, or Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). Good examples of the combination of the two films are a lower Cr film and an upper Al (alloy) film and a lower Al (alloy) film and an upper Mo (alloy) film. However, the gate lines **121** may be made of various metals or conductors.

[0074] In addition, the lateral sides of the gate lines **121** are inclined relative to a surface of the substrate **110**, and the inclination angle thereof ranges about 30-80 degrees.

[0075] A gate insulating layer **140** preferably made of silicon nitride (SiNx) is formed on the gate lines **121**.

[0076] A plurality of semiconductor stripes **151** and a plurality of semiconductor islands **154b**, which are prefer-

ably made of hydrogenated amorphous silicon (abbreviated as "a-Si") or polysilicon, are formed on the gate insulating layer **140**. Each semiconductor stripe **151** extends substantially in the longitudinal direction and is periodically curved. Each semiconductor stripe **151** has a plurality of projections **154a** branched out toward the first gate electrodes **124a**. Each semiconductor island **154b** is disposed on the second gate electrodes **124b**.

[0077] A plurality of ohmic contact stripes **161** and islands **163b**, **165a**, and **165b** preferably made of silicide or n+hydrogenated a-Si heavily doped with an N-type impurity are formed on the semiconductor stripes and islands **151** and **154b**. Each ohmic contact stripe **161** has a plurality of projections **163a**, and the projections **163a**, and the ohmic contact islands **165a** are located in pairs on the projections **154a** of the semiconductor stripes **151a**. The ohmic contact islands **163b** and **165b** are located in pairs on the semiconductor islands **154b**.

[0078] The lateral sides of the semiconductors **151** and **154b**, and the ohmic contacts **161**, **163b**, **165a**, and **165b** are inclined relative to the surface of the substrate **110**, and the inclination angles thereof are preferably in a range between about 30-80 degrees.

[0079] A plurality of data lines **171**, a plurality of second source electrodes **173b**, and a plurality of first and second drain electrodes **175a** and **175b** separated from each other are formed on the ohmic contacts **161**, **163b**, **165a**, and **165b** and the gate insulating layer **140**.

[0080] The data lines **171** for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines **121**. Each data line **171** has an end portion **179** having a large area for contact with another layer or an external device and a first source electrode **173a**. Each first source electrode **173a** is extended to the first gate electrode **124a** and encloses the first drain electrode **175a** with "U" shape.

[0081] The second source electrode **173b** is separated from the data lines **171** and at least overlaps a portion of the second gate electrode **124b**.

[0082] Each of the first and second drain electrodes **175a** and **175b** are respectively separated from the data line **171** and the second source electrode **175b**, and are respectively disposed opposite the first and second source electrodes **173a** and **173b** with the respect to the first and second gate electrodes **124a** and **124b**. The first drain electrode **175a** includes an end portion having a large area for contact with another layer and another end portion enclosed by the first source electrode **173a**.

[0083] Each set of the first gate electrode **124a**, the first source electrode **173a**, and the first drain electrode **175a** along with a projection **154a** of a semiconductor stripe **151** form a TFT Q1 having a channel formed in the semiconductor projection **154a** disposed between the first source electrode **173a** and the first drain electrode **175a**. Each set of the second gate electrode **124b**, the second source electrode **173b**, and the second drain electrode **175b** along with the second semiconductor islands **154b** form a TFT Q2 having a channel formed in the semiconductor island **154b** disposed between the second source electrode **173b** and the second drain electrode **175b**.

[0084] The data lines 171, the second source electrodes 173a, and the drain electrodes 175a and 175b are preferably made of a refractory metal such as Cr, Mo, Ta, Ti, or alloys thereof. However, they may have a multilayered structure including a refractory metal film (not shown) and a low resistivity film (not shown). Good examples of the multilayered structure are a double-layered structure including a lower Cr/Mo (alloy) film and an upper Al (alloy) film and a triple-layered structure of a lower Mo (alloy) film, an intermediate Al (alloy) film, and an upper Mo (alloy) film. However, the data conductors 171 and 175 may be made of various metals or conductors.

[0085] Like the gate lines 121, the data lines 171, the second source electrodes 173a, and the drain electrodes 175a and 175b have inclined lateral sides, and the inclination angles thereof range about 30-80 degrees.

[0086] The ohmic contacts 161, 163b, 165a, and 165b are interposed only between the underlying semiconductors 151 and 154b, and the overlying data lines 171, the second source electrodes 173b, and the overlying drain electrodes 175a and 175b thereon, and reduce the contact resistance therebetween. Although the semiconductor stripes 151 are narrower than the data lines 171 at most places, the width of the semiconductor stripes 151 becomes large near the gate lines 121 as described above, to smooth the profile of the surface, thereby preventing disconnection of the data lines 171. The semiconductors 154a and 154b respectively include a plurality of exposed portions, which are not covered with the data lines 171 and the first and the second drain electrodes 175a and 175b, such as portions respectively located between the first and second source electrodes 173a and 173b, and the first and second drain electrodes 175a and 175b.

[0087] A passivation layer 180 is formed on the data lines 171, the second source electrodes 173b, and the drain electrodes 175a and 175b, and exposed portions of the semiconductors 151 and 154b that are not covered with the data lines 171, the second source electrodes 173b, and the drain electrodes 175a and 175b. The passivation layer 180 is preferably made of a photosensitive organic material having a good flatness characteristic, a low dielectric insulating material such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD), or inorganic material such as silicon nitride and silicon oxide. The passivation layer 180 may have a double-layered structure including a lower inorganic film and an upper organic film in order to prevent the channel portions of the semiconductor 151 and 154b from being in direct contact with organic material.

[0088] The passivation layer 180 has a plurality of contact holes 182, 183, 185a, and 185b exposing the end portions 179 of the data lines 171, the second source electrodes 173b, and the drain electrodes 175a and 175b, respectively. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 181 exposing the end portions 129 of the gate lines 121.

[0089] A plurality of pixel electrodes 191, a plurality of contact assistants 81 and 82, and a plurality of shielding electrodes 88, which are preferably made of a transparent conductive material such as ITO or IZO, are formed on the passivation layer 180. For a reflective LCD, the pixel electrodes 191 may be made of an opaque reflective material such as Ag or Al.

[0090] The pixel electrodes 191 are physically and electrically connected to the first and second drain electrodes 175a and 175b through the contact holes 185a and 185b such that the pixel electrodes 191 receive the data/common voltages from the first and second drain electrodes 175a and 175b.

[0091] The pixel electrodes 191 supplied with the data voltages generate electric fields in cooperation with the common electrode 270, which reorient liquid crystal molecules of the LC layer 3 disposed therebetween.

[0092] A pixel electrode 191 and the common electrode 270 form a capacitor called a "liquid crystal capacitor," which stores applied voltages after turn-off of the main TFT Q1. An additional capacitor called a "storage capacitor," which is connected in parallel to the liquid crystal capacitor, may be provided for enhancing the voltage storing capacity.

[0093] The shielding electrode 88 is supplied with the common voltage, and it includes longitudinal portions extending along the data lines 171 and transverse portions extending along the gate lines 121 to connect adjacent longitudinal portions. The longitudinal portions fully cover the data lines 171, while each of the transverse portions lies within the boundary of a gate line 121, and the longitudinal portions include a plurality of protrusions connected to the second source electrodes 173b through the contact holes 183.

[0094] The shielding electrode 88 blocks electromagnetic interference between the data lines 171 and the pixel electrodes 191 and between the data lines 171 and the common electrode 270 to reduce the distortion of the voltage of the pixel electrodes 190 and the signal delay of the data voltages carried by the data lines 171.

[0095] Furthermore, since the pixel electrodes 191 are required to be spaced apart from the shielding electrodes 88 for preventing a short therebetween, the pixel electrodes 191 become farther from the data lines 171 such that the parasitic capacitance therebetween is reduced.

[0096] Moreover, since the permittivity of the LC layer 3 is larger than that of the passivation layer 180, the parasitic capacitance between the data lines 171 and the shielding electrodes 88 is reduced compared with that between the data lines 171 and the common electrode 270 without the shielding electrodes 88.

[0097] In addition, the distance between the pixel electrodes 191 and the shielding electrodes 88 can be uniformly maintained since they are made at the same layer and thus the parasitic capacitance therebetween can be made to be uniform.

[0098] The contact assistants 81 and 82 are connected to the exposed end portions 129 of the gate lines 121 and the exposed end portions 179 of the data lines 171 through the contact holes 181 and 182, respectively. The contact assistants 81 and 82 protect the exposed end portions 129 and 179 and complement the adhesion between the exposed end portions 129 and 179 and external devices.

[0099] FIG. 5 is a layout view of a thin film transistor array panel for an LCD according to another embodiment of the present invention, and FIG. 6 is a sectional view of the thin film transistor array panel shown in FIG. 5 taken along the line VI-VI.

[0100] Referring to FIGS. 5 and 6, layered structures of the panel 100 according to this embodiment are almost the same as those shown in FIGS. 3 and 4.

[0101] A plurality of gate lines 121 including a plurality of gate electrodes 124a and 124b and a plurality of end portions 129 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154a and a plurality of semiconductor islands 154b, and a plurality of ohmic contact stripes 161 including a plurality of projections 163a, and a plurality of ohmic contact islands 163b, 165a, and 165b, are sequentially formed thereon. A plurality of data lines 171 including a plurality of first source electrodes 173a, a plurality of second source electrodes 173b, and a plurality of first and second drain electrodes 175a and 175b are formed on the ohmic contacts 161, 163b, 165a, and 165b, and a passivation layer 180 is formed thereon. A plurality of contact holes 181, 182, 183, 185a, and 185b are provided at the passivation layer 180 and the gate insulating layer 140. A plurality of pixel electrodes 191, a plurality of shielding electrodes 88, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180.

[0102] Differing from the LCD shown in FIGS. 3 and 4, the shielding electrodes 88 include a plurality of openings 89 disposed at the longitudinal portions of the shielding electrodes 88 and extended to the data lines 171 in this embodiment.

[0103] In this embodiment, the parasitic capacitance between the data lines 171 and the shielding electrode 88 may be reduced due to the openings 89 of the shielding electrodes 88, such that the delay of the signals applied to the data lines 171 may be reduced.

[0104] FIG. 7 is a layout view of a thin film transistor array panel for an LCD according to another embodiment of the present invention, and FIG. 8 is a sectional view of the thin film transistor array panel shown in FIG. 7 taken along the line VIII-VIII'-VIII''.

[0105] Referring to FIGS. 7 and 8, layered structures of the panels 100 according to this embodiment are almost the same as those shown in FIGS. 3 and 4.

[0106] A plurality of gate lines 121 including a plurality of gate electrodes 124a and 124b and a plurality of end portions 129 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154a and a plurality of semiconductor islands 154b, and a plurality of ohmic contact stripes 161 including a plurality of projections 163a, and a plurality of ohmic contact islands 163b, 165a, and 165b, are sequentially formed thereon. A plurality of data lines 171 including a plurality of first source electrodes 173a, a plurality of second source electrodes 173b, and a plurality of first and second drain electrodes 175a and 175b are formed on the ohmic contacts 161, 163b, 165a, and 165b, and a passivation layer 180 is formed thereon. A plurality of contact holes 181, 182, 183, 185a, and 185b are provided at the passivation layer 180 and the gate insulating layer 140. A plurality of pixel electrodes 191, a plurality of shielding electrodes 88, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180.

[0107] Differing from the LCD shown in FIGS. 3 and 4, the second source electrodes 173b overlap the gate lines 121

and the transverse portions of the shielding electrodes 88, and the contact holes 183 are disposed under the transverse portions of the shielding electrodes 88 in this embodiment. Accordingly, the aperture ratio of the pixel may be maximized.

[0108] FIG. 9 is a layout view of a thin film transistor array panel for an LCD according to another embodiment of the present invention, and FIG. 10 is a sectional view of the thin film transistor array panel shown in FIG. 9 taken along the line X-X'-X''.

[0109] Referring to FIGS. 9 and 10, layered structures of the panels 100 according to this embodiment are almost the same as those shown in FIGS. 7 and 8.

[0110] A plurality of gate lines 121 including a plurality of gate electrodes 124a and 124b and a plurality of end portions 129 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154a and a plurality of semiconductor islands 154b, and a plurality of ohmic contact stripes 161 including a plurality of projections 163a, and a plurality of ohmic contact islands 163b, 165a, and 165b, are sequentially formed thereon. A plurality of data lines 171 including a plurality of first source electrodes 173a, a plurality of second source electrodes 173b, and a plurality of first and second drain electrodes 175a and 175b are formed on the ohmic contacts 161, 163b, 165a, and 165b, and a passivation layer 180 is formed thereon. A plurality of contact holes 181, 182, 183, 185a, and 185b are provided at the passivation layer 180 and the gate insulating layer 140. A plurality of pixel electrodes 191, a plurality of shielding electrodes 88, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180.

[0111] Differing from the LCD shown in FIGS. 7 and 8, the shielding electrodes 88 include a plurality of openings 89 disposed at the longitudinal portions of the shielding electrodes 88 and overlapping the data lines 171 in this embodiment.

[0112] In this embodiment, the parasitic capacitances between the data lines 171 and the shielding electrode 88 may be also reduced due to the openings 89 of the shielding electrodes 88, such that the delay of the signals applied to the data lines 171 may be reduced.

[0113] FIG. 11 is a layout view of a thin film transistor array panel for an LCD according to another embodiment of the present invention, and FIG. 12 is a sectional view of the thin film transistor array panel shown in FIG. 11 taken along the line XII-XII'.

[0114] Referring to FIGS. 11 and 12, layered structures of the panels 100 according to this embodiment are almost the same as those shown in FIGS. 3 and 4.

[0115] A plurality of gate lines 121 including a plurality of gate electrodes 124a and 124b and a plurality of end portions 129 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154a and a plurality of semiconductor islands 154b, and a plurality of ohmic contact stripes 161 including a plurality of projections 163a and a plurality of ohmic contact islands 163b, 165a, and 165b are sequentially formed thereon. A plurality of data lines 171 including a plurality of first source electrodes 173a, a plurality of second

source electrodes **173b**, and a plurality of first and second drain electrodes **175a** and **175b** are formed on the ohmic contacts **161**, **163b**, **165a**, and **165b**, and a passivation layer **180** is formed thereon. A plurality of contact holes **181**, **182**, **183**, **185a**, and **185b** are provided at the passivation layer **180** and the gate insulating layer **140**. A plurality of pixel electrodes **191**, a plurality of shielding electrodes **88**, and a plurality of contact assistants **81** and **82** are formed on the passivation layer **180**.

[0116] Differing from the LCD shown in **FIGS. 3 and 4**, the semiconductor stripes **151** have almost the same planar shapes as the data lines **171** and the drain electrodes **175a** and **175b** as well as the underlying ohmic contacts **161**, **165a**, and **165b**. However, the projections **154a** of the semiconductor stripes **151** and the semiconductor islands **154b** include some exposed portions, which are not covered with the data lines **171** and the drain electrodes **175a** and **175b**, such as portions located between the source electrodes **173a** and **173b** and the drain electrodes **175a** and **175b**.

[0117] A manufacturing method of the TFT array panel according to one embodiment simultaneously forms the data lines **171**, the second source electrodes **173b**, the drain electrodes **175a** and **175b**, the semiconductors **151** and **154b**, and the ohmic contacts **161**, **163b**, **165a**, and **165b** using one photolithography process.

[0118] A photoresist pattern for the photolithography process has position-dependent thickness, and in particular, it has first and second portions with decreased thickness. The first portions are located on wire areas that will be occupied by the data lines **171**, the second source electrodes **173b**, and the drain electrodes **175a** and **175b**, and the second portions are located on channel areas of TFTs Q1 and Q2.

[0119] The position-dependent thickness of the photoresist can be obtained by several techniques, for example, by providing translucent areas on the exposure mask as well as transparent areas and light blocking opaque areas. The translucent areas may have a slit pattern, a lattice pattern, or be a thin film(s) with intermediate transmittance or intermediate thickness. When using a slit pattern, it is preferable that the width of the slits or the distance between the slits is smaller than the resolution of a light exposer used for the photolithography. Another example is to use reflowable photoresist. In detail, once a photoresist pattern made of a reflowable material is formed by using a normal exposure mask with only transparent areas and opaque areas, it is subject to a reflow process to flow onto areas without the photoresist, thereby forming thin portions.

[0120] As a result, the manufacturing process is simplified by omitting a photolithography step.

[0121] Many of the above-described features of the LCD shown in **FIGS. 1-10** may be appropriate for the LCD shown in **FIGS. 11 and 12**.

[0122] As above-described, the common voltage as a pre-charging voltage is supplied to all the pixels as the same voltage by using the shielding electrode for the pre-charge operation, and accordingly the characteristics of the display device may be uniform and stable.

[0123] While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications

and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

What is claimed is:

1. A liquid crystal display comprising:

a plurality of pixels including first and second thin film transistors and a pixel electrode connected to the first and second thin film transistors;

a first gate line transmitting a first gate signal and connected to the first thin film transistor;

a second gate line transmitting a second gate signal and connected to the second thin film transistor; and

a data line transmitting a data signal and connected to the first thin film transistor,

wherein the second thin film transistor receives a uniform voltage and transmits the uniform voltage to the pixel electrode according to the second gate signal.

2. The liquid crystal display of claim 1, wherein the second thin film transistor is turned on more quickly than the first thin film transistor.

3. The liquid crystal display of claim 1, further comprising:

a common electrode facing the pixel electrode; and

a liquid crystal layer formed between the common electrode and the pixel electrode.

4. The liquid crystal display of claim 1, wherein the uniform voltage is the voltage supplied to the common electrode.

5. A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a data line intersecting the gate line;

a shielding electrode formed on the data line;

a first thin film transistor connected to the gate line and the data line;

a second thin film transistor connected to the gate line and the shielding electrode;

a pixel electrode connected to the first and second thin film transistors; and

a passivation layer formed under the shielding electrode and the pixel electrode, and over the data line.

6. The thin film transistor array panel of claim 5, wherein the shielding electrode has an opening extended along the data line.

7. The thin film transistor array panel of claim 5, wherein the first thin film transistor includes:

a first gate electrode connected to the gate line;

a first semiconductor overlapping the first gate electrode;

a first source electrode connected to the data line and overlapping the first semiconductor; and

a first drain electrode overlapping the first semiconductor and connected to the pixel electrode.

8. The thin film transistor array panel of claim 7, wherein the second thin film transistor includes:

- a second gate electrode connected to the gate line;
- a second semiconductor overlapping the second gate electrode;
- a second source electrode connected to the shielding electrode and overlapping the second semiconductor; and
- a second drain electrode overlapping the second semiconductor and connected to the pixel electrode.

9. The thin film transistor array panel of claim 8, wherein the shielding electrode comprises a protrusion extended to the second semiconductor, wherein the second source electrode is connected to the protrusion.

10. The thin film transistor array panel of claim 8, wherein the shielding electrode has a connection connecting the adjacent shielding electrodes to each other and the shielding electrode overlaps at least the gate line.

11. The thin film transistor array panel of claim 10, wherein the second source electrode is disposed on the gate line and is connected to the connection on the gate line.

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专利名称(译)	薄膜晶体管阵列面板和包括其的液晶显示器		
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摘要(译)

提供一种液晶显示器，包括多个像素，包括第一和第二薄膜晶体管，以及连接到第一和第二薄膜晶体管的像素电极，传输第一栅极信号并连接到第一薄膜的第一栅极线薄膜晶体管，传输第二栅极信号并连接到第二薄膜晶体管的第二栅极线，以及传输数据信号并连接到第一薄膜晶体管的数据线。第二薄膜晶体管接收均匀电压，并根据第二栅极信号将均匀电压传输至像素电极。

