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(54) **ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE USING THE SAME**

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(57) **ABSTRACT**

An array substrate for a liquid crystal display device includes: a gate line on a substrate along a first direction; a data line along a second direction and crossing the gate line, the crossing of the data line and the gate line defining a pixel region having a parallelogrammic shape; a thin film transistor connected to the gate line and the data line; and a pixel electrode in the pixel region and connected to the thin film transistor.

(73) **Assignee: LG.Philips LCD Co., Ltd.**

(21) **Appl. No.: 11/022,755**

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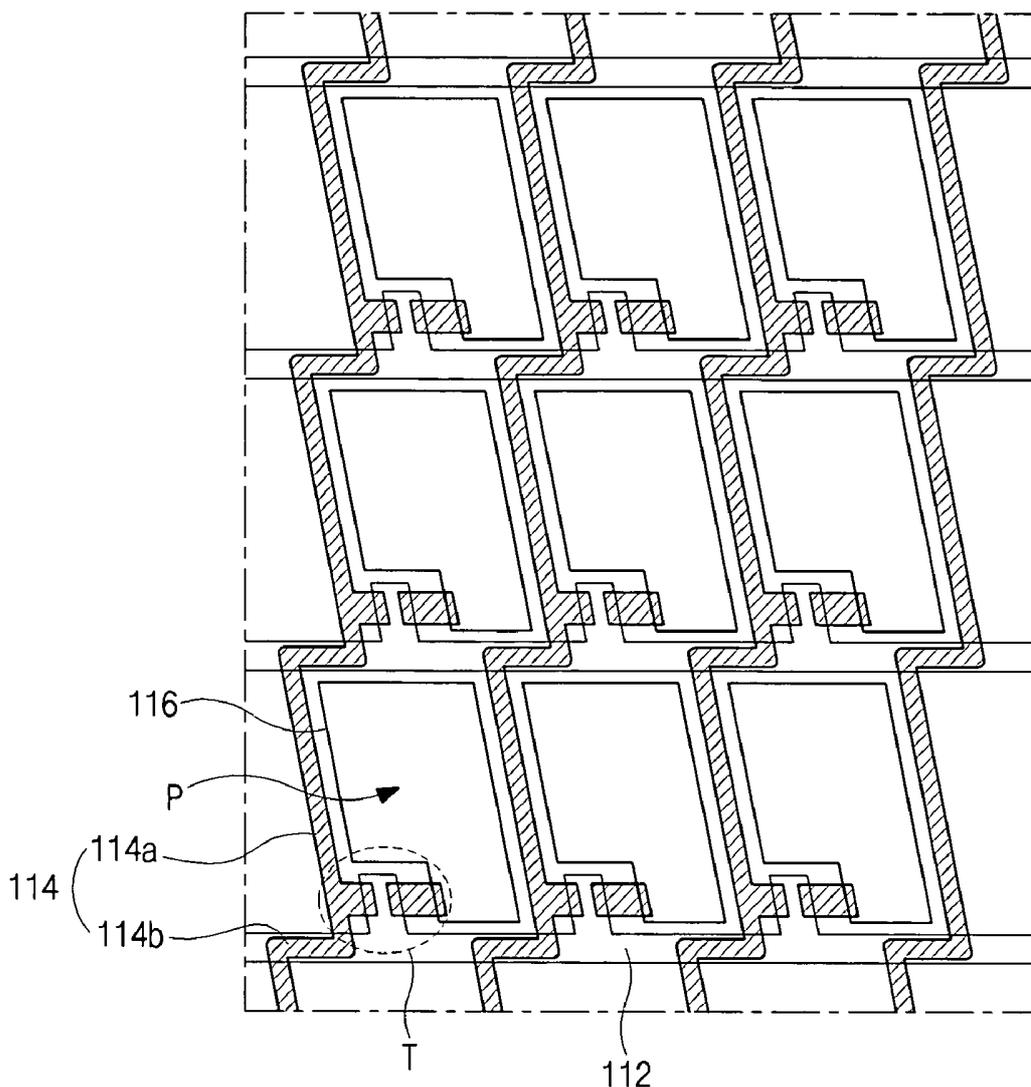


FIG. 1
RELATED ART

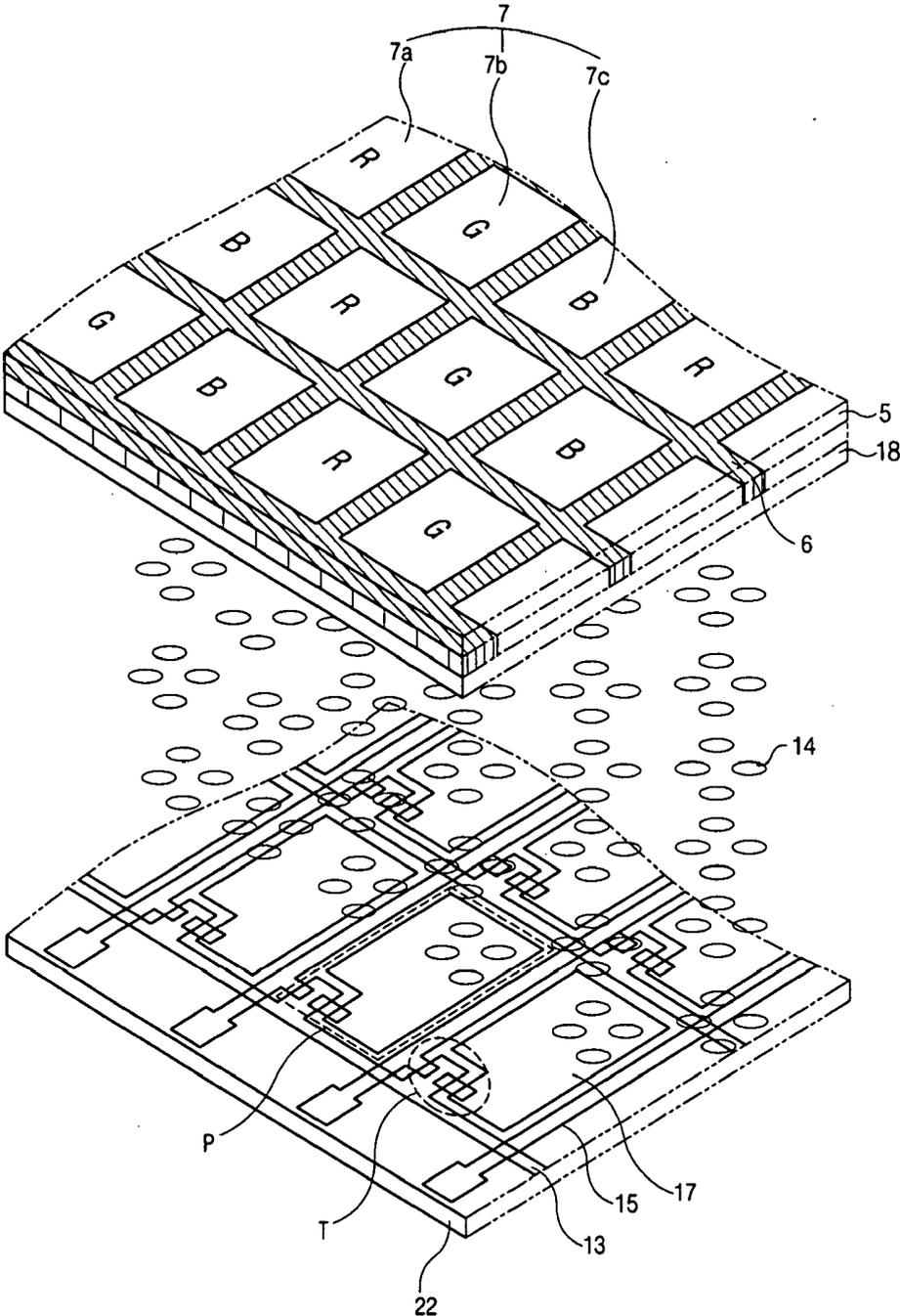


FIG. 2
RELATED ART

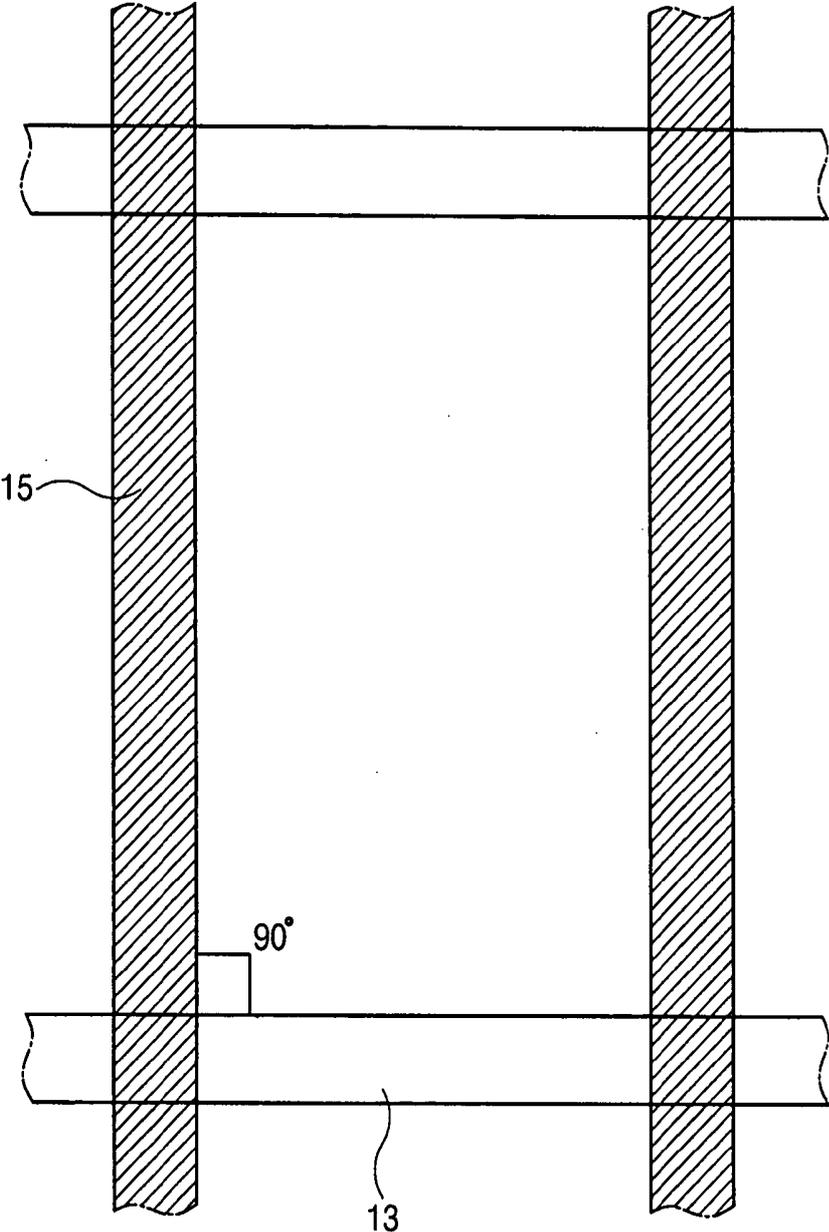


FIG. 3

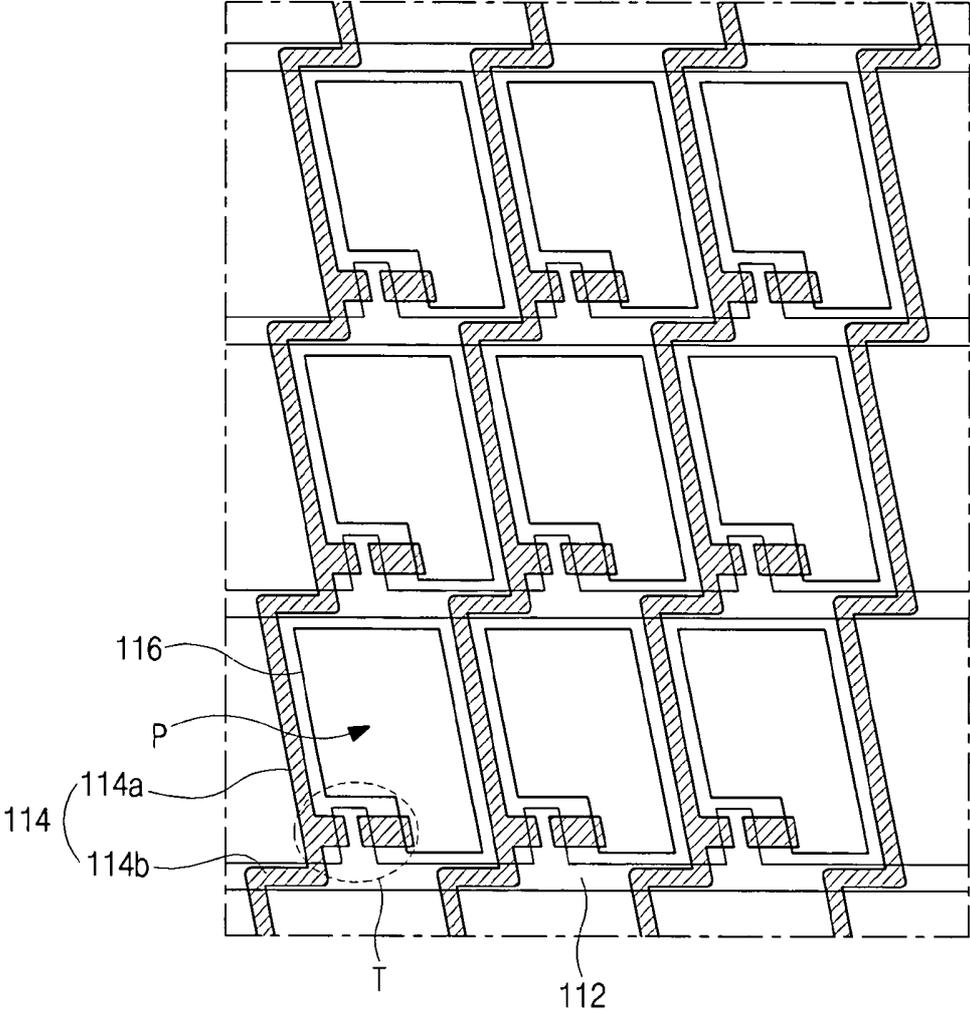


FIG. 4

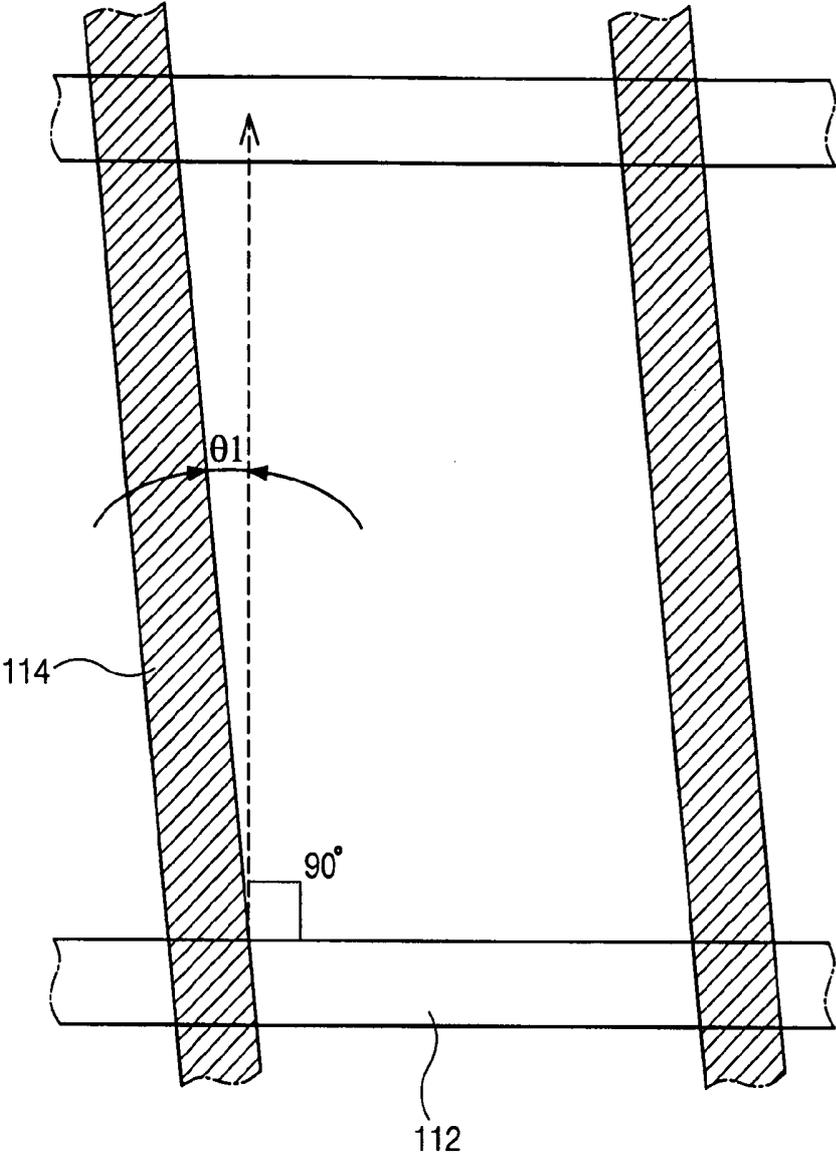


FIG. 5

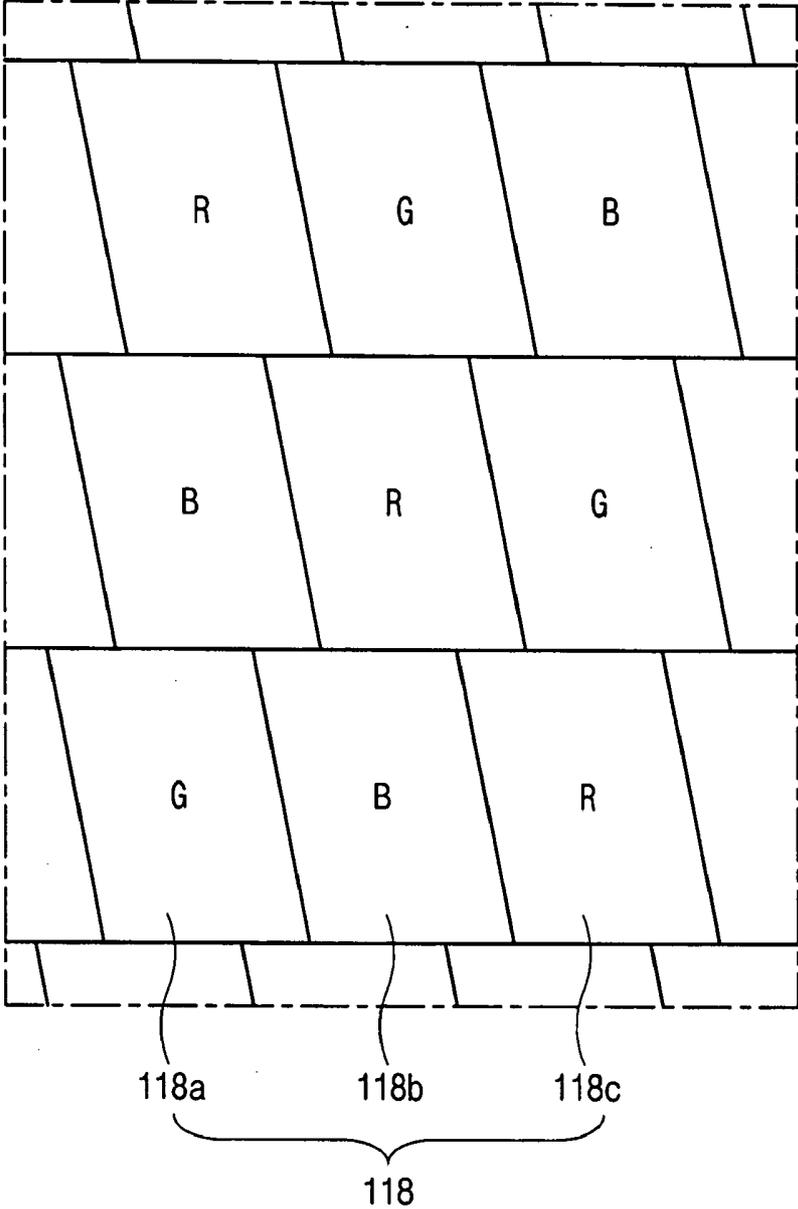


FIG. 6

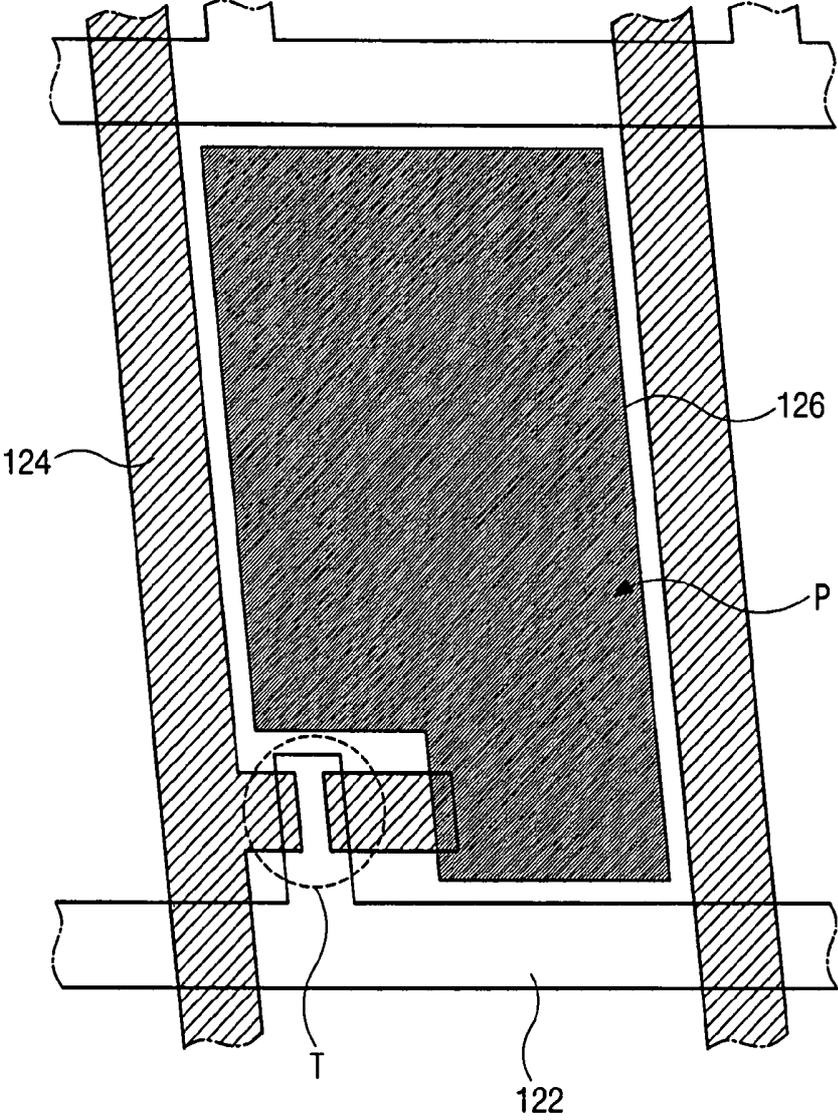


FIG. 7

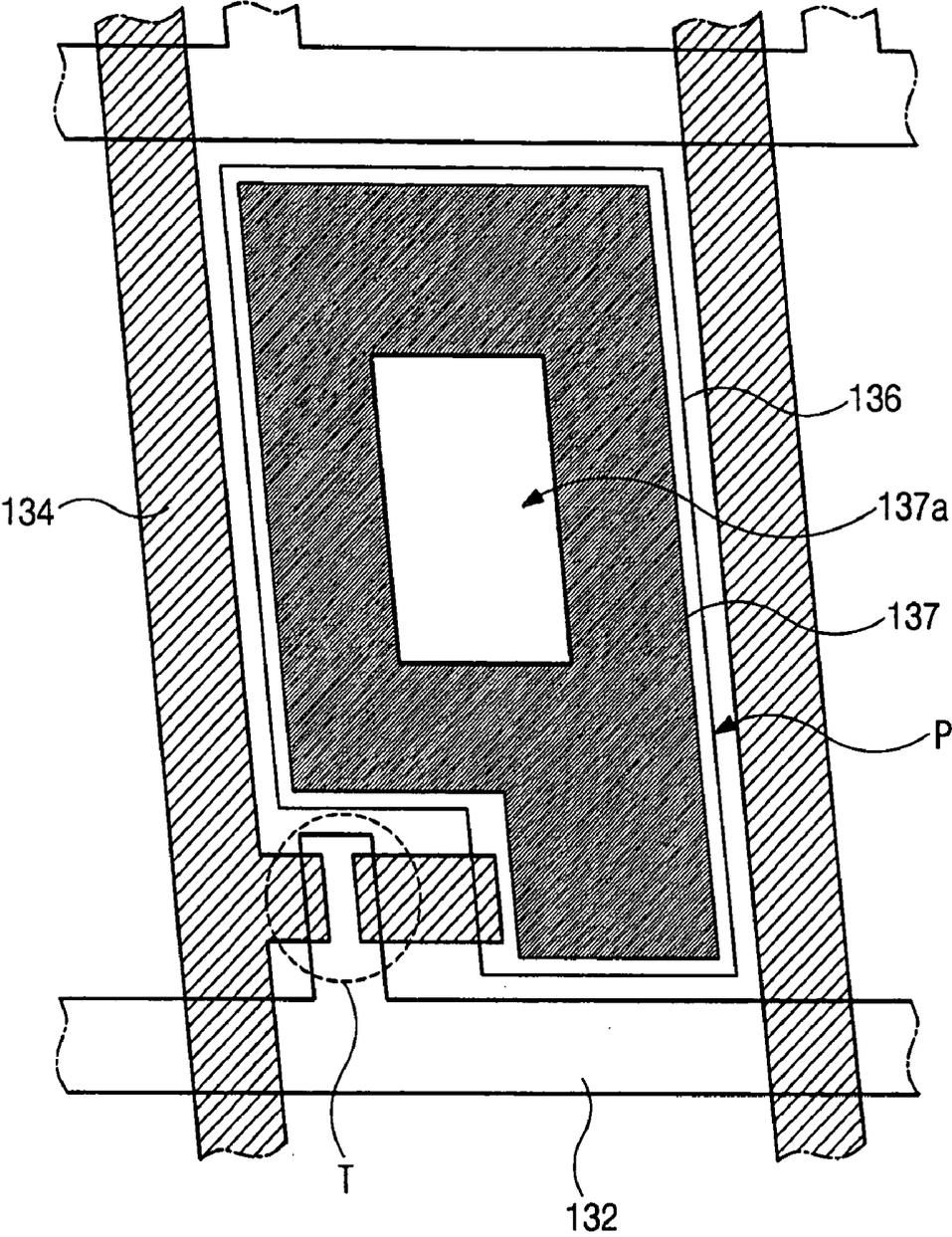


FIG. 8

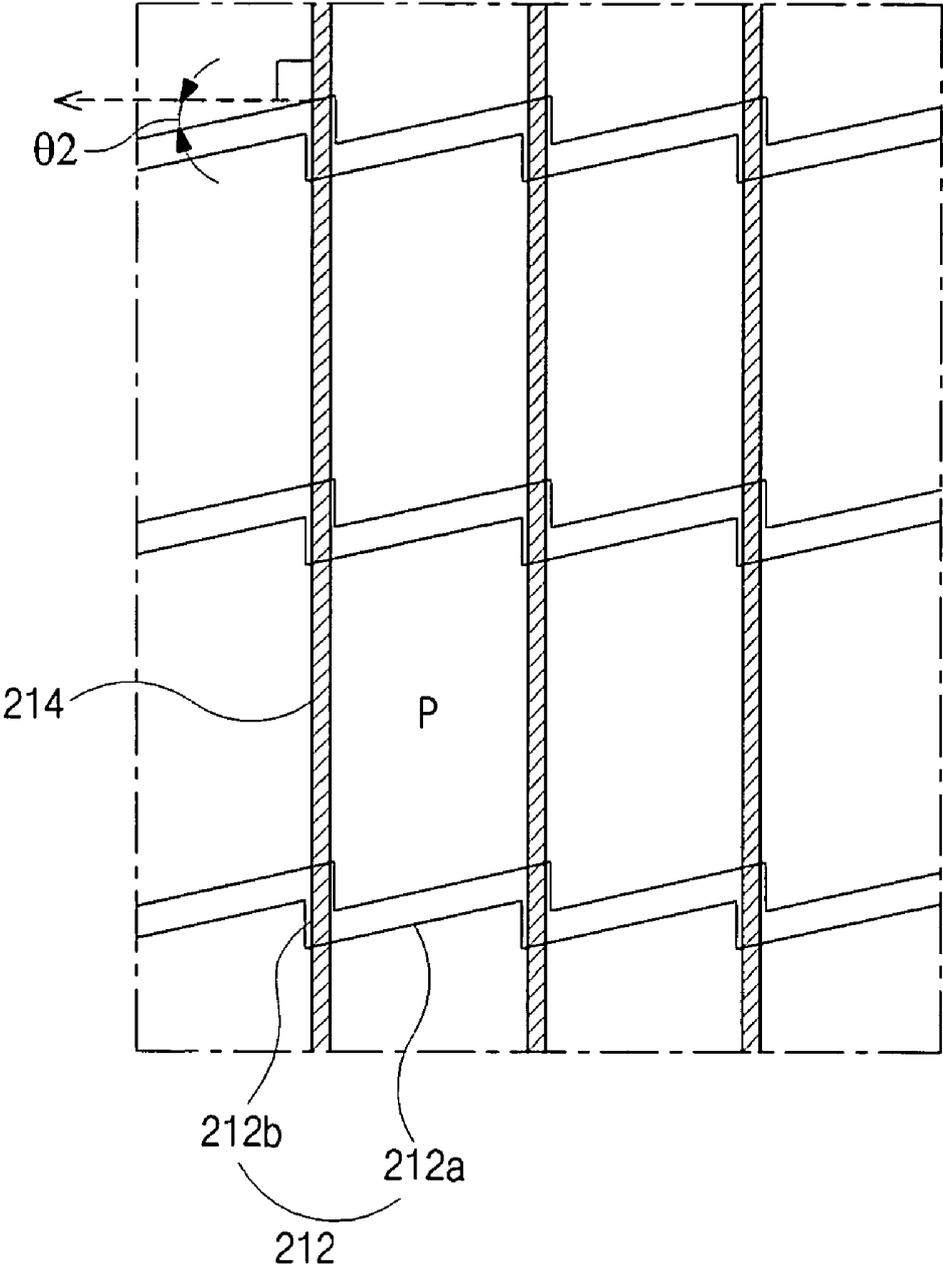


FIG. 9

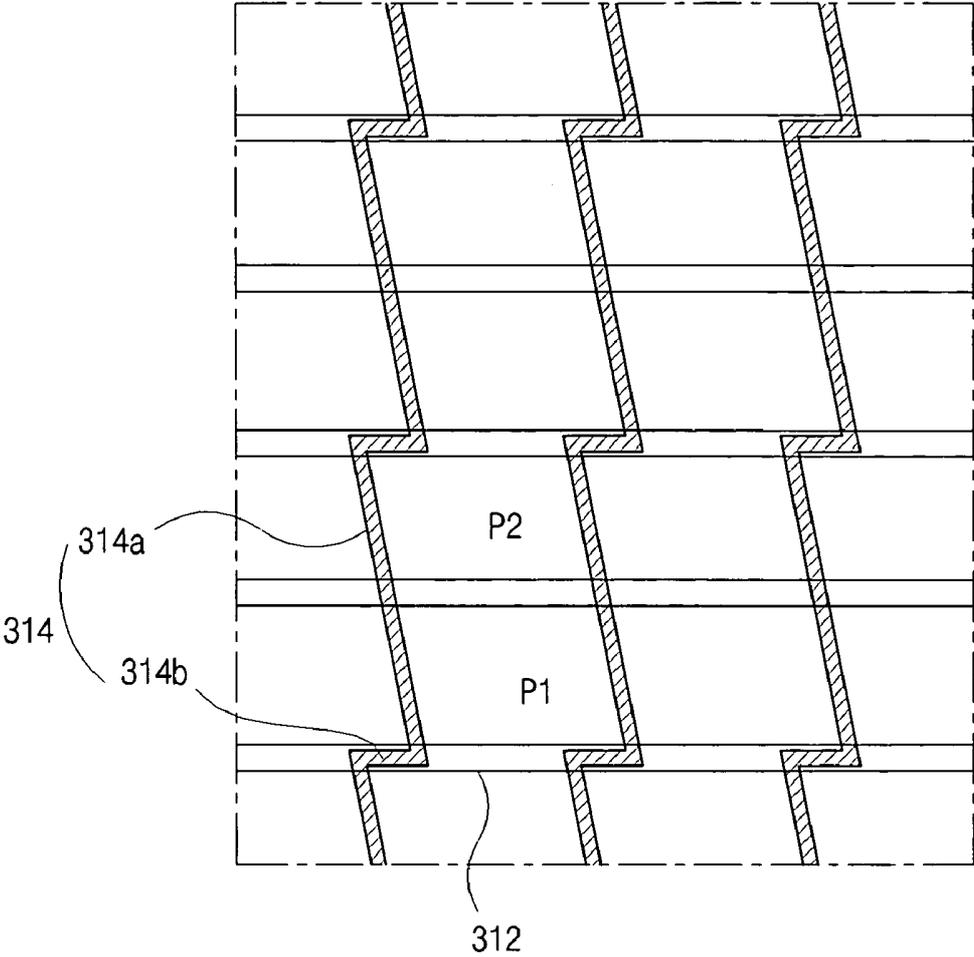
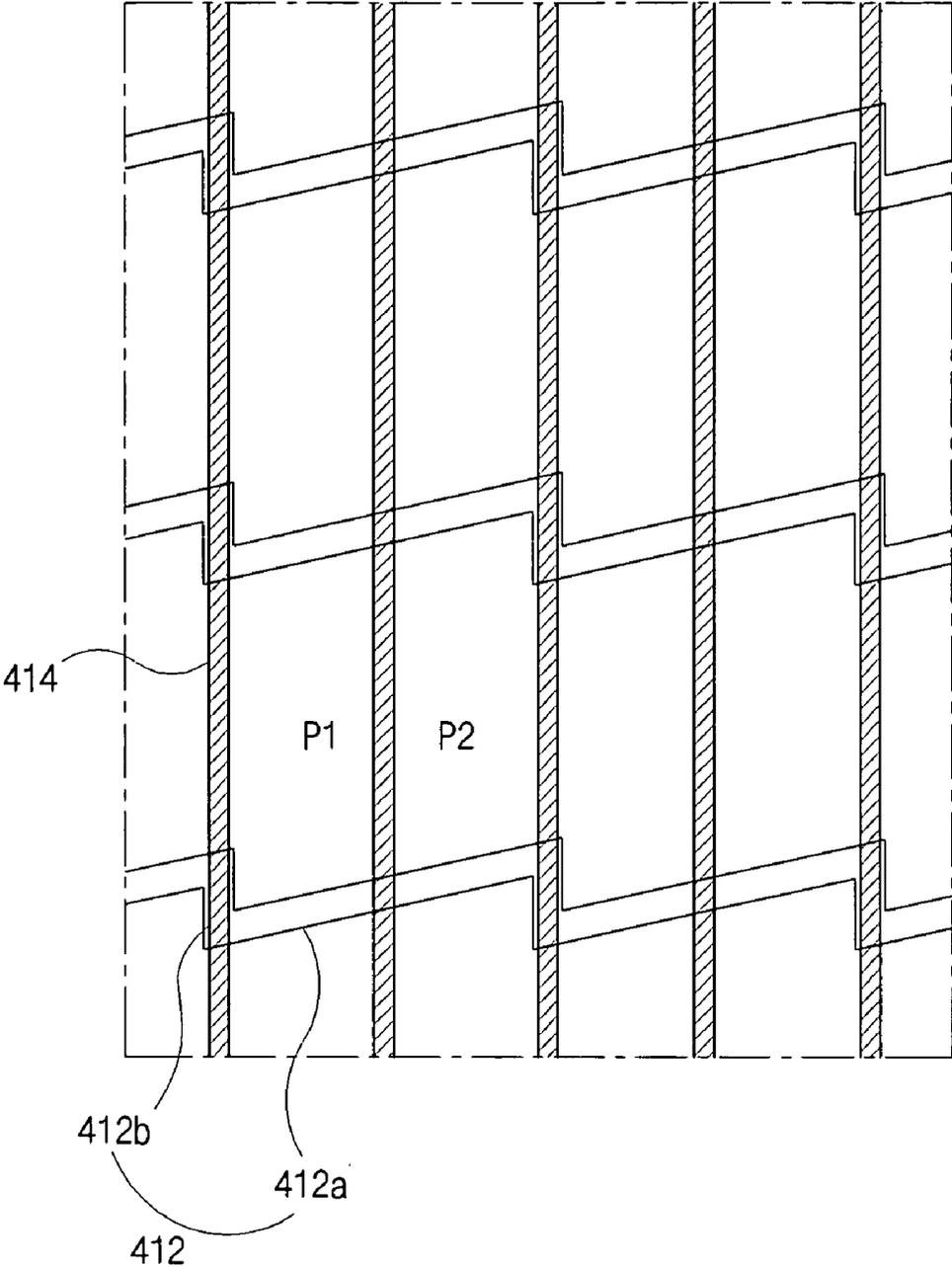


FIG. 10



ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE USING THE SAME

[0001] The present invention claims the benefit of Korean Patent Application No. 2003-0099427, filed in Korea on Dec. 29, 2003, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display device, and more particularly, to an array substrate and a liquid crystal display device using the array substrate.

[0004] 2. Discussion of the Related Art

[0005] In general, the LCD devices include two substrates, each having electrodes that face each other, and a liquid crystal layer interposed between the electrodes. When a voltage is supplied to the electrodes, an electric field is generated to modulate light transmittance through the liquid crystal layer by reorienting the liquid crystal molecules, thereby displaying images. Among various types of LCD devices, active matrix liquid crystal display (AM-LCD) devices having thin film transistors (TFTs) and pixel electrodes arranged in matrix have been widely researched because of their superior resolution and capability to smoothly display moving images.

[0006] In a related art LCD device, a pixel electrode and a common electrode are positioned on a lower substrate and on an upper substrate, respectively. Thus, a longitudinal electric field is induced between the lower and upper substrates of the related art LCD device. This longitudinal electric field, which is perpendicular to the lower and upper substrates, drives liquid crystal molecules between the lower and upper substrates. Accordingly, the related art LCD device has superior light transmittance and aperture ratio. In addition, since the common electrode is grounded, breakdown of the liquid crystal cell is prevented.

[0007] FIG. 1 is an exploded perspective view of a liquid crystal display device according to the related art. In FIG. 1, a liquid crystal display (LCD) device includes a first substrate 22 and a second substrate 5, and a liquid crystal material 14 interposed therebetween. The first substrate 22 and the second substrate 5 face each other and are spaced apart from each other. A gate line 13 formed on the first substrate 22 crosses a data line 15 to define a pixel region "P." A thin film transistor (TFT) "T" used as a switching element is connected to the gate line 13 and the data line 15 within the pixel region "P." A pixel electrode 17 is also positioned in the pixel region "P" and connected to the TFT "T."

[0008] A black matrix 6 having an open portion corresponding to the pixel region "P" is formed on the second substrate 5 and a color filter layer 7 including one of red, green and blue sub-color filters 7a, 7b and 7c is formed in the open portion. The color filter layer corresponds to the pixel electrode 17. A common electrode 18 is formed on the black matrix 6 and the color filter layer 7. The first substrate 22 having the TFT "T" and the pixel electrode 17 may be referred to as an array substrate and the second substrate 5 having the color filter layer 7 may be referred to as a color filter substrate.

[0009] FIG. 2 is a plan view showing a pixel region of an array substrate for a liquid crystal display device according to the related art. In FIG. 2, a gate line 13 is disposed along a first direction and a data line 15 is disposed along a second direction perpendicular to the first direction. Accordingly, the gate line 13 and the data line 15 perpendicularly cross each other. Since the gate line 13 and the data line 15 are formed of a metallic material having relatively high reflectance, an incident light reflects from the gate line 13 and the data line 15. The light reflecting from the gate line 13 and the data line 15 makes an interference pattern having a wave shape due to the periodicity of the gate line 13 and the data line 15. The interference pattern may be referred to as a moire phenomenon that deteriorates the display quality of the LCD device.

SUMMARY OF THE INVENTION

[0010] Accordingly, the present invention is directed to an array substrate and a liquid crystal display device using the array substrate that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0011] An object of the present invention is to provide an array substrate for a liquid crystal display device having improved display quality and a liquid crystal display device using the array substrate.

[0012] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. These and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0013] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for a liquid crystal display device includes: a gate line on a substrate along a first direction; a data line along a second direction and crossing the gate line, the crossing of the data line and the gate line defining a pixel region having a parallelogrammic shape; a thin film transistor connected to the gate line and the data line; and a pixel electrode in the pixel region and connected to the thin film transistor.

[0014] In another aspect, a liquid crystal display device includes: first and second substrates facing each other and spaced apart from each other; a gate line on the first substrate along a first direction; a data line along a second direction and crossing the gate line, the crossing of the data line and the gate line defining a pixel region having a parallelogrammic shape; a thin film transistor connected to the gate line and the data line; a pixel electrode in the pixel region and connected to the thin film transistor; a color filter layer on the second substrate; and a common electrode on the color filter layer.

[0015] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are included to provide a further understanding of the invention and are

incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0017] FIG. 1 is an exploded perspective view of a liquid crystal display device according to the related art.

[0018] FIG. 2 is a plan view showing a pixel region of an array substrate for a liquid crystal display device according to the related art.

[0019] FIG. 3 is a plan view showing an array substrate for a liquid crystal display device according to an embodiment of the present invention.

[0020] FIG. 4 is a plan view showing a pixel region of an array substrate for a liquid crystal display device according to an embodiment of the present invention.

[0021] FIG. 5 is a plan view showing a color filter substrate for a liquid crystal display device according to an embodiment of the present invention.

[0022] FIG. 6 is a plan view showing a pixel region of an array substrate for a reflective liquid crystal display device according to an embodiment of the present invention.

[0023] FIG. 7 is a plan view showing a pixel region of an array substrate for a transmissive liquid crystal display device according to an embodiment of the present invention.

[0024] FIG. 8 is a plan view showing an array substrate for a liquid crystal display device according to an embodiment of the present invention.

[0025] FIG. 9 is a plan view showing an array substrate for a liquid crystal display device according to an embodiment of the present invention.

[0026] FIG. 10 is a plan view showing an array substrate for a liquid crystal display device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] Reference will now be made in detail to the preferred embodiments of the present invention, an example of which is illustrated in the accompanying drawings.

[0028] FIG. 3 is a plan view showing an array substrate for a liquid crystal display device according to an embodiment of the present invention. As shown in FIG. 3, a gate line 112 is formed on a first substrate (not shown) along a first direction and a data line 114 is formed along a second direction. The gate line 112 crosses the data line 114 to define a pixel region "P." Since the gate line 112 has a straight shape and the data line 114 has a zigzag shape, the pixel region "P" has a parallelogrammic shape. The data line 114 includes a first portion 114a tilted with respect to a virtual line perpendicular to the gate line 112 and a second portion 114b parallel to the gate line 112. The second portion 114b is disposed at the corner of every pixel region "P." A thin film transistor (TFT) "T" is connected to the gate line 112 and the data line 114. The TFT "T" includes a gate electrode connected to the gate line 112, a source electrode connected to the data line 114 and a drain electrode spaced apart from the source electrode. A pixel electrode 116 connected to the drain electrode is formed within the pixel region "P."

[0029] The second portion 114b overlaps the gate line 112 in the embodiment shown in FIG. 3. However, the second portion 114b does not have to overlap the gate line 112 in other embodiments. Accordingly, the second portion 114b can be separated from the gate line 112 in plan a view to minimize a signal delay due to parasitic capacitance between the gate line 112 and the data line 114.

[0030] FIG. 4 is a plan view showing a pixel region of an array substrate for a liquid crystal display device according to an embodiment of the present invention. As shown in FIG. 4, even though a data line 114 crosses a gate line 112, the data line 114 is tilted with respect to a virtual line perpendicular to the gate line 112. Accordingly, the data line 114 is not perpendicular to the gate line 112 and an angle between the gate line 112 and the data line 114 is not 90°. For example, the angle between the gate line 112 and the data line 114 may be about $90^\circ + \theta_1$, where θ_1 is a tilt angle within a range of about 0° to about 10°, such as greater than 0° and smaller than 10°. In another embodiment, a tilt direction of the data line 114 may be in an opposite direction with respect to a virtual line perpendicular to the gate line 112. As a result, the data line 114 may cross the gate line 112 at a cross angle within ranges of about 80° to about 90° and about 90° to about 100°, such as a range of about 80° to about 100° except for 90°. In other words, the data line 114 may cross the gate line 112 with a cross angle greater than 80° and smaller than 90° or greater than 90° and smaller than 100°.

[0031] The gate line 112 and the data line 114 have a periodicity even when the gate line 112 and the data line 114 cross each other with a crossing angle other than 90°. However, since the periodicity when the gate line 112 and the data line 114 have a crossing angle other than 90° unlike when the gate line and the data line have a cross angle of 90°, an interference pattern is reduced while images are displayed. Accordingly, the moire phenomenon is reduced and display quality of an LCD device is improved.

[0032] In order to improve an aperture ratio of an LCD device, a black matrix of a color filter substrate for an LCD device may be omitted in embodiments of the present invention. In the related art where the gate line and the data line cross each other with a cross angle of 90°, the moire phenomenon becomes even more severe when the black matrix is omitted. However, the moire phenomenon is prevented in embodiments of the present invention by the gate line 112 and the data line 114 having a crossing angle other than 90°, even when the black matrix is omitted.

[0033] FIG. 5 is a plan view showing a color filter substrate for a liquid crystal display device according to an embodiment of the present invention. As shown in FIG. 5, a color filter layer 118 including red (R), green (G) and blue (B) sub-color filters 118a, 118b and 118c is formed on a second substrate (not shown). The R, G and B sub-color filters 118a, 118b and 118c are alternately disposed. Each sub-color filter 118a, 118b and 118c has a parallelogrammic shape and corresponds to the pixel region "P" (of FIG. 3). Although not shown in FIGS. 3 and 4, when the pixel region "P" (of FIG. 3) has a parallelogrammic shape, a color filter layer may also have a parallelogrammic shape. A black matrix is omitted on the color filter substrate. A common electrode (not shown) of a transparent conductive material is formed on the color filter layer 118.

[0034] Embodiments of the present invention can be used in a transmissive LCD device, a reflective LCD device or a transmissive LCD device. The moire phenomenon is more severe in a reflective LCD device and a transmissive LCD device because an ambient light is used as a light source. However, the moire phenomenon is prevented and display quality is improved by the gate line 112 and the data line 114 having a crossing angle of other than 90° in a reflective LCD device and a transmissive LCD device.

[0035] FIG. 6 is a plane view showing a pixel region of an array substrate for a reflective liquid crystal display device according to an embodiment of the present invention. As shown in FIG. 6, a gate line 122 is formed on a first substrate (not shown) along a first direction and a data line 124 is formed along a second direction. The gate line 122 crosses the data line 124 to define a pixel region "P." The data line 124 is tilted with respect to a virtual line perpendicular to the gate line 122. Accordingly, the data line 124 is not perpendicular to the gate line 122 and an angle between the gate line 122 and the data line 124 is not 90°. In addition, the pixel region "P" has a parallelogrammic shape. A thin film transistor (TFT) "T" is connected to the gate line 122 and the data line 124. The TFT "T" includes a gate electrode connected to the gate line 122, a source electrode connected to the data line 124 and a drain electrode spaced apart from the source electrode. A pixel electrode 126 connected to the drain electrode is formed in the pixel region "P." The pixel electrode 126 includes a metallic material having a relatively high reflectance to reflect an ambient light. Moreover, the pixel electrode 126 may have an unevenness on a surface thereof to prevent mirror reflection. Since a periodic disposition of convex portions of the unevenness causes a moire phenomenon, the convex portions can be randomly disposed to prevent the moire phenomenon.

[0036] FIG. 7 is a plan view showing a pixel region of an array substrate for a transmissive liquid crystal display device according to an embodiment of the present invention. As shown in FIG. 7, a gate line 132 is formed on a first substrate (not shown) along a first direction and a data line 134 is formed along a second direction. The gate line 132 crosses the data line 134 to define a pixel region "P." The data line 134 is tilted with respect to a virtual line perpendicular to the gate line 132. Accordingly, the data line 134 is not perpendicular to the gate line 132 and an angle between the gate line 132 and the data line 134 is not 90°. In addition, the pixel region "P" has a parallelogrammic shape. A thin film transistor (TFT) "T" is connected to the gate line 132 and the data line 134. The TFT "T" includes a gate electrode connected to the gate line 132, a source electrode connected to the data line 134 and a drain electrode spaced apart from the source electrode. A pixel electrode 136 connected to the drain electrode is formed in the pixel region "P." The pixel electrode 136 includes a transparent conductive material. Moreover, a reflective plate 137 having an open portion 137a is also formed in the pixel region "P." The reflective plate 137 can be connected to the drain electrode of the TFT "T." As in a reflective LCD device, the reflective plate 137 may have an unevenness on a surface thereof to prevent mirror reflection. Since a periodic disposition of convex portions of the unevenness causes a moire phenomenon, the convex portions may be randomly disposed to prevent the moire phenomenon.

[0037] In embodiments of the present invention, a data line having a zigzag shape is tilted with respect to a virtual line perpendicular to a gate line. In an LCD device according to other embodiments of the present invention, a gate line having a zigzag shape is tilted with respect to a virtual line perpendicular to a data line.

[0038] FIG. 8 is a plan view showing an array substrate for a liquid crystal display device according to a second embodiment of the present invention. As shown in FIG. 8, a gate line 212 is formed on a substrate along a first direction and a data line 214 is formed along a second direction. The gate line 212 and the data line 214 cross each other to define a pixel region "P." Since the gate line 212 has a zigzag shape and the data line 214 has a straight shape, the pixel region "P" has a parallelogrammic shape. The gate line 212 includes a first portion 212a tilted with respect to a virtual line perpendicular to the data line 214 and a second portion 212b parallel to the data line 214.

[0039] The second portion 212b overlaps the data line 214 in FIG. 8. However, the second portion 212b does not have to overlap the data line 214 in other embodiments. Accordingly, the second portion 212b can be separated from the data line 214 in a plan view to minimize a signal delay due to a parasitic capacitance between the gate line 212 and the data line 214. The second portion 212b is disposed at a corner of every pixel region "P."

[0040] Even though not shown in FIG. 8, a thin film transistor (TFT) is connected to the gate line 212 and the data line 214 and a pixel electrode connected to the TFT is formed in the pixel region "P." The TFT "T" includes a gate electrode connected to the gate line 112, a source electrode connected to the data line 114 and a drain electrode spaced apart from the source electrode. A pixel electrode 116 connected to the drain electrode is formed in the pixel region "P."

[0041] The gate line 214 is tilted with respect to a virtual line perpendicular to the data line 214. Accordingly, the gate line 214 is not perpendicular to the data line 214 and an angle between the gate line 212 and the data line 214 is not 90°. For example, the angle between the gate line 212 and the data line 214 may be about 90°+θ2, where θ2 is a tilt angle within a range of about 0° to about 10°. In addition, a tilt direction of the gate line 214 may be in the opposite direction with respect to a virtual line perpendicular to the data line 214 in other embodiments. As a result, the gate line 212 may cross the data line 214 with a cross angle within ranges of about 80° to about 90° and about 90° to about 100°, such as a range of about 80° to about 100° that does not include 90°. Furthermore, a color filter layer of an LCD device may also have a parallelogrammic shape corresponding to the pixel region "P."

[0042] In embodiments of the present invention shown in FIGS. 3 to 8, a periodicity of a gate line and a data line is with respect to each pixel region. In another embodiment, a gate line and a data line may be disposed to have a periodicity with respect to two or more pixel regions.

[0043] FIG. 9 is a plan view showing an array substrate for a liquid crystal display device according to an embodiment of the present invention. As shown in FIG. 9, a gate line 312 is formed on a substrate (not shown) along a first direction and a data line 314 is formed along a second

direction. The gate line **312** and the data line **314** cross each other to define a pixel region "P1" or "P2." In addition, the gate line **312** has a straight shape and the data line **314** has a zigzag shape. The data line **314** includes a first portion **314a** tilted with respect to a virtual line perpendicular to the gate line **312** and a second portion **314b** parallel to the gate line **312**. The second portion **314b** is disposed for every two pixel regions "P1" and "P2" along the second direction.

[0044] Accordingly, a periodicity of the zigzag shape for the data line **314** corresponds to the two adjacent pixel regions "P1" and "P2" along the second direction. As a result, each of the adjacent pixel regions "P1" and "P2" has a parallelogrammic shape and the two adjacent pixel regions "P1" and "P2" together as a whole also have a parallelogrammic shape.

[0045] The second portion **314b** overlaps the gate line **312** in FIG. 9. However, the second portion **314b** does not have to overlap the gate line **312** in other embodiments. Accordingly, the second portion **314b** can be separated from the gate line **312** in a plan view to minimize a signal delay due to a parasitic capacitance between the gate line **312** and the data line **314**.

[0046] FIG. 10 is a plan view showing an array substrate for a liquid crystal display device according to an embodiment of the present invention. As shown in FIG. 10, a gate line **412** is formed on a substrate (not shown) along a first direction and a data line **414** is formed along a second direction. The gate line **412** and the data line **414** cross each other to define a pixel region "P1" or "P2." The gate line **412** has a zigzag shape and the data line **414** has a straight shape. The gate line **412** includes a first portion **412a** tilted with respect to a virtual line perpendicular to the data line **414** and a second portion **412b** parallel to the data line **414**. The second portion **412b** is disposed for every two adjacent pixel regions "P1" and "P2" along the first direction. Moreover, since a periodicity of the zigzag shape for the gate line **412** corresponds to every two adjacent pixel regions "P1" and "P2" along the first direction, each of the adjacent pixel regions "P1" and "P2" has a parallelogrammic shape and the two adjacent pixel regions "P1" and "P2" together as a whole also have a parallelogrammic shape.

[0047] The second portion **412b** overlaps the data line **414** in FIG. 10. However, the second portion **412b** does not have to overlap the data line **414** in other embodiments. Accordingly, the second portion **412b** may be separated from the data line **414** in a plan view to minimize a signal delay due to a parasitic capacitance between the gate line **412** and the data line **414**.

[0048] Although not shown in FIGS. 9 and 10, the gate line **312** and the data line **314** have a crossing angle within ranges of about 80° to about 90° and about 90° to about 100°, such as a range of about 80° to about 100° not including 90°, and the gate line **412** and the data line **414** can have a crossing angle within ranges of about 80° to about 90° and about 90° to about 100°, such as a range of about 80° to about 100° not including 90°. In addition, the data line **314** is tilted with respect to a virtual line perpendicular to the gate line **312** with a tilt angle within a range of about 0° to about 10° in FIG. 9, and the gate line **412** is tilted with respect to a line perpendicular to the data line **414** with a tilt angle within a range of about 0° to about 10° in FIG. 10. Thus, in an LCD device according to embodiments of the

present invention, since a gate line is not perpendicular to a data line, an interference pattern (moire phenomenon) due to a periodicity of the gate line and the data line is prevented and display quality of the LCD device is improved.

[0049] It will be apparent to those skilled in the art that various modifications and variations can be made in the array substrate and the liquid crystal display device using the same of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An array substrate for a liquid crystal display device, comprising:

a gate line on a substrate along a first direction;

a data line along a second direction and crossing the gate line, the crossing of the data line and the gate line defining a pixel region having a parallelogrammic shape;

a thin film transistor connected to the gate line and the data line; and

a pixel electrode in the pixel region and connected to the thin film transistor.

2. The substrate according to claim 1, wherein the gate line crosses the data line with a crossing angle greater than 80° and smaller than 100° but not equal to 90°.

3. The substrate according to claim 1, wherein the data line has a zigzag shape.

4. The substrate according to claim 3, wherein two adjacent pixel regions together along the second direction have a parallelogrammic shape as a whole.

5. The substrate according to claim 3, wherein the data line has a first portion tilted with respect to a virtual line perpendicular to the gate line and a second portion parallel to the gate line.

6. The substrate according to claim 5, wherein the second portion is separated from the gate line in a plan view.

7. The substrate according to claim 5, wherein the tilted first portion is disposed along two adjacent pixel regions.

8. The substrate according to claim 1, wherein the gate line has a zigzag shape.

9. The substrate according to claim 5, wherein two adjacent pixel regions together along the first direction have a parallelogrammic shape as a whole.

10. The substrate according to claim 8, wherein the gate line has a first portion tilted with respect to a virtual line perpendicular to the data line and a second portion parallel to the data line.

11. The substrate according to claim 10, wherein the second portion is separated from the data line in a plan view.

12. The substrate according to claim 8, wherein the tilted first portion is disposed along two adjacent pixel regions.

13. The substrate according to claim 1, wherein the pixel electrode includes a material for reflecting light that has an uneven surface to prevent mirror reflection.

14. The substrate according to claim 1, further comprising a reflecting plate in the pixel region, the reflecting plate having an open portion and the pixel electrode including a transparent conductive material.

15. A liquid crystal display device, comprising:

first and second substrates facing each other and spaced apart from each other;

a gate line on the first substrate along a first direction;

a data line along a second direction and crossing the gate line, the crossing of the data line and the gate line defining a pixel region having a parallelogrammic shape;

a thin film transistor connected to the gate line and the data line;

a pixel electrode in the pixel region and connected to the thin film transistor;

a color filter layer on the second substrate; and

a common electrode on the color filter layer.

16. The device according to claim 15, wherein the color filter layer includes one of a red, green and blue sub-color filters, the color filter layer corresponding to the pixel region and having a parallelogrammic shape.

17. The device according to claim 15, wherein the gate line crosses the data line with a cross angle greater than 80° and smaller than 100° but not equal to 90° .

18. The device according to claim 15, further comprising a reflecting plate in the pixel region, the reflecting plate having an open portion and the pixel electrode including a transparent conductive material.

* * * * *

专利名称(译)	阵列基板和使用其的液晶显示装置		
公开(公告)号	US20050140893A1	公开(公告)日	2005-06-30
申请号	US11/022755	申请日	2004-12-28
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG.PHILIPS LCD CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	HONG SOON KWANG		
发明人	HONG, SOON-KWANG		
IPC分类号	G02F1/1343 G02F1/1362		
CPC分类号	G02F1/136286 G02F1/134336		
优先权	1020030099427 2003-12-29 KR		
其他公开文献	US7697101		
外部链接	Espacenet USPTO		

摘要(译)

一种用于液晶显示装置的阵列基板，包括：沿第一方向在基板上的栅极线；沿着第二方向并与栅极线交叉的数据线，数据线和栅极线的交叉限定了具有平行四边形形状的像素区域；薄膜晶体管连接到栅极线 and 数据线；像素区域中的像素电极连接到薄膜晶体管。

