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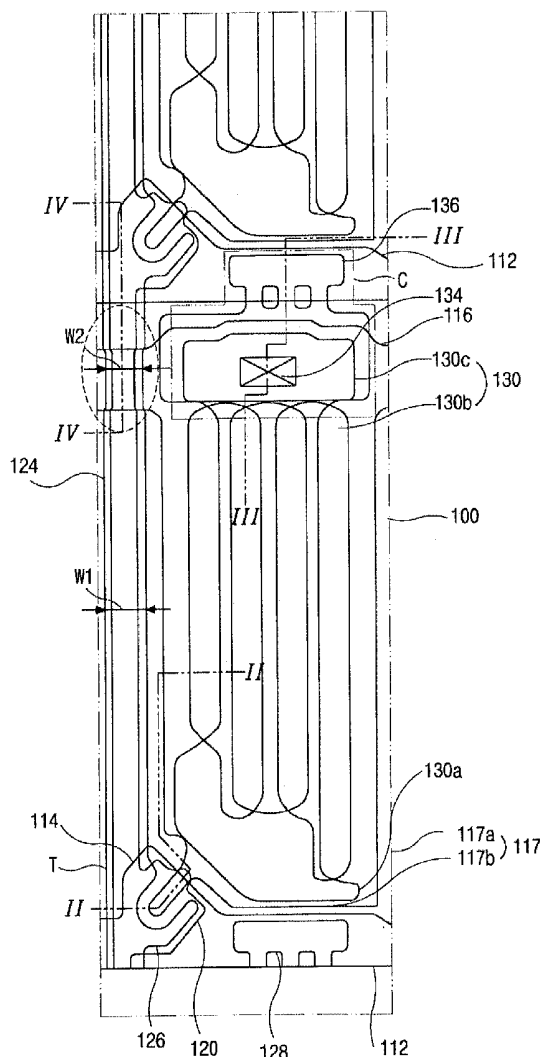
(19) **United States**(12) **Patent Application Publication**(10) **Pub. No.: US 2003/0117560 A1****Yang et al.**(43) **Pub. Date:****Jun. 26, 2003**(54) **ARRAY SUBSTRATE FOR IPS MODE
LIQUID CRYSTAL DISPLAY DEVICE AND
METHOD FOR FABRICATING THE SAME**(52) **U.S. Cl. 349/141**(76) **Inventors: Yun Suk Yang, Busan-city (KR);
Myung Ho Do, Chilgok-gun (KR)**(57) **ABSTRACT**

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An array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device includes a substrate having a plurality of pixel regions, a plurality of gate lines and a plurality of common lines in a horizontal direction. A plurality of data lines cross the gate line and the common line, the data line in a crossing portion between the data line and the gate line and between the data line and the common line having a substantially the same line width as the data line. A thin film transistor is at a crossing point of the gate and data lines. A pixel electrode has an extension portion, a plurality of vertical portions and a horizontal portion. A common electrode has a plurality of vertical portions and a horizontal portion. A transparent electrode pattern covers the horizontal portion of the pixel electrode.

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Dec. 24, 2001 (KR) 2001-84590

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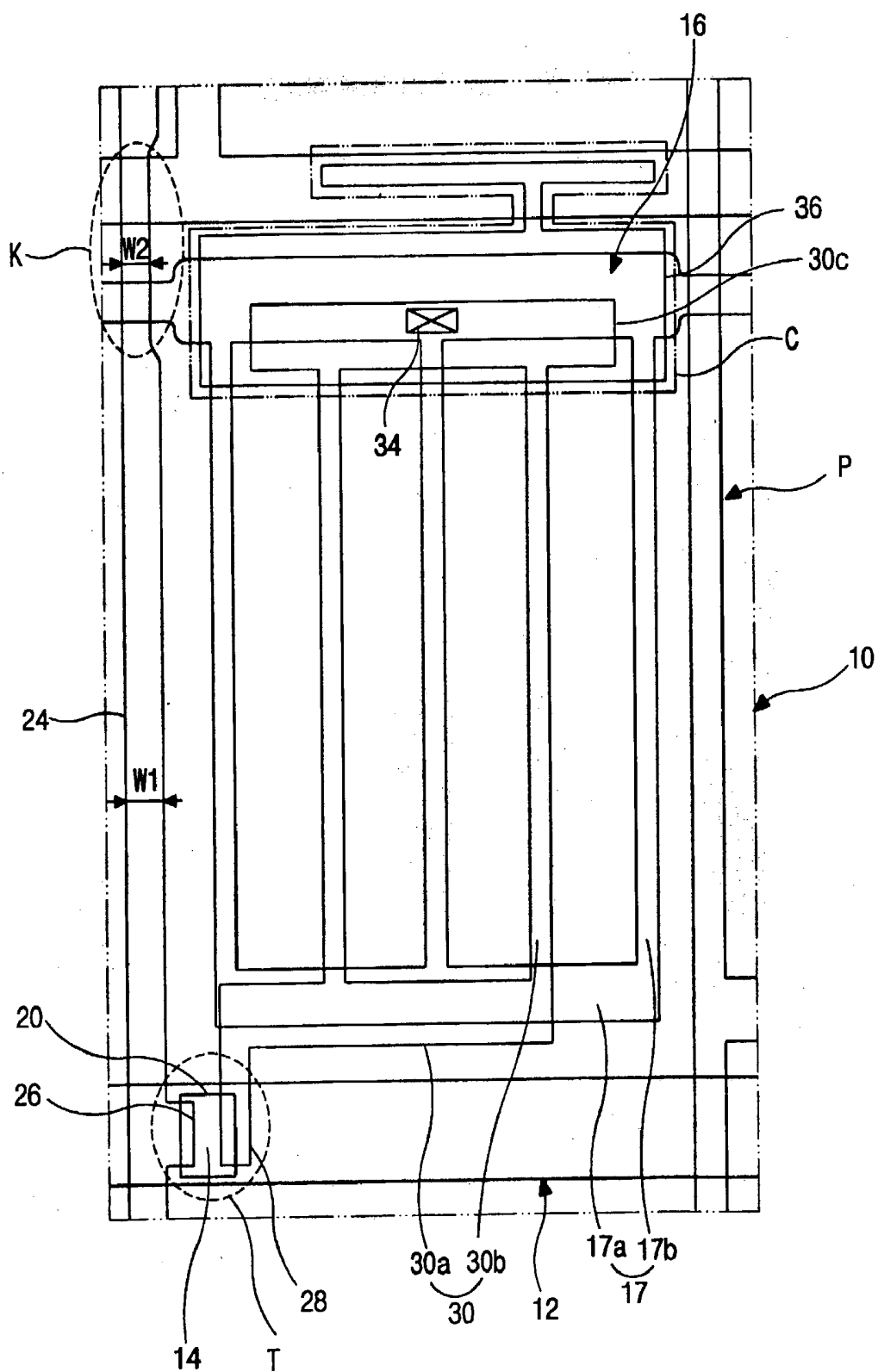


FIG. 1
(RELATED ART)

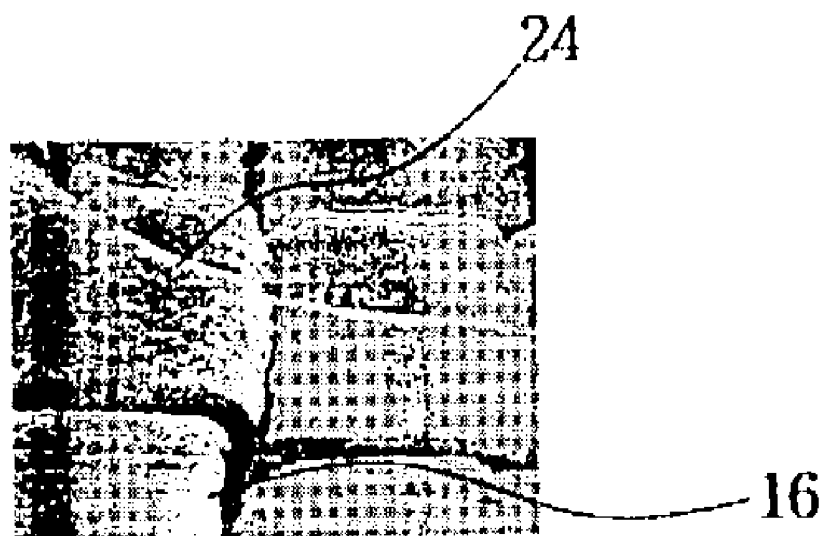


FIG. 2
(RELATED ART)

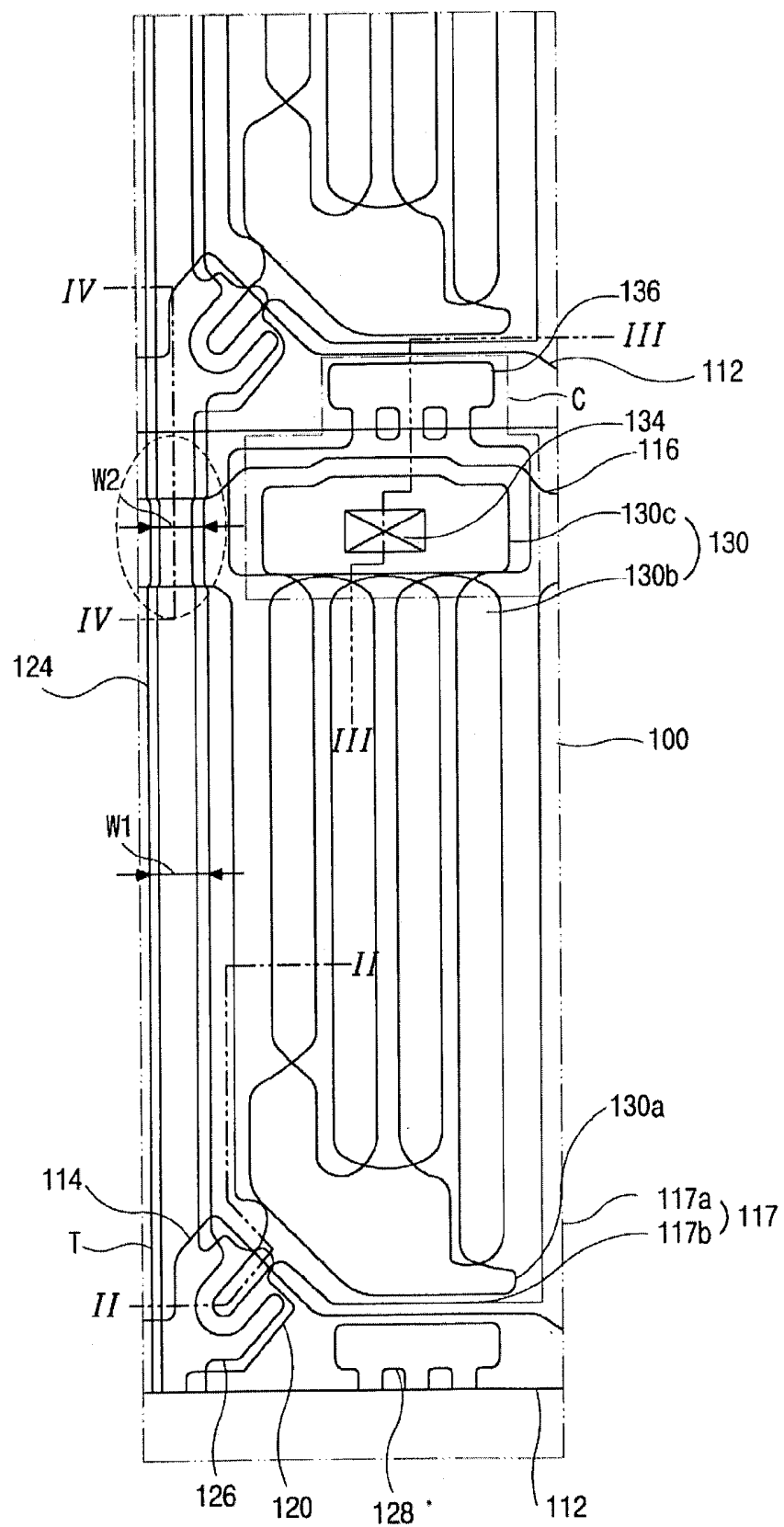


FIG. 3

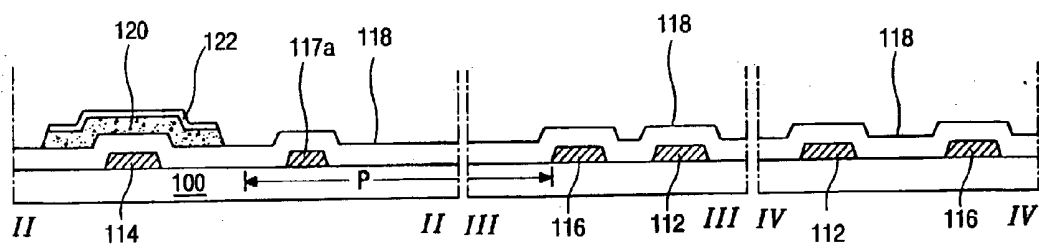


FIG. 4A

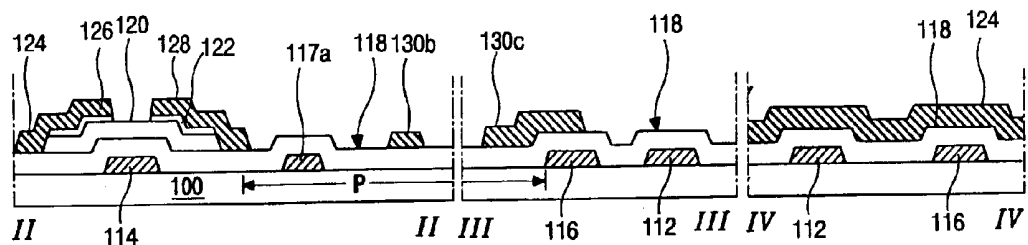


FIG. 4B

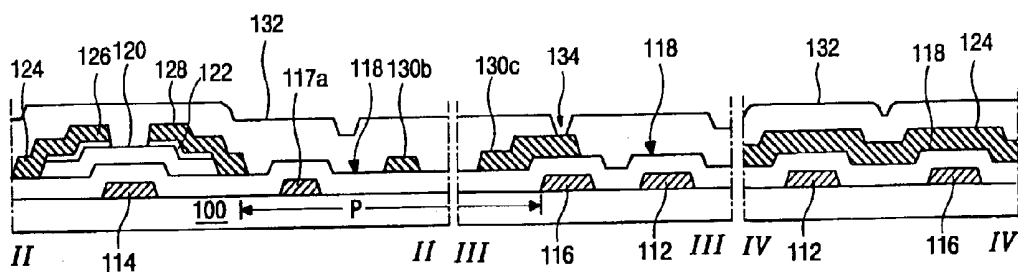


FIG. 4C

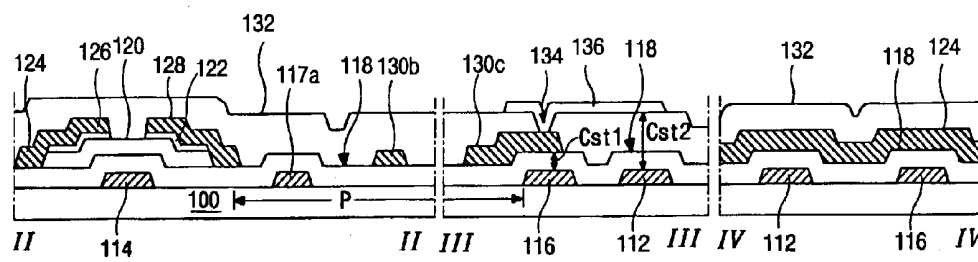


FIG. 4D

ARRAY SUBSTRATE FOR IPS MODE LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR FABRICATING THE SAME

[0001] This application claims the benefit of Korean Patent Application No. **2001-84590**, filed on Dec. 24, 2001 in Korea, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display (LCD) device and more particularly, to an array substrate for In-Plane Switching (IPS) mode liquid crystal display device and fabricating method for the same in order to prevent a break of a data line.

[0004] 2. Discussion of the Related Art

[0005] A typical liquid crystal display (LCD) device uses optical anisotropy and polarization properties of liquid crystal molecules. The liquid crystal molecules have a definite orientation order in alignment resulting from their thin and long shapes. The alignment direction of the liquid crystal molecules can be controlled by supplying an electric field to the liquid crystal molecules. In other words, as the alignment direction of the electric field is changed, the alignment of the liquid crystal molecules also changes. Because incident light is refracted to the orientation of the liquid crystal molecules due to the optical anisotropy of the aligned liquid crystal molecules, image data is displayed.

[0006] Active matrix LCDs, in which the thin film transistors and the pixel electrodes are arranged in the form of a matrix, are widely used because of their high resolution and superiority in displaying moving images. An array substrate for the in-plane switching (IPS) mode liquid crystal display (LCD) device and the fabricating method for the same will be described hereinafter with reference to the following figures.

[0007] **FIG. 1** is a plan view of a pixel of an array substrate for a related art in-plane switching (IPS) mode liquid crystal display (LCD) device. In **FIG. 1**, a plurality of gate lines **12**, common lines **16** and data lines **24** are formed on an array substrate **10** for the related art in-plane switching (IPS) mode liquid crystal display (LCD) device. The common line **16** is spaced apart from the gate line **12** and the data line **24** crosses the gate line **12** and the common line **16**. The data line **24** defines a pixel region "P" by crossing the gate line **12**. A thin film transistor is formed in a crossing point of the gate line **12** and the data line **24**. The thin film transistor includes a gate electrode **14**, an active layer **20**, a source electrode **26** and a drain electrode **28**. The active layer **20**, the source electrode **26** and the drain electrode **28** are formed over the gate electrode **14**. The source electrode **26** communicates with the data line **24** and the gate electrode **14** communicates with the gate line **12**. A pixel electrode **30** and a common electrode **17** are formed in the pixel region "P" in **FIG. 1**. The pixel electrode **30** is electrically connected to the drain electrode **28**. The common electrode **17** is formed parallel with the pixel electrode **30**. The pixel electrode **30** includes an extension portion **30a**, a plurality of vertical portions **30b** and a horizontal portion **30c**. The extension portion **30a** is extended from the drain electrode **28** and the plurality of the vertical portions **30b** is vertically

extended from the extension portion **30a**. The vertical portions **30b** are spaced from each other. The horizontal portion **30c** connects the vertical portions **30b** into one portion. The common electrode **17** includes a plurality of vertical portions **17b** and a horizontal portion **17a**. The vertical portions **17b** are vertically extended from the common line **16** and arranged in an alternating order with the vertical portions **30b** of the pixel electrode **30**. The horizontal portion **17a** connects the plurality of the vertical portions **17b** into one portion. The vertical portion **17b** of the common electrode **17** is spaced apart from the data line **24**. A transparent electrode pattern **36** contacts the horizontal portion **30c** of the pixel electrode **30** through a contact hole **34**. The transparent electrode pattern **36** is formed over the gate line **12** adjacent to the common line **16** and extended to the gate line **12**. An auxiliary storage capacitor "C" is formed over the gate line **12** and the common line **16** and forms a dual storage capacitor structure. A line width **W2** of the data line **24** in a portion where the data line **24** crosses the gate line **12** and the common line **16** is narrower than a line width **W1** of the data line **24** in other areas. The reason is to minimize a fluctuation of the storage capacitance by reducing an overlapped area between the data line **24** and the gate line **12** and between the data line **24** and the common line **16**. However, the line width **W2** of the data line **24**, which is patterned in a crossing portion "K" cannot overcome a step difference in the crossing portion "K". Accordingly, the data line **24** may be severed owing to the step difference in the crossing portion "K".

[0008] **FIG. 2** is a microphotograph of "K" portion of **FIG. 1** illustrating a severing of the data line in a crossing portion between the data line **24** and the common line **16**. The microphotograph illustrates that the data line **24** is severed in the crossing portion "K" between the data line and the common line because the data line **24** cannot overcome the step difference between the data line **24** and the common line **16**. The array substrate **10** that has a severed data line **24** is not available and this subsequently decreases a manufacturing yield.

SUMMARY OF THE INVENTION

[0009] Accordingly, the present invention is directed to an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device and method for fabricating the same that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

[0010] An advantage of the present invention is to provide the array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device in order to prevent a data line from being severed owing to a step difference between the data line and a common line.

[0011] Another advantage of the present invention is to provide a fabricating method for the array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device in order to prevent a data line from being severed owing to a step difference between the data line and a common line.

[0012] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and

attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0013] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device comprises a substrate including a plurality of pixel regions; a plurality of gate lines and a plurality of common lines in a horizontal direction; a plurality of data lines crossing the gate line and the common line, the data line in a crossing portion between the data line and the gate line and between the data line and the common line having a substantially same line width as the data line; a thin film transistor at a crossing point of the gate and data lines; a pixel electrode having an extension portion, a plurality of vertical portions and a horizontal portion; a common electrode having a plurality of vertical portions and a horizontal portion; and a transparent electrode pattern covering the horizontal portion of the pixel electrode. The gate line and the common line are formed on a same layer using the same material. The gate line and the common line include one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo) and chromium (Cr). The common line and the horizontal portion of the pixel electrode have an interposed insulation layer and form a first storage capacitor. The transparent electrode pattern contacting the horizontal portion of the pixel electrode and the gate line have an interposed insulation layer and form a second storage capacitor. The source electrode has an U-shape. The active layer is extended under the data line. The line width of the data line is between $8\ \mu\text{m}$ to $10\ \mu\text{m}$.

[0014] A fabrication method of an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device comprises forming a plurality of gate lines and a plurality of common lines on a substrate; forming a plurality of data lines crossing the gate line and the common line, the data line in a crossing portion between the data line and the gate line and between the data line and the common line having a substantially same line width as the data line; forming a thin film transistor at a crossing point of the gate and data lines; forming a pixel electrode having an extension portion, a plurality of vertical portions and a horizontal portion; forming a common electrode having a plurality of vertical portions and a horizontal portion; and forming a transparent electrode pattern covering the horizontal portion of the pixel electrode.

[0015] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0017] In the drawings:

[0018] FIG. 1 is a plan view of a pixel of an array substrate for a related art in-plane switching (IPS) mode liquid crystal display (LCD) device;

[0019] FIG. 2 is a microphotograph of K portion of FIG. 1 illustrating a severing of a data line in a crossing portion between the data line and a common line;

[0020] FIG. 3 is a plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to the present invention; and

[0021] FIGS. 4A to 4D are cross-sectional views taken along II-II, III-III and IV-IV of FIG. 3 illustrating a fabrication process according to a fabrication sequence of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0022] Reference will now be made in detail to embodiment of the present invention, example of which is illustrated in the accompanying drawings.

[0023] FIG. 3 is a plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to the present invention. In FIG. 3, a plurality of gate lines 112 and a plurality of common lines 116 are formed on an array substrate 100 in a horizontal direction. The common line 116 is parallel with the gate line 112 and spaced apart from the gate line 112. A data line 124 crosses the gate line 112 and the common line 116 and defines a pixel region "P" by crossing the gate line 112. Unlike the related art, a line width W2 of the data line 124 in a crossing portion between the data line 124 and the gate line 112 and between the data line 124 and the common line 116 is substantially the same as a line width W1 of the data line 124 in other areas according to the present invention. The line width W1 and W2 are patterned to have a width ranging from $8\ \mu\text{m}$ ~ $10\ \mu\text{m}$. A thin film transistor "T" is formed near the crossing point of the gate line 112 and the data line 124. The thin film transistor "T" includes a gate electrode 114, a semiconductor layer 120, a source electrode and a drain electrode 128. The source electrode 126 communicates with the data line 124 and the gate electrode 114 communicates with the gate line 112. The source electrode 126 has a U-shape and surrounds the drain electrode 128 that is spaced apart from the source electrode 126. A semiconductor line 121 is formed under the data line 124. The semiconductor line 121 is extended from the semiconductor layer 120 along the data line 124 in order to improve an adhesion property of the data line 124. A pixel electrode 130 and a common electrode 117 are formed in the pixel region "P". The pixel electrode 130 is connected to the drain electrode 128. The common electrode 117 is arranged in an alternating pattern with the pixel electrode 130 and connected to the common line 116. The pixel electrode 130 includes an extension portion 130a, a vertical portion 130b and a horizontal portion 130c. The extension portion 130a is extended from the drain electrode 128 and a plurality of vertical portions 130b is vertically extended from the extension portion 130a. The plurality of the vertical portions 130b is spaced from each other. The horizontal portion 130c connects the plurality of the vertical portions 130b into one portion. The common electrode 117 includes a plurality of vertical portions 117b and a horizontal portion 117a. The plurality of vertical portions 117b is vertically extended from the common line 116 and arranged in an alternating pattern with the vertical portions 130b of the pixel electrode

130. The horizontal portion **117a** connects the plurality of vertical portions into one portion. A transparent electrode pattern **136** contacts the horizontal portion **130c** of the pixel electrode **130** through a contact hole **134**. The transparent electrode pattern **136** is formed over the gate line **112** adjacent to the common line **116** and extended to the gate line **112**. A storage capacitor "C" is formed over the gate line **112** and the common line **116** and forms a dual storage capacitor structure. If the line width **W2** of the data line **124** in the crossing portion of the data line **124** and the common line **116** is formed to have substantially the same width of about $8\text{ }\mu\text{m}$ – $10\text{ }\mu\text{m}$ as the line width **W1** of the data line **124** in the pixel region "P", a fluctuation of a storage capacitance of the storage capacitor "C" does not affect the driving of a liquid crystal panel, which is generated by an overlapped area between the data line **124** and the gate line **112** and between the data line **124** and the common line **116**.

[0024] A fabrication method of an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device will be described hereinafter with reference to figures. **FIGS. 4A** to **4C** are cross-sectional views taken along II-II, III-III and IV-IV of **FIG. 3** illustrating a fabrication process according to a fabrication sequence of the present invention. In **FIG. 4A**, the gate line **112**, the common line **116** and the common electrode **117** are formed on the array substrate **100** by depositing and patterning one of a conductive metal material including aluminum (Al), aluminum alloy (Al alloy) such as aluminum neodymium (AlNd), chromium (Cr), molybdenum (Mo) and tungsten (W), for example. The gate electrode **114** is also formed at the same time with the gate line **112**. The common line **116** is spaced apart from the gate line **112** and parallel with the gate line **112**. As stated above, the common electrode **117** includes the plurality of vertical portions **117b** and the horizontal portion **117a**. The vertical portions **117b** are vertically extended from the common line **116** and the horizontal portion **117a** connects the vertical portions **117b** into one portion. A gate insulating layer **118** is then formed on the substrate **100** by depositing inorganic insulating material such as silicon nitride (SiNx) or silicon oxide (SiO₂), for example. A semiconductor layer **120** and **122** and a semiconductor line **121** are subsequently formed on the substrate **100** by depositing and patterning amorphous silicon (a-Si:H) and then doped amorphous silicon (n+a-Si:H or p+a-Si:H). The semiconductor layer comprises an active layer **120**, which is formed using amorphous silicon (a-Si:H), and an ohmic contact layer **122**, which is formed using doped amorphous silicon (n+a-Si:H or p+a-Si:H).

[0025] In **FIG. 4B**, the data line **124**, the source electrode **126**, the drain electrode **128** and the pixel electrode **130** are formed on the substrate **100** by depositing and patterning one of a conductive metal material including aluminum (Al), aluminum alloy (Al alloy) such as aluminum neodymium (AlNd), chromium (Cr), molybdenum (Mo) and tungsten (W), for example. The data line **124** defines the pixel region "P" by crossing the gate line **112**. The source electrode **126** is formed by being extended from the data line **124** and overlapped with a part of the semiconductor layer **120** and **122**. The drain electrode **128** is spaced apart from the source electrode **126**. The pixel electrode **130** includes the extension portion **130a**, the plurality of vertical portions **130b** and the horizontal portion **130c** as stated previously. As stated above, the line width **W2** of the data line **124** in the crossing portion between the data line **124** and the gate line **112** and

between the data line **124** and the common line **116** is $8\text{ }\mu\text{m}$ – $10\text{ }\mu\text{m}$. This line width **W2** of the data line **124** is about the same as the line width **W1** of the data line **124** in the pixel region "P". That is, the line width **W2** of the data line **124** near in the crossing portion between the data line **124** and the gate line **112** and between the data line **124** and the common line **116** is enlarged unlike the related art array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device. The active layer **120** is exposed by etching the ohmic contact layer **122** between the source electrode **126** and the drain electrode **128**.

[0026] In **FIG. 4C**, a passivation layer **132** is formed on the substrate **100** by depositing one of an organic insulating material including benzocyclobutene (BCB) and acryl-based resin, for example. The passivation layer **132** may be formed on the substrate **100** by depositing one of an inorganic insulating material including silicon nitride (SiNx) and silicon oxide (SiO₂), for example. A storage contact hole **134**, which exposes a part of the horizontal portion **130c** of the pixel electrode **130**, is formed by patterning the passivation layer **132**.

[0027] In **FIG. 4D**, a transparent electrode pattern **136** is over the common line **116** and the gate line **112**. The transparent electrode pattern **136** contacts the exposed horizontal portion **130c** of the pixel electrode **130** and is extended to the gate line **112**. A dual storage capacitor is formed in this array substrate structure as shown in **FIG. 4D**. The dual storage capacitor includes a first storage capacitor C_{St1} and a second storage capacitor C_{St2} . The common line **116** serves as a first capacitor electrode and the horizontal portion **130c** of the pixel electrode **130** serves as a second capacitor electrode in the first storage capacitor C_{St1} . The transparent electrode pattern **136** serves as a first capacitor electrode and the gate line **112**, which is overlapped with the transparent electrode pattern **136**, serves as a second capacitor electrode in the second storage capacitor C_{St2} .

[0028] In the present invention, a line width of a data line in a crossing portion between the data line and a gate line and between the data line and the common line is widened.

[0029] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device, comprising:

- a substrate having a plurality of pixel regions;
- a plurality of gate lines and a plurality of common lines in a horizontal direction;
- a plurality of data lines crossing the gate line and the common line, the data line in a crossing portion between the data line and the gate line and between the data line and the common line having a substantially same line width as the data line;
- a thin film transistor at a crossing point of the gate and data lines;

a pixel electrode having an extension portion, a plurality of vertical portions and a horizontal portion;

a common electrode having a plurality of vertical portions and a horizontal portion; and

a transparent electrode pattern covering the horizontal portion of the pixel electrode.

2. The array substrate according to claim 1, wherein the gate line and the common line are formed on a same layer using the same material.

3. The array substrate according to claim 1, wherein the gate line and the common line include one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo) and chromium (Cr).

4. The array substrate according to claim 1, wherein the common line and the horizontal portion of the pixel electrode have an interposed insulation layer and form a first storage capacitor.

5. The array substrate according to claim 1, wherein the transparent electrode pattern contacting the horizontal portion of the pixel electrode and the gate line have an interposed insulation layer and form a second storage capacitor.

6. The array substrate according to claim 1, wherein the thin film transistor includes a gate electrode, an active layer and source and drain electrodes.

7. The array substrate according to claim 6, wherein the source electrode has an U-shape.

8. The array substrate according to claim 6, wherein the active layer is extended under the data line.

9. The array substrate according to claim 1, wherein the line width of the data line is between about 8 μm to about 10 μm .

10. The array substrate according to claim 1, wherein the transparent electrode pattern contacts the horizontal portion of the pixel electrode.

11. A method for fabricating an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device, comprising:

forming a plurality of gate lines and a plurality of common lines on a substrate;

forming a plurality of data lines crossing the gate line and the common line, the data line in a crossing portion between the data line and the gate line and between the

data line and the common line having a substantially same line width as the data line;

forming a thin film transistor at a crossing point of the gate and data lines;

forming a pixel electrode having an extension portion, a plurality of vertical portions and a horizontal portion; forming a common electrode including a plurality of vertical portions and a horizontal portion; and

forming a transparent electrode pattern covering the horizontal portion of the pixel electrode.

12. The method according to claim 11, wherein the gate line and the common line are formed on a same layer using the same material.

13. The method according to claim 11, wherein the gate line and the common line are formed one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo) and chromium (Cr).

14. The method according to claim 11, wherein the common line and the horizontal portion of the pixel electrode have an interposed insulation layer and form a first storage capacitor.

15. The method according to claim 11, wherein the transparent electrode pattern contacting the horizontal portion of the pixel electrode and the gate line have an interposed insulation layer and form a second storage capacitor.

16. The method according to claim 11, wherein forming the thin film transistor at a crossing point of the gate and data lines includes:

forming a gate electrode on the substrate;

forming an active layer on the gate electrode; and

forming source and drain electrodes on the active layer.

17. The method according to claim 16, wherein the source electrode has an U-shape.

18. The method according to claim 16, wherein the active layer is extended under the data line.

19. The method according to claim 11, wherein the line width of the data line is between 8 μm to 10 μm .

20. The method according to claim 11, wherein the transparent electrode pattern contacts the horizontal portion of the pixel electrode.

* * * * *

专利名称(译)	用于IPS模式液晶显示装置的阵列基板及其制造方法		
公开(公告)号	US20030117560A1	公开(公告)日	2003-06-26
申请号	US10/320625	申请日	2002-12-17
[标]申请(专利权)人(译)	杨云SUK DO MYUNG HO		
申请(专利权)人(译)	杨云SUK DO MYUNG HO		
当前申请(专利权)人(译)	杨云SUK DO MYUNG HO		
[标]发明人	YANG YUN SUK DO MYUNG HO		
发明人	YANG, YUN SUK DO, MYUNG HO		
IPC分类号	G02F1/1343		
CPC分类号	G02F1/134363		
优先权	1020010084590 2001-12-24 KR		
其他公开文献	US6791652		
外部链接	Espacenet USPTO		

摘要(译)

一种用于面内切换 (IPS) 模式液晶显示 (LCD) 器件的阵列基板, 包括具有多个像素区域, 多条栅极线和多个水平方向的公共线的基板。多条数据线与栅极线和公共线交叉, 数据线在数据线和栅极线之间的交叉部分中以及数据线和公共线之间具有与数据线基本相同的线宽。薄膜晶体管位于栅极线和数据线的交叉点处。像素电极具有延伸部分, 多个垂直部分和水平部分。公共电极具有多个垂直部分和水平部分。透明电极图案覆盖像素电极的水平部分。

