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(54) ARRAY SUBSTRATE FOR IPS MODE LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR FABRICATING THE SAME

(76) Inventors: **Ik-Soo Kim**, Gunpo-si (KR); **Gee-Sung Chae**, Incheon-kwangyokshi (KR)

Correspondence Address:
Song K. Jung
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006 (US)

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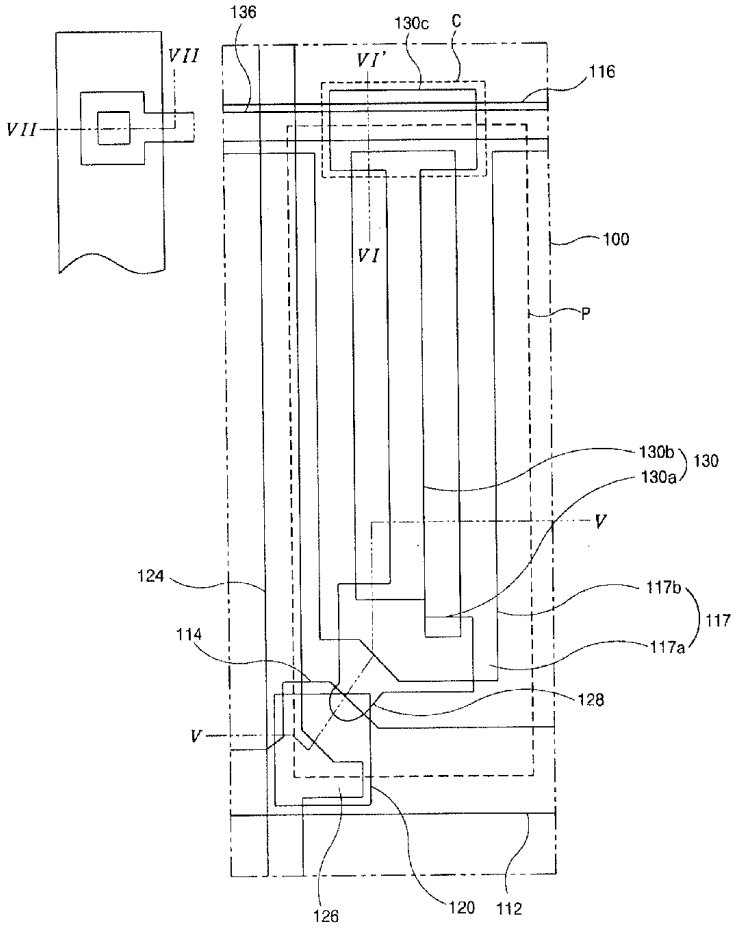
(57) **ABSTRACT**

An array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device includes a pixel electrode having an extension portion, a vertical portion and a horizontal portion, the extension portion being extended from the drain electrode to the pixel region, the vertical portion being vertically extended from the extension portion and the horizontal portion being over the common line and being connected to the vertical portion. The device includes a common electrode having a plurality of vertical portions and a horizontal portion, the plurality of the vertical portions being vertically extended from the common line and arranged in an alternating pattern with the vertical portion of the pixel electrode, the horizontal portion connecting the plurality of the vertical portions into one. An auxiliary line is over the horizontal portion of the pixel electrode and being overlapped with the common line.



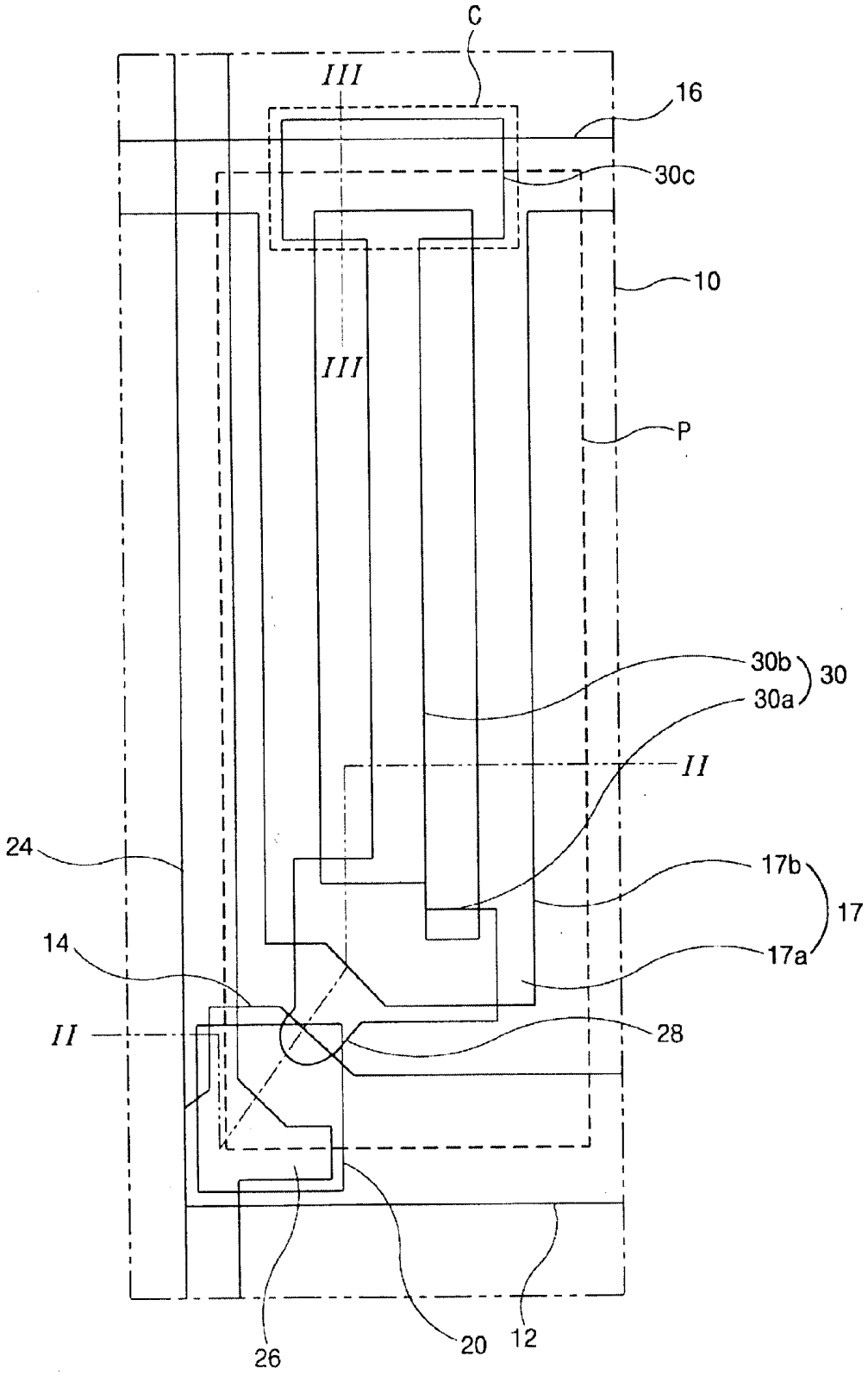


FIG. 1
(RELATED ART)

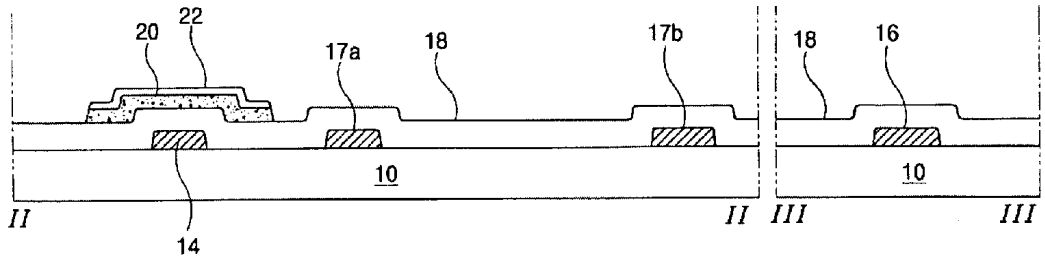


FIG. 2A
(RELATED ART)

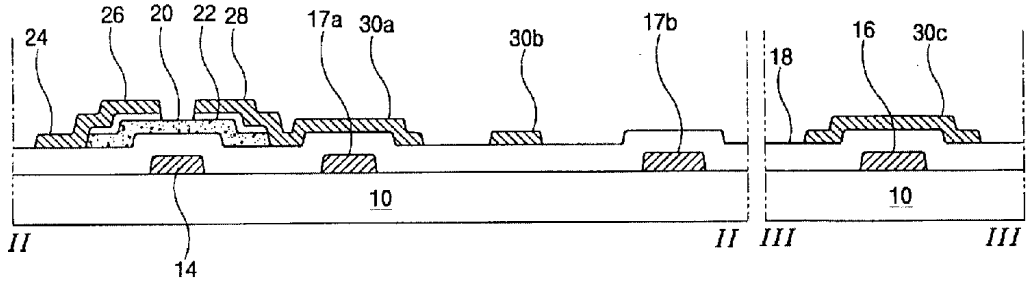


FIG. 2B
(RELATED ART)

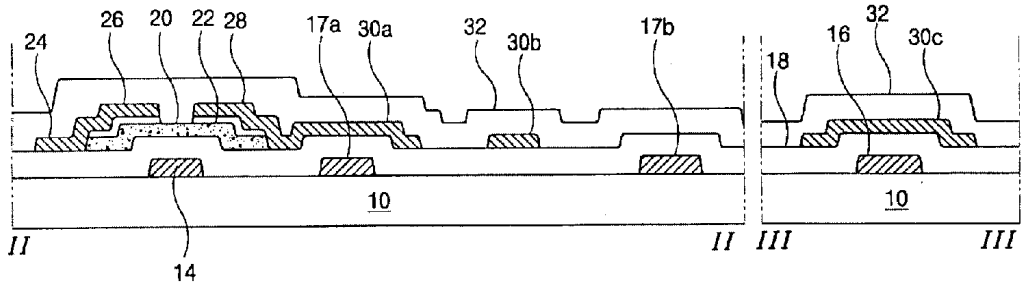


FIG. 2C
(RELATED ART)

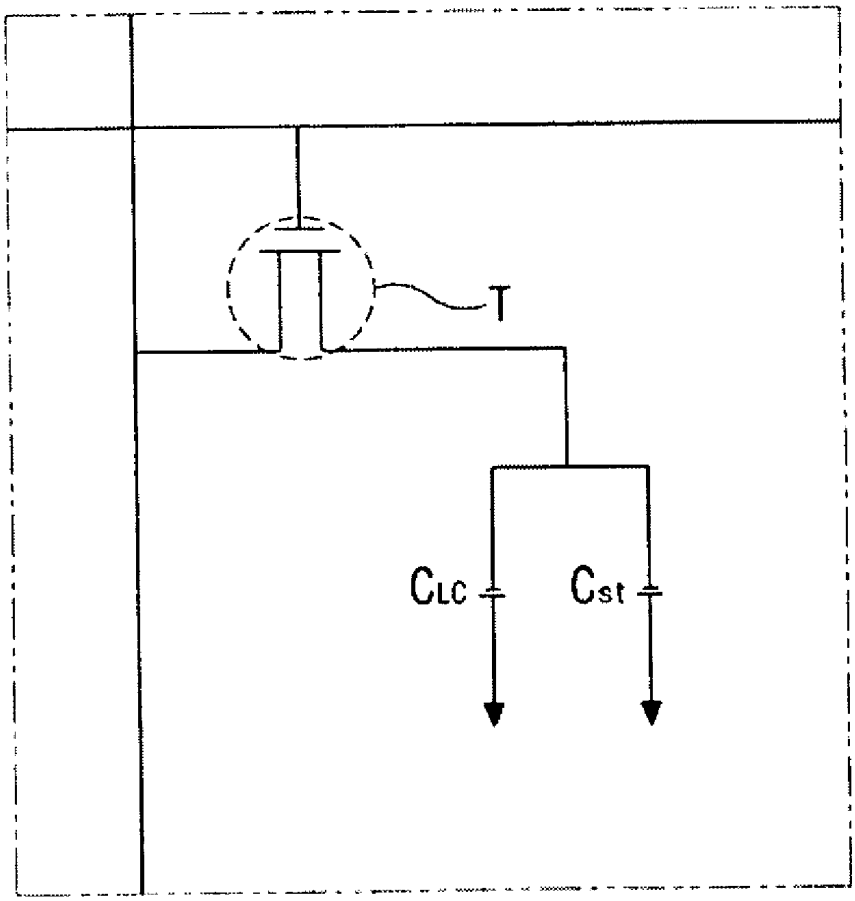


FIG. 3
(RELATED ART)

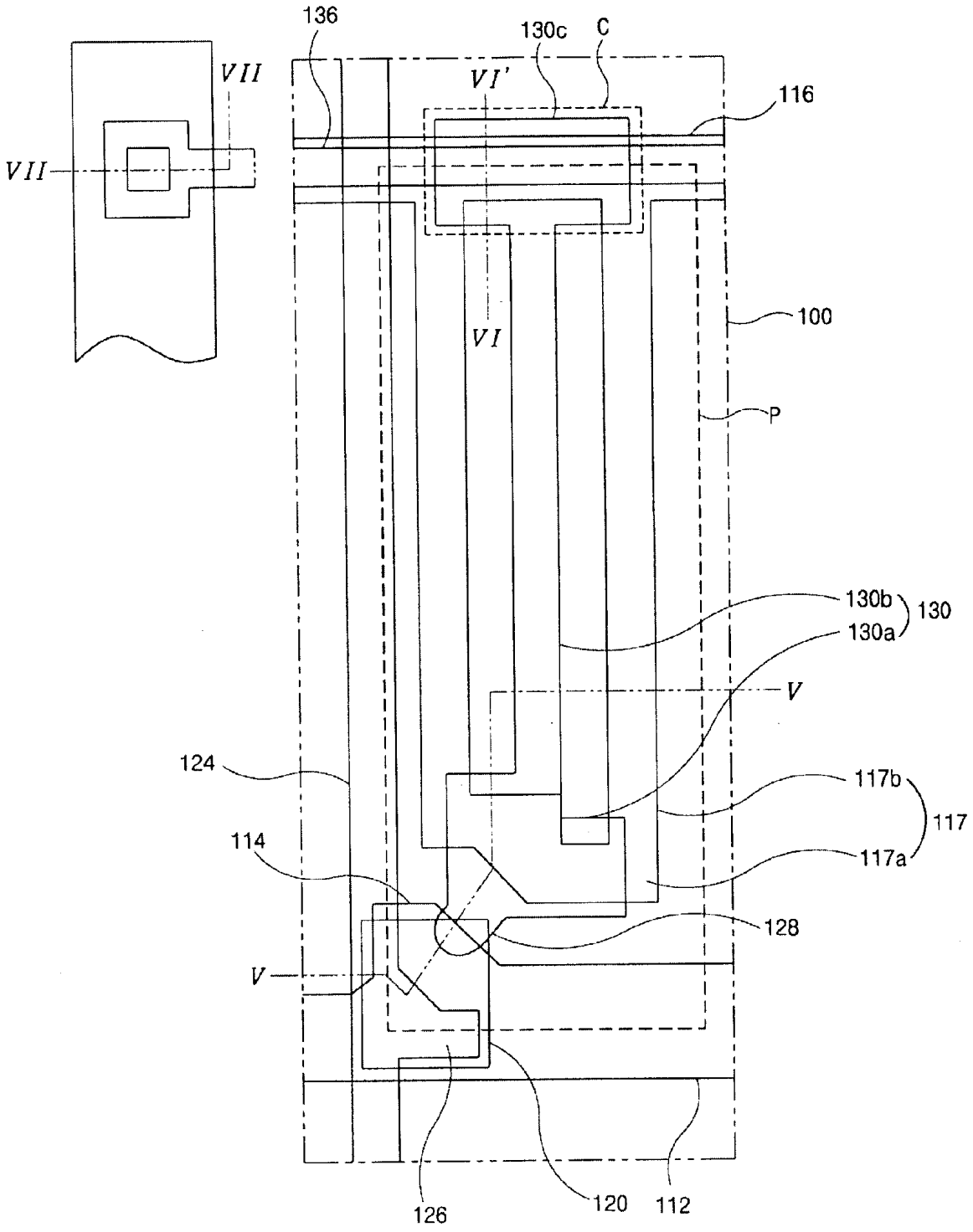

136
130c
C
VII
VI'
116
VII
100
VI
P
130b
130
130a
V
124
117b
117
114
117a
128
V
126
120
112

FIG. 4

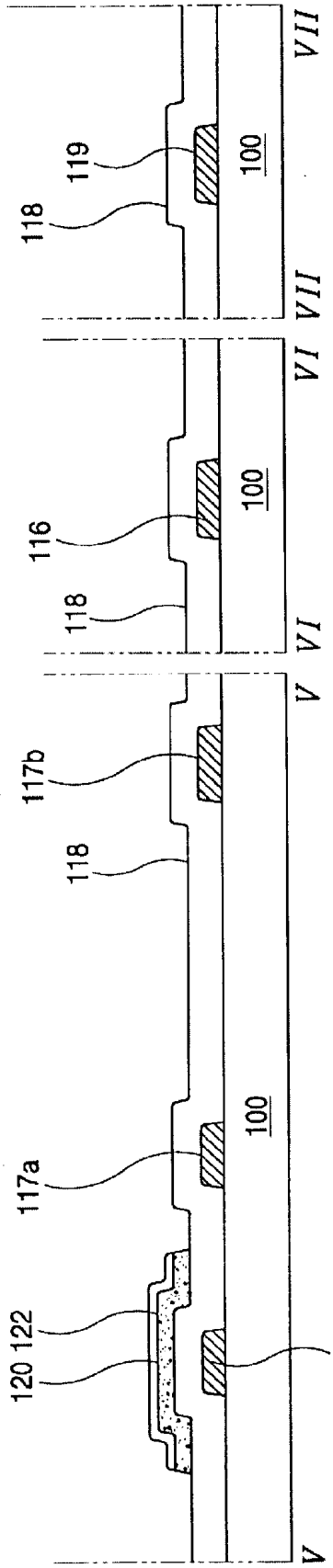

VII
119
118
100
VII
VI
116
118
100
VI
V
117b
118
100
117a
120 122
114
V

FIG. 5A

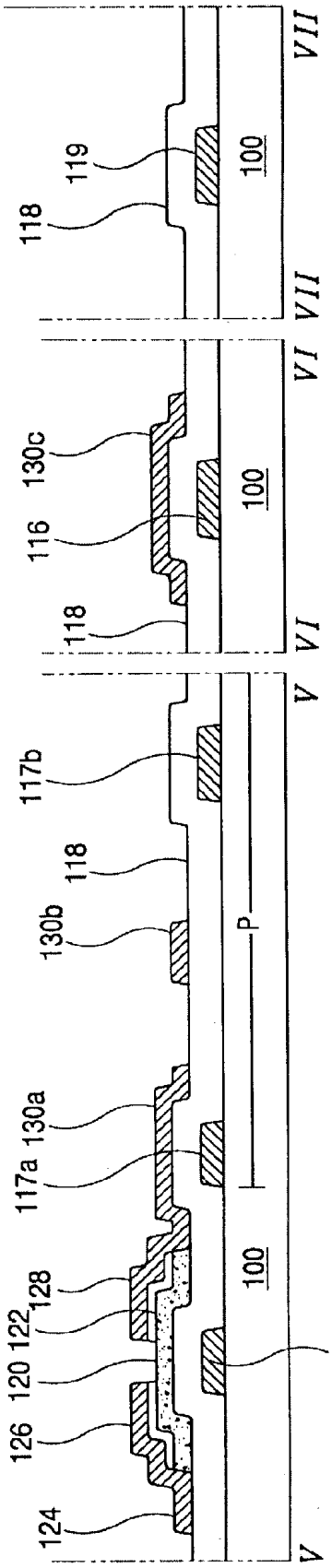

VII
119
118
100
VII
VI
130c
116
118
100
VI
V
117b
118
130b
P
130a
117a
128
122
120
126
124
100
114
V

FIG. 5B

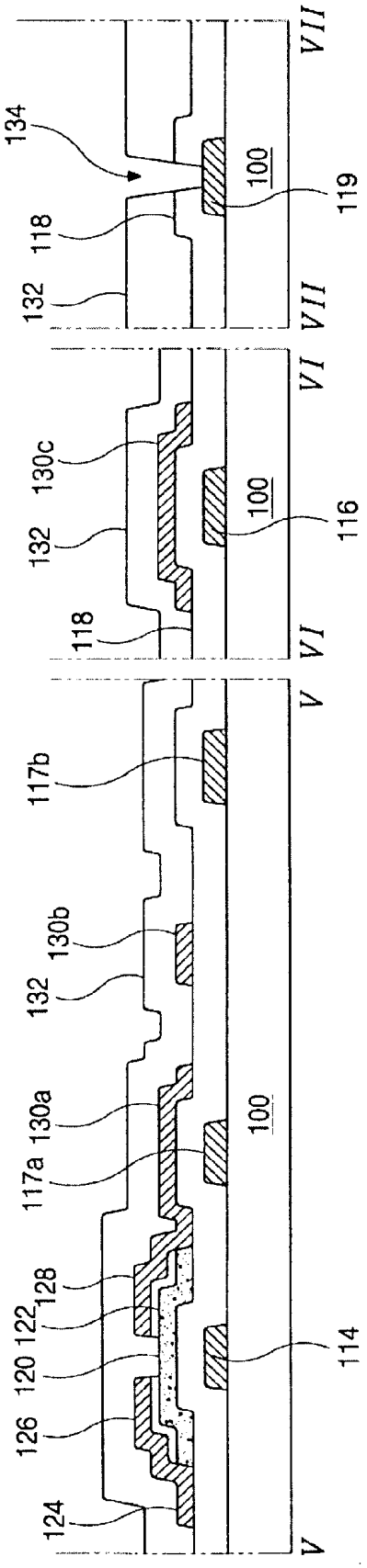

VII
134
100
119
118
132
VII
VI
130c
100
116
132
118
VI
V
117b
130b
132
100
130a
117a
128
122
120
126
124
114
V

FIG. 5C

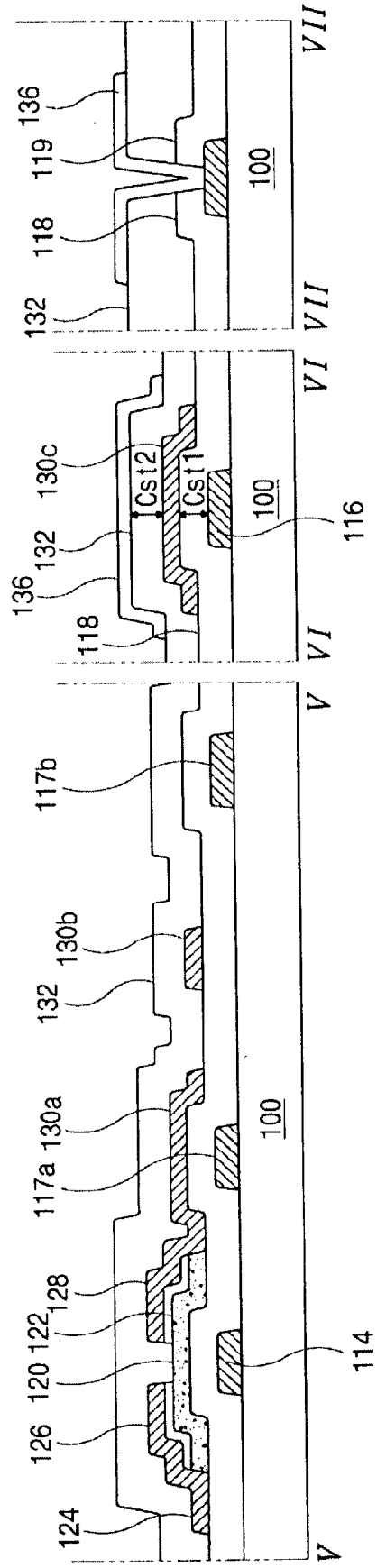

VII
136
119
118
132
100
VII
VI
130c
Cst2
Cst1
132
136
118
100
116
VI
V
117b
130b
132
130a
117a
128
122
120
126
124
100
114
V

FIG. 5D

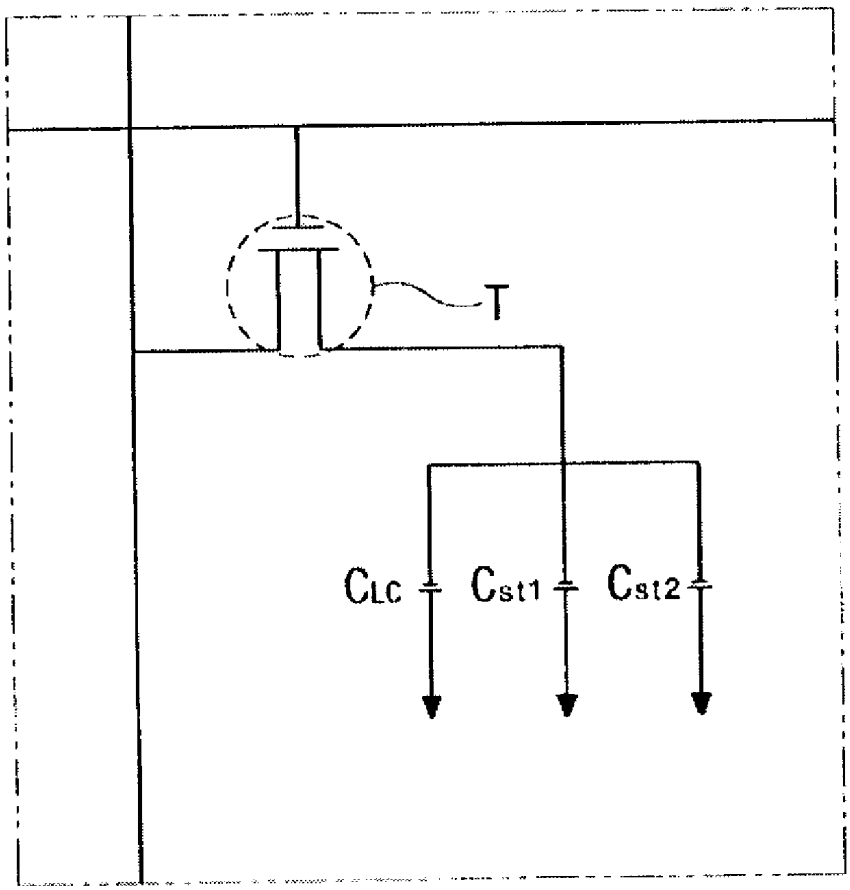


FIG. 6

ARRAY SUBSTRATE FOR IPS MODE LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR FABRICATING THE SAME

[0001] This application claims the benefit of Korean Patent Application No. 2001-84259, filed on Dec. 24, 2001 in Korea, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display (LCD) device and more particularly, to an array substrate for In-Plane Switching (IPS) mode liquid crystal display device and fabricating method for the same in order to realize a minute pixel.

[0004] 2. Discussion of the Related Art

[0005] A typical liquid crystal display (LCD) device uses optical anisotropy and polarization properties of liquid crystal molecules. The liquid crystal molecules have a definite orientation order in alignment resulting from their thin and long shapes. The alignment direction of the liquid crystal molecules can be controlled by supplying an electric field to the liquid crystal molecules. In other words, as the alignment direction of the electric field is changed, the alignment of the liquid crystal molecules also changes. Because incident light is refracted to the orientation of the liquid crystal molecules due to the optical anisotropy of the aligned liquid crystal molecules, image data is displayed.

[0006] Currently, active matrix LCDs, in which the thin film transistors and the pixel electrodes are arranged in the form of a matrix, are widely used because of their high resolution and superiority in displaying moving images. An array substrate for the related art in-plane switching (IPS) mode liquid crystal display (LCD) device and the fabricating method for the same will be described hereinafter.

[0007] **FIG. 1** is a plan view of a pixel of an array substrate for a related art in-plane switching (IPS) mode liquid crystal display (LCD) device. As shown in the figure, a plurality of gate lines **12** and common lines **16** are horizontally formed on an array substrate **10** and they are spaced apart from each other. A plurality of data lines **24** is vertically formed on the array substrate **10** and cross the gate lines **12** and the common lines **16**. The data line **24** defines a pixel "P" by crossing the gate line **12**. A thin film transistor "T" is formed in a cross point of the gate line **12** and the data line **24**. The thin film transistor "T" includes a gate electrode **14**, an active layer **20**, a source electrode **26** and a drain electrode **28**. The active layer **20**, the source electrode **26** and the drain electrode **28** are formed over the gate electrode **14**. The gate electrode **14** communicates with the gate line **12** and the source electrode **26** communicates with the data line **24**. A pixel electrode **30** that communicates with the drain electrode **28** and a common electrode **17** that is parallel with the pixel electrode **30** are formed in the pixel region "P". The common electrode **17** communicates with the common line **16**. The pixel electrode **30** includes an extension portion **30***a*, a vertical portion **30***b* and a horizontal portion **30***c*. The extension portion **30***a* of the pixel electrode **30** is extended from the drain electrode **28** and the vertical portion **30***b* of the pixel electrode **30** is vertically extended from the extension portion **30***a*. The horizontal portion **30***c* of the pixel electrode **30** is formed over the common line **16** and connected to the vertical portion **30***b*. The common electrode **17** includes a horizontal portion **17***a* and a plurality of vertical portions **17***b*. The plurality of vertical portions **17***b* of the common electrode **17** is arranged in an alternating order with the vertical portion **30***b* of the pixel electrode **30**. The horizontal portion **17***a* of the common electrode **17** connects the plurality of the vertical portion **17***b* into one portion. An auxiliary storage capacitor "C" is formed in the pixel region "P". The auxiliary storage capacitor "C" uses a portion of the common line **16** as a first storage electrode and the horizontal portion of the pixel electrode **30***c* as a second storage electrode.

[0008] **FIGS. 2A** to **2C** are cross-sectional views taken along II-II and III-III of **FIG. 1** illustrating a fabrication process according to a fabrication sequence of the related art. In **FIG. 2A**, the gate line **12** of **FIG. 1** including the gate electrode **14**, the common line **16** and the common electrode **17** are formed on the substrate **10** by depositing and patterning conductive metal material such as aluminum (Al), aluminum neodymium (AlNd), chromium (Cr), molybdenum (Mo) or tungsten (W), for example. A gate insulating layer **18** is then formed on the substrate **10** by depositing inorganic insulating material such as silicon nitride (SiNx) or silicon oxide (SiO_2), for example. The active layer **20** and an ohmic contact layer **22** are formed on the gate insulating layer **18** by depositing and patterning amorphous silicon (a-Si:H) and doped amorphous silicon (n+a-Si:H or p+a-Si:H).

[0009] In **FIG. 2B**, the data line **24**, the source electrode **26**, the drain electrode **28** and the pixel electrode **30** are formed on the substrate **10** by depositing and patterning conductive metal material such as aluminum (Al), aluminum neodymium (AlNd), chromium (Cr), molybdenum (Mo) or tungsten (W), for example. The data line **24** defines the pixel region "P" by crossing the gate line **12** and the common line **16**. The source electrode **26** is formed by being extended from the data line **24** and partially overlapped with the active layer **20**. The drain electrode **28** is spaced apart from the source electrode **26**. The pixel electrode **30** comprises the extension portion **30***a*, the vertical portion **30***b* and the horizontal portion **30***c*. The horizontal portion **30***b* of the pixel electrode **30** is formed on the common line **16**. The active layer **20** portion between the source electrode **26** and the drain electrode **28** is exposed by etching the ohmic contact layer **22** between the source electrode **26** and the drain electrode **28**.

[0010] In **FIG. 2C, a** passivation layer **32** is formed on the substrate **10** by coating organic insulating material such as benzocyclobutene (BCB), for example, or by depositing inorganic insulating material such as silicon nitride (SiNx) or silicon oxide (SiO_2), for example.

[0011] **FIG. 3** is a circuit diagram of **FIG. 1**. A capacitor communicates with the thin film transistor "T" in series. The capacitor includes a liquid crystal capacitor (C_{LC}) and a storage capacitor (C_{ST}), which is connected in parallel to the liquid crystal capacitor (C_{LC}).

[0012] However, if the pixel structure stated above for the in-plane switching (IPS) mode liquid crystal display (LCD) device that drives a minute pixel, an area for the storage capacitor "C" is limited. Moreover, if the area for the storage capacitor "C" is designed to be larger in order to secure a

capacitance of the storage capacitor "C", an aperture ratio of the liquid crystal panel is decreased.

SUMMARY OF THE INVENTION

[0013] Accordingly, the present invention is directed to an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device and method for fabricating the same that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

[0014] An advantage of the present invention is to provide the array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device in order to secure enough auxiliary capacitance without enlarging an area of a storage capacitor "C".

[0015] Another advantage of the present invention is to provide a fabricating method for the array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device in order to secure enough auxiliary capacitance without enlarging an area of a storage capacitor "C".

[0016] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0017] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device comprises a substrate having a plurality of pixel regions, a plurality of gate lines and a plurality of common lines in a horizontal direction, the common line being spaced apart from the gate line; a plurality of data lines crossing the gate line and the common line; a thin film transistor at a cross point of the gate line and the data line, the thin film transistor having a gate electrode, an active layer, a source electrode and a drain electrode; a pixel electrode having an extension portion, a vertical portion and a horizontal portion, the extension portion being extended from the drain electrode to the pixel region, the vertical portion being vertically extended from the extension portion and the horizontal portion being over the common line and being connected to the vertical portion; a common electrode having a plurality of vertical portions and a horizontal portion, the plurality of the vertical portions being vertically extended from the common line and arranged in an alternating pattern with the vertical portion of the pixel electrode, the horizontal portion connecting the plurality of the vertical portions into one portion, and an auxiliary line over the horizontal portion of the pixel electrode and being overlapped with the common line.

[0018] The array substrate further comprises a dummy line, referred to as a common guard ring, in a non-display area of the substrate that communicates with the auxiliary line in order to apply a common voltage to the auxiliary line. The gate line, the common line and the dummy line are formed one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr). The common line and the horizontal portion of the pixel electrode having an insulating layer therebetween forms a first auxiliary storage capacitor and the horizontal portion of the pixel electrode and the auxiliary line having an insulating layer therebetween forms a second auxiliary storage capacitor.

[0019] A fabrication method of an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device comprises forming a plurality of gate lines, a plurality of common lines and a dummy line on an array substrate, the gate line and the common line being formed in a horizontal direction and spaced apart from each other, the dummy line being formed in a non-display area; forming a plurality of data lines crossing the gate line and the common line; forming a thin film transistor at a cross point of the gate line and the data line, the thin film transistor including a gate electrode, an active layer, a source electrode and a drain electrode; forming a pixel electrode having an extension portion, a vertical portion and a horizontal portion, the extension portion being extended from the drain electrode, the vertical portion being vertically extended from the extension portion and the horizontal portion being over the common line and connected to the vertical portion; forming a common electrode having a plurality of vertical portions and a horizontal portion, the plurality of the vertical portions being vertically extended from the common line and arranged in an alternating pattern with the vertical portion of the pixel electrode, the horizontal portion connecting the plurality of the vertical portions into one portion; and forming an auxiliary line over the horizontal portion of the pixel electrode, the auxiliary line being overlapped with the common line and one end of the auxiliary line communicating with the dummy line.

[0020] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWING

[0021] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0022] In the drawings:

[0023] **FIG. 1** is a plan view of a pixel of an array substrate for a related art in-plane switching (IPS) mode liquid crystal display (LCD) device;

[0024] **FIGS. 2A** to **2C** are cross-sectional views taken along II-II and III-III of **FIG. 1** illustrating a fabrication process according to a fabrication sequence of the related art;

[0025] **FIG. 3** is a circuit diagram of **FIG. 1**;

[0026] **FIG. 4 a** plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to the present invention;

[0027] **FIGS. 5A** to **5D** are cross-sectional views taken along V-V, VI-VI and VII-VII of **FIG. 4** illustrating a fabrication process according to a fabrication sequence of the present invention; and

[0028] **FIG. 6** is a circuit diagram of **FIG. 4**.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0029] Reference will now be made in detail to the illustrated embodiment of the present invention, which is illustrated in the accompanying drawings.

[0030] **FIG. 4 a** plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to the present invention.

[0031] As shown in the figure, the array substrate for the in-plane switching (IPS) mode liquid crystal display (LCD) device of the present invention includes a plurality of gate lines **112**, a plurality of common lines **116** and a plurality of data lines **124**. The gate line **112** and the common line **116** are spaced apart from each other and parallel with each other. The data line **124** vertically crosses the gate line **112** and the common line **116** and defines a pixel region "P" by crossing the gate line **112**. A thin film transistor, which includes a gate electrode **114**, an active layer **120**, a source electrode **126** and a drain electrode **128**, is formed in a crossing point of the gate line **112** and the data line **124**. The source electrode **126** communicates with the data line **124** and the gate electrode **114** communicates with the gate line **112**. A pixel electrode **130** and a common electrode **117** are formed in the pixel region "P". The pixel electrode **130** communicates with the drain electrode **128**. The common electrode **117** communicates with the common line **116** and is formed parallel to the pixel electrode **130**. The pixel electrode **130** includes an extension portion **130***a*, a vertical portion **130***b* and a horizontal portion **130***c*. The extension portion **130***a* of the pixel electrode **130** is extended from the drain electrode **128** and the vertical portion **130***b* of the pixel electrode **130** is vertically extended from the extension portion **130***a* of the pixel electrode **130**. The horizontal portion **130***c* of the pixel electrode **130** is positioned over the common line **116** and connected to the vertical portion **130***b*. The common electrode **117** includes a plurality of vertical portions **117***b* and a horizontal portion **117***a*. The vertical portions **117***b* of the common electrode **117** are vertically extended from the common line **116** and arranged in an alternating pattern with the vertical portion **130***b* of the pixel electrode **130***a*. The horizontal portion **117***a* of the common electrode **117** connects the plurality of the vertical portions **117***b* of the common electrode **117** into one portion. An auxiliary line **136** is further formed over the horizontal portion **130***c* of the pixel electrode **130** according to the present invention. The auxiliary line **136** is overlapped with the common line **116** and extended to a non-display area of the array substrate in order to electrically communicate with a dummy line **119** (not shown in **FIG. 4**). The dummy line **119** applies same voltage as the common line **116** to the auxiliary line **136**. A dual storage is subsequently formed that includes a first electrode, a second electrode and a third electrode. The common line **116** serves as the first electrode, the horizontal portion **130***c* of the pixel electrode **130** the second electrode and the auxiliary line **119** the third electrode. With this array structure of the present invention, an area for the storage capacitor "C" can be reduced and enough auxiliary capacitance can be secured.

[0032] A fabrication method of the in-plane switching (IPS) mode liquid crystal display (LCD) device according to the present invention will be described hereinafter with reference to **FIGS. 5A** to **5**D.

[0033] **FIGS. 5A** to **5**D are cross-sectional views taken along V-V, VI-VI and VII-VII of **FIG. 4** illustrating a fabrication process according to a fabrication sequence of the present invention. In **FIG. 5**A, the gate line **112** (not shown in **FIG. 5A**) including the gate electrode **114**, the common line **116** and the common electrode **117** are formed on a substrate **100** by depositing conductive metal material such as copper (Cu), aluminum (Al), aluminum alloy (Al alloy) like aluminum neodymium (AlNd), chromium (Cr), molybdenum (Mo) or tungsten (W), for example, and then by a first masking process. The common electrode **117** includes the plurality of vertical portions **117***b*, which is vertically extended from the common line **116**, and the horizontal portion **117***a*, which connects the plurality of the vertical portions **117***b* into one portion. The dummy line for applying common voltage to the auxiliary line **136** is further formed in the non-display area of the substrate **100**. A gate insulating layer **118** is then formed on the substrate **100** by depositing inorganic insulating material such as silicon nitride (SiNx) or silicon oxide (SiO_2), for example. An active layer **120** and a ohmic contact layer **122** is subsequently formed on the substrate **100** by depositing and patterning amorphous silicon (a-Si:H) and then doped amorphous silicon (n+a-Si:H or p+a-Si:H).

[0034] In **FIG. 5**B, the data line **124**, the source electrode **126**, the drain electrode **128** and the pixel electrode **130** are formed on the substrate **100** by depositing and patterning conductive metal material such as copper (Cu), aluminum (Al), aluminum alloy (Al alloy) like aluminum neodymium (AlNd), chromium (Cr), molybdenum (Mo) or tungsten (W), for example. The data line **124** crosses the gate line **112** and the common line **116**, and defines a pixel region "P" by crossing the gate line **112**. The source electrode **126** is extended from the data line **124** and overlapped with a part of the active layer **120**. The drain electrode **128** is spaced apart from the source electrode **126** on the active layer **120**. As stated above, the pixel electrode **130** includes the extension portion **130***a*, the vertical portion **130***b* and the horizontal portion **130***c*. The horizontal portion **130***c* of the pixel electrode **130** is formed over the common line **116**. A portion of the active layer **120** between the source electrode **126** and the drain electrode **128** is exposed by etching a portion of the ohmic contact layer **122** between the source electrode **126** and the drain electrode **128**.

[0035] In **FIG. 5C, a** passivation layer **132** is formed on the substrate **100** by depositing inorganic insulating material such as silicon nitride (SiNx) or silicon oxide (SiO_2), for example. A contact hole **134**, which exposes a part of the dummy line **119**, is formed by patterning the gate insulating layer **118** and the passivation layer **132**.

[0036] In **FIG. 5**D, the auxiliary line **136** is formed on the passivation layer **132** by depositing and patterning transparent conductive metal material such as Indium-Tin-Oxide (ITO) or Indium Zinc Oxide (IZO), for example. The auxiliary line **136** is overlapped with the common line **116** and one end of it communicates with the dummy line **119** in the non-display area of the substrate **100**. As shown in the figure, dual storage capacitor, which includes a first auxiliary storage capacitor C_{St1} and a second auxiliary storage capacitor C_{St2}, are formed under the structure of the array substrate

of the present invention. A part of the common line **116** serves as the first electrode, the horizontal portion **130***c* of the pixel electrode **130** and the auxiliary line **136** the third electrode in the dual storage capacitor.

[**0037**] **FIG. 6** is a circuit diagram of **FIG. 4**. In **FIG. 6**, **a** liquid crystal capacitor C_{LC} is connected in series to the thin film transistor "T" and the first auxiliary storage capacitor C_{St1} and the second auxiliary storage capacitor C_{St2} are connected in parallel to the liquid crystal capacitor C_{LC}. Consequently, enough auxiliary capacitance can be secured even when a width of the common line **116** should be reduced for realizing a minute pixel.

[**0038**] If the pixel structure described in the present invention for the in-plane switching (IPS) mode liquid crystal display (LCD) device that drives a minute pixel, an area for the storage capacitor "C" is not limited. Moreover, if the area for the storage capacitor "C" is designed to be larger in order to secure a capacitance of the storage capacitor "C", an aperture ratio of the liquid crystal panel is not decreased.

[**0039**] It will be apparent to those skilled in the art that various modifications and variations can be made in the fabrication and application of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An array substrate for in-plane switching mode liquid crystal display device, comprising:

a substrate having a plurality of pixel regions;

a plurality of gate lines and a plurality of common lines in horizontal direction;

a plurality of data lines crossing the gate line and the common line;

a thin film transistor at a cross point of the gate line and the data line, the thin film transistor having a gate electrode, an active layer, a source electrode and a drain electrode;

a pixel electrode having an extension portion, a vertical portion and a horizontal portion, the extension portion being extended from the drain electrode to the pixel region, the vertical portion being vertically extended from the extension portion and the horizontal portion being over the common line and being connected to the vertical portion;

a common electrode having a plurality of vertical portions and a horizontal portion, the plurality of the vertical portions being vertically extended from the common line and arranged in an alternating pattern with the vertical portion of the pixel electrode, the horizontal portion connecting the plurality of the vertical portions into one portion; and

an auxiliary line over the horizontal portion of the pixel electrode and being overlapped with the common line.

2. The array substrate according to claim 1, further comprising a dummy line in a non-display area of the substrate.

3. The array substrate according to claim 2, wherein the dummy line communicates with the auxiliary line.

4. The array substrate according to claim 2, wherein the dummy line includes one of a metal material from the group of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

5. The array substrate according to claim 1, wherein the auxiliary line includes one of Indium-Tin-Oxide (ITO) and Indium Zinc Oxide (IZO).

6. The array substrate according to claim 1, wherein the gate line, the common line and the common electrode are formed using the same material on a same layer.

7. The array substrate according to claim 1, wherein the gate line, the common line and the common electrode includes one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

8. The array substrate according to claim 1, further comprising an insulating layer between the common line and the horizontal portion of the pixel electrode to form a first auxiliary storage capacitor.

9. The array substrate according to claim 8, wherein the insulating layer includes one of silicon nitride (SiNx) and silicon oxide (SiO_2).

10. The array substrate according to claim 1, further comprising an insulating layer between the horizontal portion of the pixel electrode and the auxiliary line to form a second auxiliary storage capacitor.

11. The array substrate according to claim 10, wherein the insulating layer includes one of silicon nitride (SiNx) and silicon oxide (SiO_2).

12. A method for fabricating an array substrate for in-plane switching mode liquid crystal display device, comprising:

forming a plurality of gate lines, a plurality of common lines and a dummy line on an array substrate, the gate line and the common line being formed in a horizontal direction and spaced apart from each other, the dummy line being formed in a non-display area;

forming a plurality of data lines crossing the gate line and the common line;

forming a thin film transistor at a cross point of the gate line and the data line, the thin film transistor having a gate electrode, an active layer, a source electrode and a drain electrode;

forming a pixel electrode having an extension portion, a vertical portion and a horizontal portion, the extension portion being extended from the drain electrode, the vertical portion being vertically extended from the extension portion and the horizontal portion being over the common line and connected to the vertical portion;

forming a common electrode having a plurality of vertical portions and a horizontal portion, the plurality of the vertical portions being vertically extended from the common line and arranged in an alternating pattern with the vertical portion of the pixel electrode, the horizontal portion connecting the plurality of the vertical portions into one portion; and

forming an auxiliary line over the horizontal portion of the pixel electrode, the auxiliary line being overlapped with the common line and one end of the auxiliary line communicating with the dummy line.

13. The method according to claim 12, wherein the gate line, the common line and the dummy line are formed using the same material on a same layer.

14. The method according to claim 12, wherein the gate line, the common line and the dummy line are formed one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

15. The method according to claim 12, wherein the auxiliary line is formed one of Indium-Tin-Oxide (ITO) and Indium Zinc Oxide (IZO).

16. The method according to claim 12, further comprising forming an insulating layer between the common line and the horizontal portion of the pixel electrode to form a first auxiliary storage capacitor.

17. The method according to claim 16, wherein the insulating layer is formed one of silicon nitride (SiNx) and silicon oxide (SiO_2).

18. The method according to claim 12, further comprising forming an insulating layer between the horizontal portion of the pixel electrode and the auxiliary line to form a second auxiliary storage capacitor.

19. The method according to claim 18, wherein the insulating layer is formed one of silicon nitride (SiNx) and silicon oxide (SiO_2).

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[标]申请(专利权)人(译)	IK KIM SOO CHAE GEE SUNG		
申请(专利权)人(译)	KIM IK-SOO CHAE GEE-SUNG		
当前申请(专利权)人(译)	KIM IK-SOO CHAE GEE-SUNG		
[标]发明人	KIM IK SOO CHAE GEE SUNG		
发明人	KIM, IK-SOO CHAE, GEE-SUNG		
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摘要(译)

一种用于面内切换（IPS）模式液晶显示（LCD）器件的阵列基板，包括具有延伸部分，垂直部分和水平部分的像素电极，所述延伸部分从漏电极延伸到像素区域，垂直部分从延伸部分垂直延伸，水平部分在公共线上方并连接到垂直部分。该器件包括具有多个垂直部分和水平部分的公共电极，多个垂直部分从公共线垂直延伸并与像素电极的垂直部分交替排列，水平部分连接多个垂直部分合二为一。辅助线位于像素电极的水平部分上方并与公共线重叠。