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(54) **THIN FILM TRANSISTOR ARRAY PANEL AND LIQUID CRYSTAL DISPLAY HAVING THE SAME**

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(57) **ABSTRACT**

A liquid crystal display according to an exemplary embodiment of the present invention includes a colored subsidiary light blocking member covering a space between first and second pixel electrodes. First and third shield electrodes are placed under a data line. The first and third shield electrodes are disposed parallel to the data line and across the data line from each other. A second shield electrode connects the bottom end of the first shield electrode with the top end of the third shield electrode at an angle of about 30 degrees to about 150 degrees. With this structure, light leakage at a gap between the pixel electrode and a possible short between the shield electrodes are prevented.

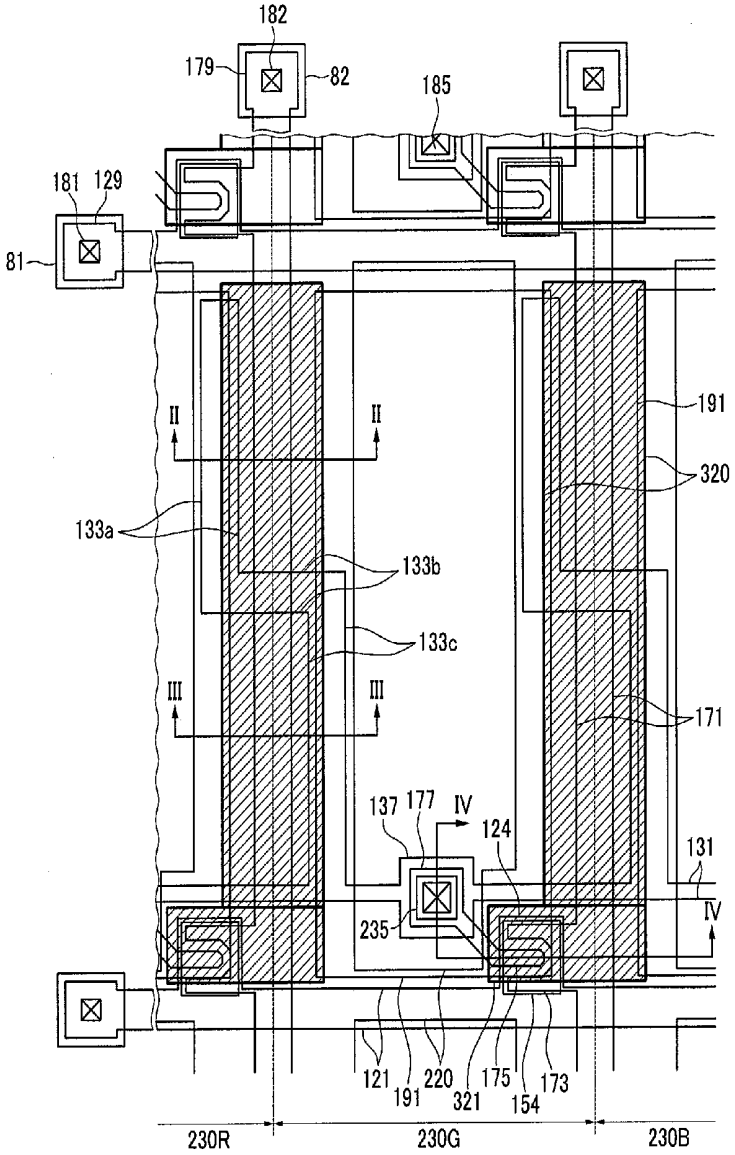
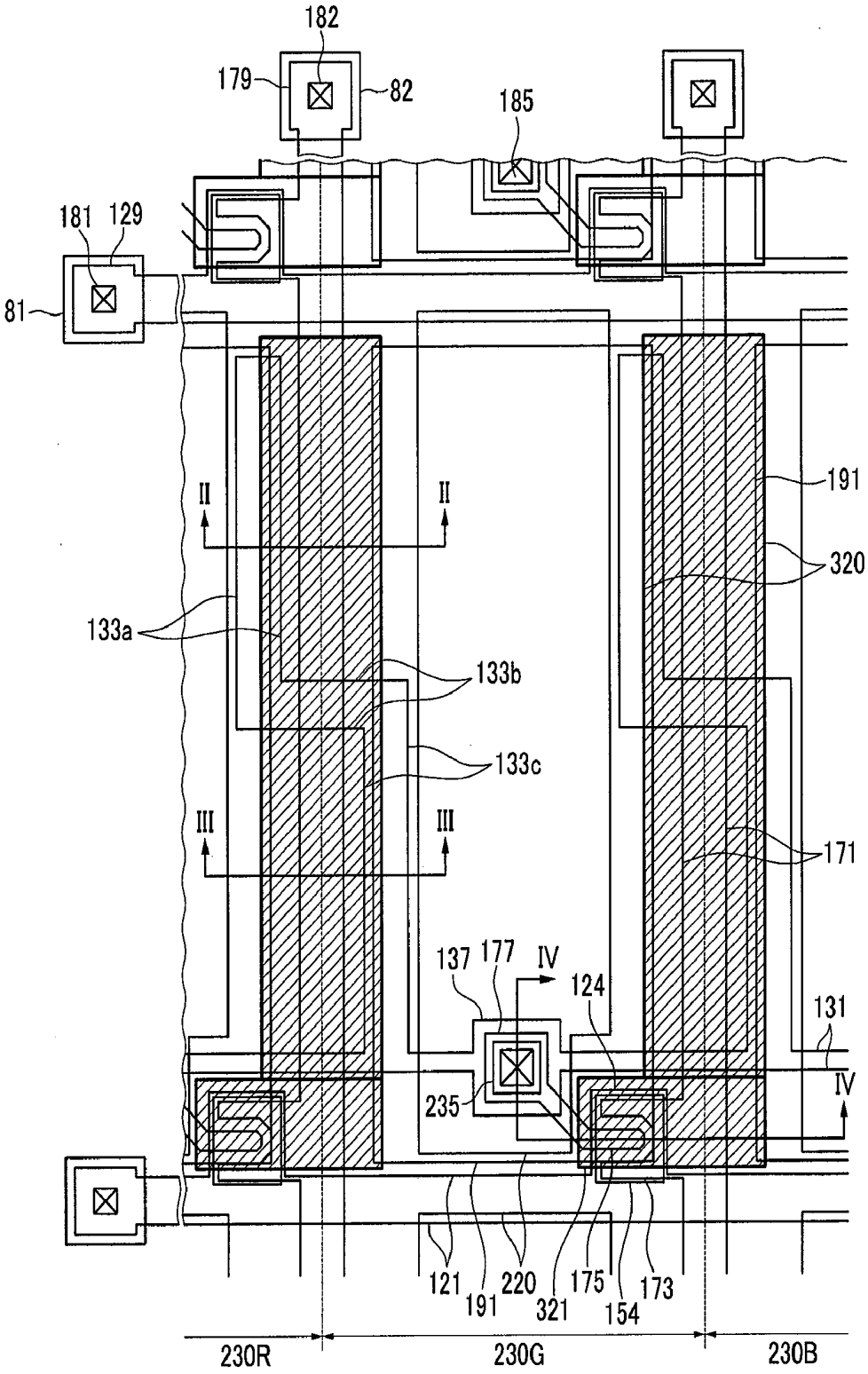


FIG.1


182
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81
II
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191
320
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133b
133c
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171
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124
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IV
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121
191
220
321
175
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173
230R
230G
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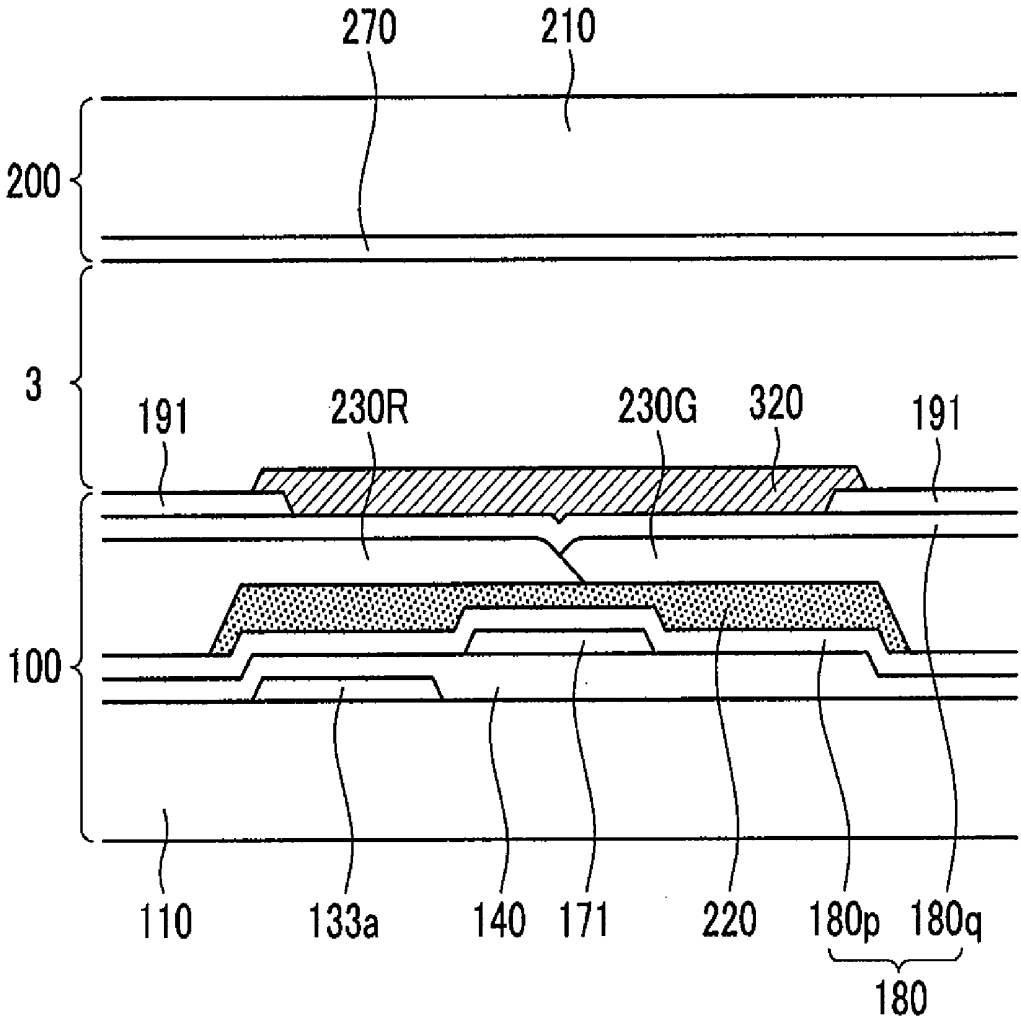
FIG.2


270
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180p
180q
180

FIG.3

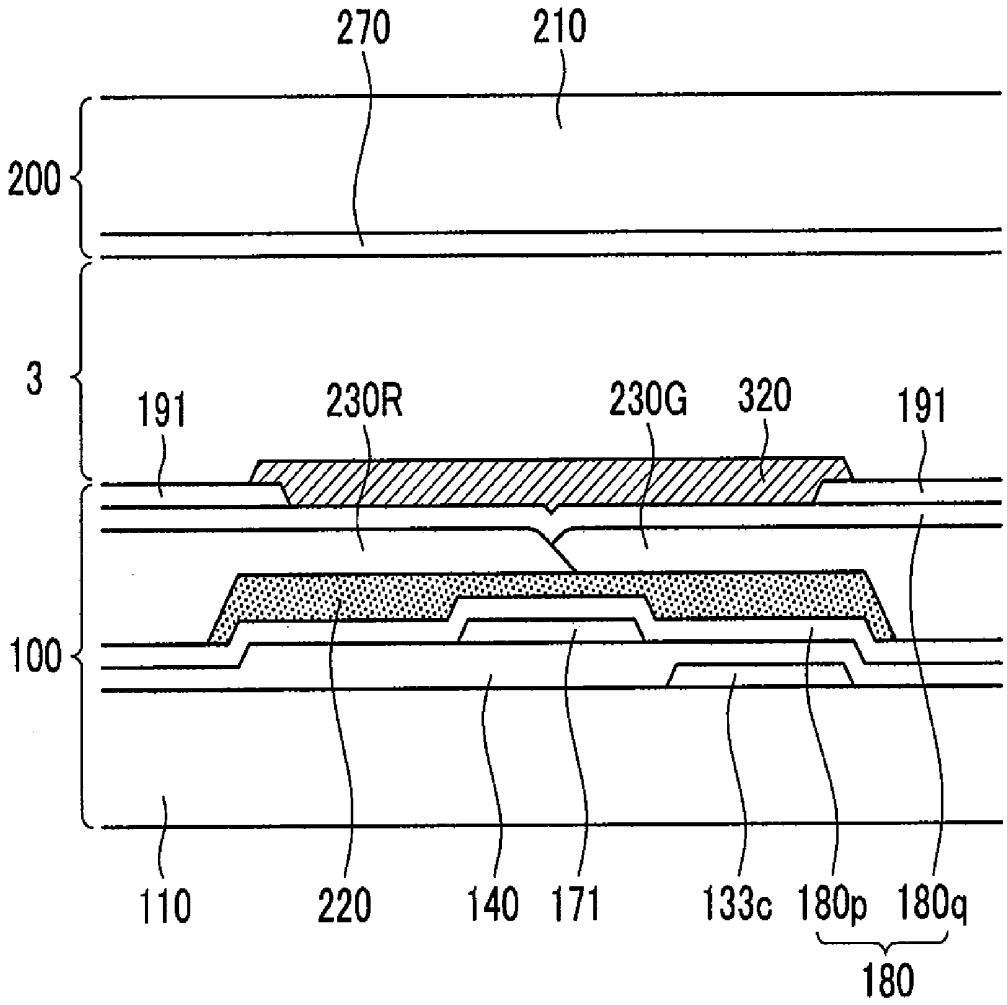
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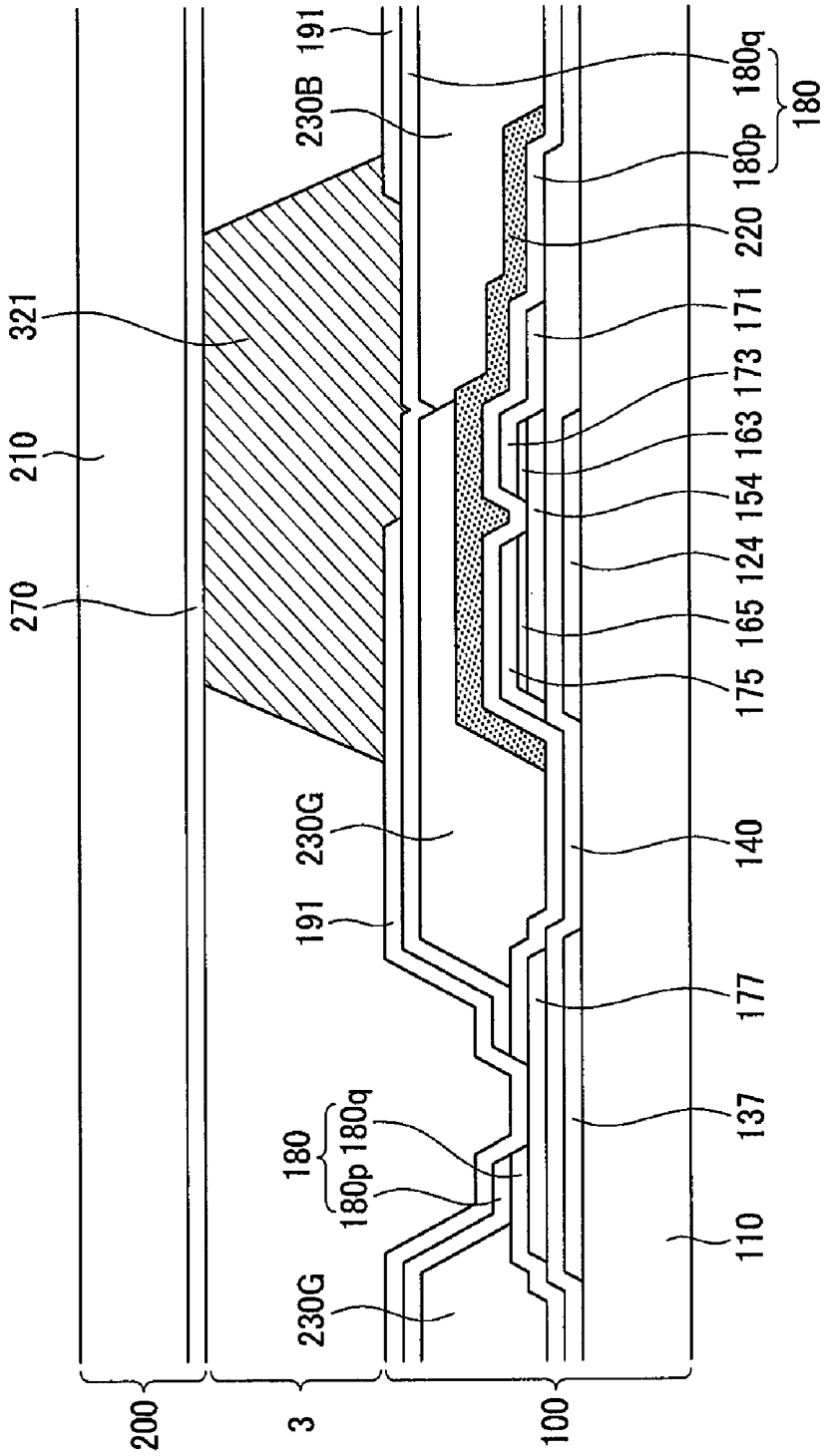
FIG.4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177
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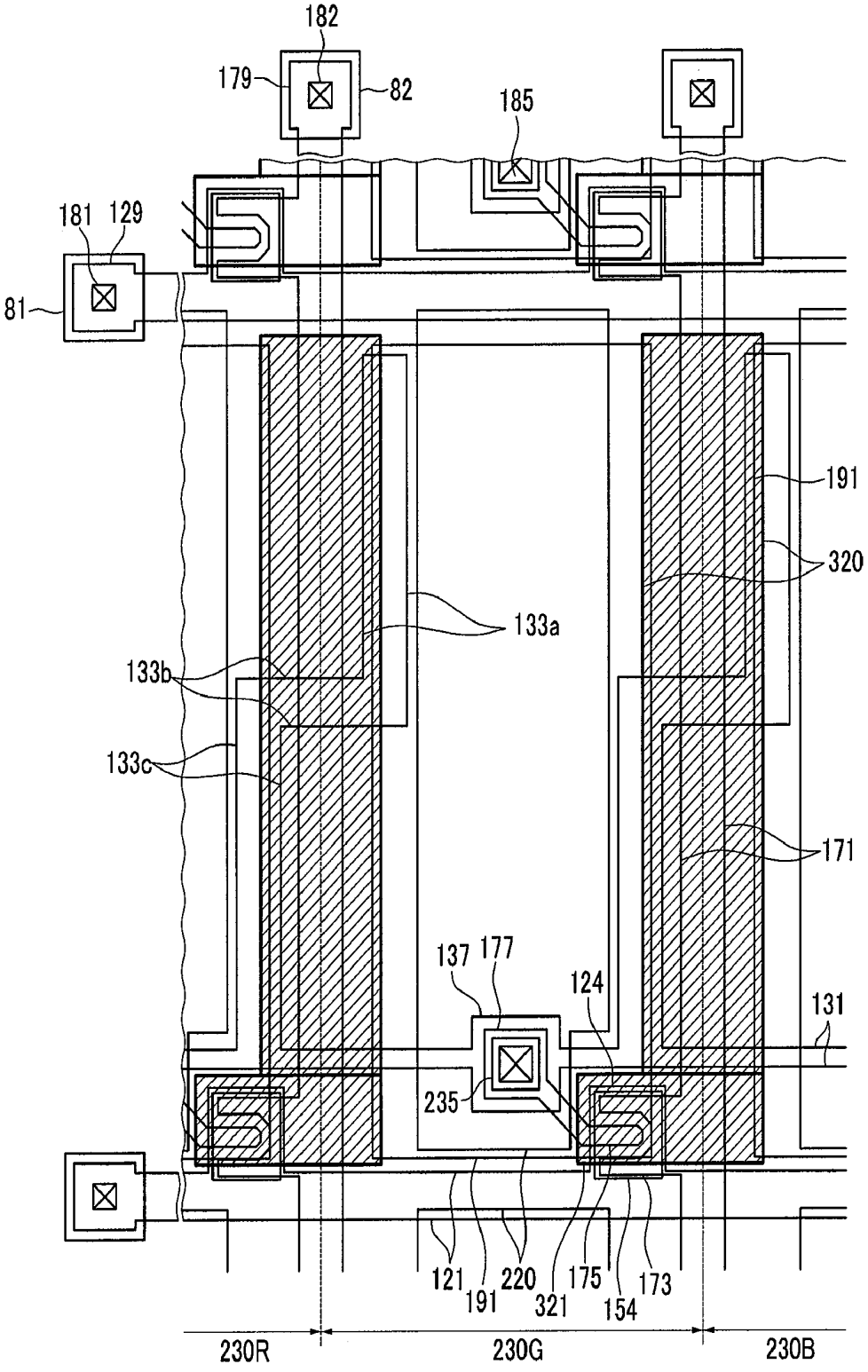
100

FIG.5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220
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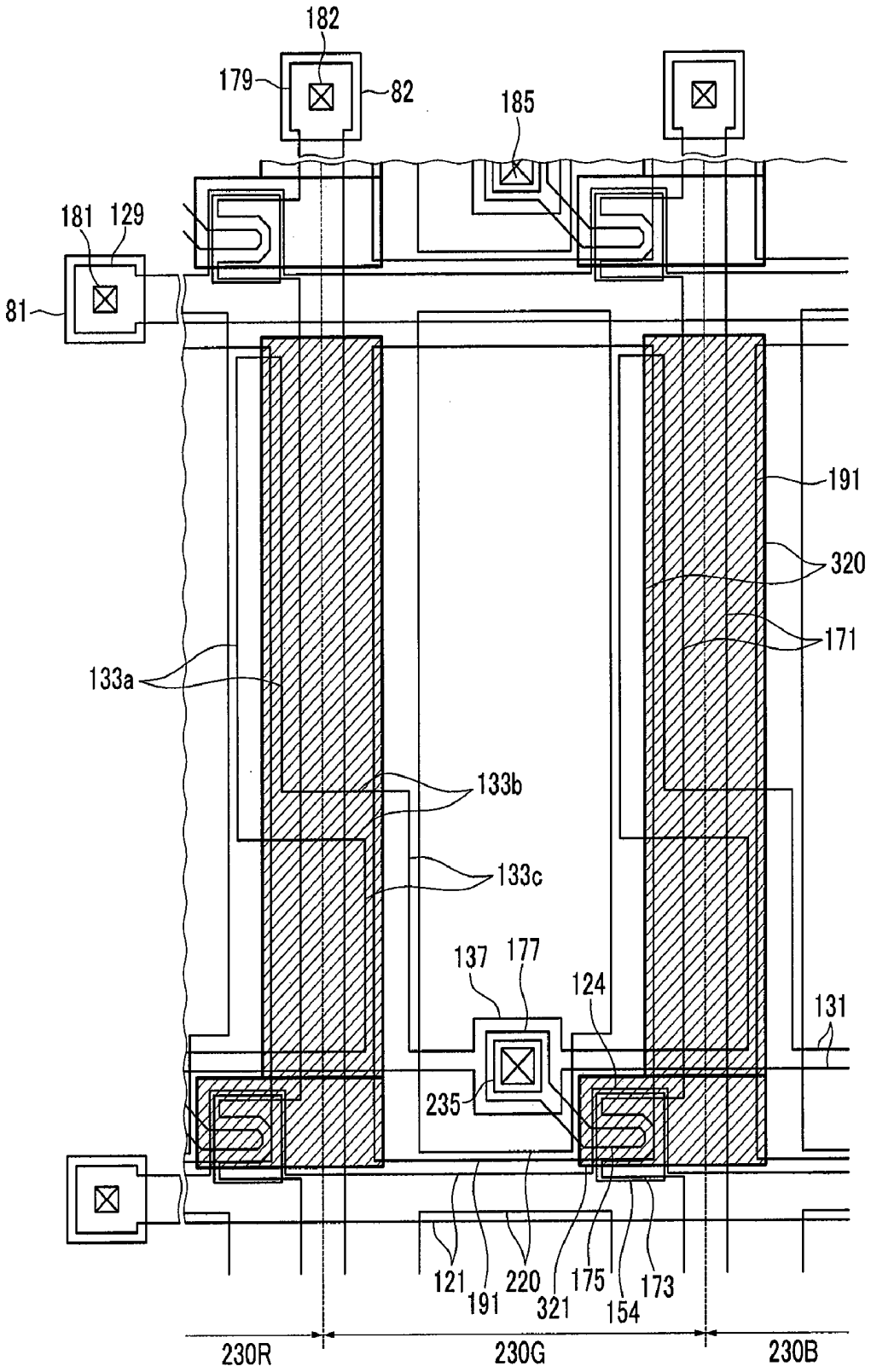
230G
230B

FIG.6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154
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230R
230G
230B

THIN FILM TRANSISTOR ARRAY PANEL AND LIQUID CRYSTAL DISPLAY HAVING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2008-0067148 filed in the Korean Intellectual Property Office on Jul. 10, 2008, the entire content of which is incorporated herein by reference.

BACKGROUND

[0002] (a) Technical Field

[0003] The present invention relates to a thin film transistor array panel and a display device having the same.

[0004] (b) Discussion of the Related Art

[0005] Liquid crystal displays are one of the widely used flat panel displays today. A liquid crystal display has two display panels on which field generating electrodes such as pixel electrodes and a common electrode are formed, and a liquid crystal layer that is interposed between the panels. In the liquid crystal display, voltages are applied to the field generating electrodes so as to generate an electric field over the liquid crystal layer, and the alignment of liquid crystal molecules of the liquid crystal layer is determined by the electric field. Accordingly, the polarization of incident light is controlled, thereby performing image display.

[0006] Liquid crystal displays with various structures have been developed to enhance their display quality, for example by increasing the aperture ratio, reducing RGB gamma distortions, preventing the leakage of light, etc.

[0007] The above information disclosed in this Background section is only for enhancement of understanding of the background of the invention and therefore it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY OF THE INVENTION

[0008] An exemplary embodiment of the present invention provides a display device with first and second display panels, and a liquid crystal layer disposed between the first and second display panels. The first display panel includes a first substrate, and a light blocking member disposed on the first substrate. A plurality of color filters are disposed on the light blocking member, a plurality of pixel electrodes are disposed on the plurality of color filters, and a subsidiary light blocking member is disposed on the pixel electrodes such that it is placed at a region between two neighboring pixel electrodes. The second display panel includes a second substrate facing the first substrate, and a common electrode disposed on the second substrate.

[0009] The subsidiary light blocking member may have a width of about 6 μm to about 13 μm.

[0010] The subsidiary light blocking member may further include a column spacer.

[0011] The subsidiary light blocking member may have a thickness of less than about 2 μm.

[0012] The first display panel may further include a gate line disposed on the first substrate, and a storage electrode line disposed on the first substrate. A data line crosses the gate line and the storage electrode line while being insulated from the gate line and the storage electrode. The data line overlaps the light blocking member. A thin film transistor includes a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode connected to the pixel electrode. A storage electrode is connected to the storage electrode line such that it is overlapped with the drain electrode. A first shield electrode is connected to the storage electrode line, and disposed parallel to the data line. A third shield electrode is disposed parallel to the data line and across the data line from the first shield electrode. A second shield electrode connects the bottom end of the first shield electrode with the top end of the third shield electrode.

[0013] The second shield electrode may be connected to the first and third electrodes at an angle of about 30 degrees to about 150 degrees.

[0014] The length ratio of the first shield electrode to the third shield electrode may be about 1:2 to about 2:1.

[0015] The first to third shield electrodes may have a width of about 3 μm to about 4 μm, respectively.

[0016] The width of the second shield electrode may be smaller than the width of the first and third shield electrodes.

[0017] Another exemplary embodiment of the present invention provides a thin film transistor array panel having an insulation substrate, a gate line disposed on the insulation substrate with a gate electrode, and a storage electrode line disposed on the insulation substrate with a shield electrode. A gate insulating layer is disposed on the gate line and the storage electrode line, a semiconductor layer is disposed on the gate insulating layer, and a data line are disposed on the gate insulating layer. The data line includes a source electrode disposed on the semiconductor layer. A drain electrode is disposed on the semiconductor layer such that it is spaced apart from the source electrode thereon, a light blocking member is disposed on the data line and the drain electrode such that it covers the data line, and color filters are disposed on the light blocking member. A pixel electrode is disposed on the color filter such that it is connected to the drain electrode. The shield electrodes include a first shield electrode connected to the storage electrode line and disposed parallel to the data line, a third shield electrode placed across the data line from the first shield electrode, and a second shield electrode connecting the bottom end of the first shield electrode with the top end of the third shield electrode.

[0018] The storage electrode line may further include a storage electrode overlapping the drain electrode.

[0019] A subsidiary light blocking member may be disposed on the pixel electrodes, and overlapped with the data line.

[0020] The subsidiary light blocking member may further include a column spacer.

[0021] As there are no portions of the first and third shield electrodes facing each other, a possible short between the shield electrodes is prevented.

[0022] With the shield electrodes, the aperture ratio is heightened, while the RGB gamma distortions are reduced.

[0023] In the case that the first and third shield electrodes are similar in length to each other, couplings at the left and right sides of the pixel are maintained equally, and a waterfall effect as well as RGB gamma distortions are reduced.

[0024] When the light blocking member has a width of about 13 μm or less, the aperture ratio is increased, while the power consumption as well as the RGB gamma distortions are reduced.

[0025] Even when the light blocking member is misaligned be being horizontally moved left or right by about 3 μm or

more, light leakage at the gap between the pixel electrodes is prevented because the colored subsidiary light blocking member covers that gap.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] FIG. **1** is a layout view of a liquid crystal display according to an exemplary embodiment of the present invention.

[0027] FIG. **2** is a cross-sectional view of the liquid crystal display shown in FIG. **1** taken along the II-II line thereof.

[0028] FIG. **3** is a cross-sectional view of the liquid crystal display shown in FIG. **1** taken along the III-III line thereof.

[0029] FIG. **4** is a cross-sectional view of the liquid crystal display shown in FIG. **1** taken along the IV-IV line thereof.

[0030] FIG. **5** is a layout view of a liquid crystal display according to an exemplary embodiment of the present invention.

[0031] FIG. **6** is a layout view of a liquid crystal display according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0032] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the present invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention. In the drawings, irrelevant portions are omitted to clearly describe the present invention, and like reference numerals designate like elements throughout the specification. Furthermore, detailed descriptions are not given to the well-known arts.

[0033] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "under" another element, it can be directly under the other element or intervening elements may also be present. On the contrary, when an element is referred to as being "directly under" another element, there are no intervening elements present.

[0034] Now, a liquid crystal display according to an exemplary embodiment of the present invention will be described in detail with reference to FIG. **1** to FIG. **6**.

[0035] FIG. **1** is a layout view of a liquid crystal display according to an exemplary embodiment of the present invention, FIG. **2** is a cross-sectional view of the liquid crystal display shown in FIG. **1** taken along the line II-II, FIG. **3** is a cross-sectional view of the liquid crystal display shown in FIG. **1** taken along the line III-III, and FIG. **4** is a cross-sectional view of the liquid crystal display shown in FIG. **1** taken along the line IV-IV.

[0036] Referring to FIG. **1** to FIG. **4**, a liquid crystal display according to an exemplary embodiment of the present invention includes first and second display panels **100** and **200**, and a liquid crystal layer **3** interposed between the two display panels **100** and **200**.

[0037] The liquid crystal layer **3** may have a positive (+) or negative (−) dielectric anisotropy. In the absence of electric field, liquid crystal molecules of the liquid crystal layer **3** may be aligned such that their directors stand substantially horizontally or vertically with respect to the surface of the two display panels **100** and **200**.

[0038] Alignment layers (not shown) may be disposed on the inner surfaces of the display panels **100** and **200**. The alignment layers may be horizontal alignment layers. Polarizers (not shown) may be attached to the outer surfaces of the display panels **100** and **200**.

[0039] The first display panel **100** will be firstly described in detail.

[0040] The first display panel **100** may include thin film transistors disposed on the inner surface of a substrate **110**.

[0041] Gate lines **121** and storage electrode lines **131** are disposed on the insulation substrate **110** that is based on transparent glass or plastic.

[0042] The gate lines **121** proceed substantially in the horizontal direction to carry gate signals. The respective gate lines **121** have a plurality of gate electrodes **124** protruding upwards ("upwards" in reference to FIG. **1**).

[0043] Each storage electrode line **131** receives a predetermined voltage, and proceeds substantially parallel to a gate line **121**. The storage electrode line **131** is placed adjacent to the lower side gate line **121**. The storage electrode line **131** includes storage electrodes **137** with a substantially square shape, which are primary storage electrodes, and first to third shield electrodes **133***a*, **133***b*, and **133***c*, which are secondary storage electrodes. The shape and disposition of the storage electrode line **131** may be altered in various manners.

[0044] The first and third shield electrodes **133***a* and **133***c* are respectively disposed under a data line **171** substantially parallel thereto. The bottom end of the first shield electrode **133***a* and the top end of the third shield electrode **133***c* are connected to each other by way of the second shield electrode **133***b*. The connection angle of the second shield electrode **133***b* to the first and third shield electrodes **133***a* and **133***c* may be about 30 degrees to about 150 degrees. When the connection angle is less than about 30 degrees, a problem may be caused in the pattern formation at the bend. By contrast, when the connection angle exceeds 150 degrees, the capacitance of the shield electrodes **133***a*, **133***b*, and **133***c* is likely to be reduced.

[0045] The connection angle may be a right angle or an obtuse angle. With such a structure of the shield electrodes **133***a*, **133***b*, and **133***c*, the aperture ratio is increased while the RGB gamma distortions are reduced, and a short between the shield electrodes is prevented.

[0046] In a liquid crystal display where the first and third shield electrodes **133***a* and **133***c* face each other while extending parallel to the data line on each side of the data line, the distance between the shield electrodes becomes small. This small separation distance between the shield electrodes undesirably decreases the reduction in aperture ratio so that a short may occur between the shield electrodes in case of a patterning error or a foreign material. The practical distance between the shield electrodes is established to be about 4 μm based on after cleaning inspection (ACI), and about 2.5 μm based on after development inspection (ADI). The structure according to an exemplary embodiment of the present invention elimi-

nates the first and third shield electrodes **133***a* and **133***c* facing each other, and hence reduces the possibility of a short between the shield electrodes.

[0047] The first to third shield electrodes **133***a*, **133***b*, and **133***c* may have a width of about 3 μm to about 4 μm. Embodiments of the invention is not limited to the first to third shield electrodes **133***a*, **133***b*, and **133***c* having the same width. Unless the aperture ratio is reduced, the width of the first and third shield electrodes **133***a* and **133***c* may be enlarged to about 4 μm, while the width of the second shield electrode **133***b* may be narrowed to about 3 μm.

[0048] The length ratio of the first shield electrode **133***a* to the third shield electrode **133***c* may be about 1:2 to about 2:1. FIG. **1** illustrates the case where the length ratio of the first shield electrode **133***a* to the third shield electrode **133***c* is about 1:1. When the length of the first shield electrode **133***a* is the same as that of the third shield electrode **133***c*, couplings at both left and right sides of the pixel is maintained equally, and the RGB gamma distortions and the waterfall effect is reduced. Although it is preferable to make the length ratio of the first shield electrode **133***a* to the third shield electrode **133***c* about 1:1, the gamma distortions and the waterfall effect is reduced even when that length ratio is in the range of about 1:2 to about 2:1.

[0049] A gate insulating layer **140** made of silicon nitride (SiNx) or silicon oxide (SiOx) is disposed on the gate line **121** and the storage electrode line **131**.

[0050] Semiconductor islands **154** are disposed on the gate insulating layer **140** with hydrogenated amorphous silicon (the amorphous silicon being abbreviated as a-Si) or polysilicon. Each semiconductor island **154** is placed on a gate electrode **124**.

[0051] Ohmic contacts **163** and **165** are disposed on the semiconductor islands **154**. The ohmic contacts **163** and **165** may be disposed with n+ hydrogenated amorphous silicon where n-type impurities such as phosphorus are doped at a high concentration, or of silicide.

[0052] The data lines **171** and drain electrodes **175** are disposed on the ohmic contacts **163** and **165** and the gate insulating layer **140**.

[0053] The data lines **171** for carrying data voltages proceed substantially in the vertical direction such that they cross the gate lines **121**. The data lines **171** are disposed substantially parallel to the first and third shield electrodes **133***a* and **133***c*, and are positioned close to the gate electrodes **124**. The data lines **171** include source electrodes **173** connected thereto on the gate electrodes **124**. In the present exemplary embodiment, the source electrodes **173** are disposed in the shape of a horizontally laid capital U, but this structure may be altered in various manners.

[0054] Each drain electrode **175** is spaced apart from a source electrode **173** by a distance, and has a narrow portion and a wide portion **177**. The narrow portion of the drain electrode **175** has an end that is partially surrounded by the source electrode **173**, and the wide portion **177** of the drain electrode **175** is substantially square-shaped while being overlapped with the storage electrode **137**. The wide portion **177** of the drain electrode **175** occupies substantially the same area as that of the storage electrode **137**, but is not outside the boundaries of the storage electrode **137** in plan view.

[0055] The gate electrode **124**, the source electrode **173**, and the drain electrode **175** form a thin film transistor (TFT) in association with the semiconductor **154**. The channel of the thin film transistor is disposed at the semiconductor **154** between the source and drain electrodes **173** and **175**.

[0056] The ohmic contacts **163** and **165** exist only between the underlying semiconductors **154** and the overlying data lines **171** and drain electrodes **175** so as to lower the contact resistance therebetween. Each semiconductor **154** has exposed portions not covered by the data line **171** and the drain electrode **175**, including a portion between the source and drain electrodes **173** and **175**.

[0057] A passivation layer **180** is disposed on the data lines **171**, the drain electrodes **175**, and the exposed portions of the semiconductors **154**. The passivation layer **180** includes lower and upper layers **180***p* and **180***q* based on an inorganic insulator such as silicon nitride and silicon oxide. One of the lower and upper layers **180***p* and **180***q* may be omitted. The lower layer **180***p* may be an organic insulating layer.

[0058] Contact holes **185** are disposed at the passivation layer **180** such that they expose the wide portions **177** of the drain electrodes **175**.

[0059] A light blocking member **220**, called the black matrix, is disposed on the lower layer **180***p*. When the width of the light blocking member **220** is about 13 μm or less, the aperture ratio is increased, while the RGB gamma distortions and the power consumption are reduced.

[0060] Red, green, and, blue color filters **230**R, **230**G, and **230**B are disposed on the lower layer **180***p* or the light blocking member **220**. The color filters **230**R, **230**G, and **230**B occupy regions between neighboring data lines **171**. The left and right boundaries of the color filters **230**R, **230**G, and **230**B are placed over the data lines **171**, and may vertically extend along the data lines **171** (see FIG. **1**). In the latter case, the color filters **230**R, **230**G, and **230**B may be disposed as stripes.

[0061] Openings **235** are disposed at the color filters **230**R, **230**G, and **230**B over the wide portions **177** of the drain electrodes **175**. Each opening **235** occupies substantially the same area as that of a wide portion **177** of a drain electrode **175**, but does not extend outside the boundaries of the wide portion **177** in plan view. The outline of the contact hole **185** is lies within the boundaries of the opening **235** in plan view.

[0062] The color filters **230**R, **230**G, and **230**B may be disposed with a photosensitive organic material containing a pigment.

[0063] Pixel electrodes **191** and contact assistants **81** and **82** are disposed on the upper layer **180***q* of the passivation layer **180**. The pixel electrodes **191** and the contact assistants **81** and **82** may be disposed with a transparent conductive material such as ITO and IZO, or a reflective metal such as aluminum, silver, chromium, and alloys thereof.

[0064] The contact assistants **81** and **82** are connected to ends **129** of the gate lines **121** and ends **179** of the data lines **171** through contact holes **181** and **182**, respectively. The contact assistants **81** and **82** assist the adhesion of the ends **129** of the gate lines **121** and the ends **179** of the data lines **171** to external devices, and protect them.

[0065] The pixel electrode **191** is connected to the drain electrode **175** of the thin film transistor through the contact hole **185** to receive a data voltage from the drain electrode **175**. The pixel electrode **191** receiving a data voltage generates an electric field in association with a common electrode **270** of the second display panel **200** so as to determine the direction of liquid crystal molecules of the liquid crystal layer **3** between the two electrodes **191** and **270**. The luminance of

the light passing through the liquid crystal layer **3** is differentiated depending upon the determined direction of the liquid crystal molecules.

[0066] The pixel electrode **191** and the common electrode **270** form a liquid crystal capacitor that maintains the applied voltage even after the thin film transistor turns off.

[0067] The pixel electrode **191** and the drain electrode **175** connected thereto overlap the storage electrode line **131** including the storage electrode **137** and the shield electrodes **133***a*, **133***b*, and **133***c* to thereby form a storage capacitor.

[0068] A colored subsidiary light blocking member **320** is disposed between the neighboring pixel electrodes **191**. The subsidiary light blocking member **320** covers all the space between the neighboring pixel electrodes **191**, and contacts the upper layer **180***q*, or the color filter **230**R or **230**G. Accordingly, even if the light blocking member **220** is misaligned after being horizontally moved left or right by about 3 μm or more, the colored subsidiary light blocking member **320** covers the gap between the neighboring pixel electrodes **191** to prevent light leakage at that gap.

[0069] The thickness of the subsidiary light blocking member **320** is established to be about 2 μm or less so as to prevent the light leakage possibly generated due to abnormal alignment of the liquid crystal molecules as the height of the light blocking member **320** increases. The distance between the neighboring pixel electrodes **191** is established to be about 6 μm, and the width of the subsidiary light blocking member **320** is preferably established to be about 6 μm or more because it covers all the space between the neighboring pixel electrodes **191**. However, if the width of the subsidiary light blocking member **320** exceeds about 13 μm, the aperture ratio is reduced. For this reason, the width of the subsidiary light blocking member **320** is preferably established to be about 13 μm or less.

[0070] The colored subsidiary light blocking member **320** includes an organic material. The subsidiary light blocking member **320** may include a column spacer **321** (see FIG. **4**). The column spacer **321** maintains a constant thickness for the liquid crystal layer **3**. The column spacer **321** is thicker than the subsidiary light blocking member **320**. A half-tone mask may be used to form the column spacer **321** and the subsidiary light blocking member **320** that differ in thickness from each other, by way of engraving either in intaglio or in relief.

[0071] The second display panel **200** will now be described in detail.

[0072] With the second display panel **200**, an overcoat (not shown) is disposed on an insulation substrate **210** based on transparent glass or plastic. The overcoat is disposed with an organic or inorganic insulating material. The overcoat may be omitted.

[0073] A common electrode **270** is disposed on the overcoat. The common electrode **270** is disposed with a transparent conductor such as ITO and IZO, and receives a common voltage.

[0074] An alignment layer (not shown) may be disposed on the common electrode **270**. In this case, the alignment layer contacts the first display panel **100**.

[0075] FIG. **5** is a layout view of a liquid crystal display according to an exemplary embodiment of the present invention. The liquid crystal display shown in FIG. **5** is similar in structure to that described with reference to FIG. **1**, except that the first shield electrode **133***a* is on the right side of the data line **171** and the third shield electrode **133***c* on the left side of the data line **171**.

[0076] FIG. **6** is a layout view of a liquid crystal display according to an exemplary embodiment of the present invention. The liquid crystal display shown in FIG. **6** is similar in structure to that described with reference to FIG. **1**, except that the length ratio of the first shield electrode **133***a* to the third shield electrode **133***c* is 2:1.

[0077] While this invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. A liquid crystal display comprising:
- a first substrate;
- a first display panel comprising a light blocking member disposed on the first substrate, a plurality of color filters disposed on the light blocking member, a plurality of pixel electrodes disposed on the plurality of color filters, and a subsidiary light blocking member disposed on the pixel electrodes while placed at the region between the neighboring pixel electrodes;
- a second display panel comprising a second substrate facing the first substrate, and a common electrode disposed on the second substrate; and
- a liquid crystal layer disposed between the first and second display panels.

2. The liquid crystal display of claim **1**, wherein the subsidiary light blocking member has a width of about 6 μm to about 13 μm.

3. The liquid crystal display of claim **2** further comprising a column spacer disposed on the pixel electrode, wherein the column spacer comprises the same material as the subsidiary light blocking member.

4. The liquid crystal display of claim **2**, wherein the subsidiary light blocking member has a thickness of less than about 2 μm.

5. The liquid crystal display of claim **4**, wherein the first display panel further comprises:
- a gate line and a storage electrode line disposed on the first substrate;
- a data line crossing the gate line and the storage electrode line while being insulated from the gate line and the storage electrode, the data line overlapping the light blocking member;
- a thin film transistor comprising a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode connected to the pixel electrode;
- a storage electrode connected to the storage electrode line, the storage electrode overlapping the drain electrode;
- a first shield electrode disposed parallel to the data line, the first shield electrode connected to the storage electrode line;
- a third shield electrode disposed parallel to the data line and across the data line from the first shield electrode; and
- a second shield electrode connecting the bottom end of the first shield electrode with the top end of the third shield electrode.

6. The liquid crystal display of claim **5**, wherein the second shield electrode is connected to the first and third shield electrodes at an angle of about 30 degrees to about 150 degrees.

7. The liquid crystal display of claim 5, wherein the length ratio of the first shield electrode to the third shield electrode is about 1:2 to about 2:1.

8. The liquid crystal display of claim 1, wherein the first display panel further comprises:

a gate line and a storage electrode line disposed on the first substrate;

a data line crossing the gate line and the storage electrode line while being insulated from the data line and the storage electrode line, the data line overlapping the light blocking member;

a thin film transistor comprising a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode connected to the pixel electrode;

a storage electrode connected to the storage electrode line, the storage electrode overlapping the drain electrode;

a first shield electrode disposed parallel to the data line, the first shield electrode connected to the storage electrode line;

a third shield electrode disposed parallel to the data line and across the data line from the first shield electrode; and

a second shield electrode connecting the bottom end of the first shield electrode with the top end of the third shield electrode.

9. The liquid crystal display of claim 8, wherein the second shield electrode is connected to the first and third shield electrodes at an angle of about 30 degrees to 150 degrees.

10. The liquid crystal display of claim 8, wherein the length ratio of the first shield electrode to the third shield electrode is about 1:2 to about 2:1.

11. The liquid crystal display of claim 8, wherein each of the first to third shield electrodes has a width of about 3 μm to about 4 μm.

12. The liquid crystal display of claim 11, wherein the second shield electrode is narrower than the first and third shield electrodes.

13. A thin film transistor array panel comprising:

an insulation substrate;

a gate line disposed on the insulation substrate, the gate line having a gate electrode;

a storage electrode line disposed on the insulating substrate, the storage electrode line having shield electrodes;

a gate insulating layer disposed on the gate line and the storage electrode line;

a semiconductor layer disposed on the gate insulating layer;

a data line disposed on the gate insulating layer, the data line having a source electrode disposed on the semiconductor layer;

a drain electrode spaced apart from the source electrode on the semiconductor layer; and

a pixel electrode connected to the drain electrode,

wherein the shield electrodes comprise a first shield electrode connected to the storage electrode line and disposed parallel to the data line, a third shield electrode disposed parallel to the data line and across the data line from the first shield electrode, and a second shield electrode connecting the bottom end of the first shield electrode with the top end of the third shield electrode.

14. The thin film transistor array panel of claim 13, wherein the storage electrode line further comprises a storage electrode overlapping the drain electrode.

15. The thin film transistor array panel of claim 14, wherein the length ratio of the first shield electrode to the third shield electrode is about 1:2 to about 2:1.

16. The thin film transistor array panel of claim 15 further comprising a subsidiary light blocking member disposed on the pixel electrodes, the subsidiary light blocking member overlapping the data line.

17. The thin film transistor array panel of claim 16, wherein the subsidiary light blocking member has a width of about 6 μm to about 13 μm.

18. The thin film transistor array panel of claim 17 further comprising a column spacer disposed on the pixel electrode overlapping the semiconductor layer, wherein the column spacer comprises the same material as the subsidiary light blocking member.

19. The thin film transistor array panel of claim 17, wherein the subsidiary light blocking member has a thickness less than about 2 μm.

20. The thin film transistor array panel of claim 13, wherein each of the first to third shield electrodes has a width of about 3 μm to about 4 μm.

21. The thin film transistor array panel of claim 20, wherein the width of the second shield electrode is narrower than the first and third shield electrodes.

22. The thin film transistor array panel of claim 13, wherein the second shield electrode is connected to the first and third shield electrodes at an angle of about 30 degrees to about 150 degrees.

23. The thin film transistor array panel of claim 13 further comprising a subsidiary light blocking member disposed on the pixel electrode, the subsidiary light blocking member overlapping the data line.

24. The thin film transistor array panel of claim 23 further comprising a column spacer disposed on the pixel electrode overlapping the semiconductor layer, wherein the column spacer comprises the same material as the subsidiary light blocking member.

25. The thin film transistor array panel of claim 13 further comprising:

a light blocking member disposed on the data line and the drain electrode, the light blocking member covering the data line; and

a color filter disposed on the light blocking member.

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专利名称(译)	薄膜晶体管阵列面板和具有该面板的液晶显示器		
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[标]申请(专利权)人(译)	崔相GUN		
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摘要(译)

根据本发明示例性实施例的液晶显示器包括覆盖第一和第二像素电极之间的空间的彩色辅助光阻挡构件。第一和第三屏蔽电极放置在数据线下面。第一和第三屏蔽电极平行于数据线设置并且彼此跨越数据线。第二屏蔽电极以约30度至约150度的角度连接第一屏蔽电极的底端和第三屏蔽电极的顶端。利用这种结构，防止了像素电极之间的间隙处的漏光和屏蔽电极之间可能的短路。