



US 20090310076A1

(19) **United States**(12) **Patent Application Publication**
Hsieh et al.(10) **Pub. No.: US 2009/0310076 A1**(43) **Pub. Date: Dec. 17, 2009**(54) **THIN FILM TRANSISTOR ARRAY FOR A
LIQUID CRYSTAL DISPLAY DEVICE AND
RELATED MANUFACTURING AND
OPERATION METHODS**(76) Inventors: **Chih-Yung Hsieh, Tainan (TW);
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HOUSTON, TX 77057-2631 (US)**(21) Appl. No.: **12/482,589**(22) Filed: **Jun. 11, 2009**(30) **Foreign Application Priority Data**

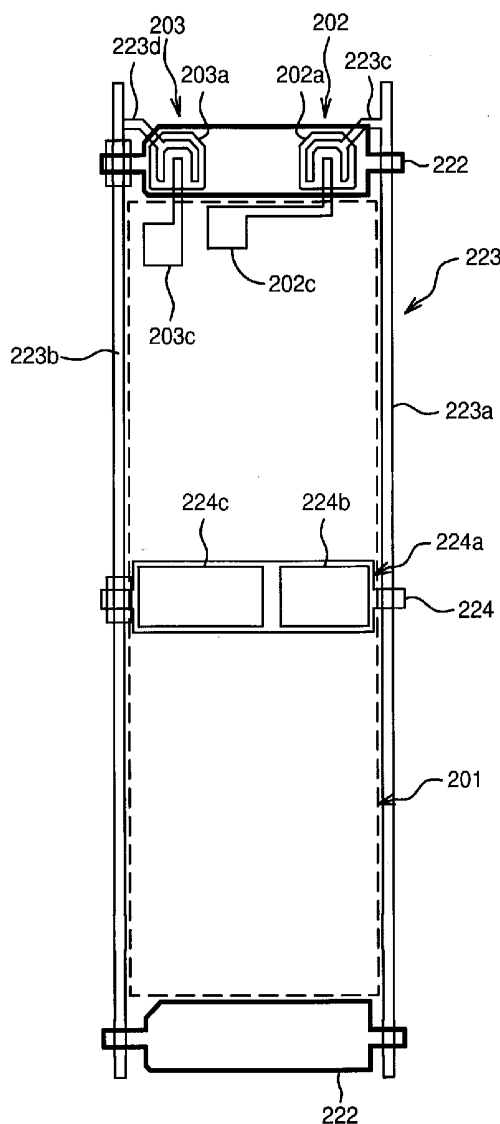
Jun. 11, 2008 (TW) 97121726

Publication Classification(51) **Int. Cl.****G02F 1/1343** (2006.01)**H01L 29/04** (2006.01)**H01L 21/00** (2006.01)(52) **U.S. Cl. 349/144; 257/59; 438/34; 257/E29.003;
257/E33.062; 257/E21.002**

(57)

ABSTRACT

In one embodiment of an invention concerning liquid crystal display devices, a first pixel electrode of a thin film transistor (TFT) array substrate may overlap a slit of a second pixel electrode of the TFT array substrate but not overlap another slit of the second pixel electrode. This may help induce a multi-domain electric field without having to precisely position a common electrode of a color filter substrate and the TFT array substrate. This may prevent position errors, enhance display quality, produce a wider viewing angle, and lower color shift sometimes associated with conventional liquid crystal display devices and methods.



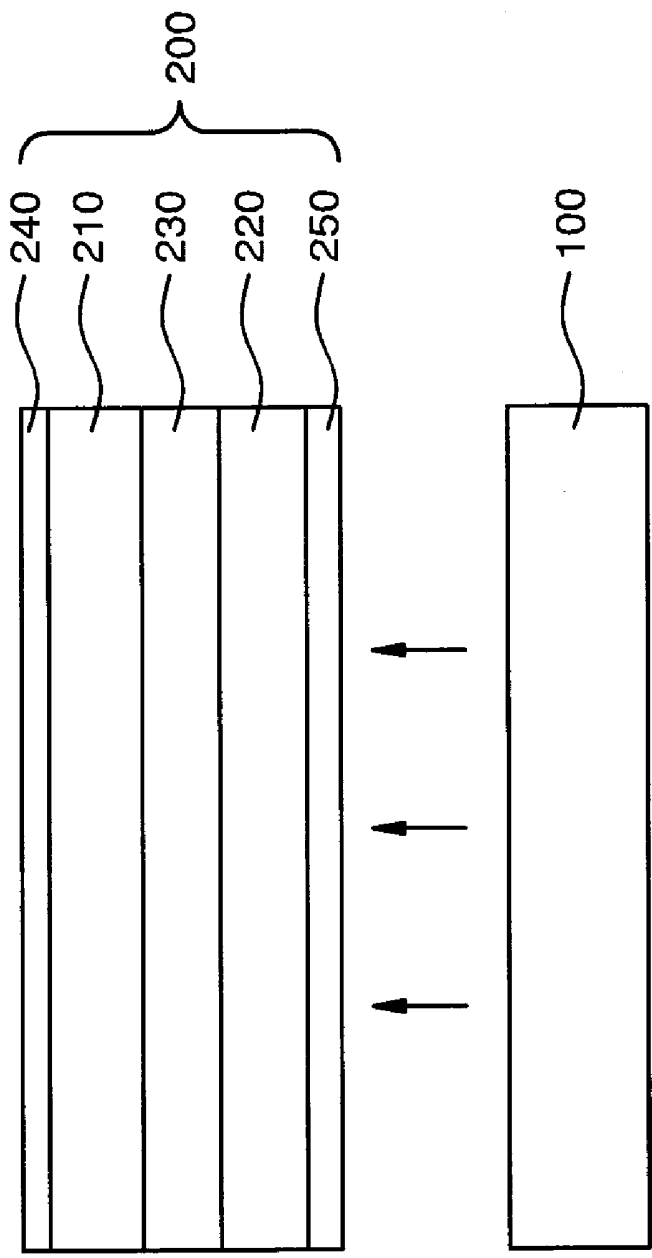


Fig. 1

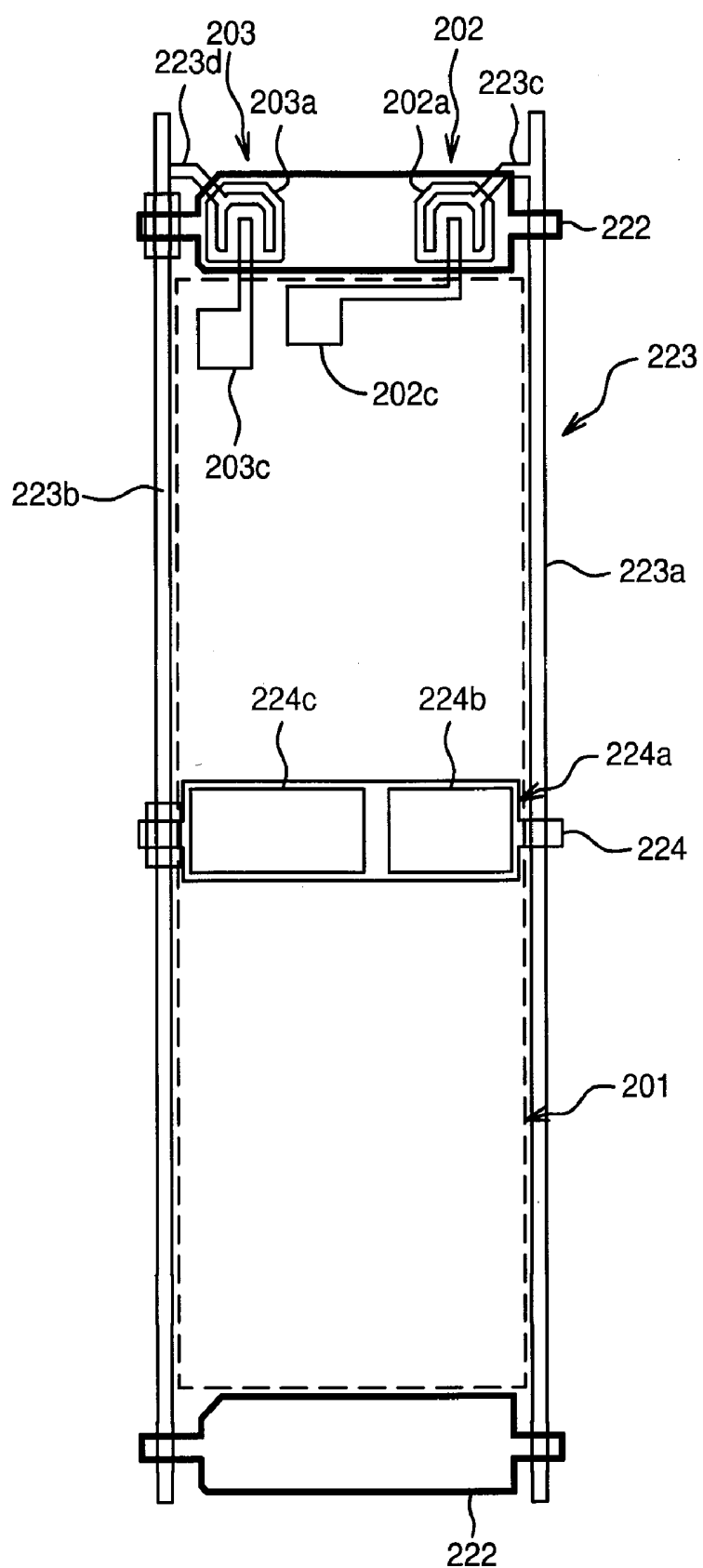


Fig. 2A

225

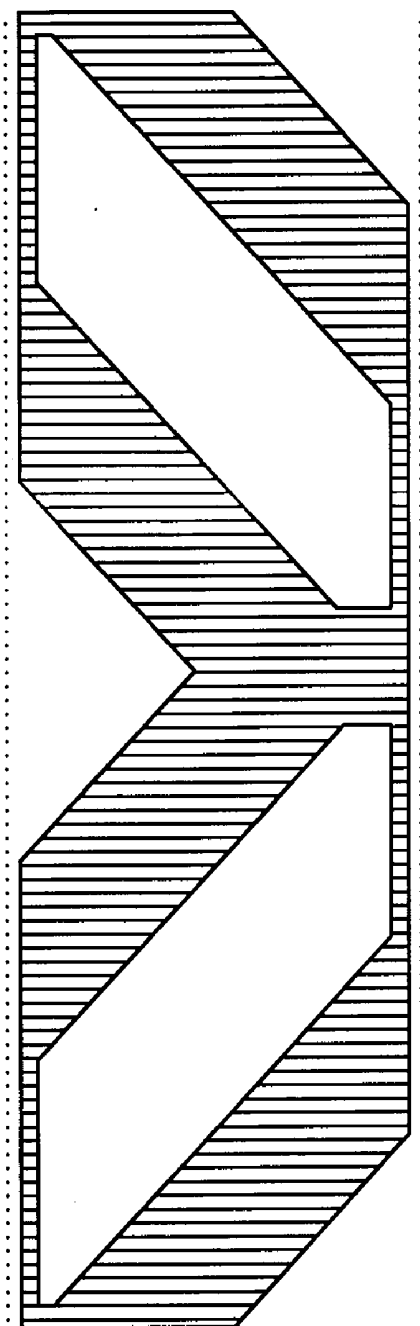


Fig. 2B

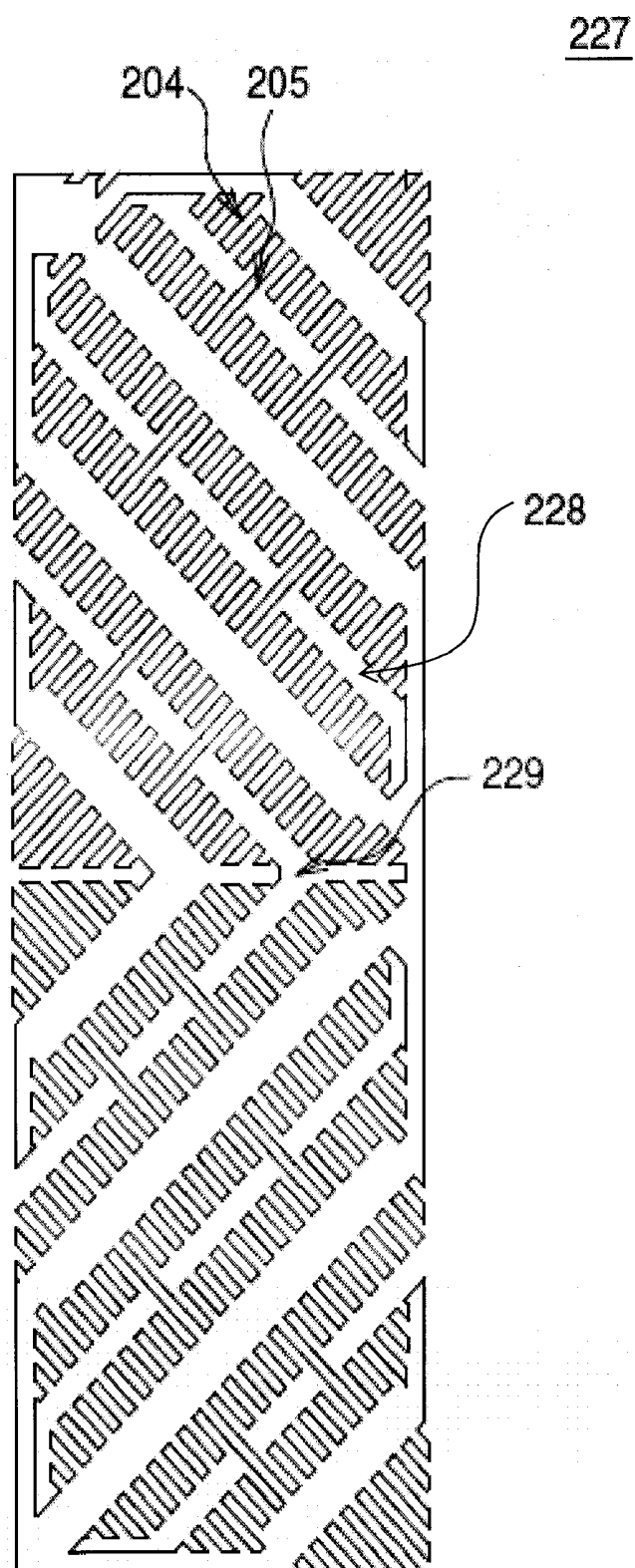


Fig. 2C

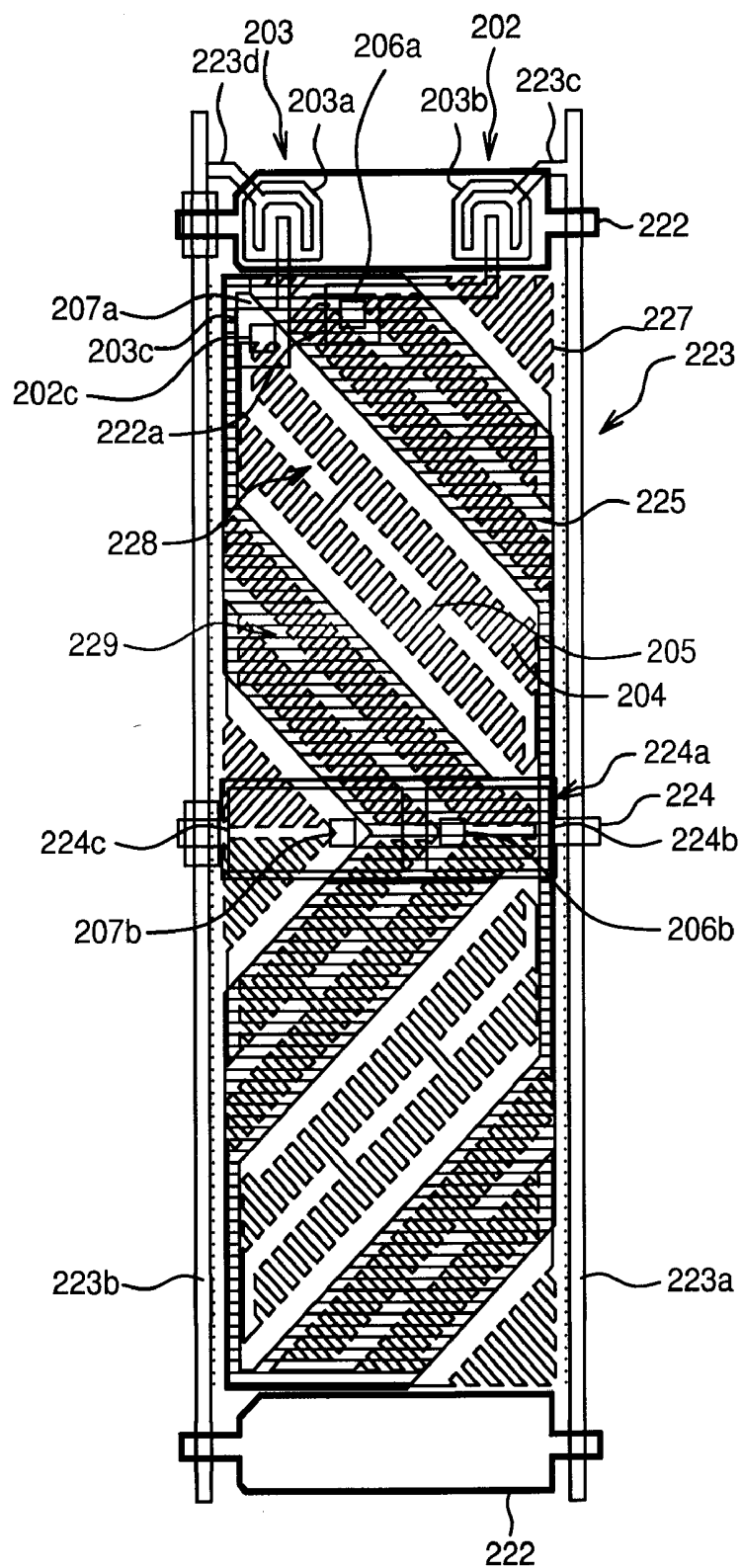


Fig. 2D

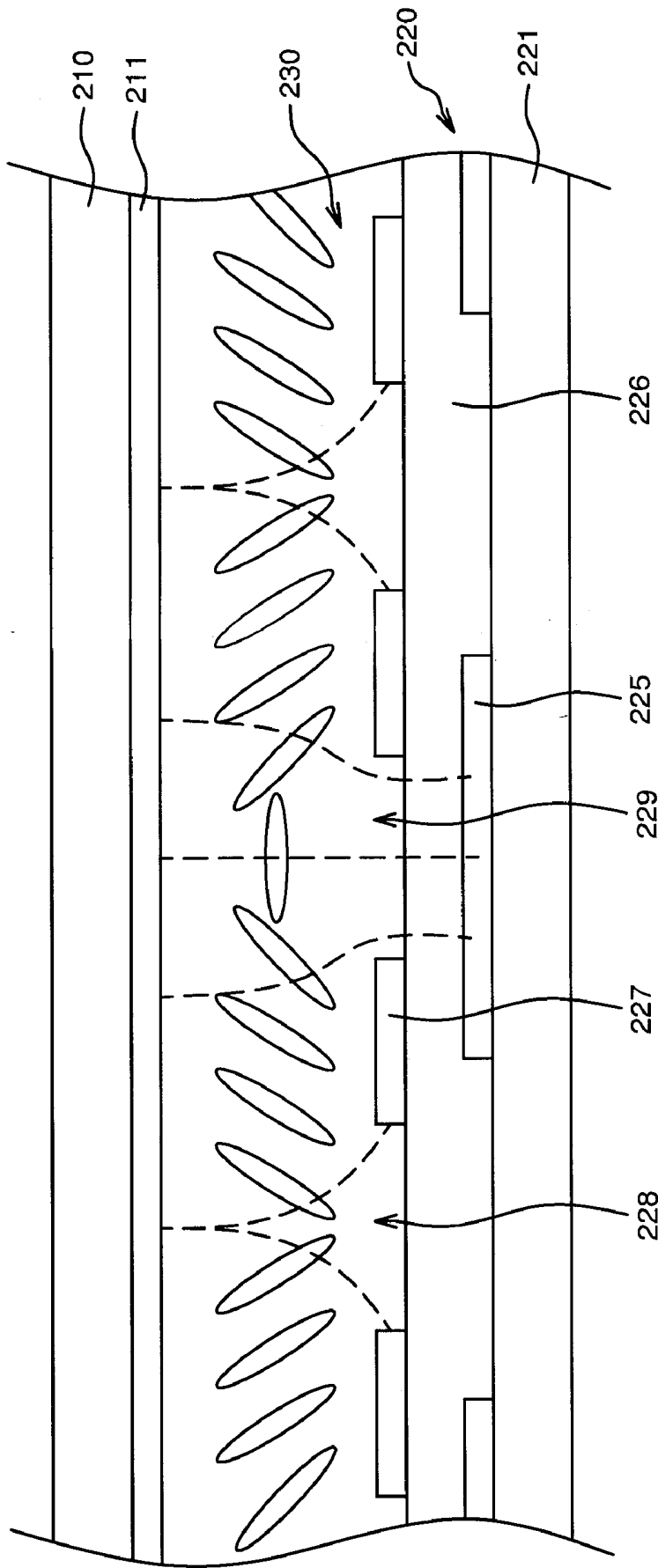


Fig. 3

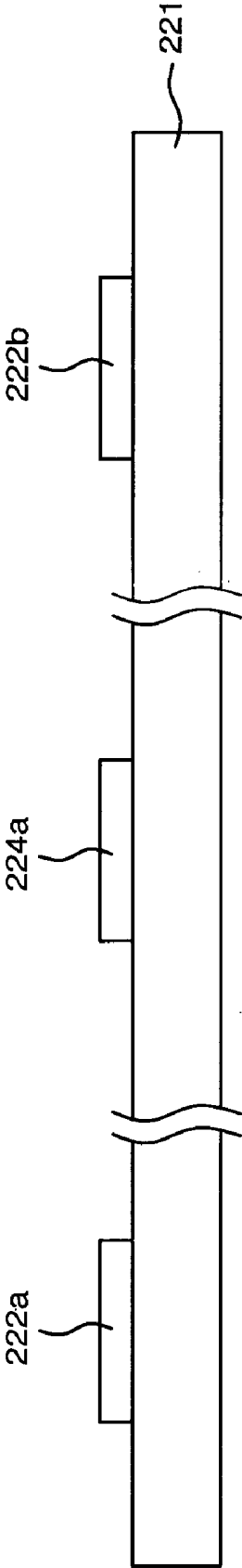


Fig. 4A

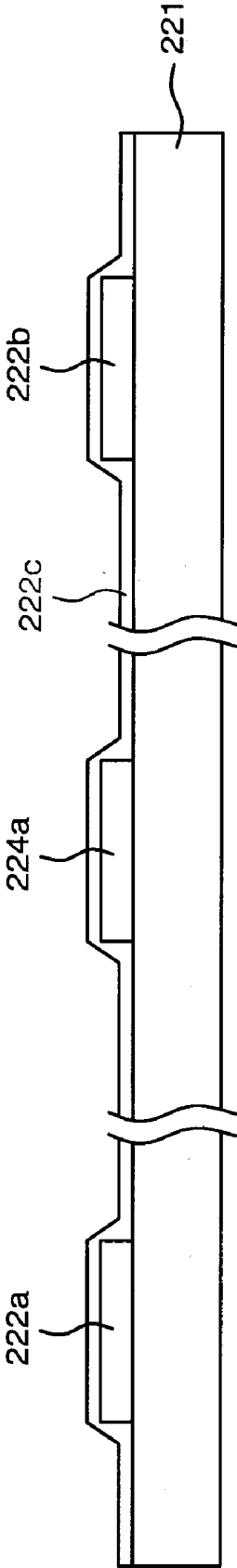


Fig. 4B

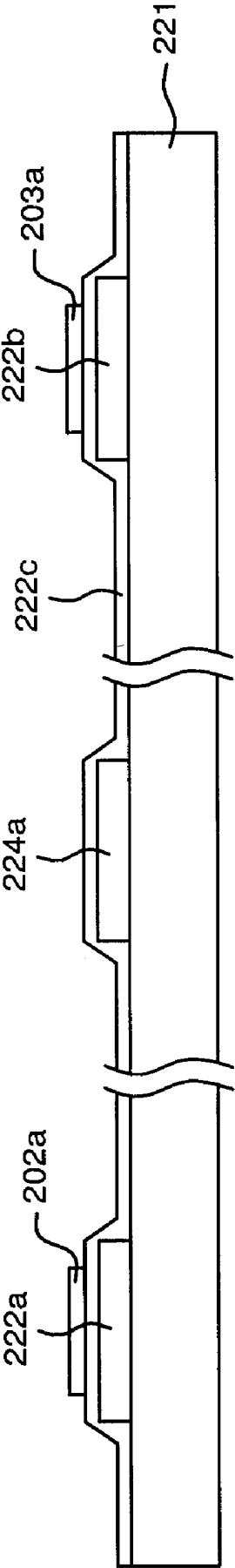


Fig. 4C

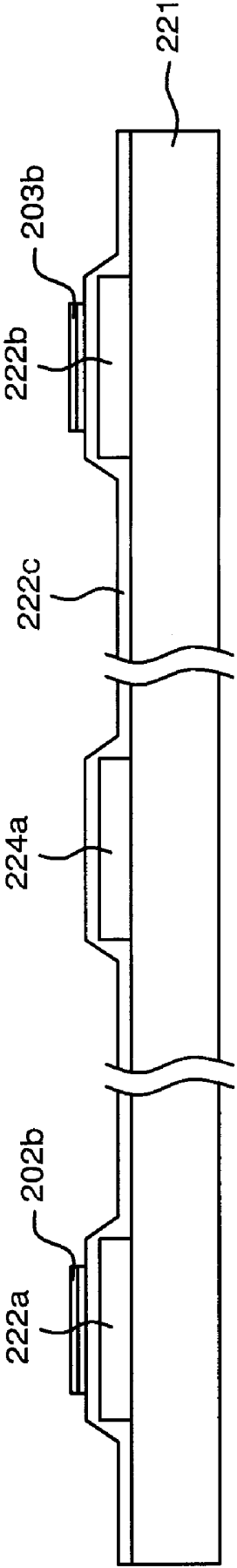


Fig. 4D

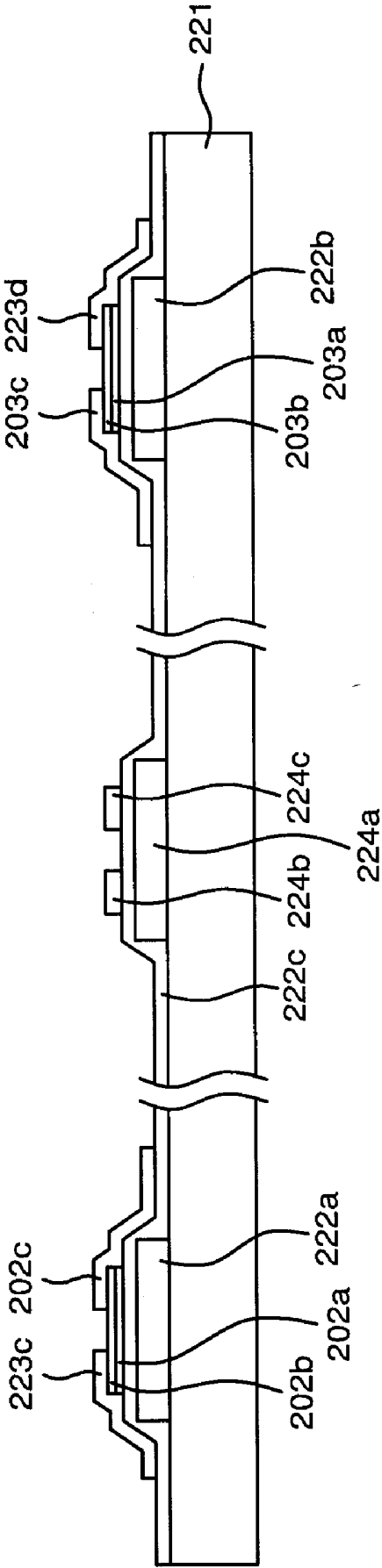


Fig. 4E

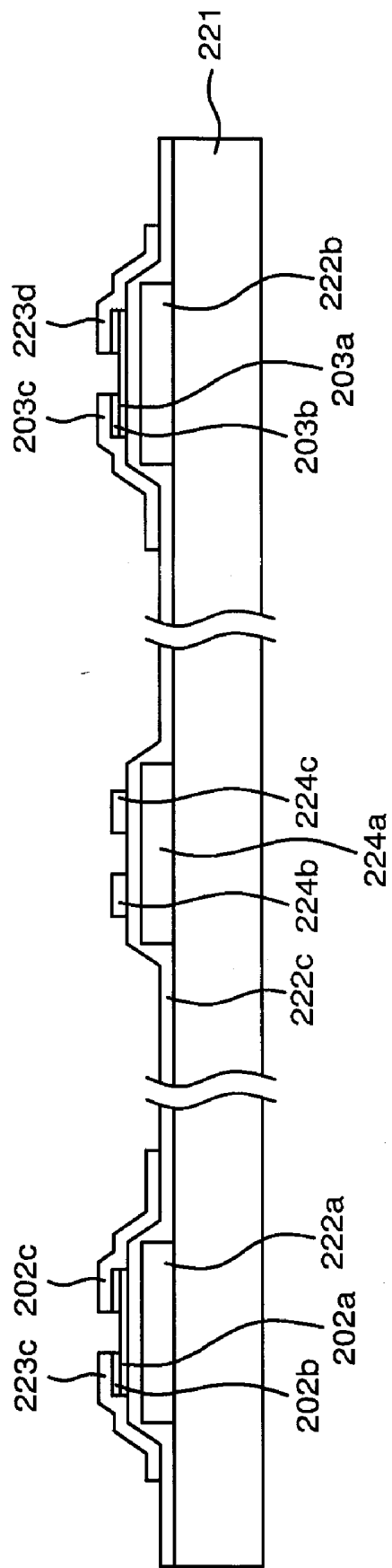


Fig. 4F

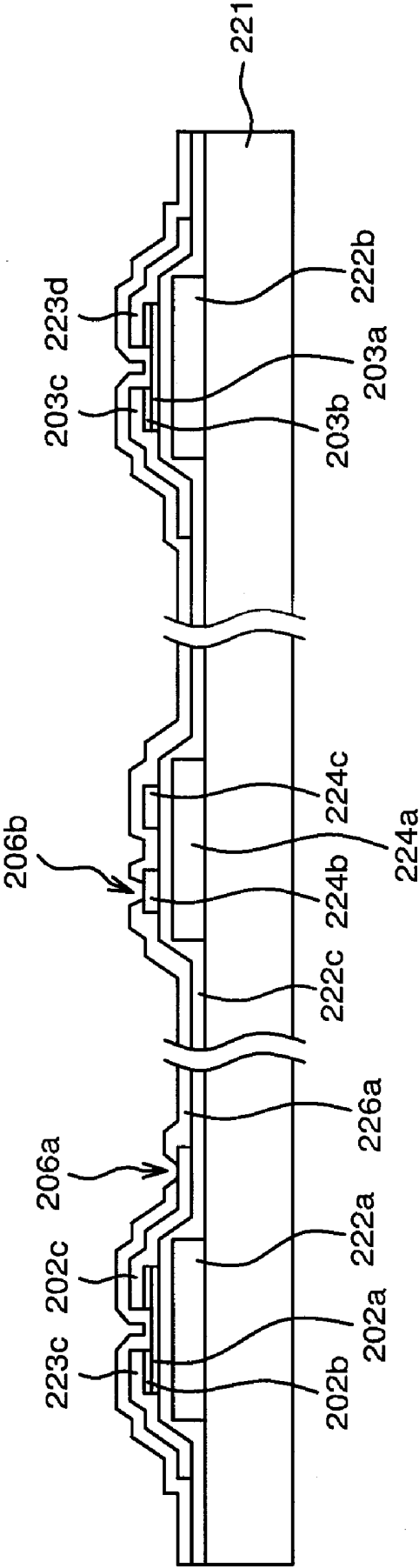


Fig. 4G

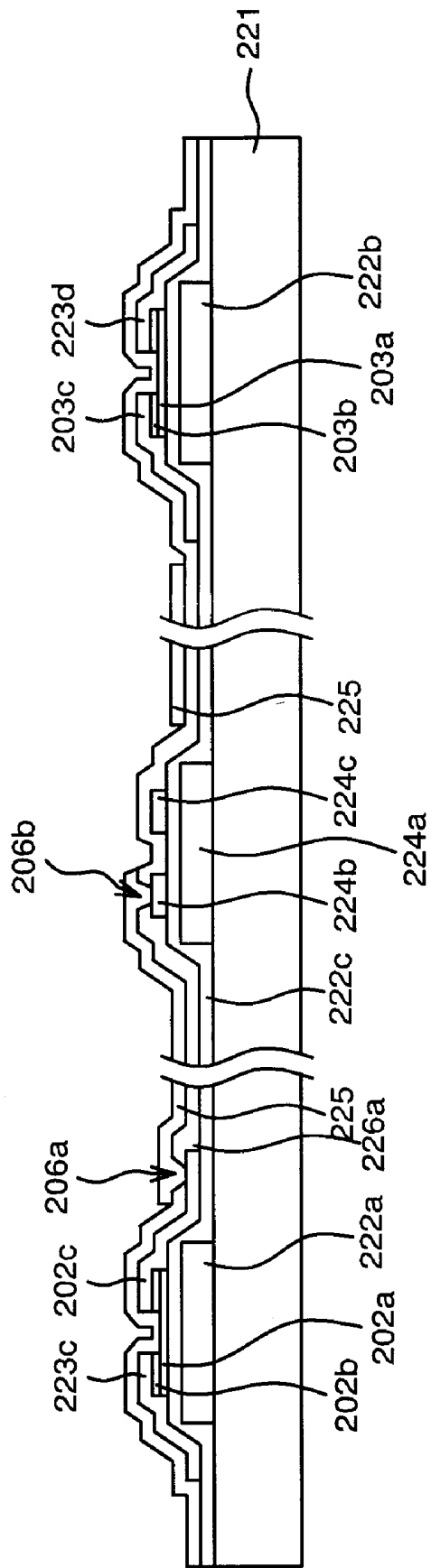


Fig. 4H

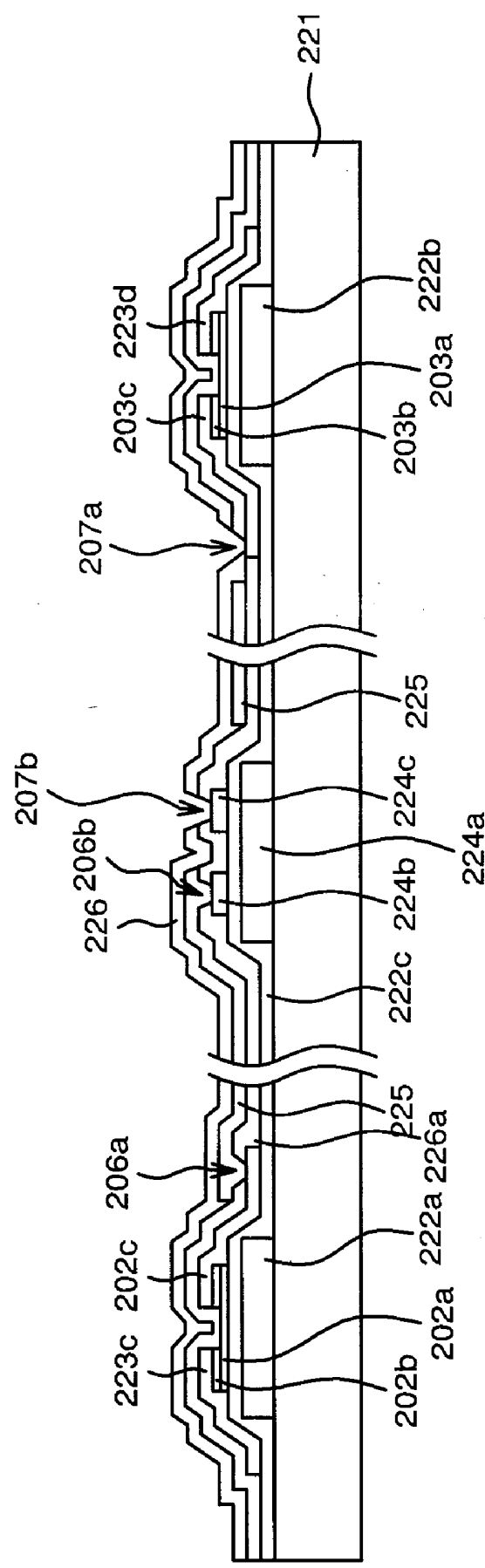


Fig. 4I

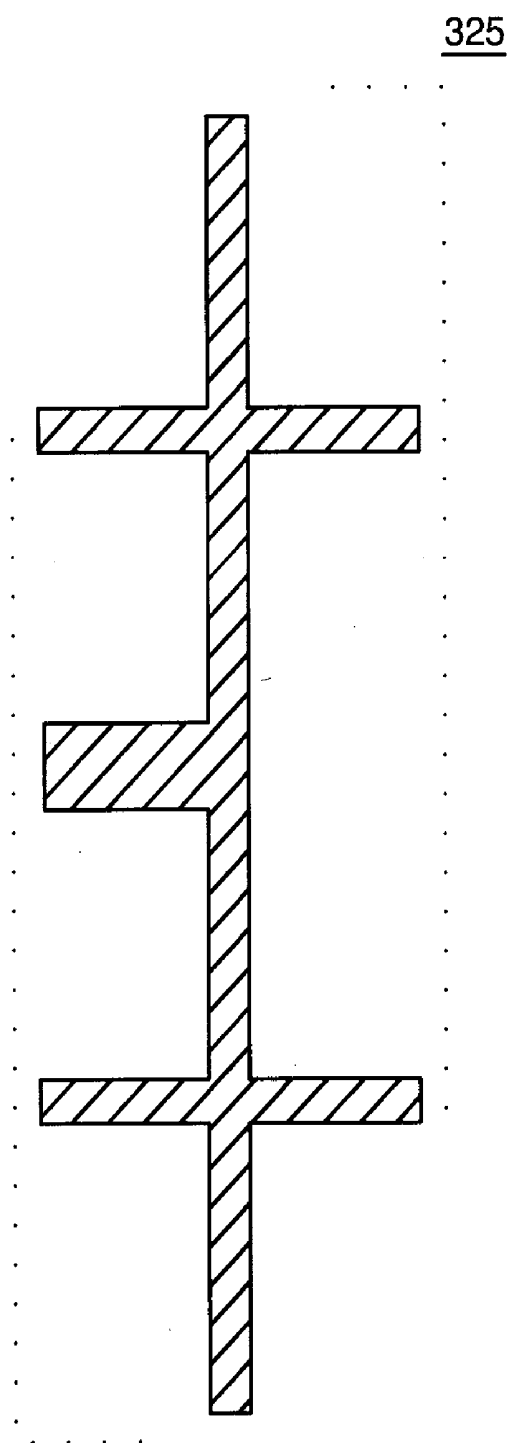


Fig. 5A

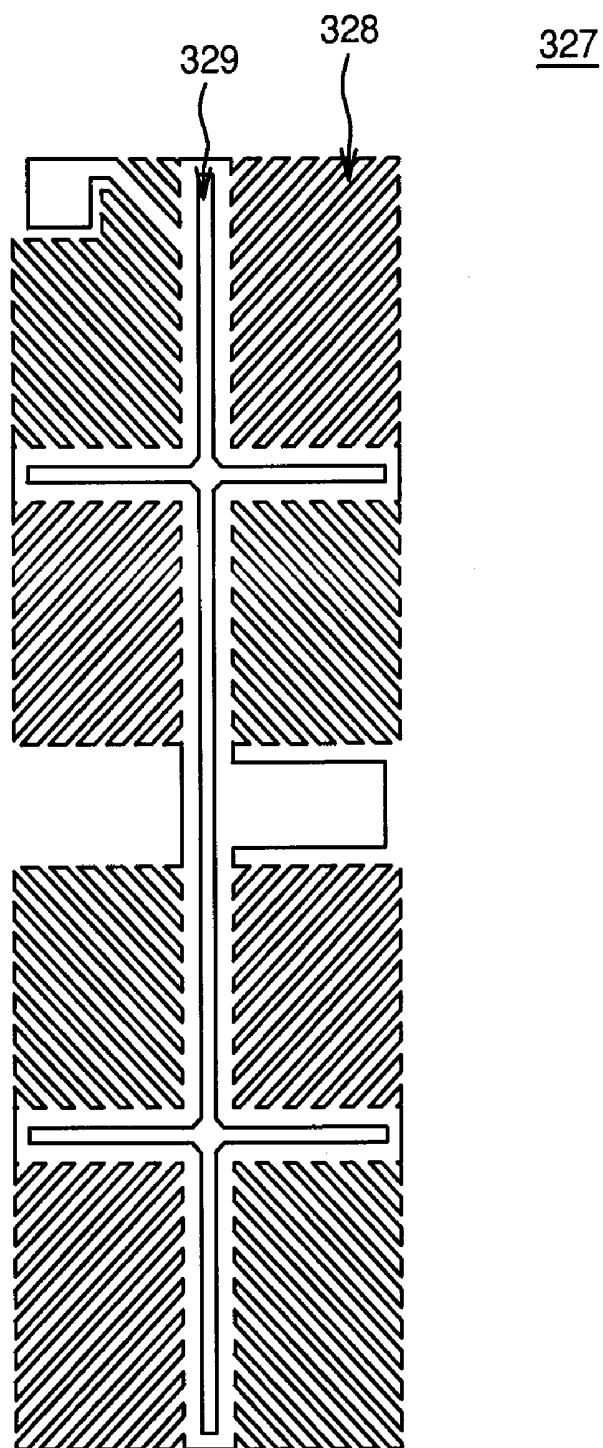


Fig. 5B

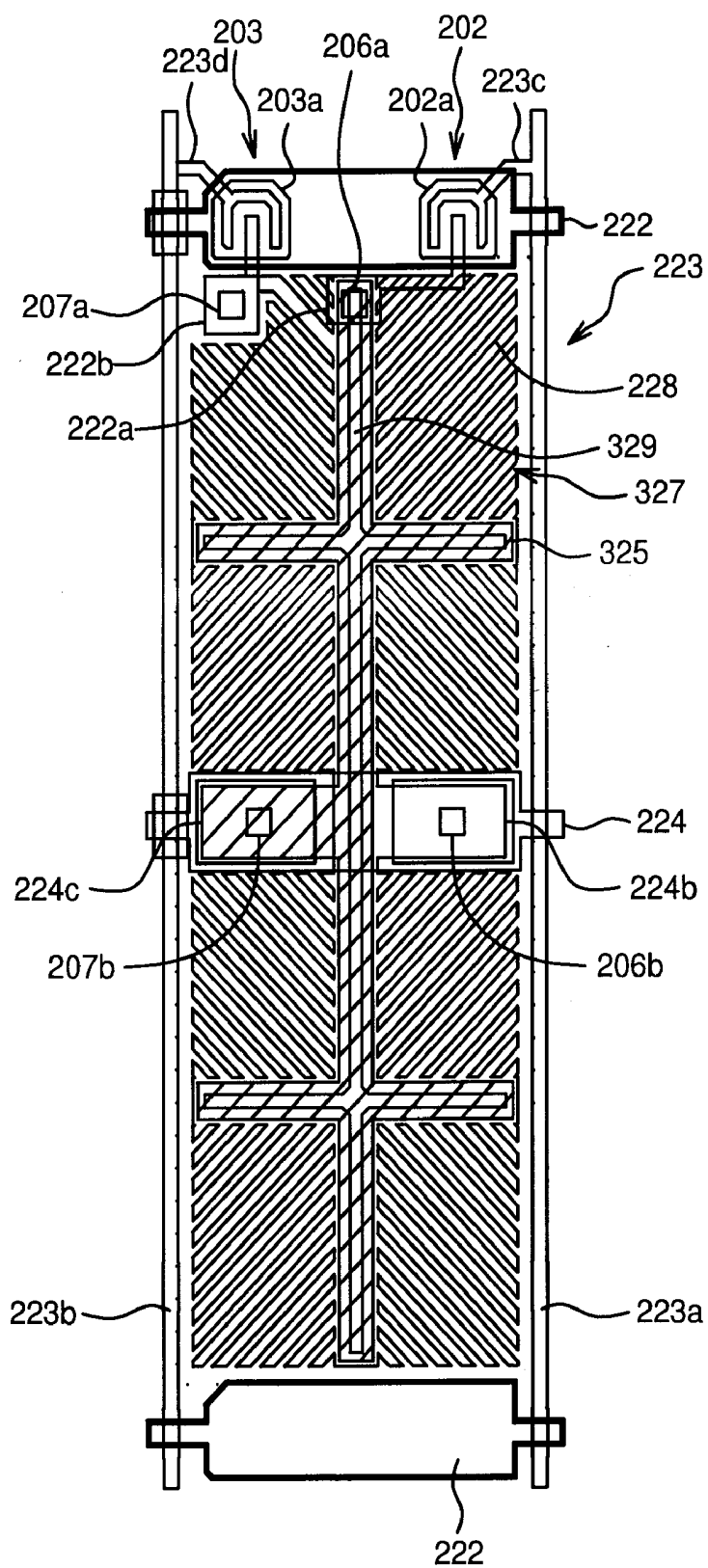


Fig. 5C

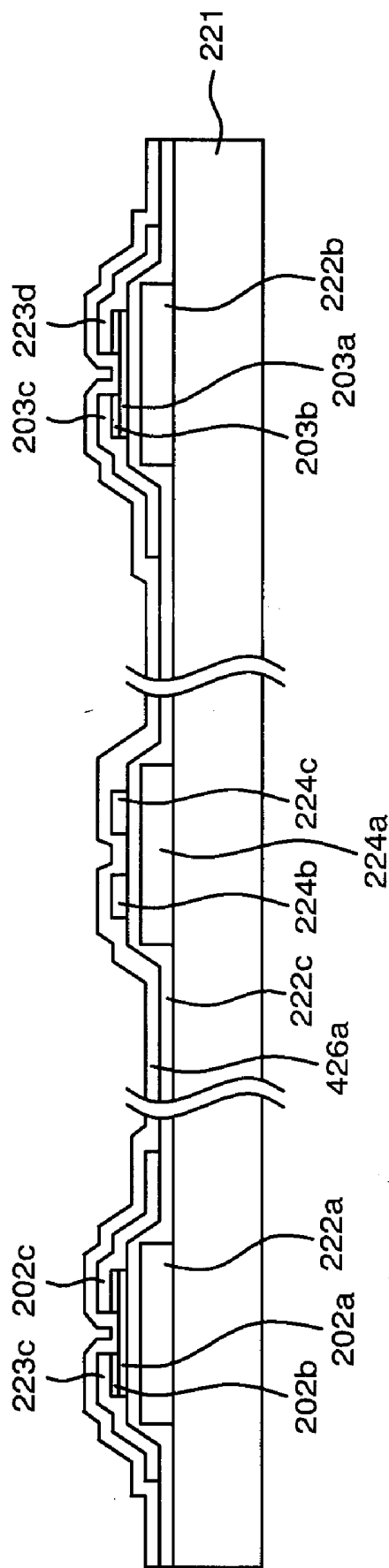


Fig. 6A

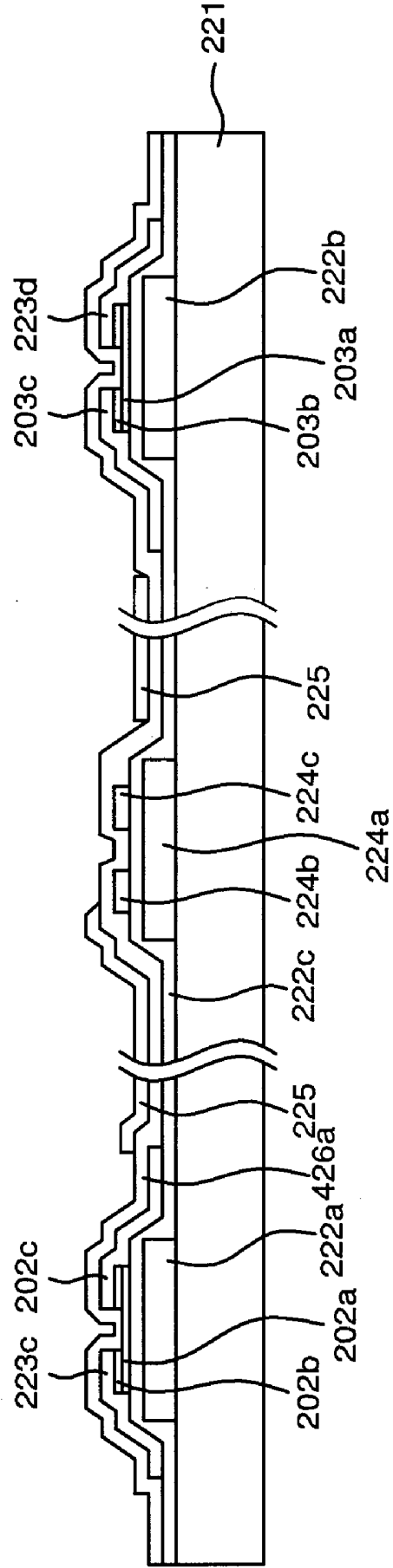


Fig. 6B

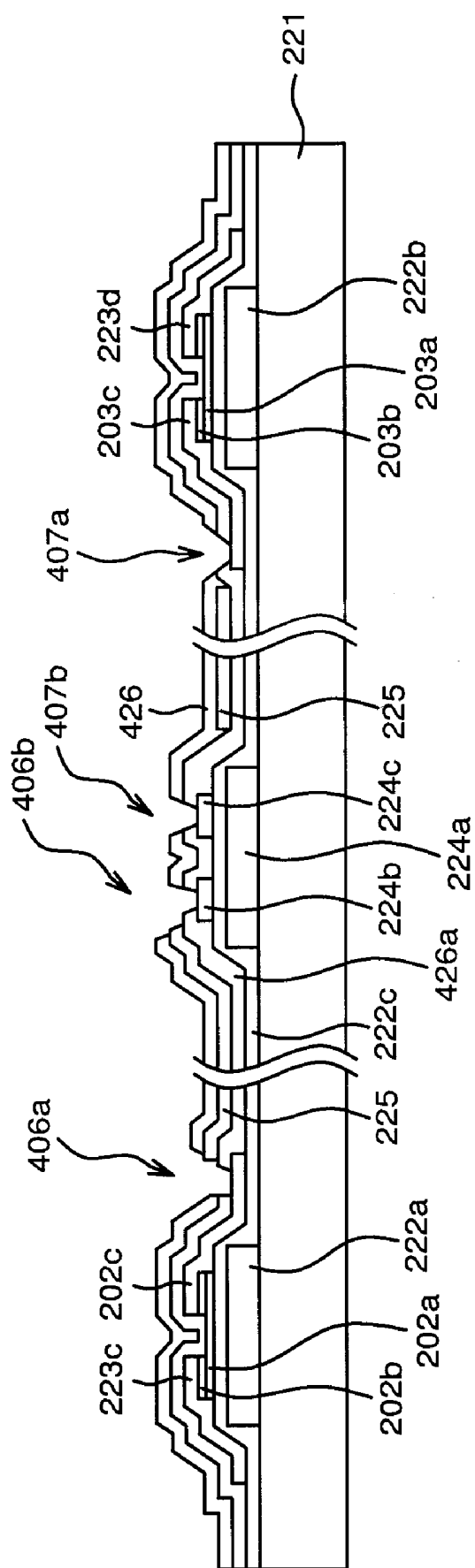


Fig. 6C

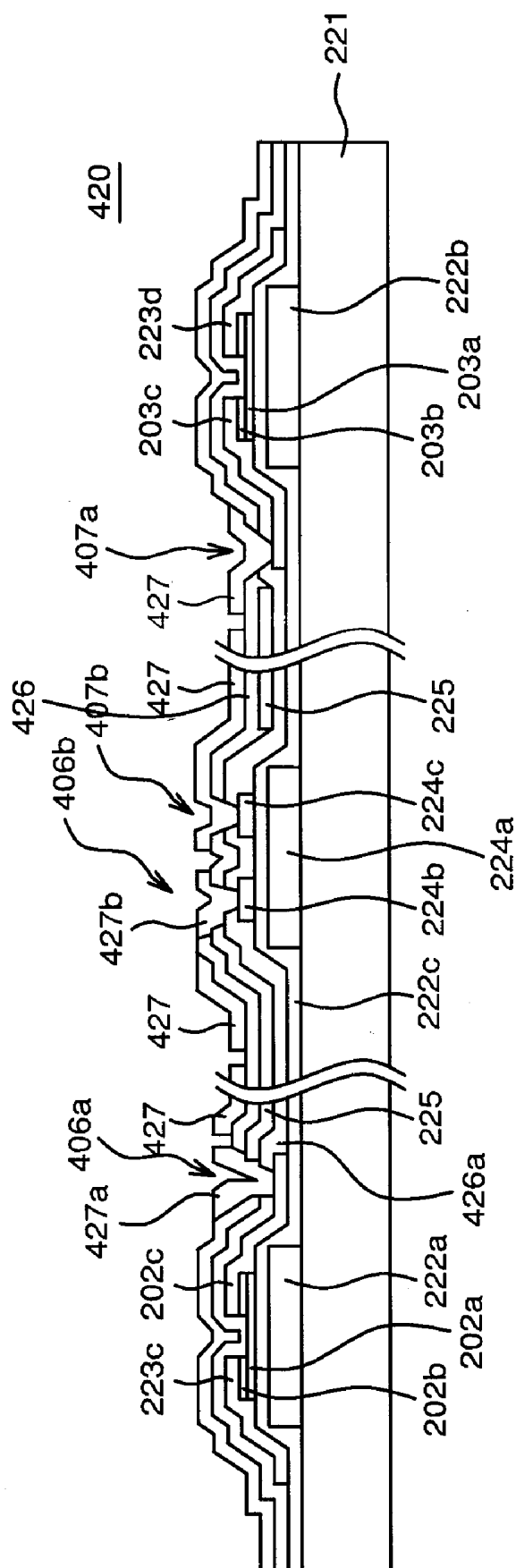


Fig. 6D

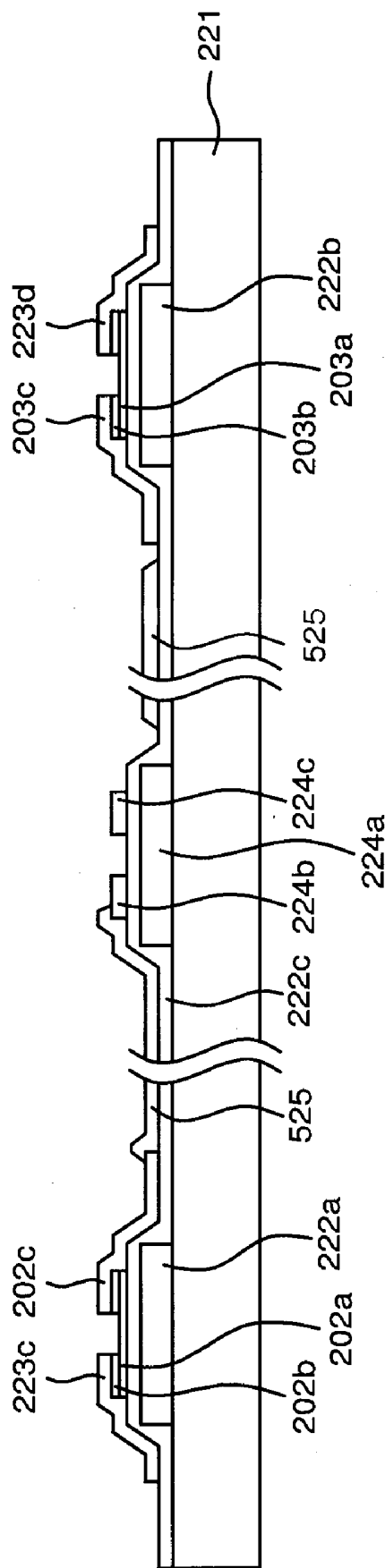


Fig. 7A

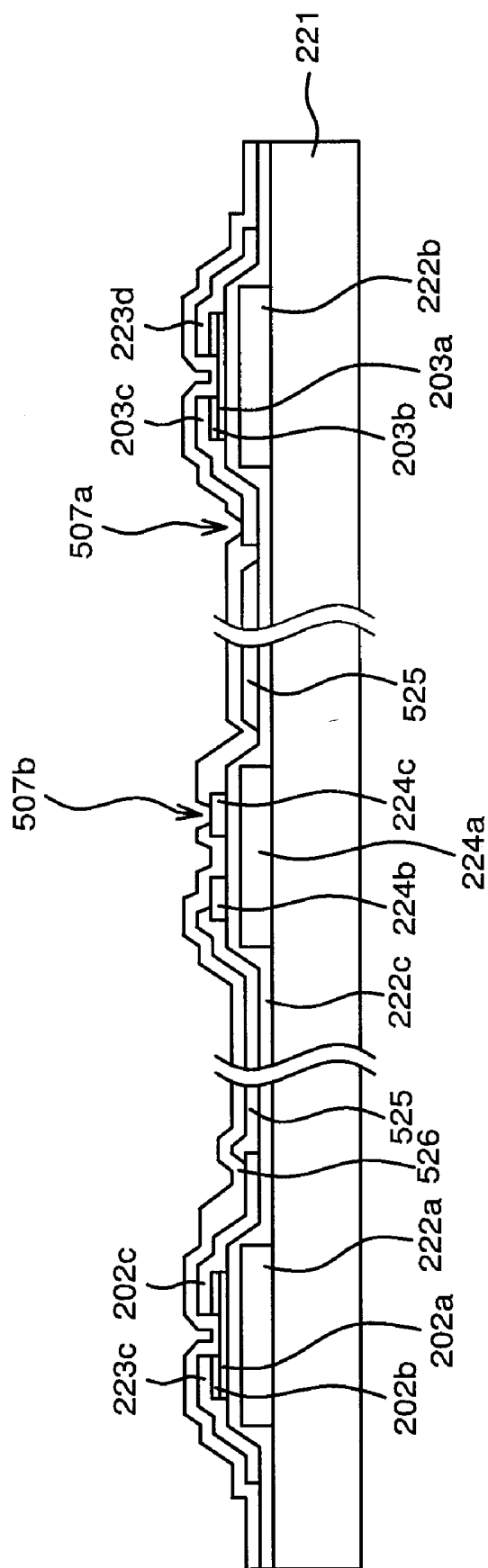


Fig. 7B

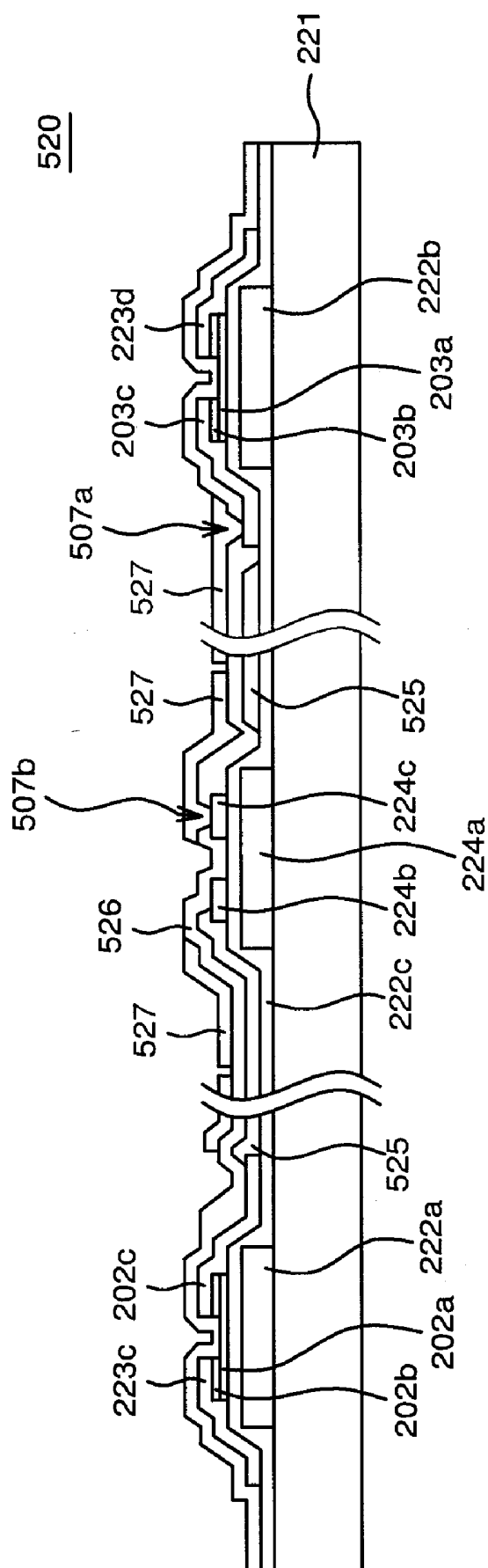


Fig. 7C

THIN FILM TRANSISTOR ARRAY FOR A LIQUID CRYSTAL DISPLAY DEVICE AND RELATED MANUFACTURING AND OPERATION METHODS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] Pursuant to 35 U.S.C. §119, this application claims priority to Taiwan Application Serial No. 97121726, filed Jun. 11, 2008, the subject matter of which is incorporated herein by reference.

BACKGROUND

[0002] Liquid crystal displays (LCD) have been widely applied in electrical products due to the rapid progress of optical and semiconductor technologies. With their advantages of high image quality, compact size, light weight, low driving voltage, and low power consumption, LCDs have been introduced into portable computers, mobile phones, personal digital assistants and color televisions.

[0003] Currently, an LCD panel may include a color filter (CF) substrate and a thin film transistor (TFT) array substrate. The CF substrate may include a plurality of color filters and a common electrode. The TFT array substrate may include parallel scanning lines, parallel data lines, TFTs, and pixel electrodes. The scanning lines may be horizontally aligned and orthogonal to the data lines. An adjacent pair of scanning lines and an adjacent pair of data lines may intersect to define a pixel area.

[0004] Many LCDs utilize liquid crystal (LC) molecule alignments to control ray transmissions and consequently have an inherently narrowed viewing angle, especially with large LCDs. To broaden the viewing angle, one may pattern the Indium Tin Oxide (ITO) electrodes of the CF substrate and the pixel electrodes of the TFT array substrate to establish a plurality of different electrode regions. The different electrode regions may induce a multi-domain electric field to align LC molecules on multi-domains and thereby achieve a broadened view angle.

[0005] However, when the patterned CF and TFT array substrates are assembled, a position error may occur between the two substrates whereby the substrates are not properly oriented with respect to one another. The position error may affect the performance of the assembled LCD panel (e.g., display quality, light transmittance, response time) and may also result in unstable LC molecule alignment and image retention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The accompanying drawings are included to provide a further understanding of various embodiments of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0007] FIG. 1 is a cross-sectional view of an LCD apparatus according to an embodiment of the invention;

[0008] FIG. 2A is a top view of a pixel region of a TFT array substrate according to an embodiment of the invention;

[0009] FIG. 2B is a top view of a pixel electrode of a TFT array substrate according to an embodiment of the invention;

[0010] FIG. 2C is a top view of a pixel electrode of a TFT array substrate according to an embodiment of the invention;

[0011] FIG. 2D is a layout view of a pixel region of a TFT array substrate according to an embodiment of the invention; [0012] FIG. 3 is a partial cross-sectional view of an LCD panel according to an embodiment of the invention;

[0013] FIGS. 4A-J are schematic diagrams for manufacturing a TFT array substrate according to an embodiment of the invention;

[0014] FIG. 5A is a top view of a pixel electrode of a TFT array substrate according to an embodiment of the invention;

[0015] FIG. 5B is a top view of a pixel electrode of a TFT array substrate according to an embodiment of the invention;

[0016] FIG. 5C is a layout view of a pixel region of a TFT array substrate according to an embodiment of the invention;

[0017] FIGS. 6A-D are schematic diagrams for manufacturing a TFT array substrate according to an embodiment of the invention; and

[0018] FIGS. 7A-C are schematic diagrams for manufacturing a TFT array substrate according to an embodiment of the invention.

DETAILED DESCRIPTION

[0019] The following description refers to the accompanying drawings. Among the various drawings the same reference numbers may be used to identify the same or similar elements. While the following description provides a thorough understanding of various aspects of the claimed invention by setting forth specific details such as particular structures, architectures, interfaces, and techniques, such details are provided for purposes of explanation and should not be viewed as limiting. Moreover, those of skill in the art will, in light of the present disclosure, appreciate that various aspects of the invention claimed may be practiced in other examples or implementations that depart from these specific details. At certain junctures in the following disclosure descriptions, well known devices, circuits, and methods have been omitted to avoid clouding the description of various embodiments of the invention with unnecessary detail.

[0020] FIG. 1 is a cross-sectional view of an LCD apparatus according to an embodiment of the invention. The LCD apparatus includes backlight module 100 and LCD panel 200. Backlight module 100 may be disposed opposite to LCD panel 200. Backlight module 100 may be, for example, an edge or bottom lighting backlight module. Backlight module 100 may include one or more optical films (not shown) for optical performance improvement. The one or more optical films may include, for example, a diffuser, prism sheet, turning prism sheet, brightness enhancement film, dual brightness enhancement film, diffused reflective polarizer film or any combination thereof. The light source (not shown) of backlight module 100 may be, for example, a cold cathode fluorescent lamp (CCFL), hot cathode fluorescent lamp (HCFL), light-emitting diode (LED), organic light emitting diode (OLED), or electro-luminescence (EL) to provide LCD panel 200 with lighting.

[0021] LCD panel 200 may include CF substrate 210, TFT array substrate 220, LC layer 230, first polarizer 240, and second polarizer 250. CF substrate 210 may be disposed opposite TFT array substrate 220. LC layer 230 may be formed between CF substrate 210 and TFT array substrate 220. TFT array substrate 220 may include an alignment layer (e.g. polyimide) in contact with LC layer 230 for orientation of LC molecules. First polarizer 240 may be disposed on one side of CF substrate 210 and opposite to a light-emitting side of TFT array substrate 220. Second polarizer 250 may be

disposed on one side of TFT array substrate **220** and opposite to a light-incident side of CF substrate **210**. When backlight module **100** provides LCD panel **200** with backlighting, the backlight may pass through LCD panel **200** from second polarizer **250** to first polarizer **240**. In some embodiments of the invention, a CF and TFT array may be disposed on the same substrate, such as a CF on array (COA).

[0022] In various embodiments of the invention, FIG. 2A is a top view of a pixel region of a TFT array substrate, FIG. 2B is a top view of first pixel electrode **225**, FIG. 2C is a top view of second pixel electrode **227**, FIG. 2D is a layout view of a pixel region of a TFT array substrate, and FIG. 3 is a partial cross-sectional view of an LCD panel.

[0023] Regarding FIGS. 2A-D and 3, TFT array substrate **220** may include substrate **221**, gate line or lines **222**, data line or lines **223**, and storage capacitor line or lines **224**. Substrate **221** may include, for example, a glass substrate or a flexible transparent substrate. Gate lines **222** and data lines **223** may be orthogonally oriented with one another (e.g., crisscrossed) on the substrate, thereby forming numerous pixel regions **201** arranged on the array. Each pixel region **201** may include at least one TFT to be electrically connected to adjacent gate line **222** and adjacent data line **223**. The material of gate lines **222** and storage capacitor lines **224** may include, for example, Al, Ag, Cu, Mo, Cr, W, Ta, Ti, and/or alloys thereof. The material of data lines **223** may include, for example, Mo, Cr, Ta, T, and/or alloys thereof. In one embodiment of the invention, the material of data lines **223** is heat-resistant metal. Storage capacitor lines **224** may be parallel (i.e., generally parallel) to gate lines **222** and may form storage capacitors, each of which may be disposed in pixel regions **201** to maintain the voltage of first pixel electrodes **225** and second pixel electrodes **227** within a predetermined range for a predetermined period after shutting down (i.e., turning off) the TFT.

[0024] Pixel region **201** may include first pixel electrode **225** and second pixel electrode **227**. Electrodes may include, for example, electrically conductive and transparent material, such as ITO, indium zinc oxide (IZO), aluminum zinc oxide (AZO), gallium-doped zinc oxide (GZO), transparent conducting oxide (TCO), or zinc oxide (ZnO).

[0025] In one embodiment of the invention, gate lines **222**, data lines **223**, first pixel electrodes **225**, and second pixel electrodes **227** may be formed individually. In one embodiment of the invention, the material for gate lines **222** and/or data lines **223** may be different from the material included in first pixel electrodes **225** and the second pixel electrodes **227**. In one embodiment of the invention, a resistance of the material included in gate lines **222** and/or data lines **223** may be different (e.g., lower) than a resistance of the material included in first pixel electrodes **225** and/or second pixel electrodes **227**.

[0026] First pixel electrodes **225** may be formed on substrate **221**. Electrode insulating layer **226** may be formed on first pixel electrodes **225**. Second pixel electrodes **227** may be formed on electrode insulating layer **226** and insulated from first pixel electrodes **225**. In one embodiment of the invention, one or more first pixel electrodes **225** may be formed in a V-shape. First pixel electrodes **225** may include openings or slits. In one embodiment of the invention, the area of each first pixel electrode **225** may be generally in a range from $\frac{1}{3}$ to $\frac{1}{2}$ of the area of each pixel region **201**. The material of the electrode insulating layer **226** may be transparent insulating

material, such as inorganic insulating material (e.g., silicon nitride or silicon oxide), organic insulating material, and/or any combination thereof.

[0027] In one embodiment of the invention, second pixel electrodes **227** may be positioned based on the location of first pixel electrodes **225**. One or more second pixel electrodes **227** may include at least one first slit or opening **228** and at least one second slit or opening **229**. First slit **228** and each first pixel electrode **225** may be “non-overlapped.” In other words, no single vertical axis intersects both first slit **228** and first pixel electrode **225**. Second slit **229** may be formed in a “V” shape and may correspond to first pixel electrode **225** so that second slit **229** “overlaps” with first pixel electrode **225**. In other words, a single vertical axis intersects both first slit **228** and first pixel electrode **225**, but first slit **228** does not necessarily contact first pixel electrode **225** directly. For example, in one embodiment of the invention first slit **228** of second pixel electrode **227** may be formed over an opening of first pixel electrode **225** (e.g., non-hashed space in FIG. 2B) and thus, first slit **228** of second pixel electrode **227** and first pixel electrode **225** may be “non-overlapped.” In an embodiment of the invention, a slit (e.g., **228** in FIG. 2c) may be an “enclosed slit” such that the slit includes a contiguous perimeter defined by second pixel electrode **227**.

[0028] In one embodiment of the invention, LC layer **230**, sandwiched between CF substrate **210** and TFT array substrate **220**, may be operated in a vertical-alignment mode.

[0029] In FIG. 2D first TFT **202** and second TFT **203** may be disposed in each pixel region **201**. First pixel electrode **225** may be electrically connected to first TFT **202**. Second pixel electrode **227** may be electrically connected to second TFT **203**. Storage capacitor line **224** may include one or more storage electrodes **224a**. One or more first auxiliary storage metallic layers **224b** and one or more second auxiliary storage metallic layers **224c** may be disposed in each pixel region **201** and on (i.e., over) storage electrode **224a**. An insulating layer may be formed for auxiliary storage metallic layers **224b** and **224c** and storage electrode **224a** to enhance the capacitance of the storage capacitor. Data lines **223** may include one or more first data lines **223a** and one or more second data lines **223b**, wherein first data line **223a** may include first source electrode **223c** and second data line **223b** may include second source electrode **223d**. First TFT **202** may electrically connect to gate line **222** and first data line **223a**, and second TFT **203** may electrically connect to gate line **222** and second data line **223b**.

[0030] In one embodiment of the invention, first slit **228** and second slit **229** of second pixel electrode **227** may include one or more finger-shaped structures **204** and one or more connection portions **205**. Finger-shaped structures **204** may be formed in first slit **228** and/or second slit **229** for improving optical characteristics. Connection portions **205** may be formed in first slit **228** and/or second slit **229** to form one or more sub-slits to, for example, limit and control singular points formed in LC layer **230** to reduce image retention.

[0031] In one embodiment of the invention, when inducing a multi-domain electric field first pixel electrode **225** may electrically connect to a first voltage level from first TFT **202**, and second pixel electrode **227** may electrically connect to a second voltage level from second TFT **203**. The first voltage level may be different (e.g., higher) than the second voltage level. Also, the electric field between common electrode layer **211** of CF substrate **210** and second pixel electrodes **227** of TFT array substrate **220** may be adjusted to induce a multi-

domain electric field and thereby broaden the view angle. Furthermore, since first pixel electrode 225 may overlap second slit 229 of second pixel electrode 227, but not overlap first slit 228 of second pixel electrode 227, an electric field relative to first slit 228 can differ from the electric field relative to second slit 229. Thus, the deflection angles of the LC molecules relative to first slits 228 and second slits 229 may differ from each other. Thus, optical transmittances of LC layer 230 relative to first slits 228 and second slits 229 may differ from each other and may lower any color shift in pixel regions 201 and/or enhance colorific quality and achieve a wider viewing angle. Thus, both slits 228, 229 contribute to the transmittances of the pixel in one embodiment of the invention.

[0032] FIGS. 4A-J are schematic diagrams for manufacturing a TFT array substrate according to an embodiment of the invention. First substrate 221 is provided. First TFTs 202, second TFTs, first storage capacitors and second storage capacitors may be formed on substrate 221. Gate lines 222 and storage capacitor lines 224 may be formed on substrate 221, and first gate electrodes 222a, second gate electrodes 222b, and storage electrodes 224a may be formed on substrate 221. First gate electrode 222a and second gate electrode 222b may be portions of gate line 222. First gate electrode 222a may correspond to first TFT 202 and second gate electrode 222b may correspond to second TFT 203.

[0033] In FIG. 4B gate insulating layer 222c may be formed on first gate electrode 222a, second gate electrode 222b, and storage electrode 224a. Gate insulating layer 222c may include, for example, silicon nitride and/or silicon oxide which may be formed with plasma enhanced chemical vapor deposition (PECVD).

[0034] In FIG. 4C first semiconductor island 202a and second semiconductor island 203a may be formed on gate insulating layer 222c. First semiconductor island 202a may be disposed on (i.e., over) first gate electrode 222a and second semiconductor island 203a may be disposed on second gate electrode 222b. First semiconductor island 202a and second semiconductor island 203a may be made of, for example, amorphous silicon (a-Si) and/or polycrystalline silicon.

[0035] In FIG. 4D first ohmic contact layer 202b may be formed on first semiconductor island 202 and second ohmic contact layer 203b may be formed on second semiconductor island 203a. First ohmic contact layer 202b and second ohmic contact layer 203b may include N+ a-Si (or silicide) heavily doped with N dopant (such as phosphorous) using, for example, ion implantation or chemical vapor deposition methods.

[0036] In FIG. 4E first data line 223a (not shown), second data line 223b (not shown), first drain electrode 202c, second drain electrode 203c, first auxiliary storage metallic layer 224b, and second auxiliary storage metallic layer 224c may be formed. First source electrode 223c and first drain electrode 202c of first data line 223a may be formed on first ohmic contact layer 202b. Second source electrode 223d and second drain electrode 203c of second data line 223b may be formed on second ohmic contact layer 203b. First auxiliary storage metallic layer 224b and second auxiliary storage metallic layer 224c may be formed on gate insulating layer 222c and positioned above storage electrode 224a. A metallic layer may be formed and patterned using photolithography and etching to form first data line 223a, second data line 223b, first drain electrode 202c, second drain electrode 203c, first auxiliary storage metallic layer 224b, and second auxiliary storage metallic layer 224c. In one embodiment of the inven-

tion, the metallic layer may include Mo, Al, Cr, Ta, Ti and/or alloys thereof. Furthermore, the metallic layer may be a multi-layer structure with heat-resistant film and lower resistance film, such as a dual-layer structure with molybdenum nitride and Al films. First auxiliary storage metallic layer 224b, gate insulating layer 222c, and storage electrode 224a may form a first storage capacitor and second auxiliary storage metallic layer 224c, gate insulating layer 222c, and storage electrode 224a may form a second storage capacitor.

[0037] In FIG. 4F portions of first ohmic contact layer 202b, between first source electrode 223c and first drain electrode 202c, may be removed, and portions of second ohmic contact layer 203b, between second source electrode 223d and second drain electrode 203c, may be removed. Also, portions of first semiconductor island 202a and second semiconductor island 203a may be exposed to form channels for first TFT 202 and second TFT 203.

[0038] In FIG. 4G insulating layer 226a may be formed on first TFT 202, second TFT 203, and the first and second storage capacitors. Insulating layer 226a may include a plurality of first contact holes 206a and 206b which may respectively expose portions of first drain electrode 202c and portions of first auxiliary storage metallic layer 224b. First contact holes 206a and 206b may include, for example, inclined or ladder-shaped sidewalls.

[0039] In FIG. 4H first pixel electrode 225 may be formed on insulating layer 226a and cover first contact holes 206a and 206b to electrically connect respectively to first drain electrode 202c of first TFT 202 and first auxiliary storage metallic layer 224b of the first storage capacitor.

[0040] In FIG. 4I electrode insulating layer 226 may be formed on insulating layer 226a and first pixel electrode 225. Electrode insulating layer 226 may include second contact holes 207a and 207b which may respectively expose portions of second drain electrode 203c and second auxiliary storage metallic layer 224c. Second contact holes 207a and 207b may include, for example, inclined or ladder-shaped sidewalls.

[0041] In FIG. 4J, second pixel electrode 227 may be formed on electrode insulating layer 226 and cover second contact holes 207a and 207b to electrically connect respectively to second drain electrode 203c of second TFT 203 and second auxiliary storage metallic layer 224c of the second storage capacitor to form TFT array substrate 220.

[0042] In one embodiment of the invention, an alignment layer and/or film may be formed on second pixel electrode 227 to lead or align the LC molecules in a vertical-alignment mode. First pixel electrode 225 and second pixel electrode 227 of TFT array substrate 220 may partially overlap to induce a multi-domain electric field without patterning or having to be precisely positioned with regard to the common electrode of the CF substrate. This may consequently prevent position errors and enhance display quality. Furthermore, TFT array substrate 220 may produce a wider viewing angle and lower color shift than associated with conventional devices and methods.

[0043] FIGS. 5A-B respectively include top views of first and second pixel electrodes of a TFT array substrate according to an embodiment of the invention. FIG. 5C is a layout view of a pixel region of a TFT array substrate according to an embodiment of the invention. Some reference numerals addressed above may be the same as used in FIGS. 5A-C. Construction for electrodes and pixel region of FIGS. 5A-C may be similar to aforementioned methods and thus are not detailed below.

[0044] First pixel electrode 325 may include a “crisscross” structure. Second slit 329 of second pixel electrode 327 may also include a crisscross structure corresponding to first pixel electrode 325. TFT array substrate 320 may thus induce a multi-domain electric field between first pixel electrode 325 and second pixel electrode 327.

[0045] In one embodiment of the invention, first pixel electrode of the present invention may include, for example, V-shape or crisscross forms. However, other embodiments are not so limited.

[0046] FIGS. 6A-D are schematic diagrams for manufacturing a TFT array substrate according to an embodiment of the invention. Some reference numerals addressed above may be the same as used in above figures. Construction for electrodes and pixel region of FIGS. 6A-D may be similar to aforementioned methods and thus are not detailed below.

[0047] When forming insulating layer 426a of TFT array substrate 420, first contact holes 206a and 206b may not be formed. In other words, after forming first pixel electrode 225, electrode insulating layer 426 may be formed on (i.e., over) insulating layer 426a and first pixel electrode 225. First contact holes 406a and 406b and second contact holes 407a and 407b may be formed in insulating layer 426a. First contact holes 406a and 406b may respectively expose portions of first pixel electrode 225, first drain electrode 202c, and portions of first auxiliary storage metallic layer 224b. Second contact hole 407a and 407b may respectively expose portions of second drain electrode 203c and second auxiliary storage metallic layer 224c. In FIG. 6D, second pixel electrode 427 may be formed on electrode insulating layer 426. Portions of second pixel electrodes 427 may cover second contact holes 407a and 407b to electrically connect to second drain electrode 203c of second TFTs 203 and second auxiliary storage metallic layer 224c of the second storage capacitor. Each second pixel electrode 427 may include, for example, two electrical connecting portions 427a and 427b which may respectively cover first contact holes 406a and 406b but may not connect to other portions of second pixel electrodes 427. For example, electrical connecting portions 427a and 427b may be isolated from other portions of second pixel electrodes 427. Since electrical connecting portions 427a and 427b may at least cover the inner sidewall, first pixel electrode 225 may electrically connect to first drain electrode 202c and first auxiliary storage metallic layers 224b respectively using electrical connecting portions 427a and 427b. First pixel electrode 225 and second pixel electrode 427 of TFT array substrate 420 may partially overlap to form a multi-domain electric field to prevent or lessen a position error between the TFT array and CF substrates, and thus achieve a wide viewing angle and low color shift. Further, first contact holes 406a and 406b and second contact holes 407a and 407b may be formed after forming electrode insulating layer 426 to simplify the manufacturing process of the TFT array substrate.

[0048] FIGS. 7A-C are schematic diagrams for manufacturing a TFT array substrate according to an embodiment of the invention. Some reference numerals addressed above may be the same as used in above figures. Construction for electrodes and pixel region of FIGS. 7A-C may be similar to aforementioned methods and thus are not detailed below.

[0049] After forming first TFT 202, second TFT 203, first and second storage capacitors, insulating layer 226a is not formed. Instead, in one embodiment of the invention, first pixel electrode 525 may be formed on substrate 221 and portions of first pixel electrodes 525 may cover first drain

electrode 202c of first TFT 202 and the first auxiliary storage metallic layers 224b of the first storage capacitors. First pixel electrode may electrically connect to first TFT 202 and the first storage capacitors. First pixel electrode 525 may directly contact gate insulating layer 222c. Electrode insulating layer 526 may be formed on first TFT 202, second TFT 203, the first storage capacitors, the second storage capacitors, and first pixel electrodes 525. Electrode insulating layer 526 may include second contact holes 507a and 507b, which may respectively expose portions of second drain electrode 203c and second auxiliary storage metallic layers 224c. Second pixel electrode 527 may be formed on electrode insulating layer 526 and may cover second contact holes 507a and 507b. Second pixel electrode 527 may electrically connect to second drain electrode 203c of second TFT 203 and second auxiliary storage metallic layers 224c of the second storage capacitors. First pixel electrode 525 and second pixel electrode 527 of TFT array substrate 520 may partially overlap to induce a multi-domain electric field to prevent or lessen occurrences of position error between the TFT array and CF substrates and achieve a wider viewing angle and lower color shift sometimes associated with conventional methods and devices. Further, to simplify the manufacturing process of the TFT array substrate, insulating layer 226a need not be formed between first pixel electrode 525 and second pixel electrode 527.

[0050] Thus, various embodiments of the TFT array substrate, manufacturing method, and applications thereof may induce multi-domain electric field to broaden viewing angles and prevent or lessen occurrences of the position error between the TFT array and CF substrates to enhance display quality. Furthermore, the TFT array substrate of the present invention may reduce any color shift problem.

[0051] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A liquid crystal (LC) display device comprising: a substrate, an electrode insulating layer, and an LC layer; a first plurality of pixel electrodes, including a first pixel electrode, formed between the substrate and the electrode insulating layer; a second plurality of pixel electrodes, including a second pixel electrode, formed between the LC layer and the electrode insulating layer; and a pixel region including the first and second pixel electrodes, the second pixel electrode including first and second enclosed slits wherein the first slit does not overlap the first pixel electrode and the second slit overlaps the first pixel electrode.
2. The device of claim 1, wherein the substrate includes data lines and gate lines that overlap to form a plurality of pixel regions including the pixel region, each pixel region including a first thin film transistor (TFT) to electrically connect to a first gate line included in the gate lines and a first data line included in the of data lines.
3. The device of claim 2, wherein the gate lines and the data lines include a first material different from a second material included in the first pixel electrodes and the second pixel electrodes.

4. The device of claim 2, wherein the pixel region includes one of the first TFTs and a second TFT, the first pixel electrode to electrically connect to the one of the TFTs and the second pixel electrode to electrically connect to the second TFT.

5. The device of claim 2, wherein first pixel electrode directly contacts a gate insulating layer formed on one of the first TFTs.

6. The device of claim 2, wherein the first pixel electrode includes a total area generally between $\frac{1}{3}$ and $\frac{1}{2}$ of a total area of the pixel region.

7. The device of claim 1, wherein the pixel region further includes a storage capacitor electrode non-overlapping the first slit.

8. The device of claim 1, wherein the pixel region further includes a storage capacitor electrode overlapping the second slit.

9. The device of claim 1, wherein the first pixel electrode is formed in a "V" shape.

10. The device of claim 1, further comprising an insulating layer between the substrate and the first plurality of pixel electrodes.

11. The device of claim 1, wherein the first pixel electrode is to electrically connect to a first voltage level, the second pixel electrode is to electrically connect to a second voltage level, and the first voltage level is to be greater than the second voltage level.

12. A method for manufacturing a liquid crystal device comprising:

forming a plurality of first thin film transistors (TFTs) and a plurality of second TFTs on a substrate;

forming a plurality of first pixel electrodes on the substrate, each of the first pixel electrodes respectively to electrically connect to one of the first TFTs;

forming an electrode insulating layer on the first pixel electrodes; and

forming a plurality of transparent second pixel electrodes on the electrode insulating layer, each of the second pixel electrodes respectively to electrically connect to one of the second TFT;

wherein each of the second pixel electrodes includes at least one first slit that does not overlap with each of the first pixel electrodes and at least one second slit that overlaps with one of the first pixel electrodes.

13. The method of claim 12, further comprising:

forming a plurality of gate lines on the substrate, wherein the gate lines include a plurality of first gate electrodes and a plurality of second gate electrodes;

forming a gate insulating layer directly on the first gate electrodes and the second gate electrodes;

forming a plurality of first semiconductor islands and a plurality of second semiconductor islands on the gate insulating layer, wherein the first semiconductor islands are respectively disposed on the first gate electrodes and the second semiconductor islands are respectively disposed on the second gate electrodes;

forming a plurality of first ohmic contact layers respectively on the first semiconductor islands and forming a plurality of second ohmic contact layers respectively on the second semiconductor islands;

forming a plurality of first data lines, a plurality of second data lines, a plurality of first drain electrodes, and a plurality of second drain electrodes, wherein a plurality of first source electrodes included in the first data lines

and the first drain electrodes are respectively disposed on the first ohmic contact layers, and a plurality of second source electrodes included in the second data lines and the second drain electrodes are respectively disposed on the second ohmic contact layers; and

removing portions of the first semiconductor islands and portions of the first ohmic contact layers between the first source electrodes and the first drain electrodes to expose the gate insulating layer, and removing portions of the second semiconductor islands and portions of the second ohmic contact layers between the second source electrodes and the second drain electrodes to expose the gate insulating layer.

14. The method as claimed in claim 12, further comprising: forming a plurality of storage capacitor lines on the substrate, wherein each of the storage capacitor lines includes a plurality of storage electrodes;

forming a gate insulating layer on the storage capacitor lines; and

forming a plurality of first auxiliary storage metallic layers and a plurality of second auxiliary storage metallic layers on the gate insulating layer, wherein the first auxiliary storage metallic layers and the second auxiliary storage metallic layers overlap the storage electrodes.

15. The method as claimed in claim 12, further comprising: forming an insulating layer on the first TFTs and the second TFTs, wherein the insulating layer includes a plurality of first contact holes respectively exposing the first drain electrodes of the first thin film transistors, and the electrode insulating layer includes a plurality of second contact holes respectively exposing the second drain electrodes of the second thin film transistors to allow the second pixel electrodes to be formed on the electrode insulating layer and cover the second contact holes.

16. The method as claimed in claim 12, further comprising the steps of:

forming an insulating layer on the first TFTs and the second TFTs, wherein the electrode insulating layer includes a plurality of first contact holes respectively exposing a plurality of first drain electrodes of the first thin film transistors and a plurality of second contact holes respectively exposing a plurality of second drain electrodes of the second thin film transistors, and the second pixel electrodes further respectively include a plurality of electrical connecting portions which respectively cover the first contact holes and are isolated from other portions of the second pixel electrodes.

17. A liquid crystal display panel, comprising:

a color filter (CF) substrate;

a thin film transistor (TFT) array substrate, coupled to the CF substrate, including:

a plurality of first pixel electrodes and a plurality of second pixel electrodes;

an electrode insulating layer between the plurality of first pixel electrodes and the plurality of second pixel electrodes, each of the second pixel electrodes including at least one first enclosed slit non-overlapped with each of the first pixel electrodes and at least one second enclosed slit overlapping one of the first pixel electrodes; and

a liquid crystal layer between the CF substrate and the TFT array substrate;

wherein the first and second slit each include a contiguous perimeter defined by the second pixel electrode.

18. The panel of claim **17**, wherein each of the first slits is non-overlapped with each storage capacitor electrode included in the TFT array substrate.

19. A liquid crystal (LC) display device comprising:
a substrate, an electrode insulating layer, and an LC layer;
a plurality of first transparent pixel electrodes between the substrate and the electrode insulating layer; and
a plurality of second transparent pixel electrodes between the electrode insulating layer and the LC layer;
wherein each of the second pixel electrodes includes at least one slit respectively overlapping one of the first pixel electrodes.

20. The device of claim **19**, wherein each of the first pixel electrodes is to electrically connect respectively to one of a plurality of first thin film transistors (TFTs) and each of the second pixel electrodes is to electrically connect respectively to one of a plurality of second TFTs.

21. The device of claim **19**, further comprising a plurality of data lines between the substrate and the LC layer; wherein the resistance of a material included in the data lines is lower than the resistance of a material included in the first pixel electrodes.

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专利名称(译)	用于液晶显示装置的薄膜晶体管阵列及相关的制造和操作方法		
公开(公告)号	US20090310076A1	公开(公告)日	2009-12-17
申请号	US12/482589	申请日	2009-06-11
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IPC分类号	G02F1/1343 H01L29/04 H01L21/00		
CPC分类号	G02F1/133707 G02F2001/134345 G02F2001/133354 G02F1/134309		
优先权	097121726 2008-06-11 TW		
其他公开文献	US8358393		
外部链接	Espacenet USPTO		

摘要(译)

在涉及液晶显示装置的发明的一个实施例中，薄膜晶体管（TFT）阵列基板的第一像素电极可以与TFT阵列基板的第二像素电极的狭缝重叠，但不与第二像素电极的另一个狭缝重叠。。这可以帮助诱导多畴电场而不必精确地定位滤色器基板的公共电极和TFT阵列基板。这可以防止位置误差，提高显示质量，产生更宽的视角，以及有时与传统液晶显示装置和方法相关的较低色移。

