



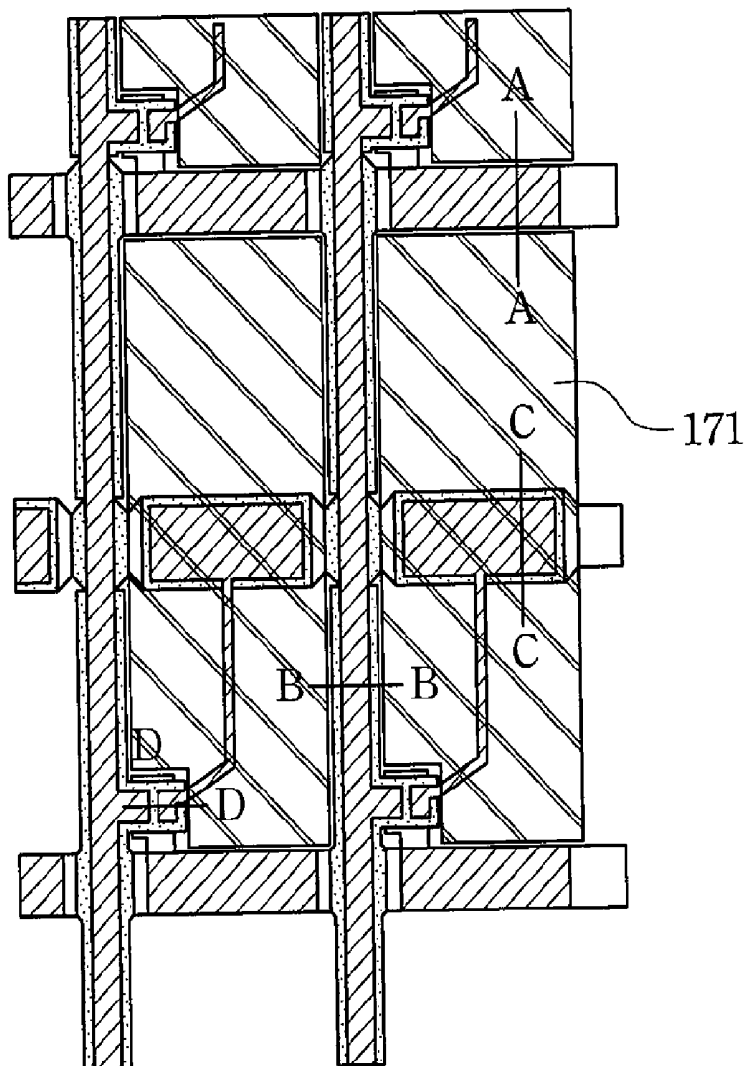
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(19) **United States**(12) **Patent Application Publication**
Wang et al.(10) **Pub. No.: US 2007/0258035 A1**(43) **Pub. Date: Nov. 8, 2007**(54) **LIQUID CRYSTAL DISPLAY ARRAY
SUBSTRATE AND ITS MANUFACTURING
METHOD**(30) **Foreign Application Priority Data**

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ATLANTA, GA 30339-5948(57) **ABSTRACT**

A liquid crystal display (LCD) array substrate and its manufacturing method are provided. Scan lines and data lines of the LCD array substrate are composed of two conductive layers to decrease their RC delay. Moreover, the dielectric layer and even the planarization layer are removed from pixel areas defined by the scan lines and the data lines to increase the light penetration percentage.

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Hsin-Chu (TW)(21) Appl. No.: **11/566,724**(22) Filed: **Dec. 5, 2006**

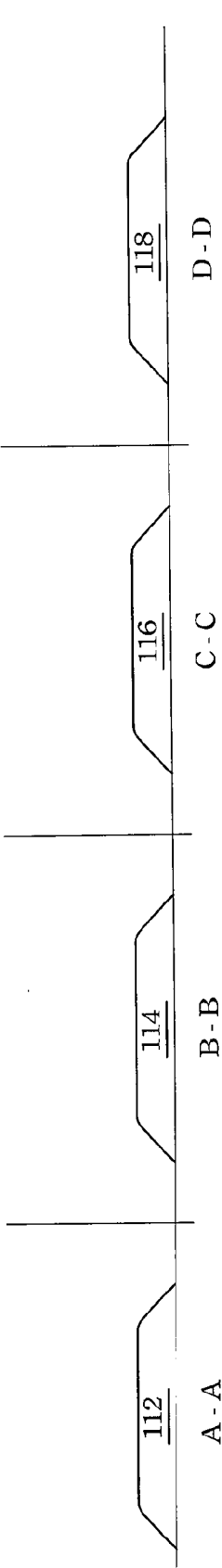


Fig. 1A

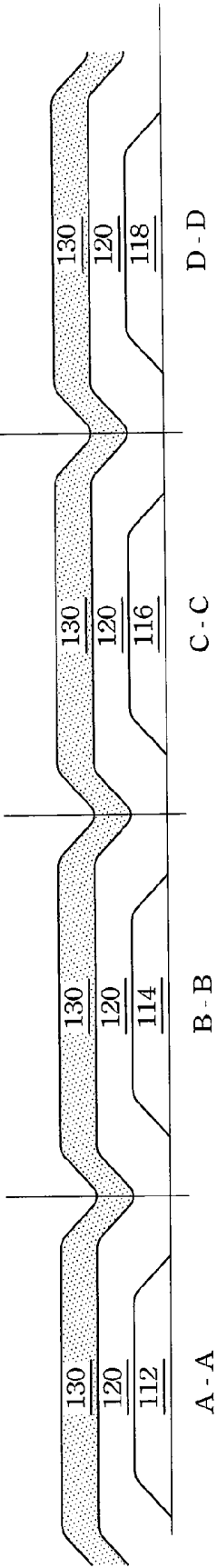


Fig. 1B

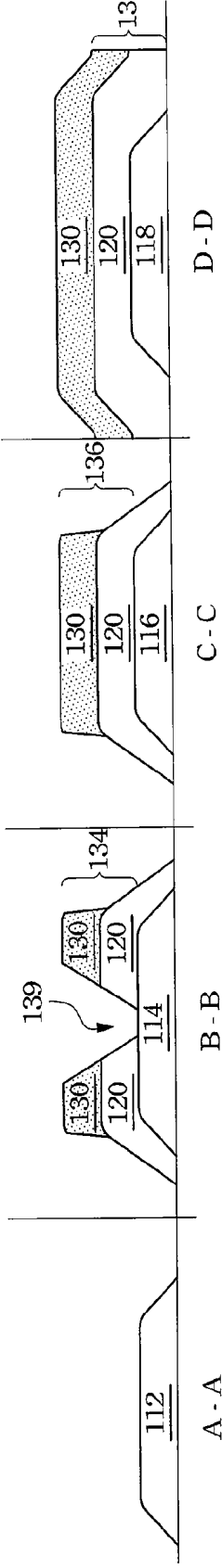


Fig. 1C

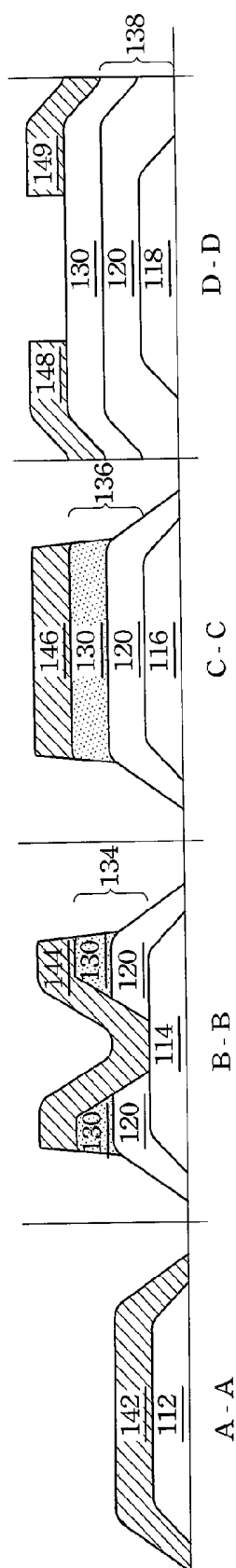


Fig. 1D

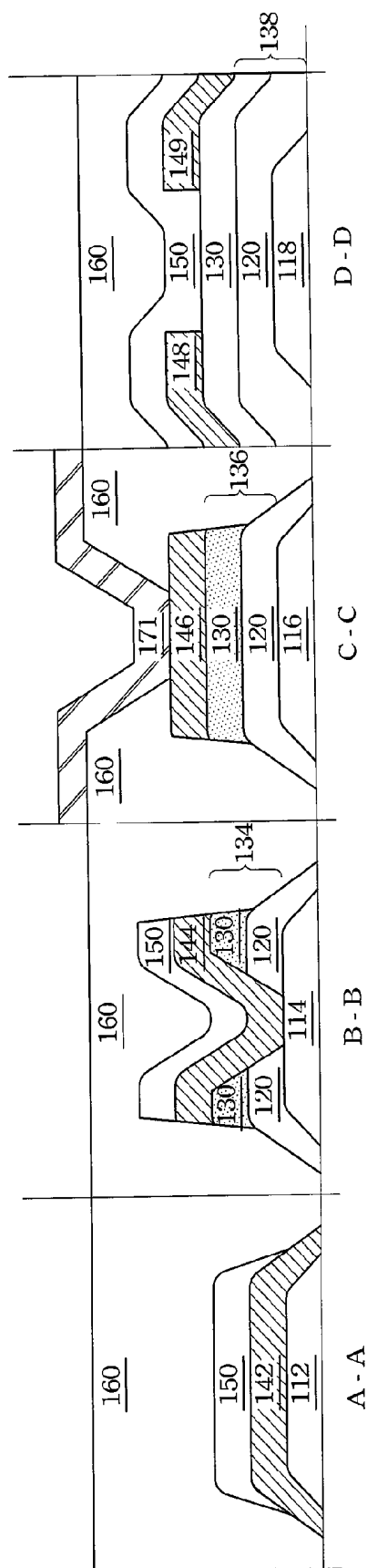


Fig. 1E

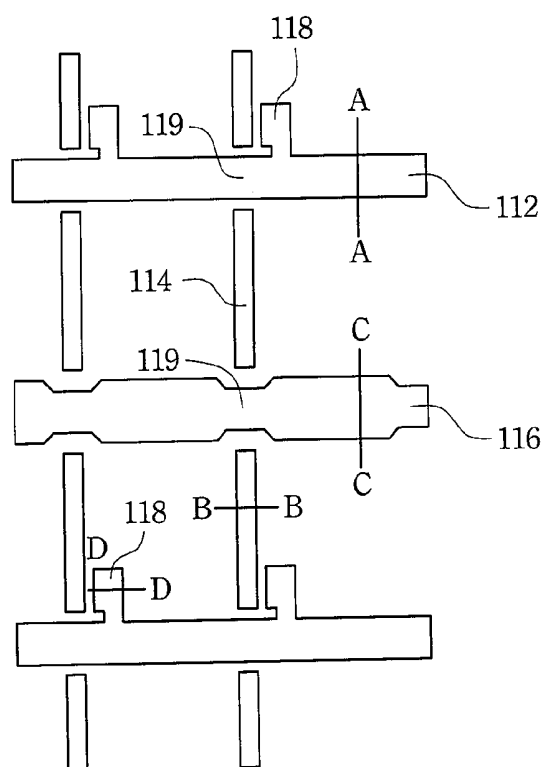


Fig. 2A

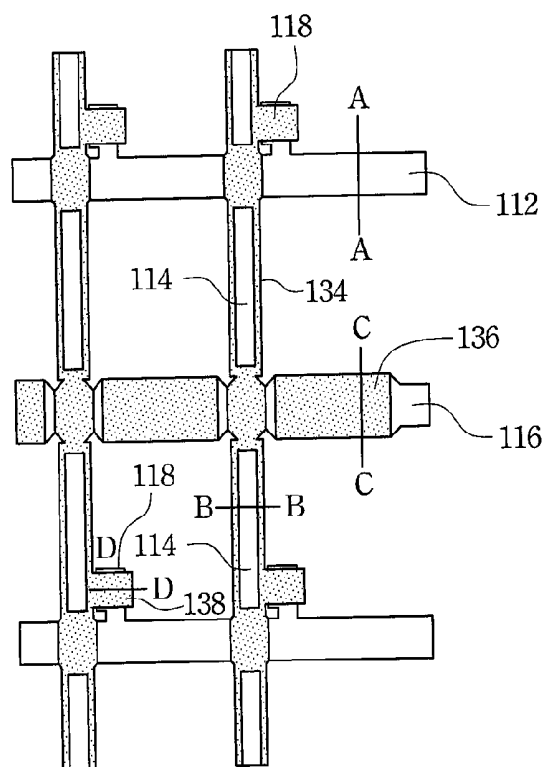


Fig. 2B

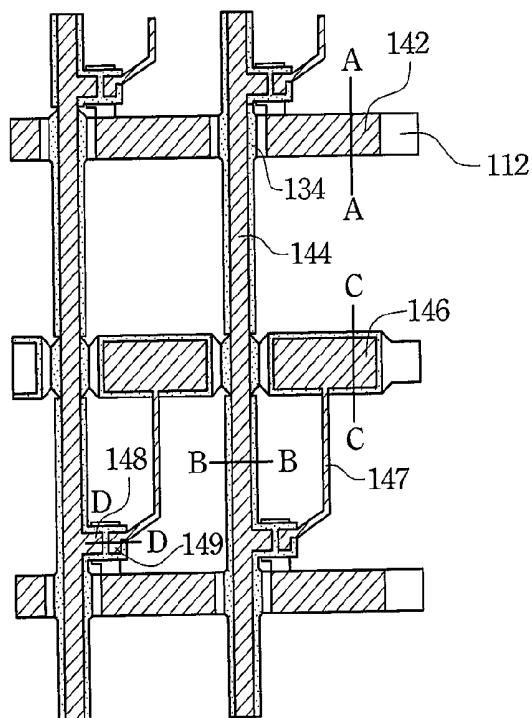


Fig. 2C

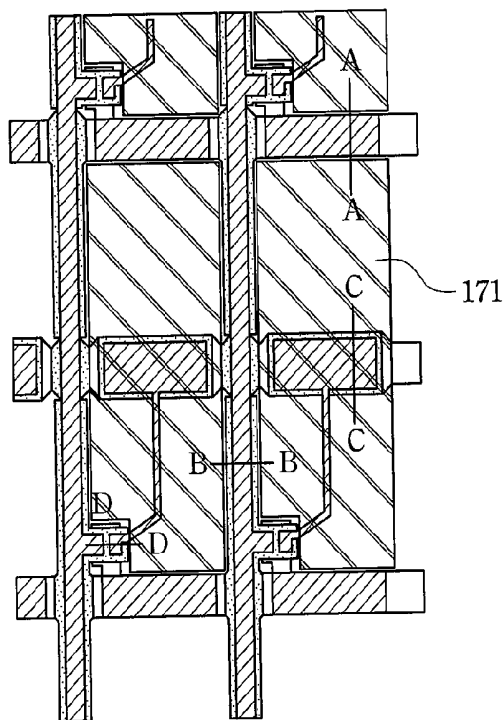


Fig. 2D

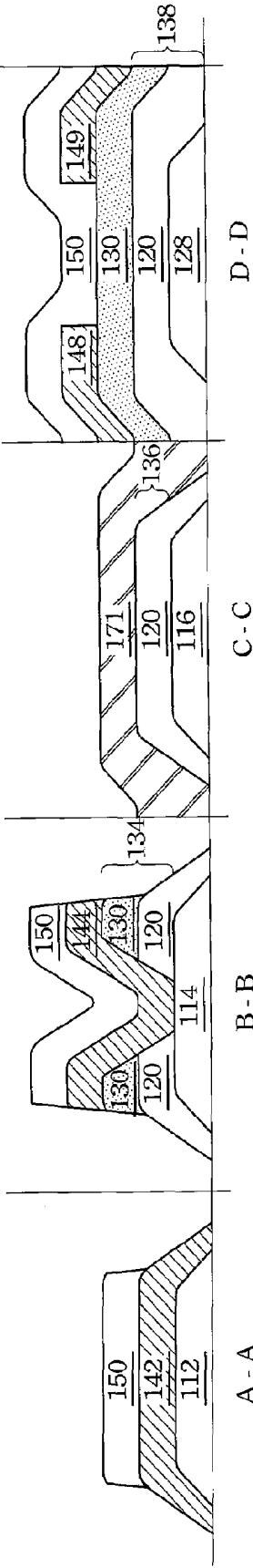


Fig. 3A

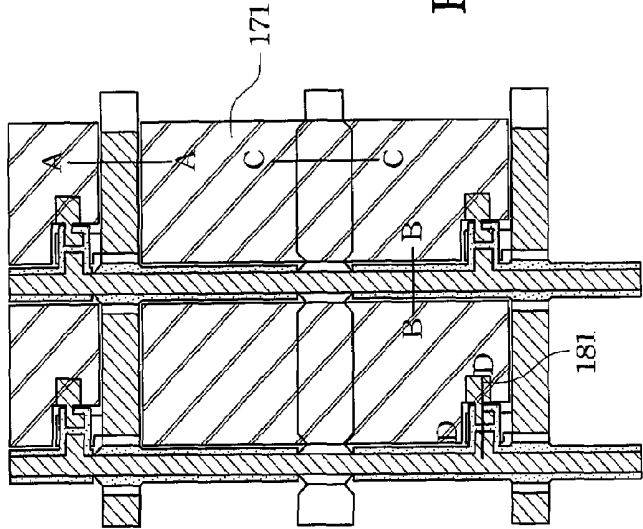


Fig. 3B

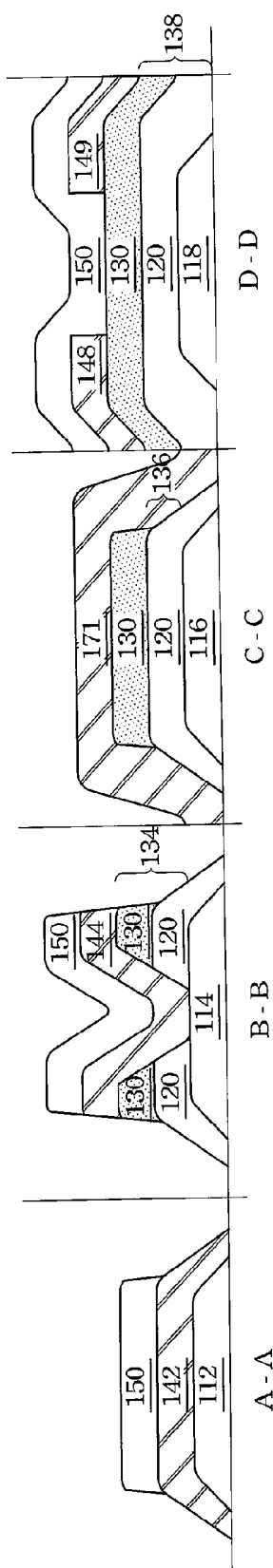


Fig. 4A

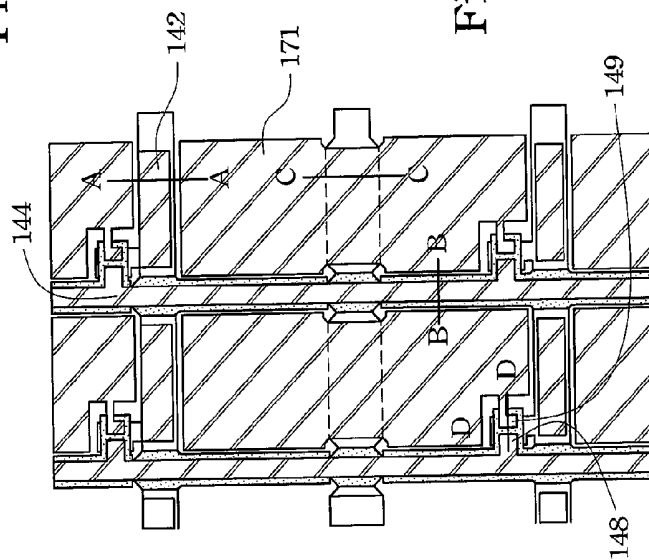


Fig. 4B

LIQUID CRYSTAL DISPLAY ARRAY SUBSTRATE AND ITS MANUFACTURING METHOD

RELATED APPLICATIONS

[0001] The present application is based on, and claims priority from, Taiwan Application Serial Number 95115636, filed May 2, 2006, the disclosure of which is hereby incorporated by reference herein in its entirety.

BACKGROUND

[0002] 1. Field of Invention

[0003] The present invention relates to a liquid crystal display (LCD). More particularly, the present invention relates to an LCD array substrate and its manufacturing method.

[0004] 2. Description of Related Art

[0005] With progress in LCD technology and an increased demand for large-scale displays, both the size and resolution of LCD screens are continually increasing. An increase in both the resistance and the capacitance of the conductive lines of the LCD is required to increase the LCD resolution. Increased the resistance and the capacitance of the conductive lines worsen the resistance-capacitance time delay (RC delay) problem in LCD. The RC delay problem affects both signal transfer in the LCDs and the LCD display quality.

[0006] Traditionally methods to reduce RC delay mainly include using a copper process and broadening the width of the conductive lines. The resistance of the conductive line can be reduced to improve the signal transfer rate by introducing the copper process of manufacturing copper conductive line to the LCD manufacturing processes. Therefore, the RC delay is also reduced. However, the copper process has many problems need to be solved. Another method to solve the RC delay problem is to broaden the width of the conductive lines. The cross-sectional area of the conductive lines is increased by broadening the width of the conductive lines. Therefore, the resistance of the conductive lines is decreased, and the RC delay is reduced. However, the size of the pixel areas is influenced by broadening the conductive line width, and thus the aperture ratio and the brightness of the LCDs.

[0007] Each LCD pixel area is composed of many different functional thin layers. Each thin layer has a different reflective index. The reflective index for each thin layer is different from the reflective indices for the other thin layers. Because different thin layers have different reflective indices, when light passes through interfaces of the different thin layers, a portion of the light is easily reflected, and the transmittance of the light is decreased. Therefore, the brightness of the LCDs is decreased. The LCDs need to use high brightness backlight modules to generate the required display brightness.

SUMMARY

[0008] It is therefore an aspect of the present invention to provide a LCD array substrate, which can reduce the RC delay of conductive lines and won't affect the aperture ratio of the LCD.

[0009] It is another aspect of the present invention to provide a manufacturing method of a LCD array substrate.

The amount of light passing through the pixel areas and the brightness of the LCD can be increased by using this method.

[0010] In accordance with the foregoing and other aspects of the present invention, a LCD array substrate is provided. The array substrate of the LCD comprises a first conductive line, two second conductive lines, a signal dielectric layer, two third conductive lines, a fourth conductive line, a transistor and a pixel electrode. The first conductive line is on a substrate and has a crossing region. The two second conductive lines are on the substrate. The two second conductive lines are separately located at two sides of the crossing region and are perpendicular to the first conductive line. The signal dielectric layer is on the second conductive lines and in the crossing region, wherein the signal dielectric layer on the second conductive lines has a first opening to expose the second conductive lines. The two third conductive lines cover the first conductive line at the two sides of the crossing region to form a scan line. The fourth conductive line covers the signal dielectric layer and the first opening to form a data line. The third conductive lines don't electrically connect with the fourth conductive line. A source electrode of the transistor electrically connects with the fourth conductive line. A gate electrode of the transistor electrically connects with the first conductive line. The pixel electrode electrically connects with a drain electrode of the transistor.

[0011] In accordance with the foregoing and other aspects of the present invention, a manufacturing method of a LCD array substrate is provided. Firstly, a patterned first metal layer is formed on a substrate to form a first conductive line, two second conductive lines and a gate electrode. The first conductive line has a crossing region and electrically connects with the gate electrode. The second conductive lines are located separately at two sides of the crossing region of the first conductive line. Secondly, a dielectric layer and a semiconducting layer are sequentially formed and patterned to cover the second conductive lines, the crossing region and the gate electrode. The dielectric layer and the semiconducting layer on the second conductive lines have a first opening to expose the second conductive lines. The semiconducting layer above the gate electrode is used as a channel layer. Thirdly, a patterned second metal layer is formed over the substrate to separately form two third conductive lines, a fourth conductive line, a source electrode and a drain electrode. The third conductive lines cover the two sides of the crossing region of the first conductive line to form a scan line. The fourth conductive line covers the semiconducting layer on the second conductive lines and the cross region to form a data line. The source electrode and the drain electrode located at two sides of the channel layer form a transistor. The third conductive lines don't connect with the fourth conductive line. Fourthly, a patterned passivation layer is formed to cover the transistor, the scan line and the data line. Finally, a pixel electrode is formed over the substrate. The pixel electrode electrically connects with the transistor.

[0012] In the structure of the LCD array substrate of the invention, the thickness of both scan lines and data lines is increased, so the cross-sectional area of the scan lines and the data lines is increased. Therefore, the resistance of the conductive lines is decreased, and the RC delay problem to pixel display quality is solved. Moreover, the occupied area

of both the scan lines and the data lines on the substrate is still the same and won't affect the size of the pixel areas on the substrate.

[0013] In the structure of the LCD array substrate of the invention, the dielectric layer is only on the conductive lines. There is no dielectric layer on the pixel areas. Therefore, the number of layers light needs to pass through is decreased, and the transparency of the pixel area is increased. The brightness of the LCDs thus is increased.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0015] FIGS. 1A-1E are cross-sectional views of the LCD array substrate in process steps according to one preferred embodiment of this invention;

[0016] FIGS. 2A-2D are top views of the LCD array substrate in process steps according to one preferred embodiment of this invention;

[0017] FIG. 3A is a cross-sectional view of the LCD array substrate in process steps according to another preferred embodiment of this invention;

[0018] FIG. 3B is a top view of the LCD array substrate in process steps according to another preferred embodiment of this invention;

[0019] FIG. 4A is a cross-sectional view of the LCD array substrate in process steps according to still another preferred embodiment of this invention; and

[0020] FIG. 4B is a top view of the LCD array substrate in process steps according to still another preferred embodiment of this invention;

DETAILED DESCRIPTION

Embodiment 1

[0021] Please refer to FIG. 1A and FIG. 2A simultaneously. FIG. 1A comprises the A-A cross-sectional view of a scan line, B-B cross-sectional view of a data line, C-C cross-sectional view of a capacitance line and D-D cross-sectional view of a gate electrode in FIG. 2A. At first, a first metal layer is formed on a transparent substrate (not shown in FIG. 1A and FIG. 2A). The first metal layer is defined to form first scan lines 112, first data lines 114, capacitance lines 116 and gate electrodes 118. In FIG. 2A, the first scan lines 112 are parallel to the capacitance lines 116. Both the first scan lines 112 and the capacitance lines 116 have crossing regions 119 respectively. The first data lines 114 are perpendicular to both the first scan lines 112 and the capacitance lines 116. The first data lines 114 are located separately at two sides of the crossing regions 119 of both the first scan lines 112 and the capacitance lines 116. The first data lines 114 don't connect with the crossing regions 119. The first scan lines 112 and the first data lines 114 on the substrate define the pixel areas.

[0022] Please refer to FIG. 1B. A dielectric layer 120 and a semiconducting layer 130 are sequentially formed over the substrate to cover the first scan lines 112, the first data lines 114, the capacitance lines 116 and the gate electrodes 118. In a preferred embodiment, the semiconducting layer 130 com-

prises an amorphous silicon layer and an n-type doped amorphous silicon layer thereon.

[0023] Please refer to FIG. 1C and FIG. 2B simultaneously. FIG. 2B is the top view of FIG. 1C. In FIG. 1C and FIG. 2B, the dielectric layer 120 and the semiconducting layer 130 are defined to form signal dielectric layers 134, capacitance dielectric layers 136 and channel layers 138. The signal dielectric layers 134 are located on the first data lines 114 and in the crossing regions 119. The capacitance dielectric layers 136 are located on the capacitance lines 116. The channel layers 138 are located above the gate electrodes 118. Each of the signal dielectric layer 134 on the first data lines 114 has an opening 139 to expose the first data lines 114. The signal dielectric layers 134 don't connect with the capacitance dielectric layers 136. Because the dielectric layer and the semiconducting layer on the pixel areas defined by the first scan lines 112 and the first data lines 114 are removed totally, the number of thin film layers that light needs to pass through is decreased and thus the transparency of the pixel areas is increased.

[0024] Please refer to FIG. 1D and FIG. 2C simultaneously. FIG. 2C is the top view of FIG. 1D. After defining the semiconducting layer and the dielectric layer, a second metal layer is formed thereon. Then, the second metal layer is defined to form second scan lines 142, second data lines 144, upper electrodes 146, source electrodes 148, drain electrodes 149 and connecting lines 147. The second scan lines 142 cover the exposed first scan lines 112 at two sides of the crossing region 119. The second data lines 144 cover the signal dielectric layers 134 and the openings 139. The upper electrodes 146 are located on the capacitance dielectric layers 136 at two sides of the crossing region 119. The source electrodes 148 and the drain electrodes 149 are located at two sides of the channel layer 138. The connecting lines 147 are used to connect the upper electrodes 146 and the drain electrodes 149.

[0025] The second scan lines 142 and the first scan lines 112 connect directly to form scan lines, which have double-layer metal structure. The second data lines 144 and the first data lines 114 connect directly through the openings 139 to form data lines, which also have double-layer metal structure. The signal dielectric layers 134 in the crossing regions 119 are used to electrically insulate the second data lines 144 from the both the first scan lines 112 and the capacitance lines 116. The gate electrodes 118, the source electrodes 148 and the drain electrodes 149 form the three electrodes of the transistors. The capacitance lines 116, the capacitance dielectric layers 136 and the upper electrodes 146 form storage capacitances.

[0026] Please refer to FIG. 1E and FIG. 2D simultaneously. FIG. 2D is the top view of FIG. 1E. In FIG. 1E and FIG. 2D, a passivation layer 150 is formed and defined to cover the second scan lines 142, the second data lines 144, the source electrodes 148 and the drain electrodes 149 to protect them from oxidizing, while the passivation layer 150 on the pixel regions and upper electrodes 146 is removed simultaneously.

[0027] Then, a planarization layer 160 is formed over the substrate and defined to expose the upper electrodes 146.

[0028] Finally, the transparent conducting layer is formed and defined to form the pixel electrodes 171, which connect with the upper electrodes 146, on the pixel areas. In this embodiment, the pixel electrodes 171 connect with the drain electrodes 149 through the upper electrodes 146 and con-

necting lines 147. Each of the pixel electrodes 171 is independent and doesn't connect with other pixel electrodes. In the LCD array substrate of the invention, both scan lines and data lines are composed of two metal layers. The scan lines are composed of the first scan lines and the second scan lines. The data lines are composed of the first data lines and the second data lines. The thicknesses of the scan lines and the data lines are increased, so the cross-sectional areas thereof are also increased. Therefore, the resistance of the scan lines and data lines is decreased and the RC delay problem to pixel display quality is solved. Moreover, because the occupied area of the scan lines and data lines is still the same, the aperture ratio of the LCDs won't be affected.

[0029] Conventionally, light has to pass the substrate, the dielectric layer, the planarization layer and the transparent conducting layer to pass through the pixel areas. However, the reflective index of each layer is different from each other, and a portion of the light is lost because reflection or refraction will be incurred when the light passes through interfaces of different thin layers. In the embodiment, the dielectric layer, which has the highest reflective index among the thin layers constructing the pixel area, is removed from the pixel areas, so the difference between the reflective indexes among the thin layers is decreased. The number of layers that the light needs to pass is reduced from five to three, and the number of interfaces that the light needs to pass through is reduced from four to two. The likelihood of the light reflected at the interfaces is reduced, and the light loss is decreased when the light passes through the pixel areas. Therefore, the brightness of the final LCD product of the invention is thus improved.

Embodiment 2

[0030] In embodiment 2, the planarization layer of the embodiment 1 is omitted, so there are some corresponding adjustments on some structures of the LCD array substrate. With the exception of no upper electrodes forming on the capacitance dielectric layer when the second metal layer is defined, all processes from the formation of the first metal layer to the formation of the passivation layer in the embodiment 2 are the same as those in the embodiment 1.

[0031] Please refer to FIG. 3A and FIG. 3B simultaneously. FIG. 3B is the top view of FIG. 3A. After the passivation layer 150 is formed over the substrate, the passivation layer 150 is defined to cover the second scan lines 142, the second data lines 144, the source electrode 148 and the drain electrodes 149. Then, the transparent conducting layer is formed and defined to form the pixel electrodes 171. The pixel electrodes 171 connect with the drain electrodes 149 of the transistors through the connecting points 181.

[0032] When the passivation layer 150 is defined, because there are no upper electrodes on the dielectric capacitance layers, the semiconducting layer 130 on the capacitance line 116 can be removed by etching to leave the dielectric layer 120 on the capacitance lines 116. Therefore, the storage capacitances are composed of the capacitance lines 116, the dielectric layers 120 and the pixel electrodes 171 in FIG. 3A. The capacitance lines 116, the dielectric layers 120 and the pixel electrodes 171 are the lower electrodes, the capacitance dielectric layers and the upper electrodes of the storage capacitances, respectively. In the embodiment 1, the capacitance dielectric layer of the storage capacitance is composed

of the dielectric layer and the semiconducting layer. In the embodiment 2, the capacitance dielectric layer of the storage capacitance is only composed of the dielectric layer. The capacitance dielectric layer of the storage capacitance of the embodiment 2 is thinner than that of the embodiment 1. Therefore, the storage capacitance of the embodiment 2 can store more electricity than the storage capacitance of the embodiment 1.

[0033] Because the planarization layer is omitted in the embodiment 2, the light only needs to pass through the substrate and the transparent conducting layer to pass through the pixel areas. Both the number of thin layers and the number of interfaces the light needs to pass through are decreased. The loss of light when the light passes through the interfaces is thus decreased.

Embodiment 3

[0034] Because the transparent conducting layer has the property of the conductor, the transparent conducting layer can be used to replace the second metal layer of embodiment 2. Therefore, not only the planarization but also the second metal layer is omitted in embodiment 3. In this embodiment, the transparent conducting layer can be used not only as the pixel electrodes but also as the conductive lines. Moreover, the number of the required masks in the processes is decreased, so that the cost of the processes is decreased. In embodiment 3, all processes from the formation of the first metal layer to the definition of the semiconducting layer and the dielectric layer are the same as those in embodiment 1.

[0035] Please refer to FIG. 4A and FIG. 4B simultaneously. FIG. 4B is the top view of FIG. 4A. After the transparent conducting layer is formed over the substrate, the transparent conducting layer is defined to form the second scan lines 142, the second data lines 144, the source electrodes 148, the drain electrodes 149 and the pixel electrodes 171. The second scan lines 142 are located on the first scan lines 112. The second data lines 144 are located on the first data lines 114. The source electrodes 148 and the drain electrodes 149 are located at the two sides of the channel layers 138. The pixel electrodes 171 are located on the pixel area. The pixel electrodes 171 on the capacitance dielectric layers 136 can be used as the upper electrodes of the storage capacitances.

[0036] Then, a passivation layer 150 is formed over the substrate and defined to cover the second scan lines 142, the second data lines 144, the source electrodes 148 and the drain electrodes 149 to protect the conductive lines and the transistors from oxidizing.

[0037] Accordingly, the present invention has the following advantages.

[0038] (1) In the LCD array substrate of the invention, the resistance of the conductive lines and the RC delay are reduced, so the display quality of the LCD is improved.

[0039] (2) In the LCD array substrate of the invention, the transparency of the pixel areas is increased, so the brightness of the LCD is increased.

[0040] The preferred embodiments of the present invention described above should not be regarded as limitations to the present invention. It will be apparent to those skilled in the art that various modifications and variations can be made to the present invention without departing from the scope or spirit of the invention. The scope of the present invention is as defined in the appended claims.

What is claimed is:

1. A manufacturing method of a LCD array substrate, comprising:

forming a patterned first metal layer on a substrate to form at least a first conductive line, at least two second conductive lines and at least a gate electrode, wherein the first conductive line has at least a crossing region and electrically connects with the gate electrode, the second conductive lines are located separately at two sides of the crossing region of the first conductive line; sequentially forming and patterning a dielectric layer and a semiconducting layer to cover the second conductive lines, the crossing region and the gate electrode, wherein the dielectric layer and the semiconducting layer on the second conductive lines have a first opening to expose the second conductive lines, the semiconducting layer above the gate electrode is used as a channel layer;

forming a patterned second metal layer over the substrate to separately form at least two third conductive lines, at least a fourth conductive line, at least a source electrode and at least a drain electrode, wherein the third conductive lines cover the first conductive line at two sides of the crossing region to form a scan line, the fourth conductive line covers the semiconducting layer on the second conductive lines and the cross region to form a data line, the source electrode and the drain electrode are located at two sides of the channel layer to form at least a transistor, the third conductive lines don't connect with the fourth conductive line;

forming a patterned passivation layer to cover the transistor, the scan line and the data line; and

forming at least a pixel electrode over the substrate, wherein the pixel electrode electrically connects with the transistor.

2. The method of claim 1, wherein the semiconducting layer comprises an amorphous silicon layer and an n-type doped amorphous silicon layer thereon.

3. The method of claim 1, further comprising:

forming at least a capacitance line parallel to the first conductive line in the step of forming the patterned first metal layer, wherein the capacitance line is at the same side of the first conductive line as the gate electrode and doesn't connect with the second conductive lines;

forming the dielectric layer on the capacitance line to form a capacitance dielectric layer; and

forming the pixel electrode on the capacitance dielectric layer to be an upper electrode.

4. The method of claim 1, further comprising forming a patterned planarization layer over the substrate after forming the patterned passivation layer and before forming the pixel electrode.

5. The method of claim 4, further comprising:

forming at least a capacitance line parallel to the first conductive line in the step of forming the patterned first metal layer, wherein the capacitance line is at the same side of the first conductive line as the gate electrode and doesn't connect with the second conductive lines;

forming the dielectric layer and the semiconducting layer on the capacitance line to form a capacitance dielectric layer; and

forming the patterned second metal layer on the capacitance dielectric layer to be an upper electrode, wherein the planarization layer has a second opening to expose

the upper electrode and the upper electrode electrically connects with the pixel electrode.

6. A manufacturing method of a LCD array substrate, comprising:

forming a patterned first metal layer on a substrate to form at least a first conductive line, at least two second conductive lines and at least a gate electrode, wherein the first conductive line has at least a crossing region and electrically connects with the gate electrode, the second conductive lines are located separately at two sides of the crossing region of the first conductive line; sequentially forming and patterning a dielectric layer and a semiconducting layer to cover the second conductive lines, the crossing region and the gate electrode, wherein the dielectric layer and the semiconducting layer on the second conductive lines have a first opening to expose the second conductive lines, the semiconducting layer above the gate electrode is used as a channel layer;

forming a patterned transparent conducting layer over the substrate to separately form at least two third conductive lines, at least a fourth conductive line, at least a source electrode, at least a drain electrode and at least a pixel electrode, wherein the third conductive lines cover the first conductive line at two sides of the crossing region to form a scan line, the fourth conductive line covers the semiconducting layer on the second conductive lines and the cross region to form a data line, the source electrode and the drain electrode are located at two sides of the channel layer to form at least a transistor, the pixel electrode is located in a pixel area over the substrate, the third conductive lines don't connect with the fourth conductive line; and

forming a patterned passivation layer to cover the transistor, the scan line and the data line.

7. The method of the claim 6, wherein the semiconducting layer comprises an amorphous silicon layer and an n-type doped amorphous silicon layer thereon.

8. The method of claim 6, further comprising:

forming a capacitance line parallel to the first conductive line in the step of forming the patterned first metal layer, wherein the capacitance line is at the same side of the first conductive line as the gate electrode and doesn't connect with the second conductive lines;

forming the dielectric layer on the capacitance line to form a capacitance dielectric layer; and

forming the patterned transparent conducting layer on the capacitance dielectric layer to be an upper electrode, wherein the upper electrode electrically connects with the pixel electrode.

9. A LCD array substrate, comprising:

at least a first conductive line on a substrate, wherein the first conductive line has at least a crossing region;

at least two second conductive lines on the substrate, wherein the second conductive lines are separately located at two sides of the crossing region and perpendicular to the first conductive line;

at least a signal dielectric layer on the second conductive lines and on the crossing region, wherein the signal dielectric layer on the second conductive lines has a first opening to expose the second conductive lines;

at least two third conductive lines covering the first conductive line at the two side of the crossing region to form a scan line;

at least a fourth conductive line covering the signal dielectric layer and the first opening to form a data line, wherein the third conductive lines don't electrically connect with the fourth conductive line;

at least a transistor, wherein a source electrode of the transistor electrically connects with the fourth conductive line, a gate electrode of the transistor electrically connects with the first conductive line; and

at least a pixel electrode, wherein the pixel electrode electrically connects with a drain electrode of the transistor.

10. The substrate of the claim 9, further comprising:

a capacitance line on the substrate and parallel to the first conductive line, wherein the capacitance line is located at the same side of the first conductive line as the gate electrode and doesn't connect with the second conductive lines

a capacitance dielectric layer on the capacitance line; and an upper electrode on the capacitance dielectric layer, wherein the upper electrode electrically connects with a drain electrode of the transistor and the pixel electrode.

11. The substrate of the claim 10, further comprising a patterned planarization layer over the substrate, wherein the planarization layer has a second opening to expose the upper electrode.

12. The substrate of the claim 10, wherein the capacitance dielectric layer comprises a dielectric layer and a semiconducting layer.

13. The substrate of the claim 10, wherein the capacitance dielectric layer comprises a dielectric layer.

14. The substrate of the claim 10, wherein a material of the upper electrode is transparent conducting material.

15. The substrate of the claim 10, wherein a material of the upper electrode is metal.

16. The substrate of the claim 9, wherein a material of the first conductive line and the second conductive lines is metal.

17. The substrate of the claim 9, wherein a material of the third conductive lines, the fourth conductive line, the source electrode and the drain electrode is metal.

18. The substrate of the claim 9, wherein a material of the third conductive lines, the fourth conductive line, the source electrode and the drain electrode is transparent conducting material.

19. The substrate of the claim 9, further comprising a passivation layer on the third conductive lines, the fourth conductive line and the transistor.

* * * * *

专利名称(译)	液晶显示器阵列基板及其制造方法		
公开(公告)号	US20070258035A1	公开(公告)日	2007-11-08
申请号	US11/566724	申请日	2006-12-05
[标]申请(专利权)人(译)	友达光电股份有限公司		
申请(专利权)人(译)	友达光电股份有限公司		
当前申请(专利权)人(译)	友达光电股份有限公司		
[标]发明人	WANG YEONG FENG YU LIANG BIN PAN CHIH JUI		
发明人	WANG, YEONG-FENG YU, LIANG-BIN PAN, CHIH-JUI		
IPC分类号	G02F1/13		
CPC分类号	G02F1/136286 G02F2001/13606 G02F2201/40 G02F2001/136295 G02F2001/13629		
优先权	095115636 2006-05-02 TW		
其他公开文献	US7738072		
外部链接	Espacenet USPTO		

摘要(译)

提供一种液晶显示 (LCD) 阵列基板及其制造方法。 LCD阵列基板的扫描线和数据线由两个导电层组成，以减少它们的RC延迟。此外，从由扫描线和数据线限定的像素区域去除介电层和甚至平坦化层，以增加光穿透百分比。

