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(19) **United States**(12) **Patent Application Publication****Hwang et al.**(10) **Pub. No.: US 2007/0188671 A1**(43) **Pub. Date: Aug. 16, 2007**(54) **ARRAY SUBSTRATE OF LIQUID CRYSTAL
DISPLAY AND FABRICATING METHOD
THEREOF**(30) **Foreign Application Priority Data**

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Kim**, Seoul (KR)**Publication Classification**(51) **Int. Cl.**
G02F 1/136 (2006.01)(52) **U.S. Cl.** **349/43**

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FALLS CHURCH, VA 22040-0747 (US)**(57) **ABSTRACT**

An array substrate of a liquid crystal device has a plurality of gate lines, data lines, pixel areas, and thin film transistors, wherein the gate lines are formed from a material of a first and second metal layer, and wherein the first metal layer of the gate line is extended on the pixel area. Also, a display device has first and second gate lines and a data line on a substrate, a thin film transistor, a pixel electrode, a first storage electrodes extending from the second gate line and wherein at least one of the first and second gate lines and the data line includes first and second line layers respectively formed of an oxidized metal later and a metal layer.

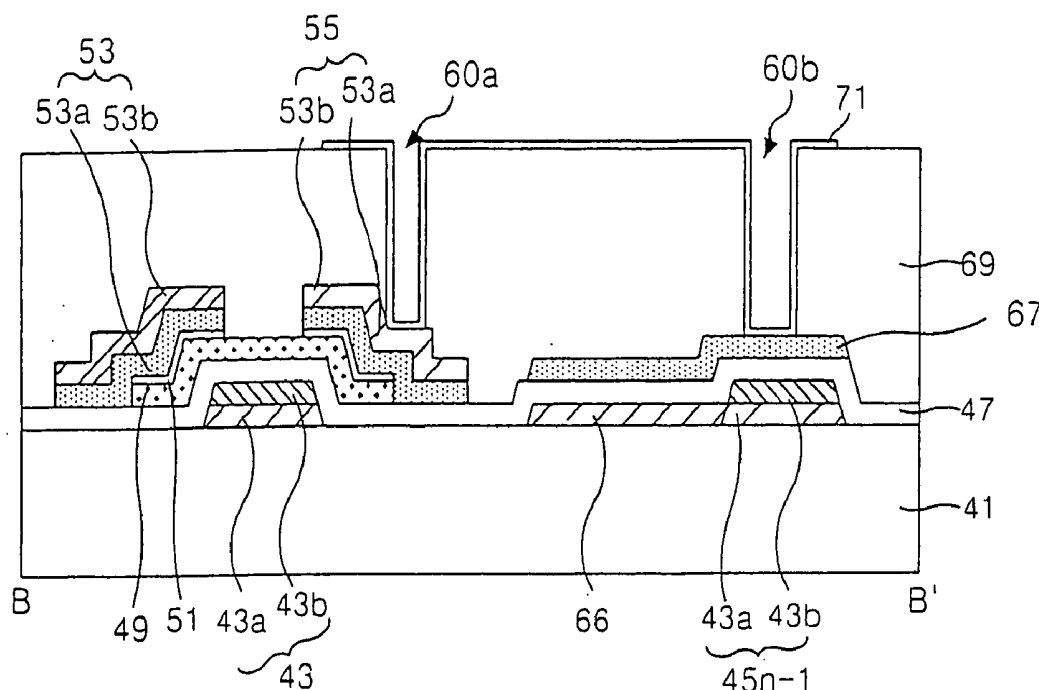
(21) Appl. No.: **11/785,200**(22) Filed: **Apr. 16, 2007****Related U.S. Application Data**(63) Continuation of application No. 10/183,683, filed on
Jun. 28, 2002.

FIG. 1
CONVENTIONAL ART

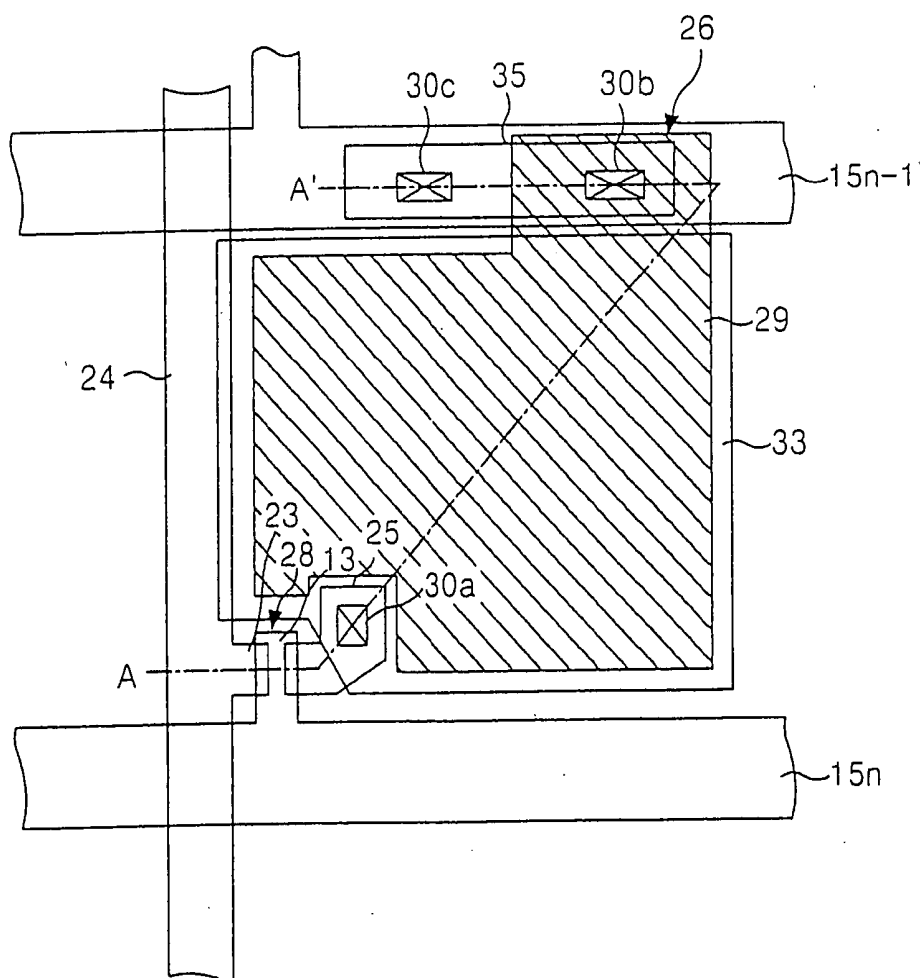


FIG. 3
CONVENTIONAL ART

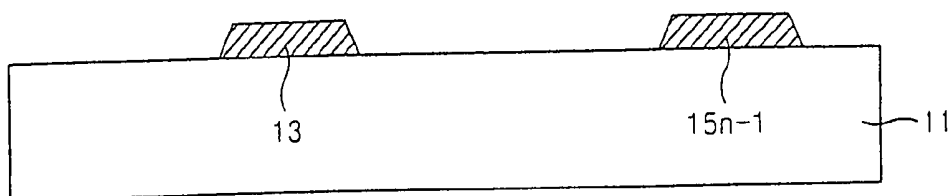


FIG. 4
CONVENTIONAL ART

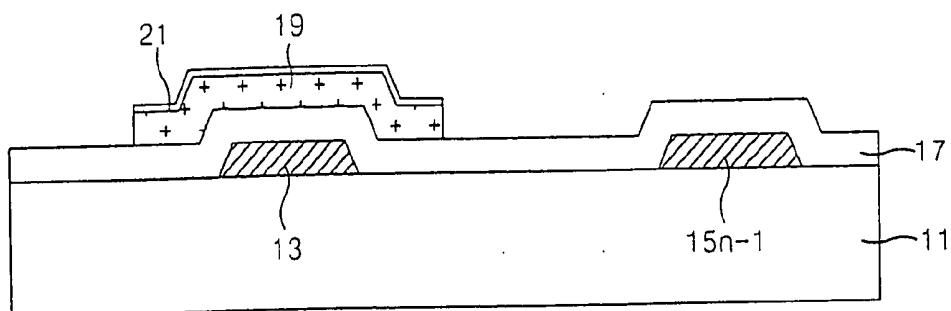


FIG. 5
CONVENTIONAL ART

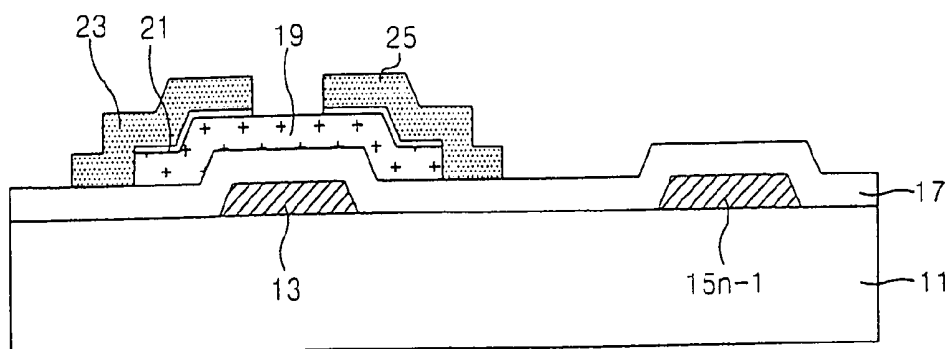


FIG. 6
CONVENTIONAL ART

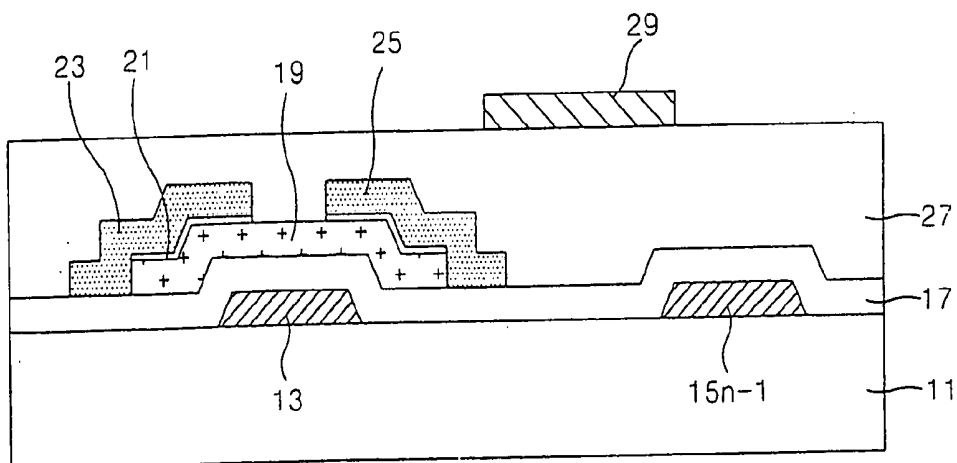


FIG. 7
CONVENTIONAL ART

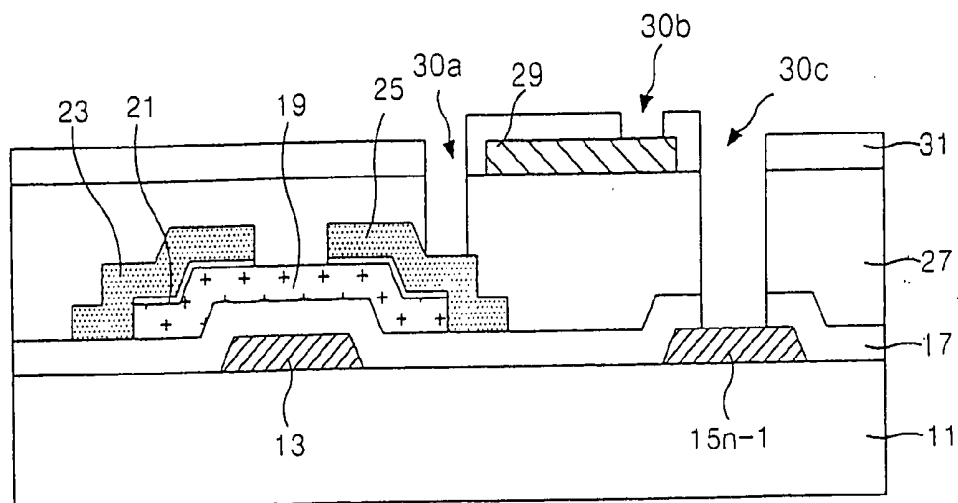


FIG. 8
CONVENTIONAL ART

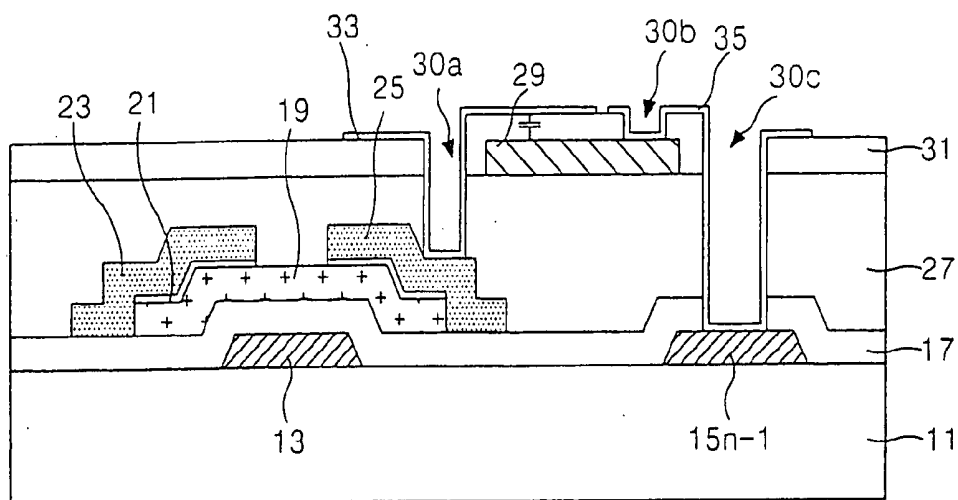


FIG. 9

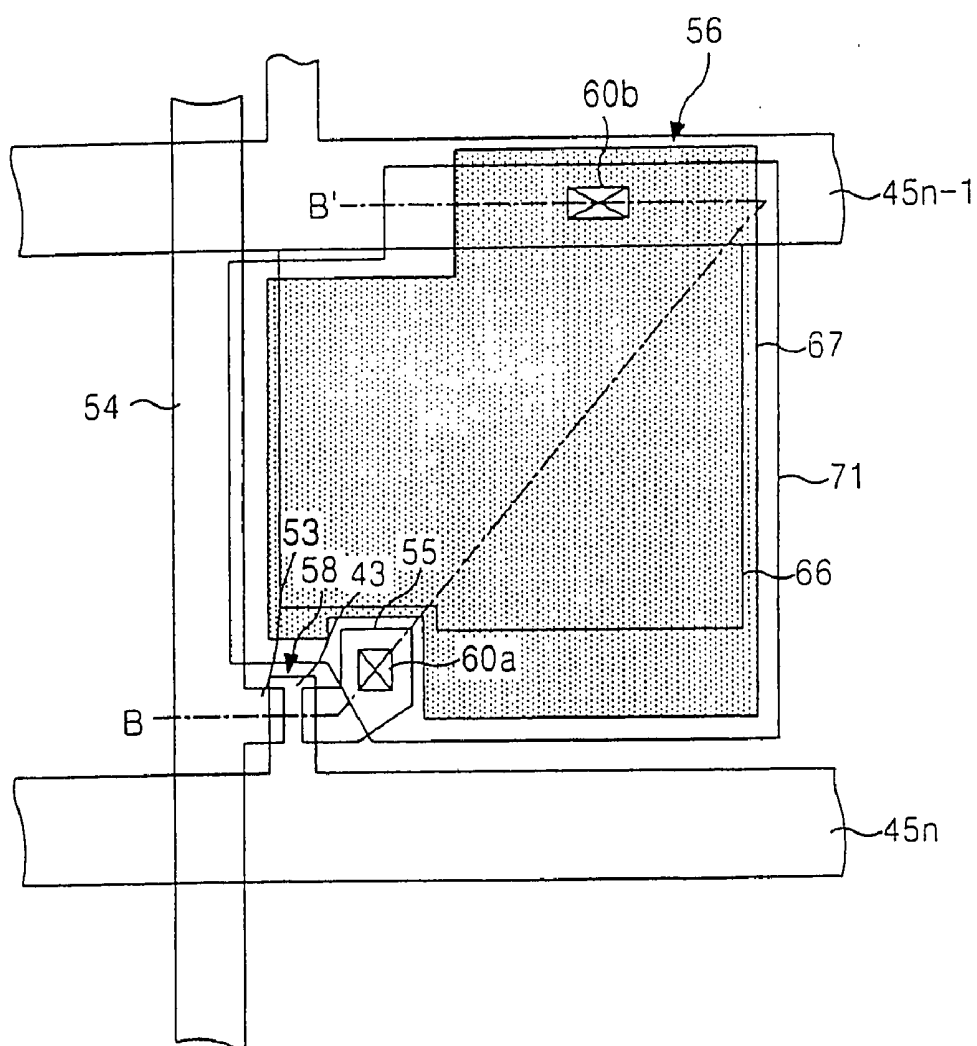


FIG. 10

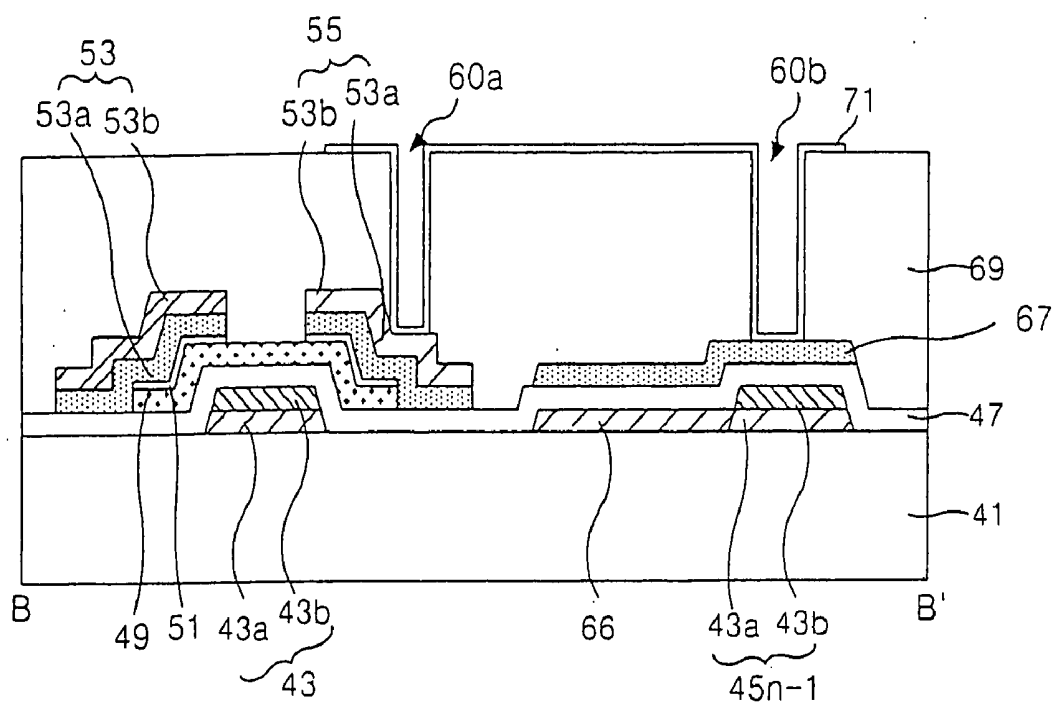


FIG. 11

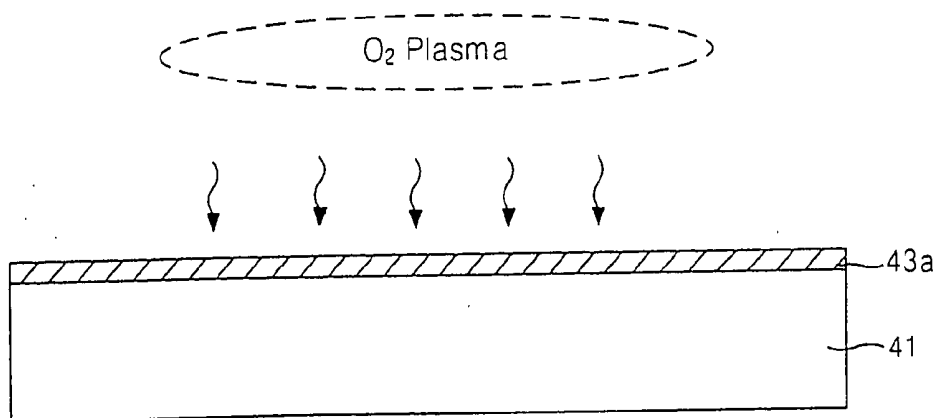


FIG. 12

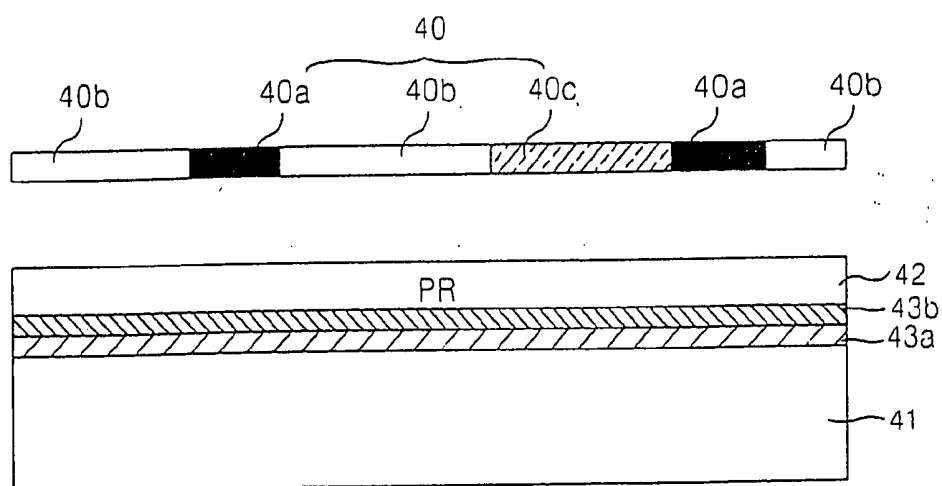


FIG.13

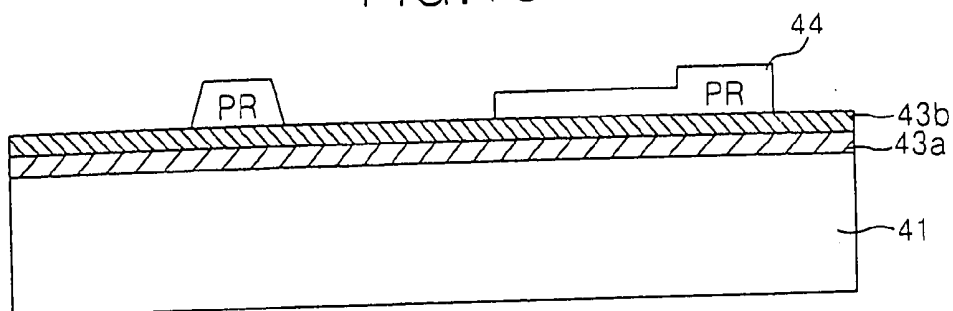


FIG.14

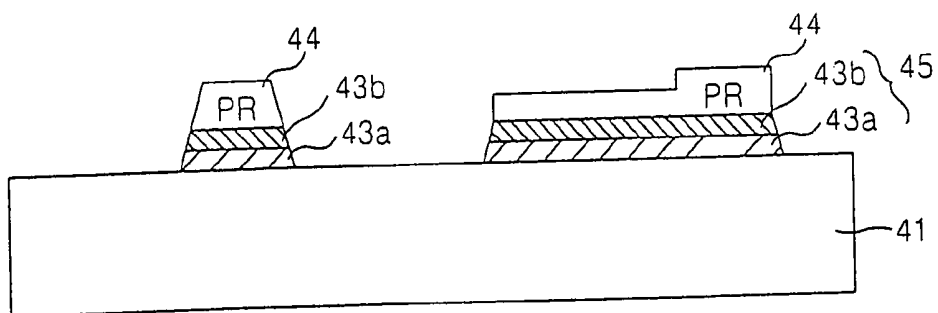


FIG.15

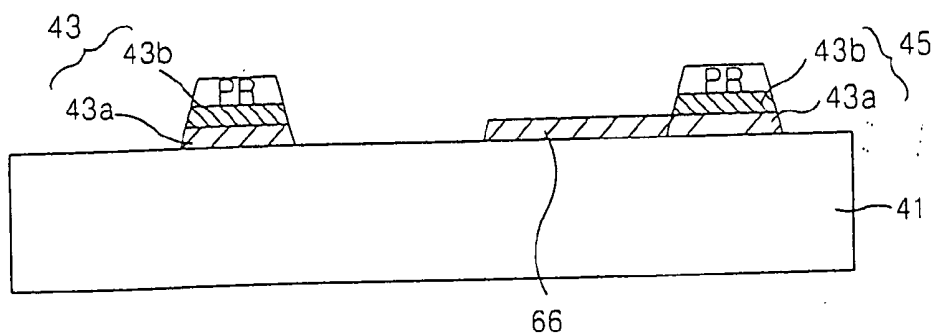


FIG. 16

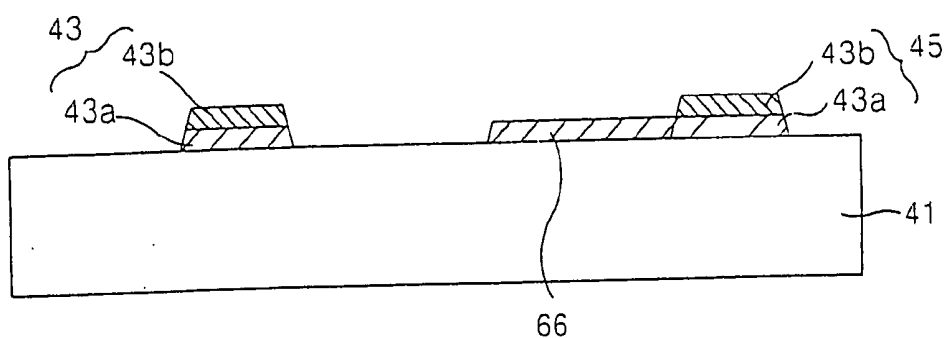


FIG. 17

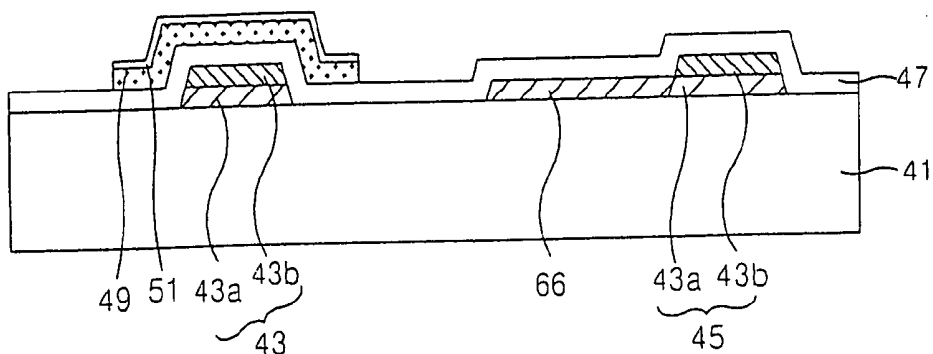


FIG. 18

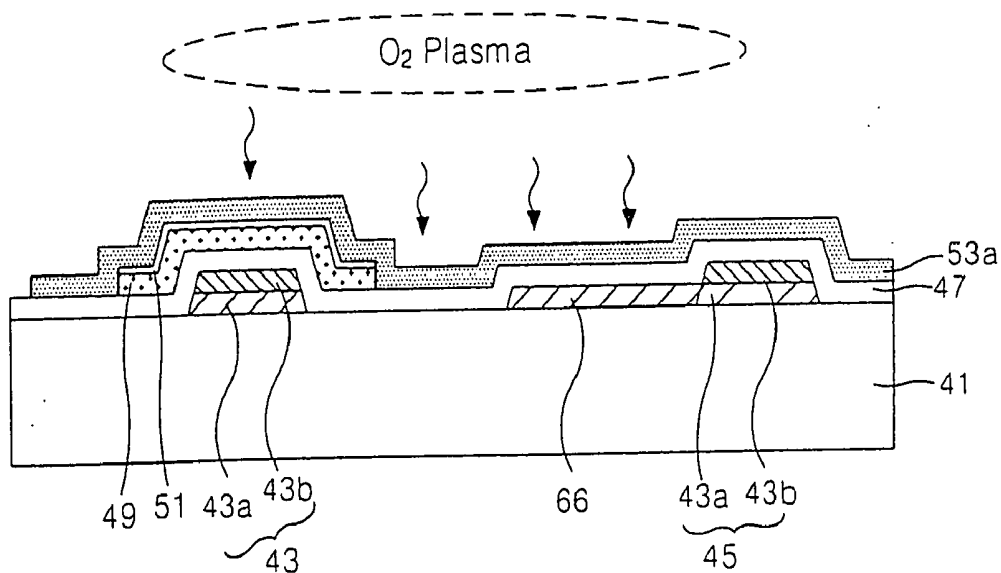


FIG. 19

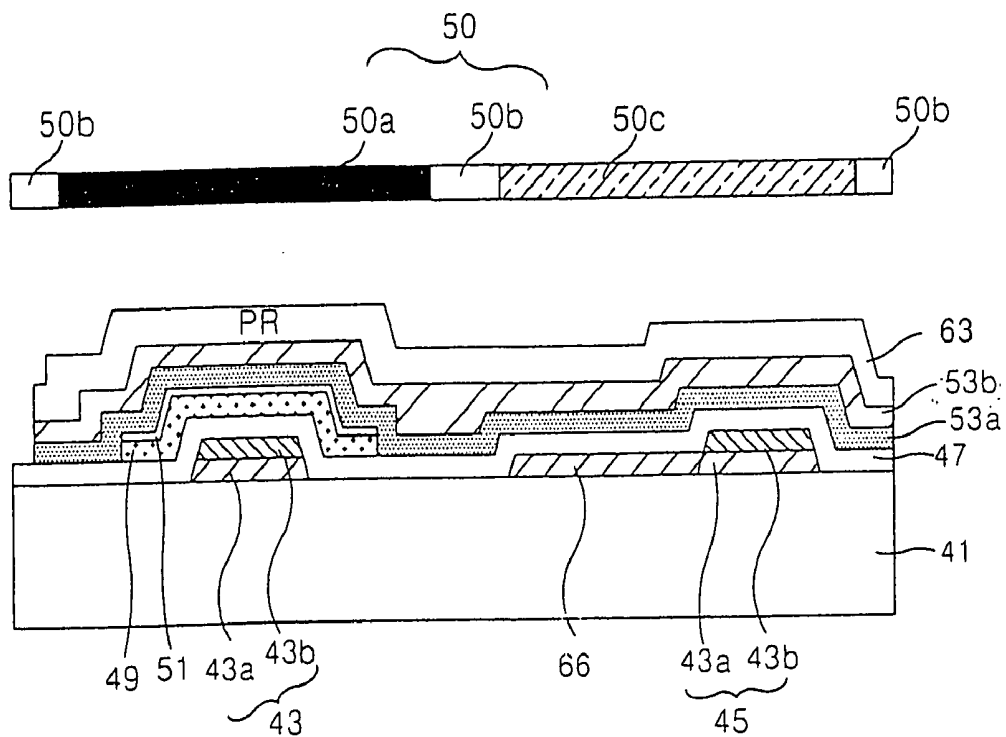


FIG.20

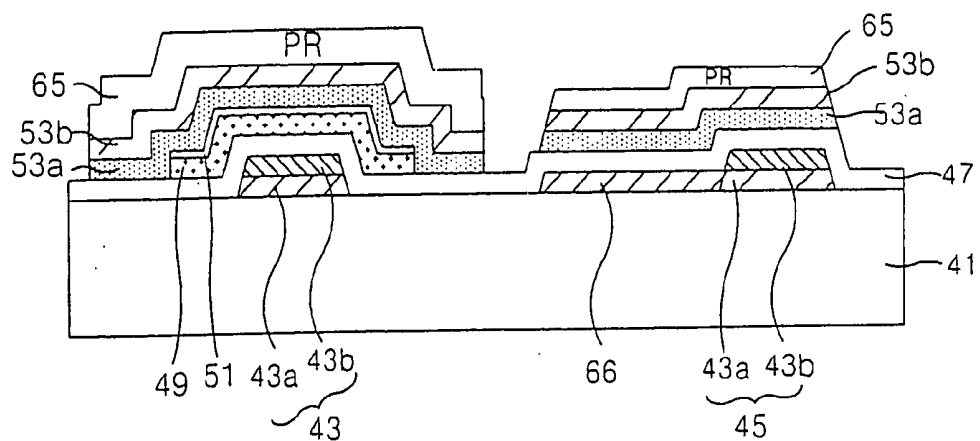


FIG.21

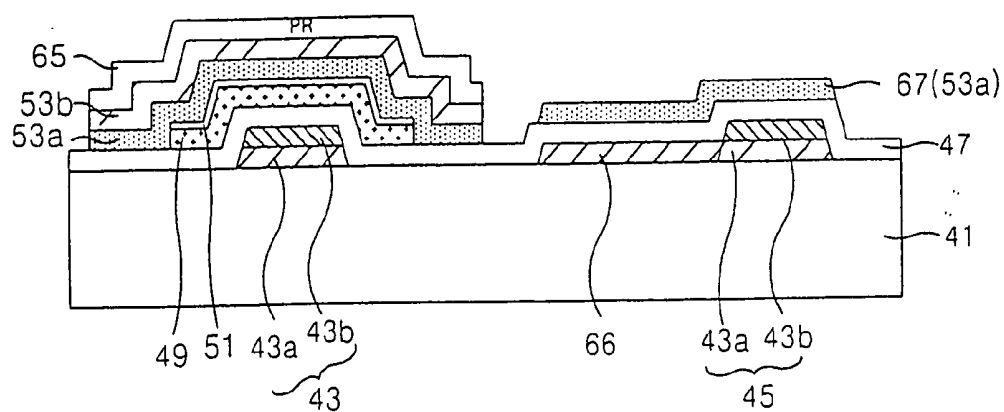


FIG.22

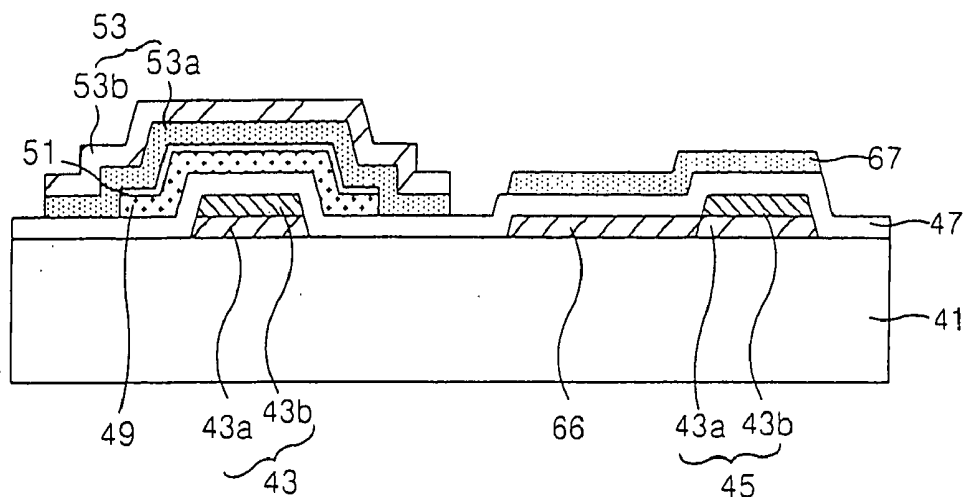


FIG.23

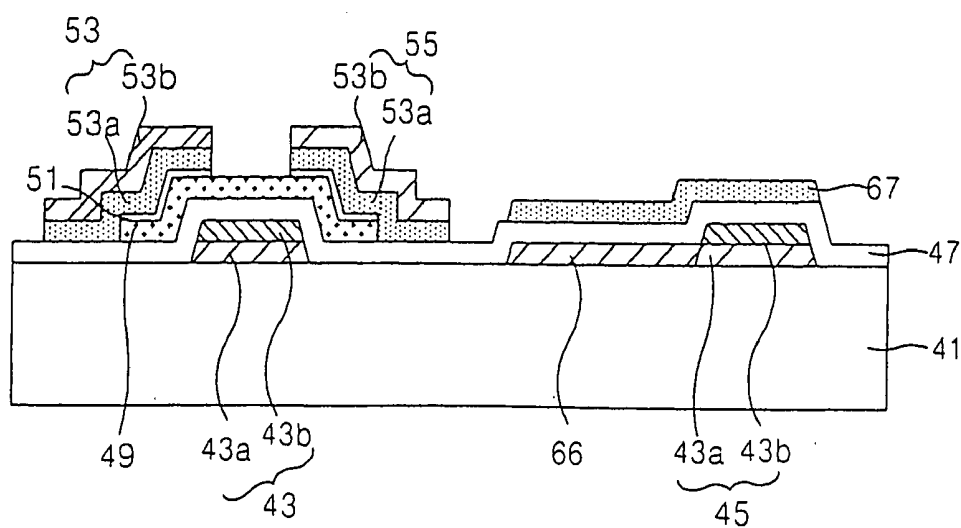


FIG. 24

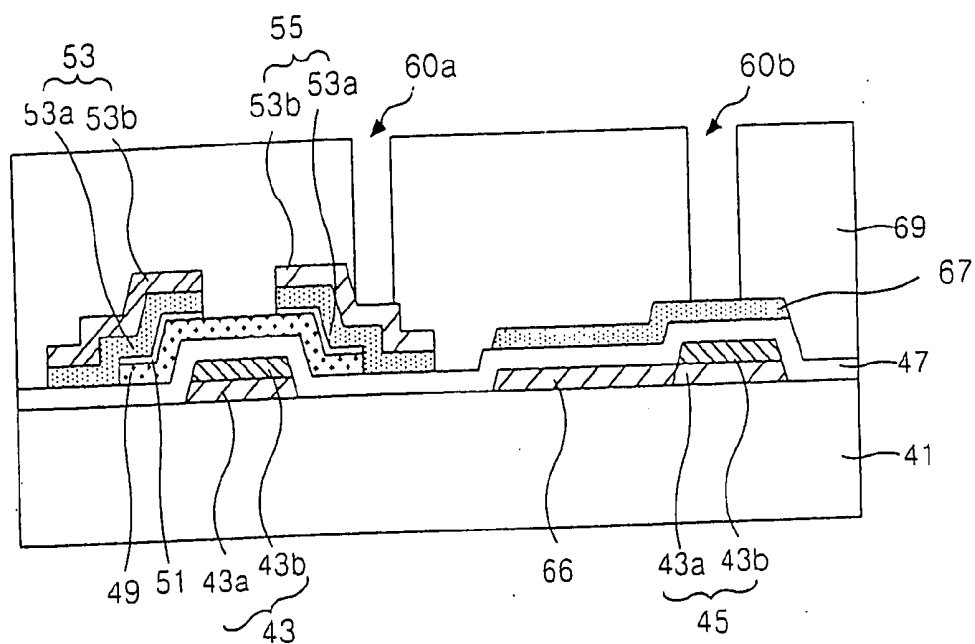


FIG. 25

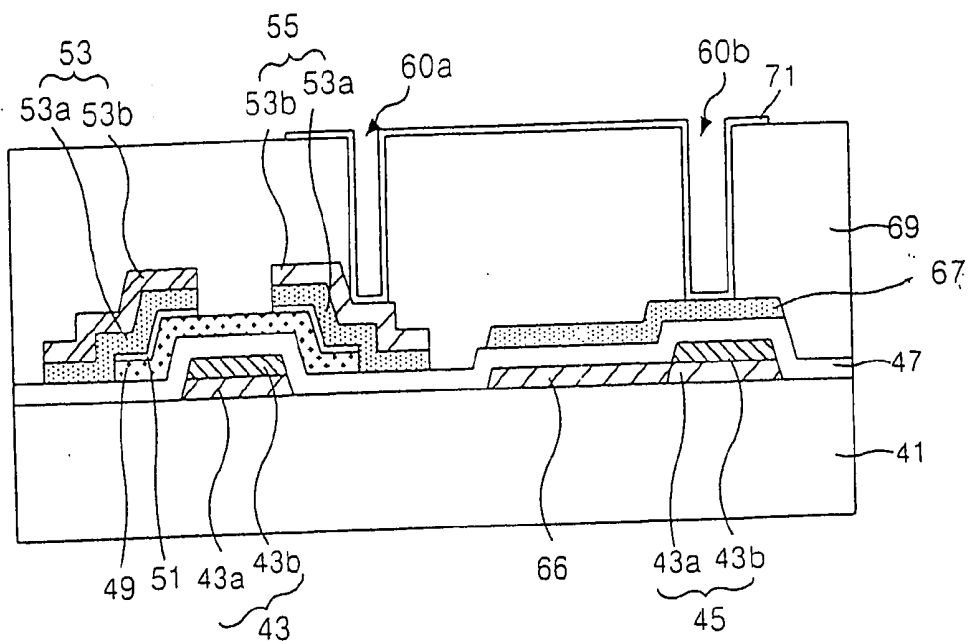
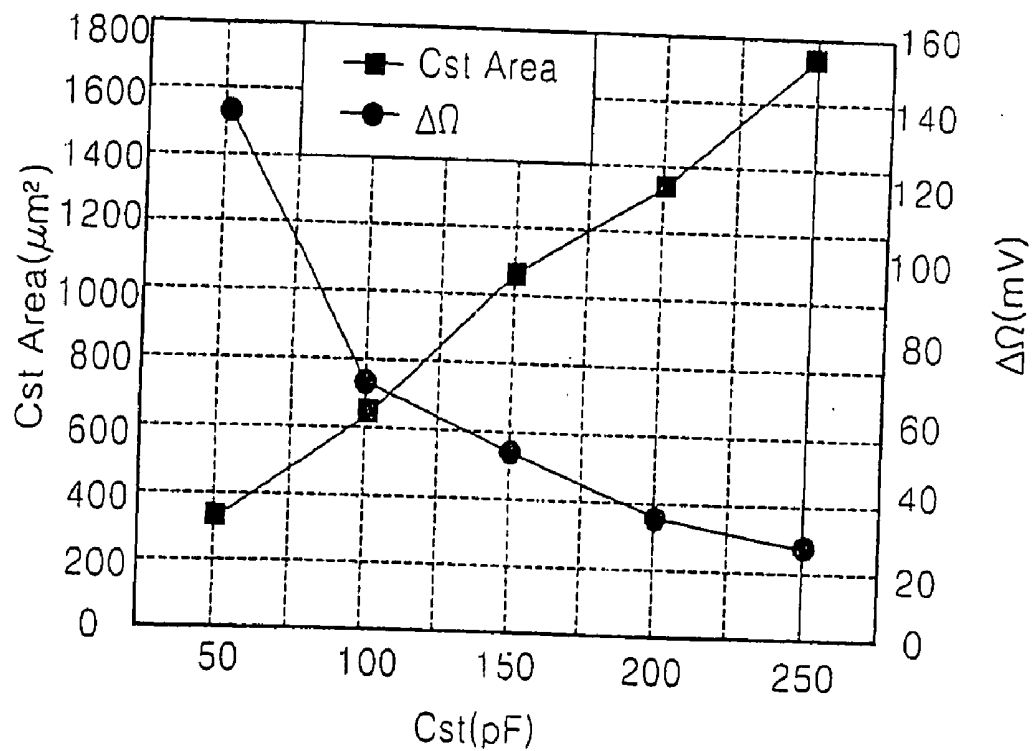


FIG. 26



ARRAY SUBSTRATE OF LIQUID CRYSTAL DISPLAY AND FABRICATING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The application is a Continuation of co-pending application Ser. No. 10/183,683, filed on Jun. 28, 2002, which claims priority to Korean Patent Application No. P2001-40605 filed Jul. 7, 2001, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to an array substrate of a liquid crystal display and a fabricating method thereof, and more particularly to an array substrate of a liquid crystal display and a fabricating method thereof that is capable of increasing the electrostatic capacitance of a storage capacitor without any decrease of an aperture ratio to reduce flickers and to lessen the number of required processes.

[0004] 2. Description of the Related Art

[0005] Generally, a liquid crystal display LCD controls a light transmittance of a liquid crystal using an electric field to display a picture. To this end, the LCD includes a liquid crystal display panel having liquid crystal pixels arranged in a matrix type, and a driving circuit for driving the liquid crystal display panel.

[0006] In the liquid crystal display panel, there are provided a pixel electrode and a common electrode for applying an electric field to each of the liquid crystal pixels. The pixel electrode is formed on a lower substrate by liquid crystal pixels, whereas the common electrode is formed on the entire surface of an upper substrate. Each pixel electrode is connected to a thin film transistor TFT used as a switching device. The pixel electrode together with the common electrode drives the liquid crystal pixel in accordance with data signals supplied through the TFT.

[0007] FIG. 1 is a plan view showing an array substrate of a conventional liquid crystal display, FIG. 2 is a sectional view of the array substrate of the liquid crystal display taken along the line "A-A" shown in FIG. 1.

[0008] Referring to FIGS. 1 and 2, a lower substrate 11 of a liquid crystal display includes a TFT 28 located at the intersection of a data line 24 and a gate line 15n, a pixel electrode 33 connected to a drain electrode 25 of the TFT 28, and a storage capacitor 26 located at the overlapping area of the pixel electrode 33 and a previous gate line 15n-1.

[0009] The TFT 28 includes a gate electrode 13 connected to the gate line 15n, a source electrode 23 connected to the data line 24, and the drain electrode 25 connected to the pixel electrode 33 through a first contact hole 30a. Also, the TFT 28 further includes a gate insulating film 17 for insulating the gate electrode 13 from the source and drain electrode 23 and 25, and semiconductor layers 19 and 21 for defining a channel between the source electrode 23 and the drain electrode 25 by a gate voltage applied to the gate electrode 13. The TFT 28 responds to a gate signal from the gate line 15 to selectively apply a data signal from the data line 24 to the pixel electrode 33.

[0010] The pixel electrode 33 is positioned at a cell area divided by the data line 24 and the gate line 15n, and is made of a transparent conductive material having a high light transmissivity, such as indium tin oxide ITO, etc. The pixel electrode 33 is formed on a second protective layer 31 spread on the entire surface of the lower substrate, is electrically connected to the drain electrode 25 through the first contact hole 30a passing through first and second protective layers 27 and 31. Such a pixel electrode 33 generates a potential difference from a common transparent electrode (not shown) provided at an upper substrate (not shown) by a data signal applied via the TFT. By this potential difference, a liquid crystal positioned between the lower substrate 11 and the upper substrate rotates due to its dielectric anisotropy. In other words, the liquid crystal display changes the molecular arrangement of the liquid crystal cells in accordance with the voltage applied by the pixels, to display images or the like.

[0011] FIGS. 3 to 8 are sectional views showing by steps a conventional fabricating method of the liquid crystal display shown in FIG. 2.

[0012] Referring to FIG. 3, there are formed the gate electrode 13 and the previous gate line 15n-1 on the lower substrate 11. Aluminum Al or Copper Cu is deposited on the entire surface of the substrate 11 by a known deposition method such as a sputtering method, etc. and is then patterned to form the gate electrode 13 and the previous gate line 15n-1.

[0013] Referring to FIG. 4, a gate insulating film 17 is formed over the gate electrode 13 and the previous gate line 15n-1. Then an active layer 19 and an ohmic contact layer 21 are formed on the gate insulating film 17. In this step, an insulating material is entirely deposited to cover the gate electrode 13 and the gate line 15n-1 by a plasma enhanced chemical vapor deposition PECVD method, to form the gate insulating film 17. The active layer 19 and the ohmic contact layer 21 are formed by depositing two semiconductor layers on the gate insulating film 17 and patterning them. Herein, the active layer 19 is formed of amorphous silicon that is not doped with impurities. The ohmic contact layer 21 is formed of amorphous silicon that is extensively doped with impurities of N type or P type.

[0014] Referring to FIG. 5, the data line 24 and the source and drain electrodes 23 and 25 are formed on the gate insulating film 17. In this step, a metal is entirely deposited by a CVD technique or sputtering technique and then patterned to form the data line 24 and the source and drain electrodes 23 and 25. The source and drain electrodes 23 and 25 are patterned, and then the area of the ohmic contact layer 21 corresponding to the gate electrode 13 is patterned to expose the active layer 19. The area corresponding to the gate electrode 13 between the source and drain electrodes 23 and 25 in the active layer 19 becomes a channel. The data line 24 and the source and drain electrodes 23 and 25 are formed of chromium Cr or molybdenum Mo.

[0015] Referring to FIG. 6, the first protective layer 27 and a storage electrode 29 are formed on the gate insulating film 17. In this step, the first protective layer 27 are formed by depositing an insulating material on the gate insulating layer 17 with the thickness of 1~2 μm to cover the source and drain electrodes 23 and 25. The first protective layer 27 is formed of an organic insulating material with a small

dielectric constant such as acrylic organic compound, Teflon, benzocyclobutene BCB, Cytop, or perfluorocyclobutane PFCB.

[0016] The storage electrode 29 is formed by depositing a transparent conductive material on the first protective layer 27, and then patterning it. The storage electrode 29 is formed of indium-tin-oxide (ITO), indium-zinc-oxide (IZO), or indium-tin-zinc-oxide (ITZO).

[0017] Referring to FIG. 7, the second protective layer 31 is formed on the first protective layer 27 and the storage electrode 29. The first to third contact holes 30a, 30b and 30c are provided through the first and/or second protective layers 27 and 31. In this step, the second protective layer 31 is formed by depositing an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x) with the thickness of around 2000-4000 Å. After that, the first to third contact holes 30a, 30b and 30c are formed by selecting removing the first and/or second protective layers 27 and 31 and the gate insulating film 17.

[0018] Referring to FIG. 8, the pixel electrode 33 and a transparent electrode 35 are formed on the second protective layer 31 and in the contact holes 30a, 30b and 30c. In this step, the pixel electrode 33 is formed by depositing a transparent conductive material on the second protective layer 31 and the first contact hole 30a, and then patterning it. The pixel electrode 33 is electrically in contact with the drain electrode 25 through the first contact hole 30a. The pixel electrode is formed of any one of ITO, IZO, or ITZO.

[0019] The transparent electrode 35 is formed by depositing a transparent conductive material on the second protective layer 31 and the second and third contact holes 30b and 30c, and then patterning it. The transparent electrode 35 is electrically in contact with the storage electrode 29 and the previous gate line 15n-1 through the second and the third contact holes 30b and 30c.

[0020] In the foregoing liquid crystal display, if the TFT turns on, electric charge is accumulated at a storage capacitor and a liquid crystal is driven. The flicker occurring during the operation of the liquid crystal display decreases if the difference (ΔV_p) of a descending voltage upon driving in relation to the accumulated voltage at the storage capacitor is smaller. The fluctuating voltage ΔV_p is decided by the capacitance Cst of the storage capacitor, the capacitance Clc of the liquid crystal, a parasitic capacitance Cgs between the gate electrode 13 and the source electrode 23 of the TFT, and a voltage difference ΔV_g of the pulse applied to the gate electrode 13. The fluctuating voltage ΔV_p is defined as follows according to FORMULA (1).

$$\Delta V_p = (C_{gs}/C_{st} + C_{lc} + C_{gs}) * \Delta V_g \quad (1)$$

[0021] Herein, Cst represents a capacitance of the storage capacitor, Clc represents a capacitance of the liquid crystal, Cgs represents a parasitic capacitance between corresponding gate and source electrodes, and ΔV_g represents a difference in the gate voltage.

[0022] According to the FORMULA (1) above, to decrease the fluctuating voltage ΔV_p for reducing flickers, the capacitance Cst of the storage capacitor should be increased, or the capacitor Clc of the liquid crystal or the parasitic capacitance Cgs or the voltage difference ΔV_g of the gate voltage should be decreased. If the capacitance Clc

of the liquid crystal, the parasitic capacitance Cgs, and the gate voltage difference ΔV_g are invariable, then at least the capacitance Cst should be increased. And to increase the capacitance Cst of the storage capacitor, the area of the storage electrode needs to be increased. However, an increase of the area of the storage electrode decreases the aperture ratio of the LCD. Particularly, the aperture ratio drops significantly in a ferroelectric LCD that requires a high capacitance Cst of the storage capacitor or in an LCD that requires high precision.

[0023] Therefore, there is a need to provide an LCD and its fabrication method that overcome these problems of the related art. Further, there is a need to reduce costs associated with the LCD and its fabrication method by eliminating or reducing the use of expensive masks in fabricating processes of the LCD.

SUMMARY OF THE INVENTION

[0024] Accordingly, it is an object of the present invention to provide a liquid crystal display (LCD) and a fabricating method thereof that is capable of increasing the electrostatic capacitance of a storage capacitor without decreasing the aperture ratio of the LCD to reduce flickers and lessen the number of fabrication steps.

[0025] It is another object of the present invention to provide an LCD and its fabrication method that overcome the problems and disadvantages associated with the related art.

[0026] In order to achieve these and other objects of the invention, an array substrate of a liquid crystal display according to an embodiment of the present invention includes a substrate; a plurality of gate lines formed on the substrate; a plurality of data lines formed on the substrate to intersect perpendicularly to the gate lines; pixel areas defined by the gate lines and the data lines; thin film transistors each formed at each intersection of the gate line and the data line; pixel electrodes each formed on each pixel area to be connected to the thin film transistor, wherein the gate lines are formed from a disposed material of a first and second metal layer, and wherein the first metal layer of the gate line is extended on the pixel area.

[0027] In the array substrate according to one embodiment, the first metal layer of the gate line is an oxidized metal layer.

[0028] In the array substrate according to one embodiment, the first metal layer of the gate line is formed from any one of a titanium oxide and an indium zinc oxide.

[0029] In the array substrate according to one embodiment, the first metal layer of the gate line is below 50 Å in the thickness.

[0030] In the array substrate according to one embodiment, the second metal layer of the gate line is formed from any one of a copper and an aluminum.

[0031] In the array substrate according to one embodiment, the first metal layer of the gate line extended on the pixel area forms a first electrode of a storage capacitor.

[0032] In the array substrate according to one embodiment, the thin film transistor includes: a gate electrode connected to the gate line; an active layer formed on a gate

insulating film over the gate electrode; a source electrode formed on the active layer and connected to the data line; and a drain electrode formed on the active layer with a constant distance from the source electrode and connected to the pixel electrode, wherein the data line, the source electrode and the drain electrode are formed from a disposed material of a third metal layer and a fourth metal layer.

[0033] In the array substrate according to one embodiment, the third metal layer is an oxidized metal layer.

[0034] In the array substrate according to one embodiment, the third metal layer is any one of a titanium oxide and an indium zinc oxide.

[0035] In the array substrate according to one embodiment, the third metal layer is below 50 Å in the thickness.

[0036] In the array substrate according to one embodiment, the third metal layer has an extending part on the pixel, the extending part overlapping the extending part of the first metal layer with the gate insulating film therebetween and forming a second electrode of the storage capacitor.

[0037] In the array substrate according to one embodiment, further comprises an insulating film between the second electrode of the storage capacitor and the pixel electrode, wherein the second electrode of the storage capacitor are electrically connected to the pixel electrode through a contact hole formed in the insulating film over the gate line.

[0038] In the array substrate according to one embodiment, the storage capacitor formed by the extending parts of the first and third metal layers has the capacitance of above 100 times in opposition to a parasitic capacitor between the gate electrode and the source electrode of the thin film transistor.

[0039] A method of fabricating a array substrate of a liquid crystal display according to another aspect of the present invention includes steps of depositing a first metal layer on a substrate; forming an oxidized metal layer by oxidizing the first metal layer; depositing a second metal layer on the oxidized metal layer; forming a photo-resist layer on the second metal layer; patterning the photo-resist layer into a first region with the photo-resist of a first thickness, a second region with the photo-resist of a second thickness and a third region without the photo-resist; etching simultaneously the oxidized metal layer and the second metal layer in the third region; etching the second metal layer in the first region to produce a first metal portion of the oxidized metal layer and a second metal portion having the oxidized and the second metal layers.

[0040] In the array substrate according to one embodiment, the oxidized metal layer includes any one of a titanium oxide and an indium zinc oxide.

[0041] In the array substrate according to one embodiment, the oxidized metal layer is below 50 Å in the thickness.

[0042] In the array substrate according to one embodiment, the second metal layer includes at least one of a copper and an aluminum.

[0043] In the array substrate according to one embodiment, the second metal portion is used for a gate line and a gate electrode.

[0044] In the array substrate according to one embodiment, the first metal portion is used for an electrode of a storage capacitor.

[0045] In the array substrate according to one embodiment, the second metal portion is used for a data line, a source electrode and a drain electrode.

[0046] In the array substrate according to one embodiment, the patterning of the photo-resist layer into the first to third regions employs a diffractive mask.

[0047] In the array substrate according to one embodiment, the photo-resist layer of the first region corresponds to a thickness of 10~50% in opposition to that of the second region.

[0048] In the array substrate according to one embodiment, further comprises an ashing for removing the photo-resist resident on the first region after the etching of the oxidized metal layer and the second metal layer.

[0049] In the array substrate according to one embodiment, the forming of the oxidized metal layer includes an exposing of the first metal layer to an O₂ plasma.

BRIEF DESCRIPTION OF THE DRAWINGS

[0050] These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

[0051] FIG. 1 is a plan view of an array substrate of a liquid crystal display according to a conventional technique;

[0052] FIG. 2 is a sectional view of the array substrate of the liquid crystal display taken along the line "A-A" shown in FIG. 1;

[0053] FIGS. 3 to 8 are sectional views representing by steps a conventional fabricating method of the array substrate of the liquid crystal display shown in FIG. 2;

[0054] FIG. 9 is a plan view of an array substrate of a liquid crystal display according to an embodiment of the present invention;

[0055] FIG. 10 is a sectional view of the array substrate of the liquid crystal display taken along the line "B-B" shown in FIG. 9;

[0056] FIGS. 11 to 25 are sectional views representing processing steps of a fabricating method of the array substrate of the liquid crystal display shown in FIG. 10 according to an embodiment of the present invention; and

[0057] FIG. 26 is a graph showing an example of the relation of capacitance of a capacitor and $\Delta\Omega$ according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0058] With reference to FIGS. 9 to 26, preferred embodiments of the present invention are explained as follows.

[0059] Referring to FIGS. 9 and 10, a lower substrate 41 of a liquid crystal display according to an embodiment of the present invention includes a TFT 58 located at the intersection of a data line 54 and a gate line 45n, a pixel electrode 71 connected to a drain electrode 55 of the TFT 58, and a

storage capacitor **56** located at the overlapping area of the pixel electrode **71** and a previous gate line **45_{n-1}**.

[0060] The TFT **58** includes a gate electrode **43** connected to a gate line **45_n**, a source electrode **53** connected to the data line **54**, and a drain electrode **55** connected to the pixel electrode **71** through a first contact hole **60a**. The TFT **58** further includes a gate insulating film **47** for insulating the gate electrode **43** from the source and drain electrodes **53** and **55**, and semiconductor layers **49** and **51** for defining a channel between the source electrode **53** and the drain electrode **55** by a gate voltage applied to the gate electrode **43**. The TFT **58** responds to a gate signal from the gate line **45_n** to selectively apply a data signal from the data line **54** to the pixel electrode **71**.

[0061] The pixel electrode **71** is positioned at a cell area divided by the data line **54** and the gate line **45_n** and is made of, e.g., a transparent conductive material having a high light transmissivity such as indium tin oxide ITO, etc. The pixel electrode **71** is formed on an organic insulating film **69** spread on the entire surface of the lower substrate **41**, is electrically connected to the drain electrode **55** through the first contact hole **60a** which is formed through the organic insulating film **69**, and is electrically connected to a second storage electrode **67** through a second contact hole **60b**. Such a pixel electrode **71** generates a potential difference from a common transparent electrode (not shown) provided at an upper substrate (not shown) by a data signal applied via the TFT **58**. By this potential difference, a liquid crystal positioned between the lower substrate **41** and the upper substrate rotates due to its dielectric anisotropy. In other words, the liquid crystal display changes the molecular arrangement of the liquid crystal by pixels in accordance with the voltage applied by the pixels, to display pictures, images or any other displayable entity.

[0062] FIGS. **11** to **25** are sectional views representing processing steps of a fabricating method of a liquid crystal display shown in FIG. **10** according to an embodiment of the present invention.

[0063] Referring to FIG. **11**, a first oxidized metal layer **43a** is formed on the substrate **41**. In this step, the first oxidized metal layer **43a** is formed by depositing titanium Ti or the like with the thickness of around 50 Å using a deposition method such as a sputtering method, etc., and then making it react with oxygen O₂ in a plasma state. As a result, the first oxidized metal layer **43a** made of a transparent conductive material such as titanium oxide TiO_x, ITO, etc. is produced.

[0064] Referring to FIG. **12**, a first metal layer **43b** and a photoresist **42** are formed on the first oxidized metal layer **43a**. A diffractive mask **40** having a shielding part **40a**, a transmission part **40b** and a diffraction part **40c** is arranged over the upper part of the photoresist **42**.

[0065] Particularly, copper Cu, aluminum Al, or any other suitable metal material is deposited on the first oxidized metal layer **43a** by a deposition method such as sputtering, etc. to form the first metal layer **43b**. The shielding parts **40a** of the diffractive mask **40** correspond respectively to the gate electrode **43** of the TFT **58** and the gate line **45** being a part of the storage capacitor to be defined later. The diffraction part **40c** corresponds to the area where a first storage electrode **66** is to be formed. The transmission part **40b**

corresponds to the other areas. The shielding part **40a** of the diffractive mask **40** shuts off UV light, the transmission part **40b** transmits the UV light, and the diffractive part **40c** transmits around 10-50% of the UV light.

[0066] Subsequently, a photoresist pattern **44** is formed on the first metal layer **43b** as shown in FIG. **13**. The photoresist pattern **44** is formed by developing the photoresist **42** with a developing solution such as alkaline aqueous solution, etc. In the step, the photoresist pattern **44** with its original thickness (before patterning) is formed at an area corresponding to the shielding part **40a** of the diffractive mask **40**. The photoresist pattern **44** with the thickness of around 10~50% of its original thickness, is formed at an area corresponding to the diffraction part **40c** of the mask **40**. The photoresist pattern **44** is eliminated at an area corresponding to the transmission part **40b** of the mask **40** to expose portions of the first metal layer **43b**.

[0067] Then, the first metal layer **43b** and the first oxidized metal layer **43a** on the substrate **41** are patterned as shown in FIG. **14**. Portions of the first oxidized metal layer **43a** and the first metal layer **43b** corresponding to the photoresist pattern **44** remain by a wet etching process. As a result, a gate electrode **43** and a gate line corresponding to the shield parts **40a** of the mask **40** are defined.

[0068] Referring to FIG. **15**, the portion of the photoresist pattern **44** with the thickness of around 10~50% of its original thickness is removed by an ashing process or any other suitable process. Then, the exposed portion of the first metal layer **43b** is selectively etched. Accordingly, the portion of the first oxidized metal layer **43a** corresponding to the diffraction part **40c** of the diffractive mask **40** extends or is connected to the gate line **45**, and is exposed. As discussed above, portions of the first oxidized metal layer **43a** and the first metal layer **43b** become the gate electrode **43** of the TFT **58**. The portion of the first oxidized metal layer **43a** extended to the pixel area becomes the first storage electrode **66**. Then, all the photoresist pattern **44** on the gate electrode **43** and the gate line **45** is eliminated as illustrated in FIG. **16**.

[0069] Referring to FIG. **17**, a gate insulating film **47**, an active layer **49** and an ohmic contact layer **51** are formed on the gate electrode **43** and the gate line **45**. This step can be implemented as follows.

[0070] Silicon nitride SiO_x or silicon oxide SiO_x is entirely deposited by a PECVD technique in the manner of covering the gate electrode **43** and the gate line **45** to form the gate insulating film **47**. Two semiconductor layers are deposited on the gate insulating film **47** and then patterned to form the active layer **49** and the ohmic contact layer **51**. Herein, the active layer **49** is formed of amorphous silicon that is not doped with impurities. The ohmic contact layer **51** is formed of amorphous silicon that is extensively doped with impurities of N type or P type.

[0071] Referring to FIG. **18**, a second oxidized metal layer **53a** is formed on the gate insulating film **47** and the ohmic contact layer **51**. The second oxidized metal layer **53a** is formed by a deposition method such as sputtering, etc. Particularly, the second oxidized metal layer **53a** is formed by depositing titanium Ti with the thickness of around 50 Å, and then making it react with oxygen O₂ in a plasma state. As a result, the second oxidized metal layer **53a** made of a transparent conductive material such as titanium oxide TiO_x or ITO is produced.

[0072] Referring to FIG. 19, a second metal layer 53b and a photoresist 63 are formed on the second oxidized metal layer 53a. A diffractive mask 50 having a shielding part 50a, a transmission part 50b and a diffraction part 50c is arranged over the upper part of the photoresist 63.

[0073] More specifically, copper Cu, aluminum Al or any other suitable metal material is deposited by a deposition method such as sputtering, etc. to form the second metal layer 53b on the second oxidized metal layer 53a. The photoresist 63 is formed after entirely depositing the second metal layer 53b on the second oxidized metal layer 53a. The shielding part 50a of the diffractive mask 50 is formed at an area corresponding to the source electrode 53 and the drain electrode 55 of the TFT to be defined later. The diffraction part 50c is formed at an area where a second storage electrode 67 is to be formed. The transmission parts 50b are formed at all the other areas. The shielding part 50a of the diffractive mask 50 shuts off UV light, the transmission part 50b transmits the UV light, and the diffractive part 50c transmits around 10~50% of the UV light.

[0074] Referring to FIG. 20, a photoresist pattern 65 is formed on the second metal layer 53b. The photoresist pattern 65 is formed by developing the photoresist 63 with a developing solution such as an alkaline aqueous solution, etc. The photoresist pattern 65 having its original thickness (before patterning), is formed at an area corresponding to the shielding part 50a of the diffractive mask 50. The photoresist pattern 65 that has the thickness of 10~50% of its original thickness, is formed at an area corresponding to the diffraction part 50c. The photoresist pattern 65 is eliminated at areas corresponding to the transmission parts 50b to expose parts of the gate insulating film 47.

[0075] Then, the second metal layer 53b and the second oxidized metal layer 53a on the ohmic contact layer 51 and the gate insulating film 47 are patterned such that portions of the gate insulating film are exposed. The second oxidized metal layer 53a and the second metal layer 53b only remain at the area corresponding to the photoresist pattern 65 by a wet etching process.

[0076] Thereafter, the portion of the photoresist pattern 65 with the thickness of 10~50% of its original thickness is eliminated by an ashing process or any other suitable process. Then, the exposed portion of the second metal layer 53b is selectively etched to expose the portion of the second oxidized metal layer 53a corresponding to the diffraction part 50c of the diffractive mask 50. Herein, this part of the second oxidized metal layer 53a becomes the second storage electrode 67.

[0077] Subsequently, the photoresist pattern 65 on the second metal layer 53b is eliminated as illustrated in FIG. 22.

[0078] Then there are formed the source electrode 53 and the drain electrode 55 as shown in FIG. 23. In this step, the second oxidized metal layer 53a and the second metal layer 53b of the TFT 58 over the gate electrode 43 are patterned to form the source electrode 53 and the drain electrode 55. The ohmic contact layer 51 at an area corresponding to the gate electrode 43 is patterned to expose a part of the active layer 49. The area corresponding to the gate electrode 43 between the source electrode 53 and the drain electrode 55 becomes a channel in the active layer 49.

[0079] Referring to FIG. 24, an organic insulating film 69 is formed and the first contact hole 60a and the second contact hole 60b are formed through the organic insulating film 69. Particularly, the organic insulating film 69 is formed by depositing an insulating material in the manner of covering the source electrode 53, the drain electrode 55 and the second storage electrode 67. The insulating material is deposited and then patterned to form the first contact hole 60a and the second contact hole 60b through the organic insulating film 69. The organic insulating film 69 is formed of an organic insulating material with a small dielectric constant such as acrylic organic compound, Teflon, benzocyclobutene BCB, Cytop, perfluorocyclobutane PFCB, etc.

[0080] After that, a pixel electrode 71 is formed on the organic insulating film 69 and in the first and second contact holes 60a and 60b as shown in FIG. 25. Particularly, the pixel electrode 71 is formed by depositing a transparent conductive material on the organic insulating film 69 and then patterning it. The pixel electrode 71 is electrically in contact with the drain electrode 55 through the first contact hole 60a. The pixel electrode is formed of any one of ITO, IZO or ITZO.

[0081] FIG. 26 is a graph showing the relation of a capacitance Cst of a storage capacitor (e.g., formed by the organic insulating film 69 and the first and second storage electrodes 66 and 67) and a fluctuating voltage difference $\Delta\Omega$ according to an embodiment of the present invention.

[0082] The fluctuating voltage difference $\Delta\Omega$ is defined by the following FORMULA (2).

$$\Delta\Omega = \Delta V_{p(max)} - \Delta V_{p(min)} \quad (2)$$

Herein, $\Delta\Omega$ is defined as the difference between the maximum value and the minimum value of the fluctuating voltage ΔV_p which is the difference of the voltage decreased upon its driving in relation to the voltage accumulated to the storage capacitor.

[0083] Referring to the graph shown in FIG. 26, if the area of the storage capacitor gets bigger, the capacitance Cst of the storage capacitor increases. Also, if the value of $\Delta\Omega$ gets smaller, the capacitance Cst of the storage capacitor increases. In one example, when the value of $\Delta\Omega$ is about 40 mV in the LCD of the present invention, the capacitance Cst of the storage capacitor is around 200 pF. In this case, the process deviation is 1 μm , the parasitic capacitance Cgs is 2.03 pF, the area of the aperture region is 2005 μm^2 , and the capacitance Cst of the storage capacitor is larger than 100 times the deviation value of the parasitic capacitance Cgs.

[0084] In the present invention, if the value of $\Delta\Omega$ gets bigger, residual images occur on a screen because the difference of the maximum value and the minimum value of the fluctuating voltage is increased. To prevent displaying of the residual images, in accordance with one embodiment the value of $\Delta\Omega$ should be made less than 50 mV. Thus, in the present invention, the area of the storage capacitor is made to be big or the value of $\Delta\Omega$ is made smaller for increasing the capacitance Cst of the storage capacitor.

[0085] As described above, the liquid crystal display and the fabricating method according to the present invention is capable of increasing the capacitance of the storage capacitor without decreasing an aperture ratio of the LCD, whereby flickers are reduced or eliminated. Also, because

the number of masks being used is reduced or is not increased, the fabrication cost can be reduced when compared with a conventional fabrication method of a liquid crystal display.

[0086] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. An array substrate of a liquid crystal display, comprising:

a substrate;

a plurality of gate lines formed on the substrate;

a plurality of data lines formed on the substrate to intersect perpendicularly to the gate lines;

pixel areas defined by the gate lines and the data lines;

thin film transistors each formed at each intersection of the gate line and the data line; and

pixel electrodes each formed on each pixel area to be connected to the thin film transistor,

wherein the gate lines are formed from a disposed material of a first and second metal layer, and wherein the first metal layer of the gate line is extended on the pixel area.

2. The array substrate according to claim 1, wherein the first metal layer of the gate line is an oxidized metal layer.

3. The array substrate according to claim 1, wherein the first metal layer of the gate line is formed from any one of a titanium oxide and an indium zinc oxide.

4. The array substrate according to claim 1, wherein the first metal layer of the gate line is below 50 Å in the thickness.

5. The array substrate according to claim 1, wherein the second metal layer of the gate line is formed from any one of a copper and an aluminum.

6. The array substrate according to claim 1, wherein the first metal layer of the gate line extended on the pixel area forms a first electrode of a storage capacitor.

7. The array substrate according to claim 1, wherein the thin film transistor includes:

a gate electrode connected to the gate line;

an active layer formed on a gate insulating film over the gate electrode;

a source electrode formed on the active layer and connected to the data line; and

a drain electrode formed on the active layer with a constant distance from the source electrode and connected to the pixel electrode,

wherein the data line, the source electrode and the drain electrode are formed from a disposed material of a third metal layer and a fourth metal layer.

8. The array substrate according to claim 7, wherein the third metal layer is an oxidized metal layer.

9. The array substrate according to claim 7, wherein the third metal layer is any one of a titanium oxide and an indium zinc oxide.

10. The array substrate according to claim 7, wherein the third metal layer is below 50 Å in the thickness.

11. The array substrate according to claim 7, wherein the third metal layer has a extending part on the pixel, the extending part overlapping the extending part of the first metal layer with the gate insulating film therebetween and forming a second electrode of the storage capacitor.

12. The array substrate according to claim 11, further comprises an insulating film between the second electrode of the storage capacitor and the pixel electrode,

wherein the second electrode of the storage capacitor are electrically connected to the pixel electrode through a contact hole formed in the insulating film over the gate line.

13. The array substrate according to claim 11, wherein the storage capacitor formed by the extending parts of the first and third metal layers has the capacitance of above 100 times in opposition to a parasitic capacitor between the gate electrode and the source electrode of the thin film transistor.

14. An array substrate of a display device, comprising:

a gate line having first and second gate line layers formed respectively of a first oxidized metal layer and a first metal layer on a substrate;

a first storage electrode extending from the gate line;

a second storage electrode over the gate line and the first storage electrode;

a TFT (thin film transistor) and a data line on the substrate; and

a pixel electrode in electrical contact with the second storage electrode.

15. The array substrate according to claim 14, wherein the data line includes first and second data line layers respectively formed of a second oxidized metal layer and a second metal layer.

16. The array substrate according to claim 14, wherein the TFT includes:

a gate electrode extending from another gate line adjacent to the gate line having the first and second gate line layers;

a source electrode extending from the data line; and

a drain electrode in electrical contact with the pixel electrode.

17. The array substrate according to claim 16, wherein the gate electrode includes first and second gate electrode layers respectively formed of the first oxidized metal layer and the first metal layer.

18. The array substrate according to claim 16, wherein at least one of the source and drain electrodes includes first and second electrode layers respectively formed of a second oxidized metal layer and a second metal layer.

19. A display device comprising:

first and second gate lines and a data line on a substrate, the first and second gate lines crossing the data line;

a TFT (thin film transistor) at an intersection area of the first gate line and the data line;

a pixel electrode connected to the TFT; and

a first storage electrode extending from the second gate line,

wherein at least one of the first and second gate lines and the data line includes first and second line layers respectively formed of an oxidized metal layer and a metal layer.

20. The display device according to claim 19, wherein the TFT includes:

a gate electrode extending from the first gate line;

a source electrode extending from the data line; and

a drain electrode in contact with the pixel electrode,

wherein at least one of the gate, source and drain electrodes includes first and second electrode layers respectively formed of an oxidized metal layer and a metal layer.

21. The display device according to claim 19, further comprising:

a second storage electrode over the second gate line and the first storage electrode, and in contact with the pixel electrode.

* * * * *

专利名称(译)	液晶显示器的阵列基板及其制造方法		
公开(公告)号	US20070188671A1	公开(公告)日	2007-08-16
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优先权	1020010040605 2001-07-07 KR		
其他公开文献	US7522224		
外部链接	Espacenet USPTO		

摘要(译)

液晶器件的阵列基板具有多条栅极线，数据线，像素区和薄膜晶体管，其中栅极线由第一和第二金属层的材料形成，并且其中第一金属层栅极线在像素区域上延伸。此外，显示装置在基板上具有第一和第二栅极线和数据线，薄膜晶体管，像素电极，从第二栅极线延伸的第一存储电极，并且其中第一和第二栅极线中的至少一个数据线包括分别由氧化金属和金属层形成的第一和第二线层。

