(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 September 2001 (27.09.2001)

PCT

(10) International Publication Number
WO 01/71703 A1

(51) International Patent Classification[7]: G09G 3/36

(21) International Application Number: PCT/EP01/02819

(22) International Filing Date: 13 March 2001 (13.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0006811.4 22 March 2000 (22.03.2000) GB

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors: HUGHES, John, R.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). PARKER, David, W.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: WILLIAMSON, Paul, L.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

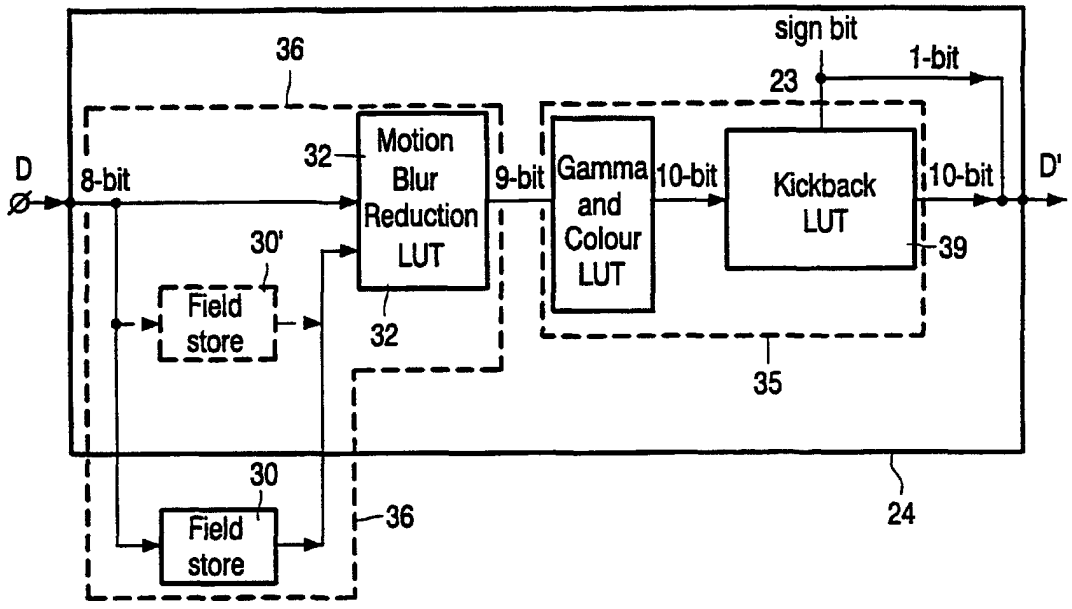
(81) Designated States *(national)*: CN, JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CONTROLLER CIRCUIT FOR LIQUID CRYSTAL MATRIX DISPLAY DEVICES



(57) Abstract: A controller circuit (24) for processing video data for an active matrix liquid crystal display device has processing circuitry for performing correction functions on the input video data (D) prior to being supplied to the drive circuit (22) of the display device comprising gamma and colour correction, and correction for reducing motion blur in the display picture. The correction circuits (35,36) are organised such that correction for motion blur reduction (36) is carried out before the gamma and colour corrections (35), which enables a beneficial decrease in semiconductor area required when implementing the circuitry in IC form through the size of field store (30) and LUT (32) components used for this function then being smaller. Gamma and colour corrections are performed together using a single LUT. Correction for kickback may further be included, such correction preferably being arranged after the gamma and colour corrections and using a separate LUT.

WO 01/71703 A1

DESCRIPTION

CONTROLLER CIRCUIT FOR LIQUID CRYSTAL MATRIX DISPLAY DEVICES

This invention relates to a controller circuit, preferably in the form of a semiconductor integrated circuit (IC), for processing video data for liquid crystal matrix display devices, the circuit having an input to which video data is applied and an output from which processed video data is supplied for the pixels of the display device.

In a typical active matrix liquid crystal display device, (AMLCD), a video signal, for example from a computer or other source, is supplied to video signal processing and control circuitry which outputs processed video signals and timing signals to row (selection) and column (source) driver circuits associated with the pixel array of the display panel and which are responsible for sampling the data of the video signal and applying the samples, in the form of data voltage signals, to the appropriate pixels of the array on a row by row basis. The row and column driver circuits, which usually comprise a shift register circuits with the latter also including a sample and hold circuit, can be provided in the form of ICs mounted on the LC display panel or possibly, if the nature of the technology used in the pixel array permits, as in the case for example of polysilicon TFT devices being used as pixel switches, fully integrated on the panel and fabricated simultaneously with the pixel array using the same thin film electronics technology.

An example of the above-described kind of active matrix liquid crystal display device and its general manner of operation is described in US-A-5,130,829 to which reference is invited for further information.

Normally the video signal processing and the timing and control circuitry is implemented in the form of one or more silicon integrated circuits (ICs) with the processing being performed digitally.

The signal processing functions performed on the applied video signal by the video signal processing and control circuitry can be various.

The present invention is concerned particularly, although not exclusively, with video signal processing for avoiding or reducing unwanted artefacts in the displayed picture due to behavioural effects of the pixels and also for gamma correction and colour temperature correction.

For gamma, colour and kickback corrections, then Look Up Tables (LUTs) can be used to provide correctional values. For the latter correction, data signal sign information usually also would be required. In AMLCDs, the data voltage signals applied to the pixels have to be periodically inverted to prevent any net DC voltage across the LC material, the inversion being for example for every successive frame (so-called field inversion) or, in addition, for every successive row of pixels (so-called line or row inversion), for adjacent columns of pixels (so-called column inversion) or such that adjacent pixels in both the row and column direction are of opposite polarity (so-called pixel inversion), according to the particular inversion drive scheme employed.

In order to reduce the extent of perceived blurring in the display picture when displaying moving images, which results from the inherent behaviour of the pixels, and particularly the slow response characteristics of the LC material to pixel voltage changes, then preferably the video data processing includes correction for achieving motion blur reduction, a preferred example of such being described in US-A-5495265 (PHN 13505), which requires for this purpose data signal information from one field to the next, and thus a field store for storing at least the data signal values for one field, as well as a LUT.

It is an object of the present invention to provide for use with a matrix display device an improved controller circuit for performing certain video signal processing operations.

It is another object of the present invention to provide a matrix display device controller circuit for performing certain video signal processing functions which can be produced as an IC at lower cost.

According to the present invention, there is provided a controller circuit for processing video data for a colour active matrix liquid crystal display device and having an input for video data processing circuitry for processing the video data and an output from which the processed video data is provided for supply to a driver circuit of the display device, wherein the processing circuitry comprises gamma and colour correction circuits which include a Look-Up Table, and a motion blur reduction circuit for modifying the video data so as to reduce perceived blurring in moving images displayed on the display device and comprising a field store for video data and a Look-Up Table, and wherein the motion blur reduction circuit precedes the gamma and colour correction circuits.

The invention provides a controller circuit for use in the driving of an active matrix LC display device and implementable in IC form which performs certain video signal processing functions to improve the quality of the picture produced by the display device and in which the circuits for performing the video signal processing functions are arranged and organised in the circuit in a manner which makes more efficient use of the semiconductor material whereby the area of semiconductor material required, and hence cost of the IC, is reduced.

The video signal processing functions performed comprise gamma correction, colour correction (to achieve white of a desired colour temperature), and motion blur reduction (to reduce blurring caused by the behaviour of the pixel, particularly the slow response to the LC material to pixel voltage change,) when displaying moving images. Preferably, the controller circuit further includes a kickback correction circuit which also follows the motion blur reduction circuit.

Having regard to the nature of these different corrections, it would be thought in principle appropriate for the gamma and colour corrections, and the kickback correction if present, to be carried out first and the motion blur correction to be carried out last as the former corrections are made to the video data in order to get the correct voltages on the pixels in the static case and the motion blur reduction is then supposed to ensure that those same

voltages appear on the pixels despite the temporal response behaviour of the pixel. However, the motion blur reduction processing of the video data signals is, in accordance with the invention, arranged instead to be carried out before the gamma, colour and optional kickback corrections. This leads to less complexity and allows the field store required for the motion blur reduction to be narrower, (fewer bits for each data value) than is the case when motion blur reduction processing is performed last, which arrangement necessitates separate correction of the positive and negative drive ranges. Moreover, the size of the associated LUT will be smaller. Substantial benefits are then obtained when the circuitry is translated into IC form, particularly in terms of the area of silicon required.

The gamma, colour and optional kickback corrections could all be performed using a single, suitably programmed, Look Up Table (LUT).

However, in a preferred embodiment incorporating kickback correction the gamma and colour corrections are performed together, using a single LUT, after the motion blur reduction processing, and the kickback correction is performed lastly. With this arrangement the size of the necessary LUT for gamma and colour correction can be considerably reduced as the need to take into account the sign of the data signal (the data signal voltages applied to the pixels periodically being inverted according to particular drive scheme employed) is required only for the kickback correction (because this is drive polarity dependent) and gamma and colour corrections can be made on the "unsigned" data value. Although a LUT is still needed for kickback correction this is smaller than the reduction in size enabled for the LUT associated with the gamma and colour combined so that, overall, the combined sizes of the LUTs is reduced.

This size reduction results in further beneficial reduction in the semiconductor area (i.e. silicon) needed for the IC, and consequently a lower cost IC.

Embodiments of active matrix LC display devices and controller circuits used therewith according to the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a schematic circuit diagram of an active matrix LC display device;

Figure 2 illustrates schematically a motion blur reduction circuit;

Figure 3 illustrates schematically an example controller IC comprising video data signal processing circuit incorporating certain signal processing functions; and

Figure 4 and 5 illustrate first and second embodiments of a controller IC incorporating certain signal processing functions in accordance with the present invention and used in the display device of Figure 1.

The same reference numbers or signs are used throughout the figures to denote the same parts or signals.

Referring to Figure 1, the active matrix LC display device shown is of generally convention form, for example as described in US-A-5 130 829 to which reference is invited for further details as to its construction and general manner of operation, and whose contents in these respects are incorporated herein by reference. Briefly, the display device, which is suitable for displaying colour video pictures, comprises a liquid crystal display panel 10 having a row and column array of pixels 12 which consists of m rows (1 to m) with n horizontally arranged pixels (1 to n) in each row. Only a few of the pixels are shown for simplicity.

Each pixel 12 is associated with a respective switching device in the form of a thin film transistor, TFT, 11. The gate terminals of all TFTs 11 associated with pixels in the same row are connected to a common row conductor 14 to which, in operation, selection (gating) signals are supplied. Likewise, the source terminals associated with all picture elements in the same column are connected to a common column conductor 16 to which data (video) signals are applied. The drain terminals of the TFTs are each connected to a respective transparent pixel electrode 20 forming part of, and

defining, the pixel's display element. The conductors 14 and 16, TFTs 11 and electrodes 20 are carried on one transparent plate while a second, spaced, transparent plate carries an electrode common to all pixels. Liquid crystal material is disposed between the plates.

The display panel is operated in conventional manner. Light from a light source disposed on one side enters the panel and is modulated according to the individual transmission characteristics of the pixels 12. The device is driven on a row at a time basis by scanning the row conductors 14 sequentially with a gating (selection) signal so as to turn on each row of TFTs in turn and applying data (video) signals to the column conductors for each row of pixels in turn as appropriate and in synchronism with the gating signals so as to build up a complete display picture in one field. Using one row at time addressing, all TFTs 11 of the addressed row are switched on for a period determined by the duration of the gating signal, corresponding to a video line time or less, during which the video information signals are transferred from the column conductors 16 to the pixels 12. Upon termination of the gating signal, the TFTs 11 of the row are turned off for the remainder of the field time thereby isolating the pixels from the conductors 16 and ensuring the applied charge is stored on the pixels until the next time they are addressed, usually in the next field period.

All the pixels are addressed in a respective field (i.e frame) period and are repeatedly addressed in successive field periods in accordance with the video data signal information of successive fields of an applied video signal.

The row conductors 14 are supplied successively with gating signals by a row driver circuit 20 comprising a digital shift register controlled by regular timing pulses from a timing and control circuit 21. In the intervals between gating signals, the row conductors 14 are supplied with a substantially constant reference potential by the drive circuit 20. Video data signals are supplied to the column conductors 16 from a column (source) driver circuit 22, comprising one or more shift register/sample and hold circuits. The circuit 22 is supplied with video data signals from an output of a controller IC 24 comprising a digital video data signal processing circuit and timing pulses from

the circuit 21 in synchronism with row scanning to provide serial to parallel conversion appropriate to the row at a time addressing of the panel 10. The circuits 20 and 22 used here are of conventional kind. According to known practice, a graphics standard converter may be arranged between the circuits 23 and 24, for converting an applied video signal to a required standard appropriate to the display device, for example from XGA to SXGA.

The timing and control circuit 21 is supplied with timing signals extracted from an applied digital video signal VS by means of a separation circuit 23 while the data signals, in digital form, from the video signal are supplied by the separation circuit to an input of the video data signal processing circuit 24.

In accordance with standard practice, the sign (polarity) of the data signal voltage applied to the pixel is periodically inverted with respect to the common electrode, at least for every successive field, and possibly also in accordance with a line, column, or pixel inversion drive scheme if employed.

Depending on the technology used to fabricate the pixel array, the row and column drive circuits 20 and 22 may be provided in the form of semiconductor (silicon) ICs mounted on one substrate of the panel and connected directly with the row and column conductors or, in the case for example of the TFTs comprising polysilicon rather than amorphous silicon TFTs, fully integrated with the pixel array and similarly comprising polysilicon TFT circuitry on the substrate fabricated simultaneously with the pixel array.

The input video signal VS, for example from a PC or other video source, comprises 8 bit digital colour (R, G and B) data signals and synchronisation signals. The controller IC 24 modifies digitally the R, G and B signals, as will be described, and the modified digital data signals output from the controller IC are subsequently converted to analogue voltage signals useable by the pixels before being supplied to the pixels. To this end, a D/A converter circuit may be incorporated in the column driver circuit 22 or connected between the controller IC 24 and that circuit.

The data signal processing functions performed by the circuit 24 comprise gamma and colour correction, kickback correction and motion blur reduction.

With regard to the colour and gamma correction, then to achieve a good colorimetric performance from the LC display the transfer characteristic (i.e. brightness versus drive) is usually transformed to be similar to that of a CRT. That is, the luminance is varied with data input signal value according to a power function with a typical gamma of 2.2. The relative gains of the R, G and B signals are modified so as to achieve a white of the desired colour temperature. Also the relative R, G and B transfer characteristics are modified to correct for the change of colour point with drive level that is typical of an LCD. All the above are achieved by using LUTs to modify the R, G and B data signal values to be supplied to the pixels. Suitable circuits for gamma and colour correction will be known to skilled persons and as such it is considered unnecessary to describe examples here in detail.

Motion blur reduction involves processing to reduce unwanted display effects which can result when moving images are displayed. When displaying a moving image on a conventional AMLCD the image becomes blurred and are particular reason for this is the slow response of the LC material of a pixel, and hence the transmission through the device, to a change in applied pixel voltage. It is known that the blurring effect can be reduced by overdriving temporal transitions in the R, G and B signals such that the desired transmission can be achieved within a single field (frame) period. The data required for deciding how much overdrive to use for a given transition can be acquired by appropriate experimentation. Examples of motion blur reduction processing are described in EP-A-5495265 and WO99/05567 to which reference is invited, and whose contents are incorporated herein as reference material.

Figure 2 shows schematically the operation of such blur reduction signal processing. A field store 30 is required to enable evaluation of the pixel voltage transition from the previous to the current field. The data signals, D, for a current field fed to an input 31 are supplied to an LUT 32 and also to the

field store 30 and the data signals for the previous field are at the same time output from the field store to the LUT 32. Thus an indication of the voltage transitions of the individual pixels is available. The LUT is appropriately preprogrammed and the amount of overdrive to be used for a given transition stored in the LUT is used to modify the data signals through an adder circuit 33 with the suitably modified data signals being output at 34. Successive fields of data signals are fed serially to the input and successive fields with appropriately modified data signals are supplied at the output.

Kickback correction is intended to overcome the phenomenon, known as kickback, due to the trailing edge of a row selection (gating) pulse applied to the row conductors 14 feeding through the TFT gate to drain capacitance, Cgd, and affecting the voltage set on a pixel. The size of this effect, that is, the voltage error caused, is dependent on the relative magnitudes of Cgd and the pixel capacitance. (The pixel capacitance will consist of the LC (display element) capacitance and also any fixed storage capacitor connected in parallel although the latter is not shown in Figure 1).

The LC capacitance varies according to the applied pixel voltage and so the magnitude of the kickback voltage depends on the voltage of the pixel. The kickback also depends on the polarity of the pixel voltage. The TFT 11 remains conducting for a greater part of the gate selection voltage drop during the negative cycle than during the positive cycle. As a result, there is more TFT channel charge contributing to the kickback during the negative than the positive cycle. If the same DC voltage correction is applied in both cycles, then because the kickback in the negative cycle is greater, the magnitude of the final pixel voltage of both cycles will be greater than the magnitude of the applied source voltage. This can be taken into account when considering the transfer characteristic.

It is conventional to compensate for the "average" value of kickback i.e. that suffered by a mid-grey pixel, by adjusting the common electrode voltage. The remaining error for pixels that are "blacker" or "whiter" than this can be compensated by adjusting the column driver circuit voltage accordingly. This adjustment can be stored in a Look-Up Table whose input is the value of the

pixel voltage. For a still picture this is the current field pixel voltage. For a moving picture this should be from the previous field. One important point to note is that although the column driver circuit output data signal alternates in polarity at field rate for any given pixel, the polarity of the kickback effect, and hence that of the kickback correction, is always the same. This has consequences for the signal processing architecture as will be seen below.

In principle, it would be expected that the gamma, colour and kickback corrections should be done first and the motion blur correction last. This is because the former corrections are being made to get the correct voltage on the pixel in a static case, and the motion blur reduction is then supposed to be ensuring that that same, corrected, voltage ends up on the pixel despite the temporal response of the display. Figure 3 is a schematic diagram depicting the ordering of the processing functions in an example controller IC 24 which follows normal expectations in this respect. In this figure, block 35 represents the combined gamma, colour and kickback correction circuitry and the block 36 represents the motion blur reduction processing circuitry, including the field store 30. The field store component 30 here is provided as a separate IC, although it could instead be incorporated in the IC 24, as signified at 30'. The gamma, colour and kickback corrections could be carried out by a single LUT as indicated in Figure 3. The input to this LUT is the 8-bit data value for one of the (R, G, B) data signals plus a single bit signal, at 37, indicating whether positive or negative polarity drive is to be used for that pixel. This signing signal is generated by logic elsewhere in the controller IC and depends on the particular inversion scheme being used. The output from this circuitry, comprising 11-bit data signals, are supplied to the processing circuitry 36 which, in turn, outputs processed, 11-bit, data signals, denoted at D'.

Figure 4 illustrates a first embodiment of a controller IC 24 according to the present invention. The same reference numbers are used to denote the same processing circuitry parts and functions. As can be seen in Figure 4, then the processing functions are re-ordered such that the motion blur reduction processing is performed first. Again, the field store of the motion blur reduction processing circuit 36 may be provided separately as shown at 30 or

within the IC 24, as shown at 30'. The output from the motion blur correction is increased to 9 bits, from 8-bits, for a data signal as it must cover a larger voltage range than just black-to-white to allow for some "overdrive". The motion blur reduction LUT can be modified to take approximate account of the later effects of the colour and gamma correction, so this will not lead to much error. A potential problem comes with the Kickback correction, which cannot be allowed for in the motion blur LUT, as there is no polarity information at that stage. The order of magnitude of the Kickback correction may be ~± 0.25 volts so the motion blur reduction calculations will be made on signals which might be ~± 0.25 volts different to those that should actually be applied to the pixels. However, in order to minimise the size of the field store, the minimum possible number of bits is used. It has been determined that a useful reduction in motion blur can be achieved by storing only the top 3 bits of the data signal in the field store. In this case, the motion blur correction only affects the top 3 bits of the drive voltage which means that it is accurate only to about 0.5 volts (taking black to white as 4 volts). So for this level of accuracy in motion blur correction, the order of processing indicated in Figure 4 can be acceptable. For static images, of course, there is no problem.

Assuming there are 1024 pixels in a row, the size of the gamma, colour and kickback LUT in Figure 4 is 1024 x 11 = 11 Kbits. This size can be reduced to 512 x 10 = 5 Kbits if the colour and gamma corrections are carried out on the unsigned drive signal and kickback correction (which is drive polarity dependent) is added afterwards. This is illustrated in Figure 5 which is schematic representation of the processing functions in the controller IC 24 in a second embodiment according to the present invention with the kickback correction circuit, here shown at 39, separated from, and following, the gamma and colour correction circuits 35. The size of the additional LUT required by the Kickback correction is very much smaller than 5 Kbits, so a net overall reduction in semiconductor silicon area needed by the IC is achieved. The sign bit is input to the kickback correction to indicate whether the correction is to be added or subtracted.

The architecture of the IC illustrated in Figure 5 thus enables the IC to be fabricated at lower cost.

In this controller IC the level dependent kickback correction will not be wholly correct for the changing parts of the displayed picture. This is because the kickback voltage depends on the pixel capacitance before the new signal is applied (i.e. the pixel value from the previous field) and the kickback correction in Figure 5 is being calculated using the current pixel value. It is estimated that in the worse case (a black to white transition) this may lead to an incorrect pixel drive voltage of the order of half a volt. It should be noted that this is quite normal with "conventional" kickback correction schemes also. The effect only applies to the edges of moving objects and will probably be difficult to observe, in normal use of the display device. A further improvement, therefore, would be to use the signal from the field store to evaluate kickback correction for moving parts of the picture.

Although the timing and control circuit 21 is shown separately in Figure 1, this circuit can be combined with the processing circuit 24 in the same IC.

In summary, therefore, there has been described a controller circuit for processing video data for an active matrix liquid crystal display device which has processing circuitry for performing correction functions on the input video data prior to being supplied to the drive circuit of the display device comprising gamma and colour correction, and correction for reducing motion blur in the display picture. The correction circuits are organised such that correction for motion blur reduction is carried out before the gamma and colour corrections, which enables a beneficial decrease in semiconductor area required when implementing the circuitry in IC form through the size of field store and LUT components used for this function then being smaller. Gamma and colour corrections are performed together using a single LUT. Correction for kickback may further be included, such correction preferably being arranged after the gamma and colour corrections and using a separate LUT.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the field of active matrix display devices

and controller circuits therefor and which may be used instead of or in addition to features already described herein.

CLAIMS

1. A controller circuit for processing video data for a colour active matrix liquid crystal display device and having an input for video data, processing circuitry for processing the video data and an output from which the processed video data is provided for supply to a driver circuit of the display device, wherein the processing circuitry comprises gamma and colour correction circuits which include a Look-Up Table, and a motion blur reduction circuit for modifying the video data so as to reduce perceived blurring in moving images displayed on the display device and comprising a field store for video data and a Look-Up Table, and wherein the motion blur reduction circuit precedes the gamma and colour correction circuits.

2. A controller circuit according to Claim 1, wherein the controller circuit further includes a kickback correction circuit for modifying the video data so as to correct for kickback effects in the display device pixels and which is arranged following the motion blur reduction circuit.

3. A controller circuit according to Claim 2, wherein the kickback correction circuit follows also the gamma and colour correction circuits.

4. A controller circuit according to any one of the preceding claims, wherein the controller circuit is in the form of one or more integrated circuits.

5. An active matrix liquid crystal display system comprising an active matrix liquid crystal display device and a controller circuit according to any one of claims 1 to 4, and in which the output of the controller circuit is connected to a drive circuit of the display device.

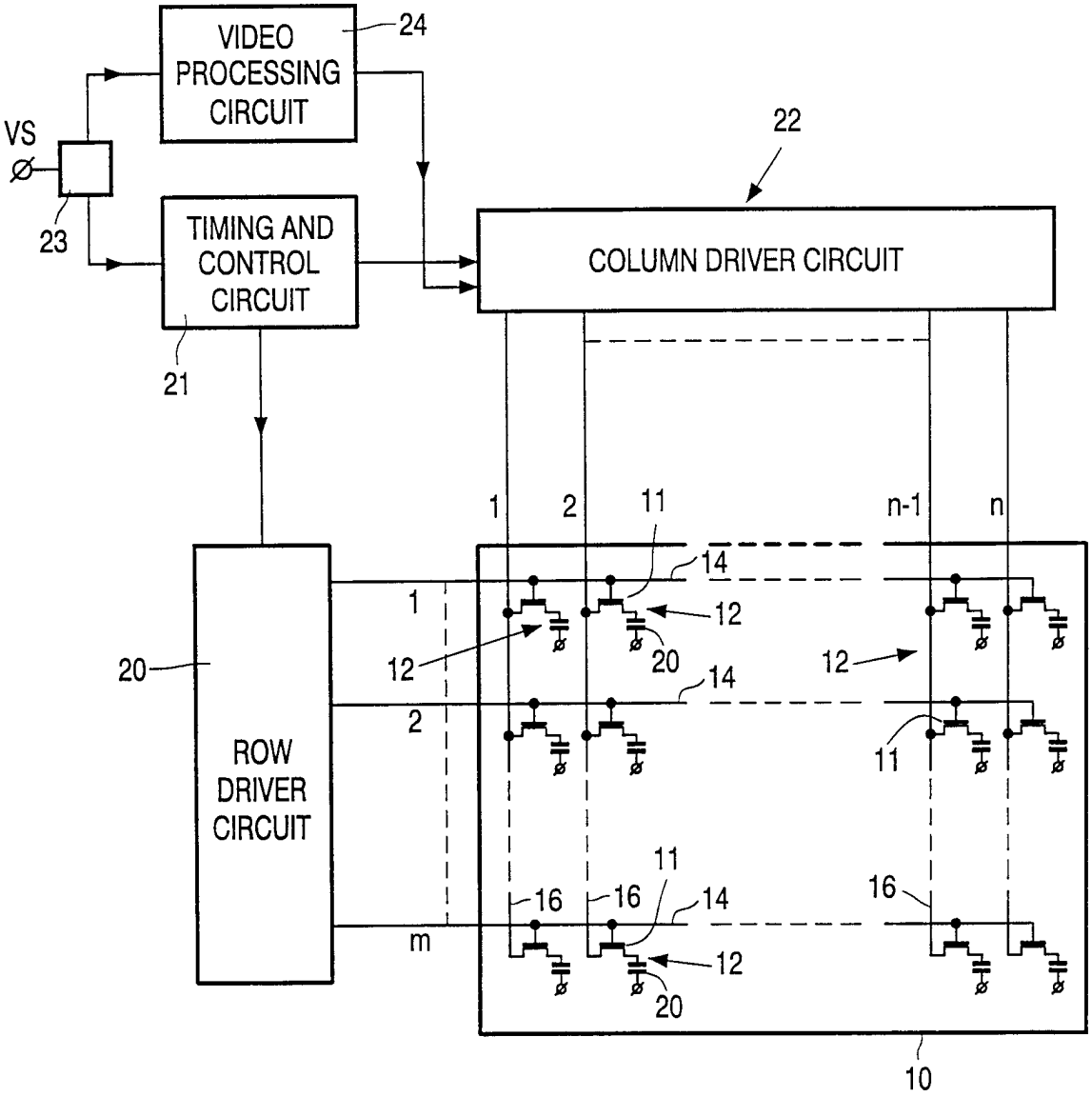

VIDEO PROCESSING CIRCUIT
24
VS
23
TIMING AND CONTROL CIRCUIT
21
22
COLUMN DRIVER CIRCUIT
ROW DRIVER CIRCUIT
20
1
2
m
n-1
n
11
12
14
16
10

FIG. 1

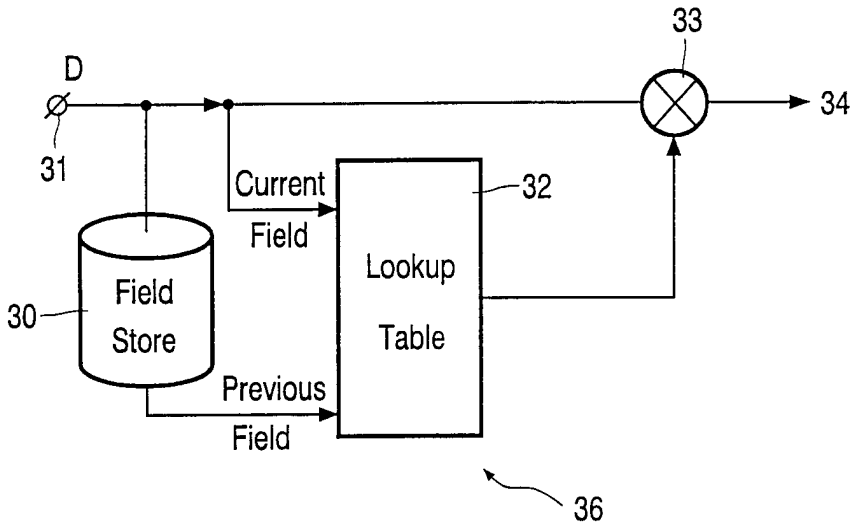

33
D
34
31
Current
Field
32
Lookup
Table
Field
Store
30
Previous
Field
36

FIG. 2

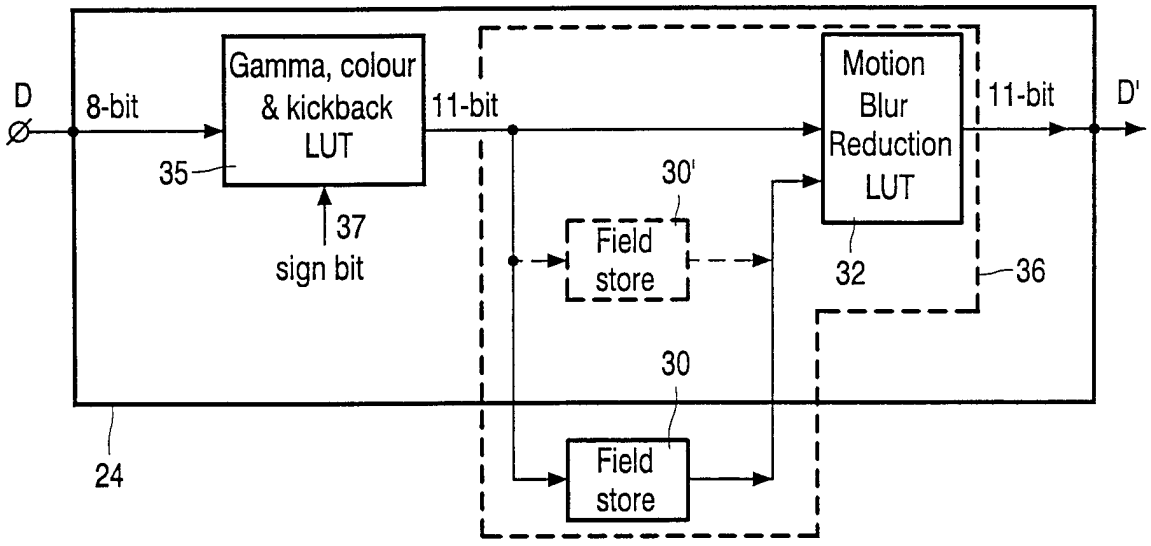

D
8-bit
Gamma, colour
& kickback
LUT
11-bit
Motion
Blur
Reduction
LUT
11-bit
D'
35
37
sign bit
30'
Field
store
32
36
30
Field
store
24

FIG. 3

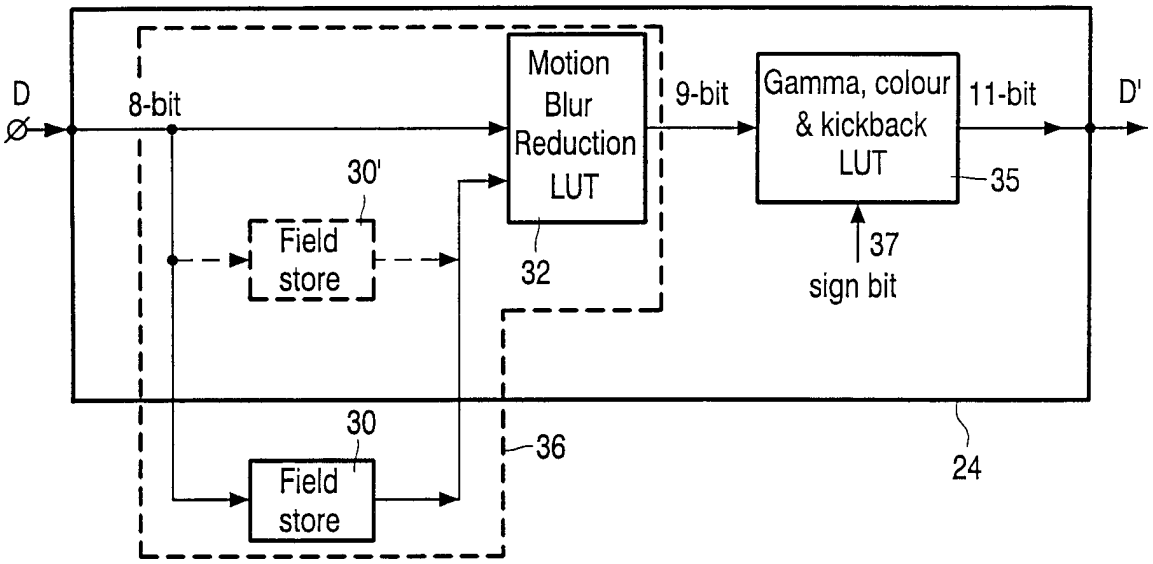

D
8-bit
Motion Blur Reduction LUT
9-bit
Gamma, colour & kickback LUT
11-bit
D'
30'
Field store
32
35
37
sign bit
30
Field store
36
24

FIG. 4

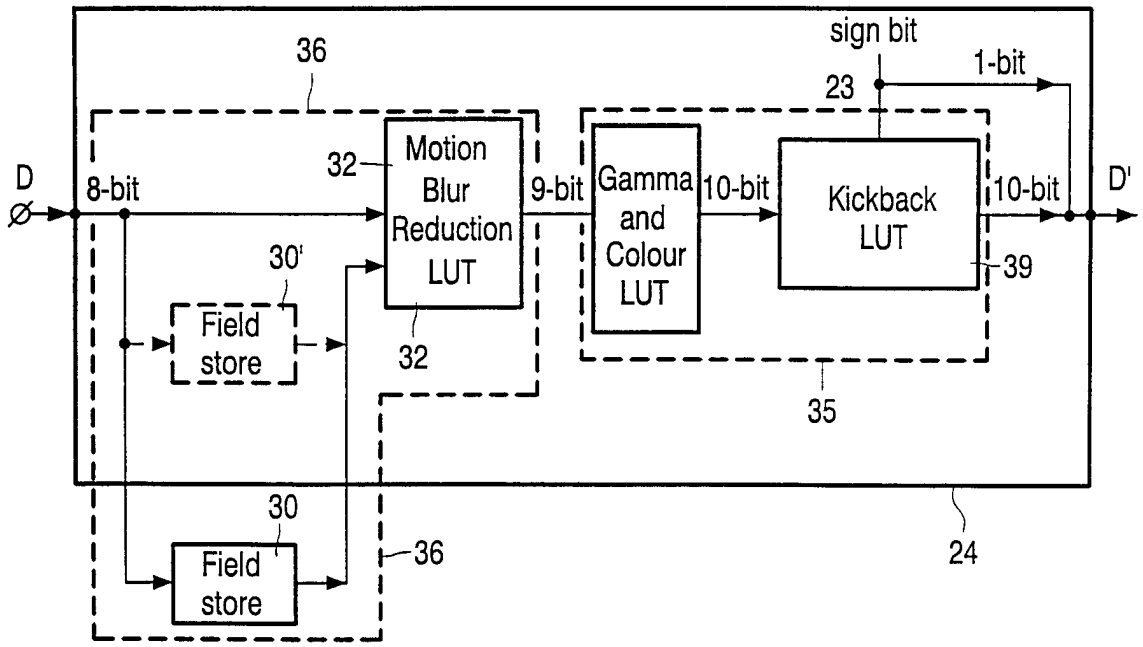

36
sign bit
1-bit
23
D
8-bit
32
Motion Blur Reduction LUT
9-bit
Gamma and Colour LUT
10-bit
Kickback LUT
10-bit
D'
30'
Field store
32
39
35
30
Field store
36
24

FIG. 5

INTERNATIONAL SEARCH REPORT

Int ational Application No
PCT/EP 01/02819

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 495 265 A (KNAPP ALAN G ET AL) 27 February 1996 (1996-02-27) cited in the application column 3, line 54 -column 6, line 42	1,2
A	EP 0 951 007 A (BARCO NV) 20 October 1999 (1999-10-20) paragraphs '0044!,'0045!,'0057!-'0062!,'0075!-'0078!	1,5
A	US 5 528 257 A (SUZUKI KOUHEI ET AL) 18 June 1996 (1996-06-18) column 5, line 52 -column 6, line 64	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 July 2001	23/07/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Amian, D

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ational Application No
PCT/EP 01/02819

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5495265 A	27-02-1996	NL 9002516 A	16-06-1992
		DE 69127172 D	11-09-1997
		DE 69127172 T	12-02-1998
		EP 0487137 A	27-05-1992
		EP 0768637 A	16-04-1997
		JP 4268599 A	24-09-1992
		KR 230513 B	15-11-1999
EP 0951007 A	20-10-1999	DE 69800055 D	27-01-2000
		DE 69800055 T	03-08-2000
		WO 9954865 A	28-10-1999
		ES 2143883 T	16-05-2000
		NO 20004555 A	16-11-2000
US 5528257 A	18-06-1996	JP 7020828 A	24-01-1995

专利名称(译)	用于液晶矩阵显示装置的控制器电路		
公开(公告)号	EP1190411A1	公开(公告)日	2002-03-27
申请号	EP2001936071	申请日	2001-03-13
[标]申请(专利权)人(译)	皇家飞利浦电子股份有限公司		
申请(专利权)人(译)	皇家飞利浦电子N.V.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	HUGHES JOHN R PARKER DAVID W		
发明人	HUGHES, JOHN, R. PARKER, DAVID, W.		
IPC分类号	G02F1/133 G09G3/20 G09G3/36 G09G5/06 H04N5/66 H04N9/30		
CPC分类号	G09G3/3611 G09G3/3614 G09G3/3648 G09G5/06 G09G2320/0219 G09G2320/0252 G09G2320/0261 G09G2320/0276 G09G2340/16		
优先权	2000006811 2000-03-22 GB		
外部链接	Espacenet		

摘要(译)

用于处理有源矩阵液晶显示装置的视频数据的控制器电路（24）具有处理电路，用于在输入到包括伽马的显示装置的驱动电路（22）之前对输入视频数据（D）执行校正功能。和颜色校正，以及用于减少显示图像中的运动模糊的校正。校正电路（35,36）被组织成使得在伽玛和颜色校正（35）之前执行用于减少运动模糊的校正（36），这使得在实现IC形式的电路时所需的半导体区域的有益减少成为可能。用于此功能的字段存储（30）和LUT（32）组件的大小则更小。使用单个LUT一起执行伽马和颜色校正。可以进一步包括对反冲的校正，这种校正优选地在伽马和颜色校正之后并且使用单独的LUT来安排。