(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 3 029 662 A1

(12) EUROPEAN PATENT APPLICATION
published in accordance with Art. 153(4) EPC

(43) Date of publication:
08.06.2016 Bulletin 2016/23

(21) Application number: **13866488.3**

(22) Date of filing: **18.10.2013**

(51) Int Cl.:
G09G 3/36 *(2006.01)*

(86) International application number:
PCT/CN2013/085521

(87) International publication number:
WO 2015/014026 (05.02.2015 Gazette 2015/05)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(30) Priority: **31.07.2013 CN 201310329312**

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(54) SHIFT REGISTER UNIT AND DRIVE METHOD THEREOF, GATE DRIVE CIRCUIT AND DISPLAY DEVICE

(57) There is provided a shift register unit and driving method thereof, a gate driving circuit and display device. By setting the voltage stabilizing capacitor (C) connected to the pull-up node (P), the shift register unit utilizes the voltage stabilizing capacitor (C2) to stabilize the potential at the pull-up node (P), so as to make the signal output from the shift register unit more stable; and at the same time, uses a very small quantity of transistors and capacitors to compose the shift register unit, so that the wiring area of the gate driving circuit is greatly reduced to provide a technical support for the design of a liquid crystal display device with a narrower frame. In the meantime, since the structure of the gate driving circuit is simplified, the manufacturing process of the gate driving circuit is simplified and the cost for manufacturing is reduced. Further, the shift register unit quickly and effectively pulls down the output signal to the low potential through two pull-down processes, thereby enhancing the pull-down capability of the gate driving circuit.

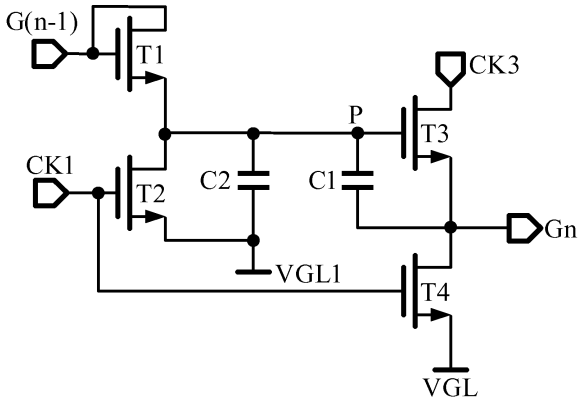

Fig.7

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Description

TECHNICAL FIELD

[0001] The present disclosure relates to the field of display technique, in particular to a shift register unit, a gate driving circuit for applying the shift register unit, a driving method for driving the shift register unit and a display device for applying the gate driving circuit.

BACKGROUND

[0002] A thin film transistor liquid crystal display TFT-LCD is widely applied to electronic products such as a TV, a mobile phone, a display and so on due to its advantages of stable picture, vivid image, eliminating radiation, saving space and power consumption and so on, and has occupied a dominant position in the field of panel display .

[0003] A liquid crystal display panel is composed of matrix of pixels in horizontal and vertical directions. When the liquid crystal display panel displays, a gate scanning signal is output through a gate driving circuit to progressively scan respective pixels. Drivers of the liquid crystal display panel mainly include a gate driver and a data driver. The data driver latches an input display data and clock signal at regular time and in sequence, and converts them into an analogy signal to be inputted to a data line of the liquid crystal display panel. The gate driver converts the input clock signal through the shift register, switches it into an on/off voltage, and in sequence applies the voltage to a scanning gate line of the liquid crystal panel to gate the pixels, that is, the shift register in the gate driver is used for producing a scanning signal in the scanning gate line.

[0004] With the development of the panel display technique, narrow-framed products have attracted more and more attention. However, the shift register in the prior art generally uses a large quantity of transistors and other electrical elements, and it not only has a complex structure, but also occupies a large wiring area, which is disadvantageous for a narrow-framed design, and at the same time adds difficulty in manufacturing process of the shift register, thereby increasing the cost for manufacturing. Moreover, the size of the transistor generally cannot be too large because the transistor is always subjected to the limitation of the wiring space. In this way, there may be a problem of failing to quickly and effectively pull down the output signal to a low potential because of a too small size of a pull-down transistor. At the same time, in the shift register unit of the prior art, since a control signal for a pull-up transistor is directly inputted to the pull-up transistor, a switch control over the pull-up transistor may be affected, thereby causing the output signal of the shift register unit unstable.

SUMMARY

[0005] The technical problem to be solved in the present disclosure is, in view of the existing technology deficiencies, to provide a shift register unit having a more stable output signal, a gate driving circuit for applying the shift register unit, a driving method for driving the shift register unit and a display device for applying the gate driving circuit, which uses a very small quantity of transistors, so that the wiring area of the gate driving circuit is greatly reduced, so as to provide a technical support for the design of the a liquid crystal display device with a narrower frame and further enhance the pull-down capability of the whole shift register unit, thereby increasing the response speed of the liquid crystal display device.

[0006] The present disclosure has the following technical solutions.

[0007] A shift register unit comprises:

a pull-up module connected to a first clock signal input terminal, a signal output terminal and a pull-up node respectively for outputting a signal inputted from the first clock signal input terminal to the signal output terminal according to a potential at the pull-up node, the pull-up node being a connecting point between the pull-up module and a pull-up driving module;

a pull-down module connected to the signal output terminal, a first signal terminal and a second clock signal input terminal respectively for pulling down a potential at the signal output terminal to the first signal terminal according to a signal output from the second clock signal input terminal;

the pull-up driving module connected to a signal input terminal and the pull-up node respectively for driving the pull-up module according to a signal inputted from the signal input terminal;

a reset module connected to a second signal terminal, a reset signal terminal and the pull-up node respectively for resetting a signal at the pull-up node according to a signal inputted from the reset signal terminal;

a voltage stabilizing module connected to the pull-up node for stabilizing the potential at the pull-up node.

[0008] Alternatively, the reset signal terminal is connected to the second clock signal input terminal.

[0009] Alternatively, the second signal terminal and the first signal terminal are at a low level; and the potential at the second signal terminal is lower than the potential at the first signal terminal.

[0010] Alternatively, the pull-up driving module comprises a pull-up driving transistor, the reset module comprises a reset transistor, the pull-up module comprises a pull-up transistor and a bootstrap capacitor, the pull-down module comprises a pull- down transistor, and the voltage stabilizing module comprises a voltage stabiliz-

ing capacitor;
the pull-up driving transistor has a gate and a drain connected to the signal input terminal, and a source connected to a drain of the reset transistor, a first terminal of the voltage stabilizing capacitor, a first terminal of the bootstrap capacitor and a gate of the pull-up transistor respectively;
the reset transistor has a gate connected to the reset signal terminal ,and a source connected to a second terminal of the voltage stabilizing capacitor and the second signal terminal respectively;
the pull-up transistor has a drain connected to the first clock signal input terminal, and a source connected to the signal output terminal, a second terminal of the bootstrap capacitor and a drain of the pull-down transistor respectively;
the pull-down transistor has a gate connected to the second clock signal input terminal and a source connected to the first signal terminal.

[0011] Alternatively, all the transistors are N-channel type transistors or all the transistors are P-channel type transistors.

[0012] According to another aspect of the present disclosure, there is further provided a driving method for driving the above shift register unit:

a driving method for driving a shift register unit comprises the following steps:
in a charging stage, inputting a previous stage of output signal or a start signal from a signal input terminal to turn on a pull-up driving transistor and a pull-up transistor, inputting a clock signal from a reset signal terminal to turn off a reset transistor, and charging a voltage stabilizing capacitor and a bootstrap capacitor by the previous stage of output signal or the start signal;
in an outputting stage, ending signal input at the signal input terminal to turn off the pull-up driving transistor, and inputting a clock signal from a second clock signal input terminal to turn off the pull-down transistor; continuously turning on the pull-up transistor, raising a potential at a pull-up node by the bootstrap capacitor through a clock signal inputted from a first clock signal input terminal, maintaining the potential at the pull-up node by the voltage stabilizing capacitor, and outputting the clock signal inputted from the first clock signal input terminal to a signal output terminal by the pull-up transistor;
in a resetting stage, inputting a clock signal from the reset signal terminal to control the reset transistor and the pull-down transistor to be turned on, pulling down the potential at the pull-up node by the reset transistor to turn off the pull-up transistor, and pulling down a potential at a signal output terminal by the pull-down transistor.

[0013] Alternatively, the reset signal input terminal is connected to the second clock signal input terminal.

[0014] According to another aspect of the present disclosure, there is further provided a gate driving circuit comprising any one of the above shift register units:

a gate driving circuit comprising any one of the above shift register units; except a last stage of shift register unit, a signal output terminal of each of other shift register units is connected to a signal input terminal of a next stage of shift register unit, and a signal input terminal of a first stage of shift register unit is connected to a start signal.

[0015] According to another aspect of the present invention, there is further provided a display device comprising the above gate driving circuit.

[0016] By setting the voltage stabilizing capacitor connected to the pull-up node, the shift register unit provided in the embodiments of the present disclosure utilizes the voltage stabilizing capacitor to stabilize the potential at the pull-up node, so as to make the signal output from the shift register unit more stable; at the same time, the present disclosure uses a very small quantity of transistors and capacitors to compose the shift register unit, so that the wiring area of the gate driving circuit is greatly reduced, so as to provide a technical support for the design of a liquid crystal display device with a narrower frame. In the meantime, since the structure of the gate driving circuit is simplified, the manufacturing process of the gate driving circuit is simplified and the cost for manufacturing is reduced. Further, the shift register unit provided in the present disclosure quickly and effectively pulls down the output signal to the low potential through two pull-down processes, thereby enhancing the pull-down capability of the gate driving circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]

Fig.1 is a schematic diagram of a module connection of a shift register unit in a first embodiment of the present disclosure;
Fig.2 is a circuit diagram of an implementation of a shift register unit in a first embodiment of the present disclosure;
Fig.3 is a circuit diagram of another implementation of a shift register unit in a first embodiment of the present disclosure;
Fig.4 is a schematic diagram of a structure of a gate driving circuit in a first embodiment of the present disclosure;
Fig.5 is a schematic diagram of driving timing and signal waveform of the shift register unit in Fig.2;
Fig.6 is a schematic diagram of a module connection of a shift register unit in a second embodiment of the present disclosure;
Fig.7 is a circuit diagram of an implementation of a shift register unit in a second embodiment of the

present disclosure;

Fig.8 is a circuit diagram of another implementation of a shift register unit in a second embodiment of the present disclosure;

Fig.9 is a schematic diagram of a structure of a gate driving circuit in a second embodiment of the present disclosure;

Fig.10 is a schematic diagram of driving timing and signal waveform of the shift register unit in Fig.7;

DETAILED DESCRIPTION

[0018] Specific implementations of the present disclosure will be further described below in combination with the accompanying figures and embodiments. The following embodiments are just used for specifying the present disclosure rather than being used to limit the scope of the disclosure.

First Embodiment

[0019] As shown in Fig.1, a shift register unit provided in the present embodiment mainly comprises: a pull-up module connected to a first clock signal input terminal, a signal output terminal and a pull-up node P respectively for outputting a signal inputted from the first clock signal input terminal to the signal output terminal according to a potential at the pull-up node P; a pull-down module connected to the signal output terminal, a first signal terminal and a second clock signal input terminal respectively for pulling down a potential at the signal output terminal according to a signal output from the second clock signal input terminal; a pull-up driving module connected to a signal input terminal and the pull-up node P respectively for driving the pull-up module according to a signal inputted from the signal input terminal; a reset module connected to a second signal terminal, a reset signal terminal and the pull-up node P respectively for resetting a signal at the pull-up node P according to a signal inputted from the reset signal terminal; a voltage stabilizing module connected to the pull-up node P for stabilizing the potential at the pull-up node P. By setting the voltage stabilizing capacitor connected to the pull-up node P, the shift register unit utilizes the voltage stabilizing capacitor to stabilize the potential at the pull-up node P, so as to make the signal output from the shift register unit more stable.

[0020] The circuit shown in Fig.2 is a specific implementation of the shift register unit provided in the present embodiment. Fig.4 is a gate driving circuit composed of the shift register unit in Fig.2. As shown in Fig.2, the shift register unit in the present embodiment comprises a pull-up driving transistor T1, a reset transistor T2, a pull-up transistor T3, a pull-down transistor T4, a bootstrap capacitor C1 and a voltage stabilizing capacitor C2, and further comprises a signal input terminal, a signal output terminal, a first clock signal input terminal, a second clock signal input terminal, a reset signal terminal, a second signal terminal VGL1 and a first signal terminal VGL. As shown in Fig.4, in the gate driving circuit of the present embodiment, except for the first stage of shift register unit, a signal input terminal of each stage of other shift register units is connected to a signal output terminal of the previous stage of shift register unit; except for the last stage of shift register unit, a signal output terminal of each stage of other shift register units is connected to a signal input terminal of the next stage of shift register unit, and a signal input terminal of the first stage of shift register unit is connected to a start signal STV. In the present embodiment, the pull-up driving transistor T1 has a gate and a drain connected to the signal input terminal, and a source connected to a drain of the reset transistor T2, a first terminal of the voltage stabilizing capacitor C2, a first terminal of the bootstrap capacitor C1 and a gate of the pull-up transistor T3 respectively, when there is inputted the start signal STV or the output signal of previous stage , the pull-up driving transistor T1 is turned on to charge the voltage stabilizing capacitor C2 and the bootstrap capacitor C1; the reset transistor T2 has a gate connected to the reset signal terminal, and a source connected to a second terminal of the voltage stabilizing capacitor C2 and the second signal terminal VGL1 respectively, wherein after the signal output at the signal output terminal is completed, the reset transistor T2 is turned on under the control of the reset signal to reset the shift register unit; the pull-up transistor T3 has a drain connected to the first clock signal input terminal, and a source connected to the signal output terminal, a second terminal of the bootstrap capacitor C1 and a drain of the pull-down transistor T4 respectively, and is used for providing the output signal to the signal output terminal; the pull-down transistor T4 has a gate connected to the second clock signal input terminal, and a source connected to the first signal terminal VGL, and is used for pulling down the output signal at the signal output terminal; the voltage capacitor C2 is used for stabilizing the potential at the pull-up node P (i.e., a gate connecting point of the pull-up transistor T3) after the signal input at the signal input terminal is completed, so as to make the output terminal more stable; the bootstrap capacitor C1 is used for raising the potential at the pull-up node, so that the potential at the pull-up node is higher than the potential at the first clock signal input terminal, so as to make the first clock signal output completely; the second signal terminal VGL1 and the first signal terminal VGL are all at a low level. In the present embodiment, in order to more completely turn off the pull-up transistor T3 and reduce a leakage current of the pull-up transistor T3, the potential at the second signal terminal VGL1 is lower than the potential at the first signal terminal VGL.

[0021] Another advantage of the shift register unit and the gate driving circuit in the present embodiment is adopting a single-channel type of transistor, that is, all the transistors are N-channel type transistors, thereby further reducing the complexity of the manufacturing process and the production cost. Of course, it is easy for

those skilled in the art to obtain that the shift register unit provided in the present disclosure can be easily changed into all the transistors being P-channel type transistors, in particular as shown in Fig.3, which is not limited to the implementations provided in the present embodiment, and will not be described repeatedly herein.

[0022] The present embodiment further provides a driving method for driving the above shift register unit. Referring to the driving timing diagram in Fig.5, all the transistors therein are N-channel type transistors, a clock signal CK1 is taken as a signal output from the reset signal terminal, and a clock signal CK is taken as a signal output from the first clock signal input terminal; a pulse width of the clock signal CK1 is two times of that of the clock signal CK and the start signal STV, and phase difference between the adjacent clock signals is 90 degrees. As such, the gate driving circuit comprising the above shift register unit needs four clock signals CK1~CK4. By adding the clock signal CK and the clock signal CKB, the gate driving circuit totally needs six clock signals. The operating process of the method for driving the shift register unit mainly comprises the following stages:

[0023] in a charging stage t1, the signal input terminal inputs a previous stage of output signal G(n-1) or the start signal STV, the potential at the pull-up node P is raised, the pull-up driving transistor T1 and the pull-up transistor T3 are turned on, the reset signal terminal inputs a low level signal to turn off the reset transistor T2, the second clock signal input terminal inputs a high level signal to turn on the pull-down transistor T4, the previous stage of output signal G(n-1) or the start signal STV charges the voltage stabilizing capacitor C2 and the bootstrap capacitor C1, and a signal output terminal Gn outputs the low level signal.

[0024] in a outputting stage t2, the signal input at the signal input terminal is ended, the pull-up driving transistor T1 is turned off, the second clock signal input terminal outputs the low level signal, and the pull-down transistor T4 is turned off; the first clock signal input terminal outputs the high level signal , the bootstrap capacitor C1 continuously raises the potential at the pull-up node P, the voltage stabilizing capacitor C2 maintains the potential at the pull-up node, and the pull-up transistor T3 completely outputs the high level signal at the first clock input terminal to the signal output terminal Gn;

[0025] in a resetting stage t3, the reset signal terminal outputs the high level signal, the reset transistor T2 and the pull-down transistor T4 are turned on, the second signal terminal VGL1 pulls down the potential at the pull-up node P, the pull-up transistor T3 is turned off, the second clock signal input terminal outputs the high level signal, the pull-down transistor T4 is turned on, and the potential at the signal output terminal Gn is pulled down to the potential at the first signal terminal VGL.

[0026] Since the potential at the second signal terminal VGL1 is lower that the potential at the first signal terminal VGL. As such, when the output signal is pulled down, the voltage at the pull-up node P is pulled down to the potential at the second signal terminal VGL1, and the voltage at the signal output terminal is pulled down to the potential at the first signal terminal VGL. Since VGL1 is smaller than VGL, the gate-source voltage VGS of the pull-up transistor T3 is smaller than 0, so that there will be a more complete turn-off and a smaller leakage current.

[0027] The embodiment of the present disclosure further provides a display device comprising the above gate driving circuit; since the used gate driving circuit has a smaller wiring area, the frame of the display device can be made to be narrower.

Second Embodiment

[0028] As shown in Fig.6, a shift register unit provided in the embodiment 2 mainly comprises: a pull-up module connected to a first clock signal input terminal, a signal output terminal and a pull-up node P respectively for outputting a signal inputted from the first clock signal input terminal to the signal output terminal according to a potential at the pull-up node P; a pull-down module connected to the signal output terminal, a first signal terminal and a second clock signal input terminal respectively for pulling down a potential at the signal output terminal according to a signal output from the second clock signal input terminal; a pull-up driving module connected to a signal input terminal and the pull-up node P respectively for driving the pull-up module according to a signal inputted from the signal input terminal; a reset module connected to a second signal terminal, a second clock signal input terminal and the pull-up node P respectively for resetting a signal at the pull-up node P according to a signal inputted from the second clock signal input terminal; a voltage stabilizing module connected to the pull-up node P for stabilizing the potential at the pull-up node P. By setting the voltage stabilizing capacitor connected to the pull-up node P, the shift register unit utilizes the voltage stabilizing capacitor to stabilize the potential at the pull-up node P, so as to make the signal output from the shift register unit more stable.

[0029] The circuit shown in Fig.7 is a specific implementation of the shift register unit provided in the present embodiment. Fig.9 is a gate driving circuit composed of the shift register unit in Fig.7. As shown in Fig.7, the shift register unit in the present embodiment comprises a pull-up driving transistor T1, a reset transistor T2, a pull-up transistor T3, a pull-down transistor T4, a bootstrap capacitor C1 and a voltage stabilizing capacitor C2, and further comprises a signal input terminal, a signal output terminal, a first clock signal input terminal, a second clock signal input terminal, a second signal terminal VGL1 and a first signal terminal VGL. As shown in Fig.9, in the gate driving circuit of the present embodiment, except for the first stage of shift register unit, a signal input terminal of each stage of other shift register units is connected to a signal output terminal of a previous stage of shift register

unit; except for the last stage of shift register unit, a signal output terminal of each stage of other shift register units is connected to a signal input terminal of the next stage of shift register unit, and a signal input terminal of the first stage of shift register unit is connected to a start signal STV. In the present embodiment, the pull-up driving transistor T1 has a gate and a drain connected to the signal input terminal, and a source connected to a drain of the reset transistor T2, a first terminal of the voltage stabilizing capacitor C2, a first terminal of the bootstrap capacitor C1 and a gate of the pull-up transistor T3 respectively, wherein when there is inputted the start signal STV or the output signal of the previous stage , the pull-up driving transistor T1 is turned on to charge the voltage stabilizing capacitor C2 and the bootstrap capacitor C1; the reset transistor T2 has a gate connected to the second clock signal input terminal, and a source connected to a second terminal of the voltage stabilizing capacitor C2 and the second signal terminal VGL1 respectively, wherein after the signal output at the signal output terminal is completed, the reset transistor T2 is turned on under the control of the second clock signal to reset the shift register unit; the pull-up transistor T3 has a drain connected to the first clock signal input terminal, and a source connected to the signal output terminal, a second terminal of the bootstrap capacitor C1 and a drain of the pull-down transistor T4 respectively, and is used for providing the output signal to the signal output terminal; the pull-down transistor T4 has a gate connected to the second clock signal input terminal, and a source connected to the first signal terminal VGL, and is used for pulling down the output signal at the signal output terminal; the voltage capacitor C2 is used for stabilizing the potential at the pull-up node (i.e., gate connecting point of the pull-up transistor T3) after the signal input at the signal input terminal is completed, so as to make the output terminal more stable; the bootstrap capacitor C1 is used for raising the potential at the pull-up node, so that the potential at the pull-up node is higher than the potential at the first clock signal input terminal, so as to make the first clock signal output completely; the second signal terminal VGL1 and the first signal terminal VGL are at a low level. In the present embodiment, in order to more completely turn off the pull-up transistor T3 and reduce a leakage current of the pull-up transistor T3, the potential at the second signal terminal VGL1 is lower than the potential at the first signal terminal VGL.

[0030] Another advantage of the shift register unit and the gate driving circuit in the present embodiment is adopting a single channel type of transistor, that is, all the transistors are N-channel type transistors, thereby further reducing the complexity of the manufacturing process and the production cost. Of course, it is easy for those skilled in the art to obtain that the shift register unit provided in the present disclosure can be easily changed into all the transistors being P-channel type transistors, in particular as shown in Fig.8, which is not limited to the implementation provided in the present embodiment, thereby details omitted herein.

[0031] The present embodiment further provides a driving method for driving the above shift register unit. Referring to the driving timing diagram in Fig.10, all the transistors therein are N-channel type transistors, a clock signal CK1 is taken as a signal inputted from the second clock signal input terminal, and a clock signal CK3 is taken as a signal inputted from the first clock signal input terminal; a pulse width of the clock signal CK1 and the clock signal CK3 is the same as that of the start signal STV. The clock signal CK1 is not actuated until the start signal STV at the same stage in the gate driving circuit comprising the above shift register unit has passed three of times, and phase difference between the adjacent clock signals is 90 degrees. As such, the whole gate driving circuit needs four clock signals CK1~CK4. The operating process of the method for driving the shift register unit mainly comprises the following stages:

[0032] in a charging stage t1, the signal input terminal inputs a previous stage of output signal G(n-1) or the start signal STV, the potential at the pull-up node P is raised, the pull-up driving transistor T1 and the pull-up transistor T3 are turned on, the second signal input terminal inputs a low level signal to turn off the reset transistor T2 and the pull-down transistor T4, the previous stage of output signal G(n-1) or the start signal STV charges the voltage stabilizing capacitor C2 and the bootstrap capacitor C1, and a signal output terminal Gn outputs the low level signal.

[0033] in an outputting stage t2, the signal input at the signal input terminal is ended, the pull-up driving transistor T1 is turned off, the second clock signal input terminal inputs the low level signal, and the pull-down transistor T4 is turned off; the first clock signal input terminal inputs the high level signal , the bootstrap capacitor C1 raises the potential at the pull-up node P, the voltage stabilizing capacitor C2 maintains the potential at the pull-up node, and the pull-up transistor T3 completely outputs the high level signal at the first clock input terminal to the signal output terminal Gn;

a resetting stage including a first stage t3 and a second stage t4:

in a first stage t3: the first clock signal input terminal inputs the low level signal; at this time, the reset transistor T2 and the pull-down transistor T4 are still turned off, the pull-up transistor T3 is still turned on, and the low level signal inputted from the first clock signal input terminal pulls down the potential at the pull-up node P; although the potential at the pull-up node P is decreased, this potential can still turn on the pull-up transistor T3 to make the low level signal at the first clock signal input terminal output completely;

in a second stage t4: the second clock input terminal inputs the high level signal, the reset transistor T2 and the pull-down transistor T4 are turned on to again pull down the potential at the pull-up node P to the potential at the second signal terminal VGL1 to turn off the pull-up transistor T3, the potential at the signal output terminal

is pulled down to the potential at the first signal terminal VGL, and the turn-on of the pull-down transistor T4 again ensures to pull down the potential at the signal output terminal to the potential at the first signal terminal VGL.

[0034] Since the potential at the second signal terminal VGL1 is lower that the potential at the first signal terminal VGL, when the output signal is pulled down, the voltage at the pull-up node P is pulled down to the potential at the second signal terminal VGL1, and the voltage at the signal output terminal is pulled down to the potential at the first signal terminal VGL. Since VGL1 is smaller than VGL, the gate-source voltage VGS of the pull-up transistor T3 is below 0, so that there will be a more complete turn-off and a smaller leakage current.

[0035] The embodiment 1 uses 6 groups of clock signals while the embodiment 2 only uses 4 groups of clock signals; in embodiment 1, the pull-up transistor 3 only functions as pulling up while in embodiment 2, the pull-up transistor T3 immediately pulls down the output signal after pulling up, and further again pulls down the output signal through the pull-down transistor T4 at the next time, such that the pull-down capability of the whole gate driving circuit is greatly enhanced.

[0036] The embodiment of the present disclosure further provides a display device comprising the above gate driving circuit; since the used gate driving circuit has a smaller wiring area, the frame of the display device can be made to be narrower; further, since the pull-down capability of the whole gate driving circuit is enhanced, the response speed of the liquid crystal display device is increased.

[0037] The above embodiments are just used for specifying the present disclosure rather than limiting the present disclosure. Those skilled in the art can make various alternations and modifications without departing from the spirit and scope of the present disclosure, and thereby all equivalent technical solutions belong to the protection scope of the present disclosure.

Claims

1. A shift register unit comprising:

a pull-up module connected to a first clock signal input terminal, a signal output terminal and a pull-up node respectively, for outputting a signal inputted from the first clock signal input terminal to the signal output terminal according to a potential at the pull-up node, the pull-up node being a connecting point between the pull-up module and a pull-up driving module;

a pull-down module connected to the signal output terminal, a first signal terminal and a second clock signal input terminal respectively, for pulling down a potential at the signal output terminal to the first signal terminal according to a signal output from the second clock signal input terminal;

a pull-up driving module connected to a signal input terminal and the pull-up node respectively, for driving the pull-up module according to a signal inputted from the signal input terminal;

a reset module connected to a second signal terminal, a reset signal terminal and the pull-up node respectively, for resetting a signal at the pull-up node according to a signal inputted from the reset signal terminal; and

a voltage stabilizing module connected to the pull-up node, for stabilizing the potential at the pull-up node.

2. The shift register unit according to claim 1, wherein the reset signal terminal is connected to the second clock signal input terminal.

3. The shift register unit according to claim 1, wherein the first signal terminal and the second signal terminal are both at a low level; and the potential at the second signal terminal is lower than the potential at the first signal terminal.

4. The shift register unit according to any one of claims 1-3, wherein the pull-up driving module comprises a pull-up driving transistor, the reset module comprises a reset transistor, the pull-up module comprises a pull-up transistor and a bootstrap capacitor, the pull-down module comprises a pull-down transistor, and the voltage stabilizing module comprises a voltage stabilizing capacitor;

a gate and a drain of the pull-up driving transistor is connected to the signal input terminal, and a source of the pull-up driving transistor is connected to a drain of the reset transistor, a first terminal of the voltage stabilizing capacitor, a first terminal of the bootstrap capacitor and a gate of the pull-up transistor respectively;

a gate of the reset transistor is connected to the reset signal terminal, and a source of the reset transistor is connected to a second terminal of the voltage stabilizing capacitor and the second signal terminal respectively;

a drain of the pull-up transistor is connected to the first clock signal input terminal, and a source of the pull-up transistor is connected to the signal output terminal, a second terminal of the bootstrap capacitor and a drain of the pull-down transistor respectively; and

a gate of the pull-down transistor is connected to the second clock signal input terminal and a drain of the pull-down transistor is connected to the first signal terminal.

5. The shift register unit according to claim 4, wherein all the transistors are N-channel type transistors or all the transistors are P-channel type transistors.

6. A driving method for driving the shift register unit according to claim 1, comprising the following steps:

in a charging phase, inputting an output signal of a previous stage or a start signal from a signal input terminal to turn on a pull-up driving transistor and a pull-up transistor, inputting a clock signal from a reset signal terminal to turn off a reset transistor, and charging a voltage stabilizing capacitor and a bootstrap capacitor by the output signal of the previous stage or the start signal;
in an outputting stage, ending signal input at the signal input terminal to turn off the pull-up driving transistor, and inputting a clock signal from a second clock signal terminal to turn off the pull-down transistor, continuously turning on the pull-up transistor, raising a potential at a pull-up node by the bootstrap capacitor through a clock signal inputted from a first clock signal input terminal, maintaining the potential at the pull-up node by the voltage stabilizing capacitor, and outputting a signal at the first clock signal input terminal to a signal output terminal by the pull-up transistor; and
in a resetting stage, inputting a clock signal from the reset signal terminal to control the reset transistor and the pull-down transistor to be turned on, pulling down the potential at the pull-up node by the reset transistor to turn off the pull-up transistor, and pulling down a potential at a signal output terminal by the pull-down transistor.

7. The method for driving the shift register unit according to claim 6, wherein the reset signal input terminal is connected to the second clock signal input terminal.

8. A gate driving circuit comprising multiple shift register units according to any one of claims 1-5, except for a last stage of shift register unit, a signal output terminal of each stage of other shift register units is connected to a signal input terminal of a next stage of shift register unit, and a signal input terminal of a first stage of shift register unit is connected to a start signal.

9. A display device comprising the gate driving circuit according to claim 8.

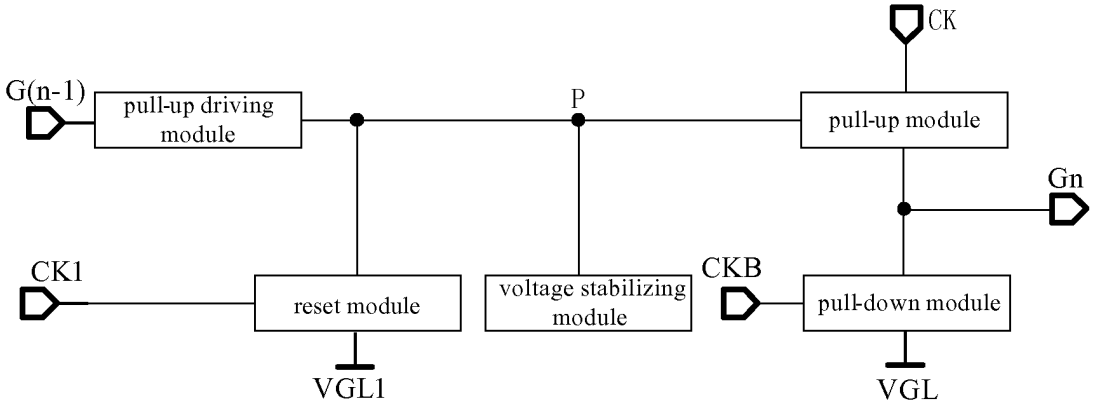


Fig.1

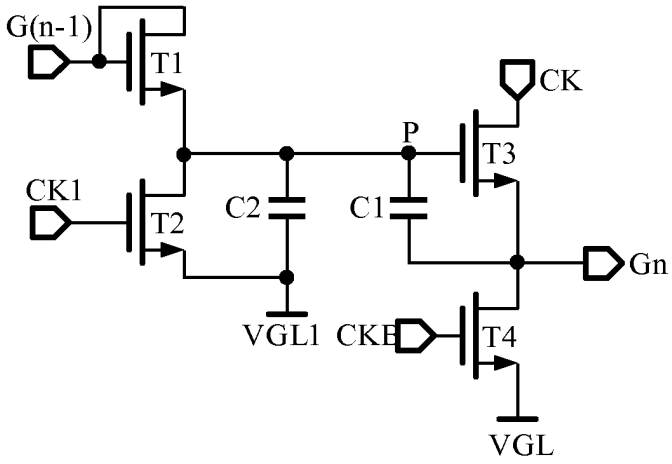


Fig.2

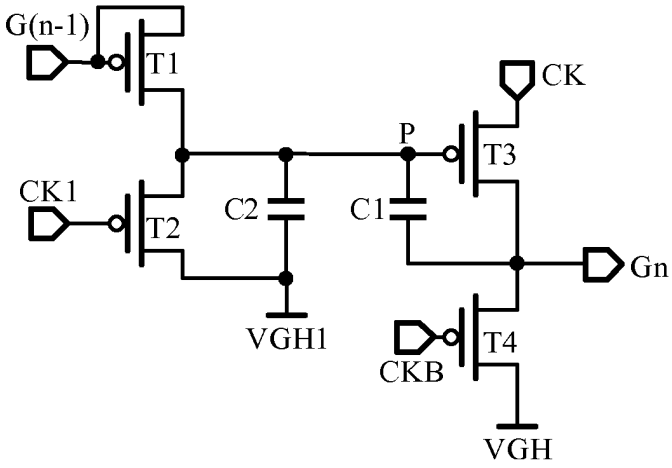
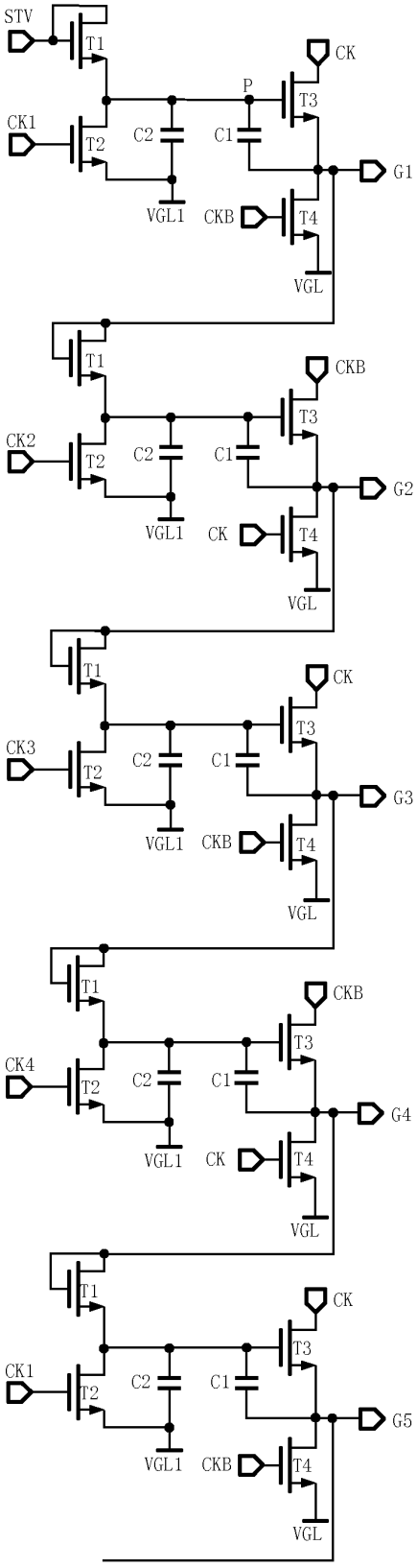


Fig.3


STV
T1
CK
P
T3
CK1
T2
C2
C1
G1
VGL1
CKB
T4
VGL
T1
CKB
T3
CK2
T2
C2
C1
G2
VGL1
CK
T4
VGL
T1
CK
T3
CK3
T2
C2
C1
G3
VGL1
CKB
T4
VGL
T1
CKB
T3
CK4
T2
C2
C1
G4
VGL1
CK
T4
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C2
C1
G5
VGL1
CKB
T4
VGL

Fig.4

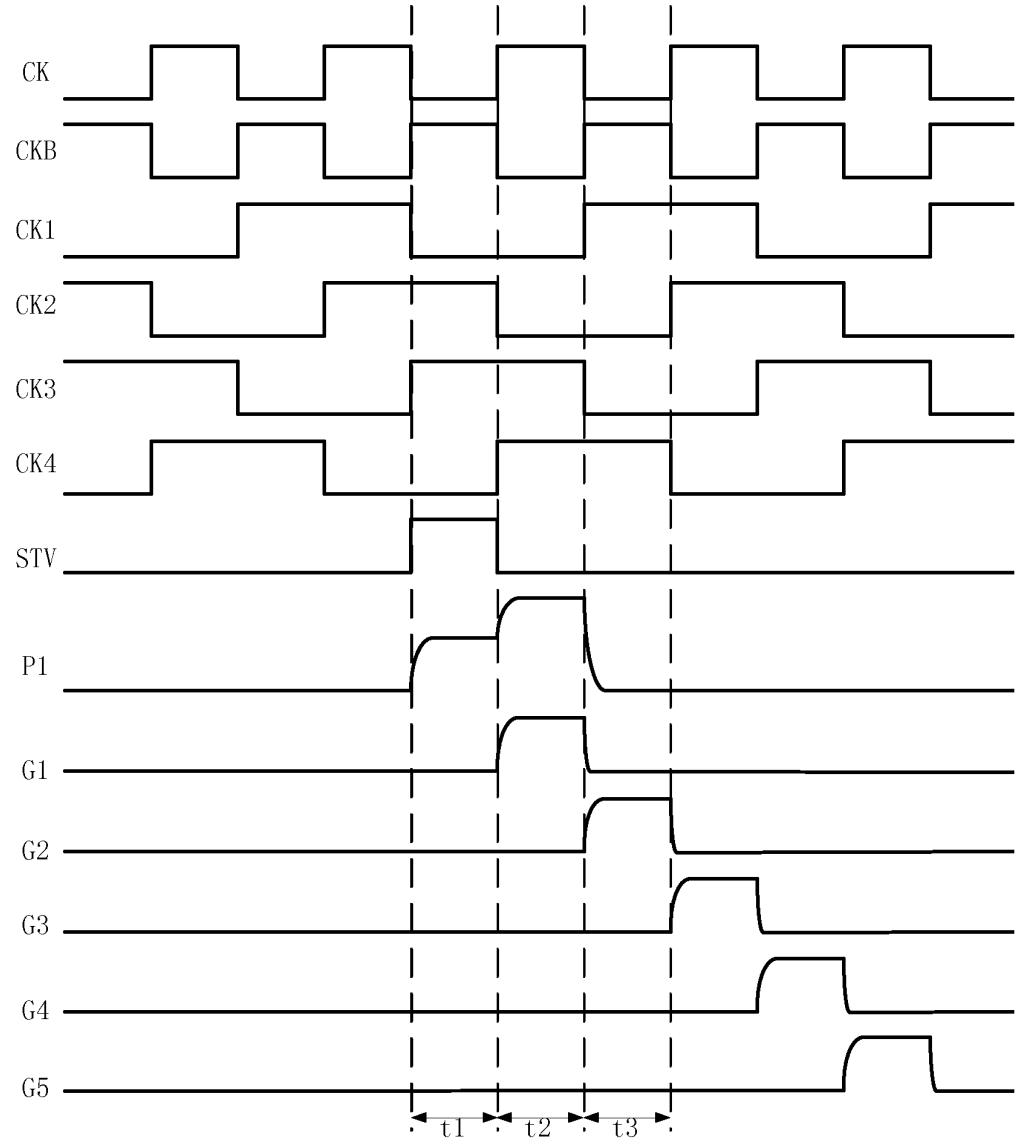
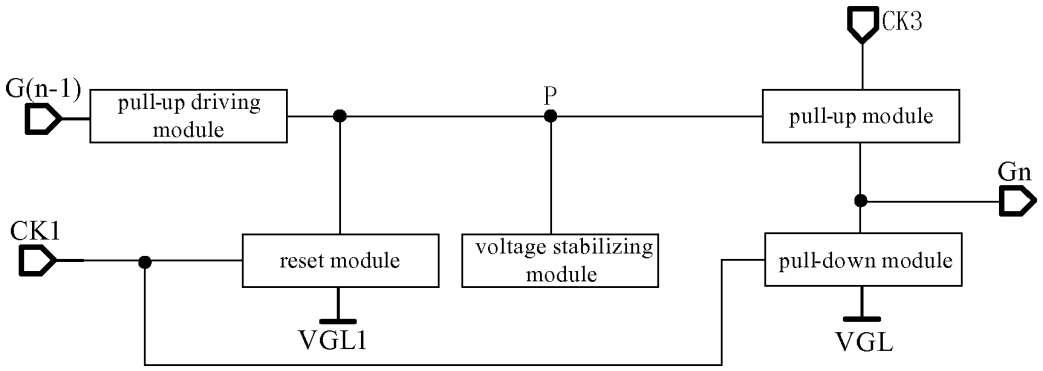

CK
CKB
CK1
CK2
CK3
CK4
STV
P1
G1
G2
G3
G4
G5
t1
t2
t3

Fig.5


CK3
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pull-up driving module
P
pull-up module
Gn
CK1
reset module
voltage stabilizing module
pull-down module
VGL1
VGL

Fig.6

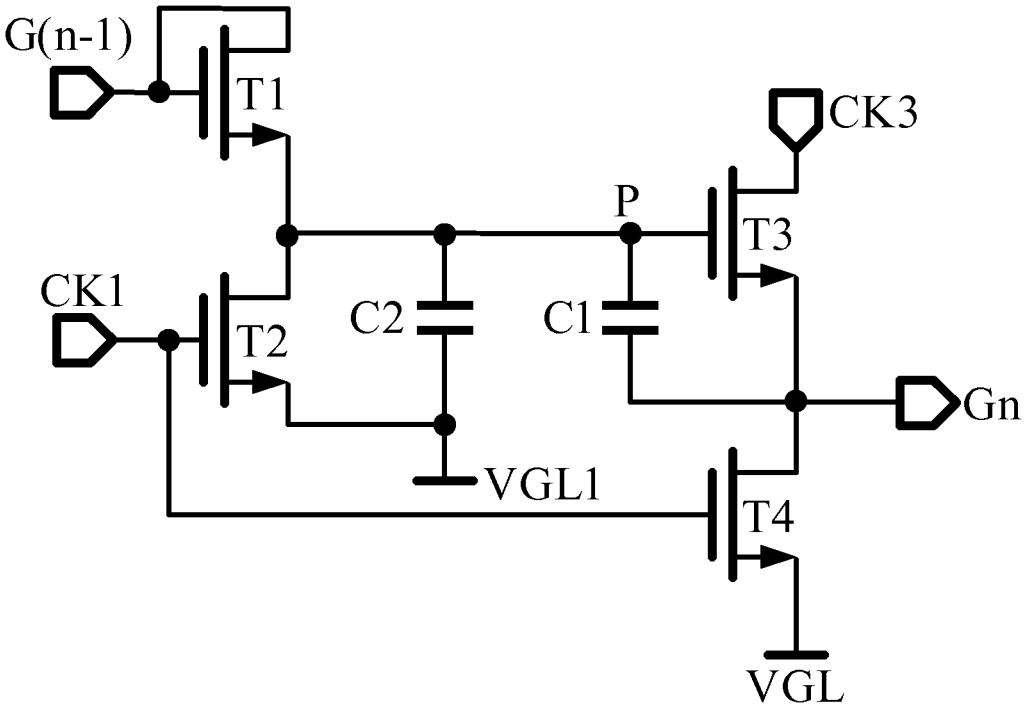

G(n-1)
T1
CK3
P
T3
CK1
T2
C2
C1
Gn
VGL1
T4
VGL

Fig.7

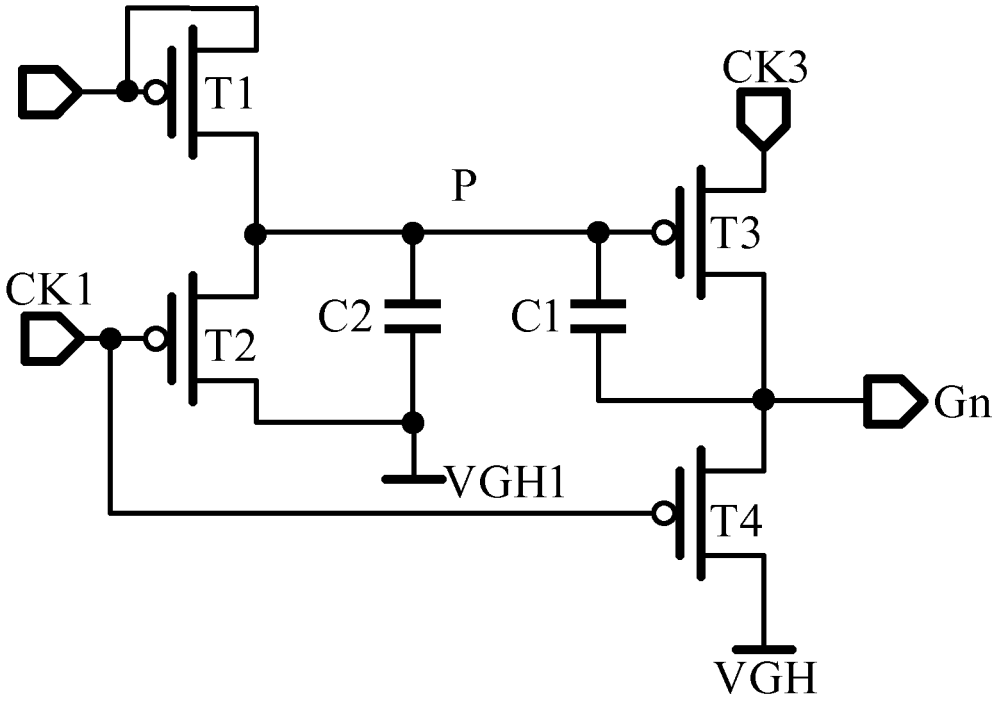
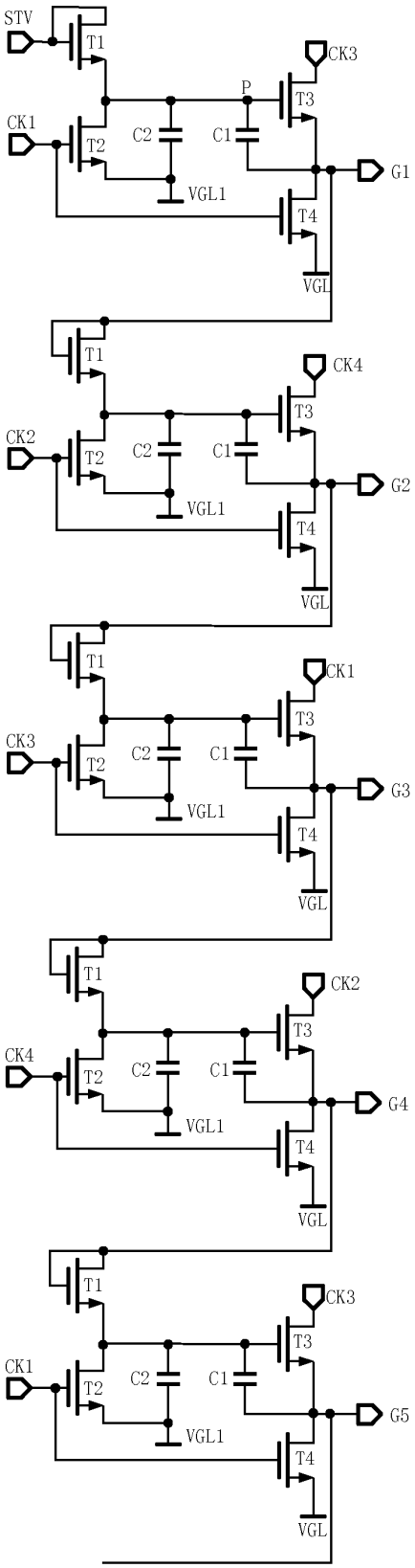

T1
CK3
P
T3
CK1
T2
C2
C1
Gn
VGH1
T4
VGH

Fig.8


STV
T1
CK3
P
T3
CK1
T2
C2
C1
G1
VGL1
T4
VGL
T1
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T2
C2
C1
G2
VGL1
T4
VGL
T1
CK1
T3
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T2
C2
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G3
VGL1
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T3
CK4
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C2
C1
G4
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CK1
T2
C2
C1
G5
VGL1
T4
VGL

Fig.9

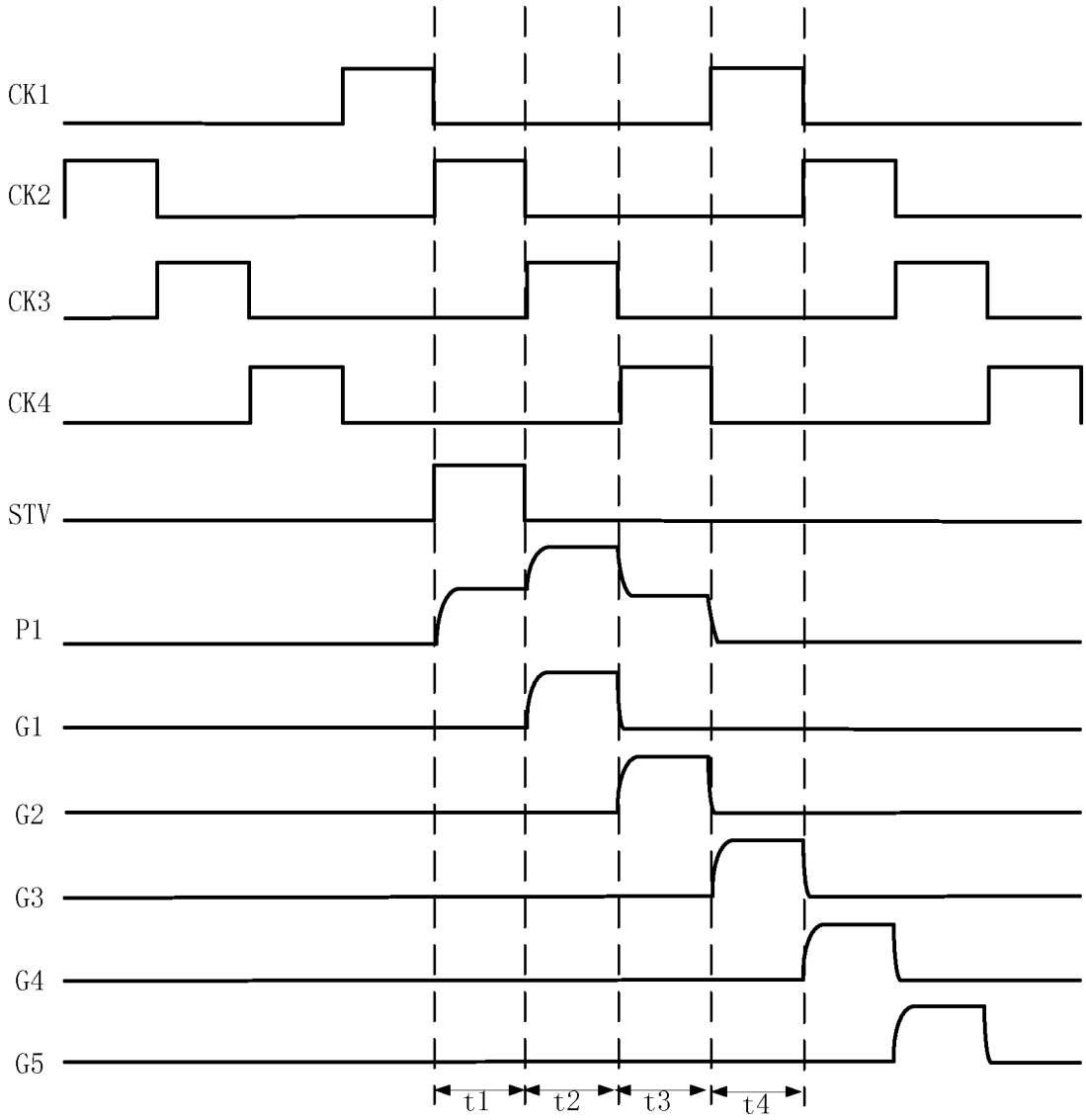

Fig.10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2013/085521

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/36 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G 3/36; G09G 3; G09G; G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNTXT, CNKI, VEN: shift, register, up, down, pull, reset, steady, voltage, capacitance, drive, clock

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN 102651186 A (BOE TECHNOLOGY GROUP CO LTD) 29 August 2012 (29.08.2012) description, paragraphs [0040]-[0047] and figures 3, 4 and 14	1-9
Y	CN 20273669 U (BOE TECHNOLOGY GROUP CO LTD) 29 August 2012 (29.08.2012) description, paragraphs [0060]-[0063] and figure 5	1-9
Y	CN 202771779 U (BOE TECHNOLOGY GROUP CO LTD) 06 March 2013 (06.03.2013) description, paragraphs [0019]-[0057] and figure 3	3-5, 8, 9
A	JP 2004199065 A (MITSUBISHI ELECTRIC CORP.) 16 August 2007 (16.08.2007) the whole document	1-9

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 April 2014	22 April 2014
Name and mailing address of the ISA State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No. (86-10) 62019451	Authorized officer NIE, Yingying Telephone No. (86-10) 62085738

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2013/085521

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN 102651186 A	29 August 2012	KR 20120115126 A	17 October 2012
		EP 2509077 A3	17 October 2012
		JP 2012221551 A	12 November 2012
		EP 2509077 A2	10 October 2012
		US 2012256817 A1	11 October 2012
CN 202736697 U	29 August 2012	None	
CN 202771779 U	06 March 2013	None	
JP 2007207411 A	16 August 2007	TW 200735027 A	16 September 2007
		CN 101030361 A	05 September 2007
		CN 100530337 C	19 August 2009
		KR 20070073634 A	10 July 2007
		KR 100838653 B1	16 June 2008
		US 2007164973 A1	19 July 2007
		US 7372300 B2	13 May 2008

Form PCT/ISA /210 (patent family annex) (July 2009)

专利名称(译)	移位寄存器单元及其驱动方法，栅极驱动电路和显示装置		
公开(公告)号	EP3029662A4	公开(公告)日	2017-03-22
申请号	EP2013866488	申请日	2013-10-18
[标]申请(专利权)人(译)	京东方科技集团股份有限公司 成都京东方光电科技有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司. 成都京东方光电科技有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司. 成都京东方光电科技有限公司.		
[标]发明人	HU LIKE QI XIAOJING		
发明人	HU, LIKE QI, XIAOJING		
IPC分类号	G09G3/36 G11C19/18		
CPC分类号	G11C19/28 G09G3/20 G09G2300/0465 G09G2310/0267 G09G2310/0286 G11C19/184		
优先权	201310329312.2 2013-07-31 CN		
其他公开文献	EP3029662A1		
外部链接	Espacenet		

摘要(译)

提供一种移位寄存器单元及其驱动方法，栅极驱动电路和显示装置。通过设置连接到上拉节点（P）的稳压电容器（C），移位寄存器单元利用稳压电容器（C2）来稳定上拉节点（P）的电位，从而使移位寄存器单元输出的信号更稳定;同时，使用极少量的晶体管和电容组成移位寄存器单元，大大减小了栅极驱动电路的布线面积，为液晶显示器件的设计提供了技术支持。一个较窄的框架。同时，由于简化了栅极驱动电路的结构，简化了栅极驱动电路的制造工艺，降低了制造成本。此外，移位寄存器单元通过两个下拉过程快速有效地将输出信号下拉到低电位，从而增强了栅极驱动电路的下拉能力。