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(54) **IMAGE DISPLAY DEVICE**

BILDANZEIGEVORRICHTUNG

DISPOSITIF D'AFFICHAGE D'IMAGE

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Description

TECHNICAL FIELD

[0001] The present invention relates to an image display device such as a liquid crystal display device.

BACKGROUND ART

[0002] As a technique to improve the response speed of a display panel included in an image display device, overdrive drive (also called overshoot drive) is conventionally known. In conventional typical overdrive drive, when the gradation value of a pixel included in a video signal is changed to a high (low) value, a voltage higher (lower) than a voltage required to obtain a desired luminance (a luminance corresponding to the gradation value after change) is applied to a pixel circuit in a display panel in the first frame period occurring after the change of the gradation value. The following discusses a liquid crystal display device as an example of an image display device.

[0003] In a liquid crystal display device that does not perform overdrive drive, when the drive voltage of a pixel is changed as shown in Fig. 9A, the luminance of the pixel changes as shown in Fig. 9B. As shown in Figs. 9A and 9B, when the drive voltage is changed with the change of a gradation value (not shown), the luminance changes slowly and thus it may take several frame periods for the luminance to reach a desired level.

[0004] On the other hand, in a liquid crystal display device that performs overdrive drive, the drive voltage of a pixel changes as shown in Fig. 10A, and the luminance of the pixel changes as shown in Fig. 10B. As shown in Figs. 10A and 10B, in one frame period starting from time 0, the drive voltage gets higher than a level required to obtain a desired luminance and the luminance changes sharply and reaches a desired level in a short time. As such, by performing overdrive drive, the response speed of a liquid crystal panel can be improved.

[0005] Liquid crystal display devices performing overdrive drive are described in, for example, JP 2000-231091 A, JP 2004-287139 A and JP 2005-49840 A. JP 2004-287139 A describes a liquid crystal display device shown in Fig. 11. In Fig. 11, an emphasis conversion unit 93 obtains an emphasis conversion signal that compensates for the optical response characteristics of a liquid crystal display panel 94, based on an input image signal (a current frame image signal), an image signal of a previous frame period which is stored in a frame memory 91, and an image signal of a second previous frame period which is stored in a frame memory 92. The drive voltage of a pixel gets higher than a level required to obtain a desired luminance, over two frame periods occurring after the change of a gradation value (see Fig. 12A), and the luminance of the pixel changes as shown in Fig. 12B. By this, the occurrence of an after-image when performing moving image display is suppressed and a halftone can be displayed properly.

[0006] US 2005/0024353 A1 shows an electro-optic display, having at least one pixel capable of achieving any one of at least four different gray levels including two extreme optical states, is driven by displaying a first image on the display, and rewriting the display to display a second image thereon, wherein, during the rewriting of the display, any pixel which has undergone a number of transitions exceeding a predetermined value without touching an extreme optical state, is driven to at least one extreme optical state before driving that pixel to its final optical state in the second image.

[0007] US 2005/0001802 A1 relates to a liquid crystal display apparatus capable of improving response time as well as display quality. The apparatus includes a timing controller to generate a plurality of compensated grayscale data, a memory to store grayscale data or the compensated grayscale data, a column driver to apply the compensated grayscale data to a plurality of data lines, a gate driver to apply a gate signal to a plurality of gate lines, and a liquid crystal panel including the gate lines, the data lines and a plurality of switching element disposed between the data lines and the gate lines.

[0008] EP 2065879 A1 shows a liquid crystal panel drive device (2) which includes a signal processing section (7) for determining an output gray scale in accordance with a gray scale transition from the gray scale which is forecasted to reach by a previous response to an input gray scale and can carry out overdrive with the output gray scale. At a temperature at which a rise gray scale transition may occur in absence of a response condition does not exist for single overdrive, the signal processing section (7) determines, as an output gray scale, a gray scale lower than a maximum gray scale with respect to a particular gray scale transition out of a rise type gray scale transition. In such a way, a display quality (especially a moving image display quality) at a low temperature can be improved.

SUMMARY OF THE INVENTION

PROBLEMS TO BE SOLVED BY THE INVENTION

[0009] However, in a conventional liquid crystal display device performing overdrive drive, a phenomenon may occur where the luminance of a pixel increases once immediately after the application of a drive voltage and decreases thereafter and increases again (or the luminance of a pixel decreases once immediately after the application of a drive voltage and increases thereafter and decreases again). This phenomenon is hereinafter referred to as double optical responsivity. If double optical responsivity occurs, when a user visually watches a screen displaying a moving image (e.g., a scroll screen), he/she recognizes the luminance of an edge portion as abnormally high (this phenomenon is hereinafter referred to as angular response). If the drive voltage is lowered to prevent angular response, then the effect of an improvement in response speed brought about by overdrive drive is impaired.

[0010] Double optical responsivity is likely to occur in, for example, an MVA (Multi-domain Vertical Alignment)-type liquid crystal panel. In the MVA-type liquid crystal panel, an alignment film surface is not subjected to a rubbing process as a domain control means and liquid crystal molecules are pretilted at a small angle by protrusions, etc., provided on a part of an electrode. Hence, at the moment of application of a drive voltage to a pixel, first, liquid crystal molecules close to a protruding portion rapidly respond, and thereafter, liquid crystal molecules in a domain are sequentially aligned like a domino toppling. Accordingly, when overdrive drive is performed, although the luminance of an area around a protruding portion in a domain changes rapidly, the luminance of an area other than the area around the protruding portion changes with a lag (see Fig. 13). As such, because overdrive drive is performed on an MVA-type liquid crystal panel does not mean the luminance rapidly changes in all areas in a domain.

[0011] When the user visually watches a liquid crystal panel, he/she recognizes the average luminance in a domain as luminance. Fig. 13 is a diagram showing a detail of the changes in luminance shown in Fig. 10B. As shown in Fig. 13, in the first frame period occurring after the change of a gradation value, both the luminance of an area around a protruding portion and the luminance of an area other than the area around the protruding portion increase and thus the average luminance increases. In the next frame period, since the luminance of the area around the protruding portion decreases at a higher speed than a speed at which the luminance of the area other than the area around the protruding portion increases, the average luminance decreases. In subsequent frame periods, the luminance of the area around the protruding portion becomes substantially constant and the luminance of the area other than the area around the protruding portion increases, and thus, the average luminance increases. As a result, double optical responsivity where the luminance of a pixel increases once and decreases thereafter and increases again occurs.

[0012] Even in the liquid crystal display device shown in Fig. 11, when the response speed of the liquid crystal display panel 94 is slow, the luminance of a pixel changes as shown in Fig. 12B. As such, even the liquid crystal display device shown in Fig. 11 cannot completely prevent double optical responsivity.

[0013] An object of the present invention is therefore to provide an image display device capable of preventing double optical responsivity occurring due to overdrive drive.

MEANS FOR SOLVING THE PROBLEMS

[0014] According to a first aspect of the present invention, there is provided an image display device that performs signal processing on a video signal and thereby displays an image, the image display device including: a display panel; a first storage unit that stores, when a gradation value of a pixel included in an input video signal has been changed from a previous frame, a gradation value before change, for each pixel; a hold count calculation unit that determines, for each pixel, a hold count indicating a number of frames inputted after a change of a gradation value; a second storage unit that stores the hold counts determined by the hold count calculation unit; an emphasis conversion unit that obtains an emphasis video signal based on the input video signal, the gradation values before change which are stored in the first storage unit, and the hold counts determined by the hold count calculation unit, the emphasis video signal compensating for optical response characteristics of the display panel; and a drive unit that drives the display panel based on the emphasis video signal.

[0015] Still according to the first aspect of the present invention, the image display device further includes: a third storage unit that stores one frame of the input video signal and outputs a video signal of the previous frame; and a gradation change detection unit that compares the input video signal with the video signal of the previous frame outputted from the third storage unit to determine, for each pixel, whether a gradation value has been changed from the previous frame.

[0016] According to a second aspect of the present invention, in the first aspect of the present invention, when a gradation value of a pixel is changed by a value greater than or equal to a predetermined value between the input video signal and the video signal of the previous frame outputted from the third storage unit, the gradation change detection unit determines that the gradation value has been changed from the previous frame.

[0017] According to a third aspect of the present invention, in the first aspect of the present invention, a maximum value of the hold counts determined by the hold count calculation unit is 3 or more.

[0018] According to a fourth aspect of the present invention, in the first aspect of the present invention, the emphasis conversion unit obtains an emphasis video signal where the changes in gradation values are emphasized more than those in the input video signal, and makes a degree of emphasis smaller with larger hold counts determined by the hold count calculation unit.

[0019] According to a fifth aspect of the present invention, in the fourth aspect of the present invention, the emphasis conversion unit includes a look up table and obtains the emphasis video signal using the look up table.

[0020] According to a sixth aspect of the present invention, in the fourth aspect of the present invention, the emphasis conversion unit includes an arithmetic circuit and obtains the emphasis video signal using the arithmetic circuit.

[0021] According to a seventh aspect of the present invention, in the fourth aspect of the present invention, the emphasis conversion unit includes a look up table and an arithmetic circuit and obtains the emphasis video signal using the look up table and the arithmetic circuit.

[0022] According to an eighth aspect of the present invention, in the first aspect of the present invention, the display panel has a response speed slower than two frame periods.

[0023] According to a ninth aspect of the present invention, in the eighth aspect of the present invention, the display panel is an MVA-type liquid crystal panel.

[0024] According to an tenth aspect of the present invention, there is provided an image display method for performing signal processing on a video signal and thereby displaying an image on a display panel, the method including the steps of: storing in a third storage unit a previous frame of the input video signal; comparing the input video signal with the video signal of the previous frame to determine, for each pixel, whether a gradation value changes from the previous frame; storing, when a gradation value of a pixel included in an input video signal has been changed from a previous frame, a gradation value before change within a first storage unit, for each pixel; determining, for each pixel, a hold count indicating a number of frames inputted after a change of a gradation value; storing the determined hold counts within a second storage unit; obtaining an emphasis video signal based on the input video signal, the stored gradation values before change within the first storage unit, and the determined hold counts, the emphasis video signal compensating for optical response characteristics of the display panel; and driving the display panel based on the emphasis video signal.

EFFECT OF THE INVENTION

[0025] According to the first or tenth aspect of the present invention, an emphasis video signal that compensates for the optical response characteristics of a display panel is obtained based on an input video signal, gradation values before change, and the hold counts, and the display panel is driven based on the emphasis video signal. As such, by obtaining an emphasis video signal according to the elapsed time after the change of gradation value by referring to the hold counts, the optical response characteristics of the display panel are favorably compensated for, enabling to prevent double optical responsivity occurring due to overdrive drive.

[0026] Still according to the first or tenth aspect of the present invention, a determination as to whether a gradation value has been changed from the previous frame can be easily made using a third storage unit and a gradation change detection unit.

[0027] According to the second aspect of the present invention, when a gradation value is changed by a certain degree or more, it is determined that the gradation value has been changed from the previous frame. This can prevent a situation where, when a gradation value slightly fluctuates due to the influence of noise, display is performed with the noise being emphasized by overdrive drive.

[0028] According to the third aspect of the present invention, by referring to the hold counts whose maximum value is 3 or more, elapsed time after the change of gradation value is measured for at least three frame periods, and an emphasis video signal according to the elapsed time is obtained. By this, the optical response characteristics of the display panel are favorably compensated for, enabling to prevent double optical responsivity occurring due to overdrive drive.

[0029] According to the fourth aspect of the present invention, when an emphasis video signal is obtained by performing a process of emphasizing changes in gradation values on an input video signal, the degree of emphasis is made smaller with longer elapsed time after the change of gradation value by referring to the hold counts. By this, an emphasis video signal capable of favorably compensating for the optical response characteristics of the display panel can be obtained. By driving the display panel based on the emphasis video signal, double optical responsivity occurring due to overdrive drive can be prevented.

[0030] According to the fifth aspect of the present invention, by referring to a look up table, an emphasis video signal can be obtained accurately and easily.

[0031] According to the sixth aspect of the present invention, by obtaining an emphasis video signal using an arithmetic circuit, the amount of circuitry for the look up table can be reduced.

[0032] According to the seventh aspect of the present invention, by providing a look up table and an arithmetic circuit, the amount of circuitry can be reduced over the case of providing only the look up table, and an emphasis video signal can be obtained accurately and easily over the case of providing only the arithmetic circuit.

[0033] According to the eighth aspect of the present invention, in an image display device including a display panel with a response speed slower than two frame periods, double optical responsivity that occurs over two frame periods or more due to overdrive drive can be prevented.

[0034] According to the ninth aspect of the present invention, in a liquid crystal display device including an MVA-type liquid crystal panel which is likely to cause double optical responsivity due to overdrive drive, double optical responsivity can be prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035]

Fig. 1 is a block diagram showing a configuration of a liquid crystal display device according to an embodiment of the present invention.

Fig. 2 is a block diagram showing a detail of an overdrive circuit in the liquid crystal display device shown in Fig. 1.

Fig. 3 is a diagram showing an exemplary configuration of a look up table included in the overdrive circuit shown in Fig. 2.

Fig. 4A is a diagram showing an example (first example) of changes in signal values in the overdrive circuit shown in Fig. 2.
Fig. 4B is a diagram showing an example (first example) of changes in output gradation value determined by the overdrive circuit shown in Fig. 2.
Fig. 4C is a diagram showing an example (first example) of changes in luminance in the liquid crystal display device shown in Fig. 1.
Fig. 5A is a diagram showing an example (second example) of changes in signal values, as in Fig. 4A.
Fig. 5B is a diagram showing an example (second example) of changes in output gradation value, as in Fig. 4B.
Fig. 5C is a diagram showing an example (second example) of changes in luminance, as in Fig. 4C.
Fig. 6A is a diagram showing an example (third example) of changes in signal values, as in Fig. 4A.
Fig. 6B is a diagram showing an example (third example) of changes in output gradation value, as in Fig. 4B.
Fig. 6C is a diagram showing an example (third example) of changes in luminance, as in Fig. 4C.
Fig. 7A is a diagram showing an example (fourth example) of changes in signal values, as in Fig. 4A.
Fig. 7B is a diagram showing an example (fourth example) of changes in output gradation value, as in Fig. 4B.
Fig. 7C is a diagram showing an example (fourth example) of changes in luminance, as in Fig. 4C.
Fig. 8A is a diagram showing changes in drive voltage in the liquid crystal display device shown in Fig. 1.
Fig. 8B is a diagram showing changes in luminance in the liquid crystal display device shown in Fig. 1.
Fig. 9A is a diagram showing changes in drive voltage in a conventional liquid crystal display device that does not perform overdrive drive.
Fig. 9B is a diagram showing changes in luminance in the conventional liquid crystal display device that does not perform overdrive drive.
Fig. 10A is a diagram showing changes in drive voltage in a conventional liquid crystal display device that performs an overshoot process.
Fig. 10B is a diagram showing changes in luminance in the conventional liquid crystal display device that performs an overshoot process.
Fig. 11 is a block diagram showing a configuration of a conventional liquid crystal display device.
Fig. 12A is a diagram showing changes in drive voltage in the liquid crystal display device shown in Fig. 11.
Fig. 12B is a diagram showing changes in luminance in the liquid crystal display device shown in Fig. 11.
Fig. 13 is a diagram showing a detail of the changes in luminance shown in Fig. 10B.

MODE FOR CARRYING OUT THE INVENTION

[0036] Fig. 1 is a block diagram showing a configuration of a liquid crystal display device according to an embodiment of the present invention. A liquid crystal display device 10 shown in Fig. 1 includes a timing control circuit 11, an overdrive circuit 12, a liquid crystal drive circuit 13, and a liquid crystal panel 14. The liquid crystal panel 14 includes a plurality of pixel circuits 15 arranged two-dimensionally. The liquid crystal display device 10 performs signal processing on an input video signal Vin supplied from an external source, and thereby displays an image on the liquid crystal panel 14.

[0037] The input video signal Vin includes a video signal Va which is image data and a synchronizing signal Sa indicating display timing. The video signal Va is inputted to the overdrive circuit 12 and the synchronizing signal Sa is inputted to the timing control circuit 11. The timing control circuit 11 outputs, based on the synchronizing signal Sa, a control signal CS for the overdrive circuit 12 and a synchronizing signal Sb for the liquid crystal drive circuit 13. The overdrive circuit 12 performs signal processing for compensating for the optical response characteristics of the liquid crystal panel 14, on the video signal Va according to the control signal CS, and outputs an obtained video signal Vb to the liquid crystal drive circuit 13. The liquid crystal drive circuit 13 drives the liquid crystal panel 14 based on the synchronizing signal Sb and the video signal Vb. Voltages according to the video signal Vb obtained by the overdrive circuit 12 are applied to the pixel circuits 15 included in the liquid crystal panel 14. In this manner, an image based on the input video signal Vin is continuously displayed on the liquid crystal panel 14.

[0038] Fig. 2 is a block diagram showing a detail of the overdrive circuit 12. As shown in Fig. 2, the overdrive circuit 12 includes first to third frame memories 21 to 23, a one-clock delay circuit 24, a two-clock delay circuit 25, a gradation change detection circuit 26, a hold count calculation circuit 27, and an emphasis conversion circuit 28. The emphasis conversion circuit 28 includes a look up table (hereinafter, referred to as LUT) 31 and an arithmetic circuit 32.

[0039] In the following, it is assumed that the video signal Va inputted to the overdrive circuit 12 has a resolution of 1920x1080 pixels and includes an 8-bit gradation value for each of RGB of each pixel. A gradation value included in the video signal Va is referred to as a current frame gradation value Din(n) and a gradation value included in the video signal Vb is referred to as an output gradation value Dout (n). Note that the resolution and number of gradation levels of the video signal Va may be arbitrarily determined according to the specifications of the liquid crystal display device 10.

[0040] The third frame memory 23 has a capacity capable of storing at least one frame of the video signal Va. The third frame memory 23 stores one frame of the video signal Va and outputs the stored video signal after one frame period, as a previous frame video signal. When the video signal Va has the above-described format (1920x1080 pixels and 8 bits for each of RGB), as the third frame memory 23, a memory having a capacity of 49,766,400 bits (=1920x1080x3x8) or more is used. A gradation value included in the video signal outputted from the third frame memory 23 is referred to as an immediately previous frame gradation value Din(n-1). Note that the superscript symbol * indicates that data is delayed by one clock.

[0041] The gradation change detection circuit 26 compares the video signal Va with the video signal outputted from the third frame memory 23 and outputs a gradation comparison result Cmp* indicating for each pixel whether the gradation value has been changed from the previous frame. More specifically, the gradation change detection circuit 26 calculates a difference between the current frame gradation value Din(n) and the immediately previous frame gradation value Din(n-1) (hereinafter, referred to as the amount of gradation change). If the amount of gradation change is greater than or equal to a predetermined threshold value, then the gradation change detection circuit 26 determines that there is a change in gradation and thus outputs Cmp*=1. If the amount of gradation change is less than the threshold value, then the gradation change detection circuit 26 determines that there is no change in gradation and thus outputs Cmp*=0. For example, when the threshold value is 5, the gradation change detection circuit 26 outputs Cmp*=1 when the amount of gradation change is ± 5 or more, and outputs Cmp*=0 when the amount of gradation change is within ± 4 gradation levels. The threshold value of the amount of gradation change is determined according to the characteristics of the video signal Va, etc. As such, when the gradation value of a pixel is changed by a value greater than or equal to the predetermined value between the video signal Va and the video signal outputted from the third frame memory 23, the gradation change detection circuit 26 determines that the gradation value has been changed from the previous frame.

[0042] The one-clock delay circuit 24 and the two-clock delay circuit 25 are provided to adjust the timing of signal processing in the overdrive circuit 12. The one-clock delay circuit 24 delays the video signal outputted from the third frame memory 23 by one clock and outputs the delayed video signal. The two-clock delay circuit 25 delays the video signal Va by two clocks and outputs the delayed video signal Va. A gradation value included in the video signal outputted from the one-clock delay circuit 24 is referred to as Din(n-1)*, and a gradation value included in the video signal outputted from the two-clock delay circuit 25 is referred to as Din(n)**.

[0043] The first frame memory 21 has a capacity capable of storing at least one frame of the video signal Va, as with the third frame memory 23. When the gradation values of pixels included in the video signal Va are changed, the first frame memory 21 stores, for each pixel, a gradation value before change. More specifically, a gradation value stored in the first frame memory 21 is updated to a gradation value Din(n-1)* outputted from the one-clock delay circuit 24, when the gradation change detection circuit 26 determines that there is a change in gradation (when Cmp*=1), and is held without being updated when the gradation change detection circuit 26 determines that there is no change in gradation (when Cmp*=0). A gradation value before change which is stored in the first frame memory 21 is referred to as Din(hold)**. Note that the superscript symbol ** indicates that data is delayed by two clocks.

[0044] The second frame memory 22 and the hold count calculation circuit 27 are provided to determine, for each pixel, the number of frames inputted after the change of a gradation value

[0045] (hereinafter, referred to as the hold count). The second frame memory 22 stores, for each pixel, the hold count which is determined for the immediately previous frame. The hold count calculation circuit 27 determines, for each pixel, the hold count for the current frame based on the gradation comparison result obtained by the gradation change detection circuit 26 and the hold count for the immediately previous frame which is outputted from the second frame memory 22.

[0046] More specifically, when the gradation change detection circuit 26 determines that there is a change in gradation (Cmp*=1), the hold count calculation circuit 27 sets the hold count for the current frame to 1, regardless of the hold count for the immediately previous frame. On the other hand, when the gradation change detection circuit 26 determines that there is no change in gradation (Cmp*=0), the hold count calculation circuit 27 sets a value obtained by adding 1 to the hold count for the immediately previous frame, as the hold count for the current frame. Note, however, that a maximum value is set for the hold count, and when a result where 1 is added exceeds the maximum value, the hold count calculation circuit 27 resets the hold count for the current frame to 0. The hold count Cnt** determined by the hold count calculation circuit 27 is outputted to the emphasis conversion circuit 28 and is also written into the second frame memory 22 so as to be referred to when determining the hold count for the next frame.

[0047] The maximum value of the hold count is determined taking into account the response characteristics of the liquid crystal panel 14, etc. For example, when the maximum value of the hold count is 7, the hold count can be represented by 3 bits. When the video signal Va has the above-described format (1920x1080 pixels and 8 bits for each of RGB), as the second frame memory 22, a memory having a capacity of 18,662,400 bits (=1920x1080x3x3 bits) or more is used. In a general liquid crystal panel, when the maximum value of the hold count is determined to be 7 or more, double optical responsivity can be substantially completely prevented.

[0048] To the emphasis conversion circuit 28 are inputted the current frame gradation value Din(n)** outputted from the two-clock delay circuit 25, the gradation value before change Din(hold)** outputted from the first frame memory 21, and the hold count Cnt** outputted from the hold count calculation circuit 27. The emphasis conversion circuit 28 determines an output gradation value Dout(n) based on these three values. When Cnt**=0, the emphasis conversion circuit 28 outputs the current frame gradation value Din(n)** as it is, as an output gradation value Dout(n). When Cnt**≠0, the emphasis conversion circuit 28 determines an output gradation value Dout(n) using the LUT 31 and the arithmetic circuit 32.

[0049] Fig. 3 is a diagram showing an exemplary configuration of the LUT 31. As shown in Fig. 3, the LUT 31 stores in advance output gradation values Dout(n) in association with some of combinations of three values inputted to the emphasis conversion circuit 28. In an example shown in Fig. 3, as the representative values of the current frame gradation value Din(n)**, nine values (0, 32, 64, 96, 128, 160, 192, 224, and 255) are selected, and as the representative values of the gradation value before change Din (hold)**, the same nine values are selected. The hold count Cnt** takes a value between 1 and 7, inclusive. In this case, the LUT 31 stores in advance 567 (=9x9x7) output gradation values Dout(n). The LUT 31 is formed using, for example, a ROM, etc.

[0050] When two gradation values Din(n)** and Din(hold)** are both included in the representative values, the emphasis conversion circuit 28 refers to the LUT 31 using these two gradation values and the hold count Cnt**, and outputs a value read from the LUT 31 as it is, as an output gradation value Dout(n). When at least one of two gradation values Din(n)** and Din(hold)** is not included in the representative values, the emphasis conversion circuit 28 refers to the LUT 31 two or four times using representative values close to the two gradation values and the hold count Cnt**, performs, by the arithmetic circuit 32, a linear interpolation operation on two or four LUT outputs, and outputs a result thereof as an output gradation value Dout(n).

[0051] For example, when Din (n) **=96, Din (hold) **=50, and Cnt**=1, the emphasis conversion circuit 28 refers to the LUT 31 by changing three values {Din(n)**, Din(hold)**, Cnt**} in two ways, i.e., {96, 32, 1} and {96, 64, 1}, and performs a linear interpolation operation on obtained two LUT outputs. When Din (n) **=100, Din (hold) **=50, and Cnt**=1, the emphasis conversion circuit 28 refers to the LUT 31 by changing the above-described three values in four ways, i.e., {96, 32, 1}, {96, 64, 1}, {128, 32, 1}, and {128, 64, 1}, and performs a linear interpolation operation on obtained four LUT outputs.

[0052] The contents of output gradation values Dout(n) stored in the LUT 31 and a linear interpolation operation performed by the arithmetic circuit 32 are determined such that in a video signal Vb the change in gradation value is emphasized more than that in a video signal Va, and the larger the hold count the smaller the degree of emphasis. Using such a LUT 31 and an arithmetic circuit 32, the emphasis conversion circuit 28 obtains a video signal Vb where the change in gradation value is emphasized more than that in the video signal Va, and makes the degree of emphasis smaller with a larger hold count.

[0053] Note that in the above description the emphasis conversion circuit 28 includes the LUT 31 and the arithmetic circuit 32 and obtains a video signal Vb using the LUT 31 and the arithmetic circuit 32. Instead of this, the emphasis conversion circuit 28 may include only the LUT 31 and obtain a video signal Vb using the LUT 31, or alternatively may include only the arithmetic circuit 32 and obtain a video signal Vb using the arithmetic circuit 32. According to the emphasis conversion circuit 28 including the LUT 31, by referring to the LUT 31, a video signal Vb can be obtained accurately and easily. According to the emphasis conversion circuit 28 including the arithmetic circuit 32, by obtaining a video signal Vb using the arithmetic circuit 32, the amount of circuitry for a LUT can be reduced. According to the emphasis conversion circuit 28 including the LUT 31 and the arithmetic circuit 32, the amount of circuitry can be reduced over the case of providing only the LUT 31, and a video signal Vb can be obtained accurately and easily over the case of providing only the arithmetic circuit 32.

[0054] A detail of the operation of the overdrive circuit 12 will be described below using four specific examples. Figs. 4A to 4C are diagrams relating to a first example. Fig. 4A shows, for a given pixel, changes in signal values in the overdrive circuit 12 for every frame time, Fig. 4B shows changes in output gradation value Dout (n) for the pixel, and Fig. 4C shows changes in luminance (response waveform) for the pixel. Figs. 5A to 5C, 6A to 6C, and 7A to 7C are diagrams showing the same contents as those in Figs. 4A to 4C, for a second example, a third example, and a fourth example, respectively.

[0055] In the first example (see Figs. 4A to 4C), the case in which the gradation value increases will be described. In the first example, the gradation value is first 0 and changes to 64 in the fourth frame. In this case, the liquid crystal display device 10 performs overdrive drive over seven frame periods from the fourth frame to the tenth frame.

[0056] In the fourth frame (a shaded portion in Fig. 4A), since Din(n)=64 and Din(n-1)=0, the amount of gradation change is +64. The gradation change detection circuit 26 determines that there is a change in gradation and thus outputs Cmp*=1. Since Cmp*=1, a gradation value before change Din(hold)** stored in the first frame memory 21 is updated to 0 using a gradation value Din (n-1) * outputted from the one-clock delay circuit 24. The hold count calculation circuit 27 outputs Cnt**=1, and the hold count stored in the second frame memory 22 is updated to 1. To the emphasis conversion circuit 28 are inputted Din(n)**=64, Din (hold) **=0, and Cnt**=1. Since two gradation values are both included in the representative values in the LUT 31, the emphasis conversion circuit 28 outputs a value read from the LUT 31 as an output gradation value Dout(n) without using the arithmetic circuit 32. As a result, Dout(n)=160.

[0057] In the fifth frame, since Din(n)=64 and Din(n-1)=64, the amount of gradation change is 0 . The gradation change detection circuit 26 determines that there is no change in gradation and thus outputs Cmp*=0. Since Cmp*=0, the gradation value before change Din(hold)** stored in the first frame memory 21 is held without being updated. The hold count calculation circuit 27 adds 1 to the hold count (the value is 1) outputted from the second frame memory 22 and outputs Cnt**=2, and the hold count stored in the second frame memory 22 is updated to 2. To the emphasis conversion circuit 28 are inputted Din(n)**=64, Din (hold) **=0, and Cnt**=2. Since two gradation values are both included in the representative values in the LUT 31, the emphasis conversion circuit 28 outputs a value read from the LUT 31 as an output gradation value Dout(n) without using the arithmetic circuit 32. As a result, Dout(n)=76. For subsequent frames, likewise, in the sixth frame to the tenth frame, output gradation values Dout(n) are 68, 66, 65, 65, and 65, respectively.

[0058] Since in the eleventh frame Din(n)=64 and Din(n-1)=64, the amount of gradation change is 0. The gradation change detection circuit 26 determines that there is no change in gradation and thus outputs Cmp*=0. Since Cmp*=0, the gradation value before change Din (hold) ** stored in the first frame memory 21 is held without being updated. When 1 is added to the hold count (the value is 7) outputted from the second frame memory 22, a result thereof exceeds a maximum value of the hold count of 7. Hence, the hold count calculation circuit 27 outputs Cnt**=0 and thus the hold count stored in the second frame memory 22 is reset to 0. To the emphasis conversion circuit 28 are inputted Din (n) **=64, Din(hold)**=0, and Cnt**=0. Since Cnt**=0, the emphasis conversion circuit 28 outputs the current frame gradation value Din(n)** as an output gradation value Dout(n) without using the LUT 31 and the arithmetic circuit 32. As a result, Dout(n)=64. For subsequent frames, likewise, in each frame in and after the twelfth frame, Dout(n)=64.

[0059] In the first example, the output gradation value changes as shown in Fig. 4B, and the luminance increases in the fourth frame and becomes substantially constant in and after the fifth frame, as shown in Fig. 4C. As such, in the first example, double optical responsivity caused by overdrive drive does not occur.

[0060] In the second example (see Figs. 5A to 5C), the case will be described in which the gradation value increases and while overdrive drive is performed over a plurality of frame periods, the gradation value further increases. In the second example, the gradation value is first 0 and changes to 64 in the fourth frame and changes to 128 in the eighth frame. In this case, the liquid crystal display device 10 performs, in the fourth frame to the seventh frame, the same overdrive drive as that in the first example, and stops the overdrive drive and performs new overdrive drive over seven frame periods from the eighth frame to the fourteenth frame.

[0061] In the eighth frame (a shaded portion on the right side in Fig. 5A), since Din(n)=128 and Din(n-1)=64, the amount of gradation change is +64. The gradation change detection circuit 26 determines that there is a change in gradation and thus outputs Cmp*=1. Since Cmp*=1, a gradation value before change Din (hold) ** stored in the first frame memory 21 is updated to 64 using a gradation value Din(n-1)* outputted from the one-clock delay circuit 24. The hold count calculation circuit 27 outputs Cnt**=1, and the hold count stored in the second frame memory 22 is updated to 1. To the emphasis conversion circuit 28 are inputted Din(n)**=128, Din(hold)**=64, and Cnt**=1. Since two gradation values are both included in the representative values in the LUT 31, the emphasis conversion circuit 28 outputs a value read from the LUT 31 as an output gradation value Dout(n) without using the arithmetic circuit 32. As a result, Dout (n) =166. For subsequent frames, likewise, in the ninth frame to the thirteenth frame, output gradation values Dout(n) are 137, 133, 131, 129, and 129, respectively. In each frame in and after the fourteenth frame, Dout(n)=128.

[0062] In the second example, the output gradation value changes as shown in Fig. 5B, and the luminance increases in the fourth frame, becomes substantially constant from the fifth frame to the seventh frame, further increases in the eighth frame, and becomes substantially constant in and after the ninth frame, as shown in Fig. 5C. As such, in the second example, too, double optical responsivity caused by overdrive drive does not occur.

[0063] In the third example (see Figs. 6A to 6C), the case will be described in which the gradation value decreases and while overdrive drive is performed over a plurality of frame periods, the gradation value increases. In the third example, the gradation value is first 128 and changes to 64 in the fourth frame and changes to 128 in the eighth frame. In this case, the liquid crystal display device 10 performs overdrive drive in the fourth frame to the seventh frame, and stops the overdrive drive and performs new overdrive drive over seven frame periods from the eighth frame to the fourteenth frame.

[0064] In the third example, the output gradation value changes as shown in Fig. 6B, and the luminance decreases in the fourth frame, becomes substantially constant from the fifth frame to the seventh frame, increases in the eighth frame, and becomes substantially constant in and after the ninth frame, as shown in Fig. 6C. As such, in the third example, too, double optical responsivity caused by overdrive drive does not occur.

[0065] In the fourth example (see Figs. 7A to 7C), the case will be described in which the gradation value increases and while overdrive drive is performed over a plurality of frame periods, the gradation value increases slightly due to the influence of noise. In the fourth example, the gradation value is first 0 and changes to 64 in the fourth frame and changes to 67 in the seventh frame for only one frame period due to the influence of noise.

[0066] In the seventh frame (a shaded portion on the right side in Fig. 7A), since Din.(n)=67 and Din(n-1)=64, the amount of gradation change is +3. The gradation change detection circuit 26 determines that there is no change in gradation and thus outputs Cmp*=0. Since Cmp*=0, a gradation value before change Din (hold) ** stored in the first frame memory 21 is held without being updated. The hold count calculation circuit 27 adds 1 to the hold count (the value is 3) outputted from the second frame memory 22 and outputs Cnt**=4, and the hold count stored in the second frame memory 22 is updated to 4. To the emphasis conversion circuit 28 are inputted Din(n)**=67, Din(hold)**=0, and Cnt**=4. Though the value of Din (hold) ** is included in the representative values in the LUT 31, the value of Din(n)** is not included in the representative values in the LUT 31. The emphasis conversion circuit 28 refers to the LUT 31 by changing three values {Din(n)**, Din(hold)**, Cnt**} in two ways, i.e., { 64, 0, 4} and {96, 0, 4}, and performs, by the arithmetic circuit 32, a linear interpolation operation on obtained two LUT outputs. As a result, Dout(n)=69. Output gradation values Dout(n) in and after the eighth frame are the same as those in the first example.

[0067] In the fourth example, the output gradation value changes as shown in Fig. 7B, and the luminance changes, as shown in Fig. 7C, in substantially the same manner as in the second example. Even in the fourth example in which the gradation value changes slightly due to the influence of noise in the above-described manner, double optical responsivity caused by overdrive drive does not occur.

[0068] Effects brought about by the liquid crystal display device 10 according to the present embodiment will be described below in comparison with conventional liquid crystal display devices. As described above, in a conventional liquid crystal display device performing overdrive drive, when the gradation value of a pixel increases, the drive voltage of the pixel changes as shown in Fig. 10A, and the luminance of the pixel changes as shown in Fig. 10B. In a liquid crystal display device shown in Fig. 11, when the gradation value of a pixel increases, the drive voltage of the pixel changes as shown in Fig. 12A, and the luminance of the pixel changes as shown in Fig. 12B. In these liquid crystal display devices, double optical responsivity where the luminance of a pixel increases once and decreases thereafter and increases again occurs.

[0069] Fig. 8A is a diagram showing changes in the drive voltage of a pixel for when the gradation value of the pixel increases in the liquid crystal display device 10 according to the present embodiment. As shown in Fig. 8A, in the first frame period occurring after the change of the gradation value (a frame period starting from time 0), a voltage higher than a voltage required to obtain a desired luminance is applied to a pixel circuit 15 in the liquid crystal panel 14. In the next frame period (a frame period starting from time T), a voltage lower than the voltage applied in the immediately previous frame period and higher than a voltage to be applied when a sufficient period of time has elapsed (hereinafter, referred to as a final voltage) is applied to the pixel circuit 15. In the next frame period (a frame period starting from time 2T), a voltage further lower than the voltage applied in the immediately previous frame period and higher than the final voltage is applied to the pixel circuit 15. Thereafter, in each frame period before the number of frames reaches a maximum value of the hold count of 7, a voltage lower than or equal to a voltage applied in an immediately previous frame period and higher than or equal to the final voltage is applied to the pixel circuit 15.

[0070] When the drive voltage of a pixel changes as shown in Fig. 8A, the luminance of the pixel changes as shown in Fig. 8B. Specifically, the luminance reaches a desired level in the first frame period occurring after the change of a gradation value, and is maintained at substantially that level in subsequent frame periods. Therefore, in the liquid crystal display device 10, double optical responsivity does not occur when the luminance of a pixel increases. For the same reason, in the liquid crystal display device 10, when the gradation value of a pixel decreases, too, double optical responsivity does not occur. As such, according to the liquid crystal display device 10 according to the present embodiment, double optical responsivity occurring due to overdrive drive can be prevented.

[0071] As described above, a liquid crystal display device 10 according to the present embodiment includes a liquid crystal panel 14; a first frame memory 21 (first storage unit) that stores, when a gradation value of a pixel included in an input video signal has been changed from the previous frame, a gradation value before change, for each pixel; a hold count calculation circuit 27 that determines, for each pixel, the hold count (the number of frames inputted after a change of a gradation value) ; a second frame memory 22 (second storage unit) that stores the hold counts determined by the hold count calculation circuit 27; an emphasis conversion circuit 28 that obtains a video signal (emphasis video signal) that compensates for the optical response characteristics of the liquid crystal panel 14 based on the input video signal, the gradation values before change which are stored in the first frame memory 21, and the hold counts determined by the hold count calculation circuit 27; and a liquid crystal drive circuit 13 that drives the liquid crystal panel 14 based on the emphasis video signal.

[0072] As such, in the liquid crystal display device 10 according to the present embodiment, an emphasis video signal that compensates for the optical response characteristics of the liquid crystal panel 14 is obtained based on an input video signal, gradation values before change, and the hold counts, and the liquid crystal panel 14 is driven based on the emphasis video signal. Accordingly, by obtaining an emphasis video signal according to the elapsed time after the change of gradation value by referring to the hold counts, the optical response characteristics of the liquid crystal panel 14 are favorably compensated for, enabling to prevent double optical responsivity occurring due to overdrive drive.

[0073] In addition, the liquid crystal display device 10 further includes a third frame memory 23 (third storage unit) that stores one frame of the input video signal and outputs a video signal of the previous frame; and a gradation change detection circuit 26 that compares the input video signal with the video signal of the previous frame outputted from the third frame memory 23 to determine, for each pixel, whether a gradation value has been changed from the previous frame. Accordingly, a determination as to whether a gradation value has been changed from the previous frame can be easily made using the third frame memory 23 and the gradation change detection circuit 26.

[0074] When the gradation value of a pixel is changed by a value greater than or equal to a predetermined value between the input video signal and the video signal of the previous frame outputted from the third frame memory 23, the gradation change detection circuit 26 determines that the gradation value has been changed from the previous frame. Accordingly, a situation can be prevented where, when a gradation value slightly fluctuates due to the influence of noise, display is performed with the noise being emphasized by overdrive drive.

[0075] A maximum value of the hold counts determined by the hold count calculation circuit 27 is 3 or more (here, 7). Accordingly, by referring to the hold counts whose maximum value is 3 or more, elapsed time after the change of gradation value is measured for at least three frame periods, and an emphasis video signal according to the elapsed time is obtained. By this, the optical response characteristics of the liquid crystal panel 14 are favorably compensated for, enabling to prevent double optical responsivity occurring due to overdrive drive.

[0076] The emphasis conversion circuit 28 obtains an emphasis video signal where the changes in gradation values are emphasized more than those in the input video signal, and makes the degree of emphasis smaller with larger hold counts determined by the hold count calculation circuit 27. As such, when an emphasis video signal is obtained by performing a process of emphasizing changes in gradation values on an input video signal, the degree of emphasis is made smaller with longer elapsed time after the change of gradation value by referring to the hold counts. By this, an emphasis video signal capable of favorably compensating for the optical response characteristics of the liquid crystal panel 14 can be obtained. By driving the liquid crystal panel 14 based on the emphasis video signal, double optical responsivity occurring due to overdrive drive can be prevented.

[0077] Double optical responsivity occurs when a liquid crystal panel has a response speed slower than one frame period. Furthermore, according to the liquid crystal display device 10 according to the present embodiment, even when a liquid crystal panel with a response speed slower than two frame periods is used, double optical responsivity occurring over two frame periods or more due to overdrive drive can be prevented. In particular, in an MVA-type liquid crystal panel where an alignment film surface is not subjected to a rubbing process as a domain control means and liquid crystal molecules are pretilted at a small angle by protrusions, etc., provided on a part of an electrode, double optical responsivity is likely to occur. According to the liquid crystal display device 10 according to the present embodiment, even when an MVA-type liquid crystal panel is used, double optical responsivity occurring over two frame periods or more due to overdrive drive can be prevented.

INDUSTRIAL APPLICABILITY

[0078] An image display device of the present invention has a feature that the device can prevent double optical responsivity occurring due to overdrive drive, and thus, can be used as various image display devices such as liquid crystal display devices.

DESCRIPTION OF REFERENCE NUMERALS

[0079]

10: LIQUID CRYSTAL DISPLAY DEVICE
11: TIMING CONTROL CIRCUIT
12: OVERDRIVE CIRCUIT
13: LIQUID CRYSTAL DRIVE CIRCUIT
14: LIQUID CRYSTAL PANEL
15: PIXEL CIRCUIT
21: FIRST FRAME MEMORY
22: SECOND FRAME MEMORY
23: THIRD FRAME MEMORY
24: ONE-CLOCK DELAY CIRCUIT
25: TWO-CLOCK DELAY CIRCUIT
26: GRADATION CHANGE DETECTION CIRCUIT
27: HOLD COUNT CALCULATION CIRCUIT
28: EMPHASIS CONVERSION CIRCUIT
31: LUT
32: ARITHMETIC CIRCUIT

Claims

1. An image display device (10) configured to perform signal processing on a video signal (Vin) and thereby to display an image, the image display device (10) comprising:

a display panel (14);
a first storage unit (23) configured to store one frame of the input video signal (Vin) and to output a video signal of the previous frame; and
a gradation change detection unit (26) configured to compare the input video signal (Vin) with the video signal of the previous frame output from the first storage unit (23) to determine, for each pixel, whether a gradation value (Din) changes from the previous frame.
a hold count calculation unit (27) configured to

determine, for each pixel, a hold count (Cnt**) indicating a number of frames input after the change of the gradation value by setting the hold count (Cnt**) to one if the gradation value (Din) changes and adding one to the hold count (Cnt**) if the gradation value (Din) does not change;
a second storage unit (22) configured to store the hold counts (Cnt**) determined by the hold count calculation unit (27);
an emphasis conversion unit (28) configured to determine an emphasis video signal; and
a drive unit (13) configured to drive the display panel (14) based on the emphasis video signal;
characterized by
a third storage unit (21) configured to store, for each pixel and in case where a gradation value (Din) of a pixel included in an input video signal (Vin) changes from the previous frame output from the first storage unit as determined by the change detection unit, the gradation value (Din) before change; and
wherein the emphasis conversion unit (28) is configured to determine the emphasis video signal based on the input video signal (Vin), the gradation values (Din(hold)**) before change which are stored in the third storage unit (21), and the hold counts (Cnt**) determined by the hold count calculation unit (27), the emphasis video signal (Dout(n)) compensating for optical response characteristics of the display panel (14).

2. The image display device (10) according to claim 1, wherein in case where a gradation value (Din) of a pixel is changed by a value greater than or equal to a predetermined value between the input video signal (Vin) and the video signal of the previous frame outputted from the first storage unit (23), the gradation change detection unit (26) is configured to determine that the gradation value (Din) changes from the previous frame.

3. The image display device (10) according to claim 1, wherein a maximum value of the hold counts (Cnt**) determined by the hold count calculation unit (27) is 3 or more.

4. The image display device (10) according to claim 1, wherein the emphasis conversion unit (28) is configured to determine the emphasis video signal where the temporal changes in gradation values (Din) are emphasized more than those in the input video signal (Vin), and is configured to make a degree of emphasis smaller with larger hold counts (Cnt**) determined by the hold count calculation unit (27).

5. The image display device (10) according to claim 4, wherein the emphasis conversion unit (28) includes a look up table (31) and is configured to determine the emphasis video signal using the look up table (31).

6. The image display device (10) according to claim 4, wherein the emphasis conversion unit (28) includes an arithmetic circuit (32), and the emphasis conversion unit (28) is configured to determine the emphasis video signal using the arithmetic circuit (32).

7. The image display device (10) according to claim 4, wherein the emphasis conversion unit (28) includes a look up table (31) and an arithmetic circuit (32), and the emphasis conversion unit (28) is configured to determine the emphasis video signal using the look up table (31) and the arithmetic circuit (32).

8. The image display device (10) according to claim 1, wherein the display panel (14) has a response speed slower than two frame periods.

9. The image display device (10) according to claim 8, wherein the display panel (14) is an multi-domain vertical alignment-type liquid crystal panel.

10. An image display method for performing signal processing on a video signal and thereby displaying an image on a display panel (14), the method comprising the steps of:

storing in a first storage unit (23) a previous frame of the input video signal (Vin);
comparing the input video signal (Vin) with the video signal of the previous frame to determine, for each pixel, whether a gradation value (Din) changes from the previous frame;
determining, for each pixel, a hold count indicating a number of frames inputted after the change of the gradation value (Din) by setting the hold count (Cnt**) to one if the gradation value (Din) changes and adding one to the hold count (Cnt**) if the gradation value (Din) does not change;
storing the determined hold counts (Cnt**) within a second storage unit (22);
determining an emphasis video signal; and
driving the display panel (14) based on the emphasis video signal;
characterized by
storing in a third storage unit (21) for each pixel, in case where a gradation value (Din) of a pixel included in aninput video signal (Vin) changes from the previous frame output from the first storage unit as determined by the comparing step, the gradation value (Din) before change; and
in that the emphasis video signal is based on the input video signal (Vin), the stored gradation

values before change within the third storage unit (21), and the determined hold counts (Cnt**) within the second sorage unit (22), the emphasis video signal compensating for optical response characteristics of the display panel (14).

Patentansprüche

1. Bildanzeigevorrichtung (10), die zum Durchführen von Signalverarbeitung an einem Videosignal (Vin) und dadurch zum Anzeigen eines Bildes konfiguriert ist, wobei die Bildanzeigevorrichtung (10) Folgendes umfasst:

ein Anzeigefeld (14);
eine erste Speichereinheit (23), die zum Speichern eines Frames des Eingangsvideosignals (Vin) und zum Ausgeben eines Videosignals des vorhergehenden Frames konfiguriert ist; und
eine Abstufungsänderungserkennungseinheit (26), die zum Vergleichen des Eingangsvideosignals (Vin) mit dem Videosignal der vorhergehenden Frameausgabe von der ersten Speichereinheit (23) konfiguriert ist, um für jedes Pixel zu bestimmen, ob sich ein Abstufungswert (Din) von dem vorhergehenden Frame ändert;
eine Haltezählwert-Berechnungseinheit (27), die zum Bestimmen eines Haltezählwertes (Cnt**) für jedes Pixel, durch welchen eine Anzahl von Frames, die nach der Änderung des Abstufungswertes eingegeben wurden, angeben wird, indem der Haltezählwert (Cnt**) auf Eins eingestellt wird, falls sich der Abstufungswert (Din) ändert, und Eins zu dem Haltezählwert (Cnt**) addiert wird, falls sich der Abstufungswert (Din) nicht ändert, konfiguriert ist;
eine zweite Speichereinheit (22), die zum Speichern der Haltezählwerte (Cnt**), die durch die Haltezählwert-Berechnungseinheit (27) bestimmt wurden, konfiguriert ist;
eine Schwerpunktumwandlungseinheit (28), die zum Bestimmen eines Schwerpunktvideosignals konfiguriert ist; und
eine Antriebseinheit (13), die zum Antreiben des Anzeigefeldes (14) auf der Grundlage des Schwerpunktvideosignals konfiguriert ist;
gekennzeichnet durch
eine dritte Speichereinheit (21), die, für jedes Pixel und in dem Fall, bei welchem sich ein Abstufungswert (Din) eines Pixels, das in einem Eingangsvideosignal (Vin) enthalten ist, von dem vorhergehenden Frame, das von der ersten Speichereinheit ausgegeben wird, ändert, wie **durch** die Änderungserkennungseinheit bestimmt, zum Speichern des Abstufungswertes (Din) vor der Änderung konfiguriert ist; und
wobei die Schwerpunktumwandlungseinheit (28) zum Bestimmen des Schwerpunktvideosignals auf der Grundlage des Eingangsvideosignals (Vin), der Abstufungswerte (Din(hold)**) vor einer Änderung, welche in der dritten Speichereinheit (21) gespeichert sind, und der Haltezählwerte (Cnt**), die **durch** die Haltezählwert-Berechnungseinheit (27) bestimmt werden, konfiguriert ist, wobei das Schwerpunktvideosignal (Dout(n)) optische Reaktionseigenschaften des Anzeigefeldes (14) kompensiert.

2. Bildanzeigevorrichtung (10) nach Anspruch 1, wobei in dem Fall, bei welchem sich ein Abstufungswert (Din) eines Pixels um einem Wert ändert, der größer als oder gleich einem vorbestimmten Wert zwischen dem Eingangsvideosignal (Vin) und dem Videosignal des vorhergehenden Frames ausgegeben von der ersten Speichereinheit (23) ist, die Abstufungsänderungserkennungseinheit (26) zum Bestimmen dessen konfiguriert ist, dass sich der Abstufungswert (Din) von dem vorhergehenden Frame ändert.

3. Bildanzeigevorrichtung (10) nach Anspruch 1, wobei ein Maximalwert der Haltezählwerte (Cnt**) bestimmt durch die Haltezählwert-Berechnungseinheit (27) 3 oder mehr ist.

4. Bildanzeigevorrichtung (10) nach Anspruch 1, wobei die Schwerpunktumwandlungseinheit (28) zum Bestimmen des Schwerpunktvideosignals, bei welchem die zeitlichen Änderungen in Abstufungswerten (Din) mehr hervorgehoben sind als diejenigen in dem Eingangsvideosignal (Vin), konfiguriert ist und dazu konfiguriert ist, ein Schwerpunktausmaß bei größeren Haltezählwerten (Cnt**), bestimmt durch die Haltezählwert-Berechnungseinheit (27), kleiner zu machen.

5. Bildanzeigevorrichtung (10) nach Anspruch 4, wobei die Schwerpunktumwandlungseinheit (28) eine Nachschlagetabelle (31) beinhaltet und zum Bestimmen des Schwerpunktvideosignals unter Verwendung der Nachschlagetabelle (31) konfiguriert ist.

6. Bildanzeigevorrichtung (10) nach Anspruch 4, wobei die Schwerpunktumwandlungseinheit (28) eine Rechenschaltung (32) beinhaltet und die Schwerpunktumwandlungseinheit (28) zum Bestimmen des Schwerpunktvideosignals unter Verwendung der Rechenschaltung (32) konfiguriert ist.

7. Bildanzeigevorrichtung (10) nach Anspruch 4, wobei die Schwerpunktumwandlungseinheit (28) eine Nachschlagetabelle (31) und eine Rechenschaltung (32) beinhaltet und die Schwerpunktumwandlungseinheit (28) zum Bestimmen des Schwerpunktvideosignals unter Verwendung der Nachschlagetabelle

(31) und der Rechenschaltung (32) konfiguriert ist.

8. Bildanzeigevorrichtung (10) nach Anspruch 1, wobei das Anzeigefeld (14) eine Reaktionsgeschwindigkeit aufweist, die langsamer als die Dauer zweier Frames ist.

9. Bildanzeigevorrichtung (10) nach Anspruch 8, wobei das Anzeigefeld (14) eine Mehrdomänen-Flüssigkristallanzeige mit vertikaler Ausrichtung ist.

10. Bildanzeigeverfahren zum Durchführen von Signalverarbeitung an einem Videosignal und dadurch Anzeigen eines Bildes auf einem Anzeigefeld (14), wobei das Verfahren folgende Schritte umfasst:

Speichern, in einer ersten Speichereinheit (23), eines vorhergehenden Frames des Eingangsvideosignals (Vin); Vergleichen des Eingangsvideosignals (Vin) mit dem Videosignal des vorhergehenden Frames, um für jedes Pixel zu bestimmen, ob sich ein Abstufungswert (Din) von dem vorhergehenden Frame ändert;
Bestimmen, für jedes Pixel, eines Haltezählwertes, der eine Anzahl von Frames angibt, die nach der Änderung des Abstufungswertes (Din) eingegeben wurden, durch Einstellung des Haltezählwertes (Cnt**) auf Eins, falls sich der Abstufungswert (Din) ändert, und Addieren von Eins zu dem Haltezählwert (Cnt**), falls sich der Abstufungswert (Din) nicht ändert;
Speichern der bestimmten Haltezählwerte (Cnt**) innerhalb einer zweiten Speichereinheit (22); Bestimmen eines Schwerpunktvideosignals; und
Antreiben des Anzeigefeldes (14) auf der Grundlage des Schwerpunktvideosignals;
gekennzeichnet durch das
Speichern, für jedes Pixel, in dem Fall, bei welchem sich ein Abstufungswert (Din) eines Pixels, das in einem Eingangsvideosignal (Vin) enthalten ist, von dem vorhergehenden Frame, das von der ersten Speichereinheit ausgegeben wird, ändert, wie **durch** den Vergleichsschritt bestimmt, des Abstufungswertes (Din) vor der Änderung in einer dritten Speichereinheit (21); und
dadurch, dass das Schwerpunktvideosignal auf dem Eingangsvideosignal (Vin), den gespeicherten Abstufungswerten vor einer Änderung innerhalb der dritten Speichereinheit (21) und den bestimmten Haltezählwerten (Cnt**) innerhalb der zweiten Speichereinheit (22) basiert, wobei das Schwerpunktvideosignal optische Reaktionseigenschaften des Anzeigefeldes (14) kompensiert.

Revendications

1. Dispositif d'affichage d'image (10) configuré pour exécuter un traitement de signal sur un signal vidéo (Vin) et ainsi afficher une image, le dispositif d'affichage d'image (10) comprenant :

un écran d'affichage (14) ;
une première unité de stockage (23) configurée pour stocker une trame du signal vidéo d'entrée (Vin) et pour délivrer en sortie un signal vidéo de la trame précédente ; et
une unité de détection de changement de gradation (26) configurée pour comparer le signal vidéo d'entrée (Vin) au signal vidéo de la trame précédente délivré en sortie de la première unité de stockage (23) pour déterminer, pour chaque pixel, si une valeur de gradation (Din) change par rapport à la trame précédente.
une unité de calcul de compte maintenu (27) configurée pour déterminer, pour chaque pixel, un compte maintenu (Cnt**) indiquant un nombre de trames d'entrée après le changement de la valeur de gradation en fixant le compte maintenu (Cnt**) à un si la valeur de gradation (Din) change et en ajoutant un au compte maintenu (Cnt**) si la valeur de gradation (Din) ne change pas ;
une deuxième unité de stockage (22) configurée pour stocker les comptes maintenus (Cnt**) déterminés par l'unité de calcul de compte maintenu (27) ;
une unité de conversion d'accentuation (28) configurée pour déterminer un signal vidéo d'accentuation ; et
une unité de commande (13) configurée pour commander l'écran d'affichage (14) sur la base du signal vidéo d'accentuation ;
caractérisé par :

une troisième unité de stockage (21) configurée pour stocker, pour chaque pixel et au cas où une valeur de gradation (Din) d'un pixel compris dans un signal vidéo d'entrée (Vin) change par rapport à la trame précédente délivrée en sortie de la première unité de stockage comme cela est déterminé par l'unité de détection de changement, la valeur de gradation (Din) avant un changement ; et
où l'unité de conversion d'accentuation (28) est configurée pour déterminer le signal vidéo d'accentuation sur la base du signal vidéo d'entrée (Vin), les valeurs de gradation (Din(hold)**) avant changement qui sont stockées dans la troisième unité de stockage (21), et les comptes maintenus (Cnt**) déterminés par l'unité de calcul de compte

maintenu (27), le signal vidéo d'accentuation (Dout(n)) compensant les caractéristiques de réponse optiques de l'écran d'affichage (14).

2. Dispositif d'affichage d'image (10) selon la revendication 1, dans lequel au cas où une valeur de gradation (Din) d'un pixel est changée en une valeur supérieure ou égale à une valeur prédéterminée entre le signal vidéo d'entrée (Vin) et le signal vidéo de la trame précédente délivrée en sortie de la première unité de stockage (23), l'unité de détection de changement de gradation (26) est configurée pour déterminer que la valeur de gradation (Din) change par rapport à la trame précédente.

3. Dispositif d'affichage d'image (10) selon la revendication 1, dans lequel une valeur maximale des comptes maintenus, déterminée par l'unité de calcul de compte maintenu (27), est égale à 3 ou plus.

4. Dispositif d'affichage d'image (10) selon la revendication 1, dans lequel l'unité de conversion d'accentuation (28) est configurée pour déterminer le signal vidéo d'accentuation où les changement temporels dans des valeurs de gradation (Din) sont plus accentués que ceux dans le signal vidéo d'entrée (Vin), et est configurée pour rendre un degré d'accentuation plus petit avec des comptes maintenus (Cnt**) plus importants déterminés par l'unité de calcul de compte maintenu (27).

5. Dispositif d'affichage d'image (10) selon la revendication 4, dans lequel l'unité de conversion d'accentuation (28) comprend une table de consultation (31) et est configurée pour déterminer le signal vidéo d'accentuation au moyen de la table de consultation (31).

6. Dispositif d'affichage d'image (10) selon la revendication 4, dans lequel l'unité de conversion d'accentuation (28) comprend un circuit arithmétique (32), et l'unité de conversion d'accentuation (28) est configurée pour déterminer le signal vidéo d'accentuation au moyen du circuit arithmétique (32).

7. Dispositif d'affichage d'image (10) selon la revendication 4, dans lequel l'unité de conversion d'accentuation (28) comprend une table de consultation (31) et un circuit arithmétique (32), et l'unité de conversion d'accentuation (28) est configurée pour déterminer le signal vidéo d'accentuation au moyen de la table de consultation (31) et du circuit arithmétique (32).

8. Dispositif d'affichage d'image (10) selon la revendication 1, dans lequel l'écran d'affichage (14) a une vitesse de réponse plus lente que deux périodes de trame.

9. Dispositif d'affichage d'image (10) selon la revendication 8, dans lequel l'écran d'affichage (14) est un écran à cristaux liquides de type à alignement vertical à domaine multiple.

10. Procédé d'affichage d'image pour exécuter un traitement de signal sur un signal vidéo et ainsi afficher une image sur un écran d'affichage (14), le procédé comprenant les étapes suivantes :

stocker, sur une première unité de stockage (23), une trame précédente du signal vidéo d'entrée (Vin) ;
comparer le signal vidéo d'entrée (Vin) au signal vidéo de la trame précédente pour déterminer, pour chaque pixel, si une valeur de gradation (Din) change par rapport à la trame précédente ;
déterminer, pour chaque pixel, un compte maintenu indiquant un nombre de trames entrées après le changement de la valeur de gradation (Din) en fixant le compte maintenu (Cnt**) à un si la valeur de gradation (Din) change et en ajoutant un au compte maintenu (Cnt**) si la valeur de gradation (Din) ne change pas ;
stocker les comptes maintenus (Cnt**) déterminés dans une deuxième unité de stockage (22) ;
déterminer un signal vidéo d'accentuation ; et
commander l'écran d'affichage (14) sur la base du signal vidéo d'accentuation ;
caractérisé par les étapes suivantes :

stocker dans une troisième unité de stockage (21), pour chaque pixel, au cas où une valeur de gradation (Din) d'un pixel compris dans un signal vidéo d'entrée (Vin) change par rapport à la trame précédente délivrée en sortie de la première unité de stockage comme cela est déterminé par l'unité de détection de changement, la valeur de gradation (Din) avant changement ; et
caractérisé en ce que le signal vidéo d'accentuation est basé sur le signal vidéo d'entrée (Vin), les valeurs de gradation stockées avant changement dans la troisième unité de stockage (21), et les comptes maintenus (Cnt**) déterminés dans la deuxième unité de stockage (22), le signal vidéo d'accentuation compensant des caractéristiques de réponse optiques de l'écran d'affichage (14).

Fig. 1

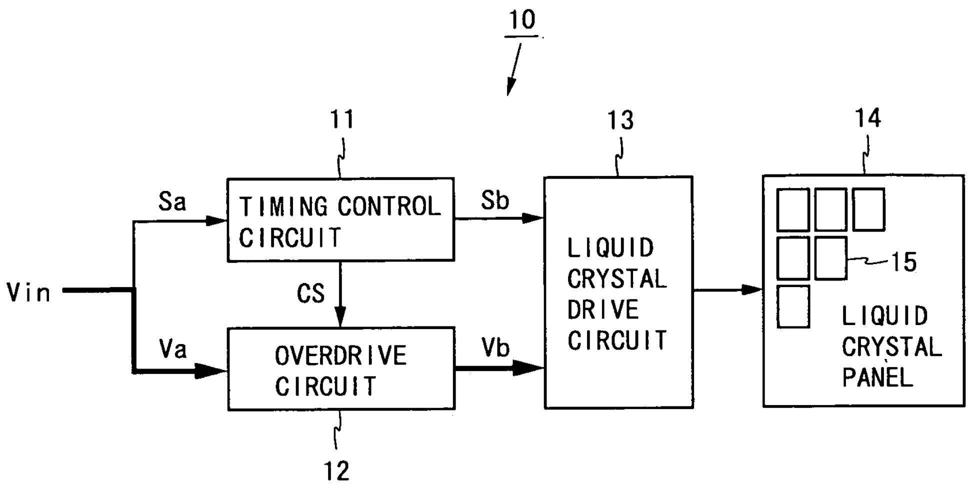

10
11
13
14
Sa
TIMING CONTROL CIRCUIT
Sb
LIQUID CRYSTAL DRIVE CIRCUIT
15
Vin
CS
LIQUID CRYSTAL PANEL
Va
OVERDRIVE CIRCUIT
Vb
12

Fig. 2

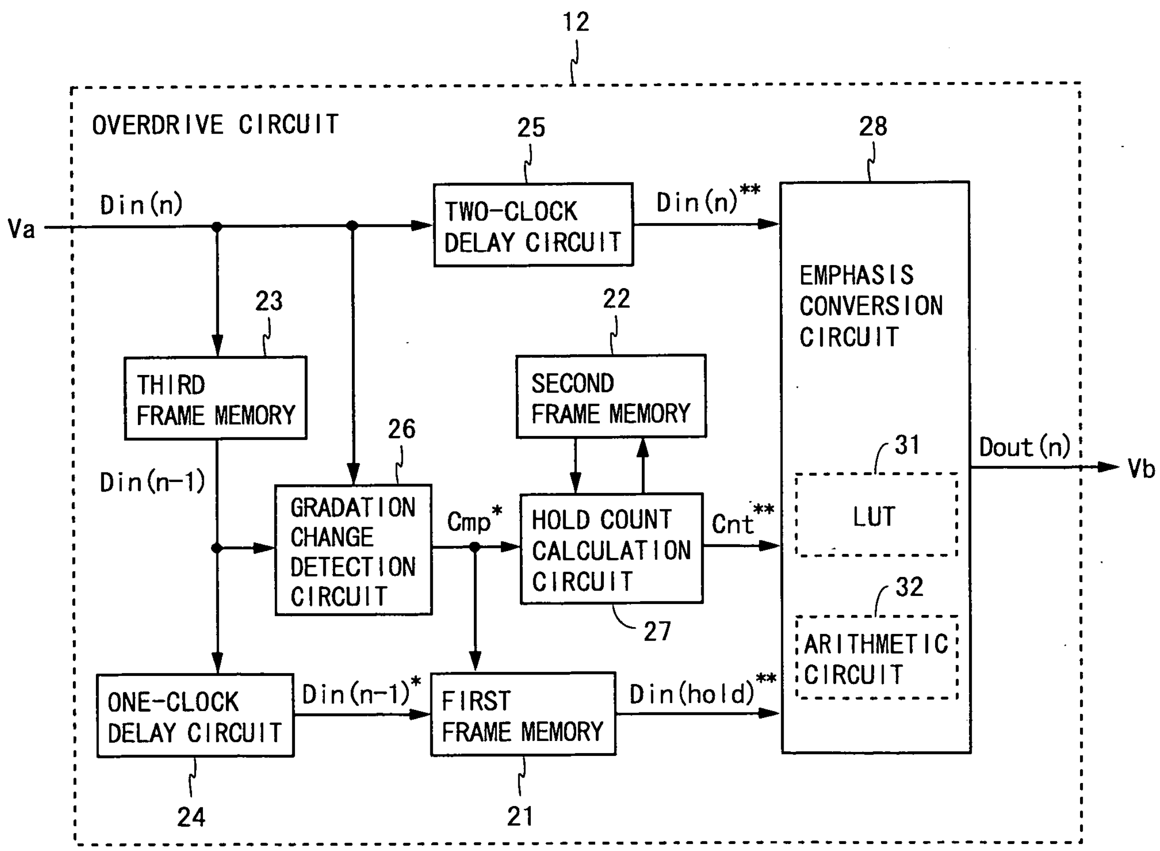

12
OVERDRIVE CIRCUIT
25
28
Va
Din(n)
TWO-CLOCK DELAY CIRCUIT
Din(n)**
23
22
EMPHASIS CONVERSION CIRCUIT
THIRD FRAME MEMORY
SECOND FRAME MEMORY
26
31
Din(n-1)
Dout(n)
Vb
GRADATION CHANGE DETECTION CIRCUIT
Cmp*
HOLD COUNT CALCULATION CIRCUIT
Cnt**
LUT
27
32
ARITHMETIC CIRCUIT
ONE-CLOCK DELAY CIRCUIT
Din(n-1)*
FIRST FRAME MEMORY
Din(hold)**
24
21

Fig. 3

HOLD COUNT Cnt**	GRADATION VALUE BEFORE CHANGE Din(hold)**	CURRENT FRAME GRADATION VALUE Din(n)**								
		0	32	64	96	128	160	192	224	255
1	0	0	90	*160*	192	210	225	238	248	255
	32	0	32	90	154	192	215	233	246	255
	64	0	25	64	120	*166*	200	227	243	255
	96									
	128									
	160									
	192									
	224									
	255									
2	0			*76*						
	⋮									
	255									
3	0			*68*						
	⋮									
	255									
4	0			*66*						
	⋮									
	255									
5	0			*65*						
	⋮									
	255									
6	0			*65*						
	⋮									
	255									
7	0			*65*						
	⋮									
	255									

Fig. 4A

TIME (FRAME)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Din(n)	0	0	0	64	64	64	64	64	64	64	64	64	64	64	64	64	64	64
Din(n-1)	0	0	0	0	64	64	64	64	64	64	64	64	64	64	64	64	64	64
Cmp*	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Din(n-1)*	0	0	0	0	64	64	64	64	64	64	64	64	64	64	64	64	64	64
Din(n)**	0	0	0	64	64	64	64	64	64	64	64	64	64	64	64	64	64	64
Cnt**	0	0	0	1	2	3	4	5	6	7	0	0	0	0	0	0	0	0
Din(hold)**	32	32	32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Dout(n)	0	0	0	160	76	68	66	65	65	65	64	64	64	64	64	64	64	64

Fig. 4B

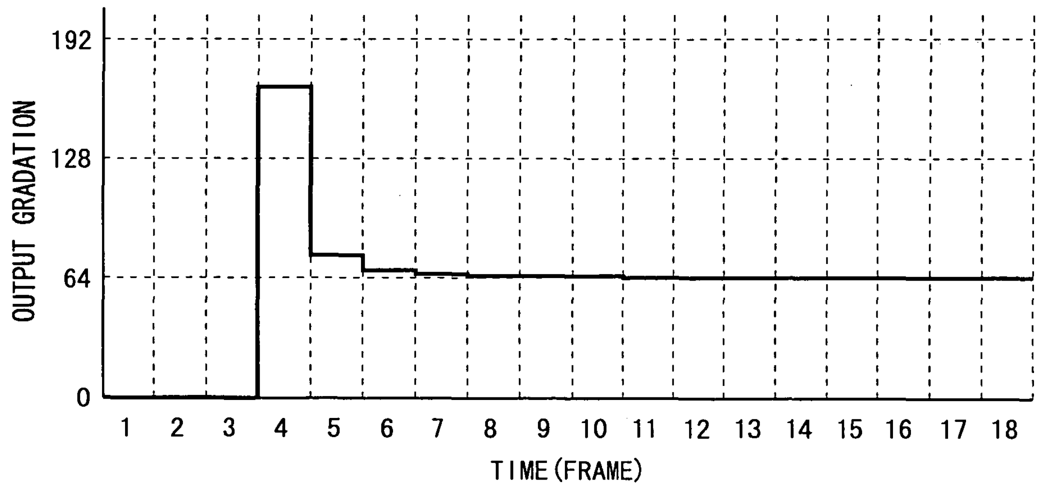


Fig. 4C

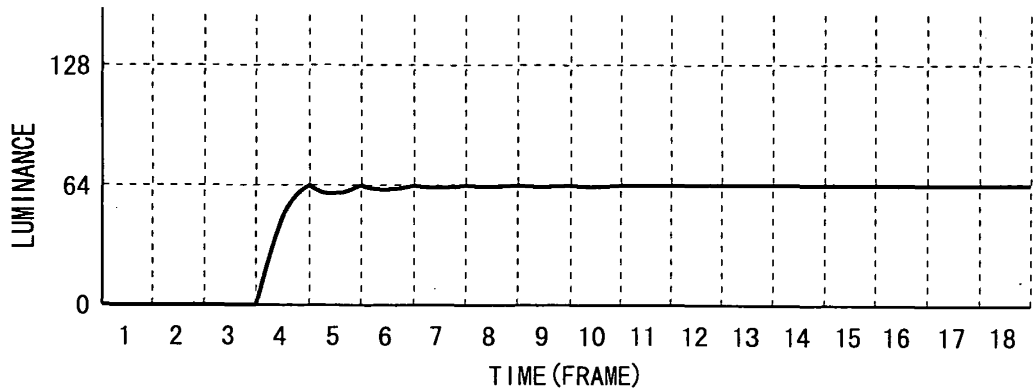


Fig. 5A

TIME (FRAME)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Din(n)	*0*	*0*	*0*	*64*	*64*	*64*	*64*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*
Din(n-1)	0	0	0	0	64	64	64	64	128	128	128	128	128	128	128	128	128	128
Cmp*	0	0	0	*1*	0	0	0	*1*	0	0	0	0	0	0	0	0	0	0
Din(n-1)*	0	0	0	0	64	64	64	64	128	128	128	128	128	128	128	128	128	128
Din(n)**	*0*	*0*	*0*	*64*	*64*	*64*	*64*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*
Cnt**	*0*	*0*	*0*	*1*	*2*	*3*	*4*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*0*	*0*	*0*	*0*
Din(hold)**	32	32	32	*0*	*0*	*0*	*0*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	64	64	64	64
Dout(n)	*0*	*0*	*0*	*160*	*76*	*68*	*66*	*166*	*137*	*133*	*131*	*129*	*129*	*128*	*128*	*128*	*128*	*128*

Fig. 5B

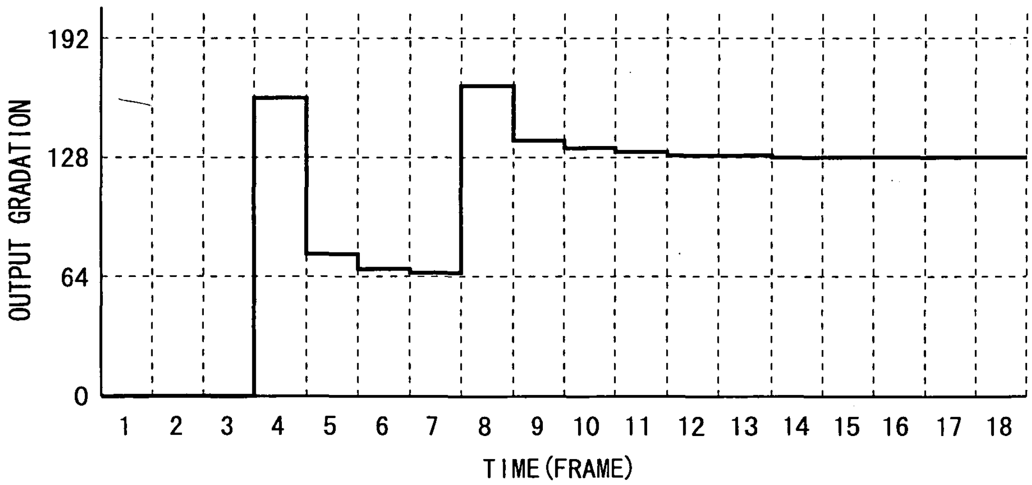


Fig. 5C

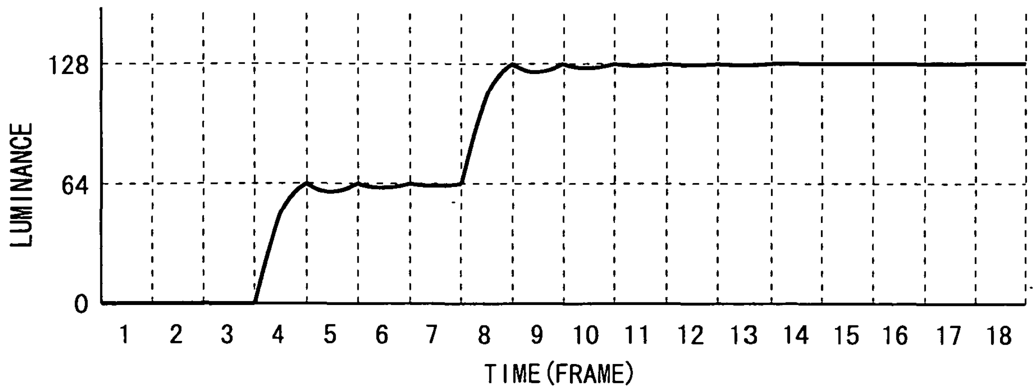


Fig. 6A

TIME (FRAME)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Din(n)	*128*	*128*	*128*	*64*	*64*	*64*	*64*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*
Din(n-1)	0	0	0	0	64	64	64	64	128	128	128	128	128	128	128	128	128	128
Cmp*	0	0	0	*1*	0	0	0	*1*	0	0	0	0	0	0	0	0	0	0
Din(n-1)*	0	0	0	0	64	64	64	64	128	128	128	128	128	128	128	128	128	128
Din(n)**	*128*	*128*	*128*	*64*	*64*	*64*	*64*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*	*128*
Cnt**	*0*	*0*	*0*	*1*	*2*	*3*	*4*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*0*	*0*	*0*	*0*
Din(hold)**	0	0	0	*128*	*128*	*128*	*128*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	64	64	64	64
Dout(n)	*0*	*0*	*0*	*32*	*62*	*64*	*64*	*166*	*137*	*133*	*131*	*129*	*129*	*128*	*128*	*128*	*128*	*128*

Fig. 6B

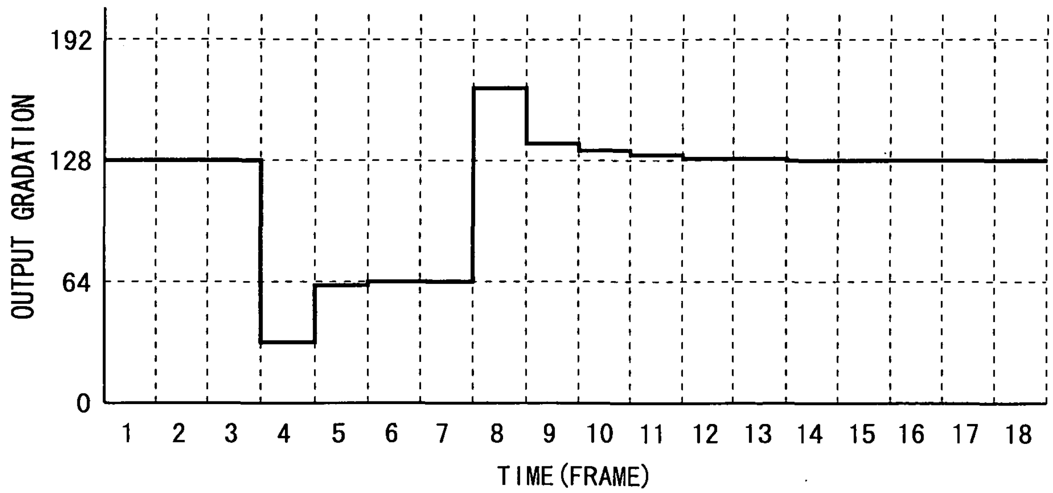


Fig. 6C

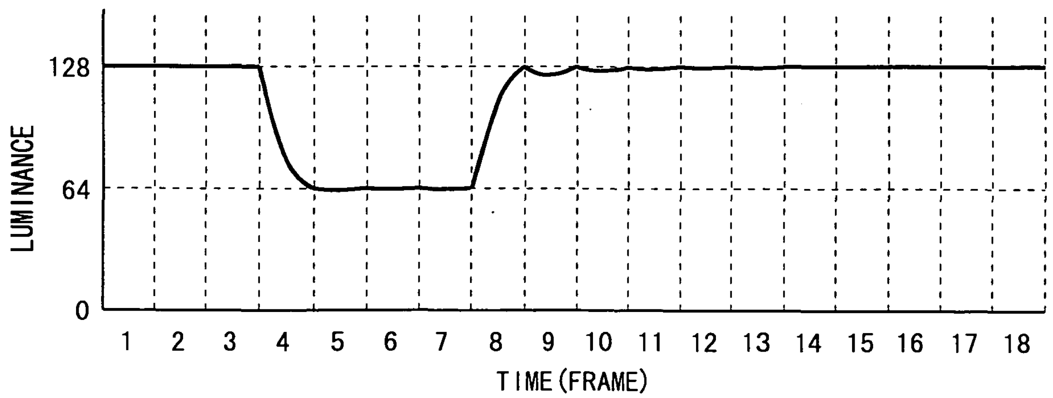


Fig. 7A

TIME (FRAME)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Din(n)	*0*	*0*	*0*	*64*	*64*	*64*	*67*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*
Din(n-1)	0	0	0	0	64	64	64	67	64	64	64	64	64	64	64	64	64	64
Cmp*	0	0	0	*1*	0	0	*0*	0	0	0	0	0	0	0	0	0	0	0
Din(n-1)*	0	0	0	0	64	64	64	67	64	64	64	64	64	64	64	64	64	64
Din(n)**	*0*	*0*	*0*	*64*	*64*	*64*	*67*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*
Cnt**	*0*	*0*	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*
Din(hold)**	32	32	32	*0*	*0*	*0*	*0*	*0*	*0*	*0*	0	0	0	0	0	0	0	0
Dout(n)	*0*	*0*	*0*	*160*	*76*	*68*	*69*	*65*	*65*	*65*	*64*	*64*	*64*	*64*	*64*	*64*	*64*	*64*

Fig. 7B

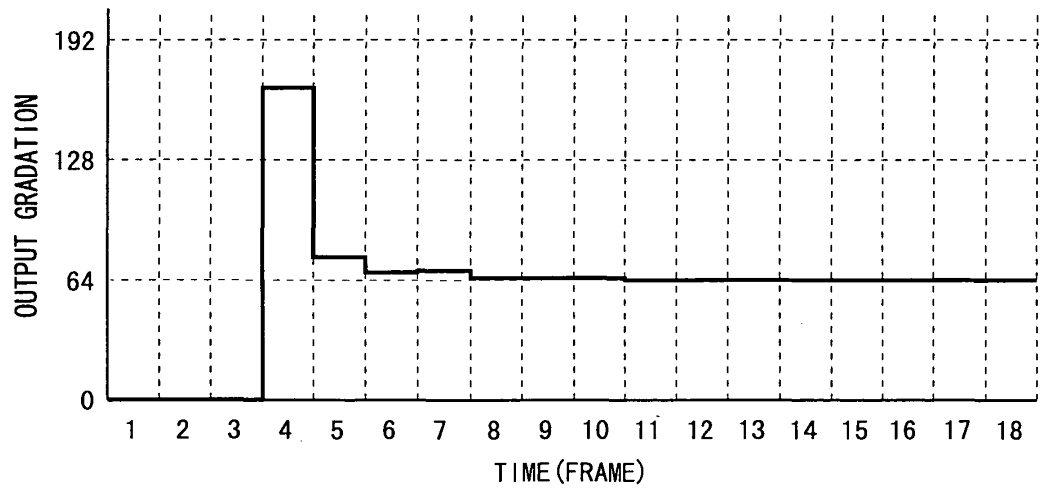


Fig. 7C

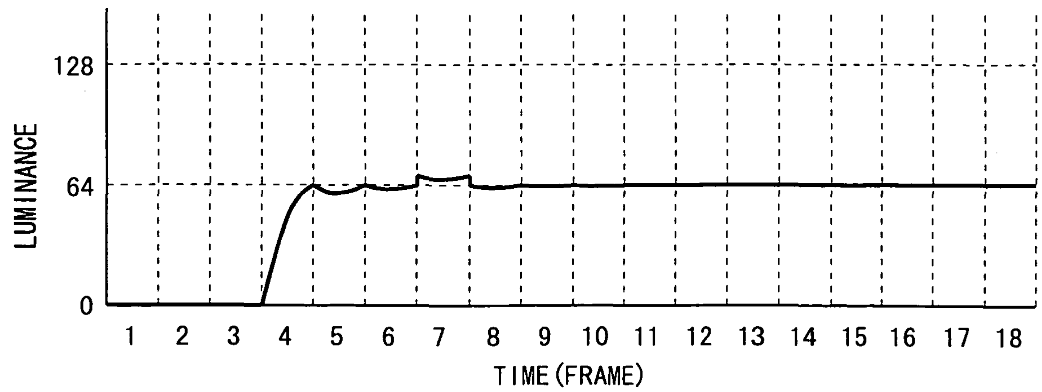


Fig. 8A

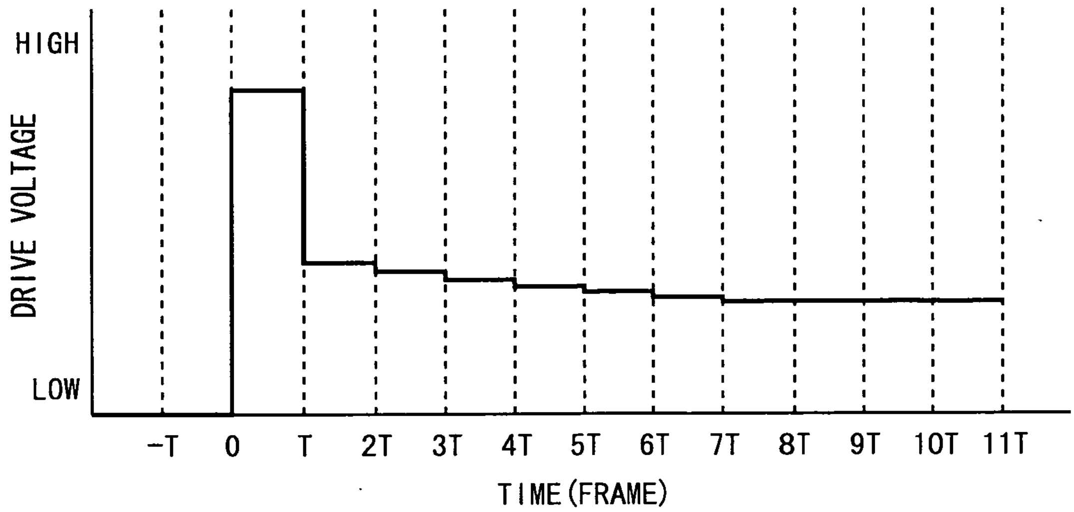

HIGH
DRIVE VOLTAGE
LOW
-T 0 T 2T 3T 4T 5T 6T 7T 8T 9T 10T 11T
TIME (FRAME)

Fig. 8B

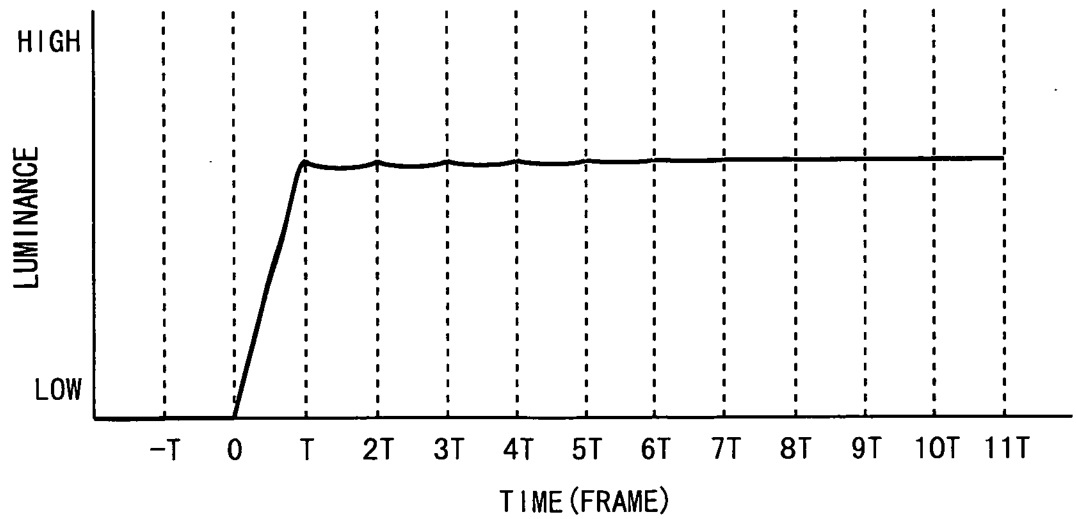

HIGH
LUMINANCE
LOW
-T 0 T 2T 3T 4T 5T 6T 7T 8T 9T 10T 11T
TIME (FRAME)

Fig. 9A

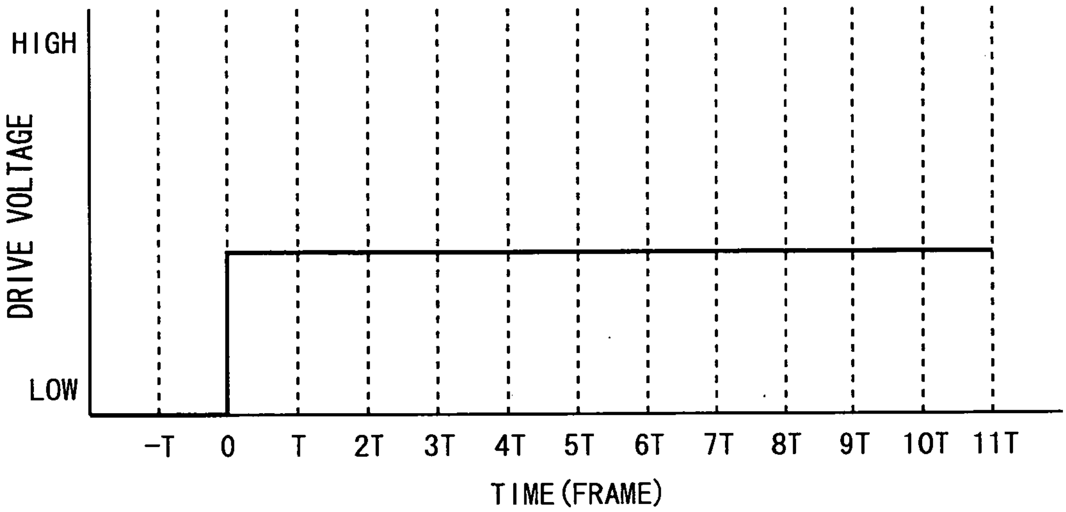

HIGH
DRIVE VOLTAGE
LOW
-T 0 T 2T 3T 4T 5T 6T 7T 8T 9T 10T 11T
TIME (FRAME)

Fig. 9B

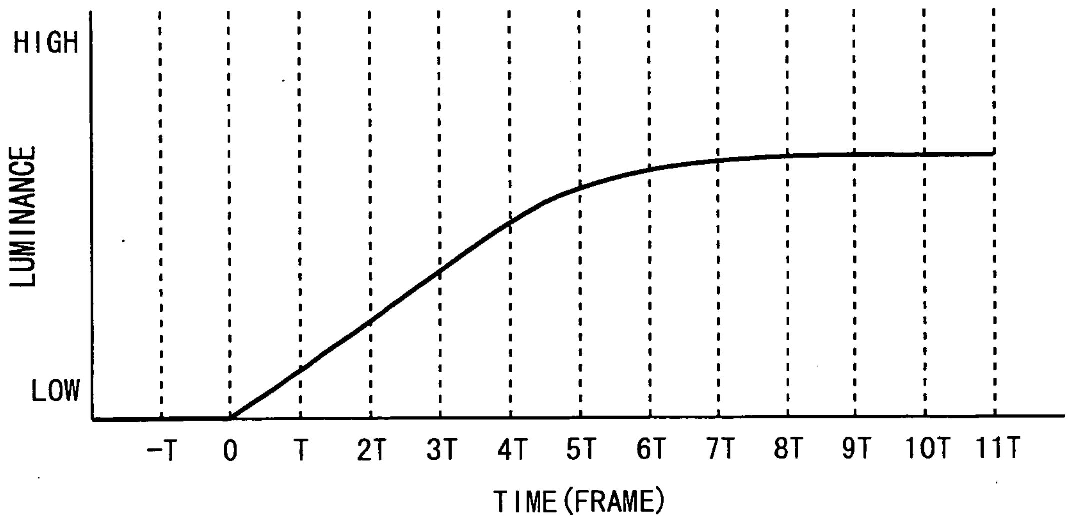

HIGH
LUMINANCE
LOW
-T 0 T 2T 3T 4T 5T 6T 7T 8T 9T 10T 11T
TIME (FRAME)

Fig. 10A

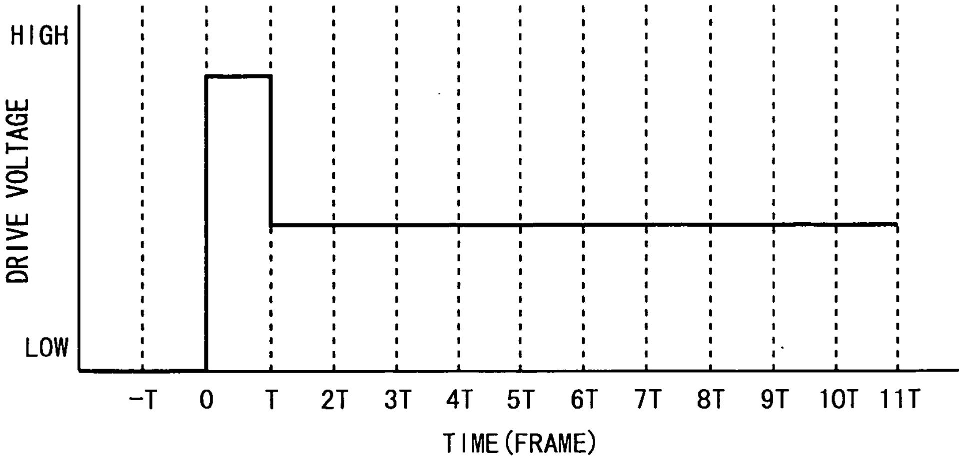


Fig. 10B

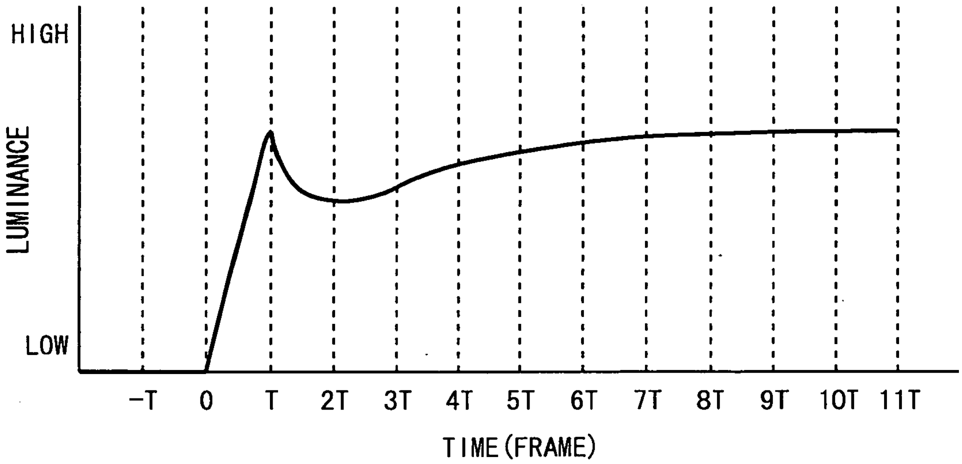


Fig. 11

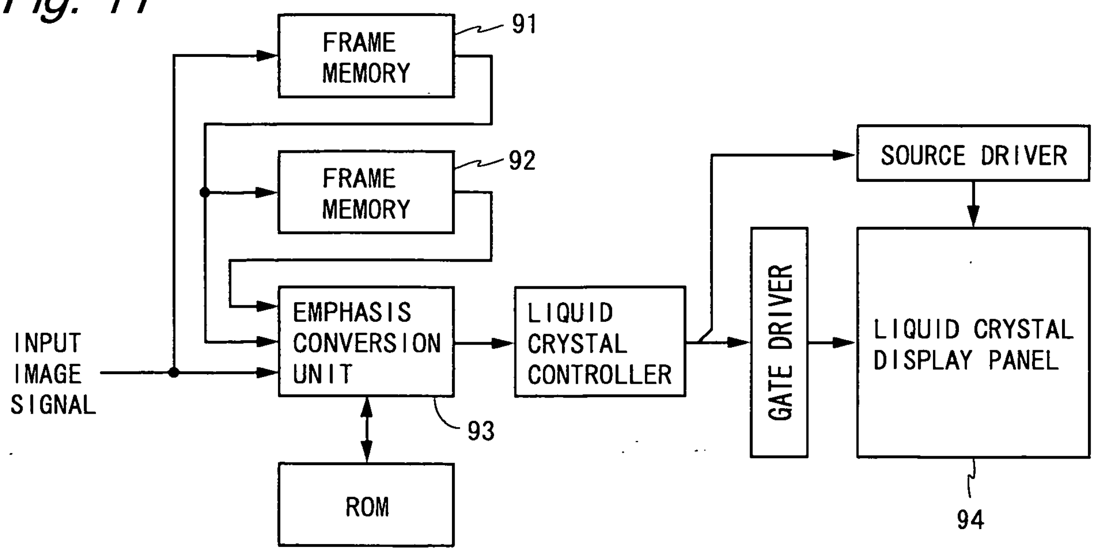


Fig. 12A

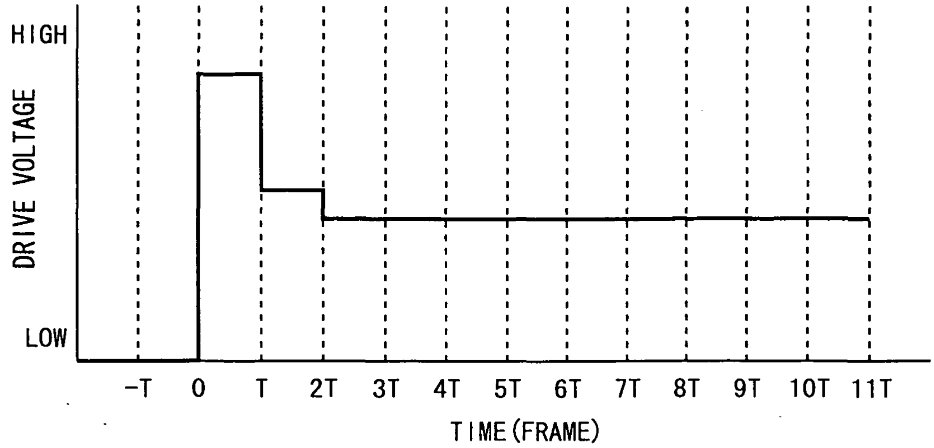


Fig. 12B

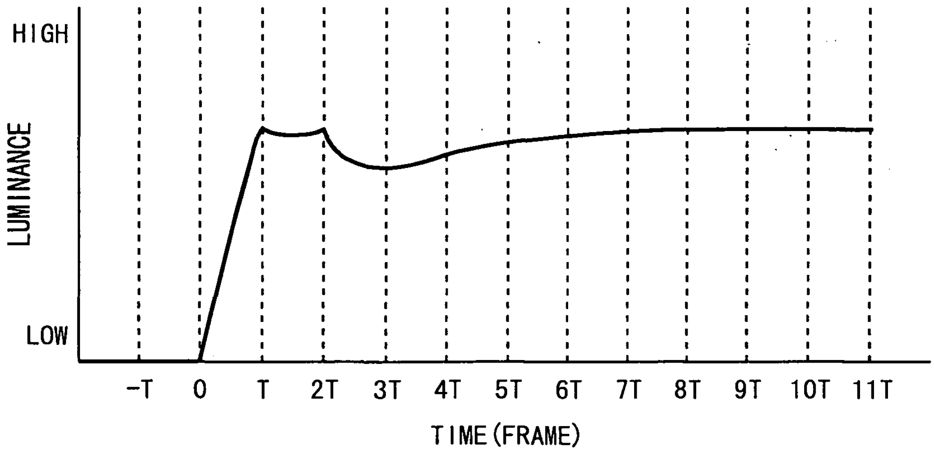
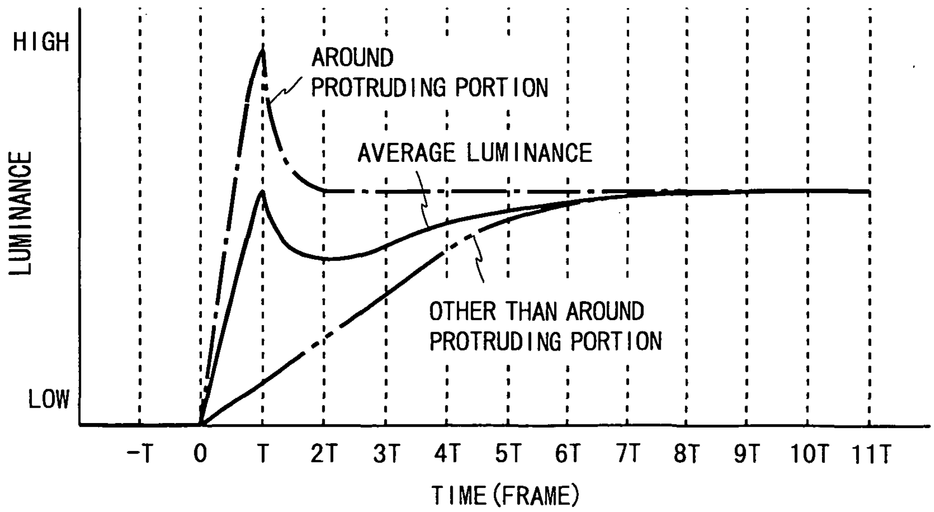


Fig. 13



REFERENCES CITED IN THE DESCRIPTION

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- US 20050001802 A1 **[0007]**
- EP 2065879 A1 **[0008]**

专利名称(译)	图像显示装置		
公开(公告)号	EP2434475B1	公开(公告)日	2015-12-02
申请号	EP2010777594	申请日	2010-01-07
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	INOUE AKIHIKO		
发明人	INOUE, AKIHIKO		
IPC分类号	G09G3/36 G02F1/133 G09G3/20 H04N5/66		
CPC分类号	G09G3/3611 G09G2310/066 G09G2320/0233 G09G2320/0252 G09G2320/0261 G09G2320/0285 G09G2320/103 G09G2340/16 G09G2360/18		
优先权	2009124752 2009-05-22 JP		
其他公开文献	EP2434475A4 EP2434475A1		
外部链接	Espacenet		

摘要(译)

灰度变化检测电路26确定灰度值是否已从前一帧改变。当灰度值改变时，第一帧存储器21存储改变之前的灰度值。保持计数计算电路27确定表示在改变灰度值之后输入的帧数的保持计数。第二帧存储器22存储所确定的保持计数。加重转换电路28执行强调视频信号上的灰度值变化的处理，并且通过较大的保持计数使重点程度变小。基于由过驱动电路12获得的视频信号驱动液晶面板14.由此，防止了由于过驱动驱动而发生的双光学响应性。

Fig. 1

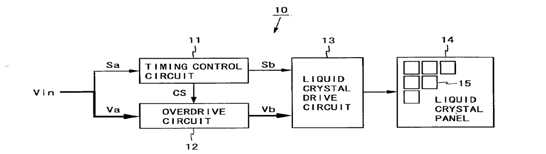

Fig. 2