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(54) **Boost converter for liquid crystal display**

Boost-Wandler für eine Flüssigkristallanzeige

Convertisseur élévateur pour affichage à cristaux liquides

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EP 2 393 191 B1

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Description

[0001] The present invention relates to liquid crystal driving technology, and to a boost converter. An embodiment relates to a liquid crystal display, and more particularly, to a boost converter for a liquid crystal display which reduces electromagnetic interference using a variable frequency when generating a panel driving voltage, and performs a boosting operation in synchronization with a synchronizing signal of image data, thereby achieving a stable boosting operation without exerting an influence on images.

[0002] FIG. 1 is a block diagram schematically illustrating the configuration of a conventional liquid crystal display. As shown in FIG. 1, the conventional liquid crystal display includes a liquid crystal panel 110 and an LCD driver IC (LDI) 120. On the liquid crystal panel 110, a plurality of gate lines and data lines are arranged perpendicular to each other to define pixel areas in the form of a matrix. The LDI 120 includes a driving circuit unit 121 for supplying driving signals and data signals to the liquid crystal panel 110, and a power supply unit 122 for supplying various power supply voltages required for the driving circuit unit 121.

[0003] The driving circuit unit 121 includes a gate driver 121A, a source driver 121B, and a timing controller 121C.

[0004] The gate driver 121A outputs a gate driving signal for driving each gate line of the liquid crystal panel 110.

[0005] The source driver 121B outputs a data signal to each data line of the liquid crystal panel 110.

[0006] The timing controller 121C controls the driving of the gate driver 121A and source driver 121B, while controlling the driving of the power supply unit 122.

[0007] The power supply unit 122 includes a power control section 122A, a source-power driving section 122B, and a gate-power driving section 122C.

[0008] The power control section 122A controls the driving of the source-power driving section 122B and gate-power driving section 122C under the control of the timing controller 121C.

[0009] In this case, the gate-power driving section 122C supplies a gate high voltage V_{GH} and a gate low voltage V_{GL} which are required for the gate driver 121A to generate the gate driving signal.

[0010] In addition, the source-power driving section 122B supplies a positive-polarity panel driving voltage VDDP (hereinafter, referred to as a "panel driving voltage VDDP") and a negative-polarity panel driving voltage VDDN, which are required for the source driver 121B to generate the data signal.

[0011] FIG. 2 illustrates a boost converter circuit which is included in the source-power driving section 122B of the LDI 120, and outputs a panel driving voltage VDDP. As shown in FIG. 2, the boost converter circuit includes: a field-effect transistor FET1 for driving a reactor L1 in response to a switching pulse LSW; a condenser Cout for storing a voltage which is loaded through a blocking diode D1 from the reactor L1 according to the switching operation of the field-effect transistor FET1; resistors R1 and R2 for dividing a panel driving voltage VDDP, which is output after being stored in the condenser Cout, at a predetermined ratio; and a controller 200 for monitoring the panel driving voltage VDDP through a voltage divided by the resistors R1 and R2 and controlling the switching pulse LSW so as to output the panel driving voltage at a target level.

[0012] The field-effect transistor FET1 repeats a series of on/off operations in response to a switching pulse LSW, as shown in FIG. 3(a), which is input to the controller 200. In this case, a boosting voltage loaded from the reactor L1 by a switching operation of the field-effect transistor FET1 is stored in the condenser Cout through the blocking diode D1.

[0013] The boosting voltage stored in the condenser Cout through a path as described above is output as the panel driving voltage VDDP.

[0014] However, when the amount of current loaded to the outside through the output terminal for the panel driving voltage VDDP is less than that accumulated in the condenser Cout, the panel driving voltage VDDP increases to an unnecessarily high level.

[0015] In order to prevent this, the panel driving voltage VDDP output from the condenser Cout is divided into voltages having predetermined levels through the use of resistors R1 and R2, and the controller 200 controls the switching pulse LSW so that a voltage having a target level can be output while monitoring the panel driving voltage VDDP based on the divided voltages.

[0016] The switching pulse LSW includes, for example, a pulse-width modulation (PWM) pulse and a pulse frequency modulation (PFM) pulse. When using the PWM pulse, the controller 200 controls the duty ratio of the PWM pulse so that a boosting voltage having a target level can be output. When using the PFM pulse, the controller 200 controls the frequency of the PFM pulse so that a boosting voltage having a target level can be output.

[0017] Generally, when the form of a switching pulse LSW to be output has been determined, the controller 200 outputs the switching pulse LSW with the same phase as shown in FIG. 3(a). Accordingly, a periodic boosting operation causes the spectrum to be concentrated to the band of a center frequency f0, as shown in FIG. 3(b).

[0018] As described above, in a conventional boost converter circuit of an LDI system, a switching pulse with the same phase is used as a switching pulse for driving a reactor, and a period boosting operation causes the energy spectrum in an amplified form to be formed, so that the energy spectrum of a harmonic frequency appears in an amplified form, too.

[0019] Furthermore, the amplified energy spectrum has a problem in that it may cause electromagnetic interference (EMI) with the frequencies of other signals used in the system.

[0020] Recently, in order to solve such a problem, there has been proposed a method of generating a switching pulse with the form of a variable frequency so as to generate a spread spectrum. However, since switching pulses with mutually different frequencies are used whenever each frame begins, panel driving voltages have differing levels little by little on all such occasions, so that there is a problem in that images are unstably displayed.

[0021] Document US 2008/0165167 discloses a printed circuit board and liquid crystal display having the same. A printed circuit board for a liquid crystal display has a structure for preventing interference between a feedback voltage generating unit or a compensating unit of a DC-DC converter and a pulse signal wiring line. The printed circuit board has a boosting circuit for boosting an input voltage to generate an analog driving voltage and a pulse signal, the boosting circuit including a control chip and an inductor coupled between an input voltage node and the control chip, the control chip supplied with a feedback voltage for controlling the amount of current flowing through the inductor, a feedback voltage generating circuit for supplying the feedback voltage to the control chip by using the analog driving voltage, and a pulse signal wiring line connecting the control chip and the inductor, and separated from the feedback voltage generating circuit.

[0022] US 2009/0135171 discloses a voltage generating system. A voltage generating system applied to a display driving apparatus is disclsoed, which is capable of changing a time point at which a signal of a pixel electrode and a signal of a common electrode perform polarity inversion, so as to adjust the frequency of an AC common voltage dynamically. A timing controller includes a control unit and a random number sequence generator. The control unit generates a control signal for a charge-pump circuit according to the random number sequence generated by the random number sequence generator.

[0023] EP 1235335 discloses an electric power converter. In the steps of switching input voltage with a switching element (10), smoothing the voltage of rectangular wave obtained by switching with a reactor L and capacitor Cf and outputting it, the voltage obtained by dividing the output voltage is compared with the sawtooth wave output from a sawtooth wave generator (14) by a comparator (12). When the switching signal in response to the result of this comparison is applied to the switching element (10), the counter (16) is actuated synchronously with the vertex of the sawtooth wave to perform opening/closing operation of the switch SW1. The time constant of the time constant circuit comprising R0 and C is adjusted according to whether a resistor R1 is present or not, and the signals of frequencies f1 and f2 coming out of the sawtooth wave generator (14) are sequentially switched to be sent to the comparator (12).

[0024] Accordingly, the present invention has been made in an effort to address the problems occurring in the related art. An object of embodiments is to provide a boost converter of an LDI capable of reducing electromagnetic interference by generating a panel driving voltage through the use of a variable frequency, while achieving a stable boosting operation using the same frequency whenever each frame begins.

[0025] In one aspect of the present invention, there is provided a boost convertor including: an oscillator configured to generate an oscillation signal having a frequency which varies in a predetermined pattern or randomly hops around a center frequency, and configured to generate an oscillation signal having a preset fixed frequency whenever each frame begins; a driver configured to perform a switching operation on the transistor, which drives the reactor generating the panel driving voltage, through use of a switching signal output from a controller; wherein the controller is configured to output the switching signal for generating a required panel driving voltage through use of the oscillation signal output from the oscillator, a voltage detected as a panel driving voltage, and a preset reference voltage.

[0026] Some features of embodiments are recited in the appended dependent claims.

[0027] In the drawings:

FIG. 1 is a block diagram schematically illustrating the configuration of a conventional liquid crystal display;

FIG. 2 illustrates a circuit diagram of a boost converter included in an LDI;

FIG. 3(a) is a waveform view of a switching pulse;

FIG. 3(b) is a view illustrating a spectrum by a conventional boosting operation;

FIG. 4 is a block diagram illustrating the configuration of a boost converter of a liquid crystal display according to an embodiment of the present invention;

FIG. 5(a) is a graph illustrating a case where a frequency varies in a predetermined pattern according to an embodiment of the present invention;

FIG. 5(b) is a graph illustrating a case where a frequency varies in a random pattern according to an embodiment of the present invention;

FIG. 5(c) is a graph illustrating a spectrum in which energy is spread due to a varied frequency according to an embodiment of the present invention;

FIG. 5(d) is a waveform view illustrating a switching pulse in which a frequency varies according to an embodiment of the present invention;

FIG. 6 is a circuit diagram illustrating the configuration of an oscillator according to a first embodiment of the present invention;

FIG. 7 is a detailed block diagram of a current source section and a counter section, shown in FIG. 6;

FIGs. 8(a) to 8(g) are waveform views illustrating the waveform at each component shown in FIG. 7;

FIG. 8(h) is a waveform view of a vertical synchronizing signal according to an embodiment of the present invention;

FIG. 8(i) is a view explaining a change in the output value of a counter section, which is determined by a

vertical synchronizing signal and a horizontal synchronizing signal, according to an embodiment of the present invention;

FIG. 9 is a detailed circuit diagram of an up/down counter according to an embodiment of the present invention;

FIG. 10 is a detailed circuit diagram of a pseudo-random bit generator according to an embodiment of the present invention;

FIG. 11 is a circuit diagram illustrating the configuration of an oscillator according to a second embodiment of the present invention;

FIGs. 12(a) to 12(d) are waveform views illustrating the waveform at each component shown in FIG. 11;

FIG. 13(a) is a view showing a result of a simulation for checking electromagnetic interference (EMI) generated by the conventional boost converter circuit;

FIG. 13(b) is a view showing a result of a simulation for confirming that electromagnetic interference (EMI) is reduced in the boost converter circuit according to an embodiment of the present invention; and

FIGs. 14(a) and 14(b) are waveform views showing the fact that it is possible to drive a panel with the same panel driving voltage at the same phase t1 and t2.

[0028] As shown in FIG. 4, the boost converter, which generates a panel driving voltage VDDP by driving a reactor L1 using a field-effect transistor FET1, includes a control block 400, which includes an oscillator 410, a panel-driving-voltage monitoring unit 420, an on-time counter 430, an off-time counter 440, an SR latch 450, and a driver 460.

[0029] The oscillator 410 generates an oscillation signal having a frequency which varies in a predetermined pattern around a center frequency f_0, as shown in FIG. 5(a), or generates an oscillation signal having a frequency which randomly hops around a center frequency f_0, as shown in FIG. 5(b). Accordingly, a spectrum by the boost converter is not concentrated to the frequency band of the center frequency f_0, and has a widely spread form, as shown in FIG. 5(c). FIG. 5(d) is a waveform view illustrating a signal which is output in the form of variable frequency from the oscillator 410. In addition, the oscillator 410 generates a preset fixed frequency through the use of a vertical synchronizing signal Vsync whenever each frame begins. Various embodiments of the oscillator 410 will be described later in detail with reference to the accompanying drawings.

[0030] The panel-driving-voltage monitoring unit 420 includes comparators CP401 and CP402, and an AND gate AD401. The comparator CP401 compares a panel driving voltage VDDP divided by resistors R1 and R2 with a reference voltage Vref, and outputs a signal according to a result of the comparison. The comparator CP402 compares the panel driving voltage VDDP divided by resistors R1 and R2 with a reference voltage SSref, which has been set for soft start, and outputs a monitoring signal according to a result of the comparison. The AND gate AD401 performs an AND operation on the output signal of the comparator CP401 and the output signal of the off-time counter 440, thereby outputting a monitoring signal.

[0031] The on-time counter 430 counts the on-time period of an oscillation signal output from the oscillator 410 after being reset by the vertical synchronizing signal Vsync.

[0032] The off-time counter 440 counts the off-time period of an oscillation signal output from the oscillator 410 after being reset by the vertical synchronizing signal Vsync.

[0033] The SR latch 450 receives the monitoring signal output from the AND gate AD401 through a set terminal S, receives a signal output from the on-time counter 430 through a reset terminal R, and outputs an error-corrected pulse having the form of a switching pulse LSW.

[0034] The driver 460 converts a pulse input from the SR latch 450 into a switching pulse LSW having a form suitable for switching the field-effect transistor FET1, and outputs the switching pulse LSW. The switching pulse LSW output from the driver 460 has the form of a variable frequency, as shown in FIG. 5(d).

[0035] The field-effect transistor FET1 repeats a series of on/off operations in response to the switching pulse LSW input from the driver 460. In this case, a boosting voltage loaded from reactor L1 by the switching operation of the field-effect transistor FET1 is stored in the condenser Cout through the blocking diode D1.

[0036] The boosting voltage stored in the condenser Cout through the above path is output as a panel driving voltage VDDP.

[0037] FIG. 6 is a circuit diagram illustrating the configuration of the oscillator 410, which operates as described above, according to a first embodiment of the present invention. As shown in FIG. 6, according to the first embodiment of the present invention, the oscillator 410 includes a first current source section 601, a second current source section 602, a counter section 603, a set-signal output section 604, a reset-signal output section 605, and an SR latch 606.

[0038] When low and high level signals are input to the set terminal S and reset terminal R of the SR latch 606, respectively, the SR latch 606 outputs low and high level signals through the output terminals Q and Qb, respectively. Accordingly, a transistor FET601 in the set-signal output section 604 is turned on, while a transistor FET602 is turned off. At the same time, a transistor FET603 in the reset-signal output section 605 is turned off, while a transistor FET604 is turned on.

[0039] Accordingly, a condenser C601 is charged with voltage supplied from the first current source section 601 through the transistor FET601. A comparator CP601 compares a charged voltage of the condenser C601, which is input through a first input terminal, with a reference voltage, and outputs a high level signal to the set

terminal S of the SR latch 606 at the moment when the charged voltage exceeds the reference voltage. At this time, a charged voltage of a condenser C602 is discharged to the ground through the transistor FET604. Thus, a low level signal is input to a first input terminal of a comparator CP602, so that the comparator CP602 outputs a low level signal through an output terminal thereof to the reset terminal R of the SR latch 606. Accordingly, the SR latch 606 outputs high and low level signals through the output terminals Q and Qb, respectively, thereof.

[0040] Thereafter, the high and low level signals output from the output terminals Q and Qb of the SR latch 606 turns off the transistor FET601 in the set-signal output section 604, while turning on the transistor FET602. At the same time, the transistor FET603 in the reset-signal output section 605 is turned on, while the transistor FET604 is turned off.

[0041] Accordingly, through a procedure as described above, low and high level signals are input to the set terminal S and reset terminal R of the SR latch 606. Therefore, the SR latch 606 outputs low and high level signals through the output terminals Q and Qb, respectively, thereof.

[0042] Consequently, the set-signal output section 604 and reset-signal output section 605, which operate as described above, cause high and low level signals to be alternately input to the set terminal S of the SR latch 606, so that the SR latch 606 outputs a square wave having a corresponding frequency through the output terminal Q thereof.

[0043] Meanwhile, the counter section 603 controls the amount of current output from the first current source section 601 and second current source section 602 in synchronization with various synchronizing signals (e.g. Vsync, Hsync, DE, etc.) to vary the charging time of the condensers C601 and C602, thereby varying the frequency of a square wave output through the output terminal Q of the SR latch 606, so that a spread spectrum is implemented. Accordingly, electromagnetic interference is reduced.

[0044] FIG. 7 is a view illustrating the configuration of the first current source section 601, the second current source section 602, and the counter section 603 according to an embodiment of the present invention. The first current source section 601 and the second current source section 602 have the same configuration, so only the first current source section 601 of the two current source sections is illustratively shown in FIG. 7.

[0045] The first current source section 601 includes a plurality of current sources I1 to In, which are connected in parallel with each other, and are connected in series with switches SW1 to SWn, respectively. The counter section 603 includes an up/down counter 701, a pseudo-random bit generator (PRBG) 702, and a multiplexer 703.

[0046] The first current source section 601 includes a plurality of current sources I1 to In, which are connected in parallel with each other, and are connected in series with switches SW1 to SWn, respectively, wherein the switches SW1 to SWn are turned on in response to an n-bit switching control signal output from the counter section 603, and outputs variable current according to the turned-on switches SW1 to SWn. For example, when the switches SW2 and SW4 of the switches SW1 to SWn are turned on in response to the switching control signal, the first current source section 601 and second current source section 602 output variable current of "Δ I=I2+I4."

[0047] The multiplexer 703 selects the output signal of the up/down counter 701 and the output signal of the pseudo-random bit generator 702 in response to a selection signal SS_SEL, and transfers the selected signal to the switches SW1 to SWn of the first and second current source sections 601 and 602.

[0048] As shown in FIGs. 8(a) and 8(b), whenever a first horizontal line of each frame is driven, the up/down counter 701 is reset in response to a vertical synchronizing signal Vsync, and outputs an n-bit switching control signal having a preset value. Thus, corresponding switches of the switches SW1 to SWn of the first and second current source sections 601 and 602 are turned on, so that the amount of current corresponding to the turned-on switches is output. Accordingly, the SR latch 606 outputs a corresponding frequency, for example, an oscillation frequency of 8 MHz as shown in FIG. 8(e), through the output terminal Q thereof.

[0049] Thereafter, the up/down counter 701 counts up or down a horizontal synchronizing signal Hsync or data enable signal DE, as shown in FIGs. 8(b) and 8(c), in a constant pattern as shown in FIG. 8(d), thereby outputting an n-bit switching control signal. Accordingly, the SR latch 606 outputs a variable frequency signal of the n bits, which periodically varies as shown in FIG. 8(e), through the output terminal Q thereof.

[0050] Also, as shown in FIGs. 8(a) and 8(f), whenever the first horizontal line of each frame is driven, the pseudo-random bit generator 702 is reset in response to a vertical synchronizing signal Vsync, and outputs an n-bit switching control signal having a preset value. Thus, corresponding switches of the switches SW1 to SWn of the first and second current source sections 601 and 602 are turned on, so that the amount of current corresponding to the turned-on switches is output. Accordingly, the SR latch 606 outputs a corresponding frequency, for example, an oscillation frequency of 8 MHz as shown in FIG. 8(g), through the output terminal Q thereof.

[0051] As described above, an oscillation signal having the same frequency is output whenever each frame begins, so that, when a variable frequency is used to reduce electromagnetic interference, an influence is not exerted on an image and a stable boosting operation can be ensured.

[0052] Thereafter, the pseudo-random bit generator 702 counts up or down a horizontal synchronizing signal Hsync or data enable signal DE, as shown in FIGs. 8(b) and 8(c), in a random pattern as shown in FIG. 8(f), thereby outputting an n-bit switching control signal. Accord-

ingly, the SR latch 606 outputs a variable frequency signal of the n bits, which randomly varies as shown in FIG. 8(g), through the output terminal Q thereof.

[0053] In FIG. 7, a selection signal SEL causes the up/down counter 701 to select an up counting operation or down counting operation, and causes the pseudo-random bit generator 702 to select a random bit generation period.

[0054] FIGs. 8(h) and 8(i) show an example where the up/down counter 701 or pseudo-random bit generator 702 changes the count period thereof through the use of the selection signal SEL whenever a vertical synchronizing signal Vsync or horizontal synchronizing signal Hsync is input or whenever a random vertical synchronizing signal Vsync or random horizontal synchronizing signal Hsync is input. Through this, whenever receiving a vertical synchronizing signal Vsync or horizontal synchronizing signal Hsync or whenever receiving a random vertical synchronizing signal Vsync or random horizontal synchronizing signal Hsync, the up/down counter 701 or pseudo-random bit generator 702 changes the count period thereof, thereby spreading the energy spectrum generated by the boost converter. Accordingly, it is possible to reduce electromagnetic interference due to energy rising.

[0055] FIG. 9 is a circuit diagram of the up/down counter 701 according to an embodiment of the present invention.

[0056] As shown in FIG. 9, the up/down counter 701 includes N-stage T flip-flops F/F901A to F/F901N, a first output signal operation module 901A, a second output signal operation module 901B, and third to N^{th} output signal operation modules 901C to 901N. The clock signal terminals of the N-stage T flip-flops F/F901A to F/F901N are connected in common to the horizontal synchronizing signal terminal Hsync, and the clear terminals thereof are connected in common to the vertical synchronizing signal terminal Vsync.

[0057] The.first output signal operation module 901A includes: an inverter I901 for inverting and outputting the selection signal SEL; an AND gate AD901 having first and second input terminals which are connected to the selection signal terminal SEL and the output terminal Q1 of the T flip-flop F/F901A, respectively; an AND gate AD902 having first and second input terminals which are connected to the inverted output terminal Qb1 of the T flip-flop F/F901A and the output terminal of the inverter I901, respectively; and an OR gate OR901 having first and second input terminals which are connected to the output terminals of the AND gates AD901 and AD902, respectively.

[0058] The second output signal operation module 901B includes: an AND gate AD903 having first and second input terminals which are connected to the output terminal of the AND gate AD901 and the output terminal Q2 of the T flip-flop F/F901B, respectively; an AND gate AD904 having first and second input terminals which are connected to the inverted output terminal Qb2 of the T flip-flop F/F901B and the output terminal of the AND gate AD902, respectively; and an OR gate OR902 having first and second input terminals which are connected to the output terminals of the AND gates AD903 and AD904, respectively.

[0059] The third to N^{th} output signal operation modules 901C to 901N have the same construction as the second output signal operation module 901B, respectively, and are provided to the rear stage of the second output signal operation module 901B.

[0060] FIG. 10 is a circuit diagram of the pseudo-random bit generator 702 according to an embodiment of the present invention. As shown in FIG. 10, the pseudo-random bit generator 702 includes N-stage D flip-flops F/F1001A to F/F1001N, a multiplexer MUX1001, and an exclusive-OR gate XOR1001. The clock signal terminals of the N-stage D flip-flops F/F1001A to F/F1001N are connected in common to the horizontal synchronizing signal terminal Hsync, and the clear terminals CLR thereof are connected in common to the vertical synchronizing signal terminal Vsync.

[0061] The multiplexer MUX1001 selectively outputs the output signals of the output terminals Q1 to Qn of the D flip-flops F/F1001A to F/F1001N in response to a selection signal SEL.

[0062] The exclusive-OR gate XOR1001 performs an exclusive-OR operation on the output signals of the multiplexer MUX1001, and feeds a result of the operation back to the input terminal D of the first-stage D flip-flop F/F1001A.

[0063] FIG. 11 is a circuit diagram illustrating the configuration of the oscillator 410 shown in FIG. 4 according to a second embodiment of the present invention. As shown in FIG. 11, the oscillator 410 may include an RC oscillation circuit 1101, a ground voltage generation section 1102, and a counter section 1103.

[0064] A first node N1 and a third node are connected via a condenser Cosc. Accordingly, when the third node N3 is at a high voltage level, the first node N1 is boosted to a voltage level corresponding to the high voltage level.

[0065] When the third node N3 is at a high voltage level, a transistor FET111 is turned off while transistors FET1112 and FET1113 are turned on, so that a fourth node N4 has the level of a ground voltage VSSA. Accordingly, electric charges of the condenser Cosc charged based on an RC time constant "Rosc·Cosc" are discharged to the fourth node N4.

[0066] The ground voltage generation section 1102 and counter section 1103 cause the ground voltage VSSA to vary to a ground voltage having a VSSA1, VSSA2, or VSSA3 level, as described later. When the voltage of the first node N1 exceeds (or falls below) a logic threshold voltage, as shown in FIG. 12(a), the voltage of a second node N2 rises, and the voltage of the third node N3 drops. In this case, since the fourth node N4 is at a high voltage level, the condenser Cosc is charged based on the RC time constant.

[0067] Such an operation is repeated, so that an RS

oscillation operation is achieved. In this case, the oscillation frequency has twice the period of the RC time when the on-resistances of transistors are ignored.

[0068] Meanwhile, when a signal having a desired frequency is generated through the use of the RC oscillation circuit 1101, as described above, a spread spectrum is implemented by varying the ground voltage VSSA, as described below.

[0069] That is to say, first, a ground voltage VSS is divided into VSSA1, VSSA2, and VSSA3 levels through the use of series resistors R1101, R1102, and R1103 for division. Then, the voltages of VSSA1, VSSA2, and VSSA3 levels are buffered through buffers BUF1101, BUF1102, and BUF1103, and one of the voltages of VSSA1, VSSA2, and VSSA3 levels is selected by the multiplexer MUX1101 and is output to be the ground voltage VSSA of the RC oscillation circuit. In this case, by controlling a ground voltage selection operation of the multiplexer MUX1101 using the counter section 1103, it is possible to vary the oscillation frequency of the RC oscillation circuit. FIGs. 12(a) to 12(d) are waveform views showing an example where the phases of the first to fourth nodes N1 to N4 vary according to the ground voltages.

[0070] To this end, the counter section 1103 may be implemented in various manners. For example, the counter section 1103 may include an up/down counter and a pseudo-random bit generator, as shown in FIG. 7, to be driven in synchronization with various synchronizing signals (e.g. Vsync, Hsync, DE, etc.), as described above. Accordingly, the frequency of an oscillation signal generated by the RC oscillation circuit 1101 varies, so that a spread spectrum is implemented. Therefore, it is possible to reduce electromagnetic interference, while ensuring a stable boosting operation which does not exert an influence on an image.

[0071] FIG. 13(a) is a view showing a result of a simulation for checking electromagnetic interference (EMI) generated by the conventional boost converter circuit, and FIG. 13(b) is a view showing a result of a simulation which confirms that electromagnetic interference (EMI) is reduced in the boost converter circuit according to the present invention.

[0072] FIGs. 14(a) and 14(b) are waveform views showing the fact that it is possible to drive a panel with the same panel driving voltage through the use of a synchronizing signal whenever each frame begins according to the present invention. For reference, FIG. 14(a) is a waveform view of a vertical synchronizing signal Vsync, horizontal synchronizing signal Hsync, or data enable signal DE, and FIG. 14(b) is a waveform view of a positive/negative panel driving voltage VDDP/VDDN.

[0073] As is apparent from the above description, the present invention provides a boost converter of an LDI, which reduces electromagnetic interference by generating a panel driving voltage through the use of a variable frequency, and uses the same frequency whenever each frame begins, so that the boosting operation can be stably performed without exerting an influence on images.

[0074] Although embodiments of the present invention have been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope of the invention as disclosed in the accompanying claims.

Claims

1. A boost converter for a liquid crystal display, wherein a transistor "FET1" performing a switching operation in response to a switching pulse causes a reactor to be driven to generate a panel driving voltage, the boost converter comprising:

   an oscillator (410) configured to generate an oscillation signal having a frequency which varies in a predetermined pattern or randomly hops around a center frequency, and to generate said oscillation signal such that it has a preset fixed frequency whenever each frame begins;
   a driver (460) configured to perform a switching operation on the transistor, which drives the reactor generating the panel driving voltage, through use of a switching signal output from a controller (420, 430, 440, 450, 460); wherein
   the controller is configured to output the switching signal for generating a required panel driving voltage through use of the oscillation signal output from the oscillator, a voltage detected as a panel driving voltage, and a preset reference voltage.

2. The boost converter according to claim 1, wherein the oscillator (410) comprises:

   first and second current source sections (601 and 602) configured to output variable current;
   a counter section (603) configured to count a synchronizing signal, and to vary output current of the first and second current source sections through use of a counted value;
   a set-signal output section (604) configured to change a charge voltage so as to correspond to the output current of the first current source section, to compare the changed charge voltage with a first reference voltage, and to generate a set signal according to a result of the comparison;
   a reset-signal output section (605) configured to change a charge voltage so as to correspond to the output current of the second current source section, to compare the changed charge voltage with a second reference voltage, and to generate a reset signal according to a result of the comparison; and

an SR latch (606) configured to generate an output signal and an inverted output signal in the form of a square wave according to the set signal and reset signal output from the set-signal output section and reset-signal output section, respectively, and to control the output current of the first and second current source sections through use of the output signal and the inverted output signal.

3. The boost converter according to claim 2, wherein each of the first and second current source sections (601 and 602) comprises:

a plurality of switches "SW1 to SWn" configured to be controlled by the counter section (603); and
a plurality of current sources "I1 to In" configured to be connected in series to the plurality of switches, respectively, and to be connected in parallel with each other.

4. The boost converter according to claim 1, wherein the oscillator (410) comprises:

an RC oscillation circuit (1101) configured to oscillate a signal having a frequency which varies depending on a change in a ground voltage;
a ground voltage generation section (1102) configured to divide a ground voltage into a plurality of voltages having mutually different levels, and to selectively output the voltages; and
a counter section (1103) configured to control a ground voltage selection operation of the ground voltage generation section in synchronization with a synchronization signal.

5. The boost converter according to claim 4, wherein the ground voltage generation section (1102) comprises:

serially-connected resistors configured to divide ground voltage VSSA into ground voltages of VSSA1, VSSA2, and VSSA3 levels;
a plurality of buffers configured to buffer the divided ground voltages VSSA1, VSSA2, and VSSA3, respectively; and
a multiplexer "MUX1101" configured to selectively output the buffered ground voltages.

6. The boost converter according to claim 2 or claim 4, wherein the counter section comprises:

an up/down counter (701) configured to be reset by a vertical synchronizing signal whenever each frame begins, to output an n-bit switching control signal having a preset value, and then to count up/down a horizontal synchronizing signal or data enable signal in a predetermined pattern, thereby outputting an n-bit switching control signal;
a pseudo-random bit generator (702) configured to be reset by a vertical synchronizing signal whenever each frame begins, to output an n-bit switching control signal having a preset value, and then to count up/down a horizontal synchronizing signal or data enable signal in a random pattern, thereby outputting an n-bit switching control signal; and
a multiplexer (703) configured to select and output an output signal of the up/down counter or an output signal of the pseudo-random bit generator in response to a selection signal.

7. The boost converter according to claim 6, wherein, in the up/down counter (701), an up/down count operation is determined depending on the selection signal.

8. The boost converter according to claim 6, wherein, in the pseudo-random bit generator (702), a random bit generation period is determined depending on the selection signal.

9. The boost converter according to claim 1, wherein the controller comprises:

a panel-driving-voltage monitoring unit (420) which comprises a first comparator "CP401" configured to compare a detection voltage of the panel driving voltage with a reference voltage and to output a signal according to a result of the comparison, a second comparator "CP402" configured to compare a detection voltage of the panel driving voltage with a reference voltage set for soft start and to output a second monitoring signal according to a result of the comparison, and an AND gate configured to perform an AND operation on the output signal of the first comparator and an output signal of an off-time counter (440) and to output a first monitoring signal according to a result of the comparison;
an on-time counter (430) configured to count an on-time period of an oscillation signal output from the oscillator (410) after being reset by a vertical synchronizing signal;
the off-time counter configured to count an off-time period of an oscillation signal output from the oscillator after being reset by a vertical synchronizing signal; and
an SR latch (450) configured to receive the first monitoring signal output from the AND gate through a set terminal of the SR latch, to receive a signal output from the on-time counter through a reset terminal of the SR latch, and to output an error-corrected pulse having the form of a

switching pulse.

Patentansprüche

1. Aufwärtswandler für eine Flüssigkristallanzeige, wobei ein Transistor "FET1", der einen Schaltvorgang als Reaktion auf einen Schaltimpuls durchführt, eine Drosselspule veranlasst, angetrieben zu werden, um eine Antriebsspannung für ein Anzeigefeld zu erzeugen, wobei der Aufwärtswandler Folgendes umfasst:

   einen Oszillator (410), der konfiguriert ist, ein Schwingungssignal mit einer Frequenz zu erzeugen, die nach einem vordefinierten Muster variiert oder zufällig um eine zentrale Frequenz springt, und das Schwingungssignal derart zu erzeugen, dass es beim Beginnen jedes Frames eine voreingestellte feste Frequenz hat;
   einen Treiber (460), der konfiguriert ist, einen Schaltvorgang am Transistor vorzunehmen, und die die Drosselspule antreibt, die die Antriebsspannung für das Anzeigefeld erzeugt, durch die Verwendung eines Schaltsignalausgangs von einer Steuerung (420, 430, 440, 450, 460), wobei
   die Steuerung konfiguriert ist, das Schaltsignal auszugeben, um eine erforderliche Antriebsspannung für ein Anzeigefeld durch die Verwendung des Schwingungssignalausgangs vom Oszillator, eine als Antriebsspannung für ein Anzeigefeld erkannte Spannung und eine voreingestellte Referenzspannung zu erzeugen.

2. Aufwärtswandler nach Anspruch 1, wobei der Oszillator (410) Folgendes umfasst:

   einen ersten und einen zweiten Stromquellenabschnitt (601 und 602), die konfiguriert sind, variablen Strom auszugeben;
   einen Zählerabschnitt (603), der konfiguriert ist, ein synchronisierendes Signal zu zählen und den Ausgangsstrom des ersten und des zweiten Stromquellenabschnitts durch die Verwendung eines gezählten Werts zu variieren;
   einen Einstellsignal-Ausgangsabschnitt (604), der konfiguriert ist, eine Ladespannung zu ändern, sodass sie dem Ausgangsstrom des ersten Stromquellenabschnitts entspricht, die geänderte Ladespannung mit einer ersten Referenzspannung zu vergleichen und ein Einstellsignal gemäß einem Ergebnis des Vergleichs zu erzeugen;
   einen Rückstellsignal-Ausgangsabschnitt (605), der konfiguriert ist, eine Ladespannung zu ändern, sodass sie dem Ausgangsstrom des zweiten Stromquellenabschnitts entspricht, die geänderte Ladespannung mit einer zweiten Referenzspannung zu vergleichen und ein Rückstellsignal gemäß einem Ergebnis des Vergleichs zu erzeugen; und
   ein SR-Latch (606), das konfiguriert ist, ein Ausgangssignal und ein invertiertes Ausgangssignal in der Form einer Rechteckschwingung gemäß dem Einstellsignal- bzw. dem Rückstellsignalausgang vom Einstellsignal-Ausgangsabschnitt bzw. vom Rückstellsignal-Ausgangsabschnitt zu erzeugen und den Ausgangsstrom des ersten und des zweiten Stromquellenabschnitts durch die Verwendung des Ausgangssignals und des invertierten Ausgangssignals zu steuern.

3. Aufwärtswandler nach Anspruch 2, wobei jeder des ersten und des zweiten Stromquellenabschnitts (601 und 602) Folgendes umfasst:

   eine Mehrzahl von Schaltern "SW1 bis SWn", die konfiguriert sind, vom Zählerabschnitt (603) gesteuert zu werden; und
   eine Mehrzahl von Stromquellen "I1 bis In", die konfiguriert sind, seriell jeweils mit der Mehrzahl von Schaltern verbunden zu sein und parallel miteinander verbunden zu sein.

4. Aufwärtswandler nach Anspruch 1, wobei der Oszillator (410) Folgendes umfasst:

   einen RC-Schwingkreis (1101), der konfiguriert ist, ein Signal mit einer Frequenz, die abhängig von einer Änderung einer Massespannung variiert, zu oszillieren;
   einen Massespannungserzeugungsabschnitt (1102), der konfiguriert ist, eine Massespannung in eine Mehrzahl von Spannungen aufzuteilen, die voneinander unterschiedliche Höhen haben und die Spannungen selektiv auszugeben; und
   einen Zählerabschnitt (1103), der konfiguriert ist, einen Massespannungsauswahlvorgang des Massespannungserzeugungsabschnitts in Synchronisation mit einem Synchronisationssignal zu steuern.

5. Aufwärtswandler nach Anspruch 4, wobei der Massespannungserzeugungsabschnitt (1102) Folgendes umfasst:

   seriell verbundene Widerstände, die konfiguriert sind, eine Massespannung VSSA in Massespannungen mit den Höhen VSSA1, VSSA2 und VSSA3 aufzuteilen;
   eine Mehrzahl von Zwischenspeichern, die konfiguriert sind, die aufgeteilten Massespannungen VVSA1, VSSA2 bzw. VSSA3 zwischenzu-

speichern; und
einen Multiplexer "MUX1101", der konfiguriert ist, die zwischengespeicherten Massespannungen selektiv auszugeben.

6. Aufwärtswandler nach Anspruch 2 oder Anspruch 4, wobei der Zählerabschnitt Folgendes umfasst:

einen Aufwärts-/Abwärtszähler (701), der konfiguriert ist, durch ein vertikales synchronisierendes Signal beim Beginnen jedes Frames rückgestellt zu werden, ein n-Bit-Schaltsteuersignal mit einem voreingestellten Wert auszugeben und dann ein horizontales synchronisierendes Signal oder Datenfreigabesignal nach einem vorbestimmten Muster nach oben oder nach unten zu zählen, wodurch ein n-Bit-Schaltsteuersignal ausgegeben wird;
einen Pseudo-Zufallsbitgenerator (702), der konfiguriert ist, durch ein vertikales synchronisierendes Signal beim Beginnen jedes Frames rückgestellt zu werden, ein n-Bit-Schaltsteuersignal mit einem voreingestellten Wert auszugeben und dann ein horizontales synchronisierendes Signal oder Datenfreigabesignal nach einem zufälligen Muster nach oben oder nach unten zu zählen, wodurch ein n-Bit-Schaltsteuersignal ausgegeben wird; und
einen Multiplexer (703), der konfiguriert ist, ein Ausgangssignal des Aufwärts-/Abwärtszählers oder ein Ausgangssignal des Pseudo-Zufallsbitgenerators als Reaktion auf ein Auswahlsignal auszuwählen und auszugeben.

7. Aufwärtswandler nach Anspruch 6, wobei im Aufwärts-/Abwärtszähler (701) ein Aufwärts-/Abwärtszählvorgang abhängig vom Auswahlsignal bestimmt wird.

8. Aufwärtswandler nach Anspruch 6, wobei im Pseudo-Zufallsbitgenerator (702) ein Zufallsbitgenerationszeitraum abhängig vom Auswahlsignal bestimmt wird.

9. Aufwärtswandler nach Anspruch 1, wobei die Steuerung Folgendes umfasst:

eine Überwachungseinheit (420) für die Antriebsspannung des Anzeigefelds, die einen ersten Komparator "CP401" umfasst, der konfiguriert ist, eine Erkennungsspannung der Antriebsspannung des Anzeigefelds mit einer Referenzspannung zu vergleichen und ein Signal gemäß einem Ergebnis des Vergleichs auszugeben; einen zweiten Komparator "CP402", der konfiguriert ist, eine Erkennungsspannung der Antriebsspannung des Anzeigefelds mit einer Referenzspannung zu vergleichen, die für einen Soft-Start festgelegt ist, und ein zweites Überwachungssignal gemäß einem Ergebnis des Vergleichs auszugeben; und ein UND-Gatter, das konfiguriert ist, eine UND-Operation am Ausgangssignal des ersten Komparators und einem Ausgangssignal eines Ausschaltzeitzählers (440) durchzuführen und ein erstes Überwachungssignal gemäß einem Ergebnis des Vergleichs auszugeben;
einen Einschaltzeitzähler (430), der konfiguriert ist, einen Einschaltzeitraum eines Schwingungssignalausgangs vom Oszillator (410) zu zählen, nachdem er durch ein vertikales synchronisierendes Signal rückgestellt wurde,
wobei der Ausschaltzeitzähler konfiguriert ist, einen Ausschaltzeitraum eines Schwingungssignalausgangs vom Oszillator zu zählen, nachdem er durch ein vertikales synchronisierendes Signal rückgestellt wurde; und
ein SR-Latch (450), das konfiguriert ist, den ersten Überwachungssignalausgang vom UND-Gatter durch ein Einstellterminal des SR-Latches zu empfangen, einen Signalausgang vom Einschaltzeitzähler durch ein Rückstellterminal des SR-Latches zu empfangen und einen fehlerkorrigierten Impuls auszugeben, der die Form eines Schaltimpulses hat.

Revendications

1. Convertisseur élévateur pour un écran à cristaux liquides, dans lequel un transistor « FET1 » effectuant une opération de commutation, en réponse à une impulsion de commutation, provoque la commande d'un réacteur afin de générer une tension de commande d'un panneau, le convertisseur élévateur comprenant :

un oscillateur (410) configuré de façon à générer un signal d'oscillation ayant une fréquence qui varie selon un modèle prédéterminé ou saute de manière aléatoire autour d'une fréquence centrale, et de façon à générer ledit signal d'oscillation, de sorte qu'il ait une fréquence fixe préétablie, quel que soit le moment où chaque trame commence ;
un système de commande (460) configuré de façon à effectuer une opération de commutation sur le transistor, qui commande le réacteur générant la tension de commande du panneau, en utilisant un signal de commutation émis par un contrôleur (420, 430, 440, 450, 460) ; dans lequel
le contrôleur est configuré de façon à émettre le signal de commutation pour générer une tension de commande de panneau requise en utilisant un signal d'oscillation émis par l'oscillateur, une

tension détectée comme une tension de commande du panneau, et une tension de référence préétablie.

2. Convertisseur élévateur selon la revendication 1, dans lequel l'oscillateur (410) comprend :

une première et une seconde sections de source de courant (601 et 602) configurées de façon à émettre un courant variable ;
une section de compteur (603), configurée de façon à décompter un signal de synchronisation, et à modifier le courant de sortie de la première et de la seconde sections de source de courant en utilisant une valeur décomptée ;
une section de sortie de signal d'initialisation (604), configurée de façon à modifier une tension de charge afin qu'elle corresponde au courant de sortie de la première section de source de courant, à comparer la tension de charge modifiée avec une première tension de référence, et à générer un signal d'initialisation selon un résultat de la comparaison ;
une section de sortie de signal de réinitialisation (605), configurée de façon à modifier une tension de charge, afin qu'elle corresponde au courant de sortie de la seconde section de source de courant, à comparer la tension de charge modifiée avec une seconde tension de référence, et à générer un signal de réinitialisation selon un résultat de la comparaison ; et
une bascule SR (initialisation-réinitialisation) (606) configurée de façon à générer un signal de sortie et un signal de sortie inversé sous la forme d'une onde carrée, selon le signal d'initialisation et le signal de réinitialisation émis par la section de sortie du signal d'initialisation et la section de sortie du signal de réinitialisation, respectivement, et de façon à contrôler le courant de sortie de la première et de la seconde sections de source de courant, en utilisant le signal de sortie et le signal de sortie inversé.

3. Convertisseur élévateur selon la revendication 2, dans lequel chacune des première et seconde sections de source de courant (601 et 602) comprend :

une pluralité d'interrupteurs « SW1 à SWn » configurés de façon à être commandés par la section de compteur (603) ; et
une pluralité de sources de courant « I1 à In » configurées de façon à être raccordées en série à la pluralité d'interrupteurs, respectivement, et à être raccordées en parallèle les unes avec les autres.

4. Convertisseur élévateur selon la revendication 1, dans lequel l'oscillateur (410) comprend :

un circuit d'oscillation RC (1101) configuré de façon à faire osciller un signal, dont la fréquence varie en fonction d'un changement de la tension de terre ;
une section de génération de tension de terre (1102) configurée de façon à diviser une tension de terre en une pluralité de tensions de niveaux réciproquement différents, et à émettre sélectivement les tensions ; et
une section de compteur (1103) configurée de façon à contrôler une opération de sélection de tension de terre de la section de génération de tension de terre, en synchronisation avec un signal de synchronisation.

5. Convertisseur élévateur selon la revendication 4, dans lequel la section de génération de tension de terre (1102) comprend :

des résistances connectées en série, configurées de façon à diviser la tension de terre VSSA en tensions de terre de niveaux VSSA1, VSSA2 et VSSA3 ;
une pluralité de lisseurs configurés de façon à lisser les tensions de terre divisées VSSA1, VSSA2 et VSSA3 respectivement ; et
un multiplexeur « MUX1101 » configuré de façon à émettre sélectivement les tensions de terre lissées.

6. Convertisseur élévateur selon la revendication 2 ou la revendication 4, dans lequel la section de compteur comprend :

un compteur plus/moins (701) configuré de façon à être réinitialisé par un signal de synchronisation vertical, quel que soit le moment où chaque trame commence, à émettre un signal de commande de commutation à bit n, ayant une valeur préétablie, et ensuite à décompter à la hausse ou à la baisse un signal de synchronisation horizontal ou un signal d'activation de données selon un modèle prédéterminé, en émettant ainsi un signal de commande de commutation à bit n ;
un générateur de bit pseudo-aléatoire (702) configuré de façon à être réinitialisé par un signal de synchronisation vertical, quel que soit le moment où chaque trame commence, à émettre un signal de commande de commutation de bit n ayant une valeur préétablie, puis à décompter à la hausse ou à la baisse un signal de synchronisation horizontal ou un signal d'activation de données selon un modèle aléatoire, en émettant ainsi un signal de commande de commutation à bit n ; et
un multiplexeur (703) configuré de façon à sélectionner et à émettre un signal de sortie du

compteur plus/moins ou un signal de sortie du générateur de bit pseudo-aléatoire en réponse à un signal de sélection.

7. Convertisseur élévateur selon la revendication 6, dans lequel, dans le compteur plus/moins (701), une opération de décompte à la hausse ou à la baisse est déterminée en fonction du signal de sélection.

8. Convertisseur élévateur selon la revendication 6, dans lequel, dans le générateur de bit pseudo-aléatoire (702), une période de génération de bit aléatoire est déterminée en fonction du signal de sélection.

9. Convertisseur élévateur selon la revendication 1, dans lequel le contrôleur comprend :

une unité de contrôle de la tension de commande de panneau (420), qui comprend un premier comparateur « CP401 », configuré de façon à comparer une tension de détection de la tension de commande de panneau avec une tension de référence et à émettre un signal selon un résultat de la comparaison, un second comparateur « CP402 » configuré de façon à comparer une tension de détection de la tension de commande de panneau avec une tension de référence établie pour démarrer en douceur, et à émettre un second signal de contrôle selon un résultat de la comparaison, et un circuit ET configuré de façon à effectuer une opération ET sur le signal de sortie du premier comparateur et un signal de sortie d'un compteur de temps froid (440) et à émettre un premier signal de contrôle selon un résultat de la comparaison ;
un compteur de temps chaud (430), configuré de façon à décompter une période de temps chaud d'un signal d'oscillation émis par l'oscillateur (410) après avoir été réinitialisé par un signal de synchronisation vertical ;
le compteur de temps froid, configuré de façon à décompter une période de temps froid d'un signal d'oscillation émis par l'oscillateur après avoir été réinitialisé par un signal de synchronisation vertical ; et
une bascule SR (450) configurée de façon à recevoir le premier signal de contrôle émis par le circuit ET à travers un terminal initialisé de la bascule SR, à recevoir un signal émis par le compteur de temps chaud, à travers un terminal réinitialisé de la bascule SR, et à émettre une impulsion à erreur corrigée ayant la forme d'une impulsion de commutation.

FIG. 1

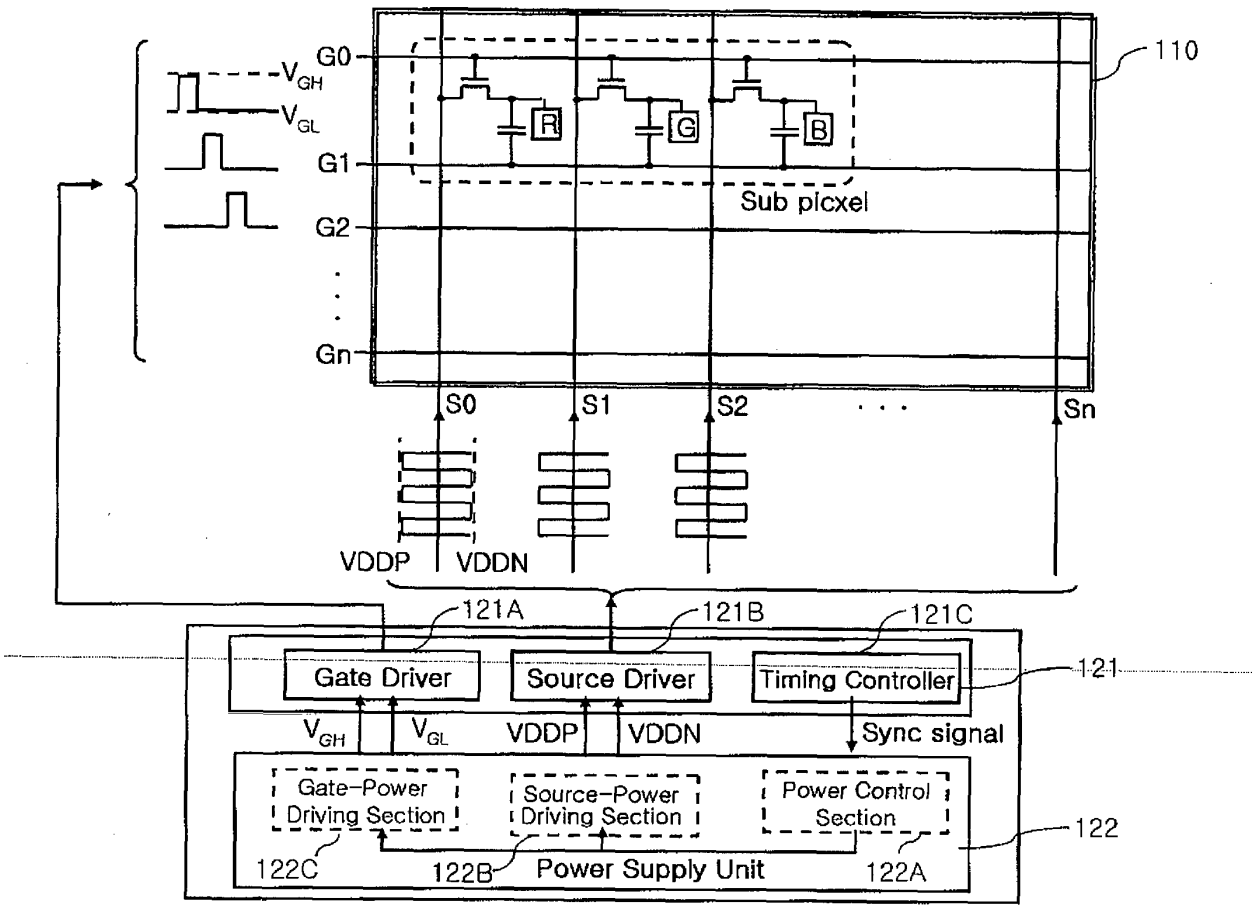

G0
G1
G2
Gn
V_{GH}
V_{GL}
R
G
B
Sub picxel
110
S0
S1
S2
Sn
VDDP
VDDN
121A
121B
121C
Gate Driver
Source Driver
Timing Controller
121
V_{GH}
V_{GL}
VDDP
VDDN
Sync signal
Gate-Power Driving Section
Source-Power Driving Section
Power Control Section
122
122C
122B
Power Supply Unit
122A

FIG. 2

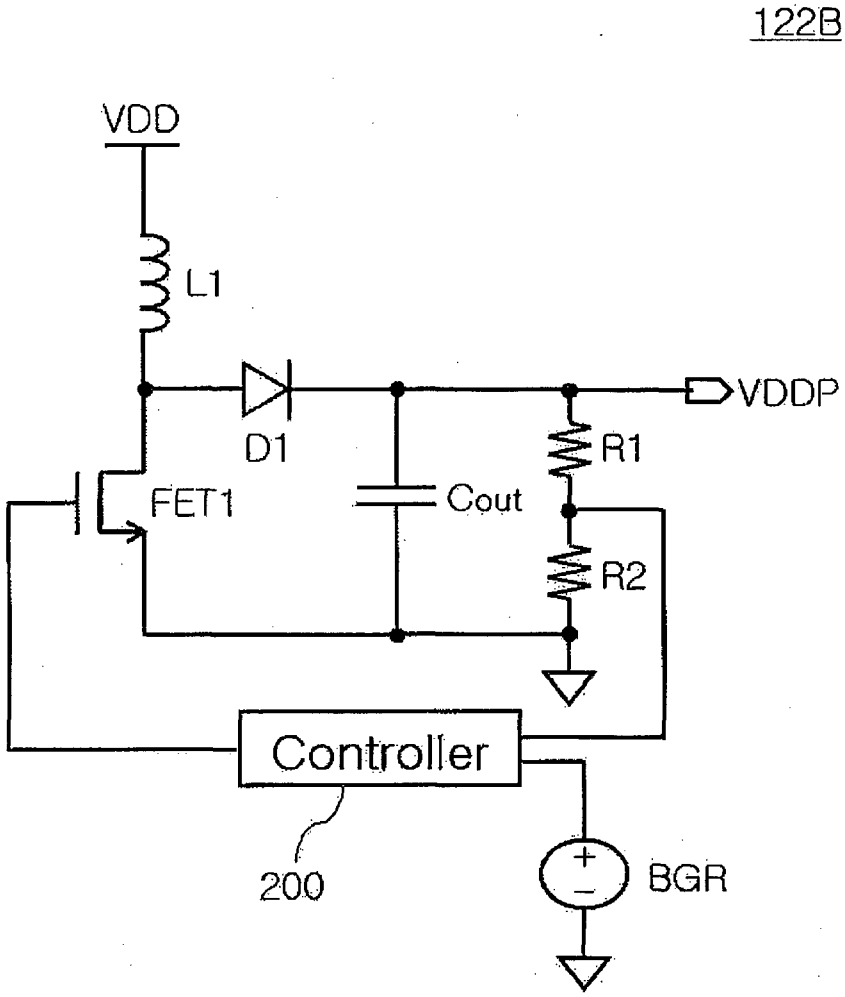


FIG. 3

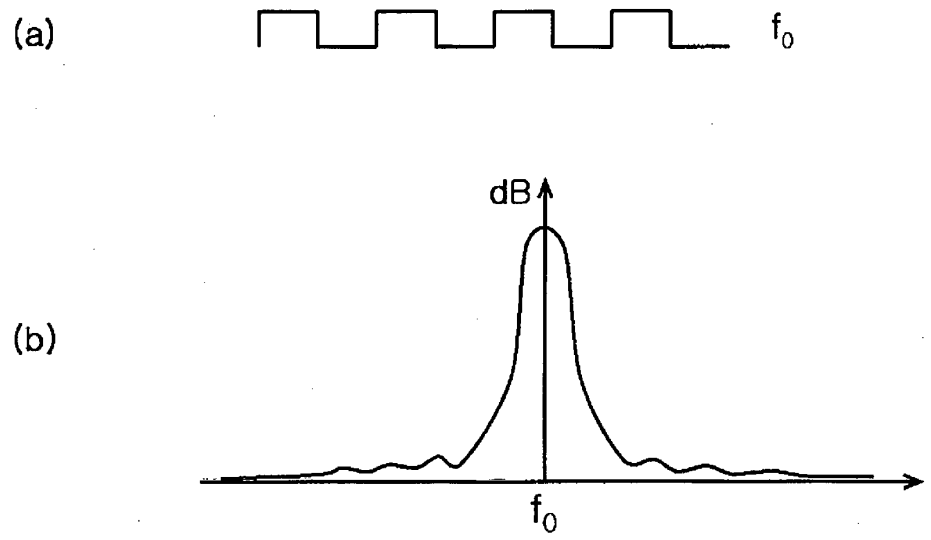

(a)
f_0
(b)
dB
f_0

FIG. 4

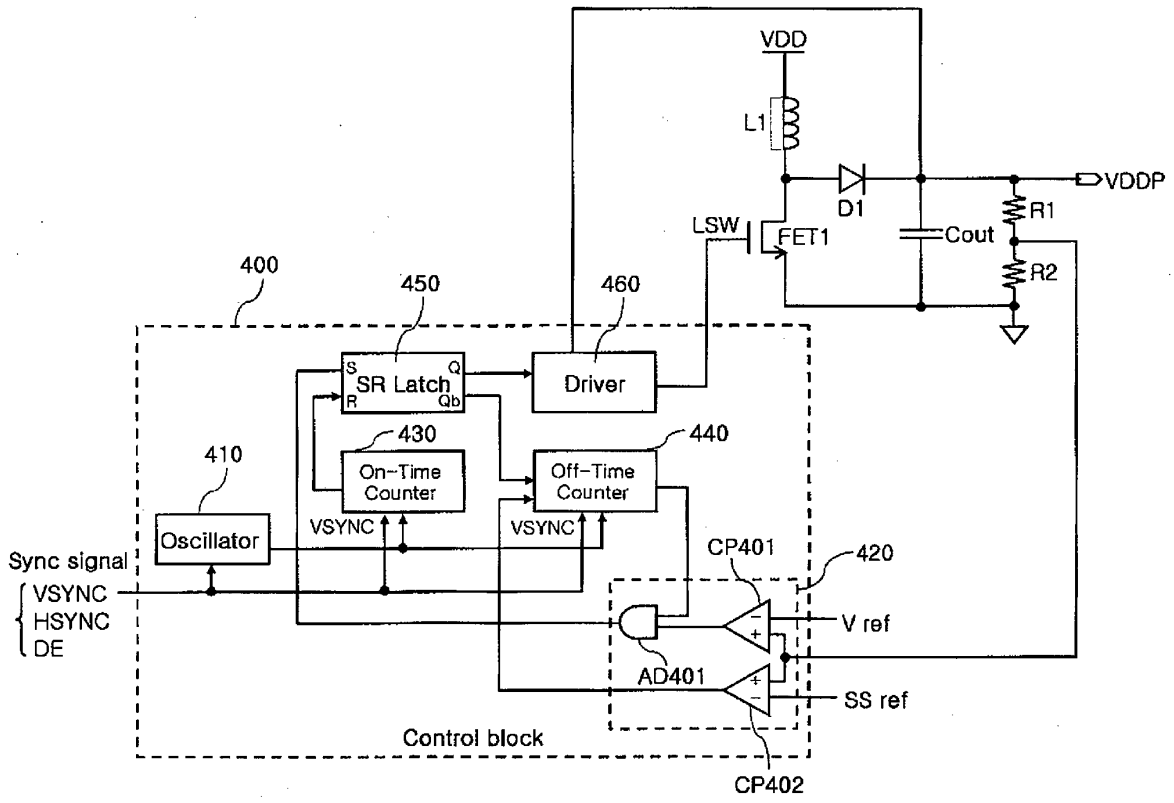

VDD
L1
D1
VDDP
R1
R2
Cout
LSW
FET1
400
450
460
SR Latch
S
R
Q
Qb
Driver
410
430
440
On-Time Counter
Off-Time Counter
Oscillator
VSYNC
VSYNC
Sync signal
VSYNC
HSYNC
DE
CP401
420
V ref
AD401
SS ref
Control block
CP402

FIG. 5

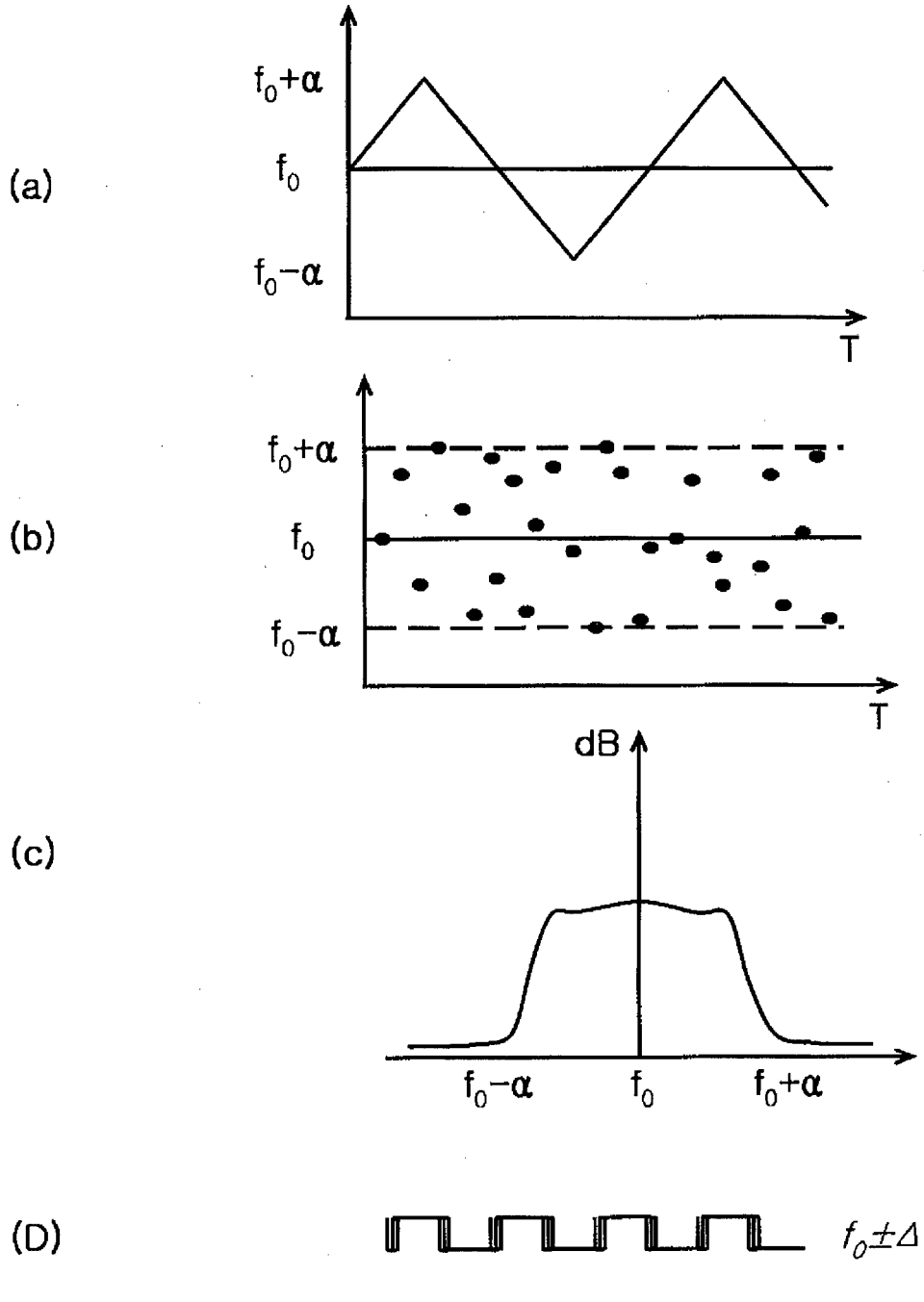

(a)
$f_0+\alpha$
f_0
$f_0-\alpha$
T
(b)
$f_0+\alpha$
f_0
$f_0-\alpha$
T
(c)
dB
$f_0-\alpha$
f_0
$f_0+\alpha$
(D)
$f_0\pm\Delta$

FIG. 6

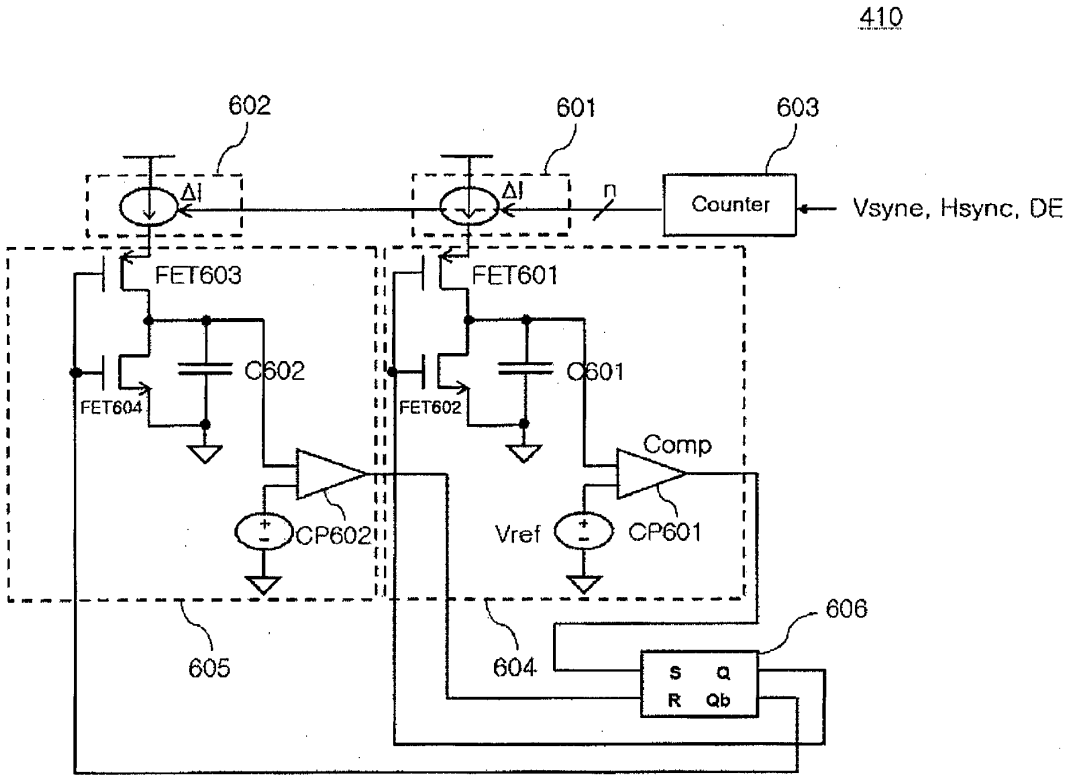

410
602
601
603
ΔI
ΔI
n
Counter
Vsyne, Hsync, DE
FET603
FET601
C602
C601
FET604
FET602
Comp
CP602
Vref
CP601
606
605
604
S Q
R Qb

FIG. 7

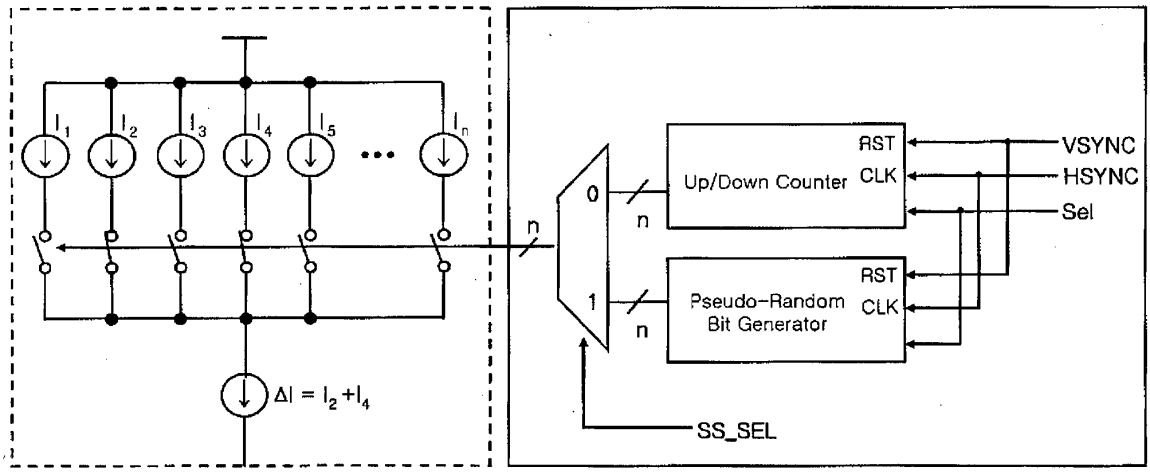

I1 I2 I3 I4 I5 ... In
ΔI = I2 +I4
n
0
1
n
n
Up/Down Counter
RST
CLK
Pseudo-Random Bit Generator
RST
CLK
VSYNC
HSYNC
Sel
SS_SEL

FIG. 8

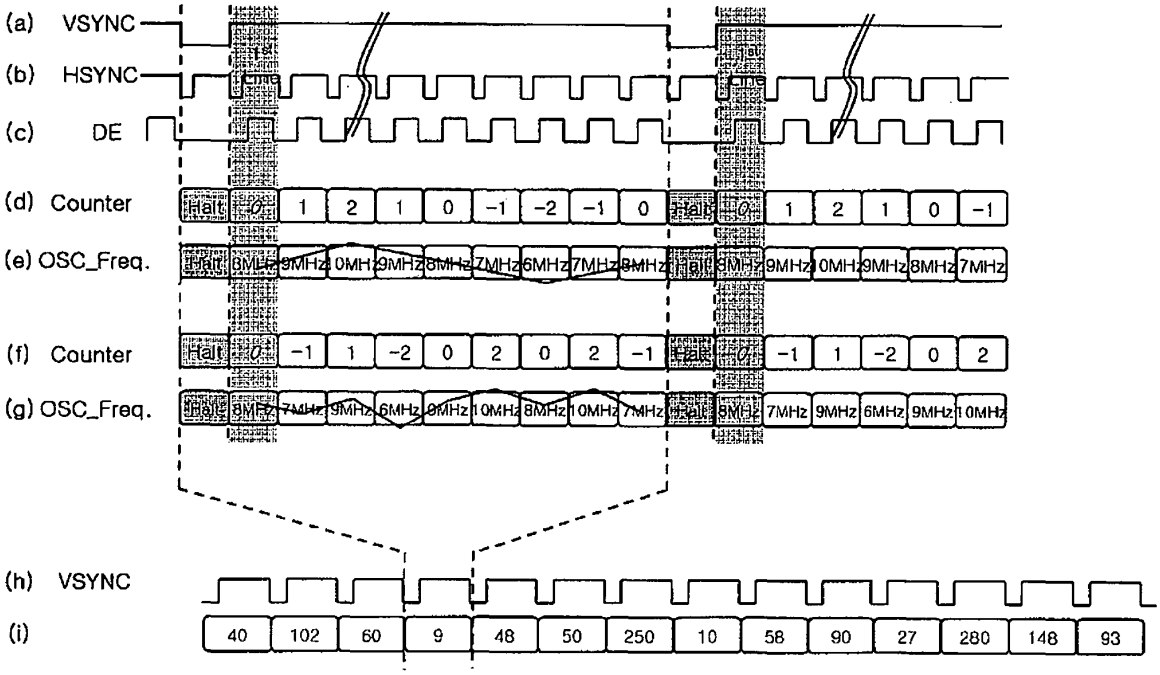

(a) VSYNC
(b) HSYNC
(c) DE
(d) Counter
(e) OSC_Freq.
(f) Counter
(g) OSC_Freq.
(h) VSYNC
(i)
Half
One
40
102
60
9
48
50
250
10
58
90
27
280
148
93

FIG. 9

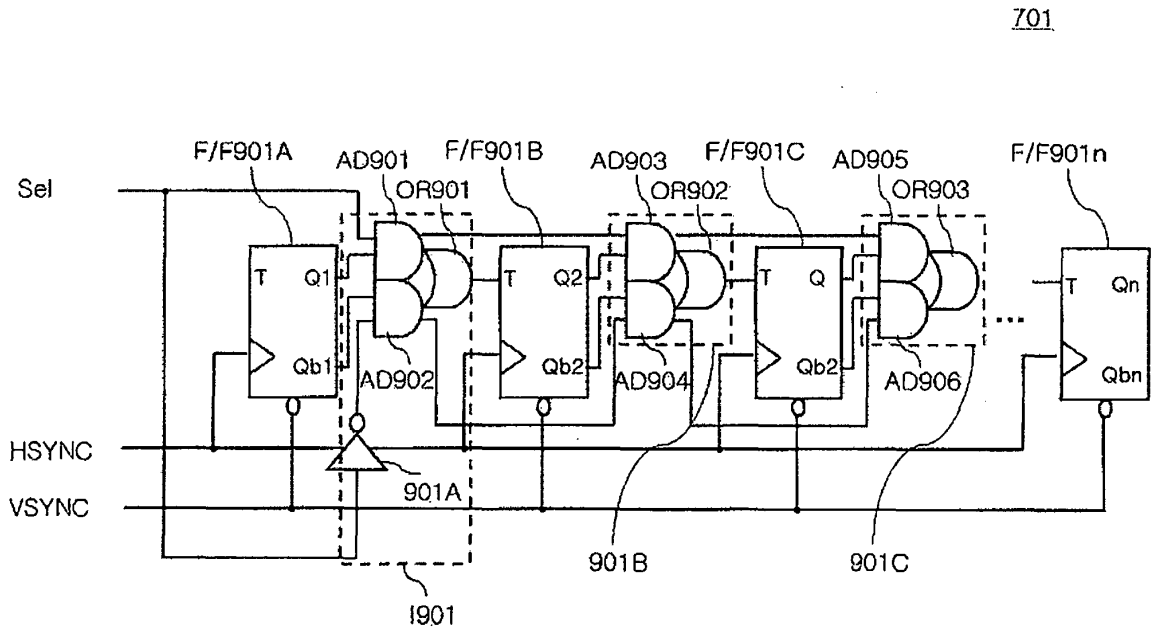

701
Sel
F/F901A
AD901
OR901
F/F901B
AD903
OR902
F/F901C
AD905
OR903
F/F901n
T
Q1
Qb1
Q2
Qb2
Q
Qn
Qbn
AD902
AD904
AD906
HSYNC
VSYNC
901A
901B
901C
1901

FIG. 10

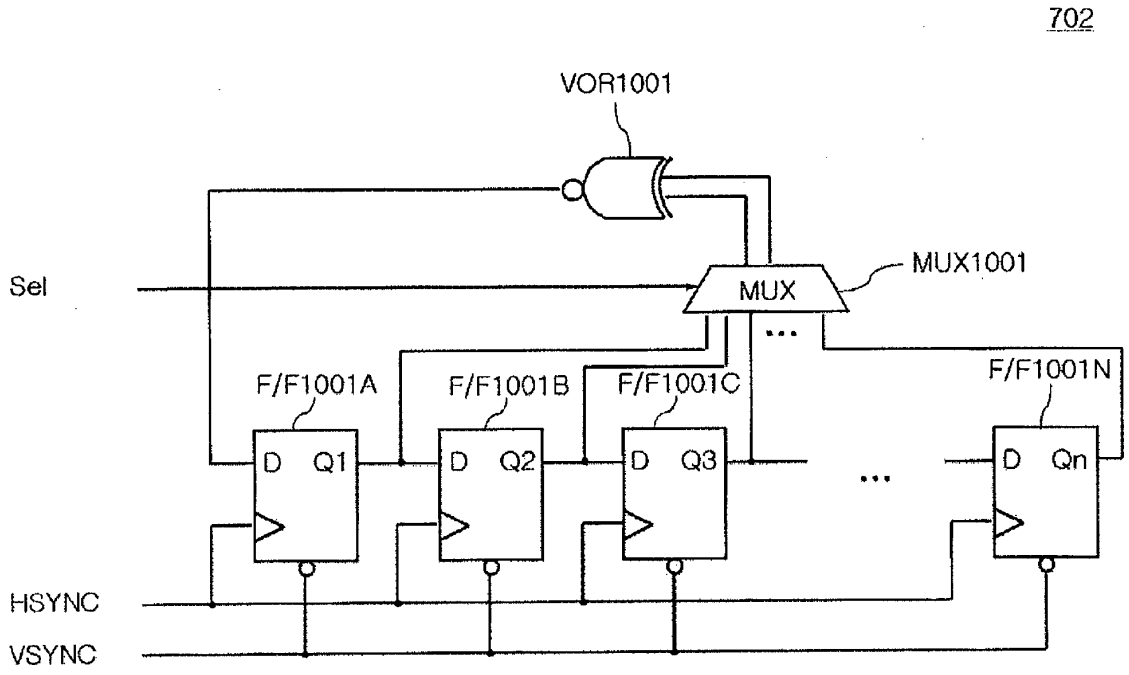

702
VOR1001
MUX1001
Sel
MUX
F/F1001A
F/F1001B
F/F1001C
F/F1001N
D Q1
D Q2
D Q3
D Qn
HSYNC
VSYNC

FIG. 11

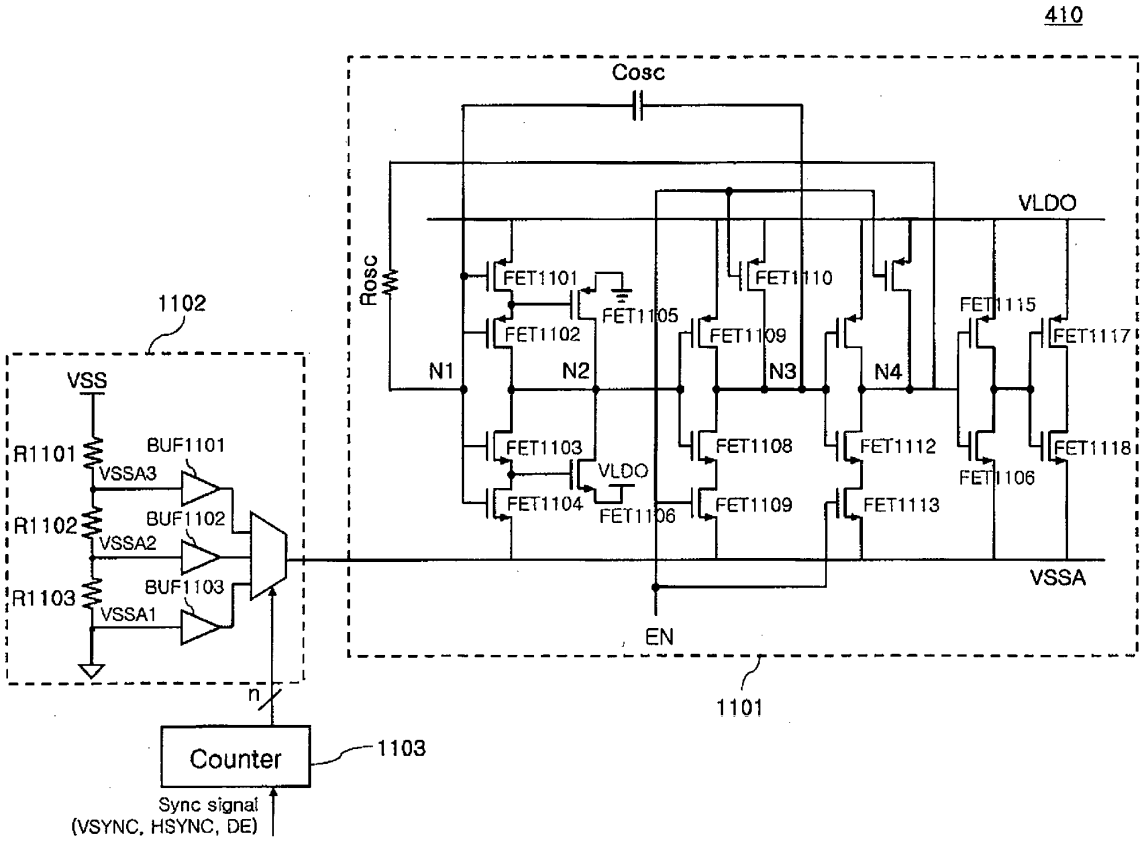

410
Cosc
VLDO
Rosc
FET1101
FET1105
FET1110
FET1102
FET1109
FET1115
FET1117
N1
N2
N3
N4
FET1103
FET1108
FET1112
FET1118
VLDO
FET1106
FET1104
FET1106
FET1109
FET1113
VSSA
EN
1101
1102
VSS
R1101
BUF1101
VSSA3
R1102
BUF1102
VSSA2
R1103
BUF1103
VSSA1
n
Counter
1103
Sync signal
(VSYNC, HSYNC, DE)

FIG. 12

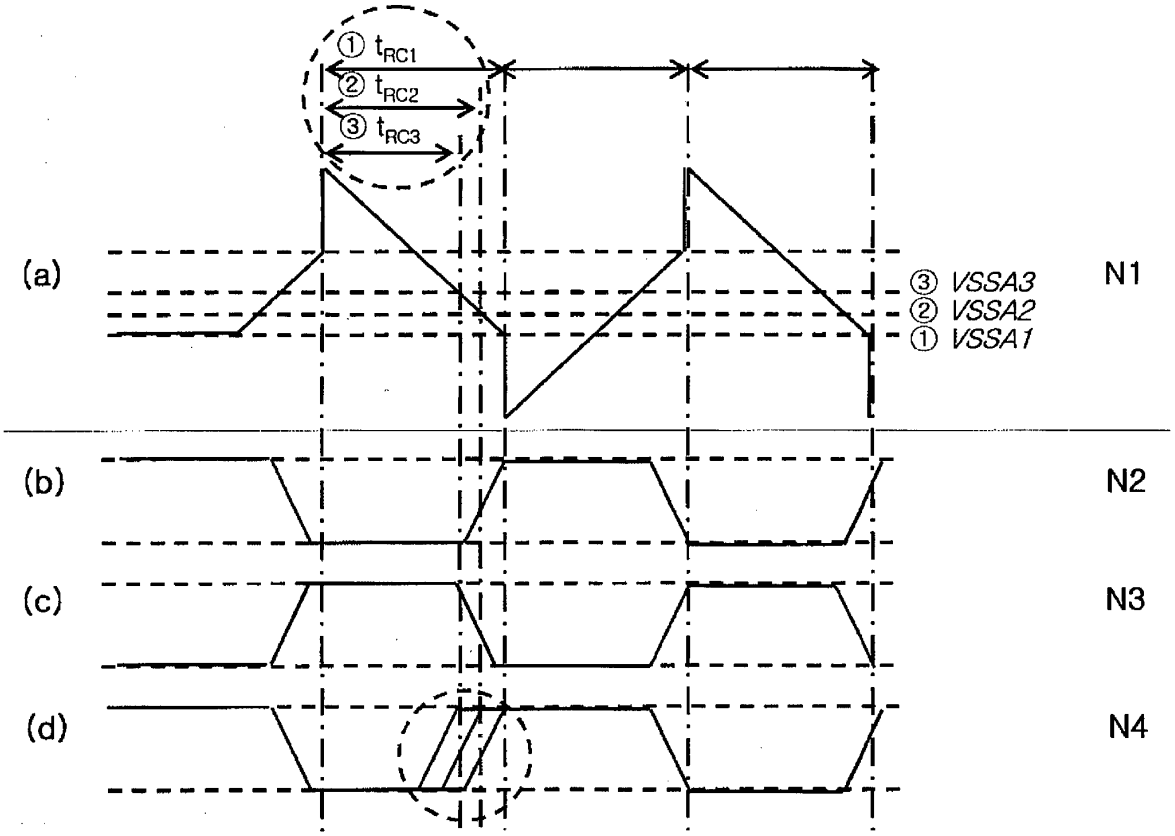


FIG. 13

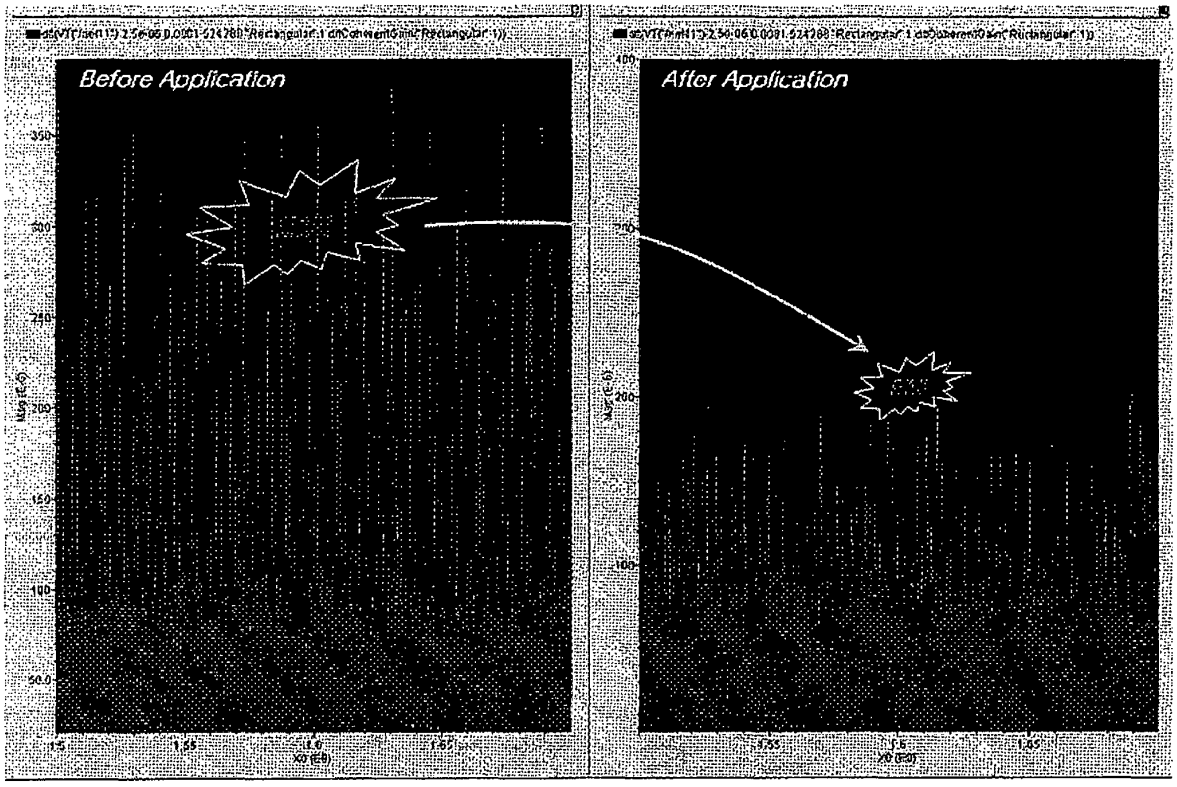
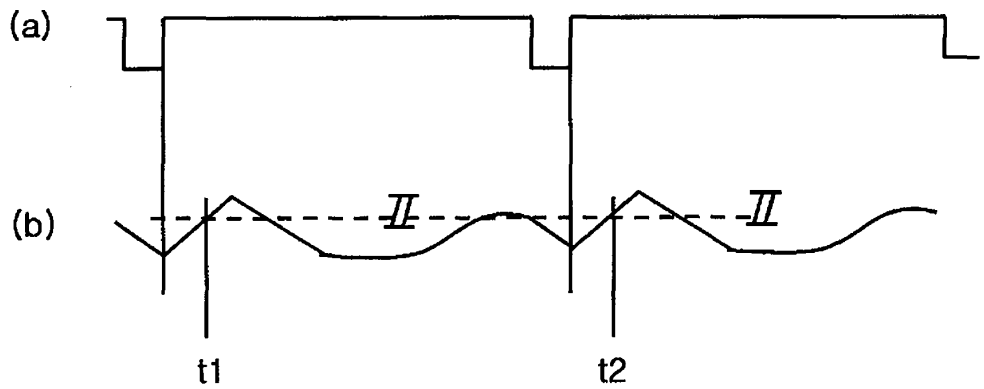


FIG. 14



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20080165167 A **[0021]**
- US 20090135171 A **[0022]**
- EP 1235335 A **[0023]**

专利名称(译)	用于液晶显示器的升压转换器		
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优先权	1020100042793 2010-05-07 KR		
其他公开文献	EP2393191A2 EP2393191A3		
外部链接	Espacenet		

摘要(译)

为了使LDI的升压转换器能够通过使用可变频率产生面板驱动电压来减少电磁干扰，同时每当每帧开始时使用相同的频率实现稳定的升压操作，振荡器产生具有频率以预定模式变化或以中心频率周围的随机模式跳跃，并且每当每帧开始时产生具有预设固定频率的振荡信号。

FIG. 1