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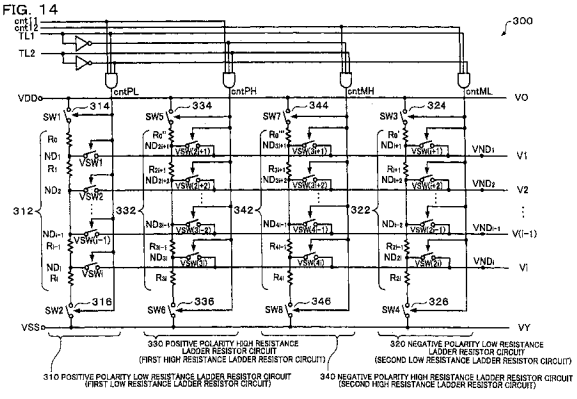
(54) Reference voltage generation circuit, display drive circuit, and display device

(57) A reference voltage generation circuit that generates multi-valued reference voltages for driving a liquid crystal display comprises: first to fourth ladder resistor circuit (312, 322, 332, 342) between first and second power source lines. First to i-th reference voltage output switching circuits (VSW1-VSWi) are respectively inserted between first to i-th division nodes (ND_1-ND_i) of the first ladder resistor circuit (312), where i is an integer larger than or equal to 2, and first to i-th reference voltage output nodes (VND_1-VND_i). (i + 1)th to 2i-th reference voltage output switching circuits (VSW(i+1)-VSW2i) are respectively inserted between (i + 1)th to 2i-th division nodes (ND_{i+1}-ND_{2i}) of the second ladder resistor circuit (322) and the first to i-th reference voltage output nodes. (2i + 1)th to 3i-th reference voltage output switching circuits (VSW(2i+1)-VSW(3i)) are respectively inserted between (2i + 1)th to 3i-th division nodes (ND_{2i+1}-ND_{3i}) of the third ladder resistor circuit (332) and the first to i-th reference voltage output nodes. (3i + 1)th to 4i-th reference voltage output switching circuits (VSW(3i+1)-VSW(4i)) are respectively inserted between (3i + 1)th to 4i-th division nodes (ND_{3i+1}-ND_{4i}) of the fourth ladder resistor circuit (342) and the first to i-th reference voltage output nodes. When polarity inversion of a voltage outputted by a polarity inversion drive system to a signal electrode at a given polarity inversion period is repeated: the first to i-th reference voltage output switching circuits are switched on during a given control period in a positive polarity driving period and switched off during a given control period in a negative polarity driving period; the (i + 1)th to 2i-th reference voltage output switching circuits are switched off during a given control period in the positive polarity driving period and switched on during a given control period in the negative polarity driving period; the (2i + 1)th to 3i-th reference voltage output switching circuits are switched on during the positive polarity driving period and switched off during the negative polarity driving period; and the (3i + 1)th to 4i-th reference voltage output switching circuits are switched on during the positive polarity driving period and switched off during the negative polarity driving period.

FIG. 14



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EUROPEAN SEARCH REPORT

Application Number
EP 05 00 6584

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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A	US 5 796 379 A (ENOMOTO ET AL) 18 August 1998 (1998-08-18) * column 7, line 45 - column 11, line 67; figures 1,2,6 * -----	1-3	
A	EP 0 852 372 A (SEIKO EPSON CORPORATION) 8 July 1998 (1998-07-08) * column 11, line 26 - column 17, line 25; figures 7-15 * -----	1-3	
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A	US 5 648 791 A (DATE ET AL) 15 July 1997 (1997-07-15) * abstract; figures 1,15,16,20 * -----	1-3	

TECHNICAL FIELDS SEARCHED (IPC)

G09G
H04N
H03M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	11 January 2006	Fulcheri, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 05 00 6584

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	参考电压产生电路，显示驱动电路和显示装置		
公开(公告)号	EP1551004A3	公开(公告)日	2006-03-08
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申请(专利权)人(译)	SEIKO EPSON CORPORATION		
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CPC分类号	G09G3/3688 G09G3/2011 G09G3/32 G09G3/3233 G09G3/325 G09G3/3614 G09G3/3685 G09G3/3696 G09G5/06 G09G2300/0842 G09G2300/0861 G09G2310/0248 G09G2310/0251 G09G2310/027 G09G2310/04 G09G2320/0276		
优先权	2002032680 2002-02-08 JP		
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摘要(译)

产生用于驱动液晶显示器的多值参考电压的参考电压产生电路包括：第一和第二电源线之间的第一至第四梯形电阻电路（312,322,332,342）。第一至第i参考电压输出切换电路（VSW1-VSWi）分别插入第一梯形电阻电路（312）的第一至第i分割节点（ND1-NDi）之间，其中i是大于或等于的整数到2，并且第一到第i个参考电压输出节点（VND1-VNDi）。第（i + 1）个第2i参考电压输出切换电路（VSW（i + 1）-VSW2i）分别插入在第（i + 1）至第2i分割节点（NDi + 1-ND2i）之间。第二梯形电阻器电路（322）和第一至第i参考电压输出节点。（2i + 1）至第3i参考电压输出切换电路（VSW（2i + 1）-VSW（3i））分别插入在第（2i + 1）至第3i分割节点（ND2i + 1-ND3i）之间）第三梯形电阻电路（332）和第一至第i参考电压输出节点。（3i + 1）至第4i参考电压输出切换电路（VSW（3i + 1）-VSW（4i））分别为插入在第四梯形电阻电路（342）的第（3i + 1）至第4i分割节点（ND3i + 1-ND4i）与第一至第i参考电压输出节点之间。当极性反转驱动系统在给定极性反转周期内向信号电极输出的电压的极性反转被重复时：第一至第i参考电压输出开关电路在正极性驱动的给定控制周期期间接通。在一个负极性驱动周期的给定控制周期内关闭周期;第（i + 1）至第2i参考电压输出切换电路在正极性驱动时段中的给定控制时段期间被关断，并且在负极性驱动时段中的给定控制时段期间被接通;第（2i + 1）至第3i参考电压输出切换电路在正极性驱动期间接通，在负极性驱动期间切断。第（3i + 1）至第4i参考电压输出切换电路在正极性驱动期间接通，在负极性驱动期间断开期。

FIG. 14