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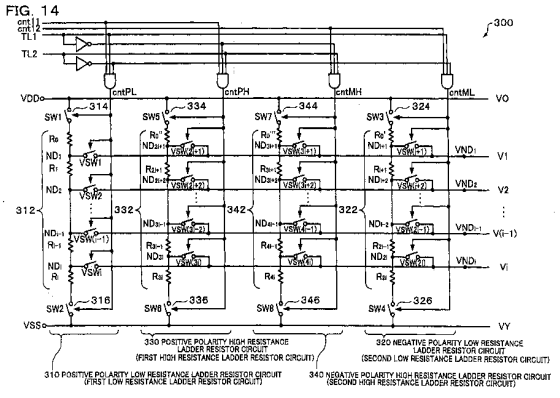
(54) Reference voltage generation circuit, display drive circuit, and display device

(57) A reference voltage generation circuit that generates multi-valued reference voltages for driving a liquid crystal display comprises: first to fourth ladder resistor circuit (312, 322, 332, 342) between first and second power source lines. First to i-th reference voltage output switching circuits (VSW1-VSWi) are respectively inserted between first to i-th division nodes (ND_1-ND_i) of the first ladder resistor circuit (312), where i is an integer larger than or equal to 2, and first to i-th reference voltage output nodes (VND_1-VND_i). (i + 1)th to 2i-th reference voltage output switching circuits (VSW(i+1) -VSW2i) are respectively inserted between (i + 1)th to 2i-th division nodes (ND_{i+1}-ND_{2i}) of the second ladder resistor circuit (322) and the first to i-th reference voltage output nodes. (2i + 1)th to 3i-th reference voltage output switching circuits (VSW(2i+1)-VSW(3i)) are respectively inserted between (2i + 1)th to 3i-th division nodes (ND_{2i+1}-ND_{3i}) of the third ladder resistor circuit (332) and the first to i-th reference voltage output nodes. (3i + 1)th to 4i-th reference voltage output switching circuits (VSW(3i+1)-VSW(4i)) are respectively inserted between (3i + 1)th to 4i-th division nodes (ND_{3i+1}-ND_{4i}) of the fourth ladder resistor circuit (342) and the first to i-th reference voltage output nodes. When polarity inversion of a voltage outputted by a polarity inversion drive system to a signal electrode at a given polarity inversion period is repeated: the first to i-th reference voltage output switching circuits are switched on during a given control period in a positive polarity driving period and switched off during a given control period in a negative polarity driving period; the (i + 1)th to 2i-th reference voltage output switching circuits are switched off during a given control period in the positive polarity driving period and switched on during a given control period in the negative polarity driving period; the (2i + 1)th to 3i-th reference voltage output switching circuits are switched on during the positive polarity driving period and switched off during the negative polarity driving period; and the (3i + 1)th to 4i-th reference voltage output switching circuits are switched on during the positive polarity driving period and switched off during the negative polarity driving period.

FIG. 14



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Description

BACKGROUND

[0001] The present invention relates to a reference voltage generation circuit, a display drive circuit and a display device.

[0002] Small-sized formation and highly fine formation are required in a display device represented by an electro-optical device of a liquid crystal device and the like. Among them, a liquid crystal device realizes low power consumption and is frequently mounted on a portable electronic device. For example, when a liquid crystal device is mounted as a display portion of a portable telephone, there is requested display of image rich in color tone by many gray scales formation.

[0003] Generally, an image signal for displaying an image is subjected to gamma correction in accordance with a display characteristic of a display device. The gamma correction is carried out by a gamma correction circuit (in wide sense, reference voltage generation circuit). Taking an example of a liquid crystal device, a gamma correction circuit generates voltage in accordance with transmittance of a pixel based on gray scale data for carrying out gray scale display.

[0004] Such a gamma correction circuit can be constituted by a ladder resistor. In this case, voltages across two opposed ends of respective resistor circuits constituting the ladder resistor are outputted as multi-valued reference voltages in accordance with gray scale value.

[0005] Now, in order to prevent a deterioration in, for example, a liquid crystal, there is carried out polarity inversion drive for inverting a polarity of a voltage applied to the liquid crystal at a given period. Therefore, it is necessary to correct the voltage to an optimum reference voltage at each time of inverting the polarity since a display characteristic is not symmetric. Therefore, a voltage of a power source inserted with a ladder resistor is alternately applied at a polarity inversion period, charge and discharge time period therefor cannot sufficiently be ensured and resistance ratios of the ladder resistor must be reduced. Thereby, current flowing to the ladder resistor is increased and power consumption is increased.

[0006] US-A-5,617,091 discloses a resistance ladder for a D-A converter which divides a potential difference between two power sources into 2^m levels by a resistance group in the center portion, then adjusting the number of resistors which are disposed at the two end portions of the resistance ladder and interposed between the resistors of the center portion and the two power sources so that the division voltages of 2^m levels are changed in (n-m) levels, with the result that the potential difference is divided into 2^n levels.

[0007] US-A-5,796,379 discloses a reference voltage generation circuit according to the pre-characterizing portion of claim 1. More particularly, thie document describes a gray-scale level voltage generation circuit in the form of a resistor array D-A converter. 16 series connected resistors of a first resistor ladder generate 16 positive voltages corresponding to 16 gray-scale levels using 5 reference voltages. Likewise, 16 series connected resistors of a second resistor ladder generate 16 negative voltages corresponding to 16 gray-scale levels using five reference voltages. Positive gray-scale level voltage lines and negative gray-scale level voltage lines, which are associated with the same gray-scale levels, are juxtaposed in pairs and arranged alternately in order of gray-scale voltage.

SUMMARY

[0008] It is an object of the present invention to provide a reference voltage generation circuit, a display drive circuit and a display device capable of reducing consumption of current even when the polarity inversion drive is carried out.

[0009] This object is achieved by a reference voltage generation circuit as claimed in claim 1 and its preferred uses as claimed in claims 2 and 3.

[0010] According to this configuration, by generating the reference voltages by using the first and second lower resistance ladder resistor circuits (i.e., first ladder resistor circuit and second ladder resistor circuit) and the first and second higher resistance ladder resistor circuits (i.e., third ladder resistor circuit and fourth ladder resistor circuit) in accordance with the polarity inversion period timing in the polarity inversion drive system, it is not necessary to alternately switch the first and second power source voltages and therefore, by reducing charge and discharge of the nodes accompanied by the switching, consumption of current can be reduced. Further, in a given control period in each of the driving periods, by using both of the first and second low resistance ladder resistor circuits and the first and second high resistance ladder resistor circuits, a charge time period of the division node can be ensured. Even when the driving period is shortened, the charge time period can still be ensured.

[0011] That is, in the driving period, in a state in which the first and second high resistance ladder resistor circuits are connected to the first and second power source lines, in a given control period in the driving period, the first and second low resistance ladder resistor circuits are connected to the first and second power source lines. In a state in which the first and second high resistance ladder resistor circuits and the first and second low resistance ladder resistor circuits are respectively connected to the first and second power source lines, current flows to the side of the first and second low resistance ladder resistor circuits having a low total resistance value. Therefore, control of connecting the first and second high resistance ladder resistor circuits to the first and second power source lines can be simplified. Further, when the control period is provided at an earlier portion of the driving period, the division nodes are driven to a given voltage via the ladder resistor circuit having

a low resistance value and therefore, a time constant determined by a load capacitance of the division node can be reduced and the charge time period can be shortened. Further, after elapse of the control period, by the first and second high resistance ladder resistor circuits, accurate reference voltage is generated. Thereby, an increase in current by using the first and second low resistance ladder resistor circuits, can be minimized and ensuring of the above-described charge time period and low power consumption can be made compatible.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0012]

Fig. 1 is a constitutional diagram schematically showing a constitution of a display device to which a display drive circuit including a reference voltage generation circuit is applied;

Fig. 2 is a functional block diagram of a signal driver IC to which a display drive circuit including a reference voltage generation circuit is applied;

Fig. 3A is a schematic view of a signal driver IC for driving a signal electrode by a unit of block and Fig. 3B shows an outline of a partial block selection register;

Fig. 4 is a view schematically showing vertical band partial display;

Fig. 5 is a view for describing principle of gamma correction;

Fig. 6 is a constitutional diagram showing a principle constitution of a reference voltage generation circuit;

Fig. 7 is a constitutional diagram schematically showing a constitution of a reference voltage generation circuit according to a first constitution example;

Fig. 8 is a timing chart showing an example of a control timing of the reference voltage generation circuit according to the first constitution example;

Fig. 9 is a constitutional diagram schematically showing a constitution of a reference voltage generation circuit according to a second constitution example;

Fig. 10 is a constitutional diagram schematically showing a constitution of a reference voltage generation circuit according to a third constitution example;

Fig. 11 is a constitutional diagram showing a specific constitution example of DAC and a voltage follower circuit;

Fig. 12A shows a switching state of a switching circuit in each mode and Fig. 12B is a circuit diagram showing an example of a circuit of generating a switching control signal;

Fig. 13 is a timing chart showing an example of an operational timing of a normal drive mode in a voltage follower circuit;

Fig. 14 is a constitutional diagram schematically showing a constitution of a reference voltage generation circuit according to a fourth constitution example;

Fig. 15 is a timing chart showing an example of a control timing of the reference voltage generation circuit according to the fourth constitution example;

Fig. 16 is a constitutional diagram showing an example of a pixel circuit of a 2 transistor system in an organic EL panel; and

Fig. 17A is a circuit constitutional diagram showing an example of a pixel circuit of a 4 transistor system in an organic EL panel and Fig. 17B is a timing chart showing an example of a display control timing of the pixel circuit.

DETAILED DESCRIPTION

[0013] A detailed description will be given of embodiments in reference to the drawings as follows. Note that the embodiments described hereunder do not in any way limit the scope of the invention defined by the claims laid out herein. Note also that all of the elements to be described below should not be taken as essential requirements to the means of the present invention.

[0014] A reference voltage generation circuit according to the embodiment can be used as a gamma correction circuit. The gamma correction circuit is included in a display drive circuit. The display drive circuit can be used in driving an electro-optical device for changing an optical characteristic by applied voltage, for example, a liquid crystal device.

[0015] Although a description will be given of a case of applying a reference voltage generation circuit according to the embodiment to a liquid crystal device as follows, the invention is not limited thereto but applicable to other display device.

1. Display device

[0016] Fig. 1 shows an outline of a constitution of a display device to which a display drive circuit including a reference voltage generation circuit according to the embodiment is applied.

[0017] A display device (in narrow sense, electro-optical device, liquid crystal device) 10 can include a display panel (in narrow sense, liquid crystal panel) 20.

[0018] The display panel 20 is formed on, for example, a glass substrate. There are arranged scan electrodes (gate lines) G_1 to G_N (N is a natural number larger than or equal to 2) arranged in Y-direction and extending in X-direction and signal electrodes (source line) S_1 to S_M (M is a natural number larger than or equal to 2) arranged in X-direction and extending in Y-direction. Further, a pixel region (pixel) is provided in correspondence with an intersection of a scan electrode G_n ($1 \leq n \leq N$, n is a natural number) and a signal electrode S_m ($1 \leq m \leq M$, m is a natural number) and a thin film transistor (hereinafter, abbreviated as TFT) 22_{nm} is arranged at the pixel region.

[0019] A gate electrode of TFT 22_{nm} is connected to the scan electrode G_n. A source electrode of TFT 22_{nm} is connected to the signal electrode S_m. A drain electrode of TFT 22_{nm} is connected to a pixel electrode 26_{nm} of a liquid crystal capacitor (in a broad sense, a liquid crystal element) 24_{nm}.

[0020] The liquid crystal capacitor 24_{nm} is formed by sealing liquid crystals between the pixel electrode 26_{nm} and an opposed electrode 28_{nm} opposed thereto and the transmittance of the pixel is changed in accordance with voltage applied between the electrodes. The opposed electrode 28_{nm} is supplied with opposed electrode voltage Vcom.

[0021] The display device 10 can include a signal driver IC 30. As the signal driver IC 30, a display drive circuit according to the embodiment can be used. The signal driver IC 30 drives the signal electrodes S_1 to S_M of the display panel 20 based on image data.

[0022] The display device 10 can include a scan driver IC 32. The scan driver IC 32 successively drives the scan electrodes G_1 to G_N of the display panel 20 in one vertical scan period.

[0023] The display device 10 can include a power source circuit 34. The power source circuit 34 generates voltage necessary for driving the signal electrode and supplies the voltage to the signal driver IC 30. Further, the power source circuit 34 generates voltage necessary for driving the scan electrode and supplies the voltage to the scan driver IC 32. Further, the power source circuit 34 can generate the opposed electrode voltage Vcom.

[0024] The display device 10 can include a common electrode drive circuit 36. The common electrode drive circuit 36 is supplied with the opposed electrode voltage Vcom generated by the power source circuit 34 and outputs the opposed electrode voltage Vcom to the opposed electrode of the display panel 20.

[0025] The display device 10 can include a signal control circuit 38. The signal control circuit 38 controls the signal driver IC 30, the scan driver IC 32 and the power source circuit 34 in accordance with content set by a host of a central processing unit (hereinafter, abbreviated as CPU), not illustrated. For example, the signal control circuit 38 sets an operation mode and supplies a vertical synchronizing signal and a horizontal synchronizing signal generated at inside thereof to the signal driver IC 30 and the scan driver IC 32 and controls a polarity inversion timing for the power source circuit 34.

[0026] Further, although in Fig. 1, the display device 10 is constituted to include the power source circuit 34, the common electrode drive circuit 36 or the signal control circuit 38, the display device 10 may be constituted by providing at least one of these at outside of the display device 10. Or, the display device 10 can be constituted to include a host.

[0027] Further, in Fig. 1, at least one of a display drive circuit having a function of the signal driver IC 30 and a scan electrode drive circuit having a function of the scan driver IC 32 may be formed on a glass substrate formed with the display panel 20.

[0028] In the display device 10 having such a constitution, the signal driver IC 30 outputs voltage in correspondence with gray scale data to the signal electrode to display gray scale based on the gray scale data. The signal driver IC 30 subjects the voltage to be outputted to the signal electrode to gamma correction based on the gray scale data. For such purpose, the signal driver IC 30 includes a reference voltage generation circuit for carrying out gamma correction (in narrow sense, gamma correction circuit).

[0029] Generally, the display panel 20 is provided with a gray scale characteristic which differs in accordance with a structure thereof or a liquid crystal material used. That is, a relationship between voltage to be applied to a liquid crystal and a transmittance of a pixel is not constant. Hence, in order to generate optimum voltage to be applied to a liquid crystal in accordance with gray scale data, gamma correction is carried out by the reference voltage generation circuit.

[0030] In order to optimize voltage outputted based on gray scale data, in gamma correction, multi-valued voltages generated by a ladder resistor are corrected. In such a case, a resistance ratio of a resistor circuit for constituting a ladder resistor is determined to generate voltage designated by a maker of fabricating the display panel 20 or the like.

2. Signal driver IC

[0031] Fig. 2 shows a functional block diagram of the signal driver IC 30 to which a display drive circuit including a reference voltage generation circuit according to the embodiment is applied.

[0032] The signal driver IC 30 includes an input latch

circuit 40, a shift register 42, a line latch circuit 44, a latch circuit 46, a partial block selection register 48, a reference voltage selection circuit (in narrow sense, gamma correction circuit) 50, DAC (Digital/Analog Converter) (in a broad sense, voltage selection circuit) 52, an output control circuit 54 and a voltage follower circuit (in a broad sense, signal electrode drive circuit) 56.

[0033] The input latch circuit 40 latches gray scale data comprising RGB signals each comprising 6 bits supplied from the signal control circuit 38 shown in Fig. 1 based on a clock signal CLK. The clock signal CLK is supplied from the signal control circuit 38.

[0034] The gray scale data latched by the input latch circuit 40 is successively shifted in the shift register 42 based on the clock signal CLK. The gray scale data inputted by being successively shifted in the shift register 42 is inputted to the line latch circuit 44.

[0035] The gray scale data inputted to the line latch circuit 44 is latched by the latch circuit 46 at a timing of a latch pulse signal LP. The latch pulse signal LP is inputted at a horizontal scan period timing.

[0036] The partial block selection register 48 holds partial block selection data. The partial block selection data is set via the input latch circuit 40 by a host, not illustrated. When 1 block is constituted by, for example, 24 outputs (for 8 pixels when 1 pixel comprises 3 dots of R, G, B) of a plurality of signal electrodes driven by the signal driver IC 30, the partial block selection data is data for setting a display line in correspondence with signal electrodes by a unit of block to a display state or a non-display state.

[0037] Fig. 3A schematically shows the signal driver IC 30 for driving signal electrodes by a unit of block and Fig. 3B shows an outline of a partial block selection register 48.

[0038] According to the signal driver IC 30, as shown by Fig. 3A, signal electrode drive circuits are arranged in a long side direction in correspondence with signal electrodes of a display panel constituting an object for driving. The signal electrode drive circuits are included in the voltage follower circuit 56 shown in Fig. 2. The partial block selection register 48 shown in Fig. 3B holds partial block selection data for setting display lines to the display state or the non-display state for each of blocks. Each of the blocks is formed of the display lines corresponding to the signal electrodes for "k" (for example "24") outputs of signal electrode drive circuits. In this case, the signal electrode drive circuits are divided into blocks B0 to Bj (j is a positive integer of 1 or more) and the partial block selection register 48 is inputted with partial block selection data BLK0_PART to BLKj_PART in correspondence with the respective blocks from the input latch circuit 40. When partial block selection data BLKz_PART ($0 \leq z \leq j$, z is an integer) is, for example, "1", the display line in correspondence with the signal electrodes of the block Bz is set to the display state. When the partial block selection data BLKz_PART is, for example, "0", the display line in correspondence with the signal electrodes of the block Bz is set to the non-display state.

[0039] The signal driver IC 30. outputs drive voltage in correspondence with gray scale data to signal electrodes of a block set to the display state. Further, signal electrodes of a block set to the non-display state are outputted with, for example, a given drive voltage and display in correspondence with gray scale data is not carried out. For example, when display lines in correspondence with signal electrodes of blocks B0 to Bx0 and Bx1 to Bj are set to the non-display state, and a display line in correspondence with signal electrodes of blocks Bx0' to Bx1' (X0' = x0 + 1, x1' = x1 - 1), partial non-display areas 58A and 58B and a partial display area 60 are provided and partial display of vertical bands can be carried out on the display panel 20 as shown by Fig. 4.

[0040] In Fig. 2, by using resistance ratios of ladder resistors determined to optimize gray scale display of the display panel constituting the object for driving, the reference voltage generation circuit 50 outputs multi-valued reference voltages V0 to VY (Y is a natural number) generated at division nodes produced by dividing a resistor between power source voltage on a high potential side (first power source voltage) V0 and power source voltage on a low potential side (second power source voltage) VSS.

[0041] Fig. 5 shows a diagram for describing principle of gamma correction.

[0042] A diagram of a gray scale characteristic showing a change in a transmittance of a pixel to voltage applied to a liquid crystal is shown here. When the transmittance of a pixel is designated by 0% to 100% (or 100% to 0%), generally, the smaller or the larger the voltage applied to the liquid crystal, the smaller the change in the transmittance. Further, the change in the transmittance is increased at a region at a vicinity of a middle of the voltage applied to the liquid crystal.

[0043] Hence, by carrying out gamma (γ) correction for changing the transmittance reversely to the above-described change in the transmittance, the transmittance subjected the gamma correction which is changed linearly in accordance with the applied voltage can be realized. Therefore, reference voltage V_γ for realizing an optimized transmittance can be generated based on gray scale data which is digital data. That is, the resistance ratios of the ladder resistors may be realized to generate such reference voltage.

[0044] Multi-valued reference voltages V0 to VY generated by the reference voltage generation circuit 50 in Fig. 2 are supplied to DAC 52.

[0045] DAC 52 selects any voltages of multi-valued reference voltages V0 to VY based on the gray scale data supplied from the latch circuit 46 and outputs the voltages to the voltage follower circuit (in a broad sense, signal electrode drive circuit) 56.

[0046] The output control circuit 54 controls an output of the voltage follower circuit 56 by using an output en-

able signal XOE for controlling to drive the signal electrode and partial block selection data BLK0_PART to BLKj_PART.

[0047] The voltage follower circuit 56 carries out, for example, impedance conversion to drive corresponding signal electrodes in accordance with a control by the output control circuit 54.

[0048] In this way, the signal driver IC 30 outputs the signals by carrying out impedance conversion by using voltages selected from multi-valued reference voltages based on gray scale data for respective signal electrodes.

[0049] Meanwhile, the reference voltage generation circuit 50 can control current flowing in the ladder resistor based on at least one of the output enable signal XOE, the latch pulse signal LP indicating a horizontal scan period timing (in a broad sense, scan period of timing) and partial block selection data BLKO_PART to BLKj_PART. Thereby, current can be made to flow to the ladder resistor only during a time period of displaying gray scale based on the generated reference voltage and low power consumption can be achieved.

[0050] Next, the reference voltage generation circuit 50 will be described in details.

3. Reference voltage generation circuit

[0051] Fig. 6 shows a principle constitution of the reference voltage generation circuit 50.

[0052] The reference voltage generation circuit 50 includes a ladder resistor circuit 70 connected with a plurality of resistor circuits in series. Each of the resistor circuits constituting the ladder resistor circuit 70 can be constituted by, for example, a single or a plurality of resistor elements. Further, each of the resistor circuits can also be constituted to make a resistor value thereof variable by connecting resistor elements or resistor elements and a single or a plurality of switching elements in series or in parallel.

[0053] The ladder resistor circuit 70 is divided by the resistor circuits to form first to i-th (i is an integer larger than or equal to 2) division nodes ND_1 to ND_i. Voltages of the first to i-th division nodes ND_1 to ND_i are outputted to first to i-th reference voltage output nodes as multi-valued first to i-th reference voltages V1 to Vi. DAC 52 is supplied with first to i-th reference voltages V1 to Vi and reference voltages V0 and VY (= VSS).

[0054] The reference voltage generation circuit 50 includes first and second switching circuits (SW1, SW2) 72 and 74. The first switching circuit 72 is inserted between one end of the ladder resistor circuit 70 and a first power source line supplied with power source voltage (first power source voltage) V0 on the high potential side. The second switching circuit 74 is inserted between other end of the ladder resistor circuit 70 and a second power source line supplied with power source voltage (second power source voltage) VSS on the low potential side. On/off state of the first switching circuit 72 is controlled based on a first switching control signal cnt1. On/off state of the second switching circuit 74 is controlled based on a second switching control signal cnt2. The first and second switching circuits 72 and 74 can be constituted by, for example, MOS transistors. The first and second switching control signals cnt1 and cnt2 may be generated based on the same given control signal or may be generated as separate control signals.

[0055] The reference voltage generation circuit 50 having such a constitution can restrain consumption of current flowing to the ladder resistor circuit 70 by controlling off state of the first and second switching circuits 72 and 74 by the first and second switching control signals (first or second switching control signal when the first and second switching circuits 72 and 74 are controlled by the same switching control signal) during a time of, for example, not driving by using first to i-th reference voltages V1 to Vi outputted from the ladder resistor circuit 70 (given driving period based on first to i-th reference voltages).

3.1 First constitution example

[0056] Fig. 7 shows an outline of a constitution of a reference voltage generation circuit according to a first constitution example.

[0057] A reference voltage generation circuit 100 according to the first constitution example includes a ladder resistor circuit 102. The ladder resistor circuit 102 includes resistor circuits (in narrow sense, resistor elements) R_0 to R_i connected in series and first to i-th reference voltages V1 to Vi are outputted from first to i-th division nodes ND_1 to ND_i which are formed by dividing the ladder resistor circuit by the resistor circuits R_0 to R_i.

[0058] In Fig. 7, reference voltage V0 to V63 necessary for displaying 64 gray scales are supplied to DAC. Among them, reference voltages V1 to V62 are outputted from the ladder resistor circuit 102 of the reference voltage generation circuit 100. That is, the ladder resistor circuit 102 includes resistor elements R_0 to R_{62} connected in series and first to 62nd reference voltages V1 to V62 are outputted from first to 62nd division nodes ND_1 to ND_{62} which are formed by dividing the ladder resistor circuit by the resistor elements R_0 to R_{62}. Further, resistance values of the resistor elements R_0 to R_{62} can realize resistance ratios determined in accordance with a gray scale characteristic shown in, for example, Fig. 5.

[0059] A first switching circuit (SW1) 104 is inserted between one end of the resistor element R_0 constituting the ladder resistor circuit 102 and the first power source line. A second switching circuit (SW2) 106 is inserted between one end of the resistor element R_{62} constituting the ladder resistor circuit 102 and the second power source line. The first and second switching circuits 104 and 106 are controlled by a switching control signal cnt. In this case, when a logical level of the switching control signal cnt is "L", the first and second switching circuits

104 and 106 are switched off to thereby electrically disconnect the both ends and when the logical level of the switching control signal cnt is "H", the first and second switching circuits 104 and 106 are switched on to thereby electrically connect the both ends.

[0060] The switching control signal cnt is generated based on the output enable signal XOE, the latch pulse signal LP and the partial block selection data BLK0_PART to BLKj_PART of each of the blocks.

[0061] When the output enable signal XOE is at logical level of "H", the voltage follower circuit 56 controlled by the output control circuit 54 brings output to signal electrodes into a high impedance state. When the output enable signal XOE is at logical level of "L", the voltage follower circuit 56 controlled by the output control circuit 54 outputs a given drive voltage to signal electrode. Therefore, when the output enable signal XOE is at logical level of "H", the signal electrode is not driven by using first to 62nd reference voltages V1 to V62. Therefore, by cutting current flowing to the crystal circuit 102 during the time period, gray scale display corrected by the gamma correction can be carried out and current flowing to the ladder resistor circuit can be minimized.

[0062] The latch pulse signal LP is a signal specifying, for example, one horizontal scan period timing and is a signal by which the logical level becomes "H" after a given horizontal scan time period. The signal driver IC 30 drives signal electrode with a rise edge of the latch pulse signal LP as a reference. Therefore, the signal electrode is not driven by using first to 62nd reference voltages V1 to V62 when the logical level of the latch pulse signal LP is "H". Therefore, by cutting current flowing to the ladder resistor circuit 102 during the time period, gray scale display corrected by gamma correction can be carried out and current flowing to the ladder resistor circuit can be minimized.

[0063] Partial block selection data BLK0_PART to BLKj_PART are data for setting display lines in correspondence with signal electrodes of the block to a display state or a non-display state by a unit of block constituting the unit by a given number of signal electrodes. That is, a display line in correspondence with a signal electrode of a block set to a non-display state becomes a partial non-display area and the signal electrode is not driven by using first to 62nd reference voltages V1 to V62. Therefore, when display lines in correspondence with signal electrodes of all the blocks are set to the non-display state by partial block selection data BLK0_PART to BLKj_PART (when BLK0_PART to BLKj_PART are all "0" (logical level "L")), by cutting current flowing to the ladder resistor circuit 102, gray scale display corrected by gamma correction can be carried out and current flowing to the ladder resistor circuit can be minimized.

[0064] Fig. 8 shows an example of a control timing of the reference voltage generation circuit 100 according to the first constitution example.

[0065] An example of a control timing in correspondence with a period for inverting a polarity of applied voltage of a liquid crystal (in a broad sense, display element) specified by a polarity inverting signal POL is shown here.

[0066] As described above, the switching control signal cnt can be generated by using the output enable signal XOE, the latch pulse signal LP and the partial block selection data BLK0_PART to BLKj_PART. Based on the switching control signal cnt, on/off state of the first and second switching circuits 104 and 106 can be controlled. When a consideration is given to a case in which the signal driver IC 30 drives a signal electrode with a fall edge of the latch pulse signal LP as a reference, only during a time period in which the logical level of the switching control signal cnt is at "H", current flows to the ladder resistor circuit 102 and consumption of current can be minimized.

3.2 Second constitution example

[0067] Fig. 9 shows an outline of a constitution of a reference voltage generation circuit according to a second constitution example.

[0068] Note that the same notations are attached to portions the same as those of the reference voltage generation circuit 100 according to the first constitution example and a description thereof will pertinently be omitted.

[0069] A point at which the reference voltage generation circuit 120 according to the second constitution example differs from the reference voltage generation circuit 100 according to the first constitution example, resides in that first to i-th reference voltage output switches VSW1 to VSWi are inserted between first to i-th division nodes ND_1 to ND_i and first to i-th reference voltage output nodes VND_1 to VND_i for outputting first to i-th reference voltages V1 to Vi. On/off state of the first to i-th reference voltage output switches VSW1 to VSWi are controlled by the switching control signal cnt for controlling on/off state of the first and second switching circuits 104 and 106 (in a broad sense, first or second switching control signal).

[0070] In Fig. 9, reference voltages V0 to V63 necessary for displaying 64 gray scales are supplied to DAC. Among them, reference voltages V1 to V62 are outputted from the ladder resistor circuit of the reference voltage generation circuit. That is, the point at which the reference voltage generation circuit 120 according to the second constitution example differs from the reference voltage generation circuit 100 according to the first constitution example, resides in that first to 62nd reference voltage output switches VSW1 to VSW62 are inserted between first to 62nd division nodes ND_1 to ND_{62} and first to 62nd reference voltage output nodes VND_1 to VND_{62} for outputting first to 62nd reference voltages V1 to V62. On/off state of the first to 62nd reference voltage output switches VSW1 to VSW62 are controlled by the switch controlling signal cnt for controlling on/off state of the first and second switching circuits 104 and

106.

[0071] In the first constitution example shown by, for example, Fig. 7, consider a case in which the first and second switching circuits 104 and 106 are switched off in a state in which voltages of first to 62nd division nodes ND_1 to ND_{62} become inherent reference voltages V1 to V62. At this occasion, voltages of first to 62nd reference voltage output nodes V1 to V62, are changed by flowing current via resistor elements R_0 to R_{62} constituting the ladder resistor circuit 102. Therefore, when the first and second switching circuits 104 and 106 are switched on, it is necessary to charge electricity until desired reference voltages are reached again.

[0072] Hence, as shown by Fig. 9, by providing first to 62nd reference voltage output switches VSW1 to VSW62, in a state in which the first and second switching circuits 104 and 106 are switched off, first to 62nd reference voltage output nodes VND_1 to VND_{62} can electrically be separated from first to 62nd division nodes ND_1 to ND_{62} and the above-described phenomenon can be avoided. Therefore, there may be constructed a constitution in which on/off state of the first to 62nd reference voltage output switches VSW1 to VSW62 are controlled similar to the first and second switching circuits 104 and 106.

3.3 Third constitution example

[0073] The signal driver IC 30 to which the reference voltage generation circuit is applied, drives signal electrodes of the display panel 20 based on gray scale data. The liquid crystal element is provided at the pixel region provided in correspondence with the intersection of the signal electrode and the scan electrode of the display panel 20. With respect to the liquid crystal sealed between the pixel electrode and the opposed electrode of the liquid crystal element, it is necessary to alternately invert a polarity of voltage applied to the liquid crystal at given timings in order to prevent deterioration.

[0074] Therefore, also with regard to the reference voltage generation circuit for generating the reference voltage in correspondence with the gray scale characteristic, it is necessary to switch voltage outputted to the signal electrode based on the same gray scale data at every time of inverting the polarity. Therefore, the first and second power source voltages of the reference voltage generation circuit are alternately switched. However, since it is necessary to drive the respective division nodes, which are formed by dividing the ladder resistor circuit by the resistor circuits, at a given reference voltage every time the polarity is inverted, charge and discharge are carried out frequently and there poses a problem that consumption of current is increased.

[0075] Hence, a reference voltage generation circuit 200 of the signal driver IC 30 includes a ladder resistor circuit for a positive polarity and a ladder resistor circuit for a negative polarity.

[0076] Fig. 10 shows an outline of a constitution of the reference voltage generation circuit 200 according to the third constitution example.

[0077] The reference voltage generation circuit 200 according to the third constitution example includes a positive polarity ladder resistor circuit 210 and a negative polarity ladder resistor circuit 220. The positive polarity ladder resistor circuit 210 generates reference voltages V1 to Vi used at a positive polarity inversion period when a logical level of polarity inversion signal POL is "H". The negative ladder resistor circuit 220 generates reference voltage V1 to Vi used in a negative polarity inversion period when the logical level of the polarity inversion signal POL is "L". By providing the two ladder resistor circuits and switching to output the reference voltages in the respective polarities in accordance with a given polarity inversion timing, optimum reference voltage in correspondence with the gray scale characteristic which is not generally a symmetric characteristic can be generated and it is not necessary to switch the power source voltages on the high potential side and the low potential side.

[0078] Further specifically, the positive polarity ladder resistor circuit 210 and the negative polarity ladder resistor circuit 220 are respectively constructed by a constitution substantially similar to that of the reference voltage generation circuit 120 according to the second constitution example shown in Fig. 9. However, on/off state of the respective switching circuits are controlled to by using the polarity inversion signal POL. Further, regardless of the polarity of the voltage applied to the liquid crystal, the power source voltages on the high potential side and the low potential side (first and second power source voltages) are fixed.

[0079] The positive polarity ladder resistor circuit 210 includes a first ladder resistor circuit 212 having resistor circuits connected in series by resistor ratios for the positive polarity. One end of the first ladder resistor circuit 212 is connected to the first power source line supplied with the first power source voltage via a first switching circuit (SW1) 214. Other end of the first ladder resistor circuit 212 is connected to the second power source line supplied with the second power source voltage via a second switching circuit (SW2) 216.

[0080] The first to i-th reference voltage output switching circuits VSW1 to VSWi are inserted between first to i-th division nodes ND_1 to ND_i which are formed by dividing the ladder resistor circuit by the resistor circuits R_0 to R_i constituting the first ladder resistor circuit 212 and first to i-th reference voltage output nodes VND_1 to VND_i.

[0081] On/off state of the first and second switching circuits SW1 and SW2 and first to i-th reference voltage output switching circuits VSW1 to VSWi are controlled by a switching control signal cnt11 (in a broad sense, first switching control signal). The switching control signal cnt11 is generated by calculating a logical product of the switching control signal cnt generated as shown by Fig. 9 and the polarity inversion signal POL. That is,

on/off state of the first and second switching circuits SW1 and SW2 and first to i-th reference voltage output switching circuits VSW1 to VSWi are controlled in accordance with the switching control signal cnt when a logical level of the polarity inversion signal POL is "H".

[0082] The negative ladder resistor circuit 220 includes a second ladder resistor circuit 222 having resistor circuits connected in series by resistance ratios for the negative polarity. One end of the second ladder resistor circuit 222 is connected to the first power source line via a third switching circuit (SW3) 224. Other end of the second ladder resistor circuit 222 is connected to the second power source line via a fourth switching circuit (SW4) 226.

[0083] The (i + 1)th to 2i-th reference voltage output switching circuits VSW(i + 1) to VSW2i are inserted between (i + 1)th to 2i-th division nodes ND_{i+1} to ND_{2i} which are formed by dividing the ladder resistor circuit by the resistor circuits R_0' and R_{i+1} to R_{2i} constituting the second ladder resistor circuit 222 and first to i-th reference voltage output nodes VND_1 to VND_i.

[0084] On/off state of the third and the fourth switching circuits SW3 and SW4 and (i + 1)th to 2i-th reference voltage output switching circuits VSW(i + 1) to VSW2i are controlled by a switching control signal cnt12 (in a broad sense, second switching control signal). The switching control signal cnt 12 is generated by calculating a logical product of the switching control signal cnt generated as shown by Fig. 9 and an inverted signal of the polarity inversion signal POL. That is, on/off state of the third and the fourth switching circuit SW3 and SW4 and (i + 1)th to 2i-th reference voltage output switching circuits VSW(i + 1) to VSW2i are controlled in accordance with the switching control signal cnt when the logical level of the polarity inversion signal POL is "L".

[0085] First to i-th reference voltages V1 to Vi generated by the two ladder resistor circuits and the reference voltages V0 and VY are outputted to DAC as the voltage selection circuit.

[0086] Next, a description will be given of a constitution of a circuit for driving signal electrodes by using multi-valued reference voltages generated by the reference voltage generation circuit.

[0087] Fig. 11 shows a specific constitution example of DAC 52 and the voltage follower circuit 56.

[0088] Only a constitution for one output is shown here.

[0089] DAC 52 can be realized by an ROM decoder circuit. DAC 52 selects any one of the reference voltages V0 and VY and first to i-th reference voltages V1 to Vi based on gray scale data of (q + 1) bits and outputs a selected one as selected voltage Vs to the voltage follower circuit 56.

[0090] The voltage follower circuit 56 drives a corresponding signal electrode in accordance with a mode set to either of a normal drive mode and a partial drive mode.

[0091] First, DAC 52 will be described. DAC 52 is inputted with gray scale data D_q to D_0 of (q + 1) bits and inverted gray scale data XD_q to XD_0 of (q + 1) bits. The inverted gray scale data XD_q to XD_0 are produced respectively by inverting bits of the gray scale data D_q to D_0. In this case, the gray scale data D_q and the inverted gray scale data XD_q are the most significant bits of the gray scale data and inverted gray scale data, respectively.

[0092] In DAC 52, any one of multi-valued reference voltage V0 to Vi and VY generated by the reference voltage generation circuit is selected based on the gray scale data.

[0093] For example, assume that the reference voltage generation circuit 200 shown in Fig. 10 generates reference voltages V0 to V63. Further, the reference voltages generated by using the positive polarity ladder resistor circuit 210 are designated by notations V0' to V63'. Further specifically, the first and second power source voltages are set to V0' and V63' and voltages of first to i-th division nodes ND_1 to ND_i are set to V1' to V62'.

[0094] Further, reference voltages generated by the negative polarity ladder resistor circuit 220 are designated by notations V63" to V0". Further specifically, the first and second power source voltages are set to V63" and V0" and the voltages of (i + 1)th to 2i-th division nodes ND_{i+1} to ND_{2i} are set to V62" to V1".

[0095] That is, the following relationships are established.

$$V0' = V63'' = V0 \quad (1)$$

$$V1' = V62'' = V1 \quad (2)$$

$$V2' = V61'' = V2 \quad (3)$$

$$V61' = V2'' = V61 \quad (62)$$

$$V62' = V1'' = V62 \quad (63)$$

$$V63' = V0'' = V63 \quad (64)$$

[0096] Assume that when the logical level of the polarity inversion signal POL is "H", the reference voltage V2' (= V2) generated by the positive polarity ladder resistor circuit 210 is selected in correspondence with 6(q = 5) bits of gray scale data D_5 to D_0 "000010" (= 2). In this case, when the logical level of the polarity inversion signal POL becomes "L" at successive polarity inversion timing, the reference voltage is selected by using inverted gray scale data XD_5 to XD_0 produced by inverting gray scale data D_5 to D_0. That is, inverted gray scale

data XD_5 to XD_0 becomes "111101" (= 61) and reference voltage V61" generated by the negative ladder resistor circuit 220 can be selected. Therefore, in the positive polarity and the negative polarity, as shown by Equation (3), in both of the cases, the second reference voltage V2 is outputted and therefore, it is not necessary to frequently repeat to charge and discharge the reference voltage output node.

[0097] The selected voltage Vs selected by DAC 52 in this way is inputted to the voltage follower circuit 56.

[0098] The voltage follower circuit 56 includes switching circuits SWA to SWD and an operational amplifier OPAMP. An output of the operational amplifier OPAMP is connected to signal electrode output node via the switching circuit SWD. The signal electrode output node is connected to an inverted input terminal of the operational amplifier OPAMP. The signal electrode output node is connected to a noninverted input terminal of the operational amplifier OPAMP via the switching circuit SWC. Further, the signal electrode output node is connected with an output of an inverter circuit for inverting the polarity inverting signal POL via the switching circuit SWB. Further, the signal electrode output node is connected with a signal line of the most significant bit of gray scale data selected in accordance with a polarity of a drive period specified by the polarity inverting signal POL via the switching circuit SWA.

[0099] On/off state of the switching circuit SWA is controlled by a switching control signal ca. On/off state of the switching circuit SWB is controlled by a switching control signal cb. On/off state of the switching circuit SWC is controlled to by a switching control signal cc. On/off state of the switching circuit SWD is controlled by a switching control signal cd.

[0100] The voltage follower circuit 56 drives the signal electrode by using the operational amplifier OPAMP based on the selected voltage Vs in the normal drive mode. Further, the voltage follower circuit 56 drives the signal electrode by using the polarity inverting signal POL or displays 8 colors by using the most significant bit of the gray scale data.

[0101] Fig. 12A shows switching states in the switching circuits SWA to SWD in the above-described modes. Fig. 12B shows an example of a circuit of generating the switching control signals ca to cb.

[0102] In the normal drive mode, the signal electrode output node is driven by the operational amplifier OPAMP during an operational amplifier drive period and during a resistor output drive period, the selected voltage Vs outputted from DAC 52 is outputted as it is by bypassing the operational amplifier OPAMP. Therefore, while switching the switching circuits SWA and SWB off, during the operational amplifier drive period, the switching circuit SWD is switched on and the switching circuit SWC is switched off and during the resistor output period, the switching circuit SWD is switched off and the switching circuit SWC is switched on.

[0103] Fig. 13 shows an example of an operational timing of the normal drive mode in the voltage follower circuit 56.

[0104] The switching circuits SWC and SWD are controlled by a control signal DrvCnt. According to the control signal DrvCnt generated by a control signal generating circuit, not illustrated, a logical level thereof is changed by a former half period (initial given period of drive period) t1 and a latter half period t2 of a selection period (drive period) t specified by the latch pulse signal LP. When the logical level of the control signal DrvCnt becomes "L" in the former half period t1, the switching circuit SWD is switched on and the switching circuit SWC is switched off. Further, when the logical level of the control signal DrvCnt becomes "H" in the later half period t2, the switching circuit SWD is switched off and the switching circuit SWC is switched on. Therefore, in the selection period t, at the former half period t1, the signal electrode is driven by converting impedance by the operational amplifier OPAMP connected by voltage follower connection and at the latter half period t2, the signal electrode is driven by using the selected voltage Vs outputted from DAC 52.

[0105] By driving the signal electrode in this way, at the former half period t1 necessary for charging liquid crystal capacitance, wiring capacitance and the like, the drive voltage Vout is elevated at high speed by the operational amplifier OPAMP connected by voltage follower connection having high drive capability and at the latter half period t2 in which high drive capability is not needed, the drive voltage can be outputted by DAC 52. Therefore, low power consumption can be achieved by minimizing a period of operating the operational amplifier OPAMP having significant consumption of current and a situation in which the selection period t is shortened and a charging period becomes deficient by an increase in a number of lines can be avoided.

[0106] In the partial mode shown in Fig. 12A, at a partial non-display area, 8 color display or POL drive is carried out. In 8 color display, by only using the most significant bit of the gray scale data, the corresponding signal electrode is driven. Therefore, while switching the switching circuits SWC and SWD off, the switching circuit SWA is switched on and the switching circuit SWB is switched off.

[0107] Therefore, when one pixel is assumed to comprise R, G and B signals, one pixel displays gray scale levels of 2^3. That is, there can be carried out image display in which while in a partial display area, a desired moving image or still image is displayed, there are constituted a variety of display colors of a partial non-display area which is set as a background thereof.

[0108] Furthermore, in POL drive of the partial drive mode shown in Fig. 12A, by applying voltage in correspondence with the polarity by using the polarity inverting signal POL, black display or white display can be carried out. For that purpose, while switching the switching circuits SWC and SWD off, the switching circuit SWB is switched on and the switching circuit SWA is switched

off.

[0109] In that case, while a desired moving image or a still image is displayed in the partial display area, black display or white display is carried out for the background color to thereby realize display of an image which is easy to see. At the same time, a DC component is not applied to liquid crystals at the non-display portion and deterioration of liquid crystals can be prevented.

[0110] Various control signals for controlling the voltage follower circuit 56 can be generated by a circuit shown by Fig. 12B. When a logical level of a 8 color display mode signal 8CMOD is "H", it shows that the mode is 8 color display of the partial drive mode. Whether 8 color display is carried out is set by, for example, a host, not illustrated. When a logical level of a POL drive mode signal POLMOD is "H", it shows that the mode is POL drive of the partial drive mode. Whether POL drive is carried out is set by, for example, a host, not illustrated.

[0111] In this way, the switching control signals ca to cd can be generated by using the various signals of 8CMOD, POLMOD and DrvCnt. Further, the switching control signals are masked by a partial block selection data BLKz_PART in correspondence with a block Bz such that 8 color display or POL drive is carried out only when a display line in correspondence with a signal electrode driven by the voltage follower circuit 56 belongs to the.block set to a non-display state and normal drive is carried out when the display line belongs to the block set to a display state.

[0112] Further, according to the voltage follower circuit 56, the output can be brought into a high impedance state by the output enable signal XOE. Therefore, the various control signals are masked by the output enable signal XOE. That is, when the logical level of the output enable signal XOE is "H", the switching control signals ca to cd control the off state of the switching circuits of respective control objects.

[0113] Further, although according to the third constitution example, the first to fourth switching circuits are provided between the first and second ladder resistor circuits 212 and 222 and the first and second power source lines, there can be constructed a constitution of omitting these. In this case, it is not necessary to alternately switch the first and second power source voltages by driving to invert the polarity and therefore, it is not necessary to ensure a charge time period of each of the division nodes and current can be reduced by increasing a resistance value of the ladder resistor circuit.

3.4 Fourth constitution example

[0114] A reference voltage generation circuit according to a fourth constitution example includes ladder resistor circuits respectively for a positive polarity and a negative polarity and having high resistance and low resistance as total resistance thereof.

[0115] Fig. 14 shows an outline of a constitution of a reference voltage generation circuit 300 according to the fourth constitution example.

[0116] That is, the reference voltage generation circuit 300 includes a low resistance ladder resistor circuit for a positive polarity (in a broad sense, first low resistance ladder resistor circuit) 310 used when total resistance is, for example, 20kΩ and voltage applied to a liquid crystal is of a positive polarity and a low resistance ladder resistor circuit for a negative polarity (in a broad sense, second low resistance ladder resistor circuit) 320 used when total resistance is, for example, 20kΩ similarly and voltage applied to a liquid crystal is of a negative polarity. Further, the reference voltage generation circuit 300 includes a high resistance ladder resistor circuit for a positive polarity (in a broad sense, first high resistance ladder resistor circuit) 330 used when total resistance is, for example, 90kΩ and voltage applied to a liquid crystal is of a positive polarity and a high resistance ladder resistor circuit for a negative polarity (in a broad sense, second high resistance ladder resistor circuit) 340 used when total resistance is, for example, 90kΩ similarly and voltage applied to a liquid crystal is of a negative polarity.

[0117] The positive polarity low resistance ladder resistor circuit 310 and the positive polarity high resistance ladder resistor circuit 330 are constructed by a constitution similar to that of the positive polarity ladder resistor circuit 210 shown in Fig. 10. The negative polarity low resistance ladder resistor circuit 320 and the negative polarity high resistance ladder resistor circuit 340 are constructed by a constitution similar to that of the negative polarity ladder resistor circuit 220 shown in Fig. 10. However, on/off state of each of the switching circuits are controlled by using the switching control signals cnt11 and cnt12 and timer count signals (in a broad sense, control period designating signals) TL1 and TL2. Further, regardless of a polarity of voltage applied to a liquid crystal, power source voltages on a high potential side and a low potential side (first and second power source voltages) are fixed.

[0118] The positive polarity low resistance ladder resistor circuit 310 includes a first ladder resistor circuit 312 having resistor circuits with total resistance of, for example, 20kΩ and connected in series by resistance ratios for a positive polarity. One end of the first ladder resistor circuit 312 is connected to the first power source line supplied with the first power source voltage via a first switching circuit (SW1) 314. Other end of the first ladder resistor circuit 322 is connected to the second power source line supplied with the second power source voltage via a second switching circuit (SW2) 316.

[0119] The first to i-th reference voltage output switching circuits VSW1 to VSWi are inserted between first to i-th division nodes ND_1 to ND_i which are formed by dividing the ladder resistor circuit by the resistor circuits R_0 to R_i constituting the first ladder resistor circuit 312 and first to i-th reference voltage output nodes VND_1 to VND_i.

[0120] On/off state of the first and second switching

circuits SW1 and SW2 and first to i-th reference voltage output switching circuits VSW1 to VSWi are controlled by a switching control signal cntPL (in a broad sense, first switching control signal). The switching control signal cntPL is generated by using the switching control signal cnt11 generated as shown in Fig. 10 and the timer count signals TL1 and TL2. That is, when a logical level of the timer count signal TL1 is "H" and a logical level of the timer count signal TL2 is "L", on/off state of the circuits are controlled in accordance with the switching control signal cnt11.

[0121] The negative polarity low resistance ladder resistor circuit 320 includes a second ladder resistor circuit 322 having resistor circuits with total resistance of, for example, 20kΩ and connected in series by resistance ratios for a negative polarity. One end of the second ladder resistor circuit 322 is connected to the first power source line supplied with the first power source voltage via a third switching circuit (SW3) 324. Other end of the second ladder resistor circuit 322 is connected to the second power source line supplied with the second power source voltage via a fourth switching circuit (SW4) 326.

[0122] The (i + 1)th to 2i-th reference voltage output switching circuits VSW(i + 1) to VSW2i are inserted between (i + 1)th to 2i-th division nodes ND_{i+1} to ND_{2i} which are formed by dividing the ladder resistor circuit by the resistor circuits R_0' and R_{i+1} to R_{2i} constituting the second ladder resistor circuit 322 and first to i-th reference voltage output nodes VND_1 to VND_i.

[0123] On/off state of the third and the fourth switching circuits SW3 and SW4 and (i + 1)th to 2i-th reference voltage output switching circuits VSW(i + 1) to VSW2i are controlled by a switching control signal cntML (in a broad sense, second switching control signal). The switching control signal cntML is generated by using the switching control signal cnt12 generated as shown in Fig. 10 and the timer count signals TL1 and TL2. That is, when the logical level of the timer count signal TL1 is "H" and the logical level of the timer count signal TL2 is "L", on/off states of the circuit are controlled in accordance with the switching control signal cnt11.

[0124] The positive polarity high resistance ladder resistor circuit 330 includes a third ladder resistor circuit 332 having resistor circuits with total resistance of, for example, 90kΩ and connected in series by resistance ratios for a positive polarity. One end of the third ladder resistor circuit 332 is connected to the first power source line supplied with the first power source voltage via a fifth switching circuit (SW5) 334. Other end of the third ladder resistor circuit 332 is connected to the second power source line supplied with the second power source voltage via a sixth switching circuit (SW6) 336.

[0125] The (2i + 1)th to 3i-th reference voltage output switching circuits VSW(2i + 1) to VSW3i are inserted between (2i + 1)th to 3i-th division nodes ND_{2i+1} to ND_{3i} which are formed by dividing the ladder resistor circuit by the resistor circuits R_0" and R_{2i+1} to R_{3i} constituting the third ladder resistor circuit 332 and first to i-th reference voltage output nodes VND_1 to VND_i.

[0126] On/off state of the fifth and the sixth switching circuits SW5 and SW6 and (2i + 1)th to 3i-th reference voltage output switching circuits VSW(2i + 1) to VSW3i are controlled by a switching control signal cntPH (in a broad sense, third switching control signal). The switching control signal cntPH is generated by using the switching control signal cnt11 generated as shown in Fig. 10 and the timer count signals TL1 and TL2. That is, when the logical level of the timer count signal TL1 is "L" and the logical level of the timer count signal TL2 is "H", on/off states of the circuits are controlled in accordance with the switching control signal cnt11.

[0127] The negative polarity high resistance ladder resistor circuit 340 includes a fourth ladder resistor circuit 342 having resistor circuits with total resistance of, for example, 90kΩ and connected in series by resistance ratios for a negative polarity. One end of the fourth ladder resistor circuit 342 is connected to the first power source line supplied with the first power source voltage via a seventh switching circuit (SW7) 344. Other end of the fourth ladder resistor circuit 342 is connected to the second power source line supplied with the second power source voltage via an eighth switching circuit (SW8) 346.

[0128] The (3i + 1)th to 4i-th reference voltage output switching circuits VSW(3i + 1) to VSW4i are inserted between (3i + 1)th to 4i-th division nodes ND_{3i+1} to ND_{4i} which are formed by dividing the ladder resistor circuit by the resistor circuits R0'" and R_{3i+1} to R_{4i} constituting the fourth ladder resistor circuit 342 and first to i-th reference voltage output nodes VND_1 to VND_i.

[0129] On/off state of the seventh and the eighth switching circuits SW7 and SW8 and (3i + 1)th to 4i-th reference voltage output switching circuits VSW(3i + 1) to VSW4i are controlled by a switching control signal cntPH (in a broad sense, fourth switching control signal). The switching control signal cntPH is generated by using the switching control signal cnt12 generated as shown in Fig. 10 and the timer count signals TL1 and TL2. That is, when the logical level of the timer count signal TL1 is "L" and the logical level of the timer count signal TL2 is "H", on/off states of the circuits are controlled in accordance with the switching control signal cnt12.

[0130] Fig. 15 shows an example of a control timing of the reference voltage generation circuit 300 shown in Fig. 14.

[0131] Shown here is a control timing when polarity inversion drive is carried out by a positive polarity with respect to the first reference voltage V1.

[0132] The signal driver IC including the reference voltage generation circuit 300 starts driving with a fall edge of the latch pulse signal LP specifying a horizontal scan period timing as a reference. Further, in the drive period, according to the reference voltage generation circuit 300, the positive high resistance ladder resistor

circuit 330 and the negative polarity high resistance ladder resistor 340 are used. Further, at an initial control period of the drive period, at the same time, the positive polarity low resistance ladder resistor circuit 310 and the negative polarity low resistance ladder resistor circuit 320 are also used. That is, in the control period, the positive polarity high resistance ladder resistor circuit 330, the negative polarity high resistance ladder resistor circuit 340, the positive polarity low resistance ladder resistor circuit 310 and the negative polarity low resistance ladder resistor circuit 320 are used.

[0133] In this way, current flows to the ladder resistor circuit having low resistance in the control period and therefore, it is not necessary to control the high resistance ladder resistor circuit.

[0134] Further, the control period is specified by the control signal DrvCnt as shown by Fig. 15. That is, after driving the operational amplifier by the voltage follower circuit 56 as shown by Fig. 13, resistor output drive is carried out.

[0135] In this way, according to the fourth constitution example, after driving the operational amplifier by using the low resistance ladder resistor circuit, resistor output drive is carried out and thereafter, the reference voltage V1 is generated by the high resistance ladder resistor circuit. Thereby, although there is a case in which a charge time period sufficient for elevating the division node to the first reference voltage V1 cannot be ensured when resistor output drive is carried out by the high resistance ladder resistor circuit after driving the operational amplifier, the charge time period can be ensured by carrying out resistor output drive by the low resistance ladder resistor circuit after driving the operational amplifier. Further, by generating the reference voltage by using the high resistance ladder resistor circuit thereafter, current flowing to the ladder resistor circuit can be reduced and low power consumption can be achieved.

[0136] Further, although according to the third constitution example, the first to eighth switching circuits SW1 to SW8 are provided between the first to fourth ladder resistor circuits 312, 322, 332 and 342 and the first and second power source lines, there can be constructed a constitution of omitting these. In this case, it is not necessary to alternately switch the first and second power source voltages by polarity inversion drive and therefore, it is not necessary to ensure the charge time period of each of the division nodes and the resistance value of the ladder resistor circuit can be increased and the current can be reduced.

4. Others

[0137] Although in the above-described, a description has been given by taking an example of the liquid crystal device having the liquid crystal panel using TFT, the invention is not limited thereto. The reference voltage generated by the reference voltage generation circuit 50 may be converted to current by a given current conversion circuit to supply to an element of a current drive type. Thereby, the invention is applicable to, for example, a signal driver IC for driving to display an organic EL panel including an organic EL element provided in correspondence with a pixel specified by a signal electrode and a scan electrode. Particularly, when polarity inversion drive is not carried out in an organic EL panel, the difference voltage generation circuits according to the first and second constitution examples can be used.

[0138] Fig. 16 shows an example of a pixel circuit of a two transistor system in an organic EL panel driven by such a signal driver IC.

[0139] The organic EL panel includes a drive TFT 800_{nm}, a switching TFT 810_{nm}, a hold capacitor TFT 820_{nm} and an organic LED 830_{nm} at an intersection of a signal electrode S_m and a scan electrode G_n. The drive TFT 800_{nm} is constituted by a p-type transistor.

[0140] The drive TFT 800_{nm} and the organic LED 830_{nm} are connected in series with a power source line.

[0141] The switching TFT 810_{nm} is inserted between a gate electrode of the drive LED 800_{nm} and the signal electrode S_m. The gate electrode of the switching TFT 810_{nm} is connected to the scan electrode G_n.

[0142] The hold capacitor 820_{nm}, is inserted between the gate electrode of the drive TFT 800_{nm}, and a capacitor line.

[0143] In the organic EL element, when the scan electrode G_n is driven and the switching TFT 810_{nm} is switched on, voltage of the signal electrode S_m is written to the hold capacitor 820_{nm} and applied to the gate electrode of the drive TFT 800_{nm}. Gate voltage Vgs is determined by voltage of the signal electrode S_m and current flowing to the drive TFT 800_{nm} is determined. Since the drive TFT 800_{nm} and the organic LED 830_{nm} are connected in series, current flowing to the drive TFT 800_{nm} becomes current flowing to the organic LED 830_{nm} as it is.

[0144] Therefore, by holding the gate voltage Vgs in accordance with the voltage of the signal electrode S_m by the hold capacitor 820_{nm}, for example, during one frame period, by flowing current in correspondence with the gate voltage Vgs to the organic LED 830_{nm}, a pixel which continues lighting during the frame can be realized.

[0145] Fig. 17A shows an example of a pixel circuit of a four transistor system in an organic EL panel driven by using a signal driver IC. Fig. 17B shows an example of a display control timing of the pixel circuit.

[0146] Also in this case, the organic EL panel includes a drive TFT 900_{nm}, a switching TFT 910_{nm}, a hold capacitor 920_{nm} and an organic LED 930_{nm}.

[0147] A point which differs from the pixel circuit of the two transistor systems shown in Fig. 16, resides in that in place of constant voltage, constant current Idata from a constant current source 950_{nm} is supplied to the pixel via a p-type TFT 940_{nm} as a switching element and that the hold capacitor 920_{nm} and the drive TFT 900_{nm} are connected to the power source line via a p-type TFT

960_{nm} as a switching element.

[0148] In the organic EL element, first, the p-type TFT 960_{nm} is turned off by gate voltage Vgp to thereby cut the power source line, the p-type TFT 940_{nm} and the switching TFT 910_{nm} are switched on by gate voltage Vsel and the constant current Idata from the constant current source 950_{nm} is made to flow to the drive TFT 900_{nm}.

[0149] During a period until current flowing to the drive TFT 900_{nm} is stabilized, voltage in accordance with the constant current Idata is held at the hold capacitor 920_{nm}.

[0150] Successively, the p-type TFT 940_{nm} and the switching TFT 910_{nm} are turned off by the gate voltage Vsel, further, the p-type TFT 960_{nm} is switched on by the gate voltage Vgp and the power source line, the drive TFT 900_{nm}, and the organic LED 930_{nm} are electrically connected. At this occasion, by voltage held at the hold capacitor 920_{nm}, current having a magnitude substantially equivalent to the constant current Idata or in accordance therewith is supplied to the organic LED 930_{nm}.

[0151] In such an organic EL element, the scan electrode can be constituted as an electrode applied with the gate voltage Vsel and the signal electrode can be constituted as a data line.

[0152] The organic LED may be provided with a light emitting layer above a transparent anode (ITO) and provided with a metal cathode further thereabove, a light emitting layer, a light transmitting cathode and a transparent seal may be provided above a metal anode and the organic LED is not limited to an element structure thereof.

[0153] By constituting the signal driver IC for driving to display the organic EL panel including the organic EL element described above as described above, the signal driver IC generally used in the organic EL panel can be provided.

[0154] Further, the invention is not limited to the above-described embodiments but various modifications can be carried out within a range of the gist of the invention. For example, the invention is applicable also to a plasma display device.

[0155] Further, the invention is not limited to the constitutions of the resistor circuit and the switching circuit in the above-described embodiments. The resistor circuit can be constituted by connecting a single or a plurality of resistor elements in series or in parallel. Or, the resistor value can be constituted to be variable by connecting resistor elements and a single or a plurality of switching circuits in series or in parallel. Further, the switching circuit can be constituted by, for example, MOS transistors.

Claims

1. A reference voltage generation circuit which generates multi-valued reference voltages for generating a gray scale value corrected by gamma correction based on gray scale data for driving a liquid crystal display, the reference voltage generation circuit comprising:

a first positive ladder resistor circuit (310) including a first ladder resistor circuit (312) including a plurality of first resistor circuits (R_0-R_i) connected in series between first and second power source lines supplied with first and second power source voltages (VDD, VSS), respectively, and
a first negative ladder resistor circuit (320) including a second ladder resistor circuit (322) including a plurality of second resistor circuits connected in series between the first and second power source lines,

characterized in that

the first positive ladder resistor circuit (310) further includes:

first to i-th reference voltage output switching circuits (VSW1-VSWi) respectively inserted between first to i-th division nodes (ND_1-ND_i), where i is an integer larger than or equal to 2, and first to i-th reference voltage output nodes (VND_1-VND_i), the first to i-th division nodes being formed by dividing the first ladder resistor circuit (312) by the first resistor circuits;
the first negative ladder resistor circuit (320) further includes:

(i + 1)th to 2i-th reference voltage output switching circuits (VSW(i+1)-VSW2i) respectively inserted between (i + 1)th to 2i-th division nodes (ND_{i+1}-ND_{2i}) and the first to i-th reference voltage output nodes, the (i + 1)th to 2i-th division nodes being formed by dividing the second ladder resistor circuit (322) by the second resistor circuits;

a second positive ladder resistor circuit (330) is provided and includes:

a third ladder resistor circuit (332) having a plurality of third resistor circuits (R_0"-R_{3i}) connected in series between the first and second power source lines and having a resistance higher than that of the first ladder resistor circuit (312), and
(2i + 1)th to 3i-th reference voltage output switching circuits (VSW(2i+1)-VSW(3i)) respectively inserted between (2i + 1)th to 3i-th division nodes (ND_{2i+1}-ND_{3i}) and the first to i-th reference voltage output nodes,

the (2i + 1)th to 3i-th division nodes being formed by dividing the third ladder resistor circuit (332) by the third resistor circuits; and

a second negative ladder resistor circuit (340) is provided and includes:

a fourth ladder resistor circuit (342) having a plurality of fourth resistor circuits (R_0'''-R_{4i}) connected in series between the first and second power source lines and having a resistance higher than that of the second ladder resistor circuit (322), and
(3i + 1)th to 4i-th reference voltage output switching circuits (VSW(3i+1)-VSW(4i)) respectively inserted between (3i + 1)th to 4i-th division nodes (ND_{3i+1}-ND_{4i}) and the first to i-th reference voltage output nodes, the (3i + 1)th to 4i-th division nodes being formed by dividing the fourth ladder resistor circuit (342) by the fourth resistor circuits,

wherein when polarity inversion of a voltage outputted by a polarity inversion drive system to a signal electrode at a given polarity inversion period is repeated:

the first to i-th reference voltage output switching circuits are switched on during a given control period in a positive polarity driving period and switched off during a given control period in a negative polarity driving period,
the (i + 1)th to 2i-th reference voltage output switching circuits are switched off during a given control period in the positive polarity driving period and switched on during a given control period in the negative polarity driving period,
the (2i + 1)th to 3i-th reference voltage output switching circuits are switched on during the positive polarity driving period and switched off during the negative polarity driving period, and
the (3i + 1)th to 4i-th reference voltage output switching circuits are switched on during the positive polarity driving period and switched off during the negative polarity driving period.

2. A display drive circuit comprising:

the reference voltage generation circuit (50) as defined in claim 1;
a voltage selection circuit (52) which selects a voltage based on gray scale data, from the multi-valued reference voltages generated by the reference voltage generation circuit; and
a signal electrode drive circuit (56) which drives a signal electrode by using the voltage selected by the voltage selection circuit.

3. A display device comprising:

a plurality of signal electrodes;
a plurality of scan electrodes intersecting with the signal electrodes;
a pixel specified by one of the signal electrodes and one of the scan electrodes;
the display drive circuit as defined by claim 2 which drives the signal electrodes; and
a scan electrode drive circuit which drives the scan electrodes.

FIG. 1

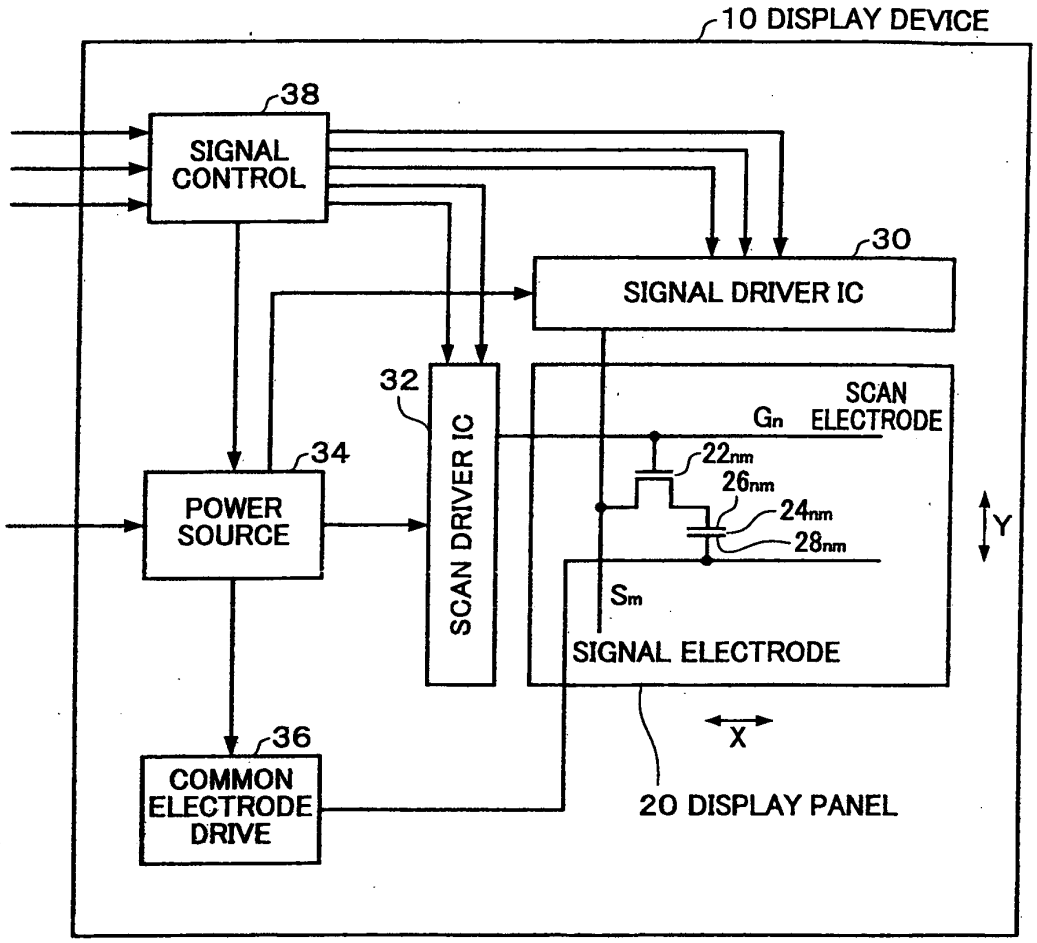

10 DISPLAY DEVICE
38
SIGNAL CONTROL
30
SIGNAL DRIVER IC
32
SCAN DRIVER IC
SCAN ELECTRODE
Gn
22nm
26nm
24nm
28nm
34
POWER SOURCE
Y
Sm
SIGNAL ELECTRODE
X
36
COMMON ELECTRODE DRIVE
20 DISPLAY PANEL

FIG. 2

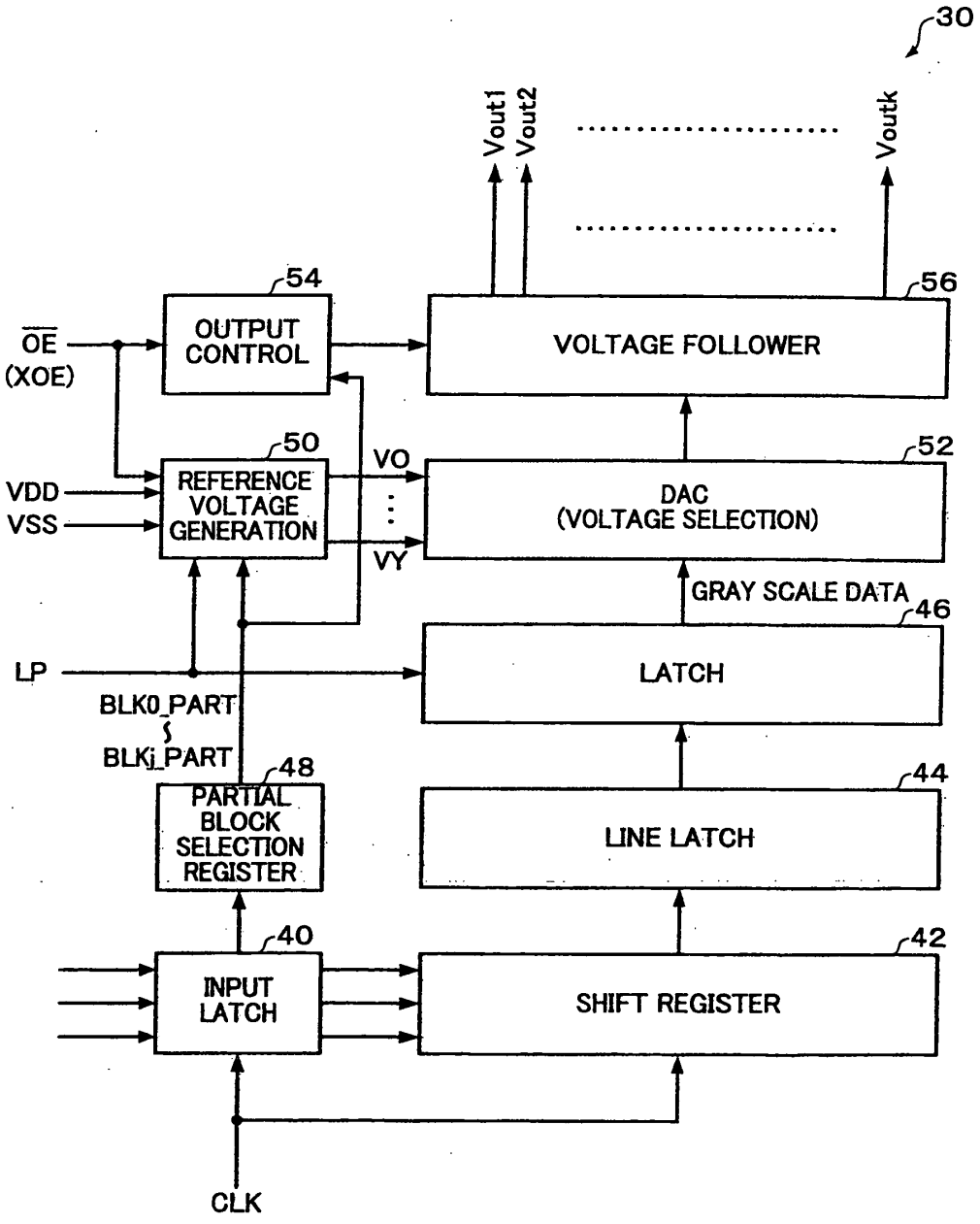

30
Vout1
Vout2
Voutk
54
OUTPUT CONTROL
56
VOLTAGE FOLLOWER
OE
(XOE)
50
REFERENCE VOLTAGE GENERATION
VDD
VSS
VO
VY
52
DAC (VOLTAGE SELECTION)
GRAY SCALE DATA
46
LATCH
LP
BLK0_PART
BLKj_PART
48
PARTIAL BLOCK SELECTION REGISTER
44
LINE LATCH
40
INPUT LATCH
42
SHIFT REGISTER
CLK

FIG. 3A

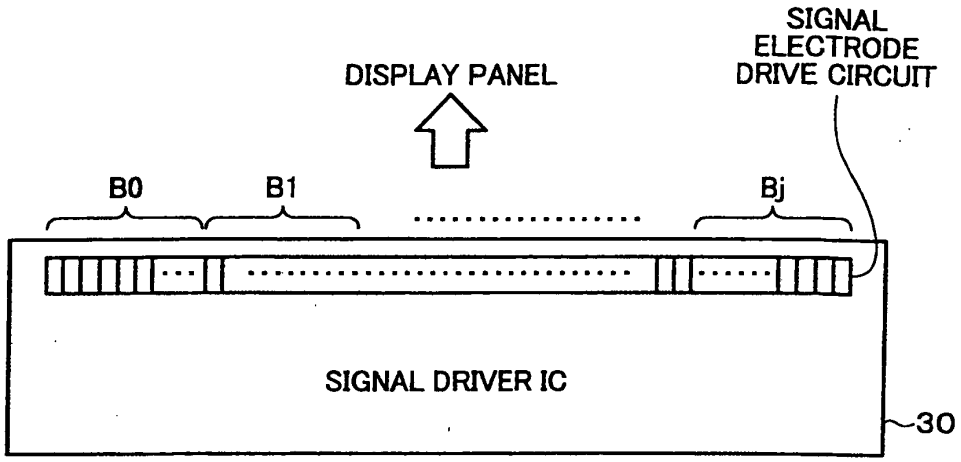

SIGNAL
ELECTRODE
DRIVE CIRCUIT
DISPLAY PANEL
B0
B1
Bj
SIGNAL DRIVER IC
30

FIG. 3B

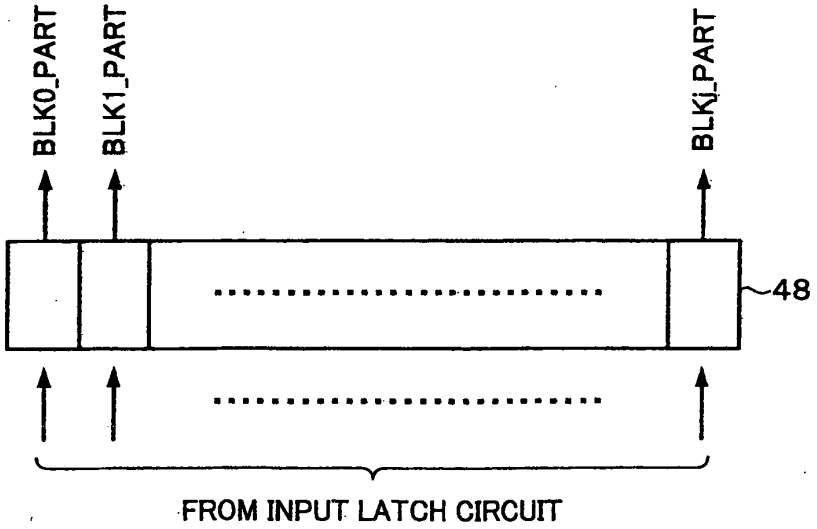

BLK0_PART
BLK1_PART
BLKj_PART
48
FROM INPUT LATCH CIRCUIT

FIG. 4

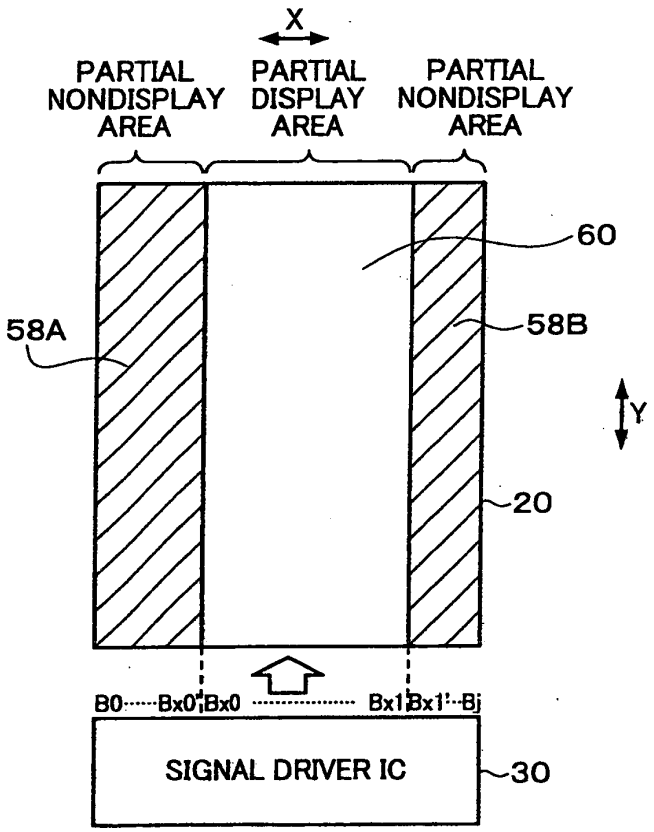

X
PARTIAL NONDISPLAY AREA
PARTIAL DISPLAY AREA
PARTIAL NONDISPLAY AREA
60
58A
58B
Y
20
B0
Bx0'
Bx0
Bx1
Bx1'
Bj
SIGNAL DRIVER IC
30

FIG. 5

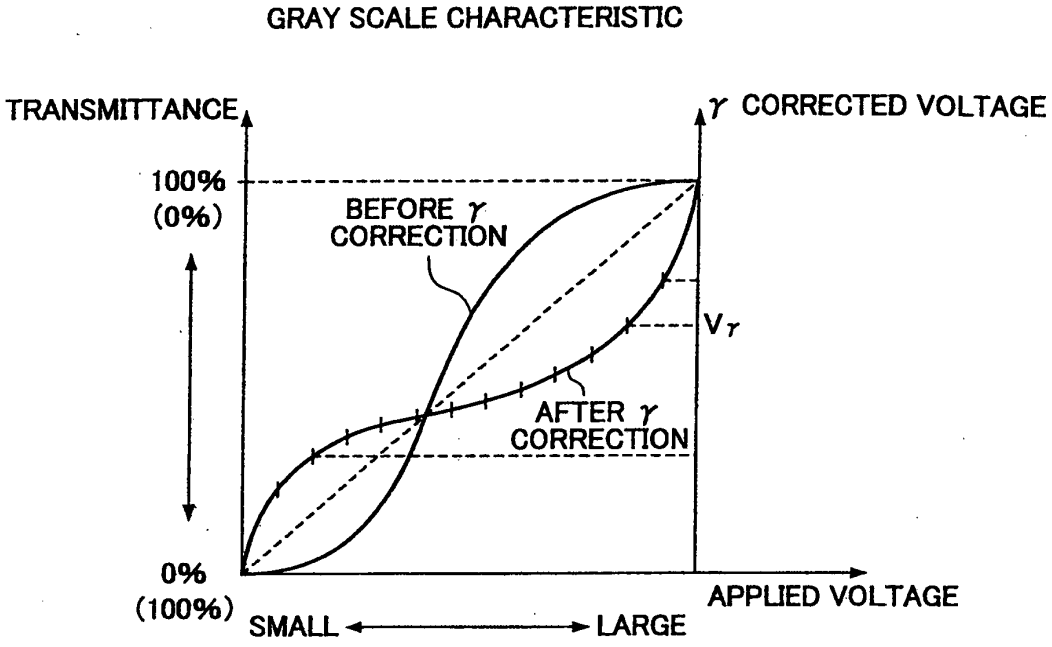

GRAY SCALE CHARACTERISTIC
TRANSMITTANCE
γ CORRECTED VOLTAGE
100%
(0%)
BEFORE γ
CORRECTION
Vγ
AFTER γ
CORRECTION
0%
(100%)
APPLIED VOLTAGE
SMALL
LARGE

FIG. 6

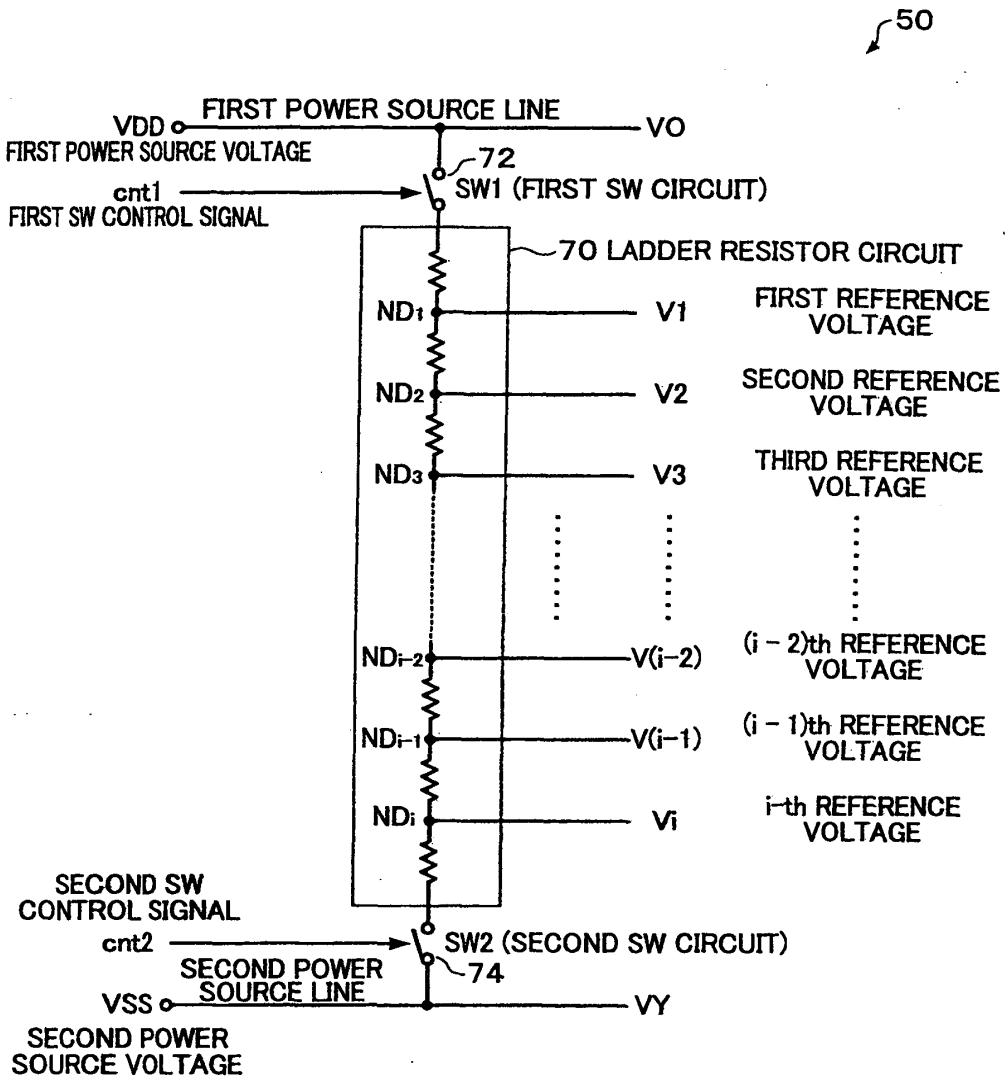

50
FIRST POWER SOURCE LINE
VDD
FIRST POWER SOURCE VOLTAGE
VO
72
cnt1
FIRST SW CONTROL SIGNAL
SW1 (FIRST SW CIRCUIT)
70 LADDER RESISTOR CIRCUIT
ND1
V1
FIRST REFERENCE VOLTAGE
ND2
V2
SECOND REFERENCE VOLTAGE
ND3
V3
THIRD REFERENCE VOLTAGE
NDi-2
V(i-2)
(i - 2)th REFERENCE VOLTAGE
NDi-1
V(i-1)
(i - 1)th REFERENCE VOLTAGE
NDi
Vi
i-th REFERENCE VOLTAGE
SECOND SW CONTROL SIGNAL
cnt2
SW2 (SECOND SW CIRCUIT)
74
SECOND POWER SOURCE LINE
VSS
VY
SECOND POWER SOURCE VOLTAGE

FIG. 7

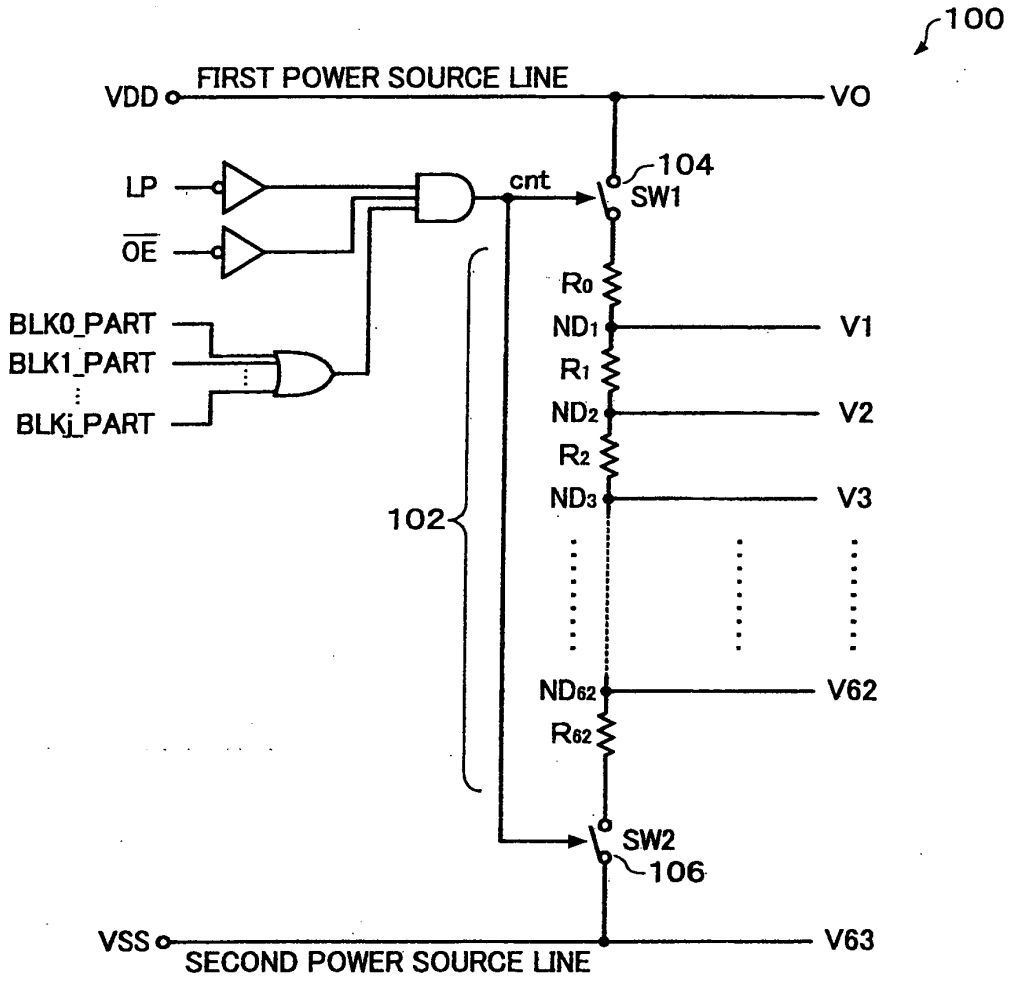

100
VDD
FIRST POWER SOURCE LINE
VO
LP
OE
cnt
104
SW1
BLK0_PART
BLK1_PART
BLKj_PART
R0
ND1
V1
R1
ND2
V2
R2
ND3
V3
102
ND62
V62
R62
SW2
106
VSS
SECOND POWER SOURCE LINE
V63

FIG. 8

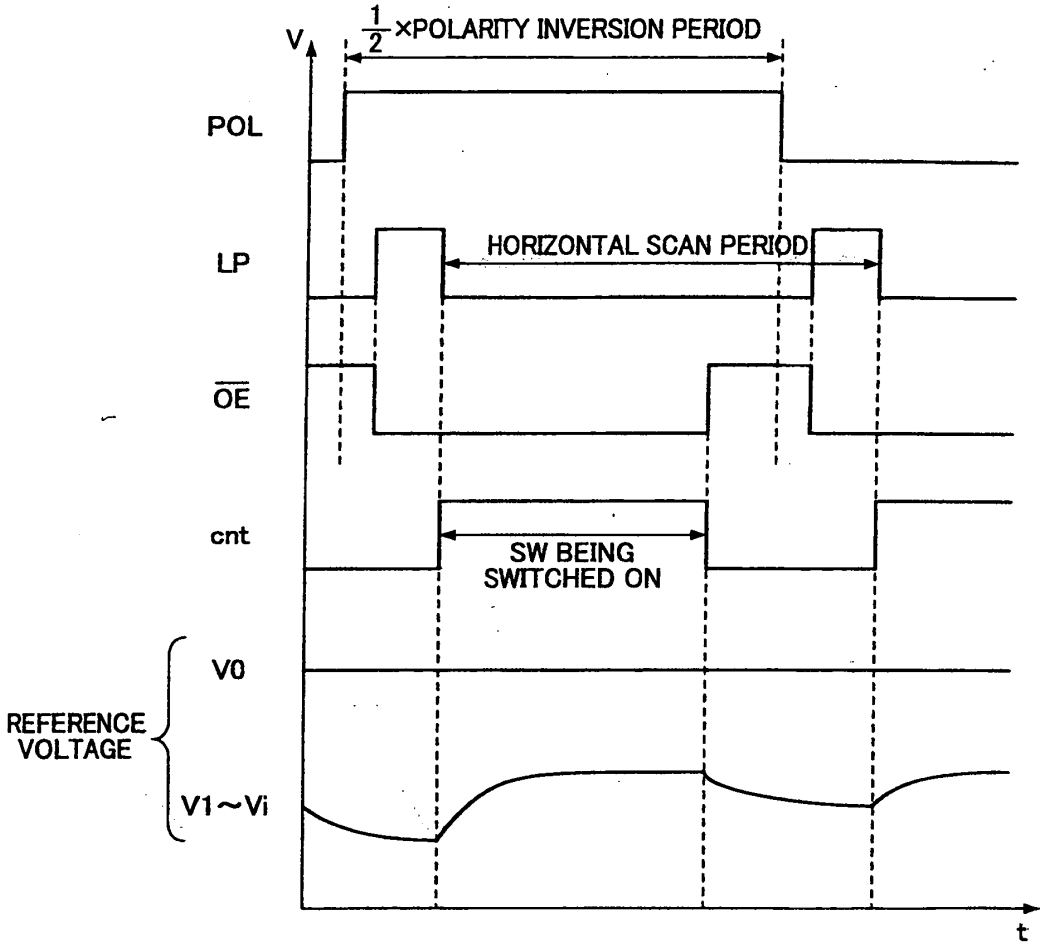

V
1/2×POLARITY INVERSION PERIOD
POL
LP
HORIZONTAL SCAN PERIOD
OE
cnt
SW BEING SWITCHED ON
V0
REFERENCE VOLTAGE
V1~Vi
t

FIG. 9

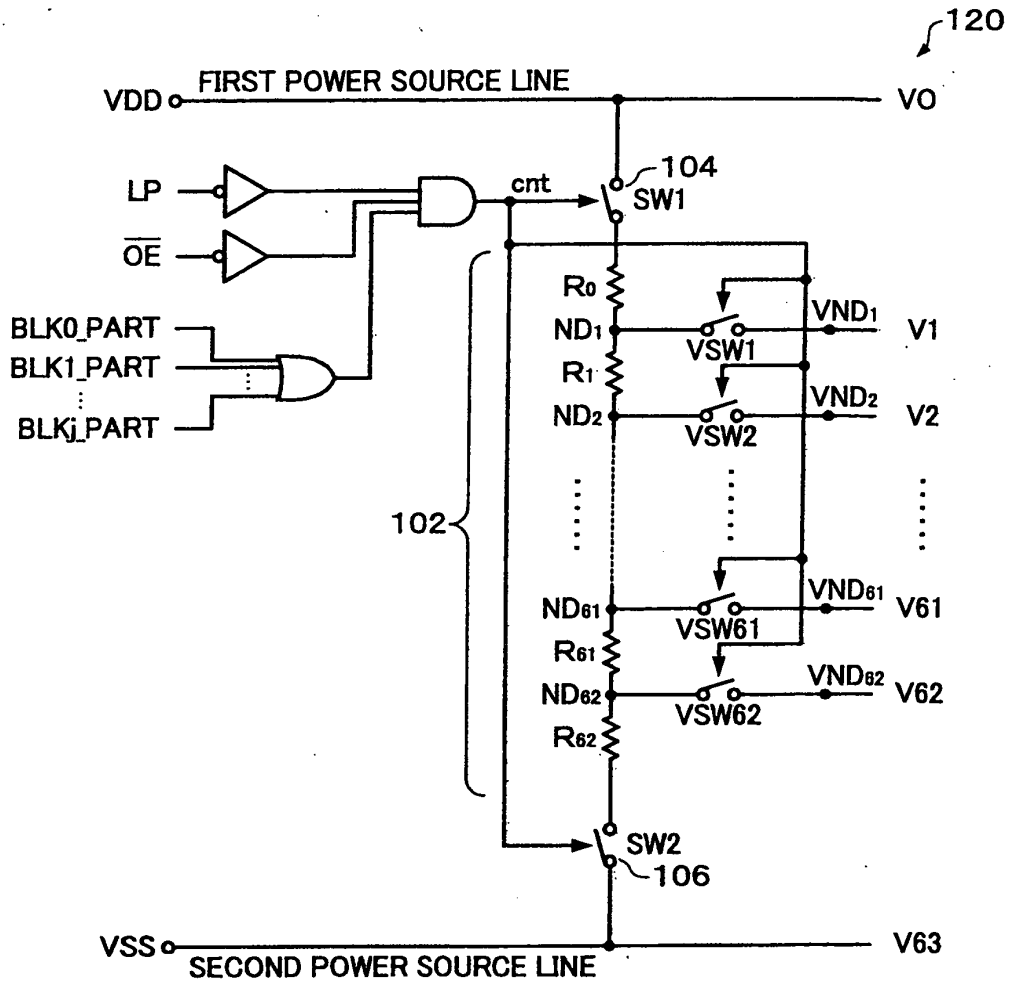

120
VDD
FIRST POWER SOURCE LINE
VO
LP
OE
cnt
104
SW1
BLK0_PART
BLK1_PART
BLKj_PART
R0
ND1
VND1
VSW1
V1
R1
ND2
VND2
VSW2
V2
102
ND61
VND61
VSW61
V61
R61
ND62
VND62
VSW62
V62
R62
SW2
106
VSS
SECOND POWER SOURCE LINE
V63

FIG. 10

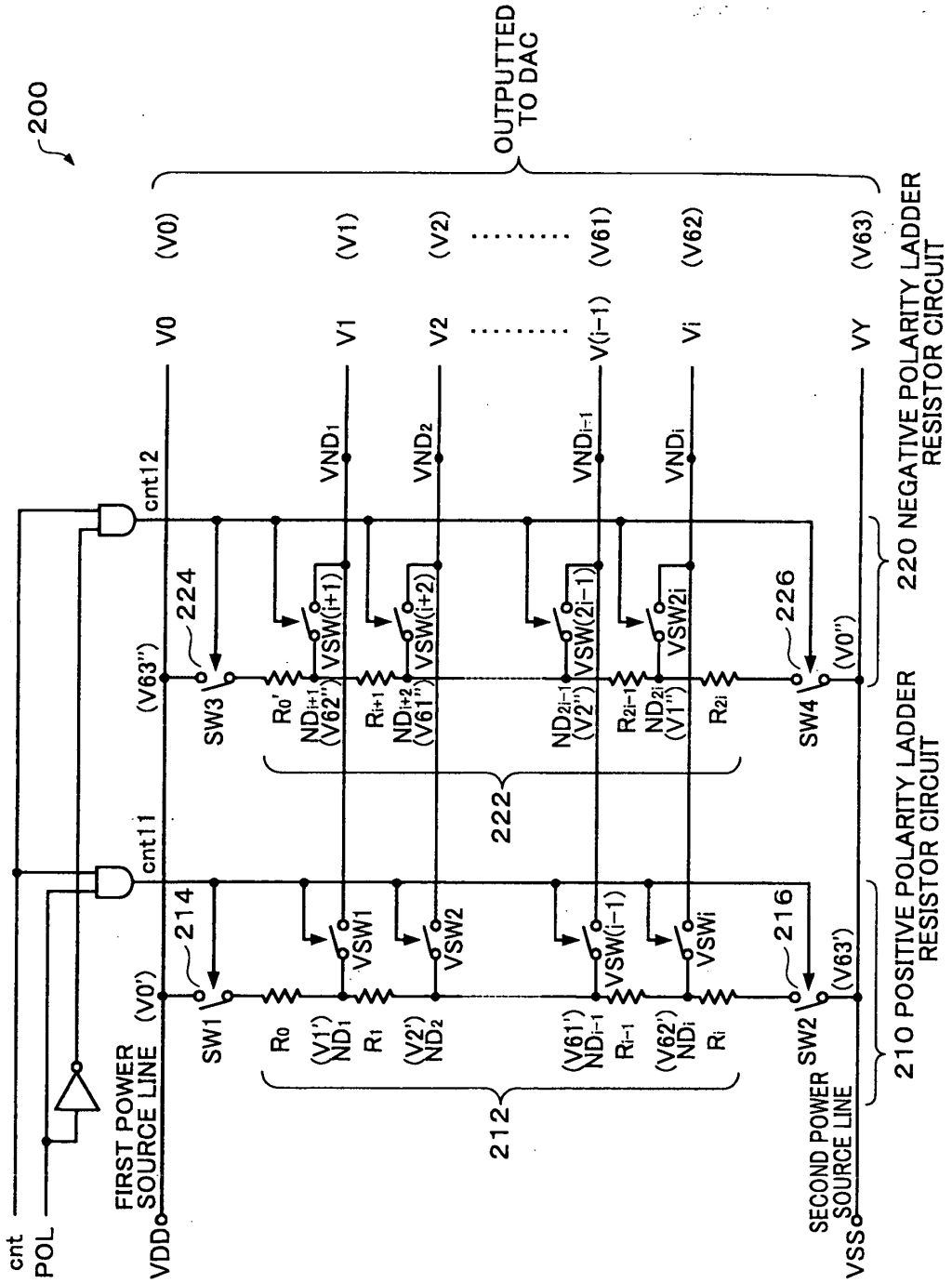

200
OUTPUTTED TO DAC
(V0)
(V1)
(V2)
(V61)
(V62)
(V63)
V0
V1
V2
V(i-1)
Vi
VY
cnt12
cnt11
cnt
POL
VDD
VSS
FIRST POWER SOURCE LINE
SECOND POWER SOURCE LINE
(V0')
(V63')
(V63'')
(V0'')
SW1
SW2
SW3
SW4
214
216
224
226
VSW1
VSW2
VSW(i-1)
VSWi
VSW(i+1)
VSW(i+2)
VSW(2i-1)
VSW2i
VND1
VND2
VNDi-1
VNDi
R0
Ri
Ri-1
Ri
R0'
Ri+1
R2i-1
R2i
(V1')
(V2')
(V61')
(V62')
(V62'')
(V61'')
(V2'')
(V1'')
ND1
ND2
NDi-1
NDi
NDi+1
NDi+2
ND2i-1
ND2i
212
222
210 POSITIVE POLARITY LADDER RESISTOR CIRCUIT
220 NEGATIVE POLARITY LADDER RESISTOR CIRCUIT

FIG. 11

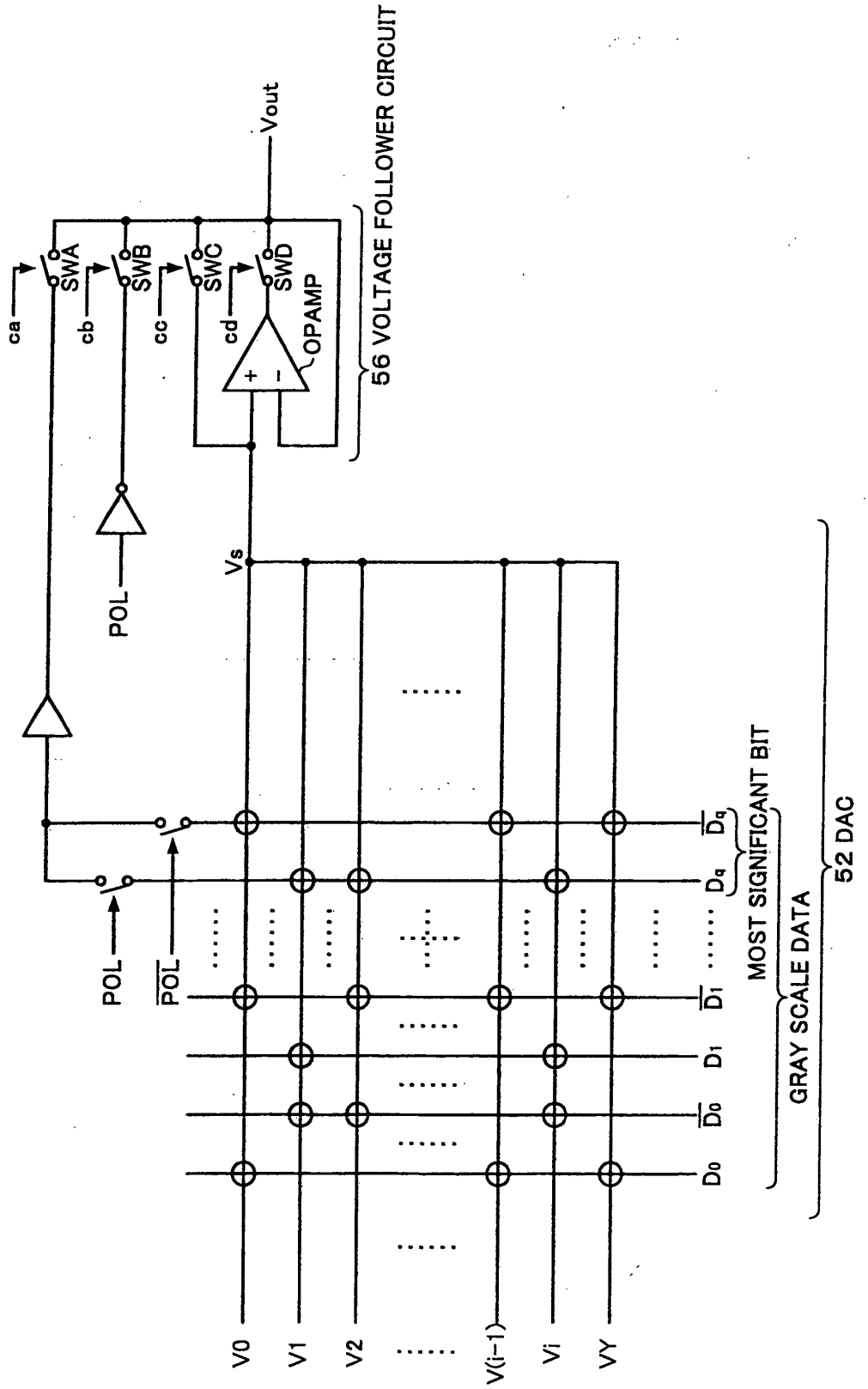

Vout
56 VOLTAGE FOLLOWER CIRCUIT
SWA
SWB
SWC
SWD
OPAMP
ca
cb
cc
cd
Vs
POL
POL
52 DAC
MOST SIGNIFICANT BIT
GRAY SCALE DATA
V0
V1
V2
V(i-1)
Vi
VY

FIG. 12A

		SWA	SWB	SWC	SWD
NORMAL DRIVE	OPERATIONAL AMPLIFIER DRIVE	OFF	OFF	OFF	(ON)
	RESISTOR OUTPUT DRIVE	OFF	OFF	(ON)	OFF
PARTIAL DRIVE	8-COLOR DRIVE	(ON)	OFF	OFF	OFF
	POL DRIVE	OFF	(ON)	OFF	OFF

FIG. 12B

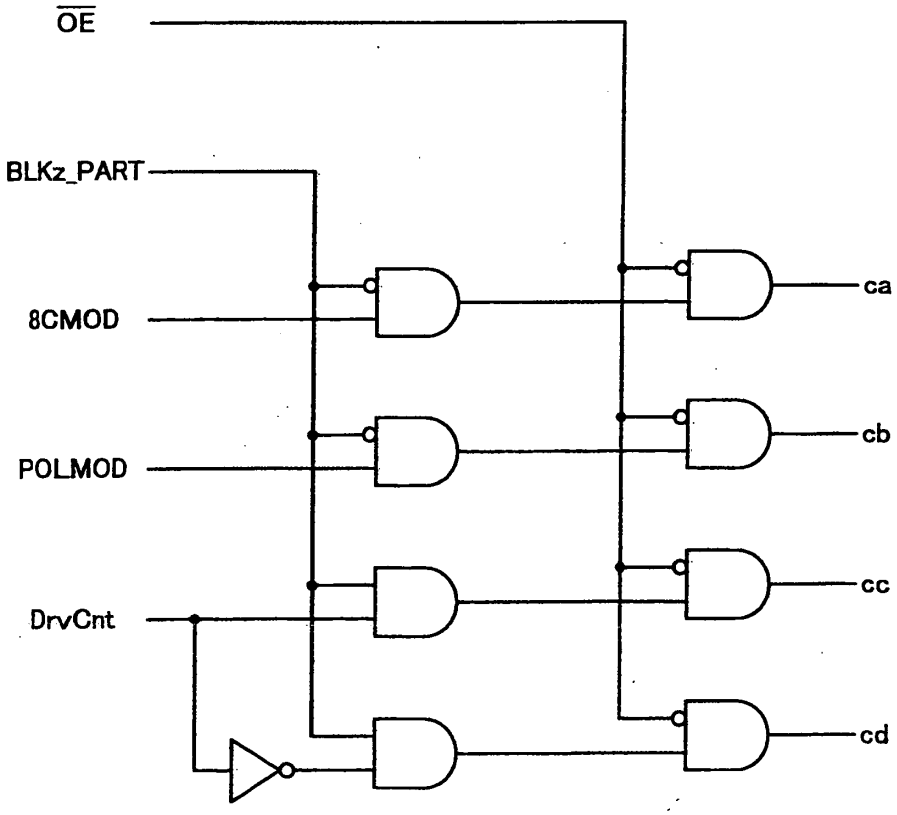
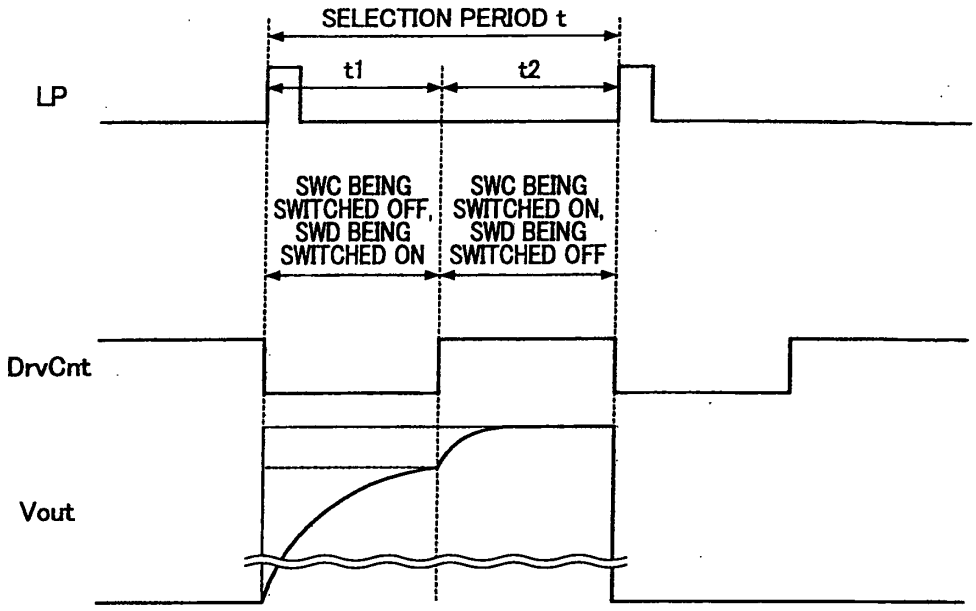


FIG. 13



NORMAL DRIVE MODE (SWA, SWB OFF)

FIG. 14

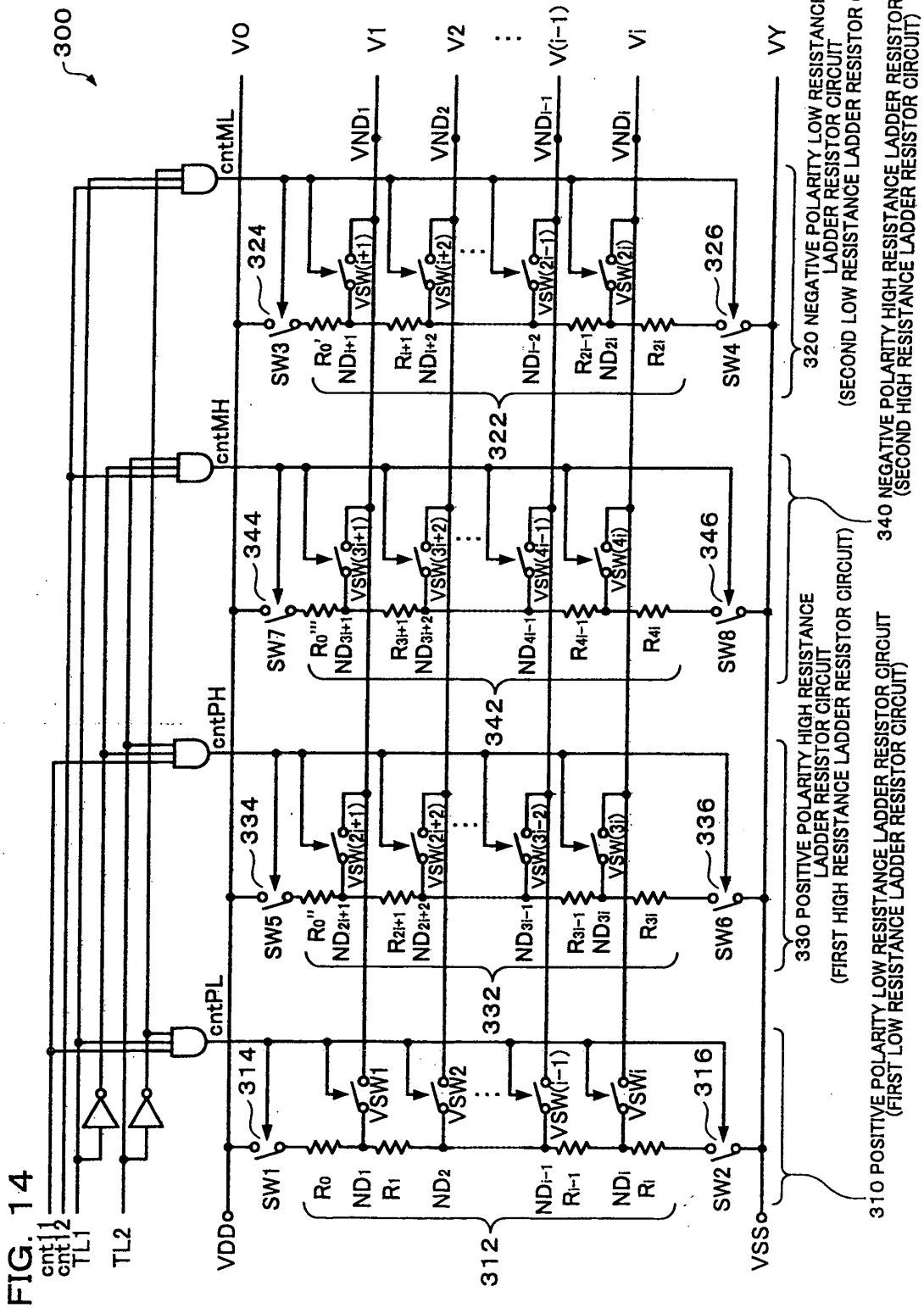

300
cntML
cntMH
cntPH
cntPL
cnt11
cnt12
TL1
TL2
VDD
VSS
V0
V1
V2
V(i−1)
Vi
VY
VND1
VND2
VNDi−1
VNDi
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
VSW1
VSW2
VSWi
VSW(i−1)
VSW(i+1)
VSW(i+2)
VSW(2i−1)
VSW(2i)
VSW(2i+1)
VSW(2i+2)
VSW(3i−2)
VSW(3i)
VSW(3i+1)
VSW(3i+2)
VSW(4i−1)
VSW(4i)
R0
R0'
R0''
R0'''
R1
R2i−1
R2i
R3i−1
R3i
R3i+1
R4i−1
R4i
ND1
ND2
NDi−1
NDi
NDi+1
NDi+2
NDi−2
ND2i−1
ND2i
ND2i+1
ND2i+2
ND3i−1
ND3i
ND3i+1
ND3i+2
ND4i−1
312
314
316
322
324
326
332
334
336
342
344
346
310 POSITIVE POLARITY LOW RESISTANCE LADDER RESISTOR CIRCUIT (FIRST LOW RESISTANCE LADDER RESISTOR CIRCUIT)
320 NEGATIVE POLARITY LOW RESISTANCE LADDER RESISTOR CIRCUIT (SECOND LOW RESISTANCE LADDER RESISTOR CIRCUIT)
330 POSITIVE POLARITY HIGH RESISTANCE LADDER RESISTOR CIRCUIT (FIRST HIGH RESISTANCE LADDER RESISTOR CIRCUIT)
340 NEGATIVE POLARITY HIGH RESISTANCE LADDER RESISTOR CIRCUIT (SECOND HIGH RESISTANCE LADDER RESISTOR CIRCUIT)

FIG. 15

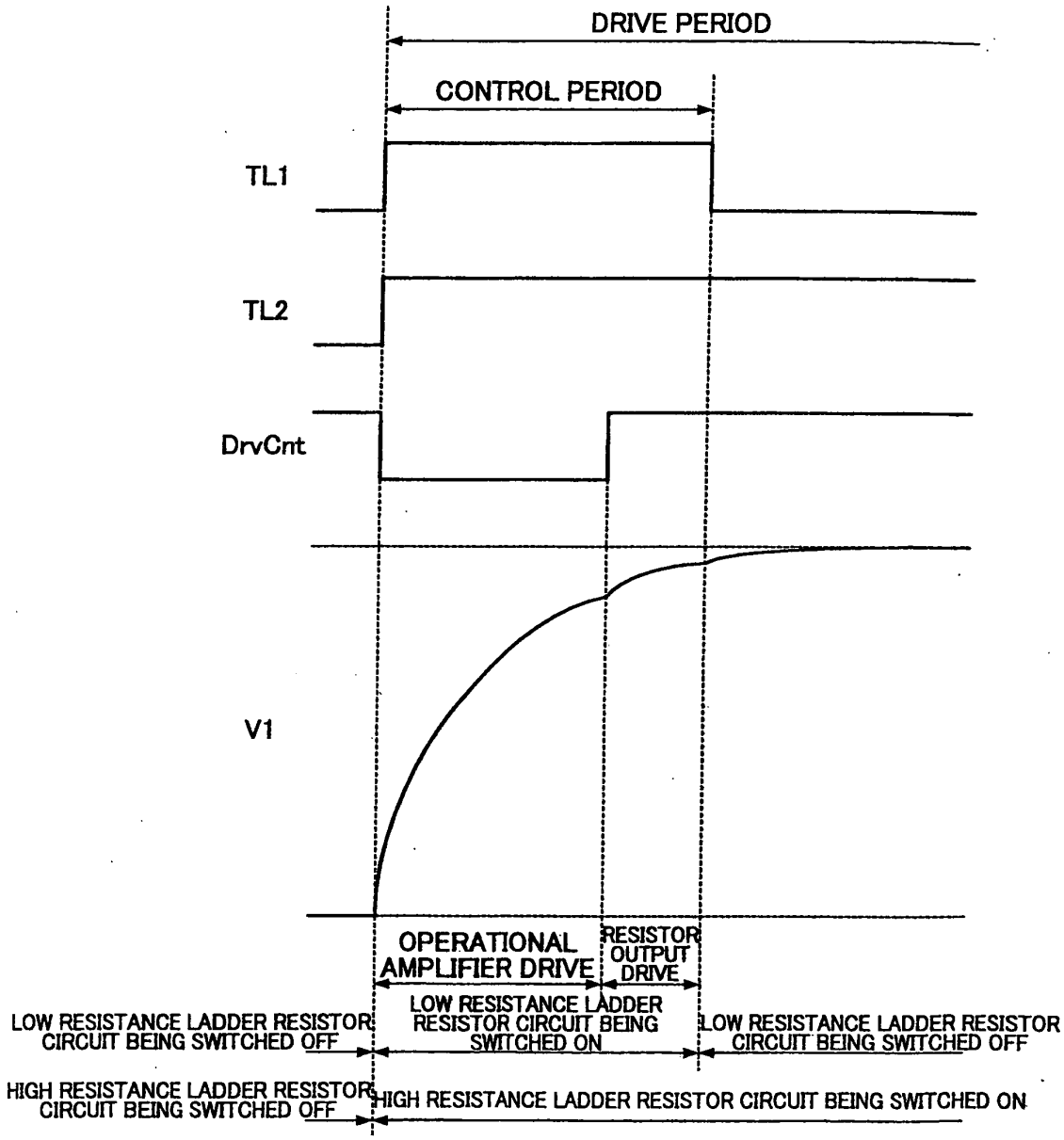

DRIVE PERIOD
CONTROL PERIOD
TL1
TL2
DrvCnt
V1
OPERATIONAL AMPLIFIER DRIVE
RESISTOR OUTPUT DRIVE
LOW RESISTANCE LADDER RESISTOR CIRCUIT BEING SWITCHED OFF
LOW RESISTANCE LADDER RESISTOR CIRCUIT BEING SWITCHED ON
LOW RESISTANCE LADDER RESISTOR CIRCUIT BEING SWITCHED OFF
HIGH RESISTANCE LADDER RESISTOR CIRCUIT BEING SWITCHED OFF
HIGH RESISTANCE LADDER RESISTOR CIRCUIT BEING SWITCHED ON

FIG. 16

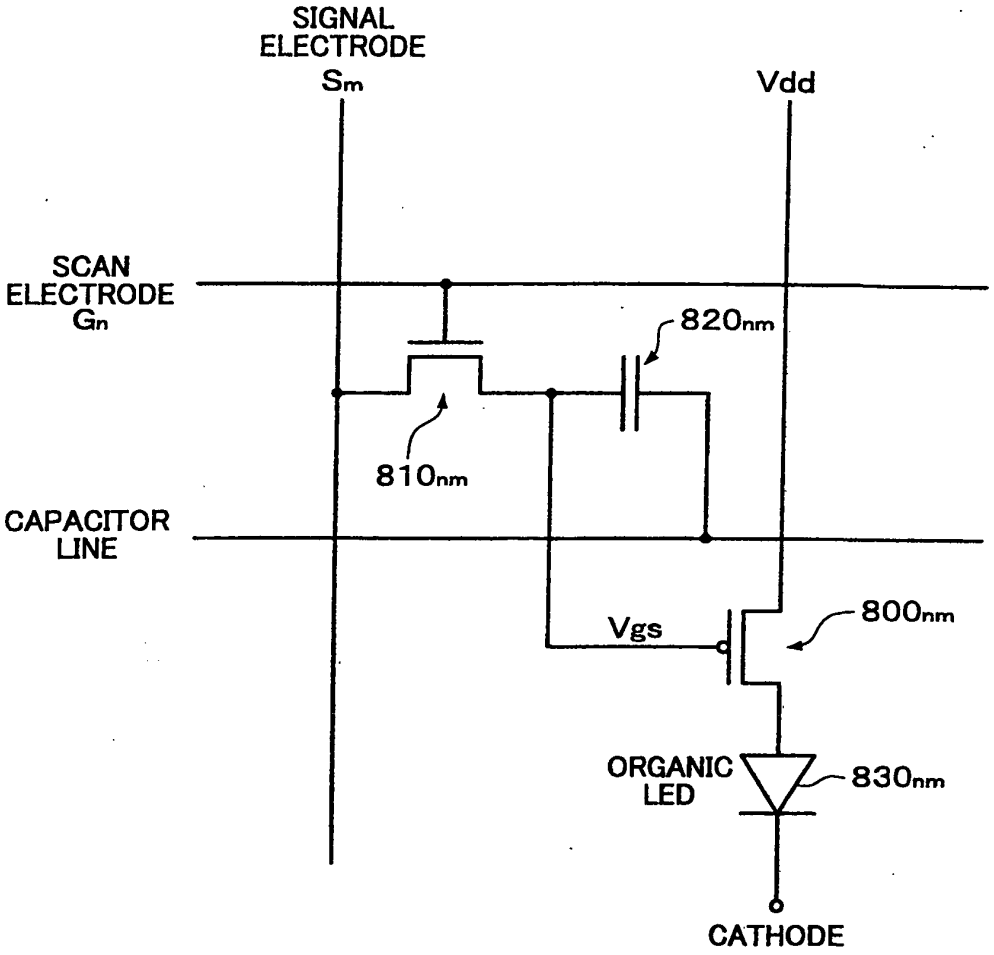

SIGNAL
ELECTRODE
Sm
Vdd
SCAN
ELECTRODE
Gn
820nm
810nm
CAPACITOR
LINE
Vgs
800nm
ORGANIC
LED
830nm
CATHODE

FIG. 17A

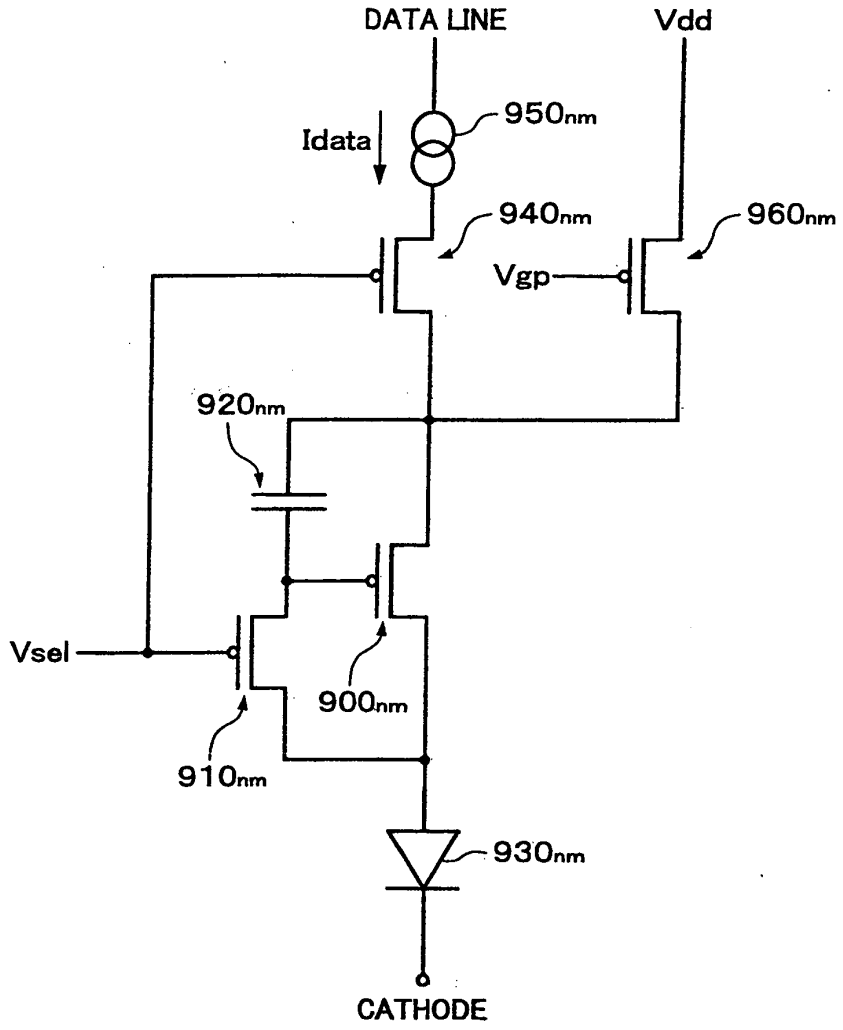
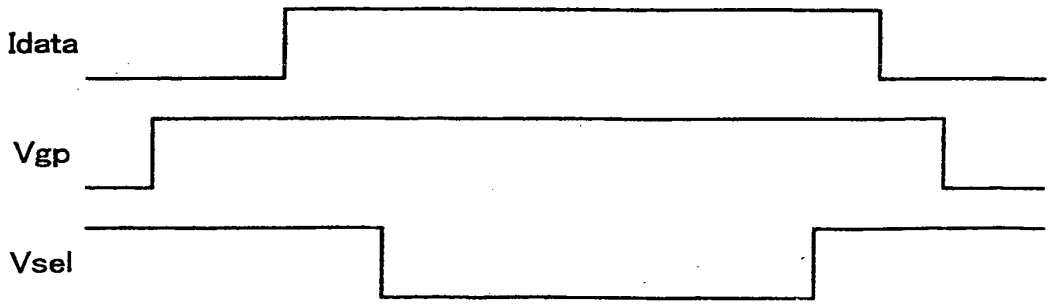
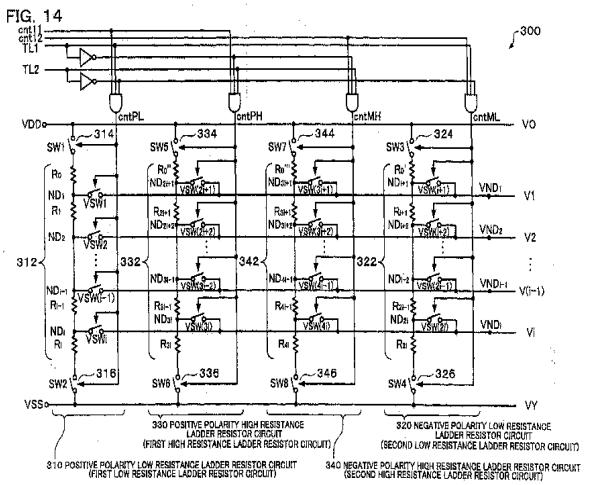


FIG. 17B



专利名称(译)	参考电压产生电路，显示驱动电路和显示装置		
公开(公告)号	EP1551004A2	公开(公告)日	2005-07-06
申请号	EP2005006584	申请日	2003-01-28
[标]申请(专利权)人(译)	精工爱普生株式会社		
申请(专利权)人(译)	SEIKO EPSON CORPORATION		
当前申请(专利权)人(译)	SEIKO EPSON CORPORATION		
[标]发明人	MORITA AKIRA		
发明人	MORITA, AKIRA		
IPC分类号	G02F1/133 G05F1/10 G09G3/20 G09G3/32 G09G3/36 G09G5/06		
CPC分类号	G09G3/3688 G09G3/2011 G09G3/32 G09G3/3233 G09G3/325 G09G3/3614 G09G3/3685 G09G3/3696 G09G5/06 G09G2300/0842 G09G2300/0861 G09G2310/0248 G09G2310/0251 G09G2310/027 G09G2310/04 G09G2320/0276		
优先权	2002032680 2002-02-08 JP		
其他公开文献	EP1551004A3		
外部链接	Espacenet		

摘要(译)



产生用于驱动液晶显示器的多值参考电压的参考电压产生电路包括：第一和第二电源线之间的第一至第四梯形电阻电路（312,322,332,342）。第一至第i参考电压输出切换电路（VSW1-VSWi）分别插入第一梯形电阻电路（312）的第一至第i分割节点（ND1-NDi）之间，其中i是大于或等于的整数到2，并且第一到第i个参考电压输出节点（VND1-VNDi）。第（i + 1）个第2i参考电压输出切换电路（VSW（i + 1）-VSW2i）分别插入在第（i + 1）至第2i分割节点（NDi + 1-ND2i）之间。第二梯形电阻器电路（322）和第一至第i参考电压输出节点。（2i + 1）至第3i参考电压输出切换电路（VSW（2i + 1）-VSW（3i））分别插入在第（2i + 1）至第3i分割节点（ND2i + 1-ND3i）之间）第三梯形电阻电路（332）和第一至第i参考电压输出节点。（3i + 1）至第4i参考电压输出切换电路（VSW（3i + 1）-VSW（4i））分别为插入在第四梯形电阻电路（342）的第（3i + 1）至第4i分割节点（ND3i + 1-ND4i）与第一至第i参考电压输出节点之间。当极性反转驱动系统在给定极性反转周期内向信号电极输出的电压的极性反转被重复时：第一至第i参考电压输出开关电路在正极性驱动的给定控制周期期间接通。在一个负极性驱动周期的给定控制周期内关闭周期;第（i + 1）至第2i参考电压输出切换电路在正极性驱动时段中的给定控制时段期间被关断，并且在负极性驱动时段中的给定控制时段期间被接通;第（2i + 1）至第3i参考电压输出切换电路在正极性驱动期间接通，在负极性驱动期间切断。第（3i + 1）至第4i参考电压输出切换电路在正极性驱动期间接通，在负极性驱动期间断开期。