(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 047 043 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
18.07.2007 Bulletin 2007/29

(51) Int Cl.:
G09G 3/36 *(2006.01)* ***G09G 3/20*** *(2006.01)*

(21) Application number: **00302974.1**

(22) Date of filing: **07.04.2000**

(54) **Image display apparatus with conversion of input video signals**

Anzeigegerät mit Umwandlung von Videoeingangssignalen

Dispositif d'affichage avec conversion des signaux vidéo d'entrée

(84) Designated Contracting States:
CH DE FR LI

(30) Priority: **19.04.1999 JP 11109899**

(43) Date of publication of application:
25.10.2000 Bulletin 2000/43

(73) Proprietor: **SONY CORPORATION**
Tokyo 141 (JP)

(72) Inventors:
- **Murayama, Hiroshi**
  Tokyo 141 (JP)
- **Fujimoto, Tadashi**
  Tokyo 141 (JP)

(74) Representative: **Pratt, Richard Wilson et al**
D Young & Co
120 Holborn
London EC1N 2DY (GB)

(56) References cited:
EP-A- 0 854 466
JP-A- 10 091 127
JP-A- 10 091 134

EP 1 047 043 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to an image display apparatus. Illustrative embodiments of the invention relate to display apparatus having displays of a dot matrix type, such as a liquid crystal display, which is capable of suitably displaying any format of image signal which is input.

2. Description of the Related Art

[0002] Conventionally, raster scan type CRTs have been widely used for image displays for computers. This CRT display receives from a computer a video signal including an analog video signal containing a vertical synchronization signal and horizontal synchronization signal mixed together to display a desired image.

[0003] Also, recently, displays using liquid crystal panels (LCD) have come under attention from the viewpoints of space-saving, energy-saving, lower costs, etc. A liquid crystal panel is a display of a dot matrix type wherein pixels are of a fixed size and each pixel is supplied with voltage separately to separately control them for the display.

[0004] There are many types of video signals depending on the resolution, input frequency, etc. For example, as the resolution, there are 640 x 480 (horizontal pixels x vertical pixels (same below)), 720 x 400, 800 x 600, 1024 x 768, 1152 x 864, 1280 x 1024, etc. Furthermore, even among signals of the same resolution of 1280 x 1024, there are a large number of frequencies of signals, such as 64 kHz/60 Hz (horizontal frequency/vertical frequency (same below)), 80 kHz/75 Hz, 91 kHz/85 Hz, 81 kHz/77 Hz, etc.

[0005] For the specifications of these video signals, those established by the Video Electronics Standard Association (VESA) are widely known.

[0006] Although there are many types of video signals as explained above, many computer displays recently used are so-called "multi-sync" types, that is, are not limited to the type of video signal and are capable of automatically handling a plurality of types of video signals and suitably displaying the image.

[0007] A multi-sync type display is ordinarily designed to detect characteristics relating to specifications of a video signal, such as the state of a synchronization signal, from an input video signal, compare the characteristics with the specifications of video signals registered in advance to identify the type of the video signal, adjust a drive cycle and amplitude of scanning lines of the display so as to match with a synchronization signal of the video signal based on the identified results, and display an image in accordance with the video signal.

[0008] However, an unregistered type of video signal is sometimes input to a multi-sync display handling a plurality of types of video signals by this method.

[0009] In such a case, up until now, the method has been taken of selecting the video signal of the closest specifications among the registered video signals and controlling the display circuit based on the specifications of that video signal or of preparing default data and controlling the display circuit by using the default data when there is no matching video signal.

[0010] Also, the VESA has established a method of determining a signal timing of a not registered signal as the GTF (generalized timing formula). The method of controlling the display circuit based on this method is also being taken.

[0011] To display an analog image signal on a display of a dot matrix type, the input image signal has to be sampled at predetermined sampling intervals to convert it from an analog to digital format and made to match with the number of horizontal and vertical pixels of the display. If the number of pixels matches and the pixels are properly controlled, basically there will be almost no effect due to the differences of displays and a stable output can be expected. If the number of horizontal and vertical pixels do not match between the signal and the display, however, proper display is no longer possible.

[0012] Note that the information on the dot intervals in the horizontal direction of image signals for such a signal conversion is called a "dot clock". This information is also included in the VESA standard. In a CRT or raster scan type display, however, display is possible even without knowing the precise number of dots in the horizontal direction. Therefore, this is a parameter which is not ordinarily used for display.

[0013] In a dot matrix type multi-sync display, an image sometimes cannot be properly displayed by the conventional method of processing explained above when a non-registered video signal is input.

[0014] In the method of using the specifications of the video signal having the closest specifications to the characteristics of the detected input signal, the disadvantages sometimes arise that a signal is processed as a signal having a different resolution (number of valid pixels) just because the horizontal and vertical frequencies happen to be close, that there is no registered signal of a close frequency, the signal is processed as a signal having a little distant frequency, and the position of the image shifts, or that the scaling rate is not suitable and therefore the image overflows from the screen or conversely becomes remarkably smaller than the screen.

[0015] Further, in the method of using default data, the method works well when the signal is close to the default data, but when this is not so, the signal sometimes will not match it at all and proper display will not be possible.

[0016] Also, the GTF only establishes the time and does not include information of the dot clock frequency, so while it is useful in determining operations of a deflection circuit of the CRT, in a dot matrix type display handling fixed pixels such as a liquid crystal display, efficient information cannot be obtained and proper display is similarly not possible.

In EP0854466 a horizontal and a vertical frequency of the input image signal are detected and based on this the number of horizontal lines is calculated and a conversion ratio is estimated (factor for scaling: number of horizontal display lines / number of lines of panel). The horizontal and vertical scaling are then based on the conversion ratio. The possibility to consider the aspect ratio of the input signal for determining the conversion ratio is mentioned.

SUMMARY OF THE INVENTION

[0017] An embodiment of the present invention seeks to provide a dot matrix type image display apparatus capable of properly displaying an image even if a non-registered image signal is input.

[0018] An image display apparatus of the present invention as claimed in claim 1.

[0019] In an image display apparatus having such a configuration, the characteristic detection means finds the number of vertical lines from the input image signal and the horizontal pixel number estimation means multiplies the found number of the vertical lines by a predetermined constant to estimate the number of horizontal pixels. Then, the A/D conversion means successively samples the signal at every horizontal period of the input image signal by a predetermined sampling cycle determined based on the estimated value of the number of horizontal pixels and converts it from an analog to digital format. The signal conversion means converts the thus generated digital image signal is converted to a display signal of a predetermined dot matrix type based on the configuration of the display means and displays it by the display means.

[0020] Preferably, the image display apparatus of the present invention further comprises a memory means in which information regarding specifications of said image signal including the number of horizontal pixels are stored for each of any plurality of types of image signals and an image signal identification means for comparing said detected predetermined characteristics with said information of image signals stored in advance to search for the same type of image signal as said input image signal from the plurality of types of image signals whose information is stored in advance; wherein said A/D conversion means performs said sampling by a sampling cycle based on said information regarding the number of horizontal pixels of the image signals stored in said memory means when an image signal of the same type as said input image signal is found and performs said sampling by a sampling cycle based on an estimated value of said calculated number of horizontal pixels when an image signal of the same type as said input image signal is not found.

[0021] Specifically, said horizontal pixel number estimation means multiplies said detected number of vertical lines with a predetermined constant between 1.6 to 1.85 when said input image signal is an image signal suitable to a display having an aspect ratio of 4:3; multiplies said detected number of vertical lines with a predetermined constant between 1.5 to 1.7 when said input image signal is an image signal suitable to a display having an aspect ratio of 5:4; and multiplies said detected number of vertical lines with a predetermined constant between 1.9 to 2.1 when said input image signal is an image signal suitable to a display having an aspect ratio of 16:9 so as to calculate the estimated value of the number of horizontal pixels.

[0022] More specifically, said display means is a liquid crystal display means.

[0023] Further, preferably, said signal conversion means performs conversion of said digital image signal based on said information regarding the specifications of the image signal stored in said memory means when an image signal of the same type as said input image signal is found and obtains information regarding the specifications of the image signal based on characteristics of said detected input image signal and performs conversion of said digital image signal based on the information when an image signal of the same type as the input image signal is not found.

[0024] Specifically, said signal conversion means obtains information regarding the specifications of the image signal in accordance with the GTF (generalized timing formula) established by the VESA (Video Electronics Standard Association) based on the characteristics of said detected input image signal when an image signal of the same type as the input image signal is not found.

[0025] More specifically, said characteristic detection means detects a vertical synchronization signal and a horizontal synchronization signal from said input image signal and counts the number of horizontal synchronization signals included in a vertical synchronization period to obtain said number of vertical lines.

[0026] Alternatively, specifically, said characteristic detection means detects a vertical synchronization signal and a horizontal synchronization signal from said input image signal, finds a horizontal frequency and vertical frequency, and divides the horizontal frequency by the vertical frequency to find the number of vertical lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] An understanding of the present invention will become clearer from the following illustrative description of the preferred embodiments given with reference to the accompanying drawings, in which:

Fig. 1 is a view of the relationship of the number of vertical lines and the number of dots in a horizontal period in an image signal having an aspect ratio of 4:3;
Fig. 2 is a block diagram of the configuration of a liquid crystal display of an embodiment of the present invention;
Fig. 3 is a block diagram of the microcomputer of the liquid crystal display shown in Fig. 2; and
Fig. 4 is a view for explaining processing of the microcomputer shown in Fig. 3 from detection of a signal to setting of control parameters.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] Below, preferred embodiments will be described with reference to the accompanying drawings.
[0029] An embodiment of the present invention will be explained with reference to Figs. 1 to 4.
[0030] Reference will be made, by way of example, to a liquid crystal display capable of properly displaying any input video signal.
[0031] First, a method of estimation of specifications of an unknown video signal used in the liquid crystal display of the present embodiment will be explained.
[0032] As explained above, when displaying a conventional analog video signal on a dot matrix type display such as a liquid crystal display panel, it is necessary to properly sample the video data for each horizontal period for each correct pixel included in that horizontal period. Information of the number of dots in the horizontal period, that is, dot clock information, becomes necessary for this.
[0033] However, the number of dots in a horizontal period is unnecessary information for a raster scan type display and is not able to be detected only by observing the signal. Also, generally, since it does not have any direct relationship with the horizontal synchronization frequency, it was unable to be obtained unless information was given separately.
[0034] However, when investigating the relationship between the number of vertical lines and the number of dots in a horizontal period for various video signals, it was found that there was a correlation between the two.
[0035] The main specification data of the video signals VGA, SVGA, XGA, and SXGA and the ratios of the total number of pixels in the horizontal direction to the total number of lines in the vertical direction are shown in Table 1.

[Table 1]

[0036]

(Table 1)

Type	VGA	SVGA	XGA	SXGA
H resolution	640	800	1024	1280
V resolution	480	600	768	1024
Fh	375	469	600	640
Fv	7499	7500	7503	6002
H_TOTAL_DOT	840	1056	1312	1688
H_FP	16	16	16	48
H_SBP	184	240	272	360
V_TOTAL_LINE	500	625	800	1066
V_FP	1	1	1	1
V_SBP	19	24	31	41
Ratio of Number of HV Pixels	1.68	1.6896	1.64	1.583

[0037] Note that the ratio of the total number of the HV pixels in Table 1 is obtained from the total number of pixels in the horizontal direction (H_TOTAL_DOT)/total number of lines in the vertical direction (V_TOTAL_LINE).
[0038] The relationship of the number of vertical lines and the number of dots in a horizontal period of a video signal having an aspect ratio of 4:3, which includes the VGA, SVGA, and XGA shown in Table 1, is shown in Fig. 1.
[0039] As shown in the figure, the number of dots in the horizontal period becomes a value of the number of vertical

lines multiplied by 1.6 to 1.85 or multiplied by about an average 1.7.

[0040] Similarly, in a video signal suitable for a display of another aspect ratio, for example in a video signal having an aspect ratio of 5:4, which includes the SXGA shown in Table 1, the number of dots in a horizontal period becomes a value of the number of vertical lines multiplied by 1.5 to 1.7 or by about an average 1.6, while in a video signal having an aspect ratio of 16:9, the number of dots in a horizontal period is the number of vertical lines multiplied by 1.9 to 2.1 or multiplied by about an average 2.0.

[0041] By using this relationship, the number of dots in a horizontal period can be estimated from the information of the number of vertical lines.

[0042] The information of the number of vertical lines is obtained easily from a video signal, so the dot clock information is to be able to be estimated by observing the input video signal without any other information.

[0043] A liquid crystal display 10 according to an illustrative embodiment of the invention is designed to estimate the dot clock information of any input video signal by using an illustrative method of estimation of the specifications of a video signal according to an embodiment of the present invention, to properly convert the video signal to a display signal of a dot matrix type, and to properly display the input video signal.

[0044] The liquid crystal display 10 of the present embodiment will be explained below.

[0045] Figure 2 is a block diagram of the configuration of the liquid crystal display 10.

[0046] The liquid crystal display 10 comprises an amplifier 11, a synchronization processor 12, a microcomputer 13, an EEPROM 14, a PLL circuit 15, an analog/digital (A/D) converter 16, a pixel converter 17, and a liquid crystal panel 18.

[0047] First, the configurations and functions of the parts of the liquid crystal display 10 will be explained.

[0048] The amplifier 11 amplifies an input video signal by a predetermined amplifying rate and outputs it to the A/D converter 16.

[0049] The synchronization processor 12 shapes the waveform of a synchronization signal of the input video signal and outputs it to the microcomputer 13, PLL circuit 15, and pixel converter 17.

[0050] The microcomputer 13 identifies the type of the input video signal based on the synchronization signal of the video signal input from the synchronization processor 12, sets control parameters for the PLL circuit 15 and the pixel converter 17 so that the PLL circuit 15 and the pixel converter 17 operate under suitable conditions in accordance with the identified video signal, and controls the operations. At this time, the microcomputer 13 refers to correction data stored in the EEPROM 14 to set the final control parameters. When the type of the input video signal is not able to be identified, the microcomputer 13 determines the control parameters by an illustrative method according to an embodiment of the present invention which will be explained later on and controls the PLL circuit 15 and the pixel converter 17 by this in the same way.

[0051] Note that the control parameter set in the PLL circuit 15 by the microcomputer 13 is specifically the number of dot clocks included in a horizontal period of the video signal. The microcomputer 13 sets the same as a frequency division rate to the PLL circuit 15. Also, the control parameters set in the pixel converter 17 are the number of horizontal valid pixels, the number of vertical valid lines, and the number of dots and the number of lines before a signal starts.

[0052] The microcomputer 13 will be explained in further detail with reference to Fig. 3 and Fig. 4.

[0053] Figure 3 is a block diagram of the microcomputer 13.

[0054] As shown in Fig. 3, the microcomputer 13 comprises a processing portion 131, a signal specification storing ROM 132, a program ROM 133, a RAM 134, an interface (I/F) portion 135, and an internal bus 136.

[0055] Note the microcomputer 13 is formed on single semiconductor integrated circuit (IC) as a one-chip microcomputer.

[0056] First, the configuration of the parts of the microcomputer will be explained.

[0057] The processing portion 131 operates based on a program stored in the program ROM 133 and performs processing for controlling the PLL circuit 15 and the pixel converter 17 based on a synchronization signal input from the synchronization processor 12 as explained above.

[0058] The detailed contents and operations of the processing portion 131 will be explained later on as the operation of the microcomputer 13.

[0059] The signal specification storing ROM 132 is a memory portion storing a horizontal frequency, a vertical frequency, a polarity of a horizontal synchronization signal, a polarity of a vertical synchronization signal, the total number of dots in the horizontal direction, a front porch in the horizontal direction, a back porch in the horizontal direction, the number of lines in the vertical direction, a front porch in the vertical direction, a back porch in the vertical direction, the number of horizontal valid pixels, and the number of vertical valid lines of all video signals which may be input to the liquid crystal display 10. The data stored in the signal specification storing ROM 132 is suitably read by the processing portion 131.

[0060] Note that the data stored in the signal specification storing ROM 132 is in the video signal format established by the VESA.

[0061] The signal specification storing ROM 132 is formed on an IC in the form of a mask ROM.

[0062] The program ROM 133 is a memory portion storing a program of the processing of the processing portion 131 and parameters for the processing. The contents of the program stored in the program ROM 133 will be also explained

later on as the operation of the microcomputer 13.

[0063] The RAM 134 is a memory portion for temporarily storing data at the time when the program ROM 133 performs control processing on the PLL circuit 15 and the encoding processor 17 in accordance with the program stored in the program ROM 133.

[0064] The I/F portion 135 is an interface for inputting and outputting data and control orders to the microcomputer 13 comprised as a one-chip microcomputer as explained above.

[0065] The I/F portion 135 is connected to the internal bus 136 inside the microcomputer 13 and connected to the external bus 19 outside the microcomputer 13. The external bus 19 has connected to it the synchronization processor 12, the EEPROM 14, the PLL circuit 15, the pixel converter 17, etc. Information relating to the video signal from the synchronization processor 12 is input, correction data from the EEPROM 14 is read, and control parameters are output to the PLL circuit 15 and the pixel converter 17 through the I/F portion 135. Note that the data transfer rate of the external bus 19 is about 100 kbits/sec in the present embodiment.

[0066] The internal bus 136 is an internal bus of the microcomputer 13 and used for transferring data between the processing portion 131, the signal specification storing ROM 132, the program ROM 133, the RAM 134, and the I/F portion 135.

[0067] Note that data transfer inside the microcomputer via the internal bus 136 can be performed in units of bus width (for example, in units of bytes or words) at a rate of almost 10 MHZ, which is the operation clock of the microcomputer 13.

[0068] Next, the operation of the microcomputer 13 having the above configuration will be explained with reference to Fig. 4.

[0069] Figure 4 is a flow chart for explaining the operation of the microcomputer 13, the content of the program stored in the program ROM 133, and the processing in the processing portion 13 based on the program.

[0070] When input of a synchronization signal from the synchronization processor 12 is started, the microcomputer 13 detects the same and start a series of processing (step S41).

[0071] First, the processing portion 131 waits for the input signal to stabilize and the detects a horizontal signal and a vertical signal from the input signal (step S42).

[0072] Then, based on the detected horizontal synchronization signal and vertical synchronization signal, it measures a horizontal synchronization signal frequency (also simply referred to as a horizontal frequency) and a vertical synchronization signal frequency (also simply referred to as a vertical frequency) and detects polarity information of the horizontal/vertical synchronization signals (step S43).

[0073] Then, based on the information, it searches through information relating to the specifications of signals stored in the signal specification storing ROM 132 and investigates whether there is a video signal having the same specifications as the measured and detected horizontal frequency, vertical frequency, and polarities of the horizontal/vertical synchronization signals (step S44).

[0074] When there is a video signal having the same specifications, namely, when the input video signal is a video signal registered in the signal specification storing ROM 132, further detailed information of the video signal, that is, information used for controlling the PLL circuit 15 and the pixel convertor 17, specifically, information of the number of dot clocks included in a horizontal period of the video signal, the number of horizontal valid pixels, the number of vertical valid lines, etc., is further read from the signal specification storing ROM 132. Also, simultaneously, the processing portion 131 reads correction data from the EEPROM 14 via the I/F portion 135 (step S45).

[0075] Based on the read information and the correction data, the processing portion 131 sets as a value of a division ratio the number of dot clocks included in the horizontal period to the PLL circuit 15 (step S46). Note that the relationship between the dot clocks and the division ratio is defined as formula (1).

[Formula 1]

$$\text{Dot clocks/Division ratio} = \text{Horizontal frequency} \quad \ldots(1)$$

[0076] Further, the processing portion 131 obtains the control parameters relating to pixel conversion processing such as the number of horizontal valid pixels, the number of vertical valid lines, and the number of horizontal dots and vertical lines before starting the signal, based on the read information and the correction data, and sets the parameters in the pixel convertor 17 (step S47).

[0077] As explained above, by setting the control parameters to the PLL circuit 15 and the pixel convertor 17, the control processing of the signal conversion on a series of newly input pixel signal ends (step S51).

[0078] On the other hand, at step S44, when the input video signal has not been registered in the signal specification storing ROM 132, it performs the processing according to an illustrative embodiment the present invention, that is,

estimates the dot clock information for the unknown signal from just the signal input from the synchronization processor 12 to obtain the control parameters for the PLL circuit 15 and the encoding processor 17.

[0079] Specifically, first, it obtains the number of vertical lines (step S48). The number of vertical lines may be obtained by counting the number of horizontal synchronization signals included in a vertical synchronization period or by dividing the horizontal frequency by the vertical frequency using the data measured in step S43.

[0080] Next, it calculates the number of dots in a horizontal period (step S49). It obtains the number of dots in a horizontal period by multiplying the number of vertical lines obtained at step S48 with a predetermined constant 1.7 as explained above with reference to Fig. 1.

[0081] Then it sets the number of dots is a horizontal period to the PLL circuit 15 as a division ratio of the PLL circuit 15 (step S46).

[0082] Next, based on the number of dots in a horizontal period and the number of vertical lines obtained in advance, it obtains the control parameters of the number of horizontal valid pixels, the number of vertical valid lines, and the number of horizontal dots and vertical lines before starting the signal from the formulas (2) to (5) by using the ratio established by the GTF (generalized timing formula) proposed by the VESA (step S50).

[Formula 2]

$$\text{Number of horizontal valid pixels} = \text{number of dots in a horizontal period} \times (0.7 + 3/\text{horizontal frequency (kHz)}) \quad \ldots(2)$$

$$\text{Number of vertical valid lines} = \text{number of vertical lines} - 0.55 \times \text{horizontal frequency (kHz)} - 1 \quad \ldots(3)$$

$$\text{Number of dots before signal starts} = \text{number of dots in horizontal period} \times (0.23 - 1.5/\text{horizontal frequency (kHz)}) \quad \ldots(4)$$

$$\text{Number of lines before signal starts} = 0.55 \times \text{horizontal frequency (kHz)} \quad \ldots(5)$$

[0083] Then, it sets the obtained parameters in the pixel converter 17 (step S47).

[0084] Also, when the input signal is unknown as well, it sets the control parameters in the above way to the PLL circuit 15 and the pixel converter 17, then ends the series of control processing for the signal conversion on the newly input signal (step S51).

[0085] The configuration and the operation of the microcomputer 13 were as explained above.

[0086] An explanation of the configuration of the different parts of the liquid crystal display 10 will follow.

[0087] The EEPROM 14 is a memory portion for storing correction data for proper display on the liquid crystal panel

18 set in consideration of an input delay of the video signal, a circuit delay of the synchronization processor 12, etc.

[0088] Since the amount of correction by the delay changes by the frequency, the measured data of a delay error in accordance with the frequency of the video signal to be displayed on the liquid crystal display 10 is written in the EEPROM 14. Note that the error is measured and the correction data is written, for example, in an adjustment process after substantial production of the liquid crystal display 10 is completed.

[0089] The PLL circuit 15 generates a predetermined clock based on the control parameter set by the microcomputer 13 and outputs it to the A/D converter 16 and the pixel converter 17. The clock generated by the PLL circuit 15 corresponds to the dot clock in the horizontal direction of the input video signal.

[0090] The A/D converter 16 successively performs sampling on the video signal input from the amplifier 11 in synchronization with the clock input from the PLL circuit 15, generates a digital signal by A/D conversion, and outputs the same to the pixel converter 17.

[0091] The pixel convertor 17 converts the input video signal based on a predetermined specification input from the A/D converter 16 to a signal having suitable specifications for displaying an image on the liquid crystal panel 18 based on the control parameters of the number of horizontal valid pixels, the number of vertical valid lines, and the number of horizontal dots and vertical lines before starting the signal and outputs the same to the liquid crystal panel 18.

[0092] The liquid crystal panel 18 is a dot matrix type liquid crystal panel and displays the video signal input from the pixel converter 17.

[0093] Next, the operation of the liquid crystal display 10 will be explained all together.

[0094] The synchronization signal of the input video signal input to the synchronization processor 12 is waveform-shaped by the synchronization processor 12 and input to the microcomputer 13.

[0095] The microcomputer 13 detects the horizontal synchronization signal and the vertical synchronization signal from the signal input from the synchronization processor 12 and, based thereon, extracts characteristic information indicating the specifications of the input video signal, such as information of the horizontal frequency, vertical frequency, and polarity of the horizontal/vertical synchronization signals.

[0096] Then, it compares the extracted information with the information of the specifications of video signals for display on the liquid crystal display 10 registered in the signal specification storing ROM 132 and identifies the type of the input video signal.

[0097] When the type of the input video signal is identified, it reads out information regarding the control of the signal from the signal specification storing ROM 132, reads the correction data such as a circuit delay stored in the EEPROM 14, and determines control parameters for the PLL circuit 15 and the pixel converter 17 based on the information and the correction data for controlling them.

[0098] Specifically, it sets a division ratio for the PLL circuit in order to generate a clock corresponding to the dot clock of the input video signal. Also, it sets a parameter regarding pixel conversion for the pixel converter 17 so that the input video signal and the pixels on the liquid crystal panel 18 properly correspond and that the signal is properly converted.

[0099] When the microcomputer 13 cannot identify the type of the input video signal, namely, when the input video signal is a not registered signal, it estimates the number of vertical lines multiplied with by predetermined constant 1.7 as the number of dots in a horizontal period, namely, the dot clock information, uses this to find information regarding the specifications of the image signal successively by a method based on the GTF. Then, it determines control parameters based on this and controls the PLL circuit 15 and the pixel converter 17.

[0100] The video signal input to the liquid crystal display 10 in a state where the PLL circuit 15 and the pixel converter 17 are set in the above way is amplified by a predetermined amplifying rate in the amplifier 11 and is properly sampled in the horizontal direction by a sampling clock synchronized with the dot clock and converted to a digital signal in the A/D converter 16. Then, it is converted to a signal for every pixel in a format suitable for display on the liquid crystal panel 18 and is applied to the liquid crystal panel 18 and displayed based on the input video signal.

[0101] As explained above, in the liquid crystal display 10 of the present embodiment, even if the input video signal is an unknown image signal which is not registered, dot clock information is estimated based on information of the number of vertical lines detectable from the input signal and control parameters for controlling the PLL circuit 15 and the pixel converter 17 are determined based on the estimated value for the control. Accordingly, it is possible to properly control the parts and to properly display the image even for such an unknown image signal.

[0102] Also, since the liquid crystal display 10 is capable of properly displaying such an unknown image signal, it is not necessary to register all image signals and therefore the types of the image signals to be registered can be reduced. Therefore, the capacity of the signal specification storing ROM 132 can be made smaller and it becomes possible to produce a more inexpensive liquid crystal display 10. Furthermore, since it is unnecessary to perform a comparison with a large amount of registered information, processing for identifying the type of the image signal and setting the control parameters can be performed at a high speed and therefore the microcomputer 13 can be substituted by more inexpensive one.

[0103] On the other hand, however, the liquid crystal display 10 has the specifications of the image signals registered in a mask ROM form in the signal specification storing ROM 132 in the microcomputer 13. Therefore, even if the amount

of registered information becomes large, it can be recorded in the microcomputer 13. As a result, it is possible to make the memory cost per bit very low. Also, since high speed accessing is possible, even if the types and information amount of the image signals increase, a video signal can be identified at a high speed.

[0104] Furthermore, fine corrections relating to a circuit delay etc. can be reflected in the control by storing the data in the EEPROM 14, so a better display is guaranteed.

[0105] Note that the present invention is not limited to the above embodiments. A variety of modification can be made.

[0106] For example, in the present embodiment, the number of vertical lines multiplied by 1.7 was estimated as the dot clock value for an unknown video signal, but the constant is not limited to 1.7. When the aspect ratio is 4:3, as explained above with reference to Fig. 1, it is preferable to use a value between 1.6 and 1.85. The constant 1.7 cannot be used for signals having different aspect ratios. However, it is sufficient to use another constant suited to the aspect ratio, thus, it is clear that the case of estimating a dot clock value using such a constant is within the scope of the present invention.

[0107] Also, in the present embodiment, information of a horizontal frequency, vertical frequency, and polarity of horizontal/vertical synchronization signals was extracted from the input image signal and compared with information of specifications of video signals registered in advance so as to identify the type of the input image signal. However, the information used for the comparison is not limited to the information of a horizontal frequency, vertical frequency, and polarity of horizontal/vertical synchronization signals. Any information regarding standards or specifications of the image signal may be used.

[0108] Also, in the liquid crystal display 10, information regarding the specifications of registered video signals was stored in the signal specification storing ROM 132 and the correction data was stored in the EEPROM 14, but the configuration of the memory portion for storing the information and the data is not limited to the above and may be any configuration. For example, all the information and data may be stored in the EEPROM 14.

[0109] Other than the above, the configuration of the microcomputer 13 may be freely modified.

[0110] As explained above, illustrative embodiments of the present invention provide a dot matrix type image display apparatus capable of properly displaying an image even if a non-registered image signal is input can be provided.

Claims

1. An image display apparatus (10), comprising:

a characteristic detection means (13) for detecting from an input image signal predetermined characteristics regarding the specification of the image signal including at least the number of lines in the vertical direction;
an A/D conversion means (16) for successively sampling the signal of every horizontal period of said input image signal using a sampling clock and converting it into a digital image signal;
a signal conversion means (17) for converting said digital image signal to a display signal of a predetermined dot matrix type based on the configuration of a display means; and
a display means (18) of a dot matrix type for displaying the image based on said display signal, **characterised by**
a horizontal pixel number estimation means (13) for multiplying said detected number of lines in the vertical direction with a predetermined constant to calculate an estimated value of the number of horizontal pixels;
and wherein the cycle of the sampling clock is based on the estimated value of the number of the horizontal pixels.

2. An image display apparatus as set forth in claim 1, further comprising:

a memory means for storing information regarding specifications of said image signal including the number of horizontal pixels for each of any plurality of types of image signals and
an image signal identification means for comparing said detected predetermined characteristics with said information of image signals stored in advance to search for the same type of image signal as said input image signal from the plurality of types of image signals whose information is stored in advance; and
wherein said A/D conversion means performs said sampling using a sampling clock based on said information regarding the number of horizontal pixels of the image signals stored in said memory means when an image signal of the same type as said input image signal is found and performs said sampling using a sampling clock based on an estimated value of said calculated number of horizontal pixels when an image signal of the same type as said input image signal is not found.

3. An image display apparatus as set forth in claim 1, wherein said horizontal pixel number estimation means multiplies said detected number of lines in the vertical direction by a predetermined constant between 1.6 to 1.85 when said input image signal is an image signal suitable to a display having an aspect ratio of 4:3,

multiplies said detected number of lines in the vertical direction by a predetermined constant between 1.5 to 1.7 when said input image signal is an image signal suitable to a display having an aspect ratio of 5:4, and
multiplies said detected number of lines in the vertical direction by a predetermined constant between 1.9 to 2.1 when said input image signal is an image signal suitable to a display having an aspect ratio of 16:9 so as to calculate the estimated value of the number of horizontal pixels.

4. An image display apparatus as set forth in claim 3, wherein:

said signal conversion means performs conversion of said digital image signal based on said information regarding the specifications of the image signal stored in said memory means when an image signal of the same type as said input image signal is found and obtains information regarding the specifications of the image signal based on characteristics of said detected input image signal and performs conversion of said digital image signal based on the information when an image signal of the same type as the input image signal is not found.

5. An image display apparatus as set forth in claim 4, wherein said signal conversion means obtains information regarding the specifications of the image signal in accordance with the GTF (generalized timing formula) established by the VESA (Video Electronics Standard Association) based on the characteristics of said detected input image signal when an image signal of the same type as the input image signal is not found.

6. An image display apparatus as set forth in claim 4, wherein said characteristic detection means detects a vertical synchronization signal and a horizontal synchronization signal from said input image signal and counts the number of horizontal synchronization signals included in a vertical synchronization period to obtain said number of lines in the vertical direction.

7. An image display apparatus as set forth in claim 4, wherein said characteristic detection means detects a vertical synchronization signal and a horizontal synchronization signal from said input image signal, finds a horizontal frequency and vertical frequency, and divides the horizontal frequency by the vertical frequency to find the number of lines in the vertical direction.

8. An image display apparatus as set forth in claim 4, wherein said display means is a liquid crystal display means.

9. An image display method comprising the steps of:

detecting from an input image signal predetermined characteristics regarding the specification of the image signal including at least the number of lines in the vertical direction;
successively sampling the signal of every horizontal period of said input image signal using a sampling clock and converting it into a digital image signal;
converting said digital image signal to a display signal of a predetermined dot matrix type based on the configuration of a display means; and
displaying the image based on said display signal on a display means (18) of a dot matrix type, **characterised by** the step of:

multiplying said detected number of lines in the vertical direction with a predetermined constant to calculate an estimated value of the number of horizontal pixels;
and wherein the cycle of the sampling clock is based on the estimated value of the number of the horizontal pixels.

Patentansprüche

1. Bilddarstellungsgerät (10) umfassend:

ein Charakteristik-Detektionsmittel (13) zur Detektion vorbestimmter Charakteristiken eines Eingangsbildsignals betreffend die Spezifikation des Bildsignals einschließlich mindestens der Zahl der Zeilen in vertikaler Richtung;
ein A/D Wandlermittel (16) zur sukzessiven Abtastung des Signals in jeder horizontalen Periode des Eingangssignals unter Verwendung eines Abtasttaktimpulses und zum Umwandeln in ein digitales Bildsignal;
ein Signalumwandlungsmittel (17) zum Umwandeln des digitalen Bildsignals in ein Darstellungssignal, das aus einer Matrix von vorbestimmten Bildpunkten besteht, die ihrerseits auf der Konfiguration eines Darstellungs-

mittels beruht; und
ein Darstellungsmittel (18) eines Bildpunkt-Matrix-Typs zum Darstellen des Bildes, das auf dem Darstellungssignal beruht,
gekennzeichnet durch
ein Horizontal-Pixelzahl-Abschätzungsmittel (13) zum Multiplizieren der detektierten Zahl von Zeilen in vertikaler Richtung mit einer vorbestimmten Konstante, um einen Schätzwert der Zahl der Horizontal-Pixel zu ermitteln; wobei der Zyklus der Abtasttaktimpulse auf dem geschätzten Wert der Zahl der Horizontal- Pixel beruht.

2. Bilddarstellungsgerät gemäß Anspruch 1, weiterhin umfassend:

ein Speichermittel zum Speichern von Spezifikationen des Bildsignals betreffenden Informationen, einschließlich der Zahl der horizontalen Pixel für jeden einer Vielzahl von Bildsignal-Typen und
ein Bildsignalidentifikationsmittel zum Vergleichen der detektierten vorbestimmten Charakteristiken mit der Information von vorher gespeicherten Bildsignalen, um unter der Vielzahl von Typen von Bildsignalen, deren Information vorher gespeichert wurde, nach dem gleichen Typ eines Bildsignals zu suchen, wie es das Eingangsbildsignal ist; wobei
ein A/D Wandlermittel das Abtasten unter Verwendung eines Abtasttaktimpulses bewirkt, der auf der Information beruht, welche die Zahl der Horizontal-Pixel der Bildsignale betreffen, welche in dem Speichermittel gespeichert sind, wenn ein Bildsignal des gleichen Typs wie das Eingangsbildsignal gefunden wird, wobei das Abtasten unter Verwendung eines Abtasttakttimpulses auf dem geschätzten Wert der berechneten Zahl von Horizontal-Pixels beruht, wenn ein Bildsignal des gleichen Typs wie das Eingangsbildsignal nicht gefunden wird.

3. Bitddarstellungsgerät gemäß Anspruch 1, wobei
das Horizontal-Pixelzahl-Abschätzungsmittel
die detektierte Zahl der Zeilen in vertikaler Richtung mit einer vorbestimmten Konstanten zwischen 1,6 und 1,85 multiplizieren, wenn das Eingangsbildsignal ein Bildsignal ist, welches für die Darstellung mit einem Bildseitenverhältnis von 4:3 geeignet ist, und
die detektierte Zahl der Zeilen in vertikaler Richtung mit einer vorbestimmten Konstanten zwischen 1,5 und 1,7 multiplizieren, wenn das Eingangsbildsignal ein Bildsignal ist, das für eine Darstellung mit einem Bildseitenverhältnis von 5:4 geeignet ist, und
die detektierte Zahl von Zeilen in vertikaler Richtung mit einer vorbestimmten Konstanten zwischen 1,9 und 2,1 multiplizieren, wenn das Eingangsbildsignal ein Bildsignal ist, dass zur Darstellung mit einem Bildseitenverhältnis von 16:9 geeignet ist, derart, dass der geschätzte Wert der Horizontal-Pixelzahl ermittelt werden kann.

4. Bilddarstellungsgerät gemäß Anspruch 3, wobei:

das Signalumwandlungsmittel eine Umwandlung des digitalen Bildsignals bewirkt, das auf der Information beruht, die die Spezifikationen des Bildsignals betrifft, welche in dem Speichermittel gespeichert sind, wenn ein Bildsignal des gleichen Typs wie das Eingangsignal gefunden ist, wodurch eine Information über die Spezifikationen des Bildsignals gewonnen wird, das auf Charakteristiken des detektierten Eingangssignals beruht, und wodurch eine Umwandlung des digitalen Bildsignals bewirkt wird, das auf der genannten Information beruht, wenn ein Bildsignal, welches vom gleichen Typ wie das Eingangsbildsignal ist, nicht gefunden wird.

5. Bilddarstellungsgerät nach Anspruch 4, wobei
das Signalumwandlungsmittel eine die Spezifikationen des Bildsignals betreffende Information erzeugt, welche Spezifikationen ihrerseits der von der VESA (Video Electronics Standard Association) eingeführten GTF (generalized timing formula) entsprechen, wobei die genannte Information auf den Charakteristiken des detektierten Eingangsbildsignals beruht, wenn ein Bildsignal, das vom gleichen Typ wie das Eingangsbildsignal ist, nicht gefunden wird.

6. Bilddarstellungsgerät gemäß Anspruch 4, wobei
das Charakteristik-Detektionsmittel ein vertikales Synchronisationssignal und ein horizontales Synchronisationssignal aus dem Eingangsbildsignal detektiert und die Zahl der horizontalen Synchronisationssignale zählt, die in einer vertikalen Synchronisationsperiode enthalten sind, um die Zahl der Zeilen in vertikaler Richtung zu ermitteln.

7. Bilddarstellungsgerät nach Anspruch 4, wobei
das Charakteristik-Detektionsmittel
aus dem Eingangsbildsignal ein vertikales Synchronisationssignal und ein horizontales Synchronisationssignal detektiert,

eine Horizontalfrequenz und eine Vertikalfrequenz ermittelt, und
die Horizontalfrequenz durch die Vertikalfrequenz dividiert, um die Zahl der Zeilen in vertikaler Richtung ermitteln.

8. Bilddarstellungsgerät gemäß Anspruch 4, wobei
das Darstellungsmittel ein Flüssigkristall-Darstellungsmittel ist.

9. Bilddarstellungsverfahren, umfassend folgende Schritte:

Detektieren eines Eingangsbildsignales auf vorbestimmter Charakteristiken, welche die Spezifikation des Bildsignals einschließlich mindestens der Zahl der Zeilen in vertikaler Richtung betreffen;
wiederholtes Abtasten des Eingangsbildsignals in jeder horizontalen Periode unter Verwendung eines Abtasttaktsignals und Umwandeln in ein digitales Bildsignal;
Umwandeln des digitalen Bildsignals in ein Darstellungssignal eines vorbestimmten Matrix-Typs von Punkten, die auf der Konfiguration eines Darstellungsmittels beruht; und
Darstellen des auf dem Bildsignal basierenden Bildes auf einem Darstellungsmittel (18) eines Punktmatrix-Typs, **gekennzeichnet durch** den folgenden Schritt:

Multiplizieren der detektierten Zahl von Zeilen in vertikaler Richtung mit einer vorbestimmten Konstanten, um einen geschätzten Wert der Zahl der Horizontal-Pixel zu ermitteln;
wobei der Zyklus der Abtasttaktimpulse auf dem geschätzten Wert der Zahl der Horizontal-Pixel beruht.

Revendications

1. Appareil d'affichage d'image (10), comprenant :

un moyen de détection de caractéristique (13) pour détecter, à partir d'un signal d'image d'entrée, des caractéristiques prédéterminées concernant la spécification du signal d'image incluant au moins le nombre de lignes suivant la direction verticale ;
un moyen de conversion A/N (16) pour échantillonner en succession le signal de chaque période horizontale dudit signal d'image d'entrée en utilisant une horloge d'échantillonnage et en le convertissant selon un signal d'image numérique ;
un moyen de conversion de signal (17) pour convertir ledit signal d'image numérique selon un signal d'affichage d'un type matrice de points prédéterminé sur la base de la configuration d'un moyen d'affichage ; et
un moyen d'affichage (18) d'un type matrice de points pour afficher l'image sur la base dudit signal d'affichage, **caractérisé par** :

un moyen d'estimation de nombre de pixels horizontaux (13) pour multiplier ledit nombre de lignes détectées suivant la direction verticale par une constante prédéterminée afin de calculer une valeur estimée du nombre de pixels horizontaux ; et dans lequel
le cycle de l'horloge d'échantillonnage est basé sur la valeur estimée du nombre des pixels horizontaux.

2. Appareil d'affichage d'image selon la revendication 1, comprenant en outre :

un moyen de mémoire pour stocker une information concernant des spécifications dudit signal d'image incluant le nombre de pixels horizontaux pour chacun d'une quelconque pluralité de types de signaux d'image ; et
un moyen d'identification de signal d'image pour comparer lesdites caractéristiques prédéterminées détectées avec ladite information de signaux d'image stockée à l'avance pour rechercher le même type de signal d'image que ledit signal d'image d'entrée à partir de la pluralité de types de signaux d'image dont l'information est stockée à l'avance ; et dans lequel
ledit moyen de conversion A/N réalise ledit échantillonnage en utilisant une horloge d'échantillonnage sur la base de ladite information concernant le nombre de pixels horizontaux des signaux d'image stockés dans ledit moyen de mémoire lorsqu'un signal d'image du même type que ledit signal d'image d'entrée est trouvé et réalise ledit échantillonnage en utilisant une horloge d'échantillonnage sur la base d'une valeur estimée dudit nombre calculé de pixels horizontaux lorsqu'un signal d'image du même type que ledit signal d'image d'entrée n'est pas trouvé.

3. Appareil d'affichage d'image selon la revendication 1, dans lequel ledit moyen d'estimation de nombre de pixels

horizontaux multiplie ledit nombre détecté de lignes suivant la direction verticale par une constante prédéterminée entre 1,6 et 1,85 lorsque ledit signal d'image d'entrée est un signal d'image qui convient pour un affichage présentant un rapport d'aspect de 4:3, multiplie ledit nombre détecté de lignes suivant la direction verticale par une constante prédéterminée entre 1,5 et 1,7 lorsque ledit signal d'image d'entrée est un signal d'image qui convient pour un affichage présentant un rapport d'aspect de 5:4 et multiplie ledit nombre détecté de lignes suivant la direction verticale par une constante prédéterminée entre 1,9 et 2,1 lorsque ledit signal d'image d'entrée est un signal d'image qui convient pour un affichage présentant un rapport d'aspect de 16:9 de manière à calculer la valeur estimée du nombre de pixels horizontaux.

4. Appareil d'affichage d'image selon la revendication 3, dans lequel :

ledit moyen de conversion de signal réalise une conversion dudit signal d'image numérique sur la base de ladite information concernant les spécifications du signal d'image stockée dans ledit moyen de mémoire lorsqu'un signal d'image du même type que ledit signal d'image d'entrée est trouvé et obtient une information concernant les spécifications du signal d'image sur la base de caractéristiques dudit signal d'image d'entrée détecté et réalise une conversion dudit signal d'image numérique sur la base de l'information lorsqu'un signal d'image du même type que le signal d'image d'entrée n'est pas trouvé.

5. Appareil d'affichage d'image selon la revendication 4, dans lequel ledit moyen de conversion de signal obtient une information concernant les spécifications du signal d'image conformément à la GTF (formule de cadencement généralisée) établie par la VESA (Association de Standards Electroniques Vidéo) sur la base des caractéristiques dudit signal d'image d'entrée détecté lorsqu'un signal d'image du même type que le signal d'image d'entrée n'est pas trouvé.

6. Appareil d'affichage d'image selon la revendication 4, dans lequel ledit moyen de détection de caractéristique détecte un signal de synchronisation verticale et un signal de synchronisation horizontale à partir dudit signal d'image d'entrée et compte le nombre de signaux de synchronisation horizontale inclus dans une période de synchronisation verticale pour obtenir ledit nombre de lignes suivant la direction verticale.

7. Appareil d'affichage d'image selon la revendication 4, dans lequel ledit moyen de détection de caractéristique détecte un signal de synchronisation verticale et un signal de synchronisation horizontale à partir dudit signal d'image d'entrée, trouve une fréquence horizontale et une fréquence verticale et divise la fréquence horizontale par la fréquence verticale pour trouver le nombre de lignes suivant la direction verticale.

8. Appareil d'affichage d'image selon la revendication 4, dans lequel ledit moyen d'affichage est un moyen d'affichage à cristaux liquides.

9. Procédé d'affichage d'image comprenant les étapes de :

détection, à partir d'un signal d'image d'entrée, de caractéristiques prédéterminées concernant la spécification du signal d'image incluant au moins le nombre de lignes suivant la direction verticale ;
échantillonnage en succession du signal de chaque période horizontale dudit signal d'image d'entrée en utilisant une horloge d'échantillonnage et sa conversion selon un signal d'image numérique ;
conversion dudit signal d'image numérique selon un signal d'affichage d'un type matrice de points prédéterminé sur la base de la configuration d'un moyen d'affichage ; et
affichage de l'image sur la base dudit signal d'affichage sur un moyen d'affichage (18) d'un type matrice de points, **caractérisé par** l'étape de :

multiplication dudit nombre de lignes détectées suivant la direction verticale par une constante prédéterminée afin de calculer une valeur estimée du nombre de pixels horizontaux ; et
dans lequel le cycle de l'horloge d'échantillonnage est basé sur la valeur estimée du nombre de pixels horizontaux.

FIG. 1

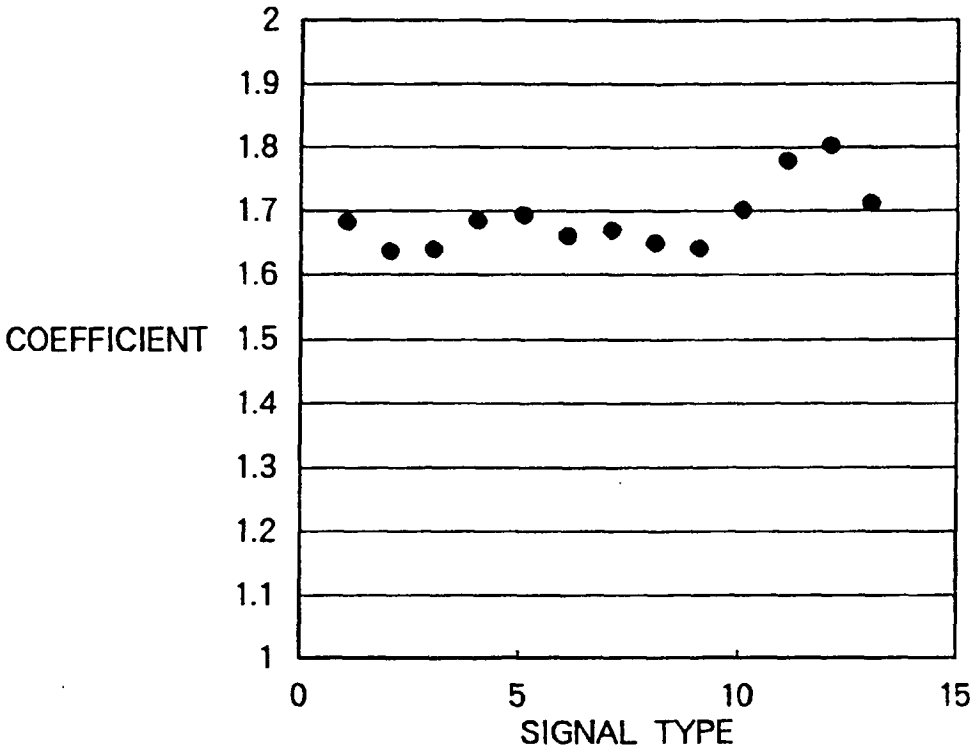


FIG. 2

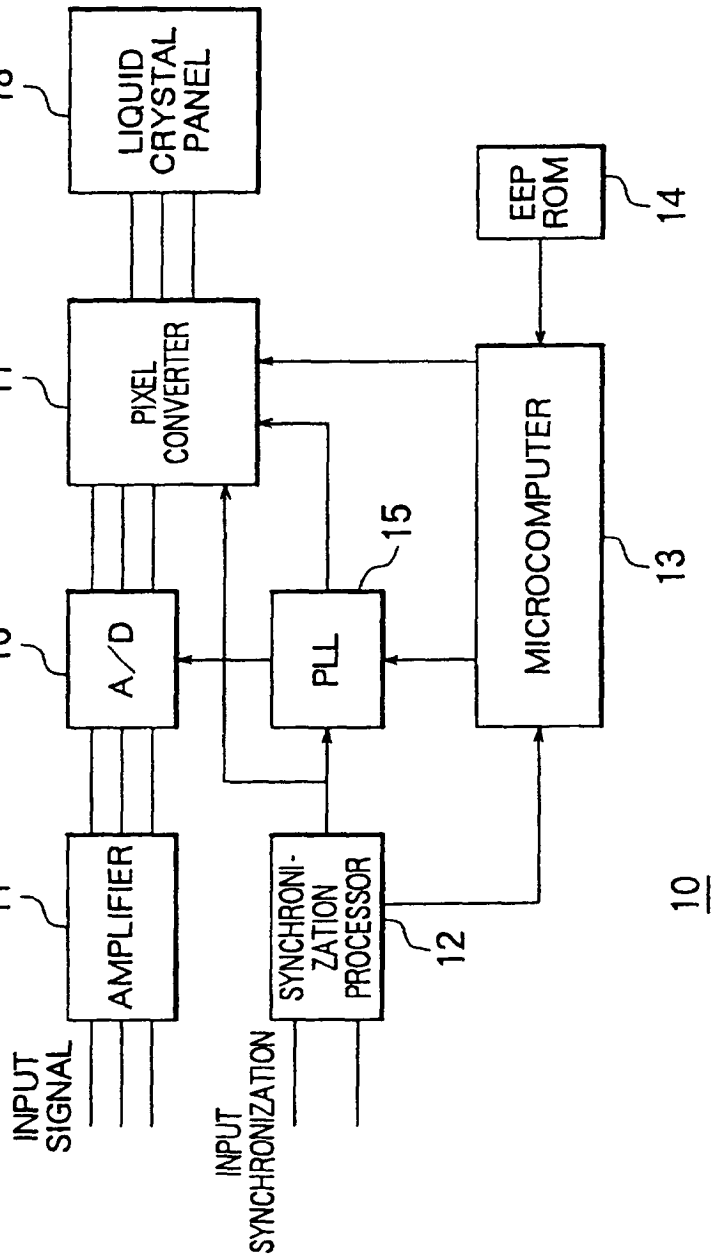

LIQUID CRYSTAL PANEL
18
EEP ROM
14
PIXEL CONVERTER
17
MICROCOMPUTER
13
15
A/D
16
PLL
AMPLIFIER
11
SYNCHRONI-ZATION PROCESSOR
12
10
INPUT SIGNAL
INPUT SYNCHRONIZATION

FIG. 3

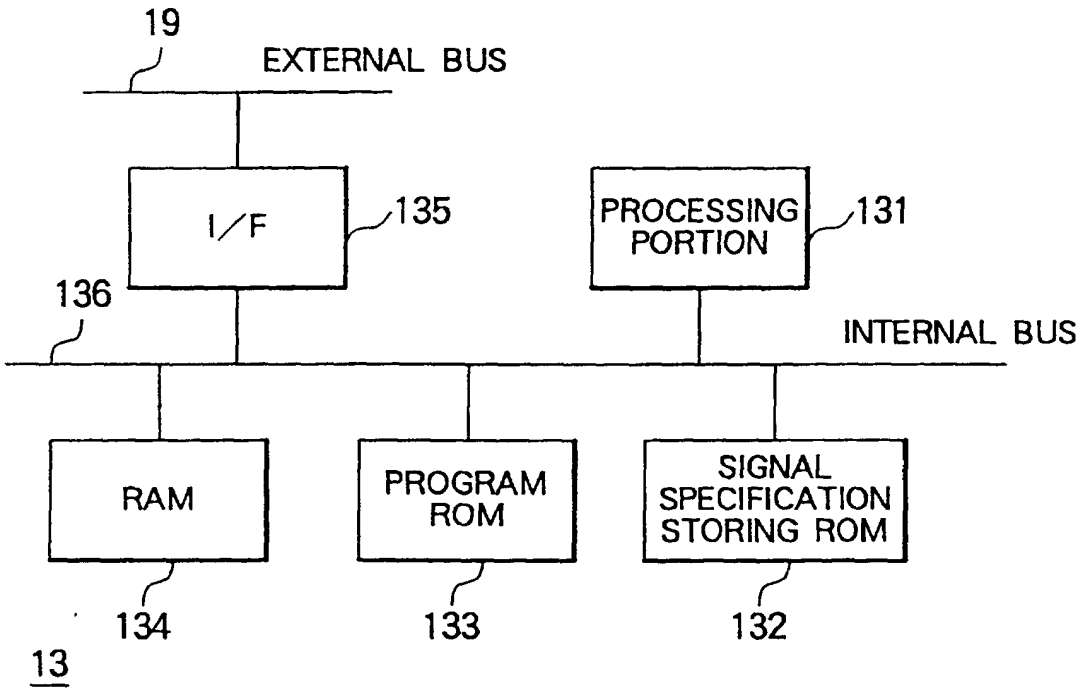
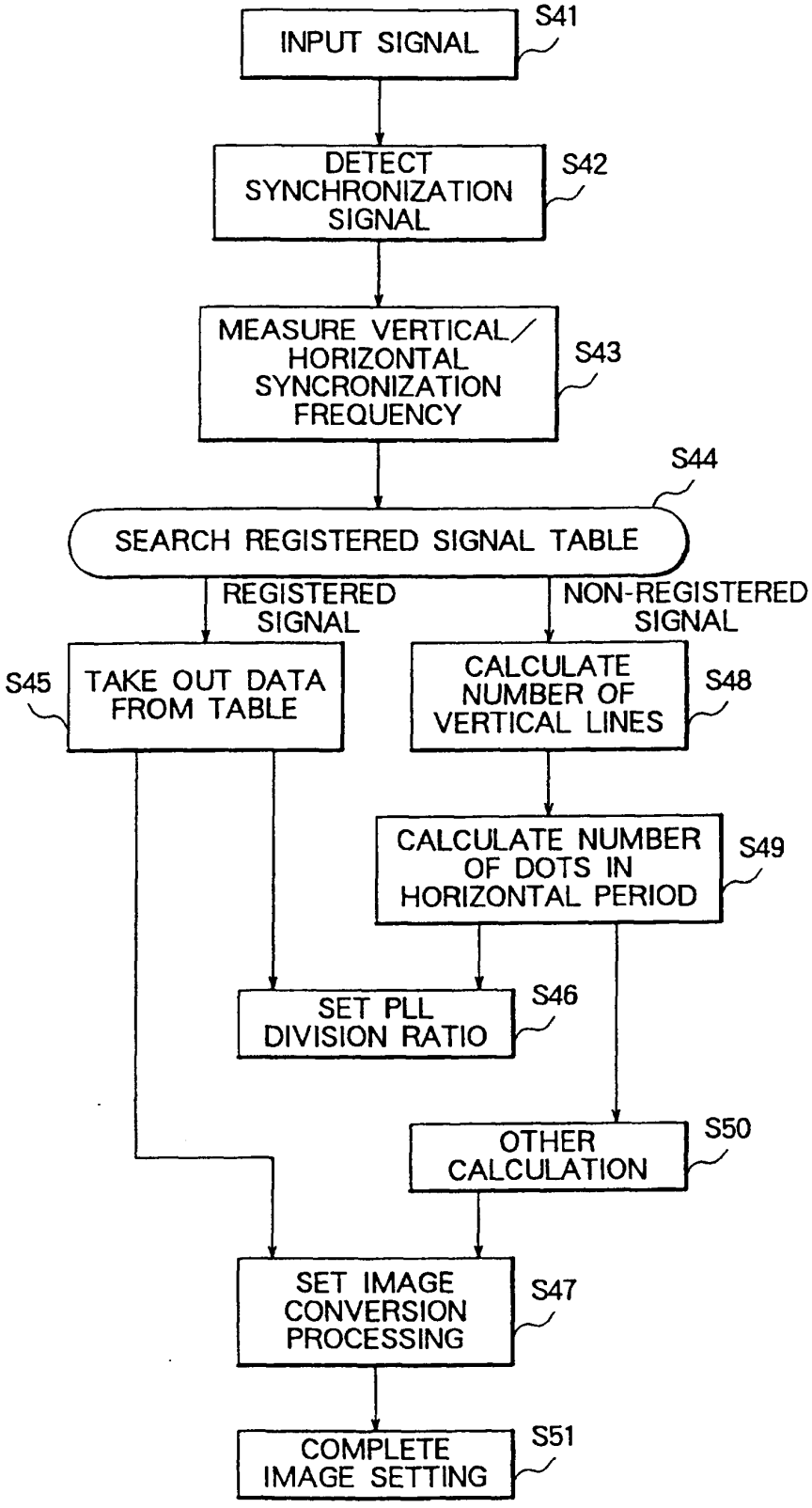

19
EXTERNAL BUS
I/F
135
PROCESSING PORTION
131
136
INTERNAL BUS
RAM
PROGRAM ROM
SIGNAL SPECIFICATION STORING ROM
134
133
132
13

FIG. 4


INPUT SIGNAL
S41
DETECT SYNCHRONIZATION SIGNAL
S42
MEASURE VERTICAL/HORIZONTAL SYNCRONIZATION FREQUENCY
S43
S44
SEARCH REGISTERED SIGNAL TABLE
REGISTERED SIGNAL
NON-REGISTERED SIGNAL
S45
TAKE OUT DATA FROM TABLE
CALCULATE NUMBER OF VERTICAL LINES
S48
CALCULATE NUMBER OF DOTS IN HORIZONTAL PERIOD
S49
SET PLL DIVISION RATIO
S46
OTHER CALCULATION
S50
SET IMAGE CONVERSION PROCESSING
S47
COMPLETE IMAGE SETTING
S51

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- EP 0854466 A **[0016]**

专利名称(译)	具有输入视频信号转换的图像显示设备		
公开(公告)号	EP1047043B1	公开(公告)日	2007-07-18
申请号	EP2000302974	申请日	2000-04-07
[标]申请(专利权)人(译)	索尼公司		
申请(专利权)人(译)	索尼公司		
当前申请(专利权)人(译)	索尼公司		
[标]发明人	MURAYAMA HIROSHI FUJIMOTO TADASHI		
发明人	MURAYAMA, HIROSHI FUJIMOTO, TADASHI		
IPC分类号	G09G3/36 G09G3/20 H04N5/66 G09G5/00 G09G5/36		
CPC分类号	G09G5/008 G09G3/3611		
优先权	1999111098 1999-04-19 JP		
其他公开文献	EP1047043A3 EP1047043A2		
外部链接	Espacenet		

摘要(译)

输入视频信号的同步信号通过同步处理器12输入到微计算机13.检测水平和垂直频率以及同步信号的极性，并与ROM中登记的视频信号的规格信息进行比较，并且识别输入视频信号。当识别时，进一步从ROM读取诸如点时钟的指定信息，而当未识别时，从同步信号获得垂直线的数量并乘以1.7并将结果视为点时钟。此外，使用广义时序公式计算指定信息。根据通过上述方法获得的规范信息，控制PLL电路15和视频信号转换器17。输入视频信号在放大器11中被放大，通过在A / D转换器16中的适当采样被转换成数字信号，被转换成适合于在视频信号转换器17中的液晶面板18上显示的信号，并被提供。液晶面板18。

[Formula 1]

$$\text{Dot clocks/Division ratio} = \text{Horizontal frequency} \quad \ldots(1)$$