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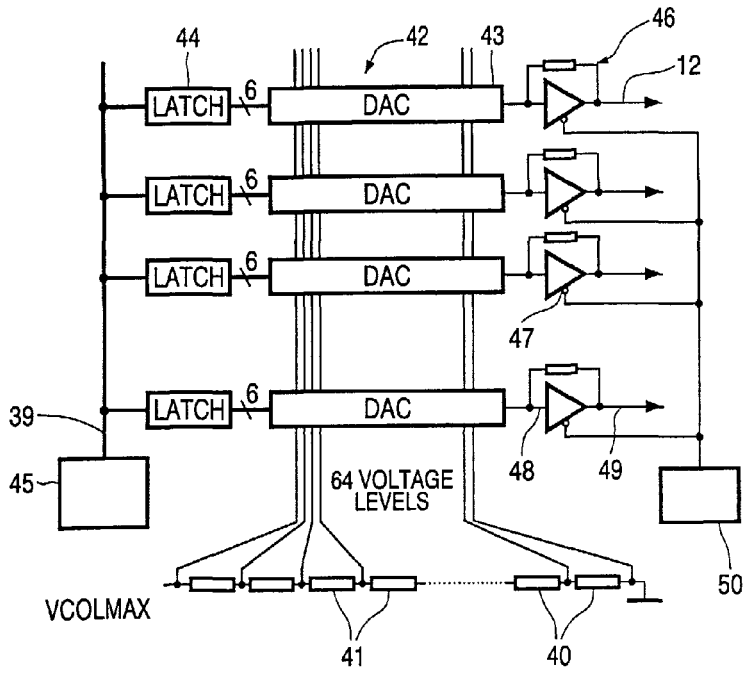
(54) Title: COLUMN DRIVER FOR LIQUID CRYSTAL DISPLAY



(57) Abstract: A liquid crystal display has a plurality of buffers 46 controlling a plurality of column lines. The buffers have a bias current control input 47 which is controlled, in the example by timing circuitry 50, to set the current during the row period for writing to each row of pixels. In particular, the row period may be divided between a drive period with a high buffer bias current and a voltage maintenance period with a lower buffer bias current.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DESCRIPTION

COLUMN DRIVER FOR LIQUID CRYSTAL DISPLAY

The invention relates to a liquid crystal display, a driver for a liquid crystal display and a method of driving a liquid crystal display.

Active matrix display devices typically comprise an array of pixels arranged in rows and columns. Each row of pixels shares a row conductor which connects to the gates of the thin film transistors of the pixels in the row. Each column of pixels shares a column conductor, to which pixel drive signals are provided. The signal on the row conductor determines whether the transistor is turned on or off, and when the transistor is turned on, by a high voltage pulse on the row conductor, a signal from the column conductor is allowed to pass on to an area of liquid crystal material, thereby altering the light transmission characteristics of the material. An additional storage capacitor may be provided as part of the pixel configuration to enable a voltage to be maintained on the liquid crystal material even after removal of the row electrode pulse. US-A-5 130 829 discloses in more detail the design of an active matrix display device.

The frame (field) period for active matrix display devices requires a row of pixels to be addressed in a short period of time, and this in turn imposes a requirement on the current driving capabilities of the transistor in order to charge or discharge the liquid crystal material to the desired voltage level. In order to meet these current requirements, the gate voltage supplied to the thin film transistor needs to fluctuate between values separated by approximately 30 volts. For example, the transistor may be turned off by applying a gate voltage of around -10 volts, or even lower, (with respect to the source) whereas a voltage of around 20 volts, or even higher, may be required to bias the transistor sufficiently to provide the required source-drain current to charge or discharge the liquid crystal material sufficiently rapidly.

The requirement for large voltage swings in the row conductors requires the row driver circuitry to be implemented using high voltage components.

The voltages provided on the column conductors typically vary by approximately 10 volts, which represents the difference between the drive signals required to drive the liquid crystal material between white and black states. Various drive schemes have been proposed enabling the voltage swing on the column conductors to be reduced, so that lower voltage components may be used in the column driver circuitry. In the so-called "common electrode drive scheme", the common electrode, connected to the full liquid crystal material layer, is driven to an oscillating voltage. The so-called "four-level drive scheme" uses more complicated row electrode waveforms in order to reduce the voltage swing on the column conductors, using capacitive coupling effects.

These drive schemes enable lower voltage components to be used for the column driver circuitry. However, there is still a significant amount of complexity and power inefficiency in the column driver circuits. Each row is addressed in turn, and during the row address period of any one row, pixel signals are provided to each column. In conventional designs each column is provided with a buffer for holding a pixel in the column to a drive signal level for the full duration of the row address period.

A difficulty is that the power needed to drive the buffers may be inconveniently large, especially for low power, battery driven applications. Typically, even when not driving a line, each buffer might have a power requirement of 3.5mW or more. This power requirement is known as the quiescent power requirement and may be distinguished from the further power required when the buffer charges the lines. The number of column lines required to drive display screens is large, and so the number of buffers needed may need to be large as well. Thus the total quiescent power requirement in prior designs may easily be too large for portable battery driven applications. It is possible to redesign buffers with a lower quiescent power requirement, but such redesign generally also lowers the ability of the buffers to deliver sufficient current to quickly charge up the column lines.

Thus, it would be generally desirable to reduce the power required to be drawn by the buffers.

According to the invention there is provided a liquid crystal display having a plurality of liquid crystal pixel electrodes arranged as an array of rows and columns; a plurality of row and column lines for driving the liquid crystal pixel electrodes; a plurality of buffers for driving the plurality of column lines, the buffers being operable at a variety of bias currents; and means for varying the buffer bias currents during a plurality of row periods, the row periods being periods for writing to a row of pixel electrodes, whilst maintaining the voltage output to provide different bias currents at different times within individual row periods.

By varying the bias current of each buffer at different times during the charging of each line, it is possible to reduce the total power consumption of the buffer, whilst still providing sufficient current to switch the column lines in the time available.

Since the capacitance of individual column lines is greater than that of individual pixel electrodes much more power is needed to charge the column lines to the required voltage than is required subsequently to maintain the voltage at the required voltage in order to charge up the pixel. Furthermore, suitable buffer amplifiers are available that have a variable current sourcing capability by varying the bias current and thus the quiescent power.

Accordingly, by varying the bias current of the buffer amplifiers to first charge up the column lines using a higher bias current and later to maintain the column lines at a given voltage using a lower bias current whilst still maintaining the voltage on the column line the amplifiers may have a considerably lower power requirement averaged over each frame than in prior arrangements.

It should be noted that the buffer bias current is not the complete current drawn by the buffer, which generally is drawn from the power supply, but varying the buffer bias current does change the ability of the buffer to source large currents.

In embodiments, the means for varying the buffer bias currents includes timing circuitry for dividing each row period into a drive period and a voltage maintenance period and controlling the buffers to use a higher bias current during a first part of the row period to charge the column lines and to use a lower bias current during a second part of the row period to maintain the voltage on the column lines.

In preferred embodiments, the period for writing each frame is divided into an addressing phase or phases including all of the row periods and a power down phase in which the buffers are inactive. It will be appreciated that this saves power, since the buffers are inactive for part of the frame time. Of course, the pixels need to be addressed more quickly than otherwise but this is achieved by the approach of the invention of varying the buffer bias current to be initially high to allow fast charging of the column lines and then lower to avoid excessive power consumption. Thus, in these preferred embodiments the buffer bias current is initially high, and then lowers whilst maintaining the voltage on the line. There is a further phase during which the buffers are substantially switched off. The further phase may for example take place after all the rows of the display have been written to, or may be a plurality of short pauses interspersed between writing to different rows.

The invention also consists of a method of operating a liquid crystal display having a plurality of rows and columns of pixel electrodes, the method comprising: converting a sequence of digital signals representing

a series of image frames into a sequence of voltage levels for driving the column lines; driving the plurality of column lines from a plurality of buffers operable at a variety of bias currents during a plurality of row periods for charging each successive row of pixel electrodes; and varying the buffer bias currents during each row period to provide different bias currents at different times within individual row periods.

The invention also relates to a column driver for driving a liquid crystal display as set out above.

Specific embodiments of the invention will now be described, purely by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a liquid crystal display according to a first embodiment of the invention;

Figure 2 shows a single pixel of the liquid crystal display of Figure 1;

Figure 3 is an equivalent electrical circuit diagram of the drive of a pixel of the first embodiment;

Figure 4 shows the column drive circuitry used in the first embodiment;

Figure 5 shows the buffer bias currents as a function of time in the first embodiment;

Figure 6 shows alternative sub-divisions of the frame time;

Figure 7 shows an alternative column drive circuit according to a second embodiment;

Figure 8 shows a buffer circuit used in the second embodiment; and

Figure 9 shows the buffer current as a function of time in the second embodiment.

It should be noted that the drawings are schematic and not to scale.

Figures 1 to 4 shows a pixel configuration for an active matrix liquid crystal display. The display is arranged as an array of pixels 2 in rows and columns. Each row of pixels shares a common row conductor 10, and each column of pixels shares a common column conductor 12. The row address signals are provided by row driver circuitry 30, and the pixel drive signals are provided by column address circuitry 32, to the array 34 of display pixels.

In order to enable a sufficient current to be driven through the thin film transistor 14, which is implemented as an amorphous silicon thin film device, a high gate voltage must be used. In particular, the period during which the transistor is turned on is approximately equal to the total frame period within which the display must be refreshed, divided by the number of rows. It is well known that the gate voltage for the on-state and the off-state differ by approximately 30 volts in order to provide the required small leakage current in the off-state, and sufficient current flow in the on-state to charge or discharge

the liquid crystal cell 16 within the available time. As a result, the row driver circuitry 30 uses high voltage components.

As shown in Figure 2, each pixel comprises a thin film transistor 14 and a liquid crystal the column conductor 12. The transistor 14 is switched on and off by a signal provided on the row conductor 10. The row conductor 10 is thus connected to the gate 14a of each transistor 14 of the associated row of pixels. Each pixel may additionally comprise a storage capacitor 20 which is connected at one end to the next row electrode, to the preceding row electrode, or to a separate capacitor electrode 22. This capacitor 20 helps to maintain the drive voltage across the liquid crystal cell 16 after the transistor 14 has been turned off. A higher total pixel capacitance is also desirable to reduce various effects, such as kickback, and to reduce the grey-level dependence of the pixel capacitance.

Figure 3 shows the equivalent circuit of the connection between the column driver 23 (which essentially comprises a voltage source 24 and a switch having resistance 25) and the pixel of the column in the selected row. The column has a column capacitance 26, which results, for example, from all of the crossovers of the column with the row conductors. The individual pixel has a pixel capacitance 27 made up of the capacitance of the pixel electrode 16 and the storage capacitor 20.

Figure 4 shows the column driver circuit for use in the first embodiment of the invention. The number n of different pixel drive signal levels are generated by a grey level generator 40, for example a resistor array including a plurality of resistors 41 arranged in series as shown. A switching matrix 42 controls the switching of the required level to each column and comprises an array of converters 43, each converter corresponding to one column line 12, for selecting one of the n grey levels based on a digital input from a latch 44. The digital input is derived from a RAM storing the required image data 45 through data input 39.

Each column line 12 is provided with a buffer 46, each of which has a bias current control input 47, a signal input 48 and a signal output 49. The signal input 48 is connected to the output from the corresponding converter 43,

the signal output 49 drives the respective column, and the bias current control input 47 is connected to a timing circuit 50, the function of which will be explained in more detail below.

The bias current control input 47 controls the bias current drawn by the buffer. The buffer 46 is capable of driving its output 49 to a voltage determined by the voltage on the signal input 48 using a variety of different bias currents. The current sourcing capability of the buffer 46 varies as a function of the bias current. Buffers having an adjustable bias current are well known in the art and will not be described further.

In use, in order to drive the liquid crystal cell 16 to a desired voltage to obtain a required grey level, an appropriate signal is provided on the column conductor 12 in synchronism with a row address pulse on the row conductor 10. This row address pulse turns on the thin film transistor 14, thereby allowing the column conductor 12 to charge the pixel electrode 16 to the desired voltage, and also to charge the storage capacitor 20 to the same voltage. The column drive signal results in charging of both capacitances 26 and 27. However the time constant for charging the column capacitor 26 (resistance 25 x capacitance 26) is much lower than the time constant for charging the pixel (TFT resistance x capacitance 27). Thus, a short column address pulse is required to charge the column capacitance 26.

After the column address pulse, but while the row address pulse is still active, there is charge transfer between the column capacitance 26 and the pixel capacitance 27, until an equilibrium is reached. The pixel capacitance is much smaller than the column capacitance, so that the equilibrium is reached with little change in the column voltage. The large time constant of the pixel results from the high TFT resistance. At the end of the row address pulse, the transistor 14 is turned off. The storage capacitor 20 reduces the effect of liquid crystal leakage and reduces the percentage variation in the pixel capacitance caused by the voltage dependency of the liquid crystal cell capacitance. The rows are addressed sequentially so that all rows are addressed in one frame period, and refreshed in subsequent field periods. The timing circuit 50 controls the buffer bias current of the buffers 46 by inputting a signal on the

control input 47 of each of the buffers. The signal may be the bias current itself. However, in the preferred embodiment shown the signal is a voltage that controls the current drawn by the buffers in order that small variations of the input impedance of the bias current control input 47 between different buffers 46 do not cause excessive variation in the bias current drawn by the different buffers.

Figure 5 illustrates the timing of the buffer bias currents. The image frame period 52, i.e. the period for each successive frame of the image, is divided into a plurality of line periods 54 for charging up the pixel capacitances 27 of successive rows of pixels. It will be appreciated that once the pixel capacitances 27 of each row have been charged to a level corresponding to the required grey level, each pixel capacitance 27 will retain its charge until it is rewritten in the next frame period 52, thereby retaining the image state of the corresponding pixels.

Each line period 54 is further subdivided into a drive phase 56 and a voltage maintenance phase 58. During the drive phase 56, a higher bias current is used for the buffers and during the voltage maintenance 58 a lower bias current is used. During the drive phase 56, the higher buffer bias current ensures that the buffers 46 are capable of supplying sufficient current to charge up the corresponding column lines 12. After the drive phase 56 is over, during the voltage maintenance phase 58, a much lower buffer bias current is used that can keep the column line 12 at the required voltage without drawing excessive current.

Consider the example of a display designed for a maximum refresh rate of 60Hz and 240 rows. The line time is given by dividing the time for one frame by the number of rows. Thus, in the example the line period is approximately 70μs, of which 17μs is the drive phase 56 and 53μs is the voltage maintenance phase 58.

By driving the buffers 46 with a high bias current in the drive phase 56 and a much lesser current during the voltage maintenance phase 58 the average power taken by the buffers is reduced whilst still maintaining the ability to rapidly charge the column lines during the drive phase 56. In this

phase the high bias current ensures that the buffers 46 are capable of delivering sufficient current to rapidly charge up the column lines 12.

An alternative, and generally preferred, division of the frame period is illustrated in Figure 6. This approach may be implemented by circuitry as shown in Figures 1 to 4, the only difference being that the timing circuitry 50 is arranged to provide timing signals as detailed below.

The frame period 52 is subdivided into an addressing phase 60 and a power down phase 62. The addressing phase 60 includes both the drive phase 56 and the voltage maintenance phase 58; during the power down phase the buffers 46 are essentially switched off. The examples shown in Figure 6 are for the same case of a 240 line display for operation at up to 60Hz, as above.

Figure 6 illustrates two ways in which the frame period, T_F, can be subdivided into addressing phase 60, AP, and power down phase 62, PDP, in which the buffer bias current is very low. Figure 6a shows the frame period T_F subdivided into an initial addressing phase 60 of 4.8ms followed by a power down phase of 16.8ms. The initial addressing phase 60 includes 240 sequential line periods 54 of 20μs, each line period for addressing a different row of pixels. As in the example of Figure 5, each line period 54 is divided into an initial drive phase 56 followed by a voltage maintenance phase. The drive phase 56 lasts 5μs and the voltage maintenance phase 58 lasts 15μs.

In the example of Figure 6b, an alternative approach is used in which each line period 54, T_L, of 70μs is subdivided into an addressing phase, AP, 60 of 20μs followed by a power down phase, PDP, 62 of 50μs, In which the buffer bias current is very low and the pixel is not addressed. The line period 54 is subdivided in the same manner as above into an initial drive phase 56 of 5μs followed by a voltage maintenance phase 58 of 15μs.

During the 5μs initial drive phase 56 the bias current for each buffer is 3.6μA which is sufficient bias current to allow the buffer to quickly charge the column to the desired voltage. This time is however too short to allow the selected pixel capacitance to fully charge through the TFT 14. Thus, the

voltage maintenance phase 58 is used to allow the pixel capacitance 27 to charge through the TFT 14. During this time the bias current is reduced to a low value of 0.4μA which allows the buffer to stay stable and to keep the column fully charged if there are any leakages. The buffer is still of low impedance even with this reduced bias current.

The average bias current during the addressing phase is 1.2 μA, which corresponds to a power of 6.6μW per buffer from a 5.5V power line. The total power during the addressing phase is thus 3.5mW. Averaged over the complete frame time, the resulting power consumption is thus 1mW, an excellent result.

The use of a power down phase requires that the addressing takes place more quickly than would otherwise be the case. This increase in speed of addressing is made possible by dividing the addressing phase into a plurality of line driving periods and dividing the line driving periods into a drive phase 56 with a high bias current and a voltage maintenance phase 58 with a lower bias current. It should be noted that if the average bias current of 1.2 μA were used throughout the addressing phase 60 rather than subdividing the addressing phase into drive phase 56 and voltage maintenance phase 58 the level of current would probably be too slow to charge the column effectively and rapidly.

The invention is not limited to operation with the hardware architecture illustrated above in Figures 1 to 4. Figure 7 illustrates an alternative architecture which uses one buffer 46 per grey level. In this approach, instead of having one buffer 46 for each column line 12, there is one buffer 46 for each grey level. When a pixel and hence a column is required to have a given grey level the column is simply connected by respective converter 43 to the appropriate buffer 46. The digital input is derived from a RAM 45 storing the required image data which is piped to the latches.

This scheme reduces the total number of buffers to 64 for a six-bit grey scale approach. A further benefit is that the matching of different buffers becomes much less critical than in the architecture of Figure 4.

Again the biasing of the buffer may be varied during the frame. The buffer bias current is initially high and then reduced to maintain the voltage on the column lines 12 without using excessive power.

There are a number of possibilities for coping with the variable load on the buffers 46 depending on the number of column lines 12 connected to each of the buffers. One approach is to use adaptive biasing buffer circuits in which the buffer bias current varies in a controlled fashion. This is illustrated schematically in Figure 8. A control circuit 80 senses the difference between the input and output voltages and also senses the rate of chance of the input voltage. The control circuit then adapts the buffer bias current depending on these parameters. The higher the rate of change of the input voltage, and the greater the difference between input and output voltages, the higher the buffer bias current. The control circuit 80 thus operates as a conventional PID (proportional-integral-differential) controller, although for simplicity the control circuit 80 may avoid any integral term.

Suitable adaptive bias circuits are known, for example from Degrauwe et al "Adaptive Biasing CMOS Amplifiers" IEEE Journal of Solid-State Circuits, Vol SC-17, No 3, June 1982, starting at page 522, and accordingly will not be described further.

Figure 9 illustrates the output as a function of time for a variety of different numbers of columns connected to a buffer. Curve 90 shows the buffer output current, BC, for a single column connected to the buffer, curve 92 for two columns connected to the buffer, and curve 94 for three columns connected to the buffer. V_C is the column voltage and V_P is the pixel voltage. As may be seen from inspection of the curves, the buffer bias current is controlled to be initially large and then reduce to quickly charge up the columns and then maintain the charge. The larger the number of columns connected to a buffer, the larger the initial size of the buffer bias current. The bias current is controlled such that the column voltages are as shown in curve 96 and the pixel voltages accordingly as shown in curve 98.

Instead of automatically sensing the load using control circuit 80, alternative embodiments of the invention may program the control circuit 80 to

control the bias current of the different buffers based on the information taken from the memory 45.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the design, manufacture and use of semiconductor devices and which may be used in addition to or instead of features described herein.

CLAIMS

1. A liquid crystal display comprising:

a plurality of liquid crystal pixel electrodes arranged as an array of rows and columns;

a plurality of row and column lines for driving the liquid crystal pixel electrodes;

a plurality of buffers for driving the plurality of column lines, the buffers being operable at a variety of bias currents; and

means for varying the buffer bias currents during a plurality of row periods, the row periods being periods for writing to a row of pixel electrodes, whilst maintaining the voltage output to provide different bias currents at different times within individual row periods.

2. A liquid crystal display according to claim 1 wherein the buffers include bias current control inputs and the means for varying the buffer bias currents comprises timing circuitry connected to the bias current control inputs for dividing each row period into a drive period and a voltage maintenance period and controlling the buffers to use a higher bias current during the drive period to charge the column lines and to use a lower bias current during the voltage maintenance period to maintain the voltage on the column lines.

3. A liquid crystal display according to claim 2 wherein the timing circuitry controls the buffers to have an addressing phase or phases including all of the row periods and a power down phase in which the buffers are inactive.

4. A liquid crystal display according to any preceding claim wherein the buffers each have a bias current control input for controlling the bias current.

5. A liquid crystal display according to any preceding claim wherein each buffer has a signal input and output, the output being connected to drive a

respective column line and the signal input being connected to a digital to analogue conversion means.

6. A liquid crystal display according to claim 5 further comprising a voltage source having a plurality of outputs supplying a respective plurality of voltage levels, wherein the digital to analogue conversion means is a switch matrix for connecting the signal input of each of the buffers to the one of the plurality of outputs of the voltage source having a voltage level corresponding to the input digital signal.

7. A liquid crystal display according to any of claims 1 to 4 wherein the plurality of buffers output a plurality of predetermined voltage levels and further comprising a switch matrix acting as a digital to analogue converter between the plurality of buffers and the plurality of column lines.

8. A method of operating a liquid crystal display having a plurality of rows and columns of pixel electrodes driven by row and column lines, the method comprising:

converting a sequence of digital signals representing a series of image frames into a sequence of voltage levels for driving the column lines;

driving the plurality of column lines from a plurality of buffers operable at a variety of bias currents during a plurality of row periods, the row periods being periods for charging each successive row of pixel electrodes; and

varying the buffer bias currents during each row period to provide different bias currents at different times within individual row periods.

9. A method according to claim 8 including dividing each row period into a drive period and a voltage maintenance period and controlling the buffer to use a higher bias current during the drive period and to use a lower bias current during the voltage maintenance period.

10. A method according to claim 8 or 9 wherein the period for writing each frame is divided into an addressing phase or phases including all of the row periods and a power down phase or phases in which the buffers are switched off.

11. A liquid crystal display driver comprising:

a digital input for accepting a sequence of digital signals representing a series of image frames;

digital to analogue conversion means for converting the sequence of digital signals on the digital input and outputting corresponding voltage levels;

a plurality of buffers for driving a plurality of column lines of the liquid crystal display during a plurality of row periods for writing to each row of pixel electrodes, the buffers being operable at a variety of bias currents; and

means for varying the buffer bias currents whilst maintaining the voltage output to provide different bias currents at different times within individual row periods.

12. A liquid crystal display driver according to claim 11 wherein the means for varying the buffer bias currents comprises timing circuitry for dividing each row period into a drive period and a voltage maintenance period and controlling the buffers to use a higher bias current during the drive period to charge the column lines using a higher bias current and to use a lower bias current during the voltage maintenance period.

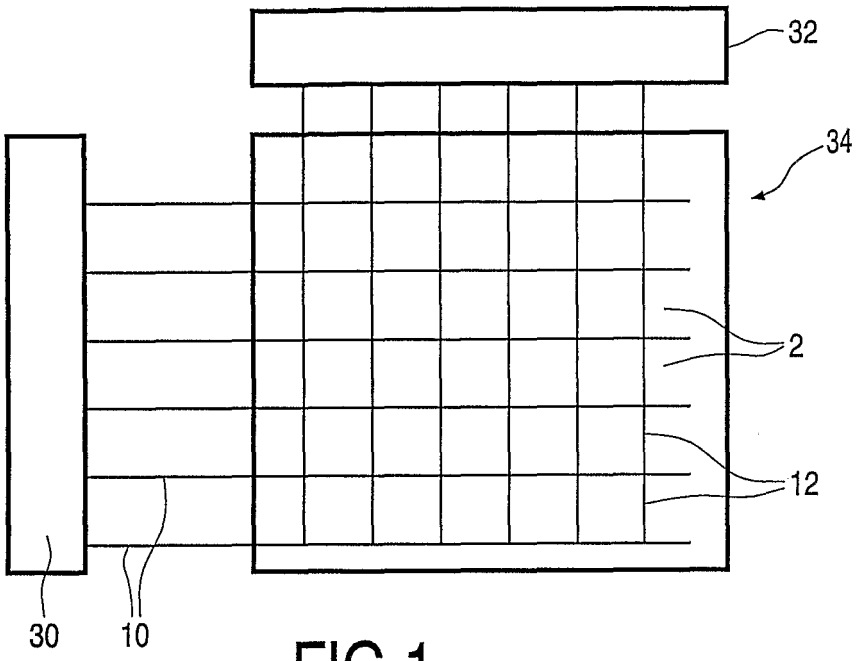


FIG.1

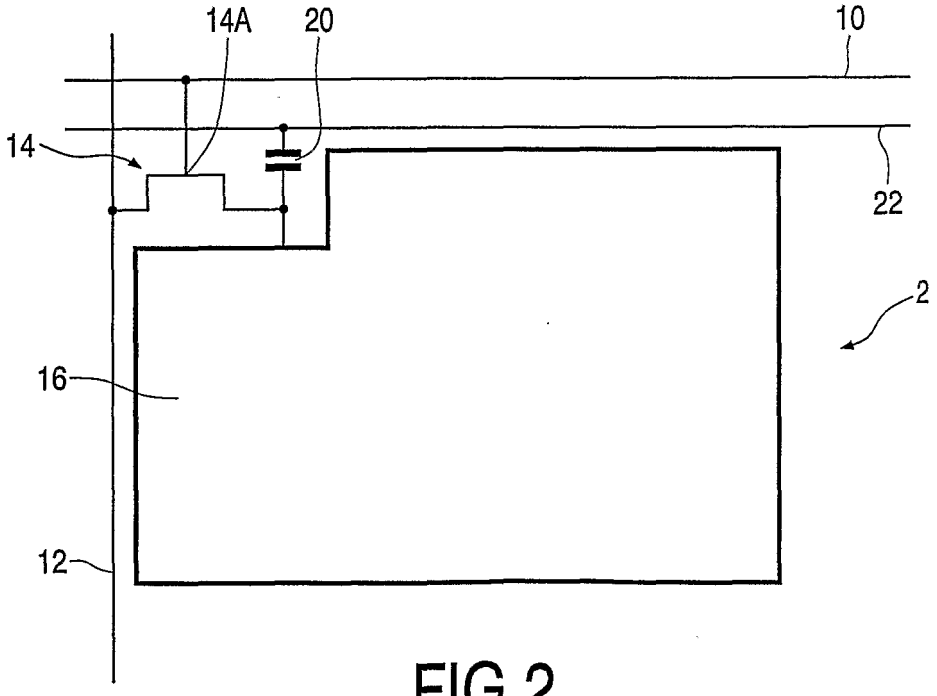
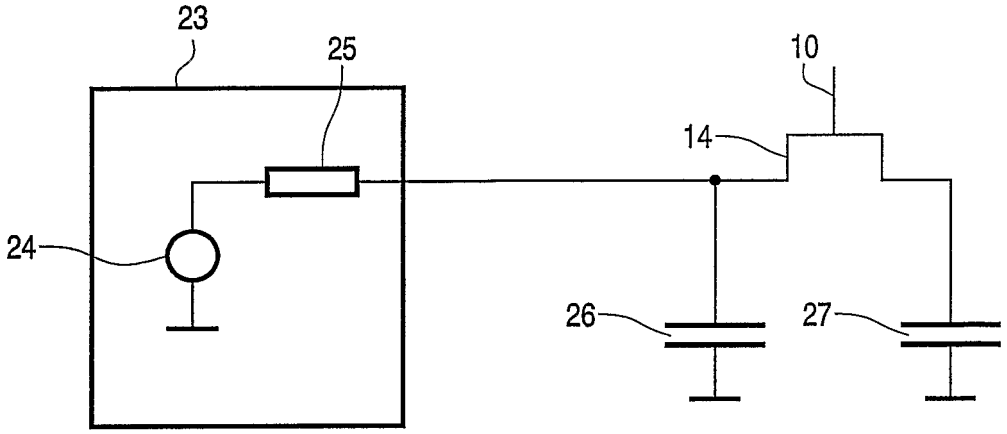


FIG.2


23
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14
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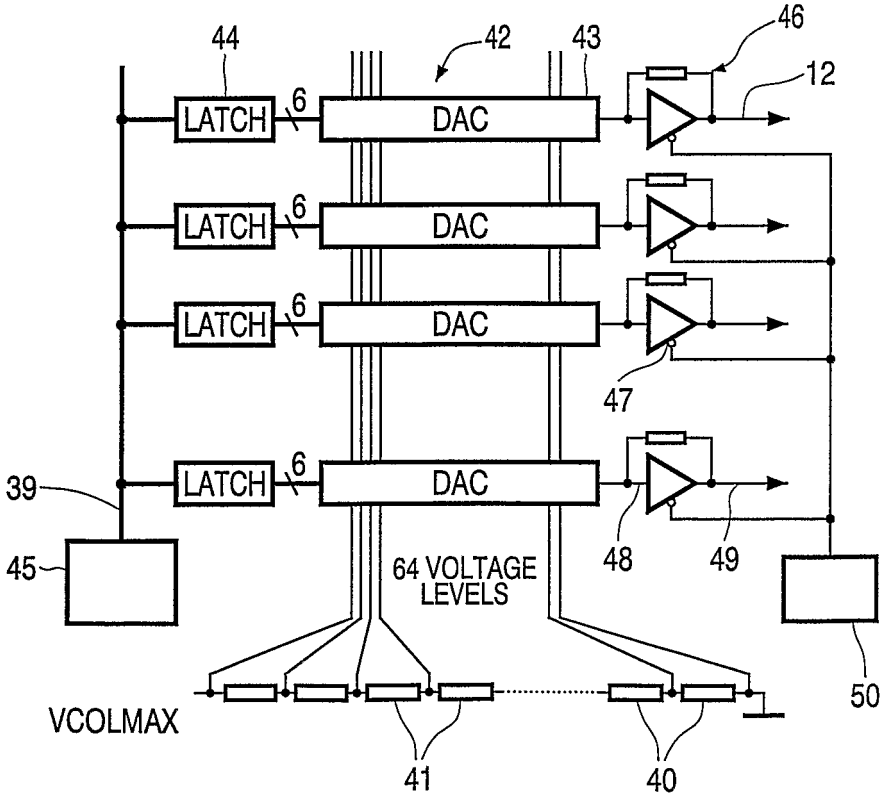
26
27

FIG.3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42
43
46
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LATCH
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DAC
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48
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64 VOLTAGE LEVELS
50
VCOLMAX
41
40

FIG.4

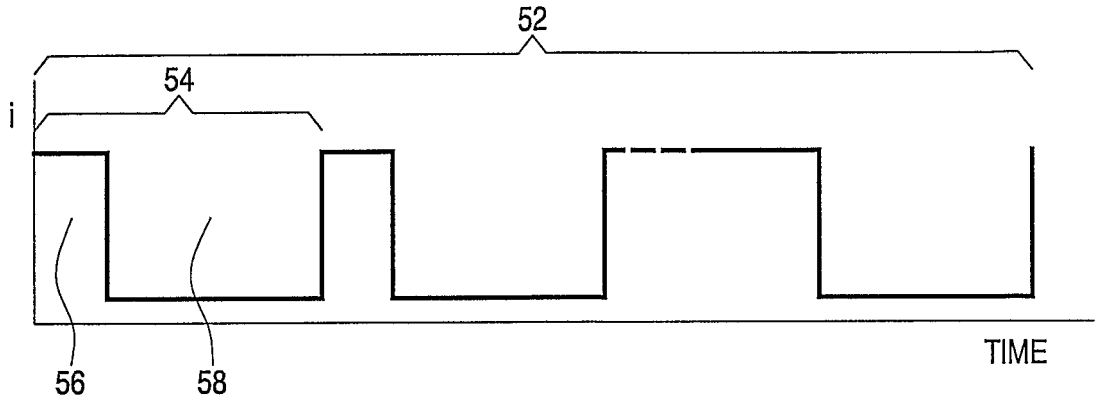


FIG.5

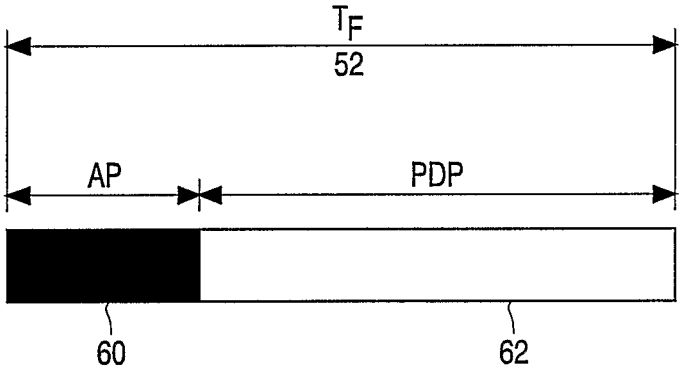


FIG.6A

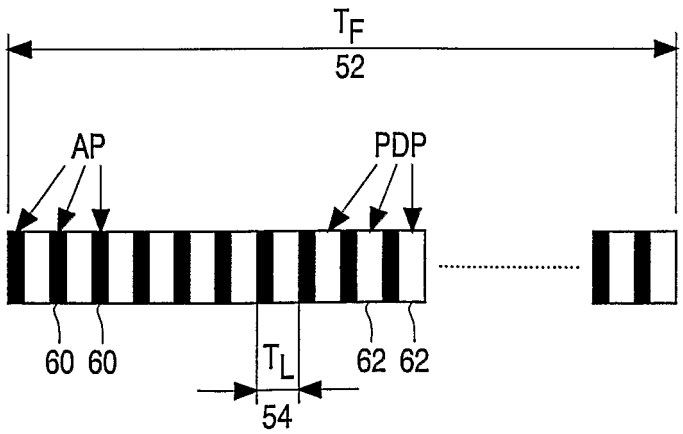
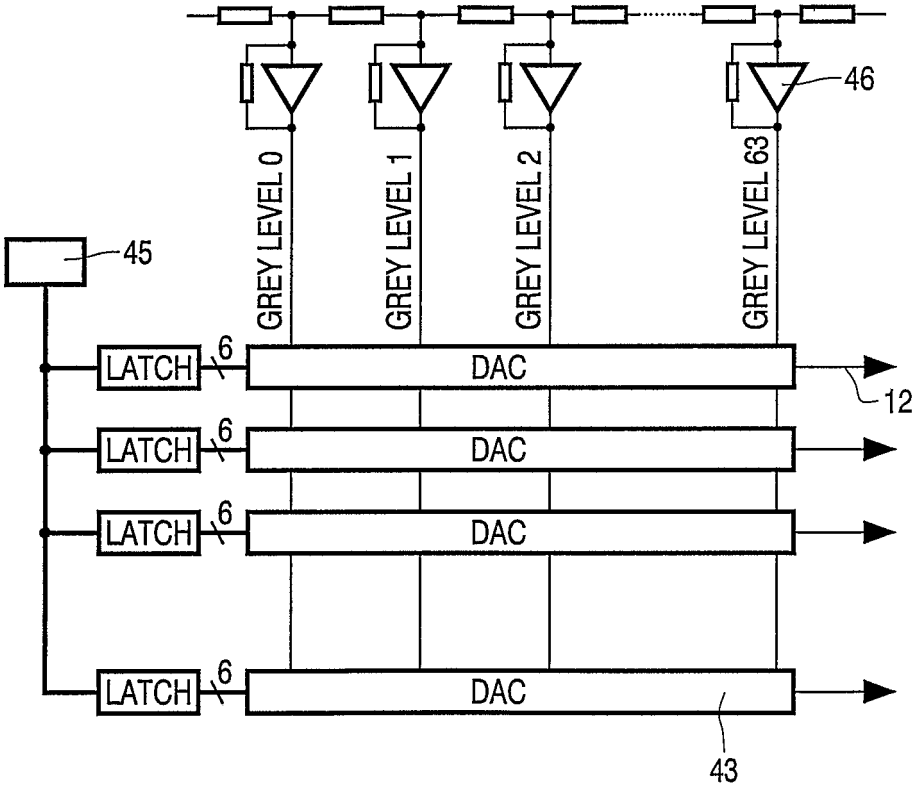


FIG.6B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12
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FIG.7

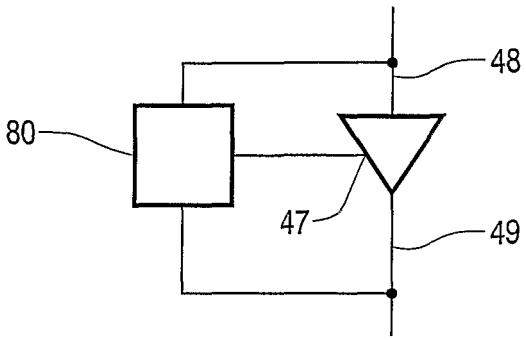

FIG.8

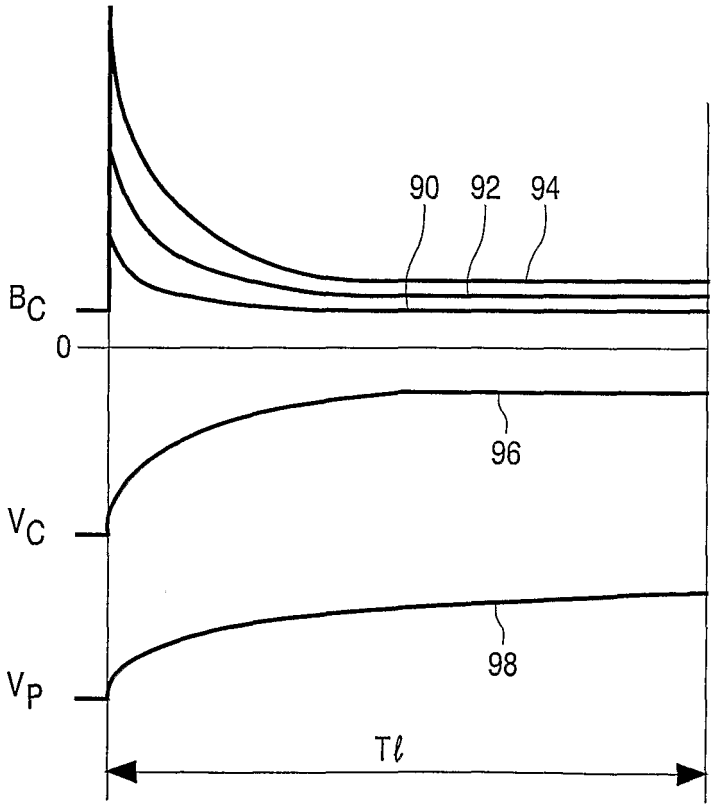

FIG.9

INTERNATIONAL SEARCH REPORT

PCT/IB 02/05131

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 157 360 A (SONG HO YOUNG ET AL) 5 December 2000 (2000-12-05) column 1 -column 2; figures 4,4A,5,5H,7 column 4 -column 5	1-12
X	US 6 184 855 B1 (SAKAGUCHI YOSHITAMI ET AL) 6 February 2001 (2001-02-06) column 8, line 35-58; figures 1,4,14 column 9, line 14 -column 10, line 50	1,4,5,8, 11
Y	the whole document	2,6,7
Y	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 07, 31 July 1997 (1997-07-31) -& JP 09 062233 A (MATSUSHITA ELECTRIC IND CO LTD), 7 March 1997 (1997-03-07) abstract; figures 1,3,9,10	2

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 March 2003	21/03/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Fulcheri, A

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 1 014 334 A (SONY CORP) 28 June 2000 (2000-06-28) abstract; figure 35	6,7
A	US 5 739 805 A (DINGWALL ANDREW GORDON FRANCIS) 14 April 1998 (1998-04-14) the whole document	1-12

INTERNATIONAL SEARCH REPORT

patent family members

PCT/IB 02/05131

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US 6157360 A	05-12-2000	AU 6550398 A	29-09-1998
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		JP 10510928 T	20-10-1998
		WO 9618990 A1	20-06-1996
		US 6046719 A	04-04-2000

专利名称(译)	用于液晶显示器的列驱动器		
公开(公告)号	EP1459287A1	公开(公告)日	2004-09-22
申请号	EP2002785826	申请日	2002-12-03
[标]申请(专利权)人(译)	皇家飞利浦电子股份有限公司		
申请(专利权)人(译)	皇家飞利浦电子N.V.		
当前申请(专利权)人(译)	皇家飞利浦电子N.V.		
[标]发明人	HECTOR JASON R KNAPP ALAN G		
发明人	HECTOR, JASON, R. KNAPP, ALAN, G.		
IPC分类号	G02F1/133 G09G3/20 G09G3/36		
CPC分类号	G09G3/2011 G09G3/3688 G09G3/3696 G09G2310/027 G09G2310/06 G09G2330/021		
优先权	2001030177 2001-12-18 GB		
外部链接	Espacenet		

摘要(译)

液晶显示器具有控制多个列线的多个缓冲器46。缓冲器具有偏置电流控制输入47，在该示例中由定时电路50控制，以在行周期期间设置电流以写入每行像素。具体地，行周期可以在具有高缓冲器偏置电流的驱动周期和具有较低缓冲器偏置电流的电压维持周期之间划分。