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(54) ARRAY SUBSTRATE, MANUFACTURING METHOD THEREOF, AND DISPLAY DEVICE

(57) An array substrate, a method of manufacturing the array substrate, and a display device are disclosed, for eliminating white Mura defects generated during the Cell process. The method comprises steps of: forming a display area and a non-display area on a substrate, a circuit bonding area being arranged within the non-display area; forming an alignment film within the display area through a patterning process; forming, through a patterning process, a transparent protection layer at least in a portion of the non-display area other than the circuit bonding area; and forming, through a rubbing-imprinting process, a plurality of lines having the same orientation on a surface of the alignment film, for an ordered arrangement of liquid crystal molecules, wherein a surface height of the transparent protection layer is lower than or equal to a surface height of the alignment film.

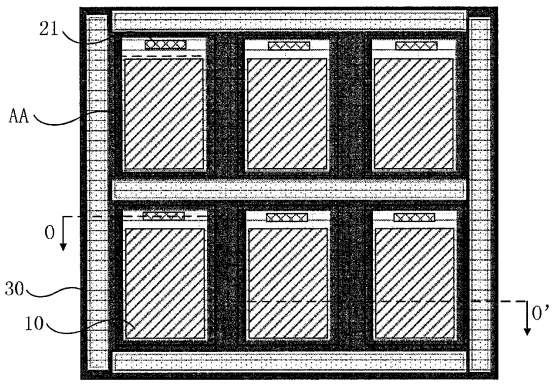


Fig. 3

EP 3 200 021 A1

Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present disclosure relates to the field of display technologies, and particularly, to an array substrate and a method of manufacturing the array substrate, and a display device.

Description of the Related Art

[0002] Thin Film Transistor Liquid Crystal Display (TFT-LCD), as a flat panel display device, has features of small volume, low power consumption, radiationless, relatively low production cost and the like, and is increasingly applied in the field of high-performance display.

[0003] A TFT-LCD comprises an array substrate and a color filter substrate. A liquid crystal layer is arranged between the array substrate and the color filter substrate, and deflection of liquid crystal molecules in the liquid crystal layer is controlled to achieve control of light intensity for the final propose of image display. Existing processes of manufacturing the TFT-LCD mainly include four stages: a color filter substrate manufacturing process, an Array process (array substrate manufacturing process), a Cell process (liquid crystal cell manufacturing process), and a Module process (module assembling process). In order to effectively control the deflection of the liquid crystal molecules, as shown in Fig. 1, in the Cell process, an alignment film 10 needs to be provided on a surface of an active display area (Active Area, and AA area for short) of array substrate that has been already manufactured, such that the liquid crystal molecules can be arranged consistently with each other on a surface of the alignment film 10. Specifically, a transparent resin layer is formed on the surface of the AA area, and then a surface of the transparent resin layer is rubbed by using a printing roller (Rubbing Cloth) so as to form regular lines, thereby finishing manufacturing of the alignment film 10.

[0004] During the process of manufacturing the alignment film, however, when a surface of a material layer of the alignment film is rubbed by the printing roller, an area outside of the AA area (non-display area) will also be rubbed. Since metal wires 20 for transmitting control signals or a metal layer for a circuit bonding area 21 are arranged within the non-display area, when the metal wires 20 or the metal layer is rubbed by the printing roller, metal scraps and excessive scraps of the rubbing cloth (Cloth) on the printing roller are generated. The metal scraps are relative hard and will damage the surface of the manufactured alignment film 10 under impacting of a water stream during cleaning, and the above cloth scraps will remain on the surface of the alignment film, such that some of the liquid crystal molecules cannot be arranged at preset positions. As a result, deflection states of the above liquid crystal molecules in a disordered arrangement state cannot be effectively controlled during display, which results in uncontrolled bright pixel points (i.e., the white Mura defect) in the AA area and adverse effects on image quality. Although in prior arts the array substrate will be optically detected and then the detected defects will be repaired, a pixel electrode layer on the array substrate has a relative thin thickness, which reduces defect recognizability in the optical detection. Thus, an omission factor of the white Mura defects increases, thereby significantly reducing product quality and display effect.

SUMMARY OF THE INVENTION

[0005] Embodiments of The present disclosure provide an array substrate and a method of manufacturing the same, and a display device, for eliminating phenomenon of white Mura defects generated during the Cell process.

[0006] According to one aspect of embodiments of the present disclosure, there is provided a method of manufacturing an array substrate, comprising steps of:

forming a display area and a non-display area on a substrate, a circuit bonding area being arranged within the non-display area;
forming an alignment film in the display area through a patterning process;
forming, through a patterning process, a transparent protection layer at least in a portion of the non-display area other than the circuit bonding area; and
forming, through a rubbing-imprinting process, a plurality of lines having the same orientation on a surface of the alignment film, for an ordered arrangement of liquid crystal molecules,
wherein a surface height of the transparent protection layer is lower than or equal to a surface height of the alignment film.

[0007] In the method of manufacturing the array substrate according to one embodiment of the present disclosure, the step of forming a transparent protection layer comprises:

coating a first resin layer on a surface of the substrate on which the alignment film has been formed;
forming photoresist on a surface of the first resin layer;
forming, through a single masking and exposing process and a single development process, a first full coverage area of the photoresist and a first full removal area of the photoresist, the first full coverage area of the photoresist corresponding to the transparent protection layer to be formed and the first full removal area of the photoresist corresponding to the circuit bonding area and a pattern of the alignment film;
etching a portion of the first resin layer corresponding

to the first removal area of the photoresist; and
peeling off the photoresist in the first full coverage area of the photoresist, so that a remaining portion of the first resin layer forms the transparent protection layer.

[0008] In the method of manufacturing the array substrate according to one embodiment of the present disclosure, the steps of forming the alignment film and the transparent protection layer comprise:

coating a first resin layer on a surface of the substrate having the display area and the non-display area;
coating a second resin layer on the first resin layer;
forming photoresist on a surface of the second resin layer;
forming, through a single masking and exposing process and a single development process, a second full coverage area of the photoresist, a second full removal area of the photoresist, and a partial removal area of the photoresist, the second full coverage area of the photoresist corresponding to the alignment film to be formed, the second full removal area of the photoresist corresponding to the circuit bonding area, and the partial removal area of the photoresist corresponding to the transparent protection layer to be formed;
etching a portion of the second resin layer and a portion of the first resin layer corresponding to the second full removal area of the photoresist;
ashing a portion of the photoresist in the partial removal area of the photoresist, and etching a portion of the second resin layer corresponding to the partial removal area of the photoresist; and
peeling off a portion of the photoresist within the second full coverage area, so that a remaining portion of the first resin layer forms the transparent protection layer.

[0009] In the method of manufacturing the array substrate according to one embodiment of the present disclosure, the transparent protection layer has a thickness in a range from 2 μm to 5 μm.

[0010] In the method of manufacturing the array substrate according to one embodiment of the present disclosure, an area of the circuit bonding area is smaller than a printing area of a printing roller for implementing the rubbing-imprinting process.

[0011] According to another aspect of embodiments of the present disclosure, there is provided an array substrate, comprising:

a substrate provided with a display area and a non-display area, a circuit bonding area being arranged within the non-display area;
an alignment film in the display area, a plurality of lines having the same orientation being formed on a surface of the alignment film, for an ordered arrangement of liquid crystal molecules; and
a transparent protection layer located at least in a portion of the non-display area other than the circuit bonding area;
wherein a surface height of the transparent protection layer is lower than or equal to a surface height of the alignment film.

[0012] In the array substrate according to one embodiment of the present disclosure, a portion of a surface of the substrate corresponding to the display area is provided only with the alignment film thereon.

[0013] In the array substrate according to one embodiment of the present disclosure, the transparent protection layer and the alignment film are disposed in sequence on a portion of a surface of the substrate corresponding to the display area.

[0014] In the array substrate according to one embodiment of the present disclosure, the transparent protection layer has a thickness in a range from 2 μm to 5 μm.

[0015] In the array substrate according to one embodiment of the present disclosure, an area of the circuit bonding area is smaller than a printing area of a printing roller for forming the lines by implementing a rubbing-imprinting process.

[0016] According to a further aspect of embodiments of the present disclosure, there is provided a display device, comprising the array substrate according to any one of the above embodiments.

[0017] Embodiments of The present disclosure provide an array substrate and a method of manufacturing the same, and a display device, for eliminating phenomenon of white Mura defects generated during the Cell process. According to the above method, during the rubbing-imprinting process on the alignment film, the presence of the protection layer can protect metal wires for transmitting control signals under the protection layer from being rubbed by the printing roller, thereby avoiding generation of metal scraps and excessive cloth scraps.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Accompanying drawings, which are used when describing embodiments of the present invention or prior arts, will be briefly introduced in order to illustrate technical solutions in the embodiments of the present invention or in prior arts more clearly. Obviously, the accompanying drawings described in the following description are only to illustrate some embodiments of the present invention, and other drawings may be obtained according to these accompanying drawings without creative work.

Fig. 1 is a partial plan view of an array substrate in prior arts;
Fig. 2 is a flowchart of a method of manufacturing an array substrate according to one exemplary embodiment of the present disclosure;
Fig. 3 is a partial plan view of an array substrate

according to one exemplary embodiment of the present disclosure;

Fig. 4 is a flowchart of forming a transparent protection layer in a method of manufacturing an array substrate according to one exemplary embodiment of the present disclosure;

Fig. 5a to Fig. 5e are schematic diagrams showing manufacturing processes of forming the transparent protection layer in the method of manufacturing the array substrate according to the exemplary embodiment of the present disclosure;

Fig. 6 is a flowchart of forming an alignment layer and a transparent protection layer in a method of manufacturing an array substrate according to another exemplary embodiment of the present disclosure; and

Fig. 7a to Fig. 7g are schematic diagrams showing manufacturing processes of forming the alignment layer and a transparent protection layer in the method of manufacturing the array substrate according to the another exemplary embodiment of the present disclosure.

Reference Numbers:

[0019]

01-substrate; 10-alignment film; 20-metal wire; 21-circuit bonding area; 30-transparent protection layer; 40-photoresist; 101-first resin layer; 201-second resin layer; 401-first full coverage area of the photoresist; 402-first full removal area of the photoresist; 411-second full coverage area of the photoresist; 412-second full removal area of the photoresist; 413-partial removal area of the photoresist; AA-display area.

DETAILED DESCRIEPTION OF THE EMBODIMENTS

[0020] Technique solution in embodiments of the present disclosure will be described clearly and thoroughly hereinafter in detail with reference to the accompanying drawings in the embodiments of the present disclosure. Obviously, the described embodiments are only some, rather than all, of embodiments of the present disclosure. Based on the embodiments of the present disclosure, all of other embodiments obtained by those skilled in the art without any creative work will fall within the scope of the present invention.

[0021] Further, in the following detailed description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the disclosed embodiments. It will be apparent, however, that one or more embodiments may be practiced without these specific details. In other instances, well-known structures and devices are schematically shown in order to simplify the drawing.

[0022] With reference to Figs. 1-3, a method of manufacturing an array substrate according to one exemplary embodiment of the present disclosure comprises the following steps:

S101: forming a display area AA and a non-display area (an area except the display area AA, which is not indicated by reference number in figures) on a substrate 01, as shown in Fig. 1;

S102: forming an alignment film in the display area AA through a patterning process, as shown in Fig. 3;

S103: forming, through a patterning process, a transparent protection layer 30 at least in a portion of the non-display area other than a circuit bonding area 21; and

S104: forming, through a rubbing-imprinting process, a plurality of lines having the same orientation on a surface of the alignment film 10, for an ordered arrangement of liquid crystal molecules in a liquid crystal layer,

wherein a surface height of the transparent protection layer 30 is lower than or equal to a surface height of the alignment film 10.

[0023] With the method of manufacturing an array substrate according to the embodiment of the present disclosure, during the rubbing-imprinting process implemented on the alignment film, the presence of the protection layer can protect metal wires for transmitting control signals under the protection layer from being rubbed by the printing roller, thereby avoiding generation of metal scraps and excessive cloth scraps.

[0024] In addition, although a surface of the circuit bonding area is not covered by the transparent protection layer, an area of the above circuit bonding area is generally set to be smaller than a printing area of the printing roller for implementing the rubbing-imprinting process during manufacturing the array substrate, and the transparent protection layer is located higher than the circuit bonding area. Thus, during implementing the rubbing-imprinting process, the printing roller will contact the transparent protection layer at periphery of the circuit bonding area and will not wear the metal layer within the circuit bonding area, thereby avoiding generation of metal scraps. As a result, during subsequent cleaning process, no hard metal scrap will damage the surface of the manufactured alignment film, and cloth scraps are reduced, thereby reducing the number of residual cloth scraps on the surface of the alignment film. Thus, the liquid crystal molecules can be orderly arranged at preset positions on the surface of the alignment film, thereby solving the problem of generation of the white Mura defects in the Cell process.

[0025] It is noted that the above circuit bonding area 21 may be used to bond a drive integrated circuits (ICs), for example, a drive IC for driving gate lines or data lines, and a flexible printed circuit board (FPC). Since the circuit bonding area 21 is exposed from the transparent protection layer 30, the bonding of the control circuit(s) will not

be adversely affected during the Module process (module assembling process) of the display device.

[0026] When the surface height of the transparent protection layer 30 is equal to the surface height of the alignment film 10, not only the problem of generation of the white Mura defects in the Cell process can be solved, but also height differences among respective film layers on the surface of the array substrate can be reduced, such that the surface of the array substrate is flat. Dust and foreign matters are prevented from being accumulated at positions where the above height differences exist during production or transportation, thereby improving product quality. Further, during manufacturing the lines on the surface of the alignment film 10, the cloth on the printing roller can be prevented from being contaminated by the above dust or foreign matters.

[0027] It is to be noted that, with reference to Figs. 5a and 5e, the surface height may be a height from a surface of the thin film type transparent protection layer 30 away from the substrate 01 to the substrate 01. Thus, when mentioning that the surface height of the transparent protection layer 30 is lower than or equal to the surface height of the alignment film 10, it is intended that the height from the surface of the transparent protection layer 30 away from the substrate 01 to the substrate 01 is lower than or equal to a height from a surface of the alignment film 10 away from the substrate 01 to the substrate 01. In such a manner, it can be ensured that during the rubbing-imprinting process, the printing roller can make a sufficient contact with the surface of the alignment film 10.

[0028] In embodiments of the present disclosure, the patterning process may include a lithography process, or include a lithography process and an etching step, and meanwhile, may also include other processes for forming predetermined patterns, such as printing, ink-jetting or the like. The lithography process is a process including film formation, exposure, development and the like, and during which photoresist, masks, exposure machine and the like are used to form patterns. A suitable patterning process may be selected according to structures formed in the present disclosure. Hereinafter, a single patterning process according to embodiments of the present disclosure will be described with an example, in which different exposed regions are formed through a single masking and exposing process, then several removal processes, such as etching, ashing or the like, are applied to the different exposed regions , and finally expected patterns are obtained.

[0029] In the following, processes of forming the transparent protection layer 30 or/and the alignment film 10 before the step S104 will be described in detail.

[0030] In the exemplary embodiment shown in Figs. 4 and 5a-5e, before the step S104, the method of forming the transparent protection layer 30 may include the following steps.

[0031] In S201, a first resin layer 101 is coated on a surface of the substrate 01 formed with the alignment film 10, as shown in Fig. 5a (which is a sectional view taken along line O-O' in Fig. 3).

[0032] When manufacturing the array substrate, metal wires 20 and the circuit bonding area 21 have already been manufactured on the substrate 01, therefore the metal wires 20 and the circuit bonding area 21 are schematically shown in the substrate 01 in the figures of the embodiments of the present disclosure.

[0033] In S202, photoresist 40 is formed on a surface of the first resin layer 101, as shown in Fig. 5b.

[0034] In S203, a first full coverage area 401 of the photoresist and a first full removal area 402 of the photoresist are formed through a single masking and exposing process and a developing process. The first full coverage area 401 corresponds to a pattern of the transparent protection layer 30 to be formed, and the first full removal area 402 corresponds to the circuit bonding area 21 and a pattern of the alignment film 10, as shown in Fig. 5c.

[0035] In S204, a portion of the first resin layer 101 corresponding to the first removal area 402 is etched off, as shown in Fig. 5d.

[0036] In S205, a portion of the photoresist 40 in the first full coverage area 401 is peeled off, so that a remaining portion of the first resin layer 101 forms the transparent protection layer 30. The transparent protection layer 30 covers a portion of the non-display area except the circuit bonding area 21.

[0037] It is noted that, for the photoresist layer in embodiments of the present disclosure, if a positive photoresist is used, after exposing and developing through a mask, a portion of the photoresist layer within an exposed region may be removed during the developing, while a portion of the photoresist layer within an unexposed region is remained during the developing. If a negative photoresist is used, the portion of the photoresist layer within the exposed region is remained during the developing, while the portion of the photoresist layer within the unexposed region is removed during the developing. The type of the photoresist is not limited in the present disclosure. However, embodiments of the present disclosure are described with examples in which the portion of the photoresist layer within the exposed region is removed, while the portion of the photoresist layer within the unexposed region is remained.

[0038] As can be seen from Fig. 5e, the surface height of the transparent protection layer 30 is lower than or equal to the surface height of the alignment film 10 within the display area AA. Thus, before performing step S104, the printing roller can make a sufficient contact with the alignment film 10, and forms a pattern of lines having the same orientation on the surface of the alignment film 10. Since the metal wires 20 are covered by the transparent protection layer 30, the printing roller can be prevented from rubbing the metal wires 20 under the protection layer, thereby avoiding generation of metal scraps and excessive cloth scraps. In addition, during manufacturing the array substrate, although the surface of the circuit bonding area 21 is not covered by the transparent pro-

tection layer 30, an area of the circuit bonding area 21 is generally smaller than a printing area (i.e., a contact area between the printing roller and an object being printed) of the printing roller and the transparent protection layer 30 is located higher than the circuit bonding area 21. Thus, the printing roller will contact the transparent protection layer 30 at periphery of the circuit bonding area 21 and will not wear the metal layer within the circuit bonding area 21, thereby avoiding generation of metal scraps. As such, during subsequent cleaning process, no hard metal scrap will damage the surface of the manufactured alignment film, and cloth scraps are reduced, thereby reducing the number of residual cloth scraps on the surface of the alignment film. Thus, the liquid crystal molecules can be orderly arranged at preset positions on the surface of the alignment film, thereby solving the problem of generation of the white Mura defects in the Cell process.

[0039] In one embodiment, the above transparent protection layer 30 may has a thickness in a range from 2 μm to 5 μm. When the thickness of the transparent protection layer 30 is smaller than 2 μm, it is hard to form a film on the substrate due to the excessively thin thickness. When the thickness of the transparent protection layer 30 is larger than 5 μm, the thickness of the transparent protection layer 30 may be larger than the thickness of the alignment film 10, which results in that during the rubbing-imprinting process, the printing roller cannot contact the surface of the alignment film 10 and thereby cannot form the lines on the surface of the alignment film 10.

[0040] In another exemplary embodiment shown in Figs. 6 and 7a-5g (7g), before step S103, the method of forming the alignment film 10 and the transparent protection layer 30 may includes the following steps.

[0041] In S301, a first resin layer 101 is coated on a surface of the substrate 01 having the display area AA and the non-display area (not indicated by reference number in Fig. 3), as shown in Fig. 7a.

[0042] In S302, a second resin layer 201 is coated on the first resin layer 101, as shown in Fig. 7b.

[0043] In S303, photoresist 40 is formed on a surface of the second resin layer 201, as shown in Fig. 7c.

[0044] In S304, a second full coverage area 411 of the photoresist, a second full removal area 412 of the photoresist, and a partial removal area 413 of the photoresist are formed through a single masking and exposing process and a single developing process, as shown in Fig. 7d. The second full coverage area 411 corresponds to the alignment film 10 to be formed, the second full removal area 412 corresponds to the circuit bonding area 21, and the partial removal area 413 corresponds to the transparent protection layer 30 to be formed.

[0045] In S305, a portion of the second resin layer 201 and a portion of the first resin layer 101 corresponding to the second full removal area 412 are etched off, so that the circuit bonding area 21 is exposed, as shown in Fig. 7e.

[0046] In S306, a portion of the photoresist 40 in the partial removal area 413 is ashed, and a portion of the second resin layer 201 corresponding to the partial removal area 413 is etched, so that a remaining portion of the second resin layer forms the alignment layer 10, as shown in Fig. 7f. During such processes, a thickness of the photoresist within the second full coverage area 411 is thinned.

[0047] In S307, a portion of the photoresist 40 within the second full coverage area 411 is peeled off, so that a remaining portion of the first resin layer forms the transparent protection layer 30, as shown in Fig. 7g.

[0048] As can be seen from Fig. 7g, the alignment layer 10 is located on the surface of the transparent protection layer 30, so that not only lines can be formed on the surface of alignment layer 10, but also the metal wires 20 underneath the protection layer can be protected from being rubbed by the printing roller because the metal wire 20 is covered by the transparent protection layer 30, thereby avoiding generation of metal scraps and excessive cloth scraps. In addition, during manufacturing the array substrate, although the surface of the circuit bonding area 21 is not covered by the transparent protection layer 30, an area of the circuit bonding area 21 is generally smaller than a printing area (i.e., a contact area between the printing roller and an object being printed) of the printing roller and the transparent protection layer 30 is located higher than the circuit bonding area 21. Thus, the printing roller will contact the transparent protection layer 30 at periphery of the circuit bonding area 21 and will not wear the metal layer within the circuit bonding area 21, thereby avoiding generation of metal scraps. As such, during subsequent cleaning process, no hard metal scrap will damage the surface of the manufactured alignment film, and cloth scraps are reduced, thereby reducing the number of residual cloth scraps on the surface of the alignment film. Thus, the liquid crystal molecules can be orderly arranged at preset positions on the surface of the alignment film, thereby solving the problem of generation of the white Mura defects in the Cell process.

[0049] In the embodiment shown in Fig. 5e, there is no layer arrangement between the alignment layer 10 and the substrate 1, thus an electric field applied across two ends of the liquid crystal layer during display will not be affected. During manufacture, however, since the first resin layer 101 covering over the surface of the alignment layer 10 needs to be etched, a higher etching precision is required so that the surface of the alignment layer 10 is prevented from being damaged during etching.

[0050] In the embodiment shown in Fig. 7g, since the alignment layer 10 is located on the surface of the transparent protection layer 30, there is no need to etch the surface of the second resin layer that forms the alignment layer 10, thus, the surface of the alignment layer 10 is protected from being damaged due to undesired etching precision. In this embodiments, however, the transparent protection layer 30 is arranged between the alignment layer 10 and the substrate 01, thus, for a Twist Nematic

(TN) type display device comprising a common electrode formed on the substrate, a distance between the common electrode and a pixel electrode on the color filter substrate is increased, therefore the electric field applied across two ends of the liquid crystal layer will be affected.

[0051] It can be understood that the above two arrangements may be selected by those skilled in the art according to practical requirements.

[0052] According to embodiments of another aspect of the present disclosure, as shown in Fig. 1, there is provided an array substrate, comprising: a substrate 01 provided with a display area AA and a non-display area (an area except the display area AA, which is not indicated by reference number in the attached drawings); an alignment film 10 in the display area AA, a plurality of lines having the same orientation being formed on a surface of the alignment film 10, for an ordered arrangement of liquid crystal molecules; and a transparent protection layer 30 located at least in a portion of the non-display area except a circuit bonding area 21. A surface height of the transparent protection layer 30 is lower than or equal to a surface height of the alignment film 10.

[0053] With the array substrate according to embodiments of the present disclosure, during the rubbing-imprinting process performed on the alignment film, the presence of the protection layer can prevent metal wires for transmitting control signals under the protection layer from being rubbed by the printing roller, thereby avoiding generation of metal scraps and excessive cloth scraps.

[0054] In one embodiment, an area of the circuit bonding area 21 is smaller than a printing area of the printing roller (not shown) for forming the lines by implementing the rubbing-imprinting process, and the printing area is a contact area between the printing roller and a printed object. As such, during manufacturing the array substrate, although the surface of the circuit bonding area 21 is not covered by the transparent protection layer 30, the area of the circuit bonding area 21 is generally smaller than the printing area of the printing roller and the transparent protection layer 30 is located higher than the circuit bonding area 21. Thus, the printing roller will contact the transparent protection layer 30 at periphery of the circuit bonding area 21 and will not wear the metal layer within the circuit bonding area 21, thereby avoiding generation of metal scraps. Therefore, during subsequent cleaning process, no hard metal scrap will damage the surface of the manufactured alignment film, and cloth scraps are reduced, thereby reducing the number of residual cloth scraps on the surface of the alignment film. Thus, the liquid crystal molecules can be orderly arranged at preset positions on the surface of the alignment film, thereby solving the problem of generation of the white Mura defects in the Cell process.

[0055] Hereinafter, a structure of the transparent protection layer 30 or the alignment film 10 will be described in detail.

[0056] As shown in Fig. 5e, in the array substrate, the portion of the surface of the substrate corresponding to the display area AA is provided only with the alignment film 10 thereon. Since the surface height of the transparent protection layer 30 is lower than or equal to the surface height of the alignment film 10 within the display area AA, the printing roller can contact the alignment film 10 before step S104 and form a pattern of lines having the same orientation on the surface of the alignment film 10. Since the metal wires 20 are covered by the transparent protection layer 30, the printing roller can be prevented from rubbing the metal wires 20 underneath the protection layer, thereby avoiding generation of metal scraps and excessive cloth scraps. In addition, during manufacturing the array substrate, although the surface of the circuit bonding area 21 is not covered by the transparent protection layer 30, an area of the circuit bonding area 21 is generally smaller than a printing area of the printing roller and the transparent protection layer 30 is located higher than the circuit bonding area 21. Thus, the printing roller will contact the transparent protection layer 30 at periphery of the circuit bonding area 21 and will not wear the metal layer within the circuit bonding area 21, thereby avoiding generation of metal scraps and excessive cloth scraps.

[0057] In one embodiment, the above transparent protection layer 30 may has a thickness in a range from 2 μm to 5 μm. When the thickness of the transparent protection layer 30 is smaller than 2 μm, it is hard to form a film on the substrate due to the excessively thin thickness. When the thickness of the transparent protection layer 30 is larger than 5 μm, the thickness of the transparent protection layer 30 may be larger than the thickness of the alignment film 10, which results in that during the rubbing-imprinting process, the printing roller cannot contact the surface of the alignment film 10 and thereby cannot form the lines on the surface of the alignment film 10.

[0058] As shown in Fig. 7g, in the array substrate, the transparent protection layer 30 and the alignment film 10 are disposed in sequence on a portion of the surface of the substrate corresponding to the display area AA. The alignment layer 10 is located on the surface of the transparent protection layer 30. As such, not only the lines can be formed on the surface of alignment layer 10, but also the metal wires 20 underneath the protection layer can be protected from being rubbed by the printing roller because the metal wire 20 is covered by the transparent protection layer 30, thereby avoiding generation of metal scraps and excessive cloth scraps. In addition, during manufacturing the array substrate, although the surface of the circuit bonding area 21 is not covered by the transparent protection layer 30, the area of the circuit bonding area 21 is generally smaller than the printing area of the printing roller and the transparent protection layer 30 is located higher than the circuit bonding area 21. Thus, the printing roller will contact the transparent protection layer 30 at periphery of the circuit bonding area 21 and will not wear the metal layer within the circuit bonding area 21, thereby avoiding generation of metal scraps.

[0059] In the embodiment shown in Fig. 5e, there is no layer arrangement between the alignment layer 10 and the substrate 1, thus an electric field applied across two ends of the liquid crystal layer during display will not be affected. During manufacture, however, since the first resin layer 101 covering over the surface of the alignment layer 10 needs to be etched, a higher etching precision is required so that the surface of the alignment layer 10 is prevented from being damaged during etching.

[0060] In the embodiment shown in Fig. 7g, since the alignment layer 10 is located on the surface of the transparent protection layer 30, there is no need to etch the surface of the second resin layer that forms the alignment layer 10, thus, the surface of the alignment layer 10 is protected from being damaged due to undesired etching precision. In this embodiments, however, the transparent protection layer 30 is arranged between the alignment layer 10 and the substrate 01, thus, for a Twist Nematic (TN) type display device comprising a common electrode formed on the substrate, a distance between the common electrode and a pixel electrode on the color filter substrate is increased, therefore the electric field applied across two ends of the liquid crystal layer will be affected.

[0061] It can be understood that the above two arrangements may be selected by those skilled in the art according to practical requirements.

[0062] In embodiments according to a further aspect of the present disclosure, there is provided a display device, comprising any one of the array substrates as described above, and having the same advantageous effects as the array substrate in the foregoing embodiments. Arrangement and advantageous effects of the array substrate have been described in detail in the foregoing embodiments, and thus will not be repeated herein.

[0063] In embodiments of the present disclosure, specifically, the display device may at least include a liquid crystal display device and an organic light emitting diode display device. For example, the display device may be a liquid crystal display, a liquid crystal TV, a digital frame, a mobile phone, a tablet computer or any other products or components having a display function.

[0064] The above description is only intended to illustrate preferred embodiments of the present disclosure, and the scope of the present invention is not limited thereto. Changes or alternatives that can be easily envisaged by those skilled in the art based on the disclosure of the present invention should fall within the scope of the present invention. Thus, the scope of the invention should be determined by the scopes of the claims.

Claims

1. A method of manufacturing an array substrate, comprising steps of:

   forming a display area and a non-display area on a substrate, a circuit bonding area being arranged within the non-display area;
   forming an alignment film in the display area through a patterning process;
   forming, through a patterning process, a transparent protection layer at least in a portion of the non-display area other than the circuit bonding area; and
   forming, through a rubbing-imprinting process, a plurality of lines having the same orientation on a surface of the alignment film, for an ordered arrangement of liquid crystal molecules,
   wherein a surface height of the transparent protection layer is lower than or equal to a surface height of the alignment film.

2. The method according to claim 1, wherein the step of forming the transparent protection layer comprises:

   coating a first resin layer on a surface of the substrate on which the alignment film has been formed;
   forming photoresist on a surface of the first resin layer;
   forming, through a single masking and exposing process and a single development process, a first full coverage area of the photoresist and a first full removal area of the photoresist, the first full coverage area of the photoresist corresponding to the transparent protection layer to be formed and the first full removal area of the photoresist corresponding to the circuit bonding area and a pattern of the alignment film;
   etching a portion of the first resin layer corresponding to the first removal area of the photoresist; and
   peeling off the photoresist in the first full coverage area of the photoresist, so that a remaining portion of the first resin layer forms the transparent protection layer.

3. The method according to claim 1, wherein the steps of forming the alignment film and the transparent protection layer comprise:

   coating a first resin layer on a surface of the substrate having the display area and the non-display area;
   coating a second resin layer on the first resin layer;
   forming photoresist on a surface of the second resin layer;
   forming, through a single masking and exposing process and a single development process, a second full coverage area of the photoresist, a second full removal area of the photoresist, and a partial removal area of the photoresist, the second full coverage area of the photoresist corre-

sponding to the alignment film to be formed, the second full removal area of the photoresist corresponding to the circuit bonding area, and the partial removal area of the photoresist corresponding to the transparent protection layer to be formed;
etching a portion of the second resin layer and a portion of the first resin layer corresponding to the second full removal area of the photoresist;
ashing a portion of the photoresist in the partial removal area of the photoresist, and etching a portion of the second resin layer corresponding to the partial removal area of the photoresist; and
peeling off a portion of the photoresist within the second full coverage area of the photoresist, so that a remaining portion of the first resin layer forms the transparent protection layer.

4. The method according to claim 2, wherein the transparent protection layer has a thickness in a range from 2 μm to 5 μm.

5. The method according to any one of claims 1 to 4, wherein an area of the circuit bonding area is smaller than a printing area of a printing roller for implementing the rubbing-imprinting process.

6. An array substrate, comprising:

a substrate provided with a display area and a non-display area, a circuit bonding area being arranged within the non-display area;
an alignment film in the display area, a plurality of lines having the same orientation being formed on a surface of the alignment film, for an ordered arrangement of liquid crystal molecules; and
a transparent protection layer located at least in a portion of the non-display area other than the circuit bonding area;
wherein a surface height of the transparent protection layer is lower than or equal to a surface height of the alignment film.

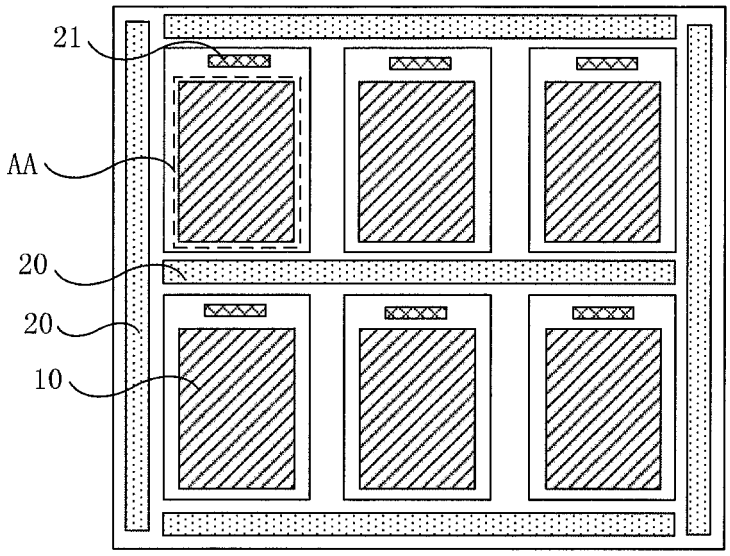
7. The array substrate according to claim 6, wherein a portion of a surface of the substrate corresponding to the display area is provided only with the alignment film thereon.

8. The array substrate according to claim 6, wherein the transparent protection layer and the alignment film are disposed in sequence on a portion of a surface of the substrate corresponding to the display area.

9. The array substrate according to claim 7, wherein the transparent protection layer has a thickness in a range from 2 μm to 5 μm.

10. The array substrate according to any one of claims 6 to 9, wherein an area of the circuit bonding area is smaller than a printing area of a printing roller for forming the lines by implementing a rubbing-imprinting process.

11. A display device, comprising the array substrate according to any one of claims 6 to 10.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AA
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Fig. 1

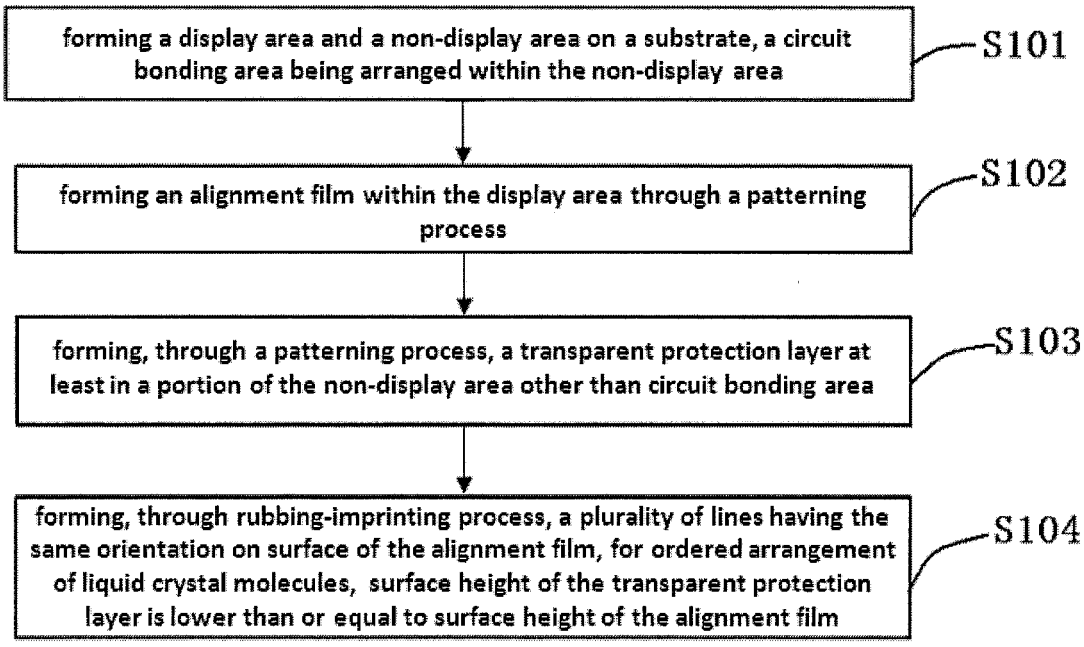
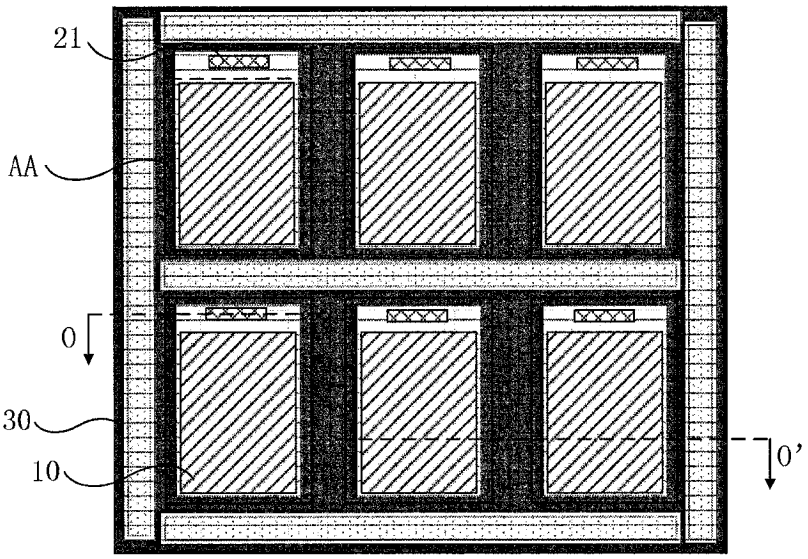

forming a display area and a non-display area on a substrate, a circuit bonding area being arranged within the non-display area
S101
forming an alignment film within the display area through a patterning process
S102
forming, through a patterning process, a transparent protection layer at least in a portion of the non-display area other than circuit bonding area
S103
forming, through rubbing-imprinting process, a plurality of lines having the same orientation on surface of the alignment film, for ordered arrangement of liquid crystal molecules, surface height of the transparent protection layer is lower than or equal to surface height of the alignment film
S104

Fig. 2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AA
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Fig. 3

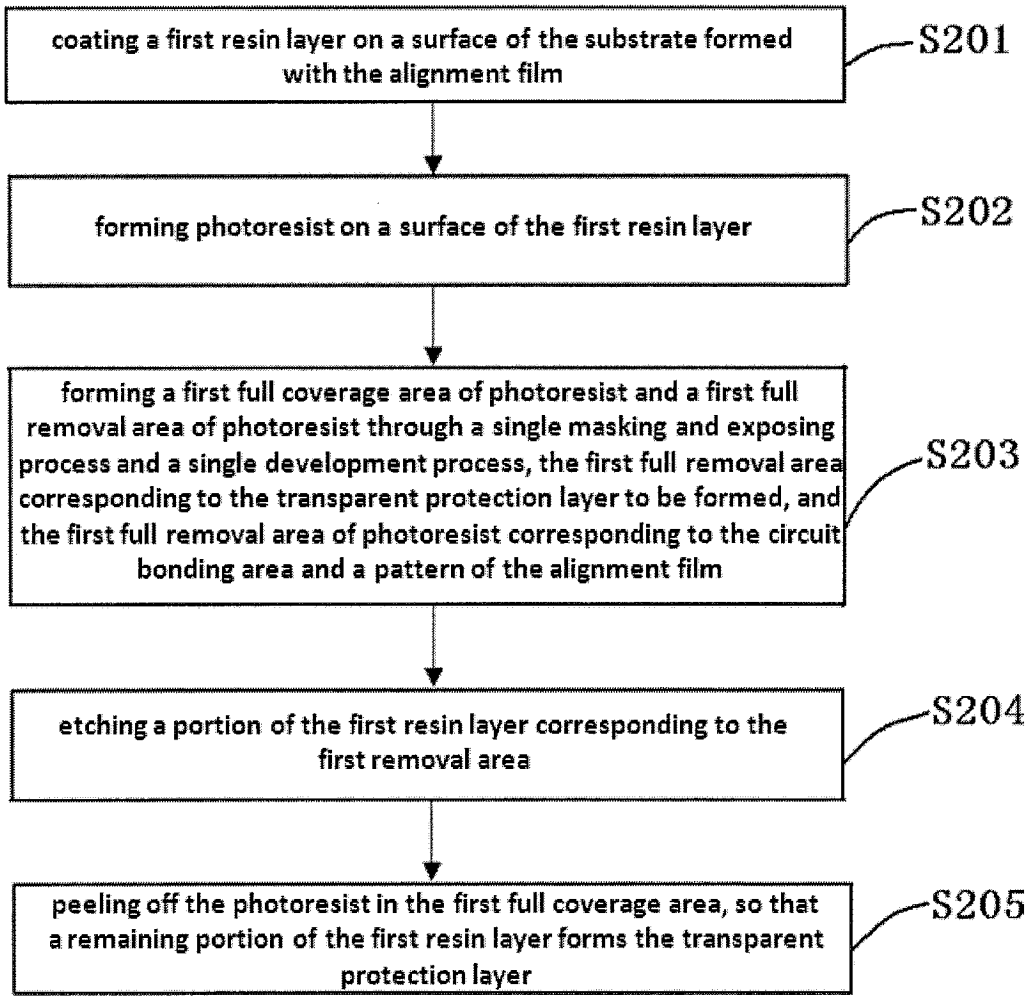
coating a first resin layer on a surface of the substrate formed with the alignment film
S201
forming photoresist on a surface of the first resin layer
S202
forming a first full coverage area of photoresist and a first full removal area of photoresist through a single masking and exposing process and a single development process, the first full removal area corresponding to the transparent protection layer to be formed, and the first full removal area of photoresist corresponding to the circuit bonding area and a pattern of the alignment film
S203
etching a portion of the first resin layer corresponding to the first removal area
S204
peeling off the photoresist in the first full coverage area, so that a remaining portion of the first resin layer forms the transparent protection layer
S205

Fig. 4

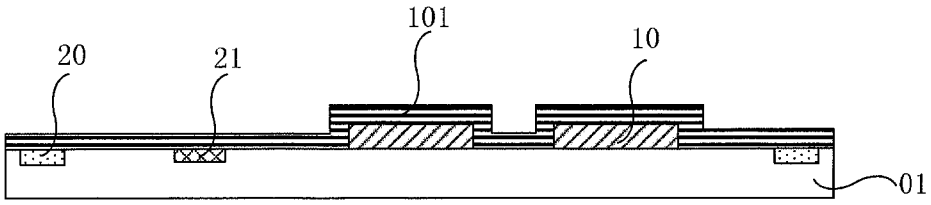

Fig. 5a

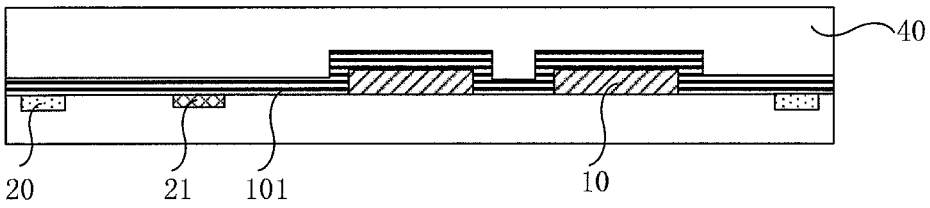

Fig. 5b

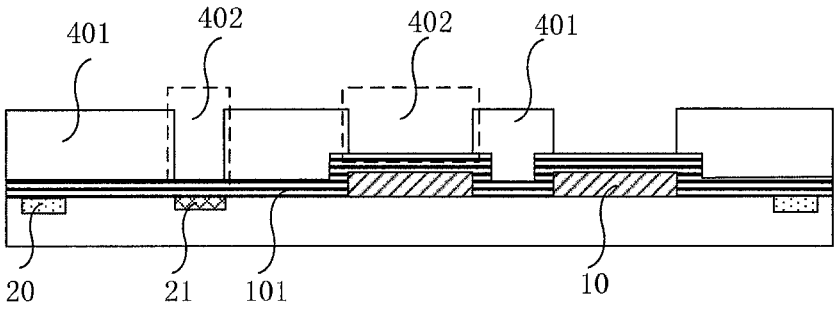

Fig. 5c

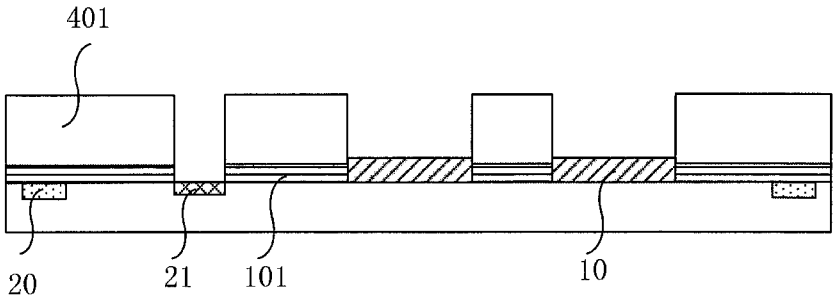

Fig. 5d

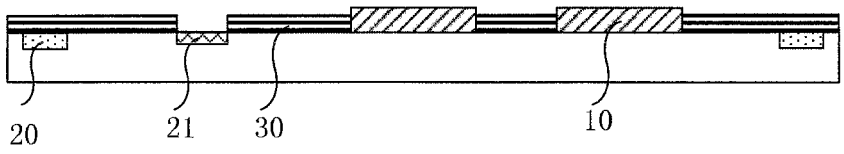
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Fig. 5e

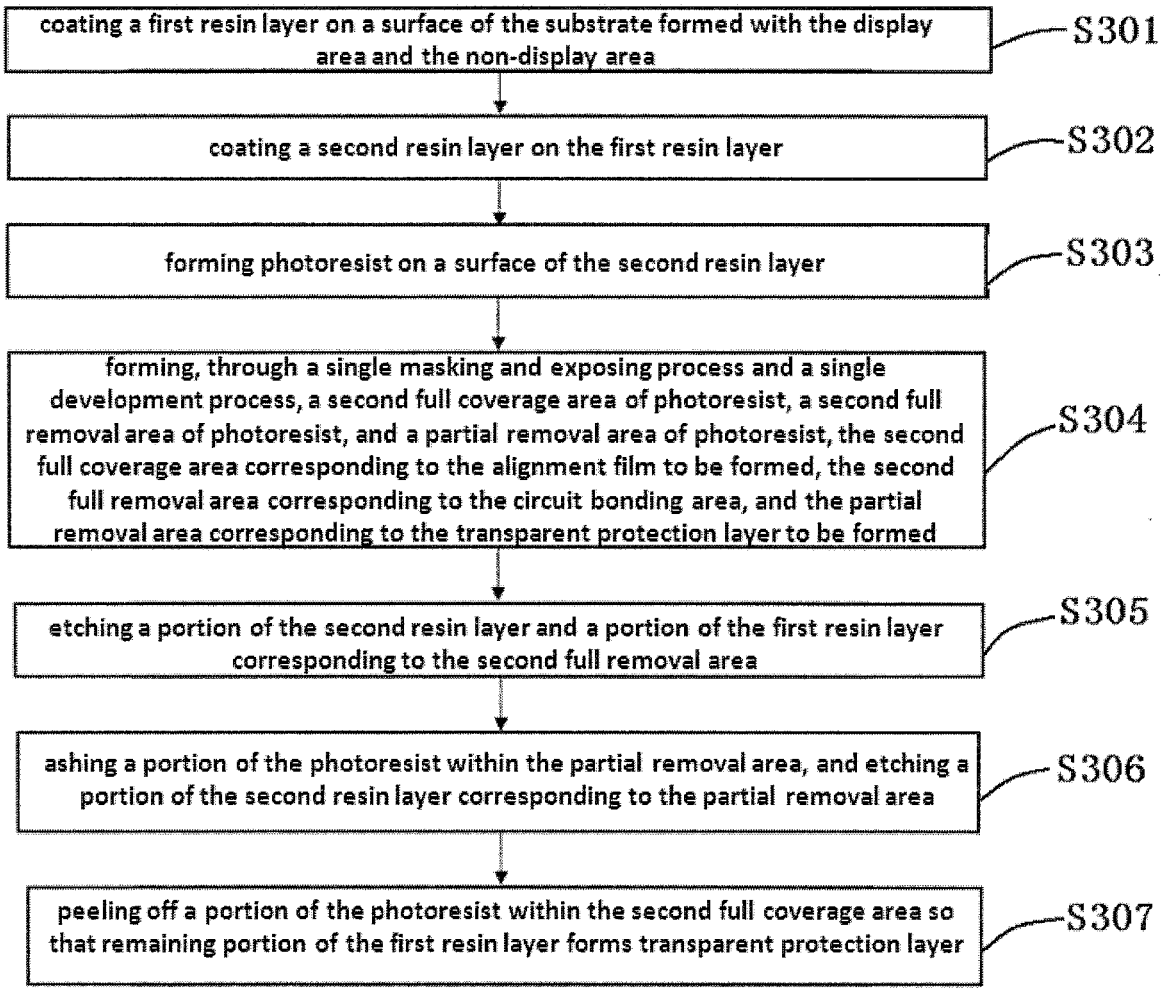
coating a first resin layer on a surface of the substrate formed with the display area and the non-display area
S301
coating a second resin layer on the first resin layer
S302
forming photoresist on a surface of the second resin layer
S303
forming, through a single masking and exposing process and a single development process, a second full coverage area of photoresist, a second full removal area of photoresist, and a partial removal area of photoresist, the second full coverage area corresponding to the alignment film to be formed, the second full removal area corresponding to the circuit bonding area, and the partial removal area corresponding to the transparent protection layer to be formed
S304
etching a portion of the second resin layer and a portion of the first resin layer corresponding to the second full removal area
S305
ashing a portion of the photoresist within the partial removal area, and etching a portion of the second resin layer corresponding to the partial removal area
S306
peeling off a portion of the photoresist within the second full coverage area so that remaining portion of the first resin layer forms transparent protection layer
S307

Fig. 6

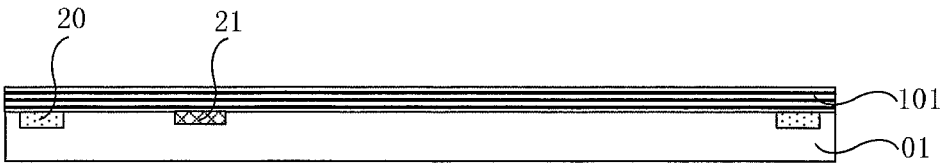

Fig. 7a

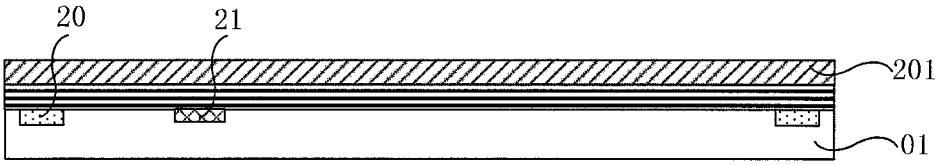

Fig. 7b

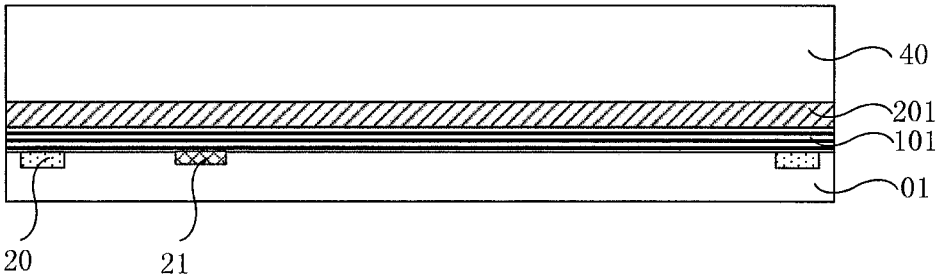

Fig. 7c

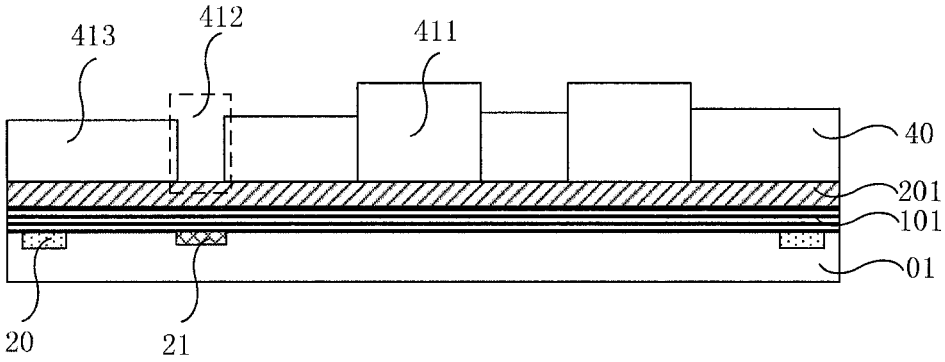

Fig. 7d

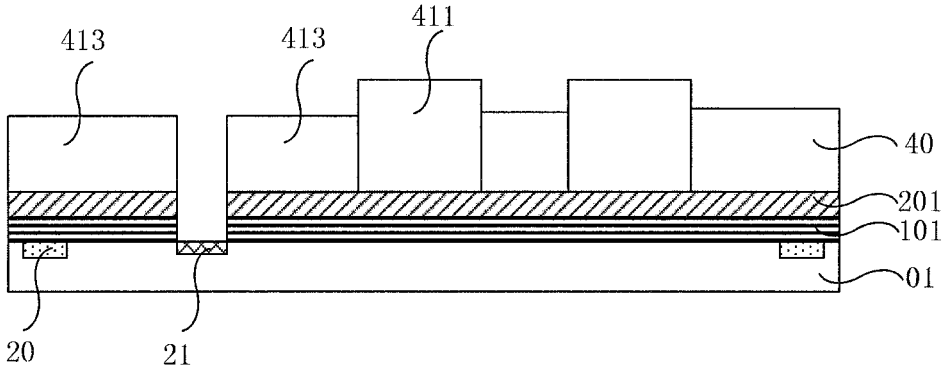

Fig. 7e

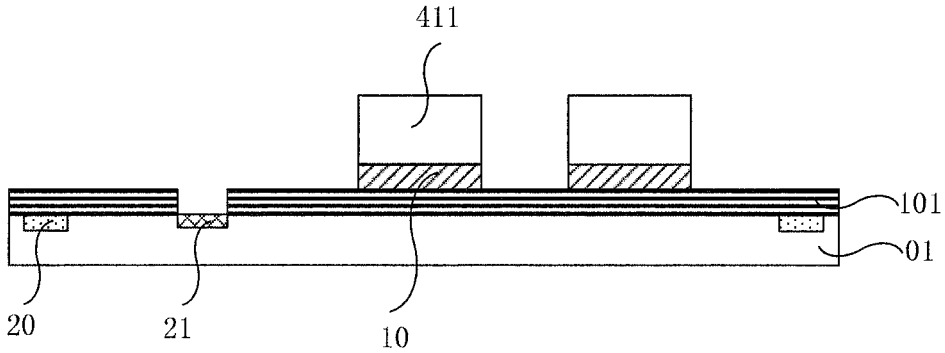

Fig. 7f

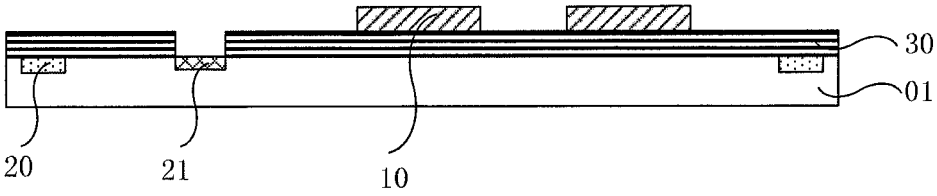

Fig. 7g

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/079442

A. CLASSIFICATION OF SUBJECT MATTER

G02F 1/1337 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI, CNPAT, WPI, EPODOC: liquid w crystal, orient+, align+, friction, non w display, peripheral, scrap+, protect+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 104280958 A (BOE TECHNOLOGY GROUP CO LTD et al.) 14 January 2015 (14.01.2015) description, paragraphs [0029]-[0075] and figures 1-7	1-11
PX	CN 104166273 A (BOE TECHNOLOGY GROUP CO LTD et al.) 26 November 2014 (26.11.2014) description, paragraphs [0028]-[0038] and figure 3	1, 5-7, 9-11
X	CN 101211068 A (QUNKANG TECH SHENZHEN CO LTD) 02 July 2008 (02.07.2008) description, page 1, line 8 to page 2, line 25 and figures 1-3	1, 5-7, 9-11
A	CN 101191935 A (QUNKANG TECH SHENZHEN CO LTD) 04 June 2008 (04.06.2008) the whole document	1-11
A	CN 102455548 A (LG DISPLAY CO LTD) 16 May 2012 (16.05.2012) the whole document	1-11
A	JP 2005164733 A (OPTREX KK. et al.) 23 June 2005 (23.06.2005) the whole document	1-11

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 July 2015	15 July 2015
Name and mailing address of the ISA State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No. (86-10) 62019451	Authorized officer LI, Yulin Telephone No. (86-10) 82245113

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2015/079442

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN 104280958 A	14 January 2015	None	
CN 104166273 A	26 November 2014	None	
CN 101211068 A	02 July 2008	CN 100582897 C	20 January 2010
CN 101191935 A	04 June 2008	None	
CN 102455548 A	16 May 2012	KR 20120039871 A	26 April 2012
		CN 102455548 B	13 May 2015
		TW 1464490 B	11 December 2014
		KR 101300034 B1	29 August 2013
		US 2012092599 A1	19 April 2012
		TW 201232117 A	01 August 2012
		US 9046715 B2	02 June 2015
JP 2005164733 A	23 June 2005	None	

Form PCT/ISA /210 (patent family annex) (July 2009)

专利名称(译)	阵列基板，其制造方法和显示装置		
公开(公告)号	EP3200021A1	公开(公告)日	2017-08-02
申请号	EP2015763811	申请日	2015-05-21
[标]申请(专利权)人(译)	京东方科技集团股份有限公司 北京京东方光电科技有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司. 北京京东方光电科技有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司. 北京京东方光电科技有限公司.		
[标]发明人	DONG TINGZE WANG YUJIA MO JUN GUAN PEIQIANG ZHANG ZHINAN		
发明人	DONG, TINGZE WANG, YUJIA MO, JUN GUAN, PEIQIANG ZHANG, ZHINAN		
IPC分类号	G02F1/1337		
CPC分类号	G02F1/13378 G02F1/133345 G02F1/133784 G02F2201/50 G02F1/133514 G02F1/134309 G02F1/136286 G02F2001/133792 G02F2201/121 G02F2201/123		
代理机构(译)	POTTER CLARKSON LLP		
优先权	201410505653.5 2014-09-26 CN		
其他公开文献	EP3200021B1 EP3200021A4		
外部链接	Espacenet		

摘要(译)

公开了一种阵列基板，制造阵列基板的方法和显示装置，用于消除在单元处理期间产生的白色Mura缺陷。该方法包括以下步骤：在基板上形成显示区域和非显示区域，电路接合区域布置在非显示区域内;通过构图工艺在显示区域内形成取向膜;通过图案化工艺形成至少在除电路接合区域之外的非显示区域的一部分中的透明保护层;通过摩擦压印工艺，在取向膜表面上形成多条具有相同取向的线，用于液晶分子的有序排列，其中透明保护层的表面高度小于或等于取向膜的表面高度。

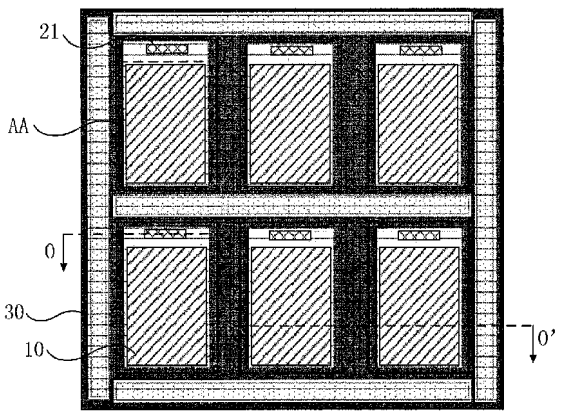

Fig. 3