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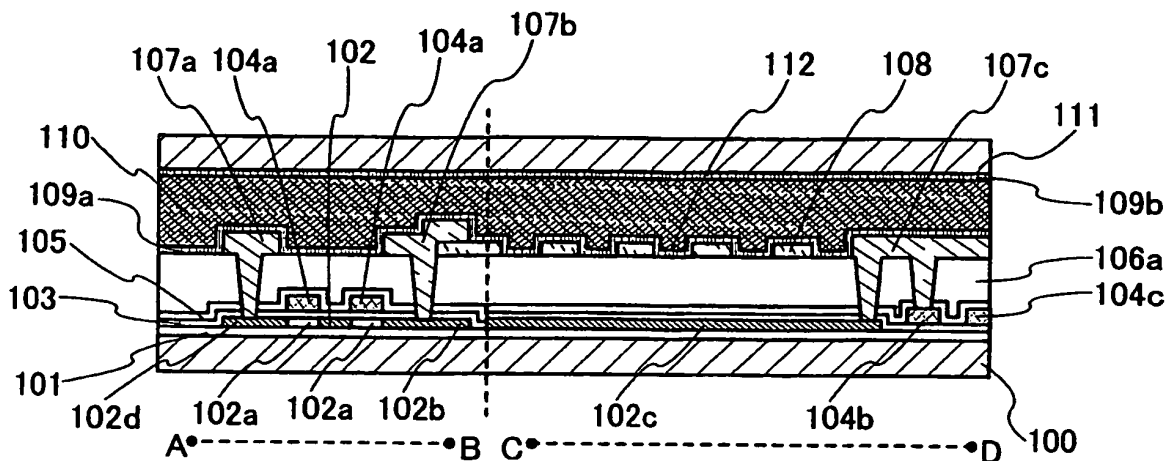
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(54) **Liquid crystal display device, semiconductor device, and electronic appliance**

(57) The liquid crystal display device includes an island-shaped first semiconductor film 102 which is formed over a base insulating film 101 and in which a source 102d, a channel forming region 102a, and a drain 102b are formed; a first electrode 102c which is formed of a material same as the first semiconductor film 102 to be the source 102d or the drain 102b and formed over the base insulating film 101; a second electrode 108 which

is formed over the first electrode 102c and includes a first opening pattern 112; and a liquid crystal 110 which is provided over the second electrode 108. The electrical contact between the drain electrode (102b) and the second electrode is provided by a conductive film (107b) which is on and in contact with the second electrode (108).

**FIG. 19A**



## Description

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

**[0001]** The present invention relates to a semiconductor device, a liquid crystal display device, and an electronic appliance including them. In particular, the present invention relates to a semiconductor device and a liquid crystal display device in which an electric field generally parallel to a substrate is generated to control liquid crystal molecules, and an electronic appliance including the semiconductor device or the liquid crystal display device.

#### 2. Description of the Related Art

**[0002]** As one of plans for technical development of a liquid crystal display device, to widen a viewing angle can be given. As a technique for realizing a wide viewing angle, a mode in which an electric field generally parallel to a substrate is generated and liquid crystal molecules are moved in a plane parallel to the substrate to control grayscale is employed. As such a mode, IPS (In-Plane Switching) and FFS (Fringe-Field Switching) are given. In these modes, a first electrode (such as a pixel electrode with which voltage is controlled for each pixel) having a slit (an opening pattern) is located under a liquid crystal and a second electrode (such as a common electrode with which common voltage is applied to all pixels) is located under the first electrode. An electric field is applied between the pixel electrode and the common electrode, so that the liquid crystal is controlled. With such layout, an electric field in a direction parallel to a substrate is applied to the liquid crystal. Therefore, the liquid crystal molecules can be controlled with the electric field. That is, the liquid crystal molecules which are aligned parallel to the substrate (so called homogeneous alignment) can be controlled in a direction parallel to the substrate; therefore, viewing angle is increased.

**[0003]** Conventionally, both common electrode and pixel electrode are formed of ITO (indium tin oxide) (Patent Document 1: Japanese Published Patent Application No. 2000-89255 (FIG 5 and 14th paragraph)).

### SUMMARY OF THE INVENTION

**[0004]** As described above, in the case of employing a structure in which the second electrode (such as the common electrode) is located under the first electrode (such as the pixel electrode), both the common electrode and the pixel electrode are formed of ITO conventionally. Accordingly, the numbers of manufacturing steps and masks, and manufacturing cost have been increased. The present invention is made in view of the foregoing, and an object of the present invention is to provide a liquid crystal display device and an electronic appliance with wide viewing angle, having less numbers of manu-

facturing steps and masks and low manufacturing cost compared with a conventional device; and to provide a manufacturing method of the liquid crystal display device.

**[0005]** To solve the aforementioned problems, a liquid crystal display device according to the present invention includes a first electrode formed over a substrate, an insulating film formed over the first electrode, a second electrode formed over the insulating film, and a liquid crystal provided over the second electrode; in which the second electrode has an opening pattern and the first electrode has a semiconductor film containing silicon.

**[0006]** A semiconductor device according to the present invention includes a first electrode formed over a substrate, an insulating film formed over the first electrode, and a second electrode formed over the insulating film; in which the second electrode has an opening pattern and the first electrode has a semiconductor film containing silicon

**[0007]** A liquid crystal display device according to the present invention includes a first electrode formed over a substrate, an insulating film formed over the first electrode, a second electrode formed over the insulating film, a liquid crystal provided over the second electrode, and a transistor formed over the substrate; in which the second electrode has an opening pattern, the first electrode has a semiconductor film containing silicon, the transistor has a semiconductor film containing silicon, and the semiconductor film included in the first electrode is formed at the same time as the semiconductor film included in the transistor.

**[0008]** A semiconductor device according to the present invention includes a first electrode formed over a substrate, an insulating film formed over the first electrode, a second electrode formed over the insulating film, and a transistor formed over the substrate; in which the second electrode has an opening pattern, the first electrode has a semiconductor film containing silicon, the transistor has a semiconductor film containing silicon, and the semiconductor film included in the first electrode is formed at the same time as the semiconductor film included in the transistor.

**[0009]** In the liquid crystal display device and the semiconductor device, the first electrode and the semiconductor film included in the transistor are formed at the same time, and then, etched and patterned at the same time. Accordingly, the first electrode and the semiconductor film included in the transistor contain the same material. In addition, an n-type impurity or a p-type impurity is introduced thereto at the same time in some cases. In such a case, they have a portion with approximately the same concentration of the impurity. Note that the transistor includes a portion to which the impurity is introduced, a portion to which the impurity is slightly introduced, a portion to which the impurity is hardly introduced, and the like. The first electrode is generally in the same states as the portion in the semiconductor film included in the transistor, to which the impurity is introduced in many cases. Thus, the first electrode can be formed

at the same time as the transistor. Therefore, an additional step is not required to form the first electrode. In addition, a liquid crystal display device with wide viewing angle and low manufacturing cost compared with a conventional device can be provided.

**[0010]** Note that the opening pattern includes not only a closed opening pattern such as a slit, but also a space which is located between the conductive patterns and in which the conductive pattern is not formed, such as a space between the comb-teeth of a comb-shaped electrode. The same can be applied to description hereinafter.

**[0011]** Note that in the aforementioned liquid crystal display device and the semiconductor device, a portion in which first and second interlayer insulating films are provided between the first electrode and the second electrode, and the second electrode and the first electrode except for the opening pattern are overlapped each other the first electrode; the first interlayer insulating film, and the second electrode can function as a capacitor. In this case, storage capacitance can be increased. Therefore, when a thin film transistor is turned off, the potential of the pixel electrode can be easily kept.

**[0012]** A liquid crystal display device according to the present invention includes a first electrode formed over a substrate, an insulating film formed over the first electrode, a second electrode formed over the insulating film, a liquid crystal provided over the second electrode, and a transistor formed over the substrate; in which the second electrode includes an opening pattern, the first electrode includes a semiconductor film containing silicon, the semiconductor film included in the first electrode is formed at the same time as the semiconductor film included in the transistor, and the semiconductor film included in the first electrode and the semiconductor film included in the transistor contain an impurity having the same conductivity type.

**[0013]** A semiconductor device according to the present invention includes a first electrode formed over a substrate, an insulating film formed over the first electrode, a second electrode formed over the insulating film, and a transistor formed over the substrate; in which the second electrode includes opening pattern, the first electrode includes a semiconductor film containing silicon, the semiconductor film included in the first electrode is formed at the same time as the semiconductor film included in the transistor, and the semiconductor film included in the first electrode and the semiconductor film included in the transistor contain an impurity having the same conductivity type.

**[0014]** When the first electrode and the transistor contain the impurity having the same conductivity type (such as an n-type or a p-type), the layout can be efficient. Accordingly, the aperture ratio can be improved.

**[0015]** A liquid crystal display device according to the present invention includes a transistor formed over a substrate, a semiconductor film formed in the transistor, a first electrode formed by a part of the semiconductor film,

an insulating film formed over the first electrode, a second electrode formed over the insulating film, and a liquid crystal provided over the second electrode; in which the second electrode includes an opening pattern.

**[0016]** A semiconductor device according to the present invention includes a transistor formed over a substrate, a semiconductor film formed in the transistor, a first electrode formed by a part of the semiconductor film, an insulating film formed over the first electrode, and a second electrode formed over the insulating film; in which the second electrode includes an opening pattern.

**[0017]** When the first electrode and the semiconductor film included in the transistor are formed in one island as described above, the layout can be efficient. Accordingly, the aperture ratio can be improved.

**[0018]** In the aforementioned structure of the liquid crystal display device according to the present invention, the first electrode is a pixel electrode and the second electrode is a common electrode.

**[0019]** In the aforementioned structure of the semiconductor device according to the present invention, the first electrode is a pixel electrode and the second electrode is a common electrode.

**[0020]** In the aforementioned structure of the liquid crystal display device according to the present invention, the first electrode is a common electrode and the second electrode is a pixel electrode.

**[0021]** In the aforementioned structure of the semiconductor device according to the present invention, the first electrode is a common electrode and the second electrode is a pixel electrode.

**[0022]** In the aforementioned structure of the liquid crystal display device according to the present invention, orientation of the liquid crystal is controlled by an electric field between the first electrode and the second electrode.

**[0023]** Note that a switch shown in the present invention may be any switch such as an electrical switch or a mechanical switch. That is, as long as current flow can be controlled, any type of switch can be used without being limited to a particular type. For example, a transistor, a diode (such as a PN diode, a PIN diode, a Schottky diode, or a diode-connected transistor), or a logic circuit that is a combination thereof may be used. In the case of using a transistor as a switch, a polarity (conductivity) type of the transistor is not particularly limited because it operates as a mere switch. However, when off current is preferred to be small, a transistor of a polarity with smaller off current is desirably used. As a transistor with small off current, a transistor having an LDD region, a transistor having a multigate structure, and the like are given. Further, an N-channel transistor is desirably used when a potential of a source terminal of the transistor functioning as a switch is close to a low potential side power source (Vss, GND, 0V, or the like). On the other hand, a P-channel transistor is desirably used when the potential of the source terminal is close to a high potential side power source (Vdd or the like). This is because it is

easy for a transistor to function as a switch when an absolute value of a gate-source voltage is increased. Note that a CMOS switch can also be applied by using both N-channel and P-channel transistors. With a CMOS switch, an operation can be appropriately performed even when the situation changes such that a voltage outputted through the switch (that is, an input voltage) is higher or lower than an output voltage. Although as a switch in the present invention, a TFT controlling a pixel electrode, a switch element used in a driver circuit portion, and the like are given; a switch can be employed in another part, if current flow is required to be controlled.

**[0024]** In the present invention, "being connected" includes "being electrically connected" and "being directly connected". Here, "being electrically connected" refers to a state in which an element capable of electric connection (such as a switch, a transistor, a capacitor, an inductor a resistor, or a diode) may be interposed in the predetermined connection. In addition, "being directly connected" refers to only a specific case of "being electrically connected", where no element capable of electric connection is interposed and direct connection is achieved. That is, "being directly connected" specifically refers to "being electrically connected" without another element interposed in the predetermined connection. Note that the description "being directly connected" means the same as "being connected in a direct manner" is also used.

**[0025]** Note that a display element, a display device, and a light emitting device can employ various modes or can include various elements. For example, a display medium whose contrast varies by an electromagnetic action can be used, such as an EL element (an organic EL element, an inorganic EL element, or an EL element including organic and inorganic substances), an electron emitting element, a liquid crystal element, electron ink, a grating light valve (GLV), a plasma display panel (PDP), a digital micromirror device (DMD), a piezoceramic display, or a carbon nanotube. Note that a display device using an EL element includes an EL display; a display device using an electron emitting element includes a field emission display (FED), an SED flat panel display (SED: Surface-conduction Electron-emitter Display), and the like; a display device using a liquid crystal element includes a liquid crystal display, a transmissive liquid crystal display, a transreflective liquid crystal display, and a reflective liquid crystal display; and a display device using electronic ink includes electronic paper. As an application of the present invention other than a liquid crystal element, for example, an electrode containing silicon is used for an electrode in an EL element and the like. Therefore, an element such as an EL element can be manufactured at low cost. In this case, an electrode may have an opening pattern, but not necessarily. When an electrode containing silicon of the present invention is used in an organic EL element, a structure in which a layer containing an organic compound is interposed between electrodes is favorably employed, but not necessarily. On the other

hand, when the electrode containing silicon of the present invention is used in an inorganic EL element, a structure in which a layer containing an inorganic compound is interposed between electrodes may be employed, or a structure in which a layer containing an inorganic compound is formed over the electrode may be employed; since AC drive is possible in the inorganic EL element. In the latter structure, light emission can be carried out with use of a lateral electric field formed by a first electrode and a second electrode. With such a structure, a component which attenuates light from the electrode or the like is not necessarily provided on a light emitting side, accordingly, luminance of the EL display device is improved and deterioration of the EL display device is suppressed.

**[0026]** Note that various types of transistors can be applied to the present invention and an applicable type of the transistor is not limited. Accordingly, the present invention can employ a thin film transistor (TFT) using a non-single crystalline semiconductor film typified by amorphous silicon or polycrystalline silicon, a transistor using a semiconductor substrate or an SOI substrate, a MOS transistor, a junction transistor, a bipolar transistor, a transistor using a compound semiconductor such as ZnO or a-InGaZnO, a transistor using an organic semiconductor or a carbon nanotube, and the like. In addition, a type of substrate on which a transistor is provided is not particularly limited. The transistor can be formed on a single crystalline substrate, an SOI substrate, a glass substrate, a plastic substrate, a paper substrate, a cellophane substrate, a stone substrate, or the like. In addition, after forming a transistor over a substrate, the transistors may be transposed to another substrate to be located thereon.

**[0027]** Note that as described above, in the present invention, various types of transistor can be used and can be formed over any substrate. Therefore, all circuits may be formed over a glass substrate, a plastic substrate, a single crystalline substrate, an SOI circuit, or any other circuit. When all circuits are formed on one substrate, the cost can be reduced by reducing the number of components and the reliability can be improved by reducing the number of connection to components in the circuits. Alternatively, it is possible that some circuits are formed on a substrate and some other circuits are formed on another substrate. That is, all of the circuits are not necessarily formed over one substrate. For example, some circuits are formed over a glass substrate with a use of a transistor while some other circuits are formed over a single crystalline substrate, and the IC chip may be connected to the glass substrate by COG (Chip On Glass) to be located thereover. Alternatively, the IC chip may be connected to the glass substrate by TAB (Tape Auto Bonding) or by using a printed board. In this manner, when some circuits are formed over one substrate, the cost can be reduced by reducing the number of components and the reliability can be improved by reducing the number of connection to components in the circuits. Fur-

ther, when portions with high drive voltage or high drive frequency, which consume more power, are not formed on one substrate, increase in power consumption can be prevented.

**[0028]** It is to be noted that a transistor can have various structures and modes, and is not limited to a specific structure. For example, a multigate structure which has two or more gates may be employed as well. With a multigate structure, off current can be reduced and reliability can be improved by improving the pressure resistance of a transistor, and flat characteristics can be obtained such that a drain-source current hardly changes even when a drain-source voltage changes in operation in a saturation region. Alternatively, a structure in which gate electrodes may be provided over and under a channel may be employed. With such a structure in which gate electrodes are provided over and under a channel, a current value can be easily increased since a channel forming region increases, an S value (sub-threshold coefficient) can be reduced since a depletion layer is easily formed. Further alternatively, a structure in which a gate electrode is provided over a channel or under the channel may be employed. Also, a forward staggered structure or an inverted staggered structure may be employed. A channel forming region may be divided into a plurality of regions, connected in parallel, or connected in series. Further, a source electrode or a drain electrode may overlap with a channel (or a part thereof). Accordingly, with such a structure in which a source electrode or a drain electrode overlaps with a channel (or a part of thereof), charges are accumulated in a part of the channel and an unstable operation can be prevented. Further, an LDD region may be provided. By providing an LDD region, off current can be reduced and reliability can be improved by improving the withstand voltage of a transistor, and flat characteristics can be obtained such that a drain-source current hardly changes even when a drain-source voltage changes in operation in a saturation region.

**[0029]** Note that in the present invention, one pixel corresponds to one element which can control brightness. Therefore, for example, one pixel shows one color element by which brightness is expressed. Accordingly, in the case of a color display device formed of color elements of R (red), G (green), and B (blue), the smallest unit of an image includes three pixels of an R pixel, a G pixel, and a B pixel. Note that color elements are not limited to three colors and may be more colors, and RGBW (W is white) or RGB to which another color such as yellow, cyan, or magenta is introduced may be used, for example. Further, when one color element is controlled by using a plurality of regions, one of the regions corresponds to one pixel. For example, in the case of performing an area gray scale display, a plurality of regions are provided for one color element to control the brightness, which express gray scale as a whole. One of the regions to control the brightness corresponds to one pixel. Therefore, in that case, one color element includes a plurality of pixels. In that case, a region which contributes to dis-

play an image may differ in size depending on the pixels. Further, in a plurality of regions controlling the brightness which are provided for one color element, that is, in a plurality of pixels included in one color element, signals provided to each pixel may slightly differ from one another so that the viewing angle is expanded. Note that the description "one pixel (for three colors)" corresponds to three pixels of R, G, and B which are considered as one pixel; while "one pixel (for one color)" corresponds to a plurality of pixels provided for one color element which are collectively considered as one pixel.

**[0030]** Note that in the present invention, there is a case where pixels are arranged in matrix. The case where pixels are arranged in matrix includes not only to a case where the pixels are arranged in a stripe pattern, which is a so-called grid configuration where longitudinal stripes and lateral stripes cross each other, but also to a case where three color elements are arranged in a so-called delta pattern when a full color display is performed using three color elements (for example, RGB). Further, a Bayer arrangement is also included. Note that the color element is not limited to three colors and may have more colors, for example, RGBW (W is white) or RGB to which yellow, cyan, or magenta is added. The size of a light emission area may be different depending on color elements.

**[0031]** A transistor is an element including at least three terminals of a gate, a drain, and a source. A channel forming region is provided between a drain region and a source region. Here, it is difficult to determine which of two terminals is a source or a drain since it depends on a structure, operating condition, and the like of the transistor. Therefore, in the present invention, regions which function as a source and a drain are referred to as a first terminal and a second terminal, respectively.

**[0032]** Note that a gate includes a gate electrode and a gate wiring (also referred to as a gate line, a gate signal line, or the like) or a part thereof. A gate electrode corresponds to a conductive film a part of which overlaps with a semiconductor forming a channel forming region, an LDD (Lightly Doped Drain) region, or the like, with a gate insulating film interposed therebetween. A gate wiring corresponds to a wiring for connecting gate electrodes of each pixel and a wiring for connecting a gate electrode and another wiring.

**[0033]** However, there is a part which functions as a gate electrode and also as a gate wiring. Such a region may be referred to as a gate electrode or a gate wiring. That is, there is a region which cannot be distinguished as a gate electrode or a gate wiring. For example, in a case where a channel forming region overlaps with a gate wiring which is extended, the overlapped region functions both as a gate wiring and as a gate electrode. Therefore, such a region may be referred to as a gate electrode or a gate wiring.

**[0034]** Further, a region which is formed of the same material as a gate electrode and connected to the gate electrode may be referred to as a gate electrode as well.

Similarly, a region which is formed of the same material as a gate wiring and connected to the gate wiring may be referred to as a gate wiring. In a strict sense, such a region does not overlap with a channel forming region or does not have a function to connect to another gate electrode in some cases. However, there is a region which is formed of the same material as a gate electrode or a gate wiring and connected to the gate electrode or the gate wiring due to manufacturing cost, reduction of steps, layout, and the like. Therefore, such a region may also be referred to as a gate electrode or a gate wiring.

**[0035]** For example, in a multigate transistor, gate electrodes of one transistor and another transistor are often connected through a conductive film formed of the same material as the gate electrode. Such a region for connecting the gate electrodes may be referred to as a gate wiring, or may be referred to as a gate electrode when a multigate transistor is considered as one transistor. That is, a component which is formed of the same material as a gate electrode or a gate wiring and connected to the gate electrode or the gate wiring may be referred to as a gate electrode or a gate wiring. Moreover, for example, a portion of a conductive film which connects a gate electrode and a gate wiring may also be referred to as a gate electrode or a gate wiring.

**[0036]** Note that a gate terminal corresponds to a part of a region of a gate electrode or a region electrically connected to the gate electrode.

**[0037]** Note that a source includes a source region, a source electrode, and a source wiring (also referred to as a source line, a source signal line, or the like) or a part thereof. A source region corresponds to a semiconductor region which contains a large amount of p-type impurities (boron, gallium, or the like) or n-type impurities (phosphorus, arsenic, or the like). Therefore, a region containing a small amount of p-type impurities or n-type impurities, that is, an LDD (Lightly Doped Drain) region is not included in a source region. A source electrode corresponds to a conductive layer a part of which is formed of a different material from a source region and electrically connected to the source region. Note that a source electrode including a source region is sometimes referred to as a source electrode. A source wiring corresponds to a wiring for connecting source electrodes of each pixel and a wiring for connecting a source electrode and another wiring.

**[0038]** However, there is a part which functions as a source electrode and also as a source wiring. Such a region may be referred to as a source electrode or a source wiring. That is, there is a region which cannot be distinguished as a source electrode or a source wiring. For example, when there is a source region overlapping with a source wiring which is extended, the region functions as a source wiring and also as a source electrode. Therefore, such a region may be referred to as a source electrode or a source wiring.

**[0039]** Further, a region which is formed of the same material as a source electrode and connected to the

source electrode; or a part which connects one source electrode and another source electrode may also be referred to as a source electrode. Further, a part overlapping with a source region may be referred to as a source electrode. Similarly, a region which is formed of the same material as a source wiring and connected to the source wiring may be referred to as a source wiring. In a strict sense, there is a case where such a region does not have a function to connect one source electrode to another source electrode. However, there is a region which is formed of the same material as a source electrode or a source wiring and connected to the source electrode or the source wiring due to manufacturing cost, reduction of steps, layout, and the like. Therefore, such a region may also be referred to as a source electrode or a source wiring.

**[0040]** For example, a conductive film a part of which connects a source electrode and a source wiring may be referred to as a source electrode or a source wiring.

**[0041]** Note that a source terminal corresponds to a part of a source region, a source electrode, or a region electrically connected to a source electrode.

**[0042]** Note that a drain is similar to a source.

**[0043]** Note that in the present invention, a semiconductor device corresponds to a device including a circuit having a semiconductor element (a transistor, a diode, or the like). Further, a semiconductor device may correspond to a general device which functions by utilizing semiconductor characteristics. A display device corresponds to a device including a display element (a liquid crystal element, a light emitting element, or the like). Note that a display device may correspond to a display panel itself in which a plurality of pixels including display elements such as a liquid crystal element or an EL element and a peripheral driver circuit for driving the pixels are formed over a substrate. Moreover, a display device may include a device provided with a flexible printed circuit (FPC) or a printed wiring board (PWB). Further, a light emitting device corresponds to a display device including a self-luminous light emitting element such as an EL element or an element used for an FED, in particular. A liquid crystal display device corresponds to a display device including a liquid crystal element.

**[0044]** In the present invention, an expression that an object is formed on or formed over a different object does not necessarily mean that the object is in direct contact with the different object. The expression may include a case where two objects are not in direct contact with each other, that is, a case where another object is interposed therebetween. Accordingly, for example, when it is described that a layer B is formed on (or over) a layer A, it means either case where the layer B is formed on and in direct contact with the layer A, or where another layer (for example, a layer C or a layer D) is formed on and in direct contact with the layer A and the layer B is formed on and in direct contact with the layer C or D. Similarly, when it is described that an object is formed above a different object, it does not necessarily mean that the

object is in direct contact with the different object, and another object may be interposed therebetween. Accordingly, for example, when it is described that a layer B is formed above a layer A, it means either case where the layer B is formed in direct contact with the layer A, or where another layer (for example, a layer C or a layer D) is formed in direct contact with the layer A and the layer B is formed in direct contact with the layer C or D. Similarly, when it is described that an object is formed below or formed under a different object, it means either case where the objects are in direct contact with each other or not in contact with each other. In addition, if not specifically limited, one surface of a substrate is referred to as an upper direction, and the other surface of the substrate is referred to as a lower direction. That is, in a case where a layer B is formed over a layer A in manufacturing steps, its structure can be considered as a structure where the layer B is formed over the layer A, even when a completed product is turned upside down. That is, an expression over or under only refers to a side of an object to which another object is formed, and does not have a general meaning of over or under, which is "a direction with respect to gravity". Needless to say, similar description can be applied to other directions such as left or right. Note that it is not limited thereto when it is particularly specified, and the direction of gravity or the like may be employed as a standard.

**[0045]** With the present invention, a semiconductor film in a transistor and a first electrode for driving a liquid crystal can be formed in the same step. As a result, the first electrode can be manufactured without increasing the numbers of masks (reticles) and manufacturing steps.

**[0046]** Accordingly, a liquid crystal display device with wide viewing angle and low manufacturing cost compared with a conventional device can be provided.

## BRIEF DESCRIPTION OF DRAWINGS

**[0047]**

FIG. 1A is a plan view for illustrating a structure of a liquid crystal display device according to the present invention, and FIG. 1B is a cross-sectional view along a line A-B of FIG. 1A;

FIG. 2A is a plan view for illustrating a structure of a liquid crystal display device according to the present invention, and FIG. 2B is a cross-sectional view along a line A-B of FIG. 2A;

FIG. 3A is a plan view for illustrating a structure of a liquid crystal display device according to the present invention, and FIG. 3B is a cross-sectional view along a line A-B of FIG. 3A;

FIG. 4A is a plan view for illustrating a structure of a liquid crystal display device according to the present invention, and FIG. 4B is a cross-sectional view along a line A-B of FIG. 4A;

FIG. 5A is a plan view for illustrating a structure of a

liquid crystal display device according to the present invention, and FIG. 5B is a cross-sectional view along a line A-B of FIG. 5A;

FIG. 6A is a plan view for illustrating a structure of a liquid crystal display device according to the present invention, and FIG. 6B is a cross-sectional view along a line A-B of FIG. 6A;

FIG. 7A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 1, and FIG. 7B is a cross-sectional view along lines A-B and C-D of FIG. 7A;

FIG. 8 illustrates another structure of FIG. 7B;

FIGS. 9A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 2, and FIG. 9B is a cross-sectional view along lines A-B and C-D of FIG. 9A;

FIG. 10A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 3, and FIG. 10B is a cross-sectional view along lines A-B, C-D, and E-F of FIG. 10A;

FIG. 11A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 4, and FIG. 11B is a cross-sectional view along lines A-B and C-D of FIG. 11A;

FIG. 12A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 5, and FIG. 12B is a cross-sectional view along lines A-B and C-D of FIG. 12A;

FIG. 13A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 6, and FIG. 13B is a cross-sectional view along lines A-B, C-D, and E-F of FIG. 13A;

FIG. 14A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 7, and FIG. 14B is a cross-sectional view along lines A-B, C-D, and E-F of FIG. 14A;

FIG. 15A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 8, and FIG. 15B is a cross-sectional view along lines A-B, C-D, and E-F of FIG. 15A;

FIG. 16A is a circuit diagram of a liquid crystal display device according to Embodiment Mode 9 and FIG. 16B is a circuit diagram of a liquid crystal display device according to Embodiment Mode 10;

FIG. 17A is a circuit diagram of a liquid crystal display device according to Embodiment Mode 11 and FIG. 17B is a circuit diagram of a liquid crystal display device according to Embodiment Mode 12;

FIG. 18A is a plan view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 13, and FIG. 18B is a cross-sectional view along lines A-B and C-D of FIG. 18A;

FIG. 19A is a cross-sectional view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 14, and FIG. 19B is a cross-sectional view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 15;

FIG 20 is a cross-sectional view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 16;

FIG 21A is a plan view of a liquid crystal display device shown in FIG 20 and FIG 21B is an enlarged view of a pixel portion of FIG 21A;

FIG 22A is a plan view of a liquid crystal display device according to Embodiment Mode 17 and FIG 22B is an enlarged view of a pixel portion of FIG 22A;

FIG 23 is a cross-sectional view for illustrating a structure of a liquid crystal display device according to Embodiment Mode 18;

FIGS. 24A to 24D are plan views for illustrating shapes of an electrode of an FFS mode liquid crystal display device according to Embodiment Mode 19; FIGS. 25A to 25D are plan views for illustrating shapes of an electrode of an IPS mode liquid crystal display device according to Embodiment Mode 20; FIGS. 26A to 26E are cross-sectional views illustrating a manufacturing method of a liquid crystal display module of Embodiment 1;

FIGS. 27A to 27D are cross-sectional views illustrating a manufacturing method of a liquid crystal display module of Embodiment 1;

FIG. 28A is a plan view of a liquid crystal display module of Embodiment 1 and FIG 28B is a cross-sectional view along a line K-L of FIG 28A;

FIGS. 29A and 29B are diagrams for illustrating a liquid crystal display module according to Embodiment 2;

FIGS. 30A and 30B are diagrams for illustrating a liquid crystal display module according to Embodiment 2;

FIGS. 31A to 31H are perspective views illustrating electronic appliances of Embodiment 3;

FIGS. 32A and 32B are cross-sectional views for illustrating a structure of an inorganic EL element according to Embodiment Mode 21;

FIG 33 is a cross-sectional view for illustrating a structure of an organic EL element according to Embodiment Mode 22; and

FIGS. 34A to 34D are cross-sectional views for illustrating a structure and manufacturing steps of a reflective liquid crystal display device according to Embodiment Mode 23.

## DETAILED DESCRIPTION OF THE INVENTION

[0048] Hereinafter, embodiment modes and embodiments in the present invention are described with reference to the accompanying drawings. However, the present invention can be carried out with many different modes and it is easily understood by those skilled in the art that modes and details can be modified in various ways without departing from the purpose and the scope of the present invention. Accordingly, the present invention should not be interpreted as being limited to the description of the embodiment modes and embodiments.

[Embodiment Mode 1]

[0049] FIGS. 1A and 1B illustrate a basic example of the present invention. FIG. 1A is a plan view and FIG 1B is a cross-sectional view.

[0050] A first electrode 102 is formed over a substrate 100. The first electrode 102 is formed with use of ITO (indium tin oxide) conventionally.

[0051] In the present invention, the first electrode 102 is formed of, for example, a semiconductor material containing silicon, although not limited thereto. Alternatively, amorphous silicon may be used but in order to enhance conductivity, polysilicon (polycrystalline silicon), single crystalline silicon, and the like may be used. Further, in many cases, the first electrode contains an impurity (a p-type impurity or an n-type impurity) such as phosphorus, boron, gallium, or arsenic to further enhance the conductivity.

[0052] The reason of using a semiconductor material containing silicon for the first electrode 102 is that silicon has high transmittance. In addition, since the first electrode 102 is thin, it can transmit light. The transmittance is preferably 50% or more, more preferably, 80% or more, so that higher visibility can be achieved.

[0053] Note that an insulating layer or a conductive layer may be provided between the substrate 100 and the first electrode 102. For example, an insulating layer for blocking an impurity intruding from the substrate 100, a gate electrode, a gate wiring, a gate insulating film, and the like may be provided.

[0054] An insulating film 106 is formed over the first electrode 102. Note that the insulating film 106 may have a single-layer structure or a stacked-layer structure.

[0055] An inorganic material or an organic material can be used for the insulating film 106. As an organic material, polyimide, acrylic, polyamide, polyimide amide, resist, siloxane, polysilazane, or the like can be used. As an inorganic material, an insulating substance containing oxygen or nitrogen, such as silicon oxide ( $\text{SiO}_x$ ), silicon nitride ( $\text{SiN}_x$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y$ ;  $x > y$ ), or silicon nitride oxide ( $\text{SiN}_x\text{O}_y$ ;  $x > y$ ) can be used. Alternatively, a stacked-layer film in which a plurality of these films are stacked may be used. Further alternatively, a stacked-layer film in which an organic material and an inorganic material are combined may be used.

[0056] Note that when an inorganic material is used for the insulating film, intrusion of moisture or an impurity can be prevented. In particular, a layer containing nitrogen can block moisture or an impurity efficiently.

[0057] Note that when an organic material is used for the insulating film, a surface thereof can be planarized. Accordingly, the insulating film can have a good effect on a layer provided thereover. For example, the layer formed over the organic material can be planarized, so that disturbance of orientation of the liquid crystal can be prevented, cutting of a wiring can be prevented, and a resist can be formed with accuracy.

[0058] A second electrode 108 is formed over the in-



ulating film 106. The second electrode 108 may be formed of a material with a high light-transmitting property. For example, one or more elements selected from indium (In), tin (Sn), and oxygen (O); or a compound or an alloy material containing one or more of the aforementioned elements as a component (such as indium tin oxide (ITO), indium zinc oxide (IZO), or indium tin oxide doped with silicon oxide (ITSO)) are desirable. In particular, IZO is preferable since it is easy to be patterned and formed into a minute shape with accuracy, although it is not limited thereto.

**[0059]** Note that the second electrode 108 has an opening pattern (slit). The opening pattern is for generating an electric field in a direction generally parallel to the substrate, between the first electrode 102 and the second electrode 108. Accordingly, as long as an electric field having a part which is generally parallel to the substrate can be generated, the opening pattern can have various shapes. Here, "generally parallel" refers to a parallel direction with small deviation. Therefore, the direction may be deviated from the parallel direction as long as the display is not disturbed. The direction may have a deviation of, for example, approximately  $\pm 10^\circ$ , or desirably, approximately  $\pm 5^\circ$ .

**[0060]** The opening pattern includes not only a closed opening pattern such as a slit, but also a space which is located between conductive patterns and in which the conductive pattern is not formed, such as a space between comb-teeth of a comb-shaped electrode. In other words, a gap or an interspace is needed between portions functioning as an electrode.

**[0061]** As described above, the electric field is generated between the second electrode 108 and the first electrode 102, so that an alignment state of liquid crystal molecules can be controlled.

**[0062]** Note that in a case where electrodes are provided in each pixel, an electrode to which a signal different among pixels depending on an image signal is provided, that is, a pixel electrode can be either the second electrode 108 or the first electrode 102. Accordingly, it is possible to set the second electrode 108 to be the pixel electrode and the first electrode 102 to be a common electrode. Alternatively, it is possible to set the second electrode 108 to be the common electrode and the first electrode 102 to be the pixel electrode.

**[0063]** Since the pixel electrode is connected to a source or drain of a transistor in many cases, when the first electrode 102 or the second electrode 108 functions as the pixel electrode, the structure can be simplified. Further, since the common electrodes in all pixels are connected to one another in many cases, when the first electrode 102 or the second electrode 108 functions as the common electrode, the structure can be simplified.

**[0064]** FIG 2A is a plan view and FIG 2B is a cross-sectional view of a case where a transistor 201 is provided. The transistor 201 is located near the first electrode 102 and the second electrode 108.

**[0065]** In this case, a film in the transistor 201 and the

first electrode 102 can be formed at the same time. As a result, the first electrode can be manufactured without increasing the numbers of masks (reticles) and manufacturing steps.

**[0066]** For example, a semiconductor layer in the transistor 201 and the first electrode 102 can be formed at the same time. The semiconductor layer in the transistor 201 and the first electrode 102 can be formed at the same time and etched at the same time, whereby patterning can be carried out at the same time. Further, in the case where the semiconductor layer is formed of polysilicon, the semiconductor layer and the first electrode 102 are crystallized at the same time.

**[0067]** Accordingly, the semiconductor layer in the transistor 201 and the first electrode 102 contain the same material.

**[0068]** Note that in a case of adding an impurity (a p-type impurity or an n-type impurity) such as phosphorus, boron, gallium, or arsenic to a part of the semiconductor layer in the transistor 201, it is desirable that the impurity is also introduced to the first electrode 102 at the same time. In a case of adding the impurity at the same time to portions, the concentration thereof is influenced by a thickness and a quality of a material of a film over the portions. When being formed under the similar layer structures, the semiconductor layer in the transistor 201 and the first electrode 102 have the impurity (a p-type impurity or an n-type impurity) at approximately the same concentration, at least partially. For example, a layer forming a source region or a drain region in the semiconductor layer in the transistor 201 and a semiconductor layer forming the first electrode 102 have impurity regions at approximately the same concentration.

**[0069]** Note that the semiconductor layer in the transistor 201 has a channel forming region in many cases. A gate electrode is located over the channel forming region with a gate insulating film therebetween. An impurity (a p-type impurity or an n-type impurity) is not introduced to the channel forming region to form a high-concentration impurity region, normally. However, there is a case where an impurity (a p-type impurity or an n-type impurity) is introduced to the channel forming region to form an extremely low-impurity region in order to adjust a value of a threshold voltage. Further, an impurity (a p-type impurity or an n-type impurity) is introduced to the semiconductor layer in the transistor 201 to form a low-concentration impurity region (LDD: Lightly Doped Drain) in some cases. Accordingly, in many cases, the semiconductor layer in the transistor 201 has a plurality of regions where impurities (p-type impurities or n-type impurities) are contained at various concentrations.

**[0070]** Note that in a case where an impurity (a p-type impurity or an n-type impurity) is introduced to the semiconductor layer in the transistor 201 and the first electrode 102 at the same time, the semiconductor layer in the transistor 201 and the first electrode 102 may be located extremely close to each other. It is because the same impurity (a p-type impurity or an n-type impurity)

is introduced thereto in many cases. Thus, the layout of the transistor 201 and the first electrode 102 can be significantly effective, which leads to improvement in aperture ratio.

**[0071]** Note that the conductivity of a part of the semiconductor layer in the transistor 201 and that of the first electrode 102 may differ from each other. In such a case, an impurity (a p-type impurity or an n-type impurity) is introduced to the first electrode 102 at the same as a transistor other than the transistor 201. Accordingly, in that case, the semiconductor layer in the transistor other than the transistor 201 and the first electrode 102 have the impurity (a p-type impurity or an n-type impurity) at approximately the same concentration, at least partially. For example, the transistor other than the transistor 201 is provided as a part of a source signal line driver circuit or a gate signal line driver circuit.

**[0072]** The transistor 201 and one of the first electrode 102 and the second electrode 108 are electrically connected in many cases. In addition, the electrode which is electrically connected to the transistor 201 functions as the pixel electrode in many cases. The transistor 201 and one of the first electrode 102 and the second electrode 108 are electrically connected through a contact hole, a wiring, or the like.

**[0073]** Note that in FIGS. 2A and 2B, a case in which the first electrode 102 is formed at the same time as the film in the transistor 201 is described; however, it is not limited thereto. The first electrode 102 may be formed at the same time as another film, such as a film in a wiring, a resistor, or a capacitor.

**[0074]** FIGS. 3A and 3B illustrate a case in which a transistor 301 is provided and a part of the transistor 301 and the first electrode 102 are contiguous with each other to form one island. FIG. 3A shows a plan view and FIG. 3B shows a cross-sectional view. Note that in this specification, "contiguous" refers to a case in which elements are formed continuously.

**[0075]** At this time, a film in the transistor 301 and the first electrode 102 are connected to each other as one film; therefore, they can be formed at the same time. As a result, the first electrode can be manufactured without increasing the numbers of masks (reticles) and manufacturing steps.

**[0076]** For example, a semiconductor layer in the transistor 301 and the first electrode 102 are connected to each other and can be formed at the same time. The semiconductor layer in the transistor 301 and the first electrode 102 can be formed at the same time and etched at the same time, whereby patterning can be carried out at the same time. Further, if the semiconductor layer is formed of polysilicon, the semiconductor layer and the first electrode 102 are crystallized at the same time. In this case, a crystal grain boundary of the semiconductor layer in the transistor 301 and that of the semiconductor layer forming the first electrode 102 extend in substantially the same direction. Here, the description "crystal grain boundaries extend in substantially the same direc-

tion" refers to a case in which, for example, grain boundaries with a longitudinal direction and a direction perpendicular to the longitudinal direction (also referred to as a short direction) have uniform longitudinal direction alignment.

**[0077]** Accordingly, the semiconductor layer in the transistor 301 and the first electrode 102 contain the same material.

**[0078]** Note that since the semiconductor layer in the transistor 301 and the first electrode 102 are contiguous and connected to each other; therefore, in some cases, it is difficult to clearly distinguish where the semiconductor layer in the transistor 301 ends and where the first electrode 102 begins.

**[0079]** Note that in a case where an impurity (a p-type impurity or an n-type impurity) such as phosphorus, boron, gallium, or arsenic is introduced to a part of the semiconductor layer in the transistor 301, it is desirable that the impurity is also introduced to the first electrode 102 at the same time. When the impurity is introduced to the semiconductor layer in the transistor 301 and the first electrode 102 at the same time, since they are contiguous with each other, they can be electrically connected to each other.

**[0080]** In that case, it is not necessary to provide a contact hole and to use another wiring in order to connect the semiconductor layer in the transistor 301 and the first electrode 102. Therefore, the layout can be significantly effective, which leads to improvement in aperture ratio.

**[0081]** Note that since the transistor 301 and the first electrode 102 are contiguous, they are electrically connected to each other in many cases. The electrode which is electrically connected to the transistor 301 functions as the pixel electrode in many cases.

**[0082]** Note that in a case of adding the impurity at the same time to portions, the concentration thereof is influenced by a thickness or a quality of a material of a film over the portions. When being formed under the similar layer structures, the semiconductor layer in the transistor 301 and the first electrode 102 have the impurity (a p-type impurity or an n-type impurity) at approximately the same concentration, at least partially.

**[0083]** Note that the semiconductor layer in the transistor 301 has a channel forming region in many cases. A gate electrode is located over the channel forming region with a gate insulating film therebetween. An impurity (a p-type impurity or an n-type impurity) is not introduced to the channel forming region to form a high-concentration impurity region, normally. However, there is a case where an impurity (a p-type impurity or an n-type impurity) is introduced to the channel forming region to form an extremely low-impurity region in order to adjust a value of a threshold voltage. Further, an impurity (a p-type impurity or an n-type impurity) is introduced to the semiconductor layer in the transistor 301 to form a low-concentration impurity region (LDD: Lightly Doped Drain) in some cases. Accordingly, in many cases, the semiconductor layer in the transistor 301 has a plurality of regions

where impurities (p-type impurities or n-type impurities) are contained at various concentrations.

**[0084]** Note that the conductivity of a part of the semiconductor layer in the transistor 301 and that of the first electrode 102 may differ from each other. In such a case, an impurity (a p-type impurity or an n-type impurity) is introduced to the first electrode 102 at the same as a transistor other than the transistor 301. Accordingly, in that case, the semiconductor layer in the transistor other than the transistor 301 and the first electrode 102 have the impurity (a p-type impurity or an n-type impurity) at approximately the same concentration, at least partially. For example, the transistor other than the transistor 301 is provided as a part of a source signal line driver circuit or a gate signal line driver circuit.

**[0085]** The transistor 301 and the first electrode 102 are electrically connected in many cases. In addition, the electrode which is electrically connected to the transistor 301, that is, the first electrode 102 functions as the pixel electrode in many cases. Accordingly, the electrode and the transistor can be efficiently located, which is favorable.

**[0086]** Note that in FIGS. 3A and 3B, a case in which the first electrode 102 is formed at the same time as the film in the transistor 301 is described; however, it is not limited thereto. The first electrode 102 may be formed at the same time as another film, such as a film in a wiring, a resistor, a capacitor, or the like.

**[0087]** Note that in FIGS. 1A to 3B, a case in which only the second electrode 108 has an opening pattern is described, but it is not limited thereto. The first electrode 102 may also have an opening pattern. Accordingly, an electric field generally parallel to the substrate is generated, and orientation of the liquid crystal molecules can be controlled. FIGS. 4A to 6B show such cases. FIGS. 4A and 4B correspond to a case shown in FIGS. 1A and 1B, in which the first electrode 102 also has an opening pattern. FIGS. 5A and 5B correspond to a case shown in FIGS. 2A and 2B, in which the first electrode 102 also has an opening pattern. FIGS. 6A and 6B correspond to a case shown in FIGS. 3A and 3B, in which the first electrode 102 also has an opening pattern.

**[0088]** When the first electrode 102 has an opening pattern as shown in FIGS. 4A to 6B, the amount of light transmitting through a portion of the opening pattern is increased. This is because the first electrode 102 and the second electrode 108 are not overlapped with each other. When the first electrode 102 and the second electrode 108 are overlapped, the amount of light transmitted therethrough is decreased unless the light transmittance is 100%. On the other hand, in a portion where the first electrode 102 and the second electrode 108 are not overlapped, light does not attenuate, which leads to increase in amount of light transmitted therethrough. As a result, it is possible to increase luminance and to reduce power consumption.

**[0089]** FIG 7A is a plan view for illustrating a structure of a liquid crystal display device according to Embodi-

ment Mode 1 in the present invention. In FIG 7A, one of a plurality of pixels provided in the liquid crystal display device is illustrated. This liquid crystal display device is a device in which an orientation of a liquid crystal is controlled by an FFS mode. In FIG 7A, a plurality of source wirings 107a are located parallel to one another (extending up and down in FIG 7A) and separately from one another, whereas a plurality of gate wirings 104c are located extending in a direction generally perpendicular to the source wirings 107a (from side to side in FIG. 7A) and are separated from one another. Auxiliary wirings 104b are located adjacent to each of the plurality of gate wirings 104c and extended to a direction generally parallel to the gate wirings 104c, that is, in a direction generally perpendicular (from side to side in FIG 7A) to the source wirings 107a. A space which is substantially rectangle is surrounded by the source wiring 107a, the auxiliary wiring 104b, and the gate wiring 104c. The pixel electrode of the liquid crystal display device is located in the space. A thin film transistor for driving the pixel electrode is located on the upper-left corner of FIG 7A.

**[0090]** As a material to be used for the gate wiring 104c, the auxiliary wiring 104b, and the source wiring 107a, one or more elements selected from aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), neodymium (Nd), chromium (Cr), nickel (Ni), platinum (Pt), gold (Au), silver (Ag), copper (Cu), magnesium (Mg), scandium (Sc), cobalt (Co), zinc (Zn), niobium (Nb), silicon (Si), phosphorus (P), boron (B), arsenic (As), gallium (Ga), indium (In), tin (Sn), and oxygen (O); a compound or an alloy material containing one or more of the aforementioned elements (for example, indium tin oxide (ITO), indium zinc oxide (IZO), indium tin oxide doped with silicon oxide (ITSO), zinc oxide (ZnO), aluminum neodymium (Al-Nd), or magnesium silver (Mg-Ag)); a substance obtained by combining such compounds; or the like can be given. Alternatively, a compound (silicide) of silicon and the aforementioned material (such as aluminum silicon, molybdenum silicon, or nickel silicide) or a compound of nitride and the aforementioned material (such as titanium nitride, tantalum nitride, or molybdenum nitride) can be used. Note that silicon (Si) may contain a large amount of n-type impurities (phosphorus or the like) or p-type impurities (boron or the like). When such an impurity is contained, conductivity of silicon is improved and silicon functions similarly to normal conductor, so that it becomes easy to use silicon as a wiring or an electrode. Silicon may be single crystalline silicon, polycrystalline silicon (polysilicon), or amorphous silicon. When single crystalline silicon or polycrystalline silicon is used, resistance can be reduced. When amorphous silicon is used, a manufacturing process can be simplified. Aluminum and silver have high conductivity, so that signal delay can be reduced, and minute processing is possible since they are easy to be etched and patterned. Copper has high conductivity, so that signal delay can be reduced. Molybdenum is desirable because it can be manufactured without a problem such as a defect of a mate-

rial, even if molybdenum is in contact with an oxide semiconductor such as ITO or IZO, or silicon; and because it is easily patterned and etched, and has high heat resistance. Titanium is desirable because it can be manufactured without a problem such as a defect of a material, even if titanium is in contact with an oxide semiconductor such as ITO or IZO, or silicon; and it is easily patterned and etched, and has high heat resistance. Tungsten is desirable because it has high heat resistance. Neodymium is desirable because it has high heat resistance. In particular, an alloy of neodymium and aluminum is desirable because heat resistance is improved and hillocks of aluminum are hardly generated. Silicon is desirable because it can be manufactured at the same time as the semiconductor layer in the transistor and has high heat resistance. Indium tin oxide (ITO), indium zinc oxide (IZO), indium tin oxide doped with silicon oxide (ITSO), zinc oxide (ZnO), and silicon (Si) are desirable because they have a light-transmitting property and can be used for a portion which is required to transmit light, such as the pixel electrode and the common electrode.

**[0091]** Note that a wiring or an electrode may have a single layer or a multilayer structure of these materials. If a single-layer structure is employed, the manufacturing process can be simplified and the number of steps can be reduced; which leads to reduction in cost. If a multilayer structure is employed, advantage of a material can be derived and disadvantage of the material can be reduced, so that a wiring and an electrode with favorable characteristics can be formed. For example, when a material with low resistance (such as aluminum) is included in the multilayer structure, the resistance of the wiring can be reduced. In addition, if a material with high heat resistance is used, for example, to be interposed between a material with low heat resistance and another advantage in a stacked-layer structure, the heat resistance of wiring or electrode as a whole can be improved. For example, a stacked-layer structure in which a layer containing aluminum is interposed between layers containing molybdenum or titanium is desirable. In addition, there is a case in which a material is directly in contact with another wiring or another electrode of another material, so that the materials are adversely affected. For example, a material may enter another material and change its characteristics; therefore, the material cannot serve its original purpose or a problem occurs in manufacturing and the material cannot be manufactured normally. In such a case, a problem can be solved when the layer is interposed between or covered with another layer. For example, if indium tin oxide (ITO) and aluminum are required to be in contact with each other, it is desirable that titanium or molybdenum is interposed therebetween. Also, if silicon and aluminum are required to be in contact with each other, it is desirable that titanium or molybdenum is interposed therebetween.

**[0092]** Note that it is desirable that the material of the gate wiring 104c and the auxiliary wiring 104b have heat resistance higher than that of the source wiring 107a. It

is because the gate wiring 104c and the auxiliary wiring 104b are located in a higher temperature in their manufacturing steps.

**[0093]** Note that it is desirable that the material of the source wiring 107a has resistance lower than that of the gate wiring 104c. It is because only signals of two values, that is, High-signal and Low-signal are given to the gate wiring 104c, whereas an analog signal which contributes display is introduced to the source wiring 107a. Accordingly, it is desirable that a material with low resistance is used for the source wiring 107a so that a signal can be applied with accuracy thereto.

**[0094]** Note that the auxiliary wiring 104b is not necessarily provided but a potential of the common electrode in each pixel can be stabilized when the auxiliary wiring 104b is provided. Note that in FIGS. 7A and 7B, the auxiliary wiring 104b and the gate wiring 104c are located to be generally parallel to each other, but it is not limited thereto. The auxiliary wiring 104b and the source wiring 107a may be located to be generally parallel to each other. In this case, the auxiliary wiring 104b is desirably formed of a material with the same quality as the source wiring 107a.

**[0095]** However, it is favorable that the auxiliary wiring 104b is located generally parallel to the gate wiring 104c because an aperture ratio can be increased and the layout can be efficient.

**[0096]** FIG. 7B is a cross-sectional view along a line A-B and a line C-D in FIG 7A. As shown in the drawing, a base insulating film 101 is formed over the substrate 100 so as to prevent diffusion of an impurity from the substrate 100. The base insulating film 101 is formed of, for example, an insulating substance containing oxygen or nitrogen, such as silicon oxide ( $\text{SiO}_x$ ), silicon nitride ( $\text{SiN}_x$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y$ :  $x > y$ ), or silicon nitride oxide ( $\text{SiN}_x\text{O}_y$ :  $x > y$ ). Alternatively, a stacked-layer film including a plurality of films thereof may be used.

**[0097]** Note that the substrate 100 is a glass substrate, a quartz substrate, a substrate formed of an insulator such as alumina, a plastic substrate with enough heat resistance to withstand a processing temperature of subsequent steps, a silicon substrate, or a metal substrate. Alternatively, polysilicon may be used.

**[0098]** Note that when the liquid crystal display device functions as a transmissive display device, it is desirable that the substrate 100 has a light-transmitting property.

**[0099]** A semiconductor film 102f and a first electrode 102c controlling the orientation of the liquid crystal are formed over the base insulating film 101. The semiconductor film 102f and the first electrode 102c are, for example, polysilicon films, which are formed by selectively etching a film in the same step. In other words, the semiconductor film 102f and the first electrode 102c are formed over the base film 101 and in the same layer. However, the present invention is not limited to film formation at the same time and etching in one step. In the semiconductor film 102f, an impurity region 102d to be a source region or a drain region and an impurity region

102b to be a drain region or a source region of the thin film transistor are formed. The impurity regions 102d and 102b are n-type impurity regions to which, for example, phosphorus or arsenic is introduced, but the impurity regions may be p-type impurity regions. An impurity for imparting n-type conductivity, phosphorus (P) and arsenic (As) are given as an example; and as an impurity for imparting p-type conductivity, boron (B) and gallium (Ga) are given as an example. However, it is desirable that the impurity regions 102d and 102b are n-type impurity regions having high conductivity. On the other hand, when a driver circuit only includes p-type transistors, it is desirable that the impurity regions 102d and 102b also have p-type conductivity type so that the manufacturing cost can be reduced.

**[0100]** The first electrode 102c functions as the common electrode to which common voltage which is same as other pixels is applied and is formed of, for example, a polysilicon film to which an impurity is introduced. The resistance of the first electrode 102 is lowered since an impurity is introduced thereto, and functions as an electrode. As shown in a dotted line in FIG 7A, the first electrode 102c has a rectangular shape with a portion 1001 in which one corner (the upper-left corner of the drawing) is lacked, and is formed over almost the whole surface of the pixel. Note that in the portion 102e of which one corner is lacked, a thin film transistor is located. When a thin film transistor is located in the portion 102e in which one corner is lacked, a region which can be used to display can be formed more efficiently, which leads to improvement in aperture ratio. The first electrode 102c has a thickness of, for example, 45 nm to 60 nm, and has sufficiently high light transmittance. In order to further improve the light transmittance, it is desirable to set the thickness of the first electrode 102 to be 40 nm or less.

**[0101]** The first electrode 102c is formed of polysilicon, for example, but may be another semiconductor material such as amorphous silicon, single crystalline silicon, organic semiconductor, or a carbon nanotube. In this case, an amorphous silicon film, an organic semiconductor film, or the like is used in the thin film transistor instead of the semiconductor film 102f. Note that the semiconductor film 102f and the first electrode 102c forming the transistor are desirably formed by selectively etching one film in the same step. In this case, the numbers of masks (reticles) and steps can be reduced, so that the manufacturing cost can be reduced. In addition, it is desirable that impurity elements of the same type are introduced to the impurity regions 102b and 102d at the same time. This is because when the impurity elements of the same type are introduced, the impurity elements can be introduced without a problem even if the impurity regions 102b and 102d are located close to each other, so that dense layout becomes possible. It is desirable to add impurity elements of either p-type or n-type because the manufacturing cost can be low compared with a case in which impurity elements of different types are introduced.

**[0102]** A gate insulating film 103 in the transistor is

formed over the whole surface including over the semiconductor film 102f.

**[0103]** However, there is a case in which the gate insulating film 103 is located only in the vicinity of the channel forming region and is not located in other parts. In addition, a thickness or a stacked-layer structure of the gate insulating film 103 may differ according to location. For example, the gate insulating film 103 may be thicker or include more layers in the vicinity of the channel forming region and may be thinner or include less layers in another location. Therefore, it becomes easy to control the addition of an impurity to the source region or the drain region. Further, when the thickness or the number of layers of the gate insulating film 103 in the vicinity of the channel forming region differs, the amount of impurity introduced to the semiconductor layer can be different by location, so that an LDD region or the like can be formed. When the LDD region is formed, leak current and generation of hot carriers can be suppressed, which can improve the reliability.

**[0104]** The gate insulating film 103 is formed of, for example, an insulating substance containing oxygen or nitrogen, such as silicon oxide ( $\text{SiO}_x$ ), silicon nitride ( $\text{SiN}_x$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y$ ;  $x > y$ ), or silicon nitride oxide ( $\text{SiN}_x\text{O}_y$ ;  $x > y$ ). Alternatively, a stacked-layer film including a plurality of these films may be used. A gate electrode 104a is formed over the gate insulating film 103 and is located above the channel forming region 102a. As shown in FIGS. 7A and 7B, the gate electrode 104a is in the same wiring layer as the auxiliary wiring 104b and the gate wiring 104c, and is connected to the gate wiring 104c. In the semiconductor film 102f, a region 102a located under the gate electrode 104a functions as a channel forming region. Note that, to a semiconductor region between the two channel forming regions 102a, an impurity which is the same as that in the impurity regions 102b and 102d is introduced. Note that in this embodiment mode, a multigate structure having two gate electrodes is employed, but the present invention is not limited to this structure.

**[0105]** An insulating film 105 and a first interlayer insulating film 106a are sequentially formed over the gate insulating film 103 and the gate electrode 104a.

**[0106]** Note that only one of the insulating film 105 and the first interlayer insulating film 106a may be formed, alternatively, each of the insulating films has a multilayer structure. An inorganic material or an organic material can be used for the insulating films. As an organic material, polyimide, acrylic, polyamide, polyimide amide, resist, siloxane, polysilazane, or the like can be used. As an inorganic material, an insulating substance containing oxygen or nitrogen, such as silicon oxide ( $\text{SiO}_x$ ), silicon nitride ( $\text{SiN}_x$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y$ ;  $x > y$ ), or silicon nitride oxide ( $\text{SiN}_x\text{O}_y$ ;  $x > y$ ) can be used. Alternatively, a stacked-layer film in which a plurality of these films are stacked may be used. Further alternatively, a stacked-layer film in which an organic material and an inorganic material are combined may be used.

**[0107]** In the gate insulating film 103, the insulating film 105, and the first interlayer insulating film 106a, a contact hole located over the impurity region 102b, a contact hole located over the impurity region 102d, a contact hole located over the first electrode 102c, and a contact hole located over the auxiliary wiring 104b are formed. Over the first interlayer insulating film 106a, the source wiring 107a, a drain wiring 107b, and a connection wiring 107c are formed. When an organic material is used for the insulating film, intrusion of moisture or an impurity can be prevented. In particular, a layer containing nitrogen can block moisture or an impurity efficiently.

**[0108]** Note that when an organic material is used for the insulating film, a surface thereof can be planarized. Accordingly, the insulating film can have a good effect on a layer provided thereover. For example, the layer formed over the organic material can be planarized, so that disturbance of orientation of the liquid crystal can be prevented.

**[0109]** The source wiring 107a is located above a source, that is, the impurity region 102d, and has a part embedded in the contact hole; therefore, the source wiring 107a and the impurity region 102d are electrically connected. Accordingly, the source electrode functions as a part of the source wiring 107a. The drain wiring 107b is located above a drain, that is, the impurity region 102b, and has a part embedded in the contact hole; therefore, the drain wiring 107b and the impurity region 102b are connected.

**[0110]** The connection wiring 107c is extended from above the first electrode 102c to above the auxiliary wiring 104b. The connection wiring 107c has a part embedded in the contact hole; therefore, the connection wiring 107c is electrically connected to both the first electrode 102c and the auxiliary wiring 104b. When the connection wiring 107c is provided in such a manner, the contact hole can be formed with accuracy since it is not required to be deep.

**[0111]** In the example shown in FIG 7B, the drain wiring 107b is formed at the same time as the source wiring 107a and the connection wiring 107c. In this case, the contact hole in which a part of the drain wiring 107b is embedded and the contact hole in which a part of the second electrode 108 is embedded is not overlapped with each other. Thus, even if the drain wiring 107b and the second electrode 108 have depressions over the contact holes, the depressions are not overlapped with each other. Therefore, a deep depressed portion is not formed in the second electrode 108, so that generation of a defect in shape of the resist pattern formed thereover can be suppressed.

**[0112]** Note that as shown in FIG 8, the second electrode 108 and the impurity region 102b may be connected directly without the drain wiring 107b. In this case, a contact hole for connecting the second electrode 108 and the impurity region 102b is required to be deep. Since the drain wiring 107bb shown in FIG 7B is not required, a region for the connection wiring can be utilized for dis-

playing an image as an opening region, which leads to improvement in aperture ratio and reduction in power consumption.

**[0113]** As described above, the first electrode 102c is connected to the auxiliary wiring 104b through the connection wiring 107c. It is desirable that a plurality of connection wirings 107c are provided in order to lower the resistance. Thus, a potential of the first electrode 102c is stabilized. In an example shown in FIG 7A, the connection wirings 107c are formed above three corners out of four corners of the first electrode 102c, except the one which is close to the thin film transistor. When the connection is made in a plurality of paths, generation of potential distribution in the first electrode 102c is suppressed. Further, when the first electrode 102c and the auxiliary wiring 104b are connected through the connection wiring 107c, the number of forming the contact holes can be reduced, which can simplify the process.

**[0114]** Note that the connection wiring 107c is formed at the same time and with use of the same material as the source wiring 107a, but it is not limited thereto. The connection wiring 107c may be formed at the same time and with use of the same material as the second electrode 108.

**[0115]** A second interlayer insulating film 106b is formed over the source wiring 107a, the drain wiring 107b, the connection wiring 107c, and the first interlayer insulating film 106a. Note that a structure in which the second interlayer insulating film 106b is not formed may be employed. An inorganic material or an organic material can be used for the second interlayer insulating film 106b. As an organic material, polyimide, acrylic, polyamide, polyimide amide, resist, siloxane, polysilazane, or the like can be used. As an inorganic material, an insulating substance containing oxygen or nitrogen, such as silicon oxide ( $\text{SiO}_x$ ), silicon nitride ( $\text{SiN}_x$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y$ ;  $x > y$ ), or silicon nitride oxide ( $\text{SiN}_x\text{O}_y$ ;  $x > y$ ) can be used. Alternatively, a stacked-layer film in which a plurality of these films are stacked may be used. Further alternatively, a stacked-layer film in which an organic material and an inorganic material are combined may be used. In the second interlayer insulating film 106b, a contact hole is formed over the drain wiring 107b.

**[0116]** The second electrode 108 which controls the orientation of the liquid crystal is formed over the interlayer insulating film 106b. The second electrode 108 functions as a pixel electrode to which voltage specific to each pixel is applied. The second electrode 108 is formed of ITO (indium tin oxide), ZnO (zinc oxide), IZO which is formed by using a target in which ZnO of 2 to 20 wt% is mixed to indium oxide, or the like. Note that the second electrode 108 and the impurity region 102b may be electrically connected through the drain wiring 107b, or may be directly connected.

**[0117]** In a case where the connection wiring is not provided as shown in FIG 8, the second electrode 108 is directly connected to the impurity region 102b in the thin film transistor.

**[0118]** As shown in FIGS. 7A and 8, the second electrode 108 is substantially rectangle and located above the first electrode 102c and the surroundings thereof. The second electrode 108 has a plurality of opening patterns 112 in a portion located above the first electrode 102c. The opening patterns 112, for example, include many slit-shaped opening patterns parallel to each other. In the example shown in FIG 7A, the opening patterns are diagonal to the source wiring 107a. Since the opening pattern 112 is provided, an electric field having a component parallel to the substrate is generated above the second electrode 108. Therefore, the orientation of the liquid crystal described later can be controlled by controlling the potential of the second electrode 108. Note that a shape of the opening pattern is not limited to that in this embodiment mode. A shape of opening pattern described in Embodiment Mode 2 or later can be employed. In other words, the opening pattern includes a space where a conductive pattern is not formed, such as a space between the comb-teeth of a comb-shaped electrode.

**[0119]** If opening patterns with different orientations are provided, a plurality of regions with different moving directions of liquid crystal molecules can be provided. In other word, a multidomain (also referred to as alignment division) structure can be realized. When a multidomain structure is employed, it can be prevented that an image cannot be displayed properly if seen from a certain direction. Accordingly, the viewing angle can be improved.

**[0120]** As shown in FIG 7A, a periphery of the first electrode 102c functioning as the common electrode extends out of the second electrode 108 functioning as the pixel electrode when seen from a direction perpendicular to the substrate 100. Thus, the second electrode 108 which is in a floating state after receiving a signal is less influenced by a signal transmitted to another pixel through the source wiring 107a. Accordingly, a defect of image quality, such as crosstalk can be suppressed. Note that the present invention is not limited to such an electrode structure and the first electrode 102c may have a portion in which its periphery does not extend out of the second electrode 108.

**[0121]** Next, an alignment film 109a and a liquid crystal 110 are stacked over the second interlayer insulating film 106b and the second electrode 108.

**[0122]** As the liquid crystal 110, a ferroelectric liquid crystal (FLC), a nematic liquid crystal, a smectic liquid crystal, a liquid crystal which is to be homogeneously aligned, a liquid crystal which is to be homeotropically aligned, or the like can be used. An opposite substrate 111 provided with the second alignment film 109b is located over the liquid crystal 110. Note that the opposite substrate 111 is provided with a color filter in many cases. In addition, a polarizing plate is provided on each outer side of the substrate 100 and the opposite substrate 111. Note that a retardation plate or a quarter-wave plate is provided as well as the polarizing plate in many cases.

**[0123]** Note that a stacked-layer structure according

to the present invention is not limited to the one described in this embodiment mode.

**[0124]** An example of a manufacturing method of a semiconductor device or a liquid crystal display device is described. First, the base insulating film 101 is formed over the substrate 100. Subsequently, a semiconductor film such as a polysilicon film or an amorphous silicon film is formed over the base insulating film 101. A resist pattern (not shown) is formed over the semiconductor film. Then, the semiconductor film is selectively etched with use of the resist pattern as a mask. In such a manner, the semiconductor film 102f and the first electrode 102c are formed in the same step. The resist pattern is removed thereafter.

**[0125]** Subsequently, the gate insulating film 103 is formed over the semiconductor film 102f, the first electrode 102c, and the base insulating film 101. The gate insulating film 103 is, for example, a silicon oxynitride film or a silicon oxide film, and formed by a plasma CVD method. Note that the gate insulating film 103 may be formed of a silicon nitride film, or a multilayer film containing silicon nitride and silicon oxide. Then, a conductive film is formed over the gate insulating film 103. The conductive film is selectively removed by etching using a resist pattern as a mask, and is patterned. Thus, two gate electrodes 104a are formed over the gate insulating film 103 which is located over the semiconductor film 102f. In addition, the auxiliary wiring 104b and the gate wiring 104c are formed at the same time as the gate electrode 104a.

**[0126]** As described above, the potential of the first electrode 102c and the second electrode 108 in each pixel can be stabilized when the auxiliary wiring 104b is provided. In addition, the auxiliary wiring 104b is not necessarily formed. Alternatively, the auxiliary wiring 104b may be formed in the same layer as another layer (for example, in the same layer as the source wiring 107a, in the same layer as the first electrode 102c, or in the same layer as the second electrode 108) or may be formed in a plurality of layers. In addition, although in FIG 7A, the auxiliary wiring 104b extends in the direction perpendicular to the source wiring 107a, a structure in which the auxiliary wiring 104b extends in the same direction as the source wiring 107a may be employed.

**[0127]** As a material to be used for the conductive film, one or more elements selected from aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), neodymium (Nd), chromium (Cr), nickel (Ni), platinum (Pt), gold (Au), silver (Ag), copper (Cu), magnesium (Mg), scandium (Sc), cobalt (Co), zinc (Zn), niobium (Nb), silicon (Si), phosphorus (P), boron (B), arsenic (As), gallium (Ga), indium (In), tin (Sn), and oxygen (O); a compound or an alloy material containing one or more of the aforementioned elements (for example, indium tin oxide (ITO), indium zinc oxide (IZO), indium tin oxide doped with silicon oxide (ITSO), zinc oxide (ZnO), aluminum neodymium (Al-Nd), or magnesium silver (Mg-Ag)); a substance obtained by combining such compounds; or the like can be given. Alternatively, a compound (silicide)

of silicon and the aforementioned material (such as aluminum silicon, molybdenum silicon, or nickel silicide) or a compound of nitride and the aforementioned material (such as titanium nitride, tantalum nitride, or molybdenum nitride) can be used. Note that silicon (Si) may contain a large amount of n-type impurities (phosphorus or the like) or p-type impurities (boron or the like).

**[0128]** Note that the wiring or the electrode may have a single layer or a multilayer structure of these materials. If a single-layer structure is employed, the manufacturing process can be simplified and the number of steps can be reduced; which leads to reduction in cost. If a multilayer structure is employed, advantage of a material can be derived and disadvantage of the material can be reduced, so that a wiring and an electrode with favorable characteristics can be formed. For example, when a material with low resistance (such as aluminum) is included in the multilayer structure, the resistance of the wiring can be reduced. In addition, if a material with high heat resistance is used, for example, to be interposed between a material with low heat resistance and another advantage in a stacked-layer structure, the heat resistance of the whole wiring or electrode can be improved. For example, a stacked-layer structure in which a layer containing aluminum is interposed between layers containing molybdenum or titanium is desirable. In addition, there is a case in which a material is directly in contact with another wiring or another electrode of another material, so that the materials are adversely affected. For example, a material may enter another material and change its characteristics; therefore, the material cannot serve its original purpose or a problem occurs in manufacturing of the material and the material cannot be manufactured normally. In such a case, a problem can be solved when the layer is interposed between or covered with another layer. For example, if indium tin oxide (ITO) and aluminum are in contact with each other, it is desirable that titanium or molybdenum is interposed therebetween. Also, if silicon and aluminum are in contact with each other, it is desirable that titanium or molybdenum is interposed therebetween.

**[0129]** Next, an impurity is injected into the semiconductor film 102f with use of the gate electrode 104a and a resist pattern (not shown) as a mask. Therefore, the impurity regions 102b and 102d and an impurity region between the gate electrodes 104a are formed. Note that an impurity element of n-type or p-type may be injected. Alternatively, both an n-type impurity element and a p-type impurity element may be injected into a specific region. In the latter case, it is set so that the injected amount of either the n-type impurity element or the p-type impurity element is more than the other.

**[0130]** Note that at this time, an LDD region may be formed by changing the thickness or the stacked-layer structure of the gate insulating film 103. In order to form the LDD region, the gate insulating film is thickened or the number of layers is increased in a portion in which the LDD region is to be formed. Accordingly, the injected

amount of the impurity is decreased, so that the LDD region can be easily formed.

**[0131]** Note that the resist pattern may be used as a mask in this step.

**[0132]** In addition, in a step of forming the impurity region, an impurity element may be injected into the first electrode 102c. In such a manner, the first electrode 102c can be formed at the same time as the impurity regions 102b and 102d. Therefore, the number of steps is not increased, so that the manufacturing cost of the liquid crystal display device can be low.

**[0133]** Note that the injection of the impurity element into the impurity region may be carried out before forming the gate electrode 104a, for example, before or after forming the gate insulating film 103. In that case, the impurity element is injected with use of the resist pattern as a mask. At this time, the impurity element may be injected into the first electrode 102c. Also in this case, the step of forming the impurity region in the transistor and the step of injecting the impurity element into the first electrode 102c can be the same step. Accordingly, the manufacturing cost of the liquid crystal display device can be low.

**[0134]** Further, in this case, a capacitor can be formed between an electrode in the same layer as the gate and the semiconductor film into which the impurity is injected. Since the gate insulating film is located between the electrode in the same layer as the gate and the semiconductor film into which the impurity is injected, a capacitor with thin thickness and large capacity can be formed.

**[0135]** Then, the first interlayer insulating film 106a and the contact holes are formed. Subsequently, a conductive film (such as a metal film) is formed over the first interlayer insulating film 106a and in the contact holes. The metal film is patterned, in other words, selectively removed. Thus, the source wiring 107a, the drain wiring 107b, and the connection wiring 107c are formed. As described above, the conductive film can be formed of various materials to have various structures. For example, a film formed of aluminum (Al), nickel (Ni), tungsten (W), molybdenum (Mo), titanium (Ti), tantalum (Ta), neodymium (Nd), platinum (Pt), gold (Au), silver (Ag), or the like; a film formed of an alloy thereof; or a stacked-layer film thereof can be used. Alternatively, silicon (Si) to which an n-type impurity is introduced may be used.

**[0136]** Then, the second interlayer insulating film 106b and the contact holes are formed. Thereafter, an ITO film, an IZO film, or a ZnO film is formed over the second interlayer insulating film 106b and in the contact holes. The film is selectively etched with use of a resist pattern. Thus, the second electrode 108 is formed.

**[0137]** Note that the contact hole in which a part of the drain wiring 107b is embedded and the contact hole in which a part of the second electrode 108 is embedded are different from each other in location. Thus, even if the drain wiring 107b and the second electrode 108 have depressions in portions located over the contact holes, the depressions are not overlapped with each other.



Therefore, a deep depressed portion is not formed in the second electrode 108, so that generation of a defect in shape of the aforementioned resist pattern can be suppressed. Thereafter, the resist pattern is removed.

**[0138]** However, the present invention is not limited thereto. For example, the contact hole in which a part of the drain wiring 107b is embedded and the contact hole in which a part of the second electrode 108 is embedded may be overlapped with each other. In this case, the contact holes can be accommodated in one location, therefore the layout can be efficient. Accordingly, the aperture ratio can be improved.

**[0139]** Subsequently, the first alignment film 109a is formed, and the liquid crystal is sealed between the first alignment film 109a and the opposite substrate 111 provided with the second alignment film 109b. Thereafter, on a side of the opposite substrate 111 or on a side of the substrate 100 which are not in contact with the liquid crystal 110 (that is, an outer side of the liquid crystal display device), an optical film or the like such as a polarizing plate, a retardation plate, a quarter-wave plate, a diffusing plate, or a prism sheet is provided. Further, a backlight or a frontlight is provided. As the backlight, a direct type or a sidelight type can be used. As a light source, a cold cathode tube or an LED (light emitting diode) can be used. As the LED, white color LED or single color LED (such as white, red, blue, green, cyan, magenta, or yellow) may be combined to be used. When the LED is used, color purity can be improved since the LED has a sharp peak of light wavelength. In such a manner, a liquid crystal display device is formed.

**[0140]** Note that a liquid crystal display device may only refer to a substrate, an opposite substrate, and a liquid crystal interposed therebetween. Alternatively, a liquid crystal display device may further include an optical film such as a polarizing plate or a retardation plate. Further alternatively, a liquid crystal display device may further include a diffusing plate, a prism sheet, a light source (such as a cold cathode tube or an LED), a light-guide plate, and the like.

**[0141]** According to Embodiment Mode 1 in the present invention, in the liquid crystal display device in which the alignment direction of the liquid crystal is controlled by an FFS mode, the first electrode 102c is formed of a polysilicon film to which an impurity is introduced, and formed in the same step as the semiconductor film 102f including the source region, the drain region, and the channel forming region of the thin film transistor. Therefore, the number of manufacturing steps and the manufacturing cost can be reduced compared with a case in which the common electrode is formed of ITO.

**[0142]** Although the connection wiring 107c is located in the same layer as the source wiring 107a and the drain wiring 107b in this embodiment mode, the connection wiring 107c may be located in another wiring layer (for example, in the same layer as the gate wiring 104c, the first electrode 102c, or the second electrode 108). In addition, the gate insulating film 103 is not necessarily

formed over the whole surface.

**[0143]** The auxiliary wiring 104b may be formed in the same layer as the source wiring 107a. In this case, the auxiliary wiring 104b may be located parallel to the gate wiring 104c, and the auxiliary wiring 104b and the gate wiring 104c may be formed in the same layer only in a portion in which the source wiring 107a and the auxiliary wiring 104b are intersected. Alternatively, the auxiliary wiring 104b and the source wiring 107a may be located in parallel.

**[0144]** The gate electrode 104a and the gate wiring 104c may be formed of different materials or in the different layers.

**[0145]** Although a so-called top gate thin film transistor in which the gate electrode is located above the channel forming region is described in this embodiment mode, the present invention is not particularly limited thereto. A so-called bottom gate thin film transistor in which the gate electrode is located under the channel forming region or a transistor having a structure in which the gate electrodes are located over and under the channel forming region may be formed.

#### [Embodiment Mode 2]

**[0146]** FIG. 9A is a plan view illustrating a structure of an FFS mode liquid crystal display device according to Embodiment Mode 2 in the present invention. FIG. 9B is a cross-sectional view along a line A-B and a line C-D of FIG. 9A. A structure of this embodiment mode is similar to that of Embodiment Mode 1, except that the first electrode 102c is electrically connected to the source wiring 107a through the transistor and functions as the pixel electrode, the second electrode 108 is electrically connected to the auxiliary wiring 104b and functions as the common electrode, a shape of the opening pattern 112 formed in the second electrode 108 is different, and connection structures of the first electrode 102c, the second electrode 108, and the wirings are different. Also, a manufacturing method of the liquid crystal display device according to this embodiment mode is almost similar to that in Embodiment Mode 1. Therefore, the description in Embodiment Mode 1 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 1 is denoted by the same reference numeral and description thereof is omitted.

**[0147]** The impurity region 102b to be a drain or a source of the transistor is directly connected to the first electrode 102c. In other words, the semiconductor layer in the transistor and the first electrode 102c are contiguous with each other to form one island. In addition, unlike Embodiment Mode 1, the contact hole located over the impurity region 102b and the contact hole located over the first electrode 102c are not formed in the first inter-layer insulating film 106a. Accordingly, the region for the contact holes can be utilized for displaying an image, which leads to improvement in aperture ratio.

**[0148]** Note that since the impurity region 102b func-

tioning as the drain or the source of the transistor and the first electrode 102 are contiguous and connected to each other; therefore, in some cases, it is difficult to clearly see where the impurity region 102b in the transistor ends and where the first electrode 102 begins.

**[0149]** Note that in a case where an impurity (a p-type impurity or an n-type impurity) such as phosphorus, boron, gallium, or arsenic is introduced to the impurity region to be as the drain or the source of the transistor, it is desirable that an impurity having the same conductivity is also introduced to the first electrode 102c at the same time. When the impurity is introduced to the impurity region and the first electrode 102c at the same time, since they are contiguous with each other, they can be electrically connected to each other. At this time, the concentration of the impurity introduced to portions is influenced by a thickness or a quality of a material of the film over the portions. When being formed under the similar layer structures, the impurity region functioning as a drain or a source of the transistor and the first electrode 102c have the impurity (a p-type impurity or an n-type impurity) at approximately the same concentration, at least partially.

**[0150]** A contact hole located over the connection wiring 107c is formed in the second interlayer insulating film 106b. The second electrode 108 has a part embedded in the contact hole, so as to be connected to the connection wiring 107c.

**[0151]** As shown in FIG. 9A, in this embodiment mode, the second electrode 108 has two kinds of opening patterns 112a and 112b. The opening pattern 112a formed in an upper region in the drawing and the opening pattern 112b formed in a lower region in the drawing have different orientations from each other.

**[0152]** If opening patterns 112a and 112b with different orientations are provided, a plurality of regions with different moving directions of liquid crystal molecules can be realized. In other word, a multidomain structure can be employed. When a multidomain structure is employed, it can be prevented that an image cannot be displayed properly if seen from a certain direction. Accordingly, the viewing angle can be improved.

**[0153]** In addition, as shown in FIGS. 9A and 9B, the first electrode 102c functions as the pixel electrode and the second electrode 108 functions as the common electrode, and the liquid crystal is located closer to the common electrode than to the pixel electrode. Accordingly, even if voltage of the pixel electrode varies among pixels, an electric field in a portion where the liquid crystal exists hardly changes due to an image; therefore, adjacent pixels are less affected each other, so that crosstalk can be reduced.

**[0154]** With this embodiment mode, an effect similar to Embodiment Mode 1 can be obtained. In addition, the opening patterns 112a and 112b with different orientations are formed in the second electrode 108. Therefore, the direction of electrical field gradient generated between the first electrode 102c and the second electrode

108 and in the liquid crystal 110 can be divided into two in a plane parallel to the substrate. Therefore, the viewing angle of the liquid crystal display device can be further improved.

**[0155]** Note that in Embodiment Mode 1, the shape of the second electrode 108 may be similar to that in this embodiment mode. In addition, in this embodiment mode, the shape of the opening pattern in the second electrode 108 may be similar to that in Embodiment Mode 1. Although only one pixel is shown in FIGS. 9A and 9B, a plurality of pixels are arranged in matrix in practice. In practice, the second electrodes 108 in pixels may be connected to each other through the connection wiring 107c. Accordingly, the resistance can be lowered, so that the sufficient voltage can be applied to the second electrode 108.

**[0156]** Note that this embodiment mode shows an example in a case in which the description in Embodiment Mode 1 is partially changed, improved, or transformed. Therefore, the description in Embodiment Mode 1 can be applied to or combined with this embodiment mode.

**[0157]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 3]

**[0158]** FIG 10A is a plan view illustrating a structure of a liquid crystal display device according to Embodiment Mode 3 in the present invention. FIG 10B is a cross-sectional view along a line A-B, a line C-D, and a line E-F of FIG 10A. A structure of this embodiment mode is similar to that of Embodiment Mode 1, except that an opening pattern 115 is formed in the first electrode 102c and except for the shape of the opening pattern 112. In other words, the liquid crystal display device according to this embodiment mode is a device in which the alignment direction of the liquid crystal is controlled by an IPS mode. The pixel portion and the common electrode are alternately arranged and are generally in parallel in a main portion, when seen from a direction perpendicular to the substrate 100 of the liquid crystal display device. In the aforementioned FFS mode, a lower electrode of the pixel electrode and the common electrode does not have an opening pattern. Note that a manufacturing method of the liquid crystal display device according to this embodiment mode is generally similar to that of Embodiment Mode 1. Accordingly, the description in Embodiment Mode 1 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 1 is denoted by the same reference numeral and description thereof is omitted.

**[0159]** The opening pattern 115 is located under a region of the second electrode 108, in which the opening pattern 112 is not formed, and the surroundings thereof. Accordingly, the first electrode 102c functioning as the common electrode and the second electrode 108 func-

tioning as the pixel electrode are alternately arranged and generally parallel except in the periphery portions. With the aforementioned electrode structure, an electric field parallel to the substrate can be generated between the first electrode 102c and the second electrode 108, and an effect such as improvement in viewing angle which is characteristics of an IPS mode can be obtained. The opening patterns 112 and 115 have wave-shapes in this embodiment mode.

**[0160]** If the opening patterns are thus provided to have different orientations, a plurality of regions with different moving directions of liquid crystal molecules can be realized. In other word, a multidomain structure can be employed. When a multidomain structure is employed, it can be prevented that an image cannot be displayed properly if seen from a certain direction. Accordingly, the viewing angle can be improved.

**[0161]** In this embodiment mode, a portion of the first electrode 102c and a portion of the second electrode 108 (portions denoted by reference numerals 120a and 120b) interpose the gate insulating film 103, the insulating film 105, the first interlayer insulating film 106a, and the second interlayer insulating film 106b. Therefore, in each portion denoted by the reference numerals 120a and 120b, the first electrode 102c, the second electrode 108, and the insulating film therebetween function as a capacitor. With provision of the capacitors 120a and 120b, the storage capacitance can be increased. Therefore, when a thin film transistor is turned off, the potential of the second electrode 108 can be easily kept.

**[0162]** With this embodiment mode, an effect similar to Embodiment Mode 1 can be obtained. Note that in this embodiment mode, the opening pattern 112 formed in the second electrode 108 may have the shape of the opening pattern 112 shown in FIGS. 7A and 7B or 9A and 9B. In this case, the opening pattern 115 included in the first electrode 102c has a shape similar to the opening pattern 112 shown in FIGS. 7A and 7B, or 9A and 9B. Note that the opening patterns 112 and 115 are required to be arranged so that the first electrode 102c and the second electrode 108 are alternately arranged and are generally in parallel except in the periphery portions, when seen from the direction perpendicular to the substrate 100 of the liquid crystal display device.

**[0163]** In addition, in Embodiment Mode 1 or 2, the opening pattern 112 may have a shape similar to that in this embodiment mode. In this case, an FFS mode liquid crystal display device in which the opening pattern 112 has the shape shown in FIGS. 10A and 10B can be obtained.

**[0164]** Note that the first electrode 102c has the opening pattern 115 in this embodiment mode. Therefore, in a portion of the opening pattern, the amount of light transmitted therethrough is increased. This is because the first electrode 102 is not provided in that portion. In a portion where the first electrode 102 is provided, the amount of light transmitted therethrough is decreased because the light transmittance is not 100%. On the other hand, in a

portion where the first electrode 102 is not provided, the light does not attenuate, which leads to increase in amount of light transmitted therethrough. As a result, it is possible to increase luminance and to reduce power consumption.

**[0165]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 and 2 is partially changed, improved, or transformed. Therefore, the description in Embodiment Modes 1 and 2 can be applied to or combined with this embodiment mode.

**[0166]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 4]

**[0167]** FIG. 11A is a plan view illustrating a structure of an IPS mode liquid crystal display device according to Embodiment Mode 4 in the present invention. FIG. 11B is a cross-sectional view along a line A-B and a line C-D of FIG. 11A. A structure in this embodiment mode is similar to Embodiment Mode 2, except that the opening pattern 115 is formed in the first electrode 102c and except for the shape of the opening pattern 112. Also, a manufacturing method of the liquid crystal display device according to this embodiment mode is generally similar to that in Embodiment Mode 2. Accordingly, the description in Embodiment Mode 2 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 2 is denoted by the same reference numeral and description thereof is omitted.

**[0168]** The impurity region 102b to be a drain or a source of the transistor is directly connected to the first electrode 102c. In other words, the semiconductor layer in the transistor and the first electrode 102c are contiguous with each other to form one island. In addition, unlike Embodiment Mode 1, the contact hole located over the impurity region 102b and the contact hole located over the first electrode 102c are not formed in the first interlayer insulating film 106a. Accordingly, the region for the contact holes can be utilized for displaying an image, which leads to improvement in aperture ratio.

**[0169]** The opening pattern 115 is located under a region of the second electrode 108, in which the opening pattern 112 is not formed and the surroundings thereof. Accordingly, the first electrode 102c functioning as the pixel electrode and the second electrode 108 functioning as the common electrode are alternately arranged and are generally in parallel except in the periphery portions. With the aforementioned electrode structure, a lateral electric field can be generated between the first electrode 102c and the second electrode 108, and an effect such as improvement in viewing angle which is characteristics of an IPS mode can be obtained. The opening patterns 112 and 115 are generally parallel to the source wiring 107a in this embodiment mode.

**[0170]** In this embodiment mode, a portion of the first electrode 102c and a portion of the second electrode 108 (portions denoted by reference numerals 121a and 121b) interpose the gate insulating film 103, the insulating film 105, the first interlayer insulating film 106a, and the second interlayer insulating film 106b. Therefore, in each portion denoted by the reference numerals 121a and 121b, the first electrode 102c, the second electrode 108, and the insulating film therebetween function as a capacitor. With provision of the capacitors 121a and 121b, the storage capacitance can be increased. Therefore, when a thin film transistor is turned off, the potential of the first electrode 102c can be easily kept.

**[0171]** In this embodiment mode, an effect similar to Embodiment Mode 1 can be obtained. Note that in this embodiment mode, the opening patterns 112 and 115 may have the shape shown in FIGS. 10A and 10B. Alternatively, the opening pattern 112 may have the shape shown in FIGS. 7A and 7B, or 9A and 9B. In this case, the opening pattern 115 has a shape similar to the opening pattern 112 shown in FIGS. 7A and 7B, or 9A and 9B. Note that the opening patterns 112 and 115 are required to be arranged so that the first electrode 102c and the second electrode 108 are alternately arranged and are generally in parallel except in the periphery portions, when seen from the direction perpendicular to the substrate 100 of the liquid crystal display device.

**[0172]** In addition, the opening patterns 112 and 115 in the IPS mode liquid crystal display device shown in Embodiment Mode 3 may have the shape shown in FIG 11A and 11B. Alternatively, in Embodiment Mode 1 or 2, the opening pattern 112 may have a shape similar to that in this embodiment mode. In the latter case, an FFS mode liquid crystal display device in which the opening pattern 112 has the shape shown in FIGS. 11A and 11B can be obtained.

**[0173]** Note that the first electrode 102c has the opening pattern 115 in this embodiment mode. Therefore, in a portion of the opening pattern, the amount of light transmitted therethrough is increased. This is because the first electrode 102 is not provided in that portion. In a portion where the first electrode 102 is provided, the amount of light transmitted therethrough is decreased because the light transmittance is not 100%. On the other hand, in a portion where the first electrode 102 is not provided, the light does not attenuate, which leads to increase in the amount of light transmitted therethrough. As a result, it is possible to increase luminance and to reduce power consumption.

**[0174]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 3 is partially changed, improved, or transformed. Therefore, the description in Embodiment Modes 1 to 3 can be applied to or combined with this embodiment mode.

**[0175]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by

combining components selected from different drawings.

[Embodiment Mode 5]

**[0176]** FIG 12A is a plan view illustrating a structure of an FFS mode liquid crystal display device according to Embodiment Mode 5 in the present invention. FIG 12B is a cross-sectional view along a line A-B and a line C-D of FIG 12A. A structure of this embodiment mode is similar to that of Embodiment Mode 1, except that the second interlayer insulating film 106b is not formed, and the second electrode 108 is formed over the first interlayer insulating film 106a. A part of the second electrode 108 is located over the drain wiring 107b and the second electrode 108 and the drain wiring 107b are directly connected therethrough.

**[0177]** The second electrode 108 is formed after the source wiring 107a, the drain wiring 107b, and the connection wiring 107c are formed. By forming the second electrode 108 after forming the drain wiring 107b, residue of etching of the drain wiring 107b is prevented from remaining on a surface of the second electrode 108, which can planarize the surface of the second electrode 108. Note that a structure in which the second electrode 108 covers the drain wiring 107b may be employed.

**[0178]** Note that the second electrode 108 may be formed at the same time as the source wiring 107a and the drain wiring 107b. That is, they may be formed of a similar material and by patterning at the same time. Accordingly, a step of forming a light-transmitting electrode can be omitted, so that the cost can be reduced.

**[0179]** Therefore, the second electrode 108 does not necessarily have a light-transmitting property. In other words, the second electrode 108 may reflect light.

**[0180]** A manufacturing method of the liquid crystal display device according to this embodiment mode is generally similar to that in Embodiment Mode 1, except that the step of forming the second interlayer insulating film 106b is omitted. Therefore, the description in Embodiment Mode 1 can be applied to this embodiment mode. Note that since the step of forming the second interlayer insulating film 106b is omitted, the manufacturing cost of the liquid crystal display device is lowered. Hereinafter, the component similar to that of Embodiment Mode 1 is denoted by the same reference numeral and description thereof is omitted.

**[0181]** With this embodiment mode, an effect similar to Embodiment Mode 1 can be obtained. Note that in this embodiment mode, the number of the interlayer insulating films is smaller by one than that of Embodiment Mode 1, an electrical field gradient between the first electrode 102c and the second electrode 108 becomes large. Therefore, a potential gradient of the same level can be obtained with low voltage, whereby power consumption of the liquid crystal display device can be reduced. This effect is enhanced when the first interlayer insulating film 106a is formed of a material with high dielectric constant (such as silicon nitride, aluminum oxide, hafnium oxide,

or tantalum oxide). In the case of forming the first interlayer insulating film 106a of a material with high dielectric constant, an effect in which storage capacitance can be increased can be also obtained. In addition, since the step of forming the second interlayer insulating film 106b is omitted, the manufacturing cost is low compared with Embodiment Mode 1.

**[0182]** Note that in this embodiment mode, a structure similar to Embodiment Mode 2 may be employed, in which the first electrode 102c and the impurity region 102b to be a drain may be connected, so that the first electrode 102c may function as the pixel electrode. In this case, there is an advantage over Embodiment Mode 2 in that the second interlayer insulating film 106b is not required. In addition, the second electrode 108 is directly connected to the connection wiring 107c in the same manner of the drain wiring 107b and the second electrode 108 in FIGS. 12A and 12B where the second electrode 108 is partially located over the drain wiring 107b. Thus, the second electrode 108 functions as the common electrode.

**[0183]** In this embodiment mode, the second electrode 108 and the opening pattern 112 may have the shapes shown in FIGS. 9A and 9B, 10A and 10B, or 11A and 11B. If the second electrode 108 and the opening pattern 112 have the shapes shown in FIGS. 10A and 10B, or 11A and 11B, the capacitors denoted by the reference numerals 120a and 120b in FIGS. 10A and 10B or the capacitors denoted by the reference numerals 121a and 121b in FIGS. 11A and 11B are formed, so that the storage capacitance can be increased. Therefore, when a thin film transistor is turned off, the potential of the second electrode 108 can be easily kept.

**[0184]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 4 is partially changed, improved, or transformed. Therefore, the description in Embodiment Modes 1 to 4 can be applied to or combined with this embodiment mode.

**[0185]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 6]

**[0186]** FIG. 13A is a plan view illustrating a structure of an IPS mode liquid crystal display device according to Embodiment Mode 6 in the present invention. FIG. 13B is a cross-sectional view along a line A-B, a line C-D, and a line E-F of FIG. 13A. A liquid crystal display device according to this embodiment mode is similar to that of Embodiment Mode 3, except that a capacitor 114 connected to the second electrode 108 is provided. Note that as long as a structure in which the capacitor is connected to the auxiliary wiring 104b and the second electrode 108, the present invention is not limited to the structure shown in this embodiment mode. In addition, a manufac-

turing method of the liquid crystal display device according to this embodiment mode is generally similar to that in Embodiment Mode 3. Therefore, the description in Embodiment Mode 3 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 3 is denoted by the same reference numeral and description thereof is omitted.

**[0187]** An electrode 113 for the capacitor which is located above the auxiliary wiring 104b is formed over the first interlayer insulating film 106a. The electrode 113 for the capacitor is located in the same layer as the source wiring 107a and formed in the same step as the source wiring 107a. The capacitor 114 includes the auxiliary wiring 104b and the electrode 113 for the capacitor with the insulating film 105 and the first interlayer insulating film 106a therebetween. Since the capacitor is formed above the auxiliary wiring 104b, an area of the opening portion is not reduced. Therefore, in a case of providing the capacitor, the aperture ratio is not decreased.

**[0188]** A contact hole located over the electrode 113 for the capacitor is formed in the second interlayer insulating film 106b. The second electrode 108 has a part embedded in the contact hole, so as to be connected to the electrode 113 for the capacitor.

**[0189]** With this embodiment mode, an effect similar to Embodiment Mode 3 can be obtained. In addition, since the capacitor 114 is connected between the second electrode 108 functioning as a pixel electrode and the auxiliary wiring 104b, the voltage of the second electrode 108 is easily kept when the thin film transistor is turned off.

**[0190]** Note that in this embodiment mode, the opening patterns 112 and 115 may have the shape shown in FIGS. 11A and 11B. Alternatively, the opening pattern 112 may have the shape shown in FIGS. 7A and 7B, or 9A and 9B. In this case, the opening pattern 115 in the first electrode 102c may have a shape similar to the opening pattern 112 shown in FIGS. 7A and 7B, or 9A and 9B. Note that the opening patterns 112 and 115 are required to be arranged so that the first electrode 102c and the second electrode 108 are alternately arranged and are generally in parallel except in the periphery portions, when seen from the direction perpendicular to the substrate 100 of the liquid crystal display device.

**[0191]** In Embodiment Mode 1 shown in FIGS. 7A and 7B, an effect similar to this embodiment mode can be obtained if the capacitor 114 is formed and connected to the second electrode 108. In addition, if the electrode 113 for the capacitor is located above the gate wiring 104c, a similar effect can be obtained because the potential of the gate wiring 104c is substantially constant when the pixel is not selected. The capacitor may keep the potential of the pixel electrode; therefore, the capacitor is preferably formed between the pixel electrode and a wiring with a constant potential. It is more preferable that the gate wiring 104c connected to the capacitor is the gate wiring in one preceding row because the potential thereof is substantially constant since its selected state is finished.

**[0192]** If the opening patterns are thus provided to have different orientations and shapes, a plurality of regions with different moving directions of liquid crystal molecules can be provided. In other word, a multidomain structure can be realized. When a multidomain structure is employed, it can be prevented that an image cannot be displayed properly if seen from a certain direction. Accordingly, the viewing angle can be improved.

**[0193]** Note that the first electrode 102c has the opening pattern 115 in this embodiment mode. Therefore, in a portion of the opening pattern, the amount of light transmitted therethrough is increased. This is because the first electrode 102 is not provided in that portion. In a portion where the first electrode 102 is provided, the amount of light transmitted therethrough is decreased because the light transmittance is not 100%. On the other hand, in a portion where the first electrode 102 is not provided, light does not attenuate, which leads to increase in amount of light transmitted therethrough. As a result, it is possible to increase luminance and to reduce power consumption.

**[0194]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 5 is partially changed, improved, or transformed. Therefore, the description in Embodiment Modes 1 to 5 can be applied to or combined with this embodiment mode.

**[0195]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 7]

**[0196]** FIG. 14A is a plan view illustrating a structure of an IPS mode liquid crystal display device according to Embodiment Mode 7 in the present invention. FIG 14B is a cross-sectional view along a line A-B, a line C-D, and a line E-F of FIG 14A. A structure in this embodiment mode is similar to that of the IPS mode liquid crystal display device according to Embodiment Mode 4, except that the opening patterns 115 and 112 have a substantially V-shape and the capacitor 117 electrically connected to the first electrode 102c, and the auxiliary wiring 104b is provided. Accordingly, the description in Embodiment Mode 4 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 4 is denoted by the same reference numeral and description thereof is omitted.

**[0197]** The capacitance 117 is formed when a part of the first electrode 102c (a lower end in FIG 14A) is located under the auxiliary wiring 104b. In other words, the capacitance 117 includes the first electrode 102c, the auxiliary wiring 104b, and the gate insulating film 103 therebetween.

**[0198]** A manufacturing method of a liquid crystal display device according to this embodiment mode is similar to Embodiment Mode 3, except that the impurity is injected into the first electrode 102c before forming a conduc-

tive film to be the auxiliary wiring 104b, and the impurity is injected into the semiconductor film 102f after forming the gate electrode 104a, the auxiliary wiring 104b, and the like. Accordingly, the resistance of a whole part of the first electrode 102c, which forms the capacitor 117, is lowered and the capacitor 117 operates only by changing the potential of the first electrode 102c with respect to the auxiliary wiring 104b.

**[0199]** With this embodiment mode, an effect similar to Embodiment Mode 4 can be obtained. In addition, since the capacitor 117 is connected between the first electrode 102c functioning as the pixel electrode and the auxiliary wiring 104b, the voltage of the second electrode 102c is easily kept when the thin film transistor is turned off.

**[0200]** Note that the capacitor 117 may be provided in Embodiment Mode 2. In this case, an effect similar to this embodiment mode can be obtained.

**[0201]** In this embodiment mode, the opening patterns 112 and 115 may have the shape shown in FIGS. 10A and 10B, or 11A and 11B. Alternatively, the opening pattern 112 may have the shape shown in FIGS. 7A and 7B, or 9A and 9B. In this case, the opening pattern 115 has the shape of the opening pattern 112 shown in FIGS. 7A and 7B, or 9A and 9B. Note that the opening patterns 112 and 115 are required to be arranged so that the first electrode 102c and the second electrode 108 are alternately arranged and generally in parallel except in the periphery portions, when seen from the direction perpendicular to the substrate 100 of the liquid crystal display device.

**[0202]** In the IPS mode liquid crystal display device according to Embodiment mode 3, 4, or 6, the opening patterns 112 and 115 may have the shape shown in FIGS. 14A and 14B. In addition, in the FFS mode liquid crystal display device according to Embodiment mode 1, 2, or 5, the opening pattern 112 may have the shape shown in FIGS. 14A and 14B.

**[0203]** The impurity region 102b functioning as a drain or a source of the transistor is directly connected to the first electrode 102c. In other words, the semiconductor layer in the transistor and the first electrode 102c are contiguous with each other to form one island. In addition, unlike Embodiment Mode 1, the contact hole located over the impurity region 102b and the contact hole located over the first electrode 102c are not formed in the first interlayer insulating film 106a. Accordingly, the region for the contact holes can be utilized for displaying an image, which leads to improvement in aperture ratio.

**[0204]** If the opening patterns are thus provided to have different orientations, a plurality of regions with different moving directions of liquid crystal molecules can be provided. In other word, a multidomain structure can be realized. When a multidomain structure is employed, it can be prevented that an image cannot be displayed properly if seen from a certain direction. Accordingly, the viewing angle can be improved.

**[0205]** Note that the first electrode 102c has the open-

ing pattern 115 in this embodiment mode. Therefore, in a portion of the opening pattern, the amount of light transmitted therethrough is increased. This is because the first electrode 102 is not provided in that portion. In a portion where the first electrode 102 is provided, the amount of light transmitted therethrough is decreased because the light transmittance is not 100%. On the other hand, in a portion where the first electrode 102 is not provided, light does not attenuate, which leads to increase in amount of light transmitted therethrough. As a result, it is possible to increase luminance and to reduce power consumption.

**[0206]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 6 is partially changed, improved, or transformed. Therefore, the description in Embodiment Modes 1 to 6 can be applied to or combined with this embodiment mode.

**[0207]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 8]

**[0208]** FIG 15A is a plan view illustrating a structure of an IPS mode liquid crystal display device according to Embodiment Mode 8 in the present invention. FIG 15B is a cross-sectional view along a line A-B, a line C-D, and a line E-F of FIG 15A. A structure in this embodiment mode is similar to that of the IPS mode liquid crystal display device according to Embodiment Mode 3, except that a capacitor 118 is provided instead of the capacitor 120b, a second auxiliary wiring 104e is formed, and the opening patterns 112 and 115 have substantially V-shapes. Accordingly, the description in Embodiment Mode 3 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 3 is denoted by the same reference numeral and description thereof is omitted.

**[0209]** The capacitor 118 is connected between the second electrode 108 and the second auxiliary wiring 104e. The capacitor 118 includes the semiconductor film 102e located over the base insulating film 101, the gate insulating film 103 located over the semiconductor film 102e, and a conductive pattern 104d which is formed over the gate insulating film 103 and located above a part of the semiconductor film 102e. The capacitor 118 is located so as not to overlap with the first electrode 102c. The semiconductor film 102e and the conductive pattern 104d are rectangles and are located adjacent to and generally parallel to the auxiliary wiring 104b. The same impurity as in the first electrode 102c is introduced to the semiconductor film 102e except in the region under the conductive pattern 104d.

**[0210]** The contact hole located above the conductive pattern 104d and the contact hole located above the semiconductor film 102e are formed in the first interlayer insulating film 106a. Conductive patterns 107d and 107e

are formed over the first interlayer insulating film 106a. The conductive pattern 107d is electrically connected to the conductive pattern 104d through the contact hole, and the conductive pattern 107e is electrically connected to the region of the semiconductor film 102e, in which an impurity is introduced, through the contact hole. The conductive pattern 107d is an elongated rectangle and is located generally parallel to the auxiliary wiring 104b. The conductive pattern 107e has a substantially frame shape and surrounds the conductive pattern 107d.

**[0211]** The contact hole located above the conductive pattern 107d is formed in the second interlayer insulating film 106b. The second electrode 108 is electrically connected to the conductive patterns 107d and 104d through the contact hole.

**[0212]** The second auxiliary wiring 104e is formed over the gate insulating film 103. The second auxiliary wiring 104e is located adjacent to the auxiliary wiring 104b and extended parallel to the auxiliary wiring 104b. A plurality of contact holes located over the second auxiliary wiring 104e are formed in the first interlayer insulating film 106a. The conductive pattern 107e is electrically connected to the second auxiliary wiring 104e through the contact hole.

**[0213]** The second auxiliary wiring 104e is located in the same layer as the conductive pattern 104d but is separated. In a region in which the second auxiliary wiring 104e is separated, the conductive pattern 104d is located. The separated portions of the second auxiliary wiring 104e are electrically connected to each other through the conductive pattern 107e. In the case where an n-type impurity is introduced to the semiconductor film 102e the potential of the second auxiliary wiring 104e is lower than the lowest potential of the source wiring 107a. In the case where a p-type impurity is introduced to the semiconductor film 102e, the potential of the second auxiliary wiring 104e is higher than the highest potential of the source wiring 107a.

**[0214]** In the liquid crystal display device with such a structure, when a driving thin film transistor is turned on, charge is accumulated in a part of the conductive pattern 104e, which is located under the conductive pattern 104d. The capacitor 118 functions in such a manner.

**[0215]** The semiconductor film 102e is formed in the same step as the semiconductor film 102f. The conductive pattern 104d and the second auxiliary wiring 104e are formed in the same step as the auxiliary wiring 104b. In a step of forming the impurity regions 102b and 102d by injecting an impurity into the semiconductor film 102f, the impurity is injected into a region in the semiconductor film 102e which is not covered with the conductive pattern 104d. The conductive patterns 107d and 107e are formed in the same step as the source wiring 107a. In addition, the contact holes formed in the first interlayer insulating film 106a are formed in the same step, and the contact holes formed in the second interlayer insulating film 106b are formed in the same step. Other steps of the manufacturing steps of the liquid crystal display device are similar to those of the liquid crystal display device ac-

cording to Embodiment Mode 3.

**[0216]** With this embodiment mode, an effect similar to Embodiment Mode 3 can be obtained. In addition, since the capacitor 118 is connected between the second electrode 108 functioning as the pixel electrode and the second auxiliary wiring 104e, the voltage of the second electrode 108 is easily kept when the thin film transistor is turned off. In addition, in the step of forming the impurity regions 102b and 102d by injecting an impurity into the semiconductor film 102f, since the impurity is injected into a region in the semiconductor film 102e, which is not covered with the conductive pattern 104d and the impurity is not required to be injected into a region in the semiconductor film 102e, which is covered with the conductive pattern 104d; the number of manufacturing steps is not necessarily increased.

**[0217]** Note that the capacitor 118 may be provided in Embodiment Mode 1. In that case, an effect similar to this embodiment mode can be obtained.

**[0218]** In embodiment mode, the opening patterns 112 and 115 may have the shape shown in FIGS. 10A and 10B, or 11A and 11B. Alternatively, the opening pattern 112 may have the shape shown in FIGS. 7A and 7B, or 9A and 9B. In this case, the opening pattern 115 has a shape of the opening pattern 112 shown in FIGS. 7A and 7B, or 9A and 9B. Note that the opening patterns 112 and 115 are required to be arranged so that the first electrode 102c and the second electrode 108 are alternately arranged and are generally in parallel except in the periphery portions, when seen from the direction perpendicular to the substrate 100 of the liquid crystal display device.

**[0219]** The impurity region 102b functioning as a drain or a source of the transistor is directly connected to the first electrode 102c. In other words, the semiconductor layer in the transistor and the first electrode 102c are contiguous with each other to form one island. In addition, unlike Embodiment Mode 1, the contact hole located over the impurity region 102b and the contact hole located over the first electrode 102c are not formed in the first interlayer insulating film 106a. Accordingly, the region for the contact holes can be utilized for displaying an image, which leads to improvement in aperture ratio.

**[0220]** If the opening patterns are thus provided to have different orientations, a plurality of regions with different moving directions of liquid crystal molecules can be provided. In other word, a multidomain structure can be realized. When a multidomain structure is employed, it can be prevented that an image cannot be displayed properly if seen from a certain direction. Accordingly, the viewing angle can be improved.

**[0221]** Note that the first electrode 102c has the opening pattern 115 in this embodiment mode. Therefore, in a portion of the opening pattern, the amount of light transmitted therethrough is increased. This is because the first electrode 102 is not provided in that portion. In a portion where the first electrode 102 is provided, the amount of light transmitted therethrough is decreased because the

light transmittance is not 100%. On the other hand, in a portion where the first electrode 102 is not provided, light does not attenuate, which leads to increase in amount of light transmitted therethrough. As a result, it is possible to increase luminance and to reduce power consumption.

**[0222]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 7 is partially changed, improved, or transformed. Therefore, the description in Embodiment Modes 1 to 7 can be applied to or combined with this embodiment mode.

**[0223]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 9]

**[0224]** FIG 16A is a circuit diagram of a liquid crystal display device according to Embodiment Mode 9. In the liquid crystal display device according to this embodiment mode, a plurality of pixels are arranged in matrix. A structure of each pixel is similar to the structure of the liquid crystal display device according to Embodiment Mode 7, except that a second auxiliary wiring 104f extended in a longitudinal direction is formed. The second auxiliary wiring 104f is formed in the same layer as the auxiliary wiring 104b and is electrically connected to the auxiliary wirings 104b at each intersection with the auxiliary wirings 104b.

**[0225]** According to this embodiment mode, an effect similar to Embodiment Mode 7 can be obtained. Further, by provision of the second auxiliary wiring 104f, the potential of the common electrode can be easily held at the same value in all pixels. Note that the liquid crystal display device according to this embodiment mode may be the FFS mode or the IPS mode. Although opening patterns included in the pixel electrode and the common electrode may have a shape similar to those shown in Embodiment Modes 1 to 8, it is not limited thereto.

**[0226]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 8 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 8 can be applied to or combined with this embodiment mode.

**[0227]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 10]

**[0228]** FIG. 16B is a circuit diagram of a liquid crystal display device according to Embodiment Mode 10. In the liquid crystal display device according to this embodiment mode, a plurality of pixels are arranged in matrix. A structure of each pixel is similar to the structure of the liquid crystal display device according to Embodiment Mode 8.



**[0229]** According to this embodiment mode, an effect similar to Embodiment Mode 8 can be obtained. Note that the liquid crystal display device according to this embodiment mode may be the FFS mode or the IPS mode. Although opening patterns included in the pixel electrode and the common electrode may have a shape similar to those shown in Embodiment Modes 1 to 8, it is not limited thereto.

**[0230]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 9 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 9 can be applied to or combined with this embodiment mode.

**[0231]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 11]

**[0232]** FIG 17A is a circuit diagram of a liquid crystal display device according to Embodiment Mode 11. The liquid crystal display device according to this embodiment mode is the FFS mode or the IPS mode, and one pixel includes a plurality of (for example, two) subpixels. A structure of each subpixel is similar to any of the structures of the pixel shown in Embodiment Modes 1 to 10. Therefore, the description in Embodiment Modes 1 to 10 can be applied to this embodiment mode. FIG. 17A shows an example where the pixel has a structure similar to that shown in Embodiment Mode 7. Hereinafter, the component similar to that of Embodiment Mode 7 is denoted by the same reference numeral and description thereof is omitted.

**[0233]** A plurality of subpixels forming one pixel are electrically connected to the same gate wiring 104c and are electrically connected to the different auxiliary wirings 104b from each other.

**[0234]** According to this embodiment mode, an effect similar to the liquid crystal display device shown in Embodiment Modes 1 to 10 can be obtained. Furthermore, since one pixel includes a plurality of subpixels, a viewing angle can be further increased. Effects in which the pixel can have redundancy and area gray scale display can be realized can be obtained as well.

**[0235]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 10 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 10 can be applied to or combined with this embodiment mode.

**[0236]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 12]

**[0237]** FIG 17B is a circuit diagram of a liquid crystal display device according to Embodiment Mode 12. The liquid crystal display device according to this embodiment mode is the FFS mode or the IPS mode. A structure is similar to that of Embodiment Mode 11, except that a plurality of subpixels forming one pixel are electrically connected to the different gate wirings 104c from each other and are electrically connected to the same auxiliary wiring 104b. A structure of each of subpixels is similar to any of the structures of the pixel shown in Embodiment Modes 1 to 10. Therefore, the description in Embodiment Modes 1 to 10 can be applied to this embodiment mode. FIG 17B shows an example where the pixel has a structure similar to that shown in Embodiment Mode 7. Hereinafter, the component similar to that of Embodiment Mode 7 is denoted by the same reference numeral and description thereof is omitted. According to this embodiment mode, an effect similar to Embodiment Mode 11 can be obtained.

**[0238]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 11 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 11 can be applied to or combined with this embodiment mode.

**[0239]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 13]

**[0240]** FIG 18A is a plan view illustrating a structure of a liquid crystal display device according to Embodiment Mode 13 in the present invention. FIG 18B is a cross-sectional view along a line A-B and a line C-D of FIG 18A. A structure of this embodiment mode is similar to that of Embodiment Mode 1, except that a transistor for driving a pixel is a bottom gate transistor and the base insulating film 101 is not formed. That is, the liquid crystal display device in this embodiment mode is the FFS mode. Therefore, the description in Embodiment Mode 1 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 1 is denoted by the same reference numeral and description thereof is omitted.

**[0241]** In this embodiment mode, the gate electrode 104a, the auxiliary wiring 104b, and the gate wiring 104c are formed over the substrate 100. The gate insulating film 103 is formed over the substrate 100, the gate electrode 104a, the auxiliary wiring 104b, and the gate wiring 104c. The semiconductor film 102f and the first electrode 102c are formed over the gate insulating film 103.

**[0242]** A manufacturing method of the liquid crystal display device according to this embodiment mode is as

follows. First, a conductive film is formed over the substrate 100 and is selectively etched. Therefore, the two gate electrodes 104a, the auxiliary wiring 104b, and the gate wiring 104c are formed over the substrate 100. Note that as the conductive film, a film formed of aluminum (Al), nickel (Ni), tungsten (W), molybdenum (Mo), titanium (Ti), tantalum (Ta), neodymium (Nd), platinum (Pt), gold (Au), silver (Ag), or the like; a film formed of an alloy thereof; or a stacked-layer film thereof can be used. Alternatively, silicon (Si) in which an n-type impurity is introduced may be used. Next, the gate insulating film 103 is formed.

**[0243]** Next, a polysilicon film is formed over the gate insulating film 103, and a resist pattern is formed over the polysilicon film. Next, the polysilicon film is etched with use of the resist pattern as a mask. In this manner, the semiconductor film 102f and the first electrode 102c are formed in the same step. Thereafter, the resist pattern is removed.

**[0244]** Next, a mask pattern is formed over the semiconductor film 102f, and an impurity is injected into the semiconductor film 102f with use of the mask pattern as a mask. Therefore, the impurity regions 102b and 102d and an impurity region between the gate electrodes 104a are formed. Note that by this treatment, the impurity is also injected into the first electrode 102c. In a case where the substrate 100 is formed using a light-transmitting material such as glass, a mask may be formed by light exposure from a rear face of the substrate 100 with use of the gate wiring as a light exposure pattern, without using a light exposure mask. In this case, the number of steps can be reduced since a light exposure mask is not used, so that manufacturing cost can be reduced. Further, there is an advantage in that a mask pattern can be formed in a self-aligned manner, so that deviation of a mask pattern is reduced and the deviation is not required to be considered. Subsequent steps are similar to those in Embodiment Mode 1.

**[0245]** According to this embodiment mode, an effect similar to Embodiment Mode 1 can be obtained. Note that in the FFS mode liquid crystal display device shown in Embodiment Mode 2 or 5, the transistor for driving a pixel may be a bottom gate transistor having a structure similar to this embodiment mode. Further, in the IPS mode liquid crystal display device shown in any one of Embodiment Modes 3, 4, and 6 to 12, the transistor for driving a pixel may be a bottom gate transistor having a structure similar to this embodiment mode. In this manner, in any of the aforementioned FFS mode liquid crystal display devices and IPS mode liquid crystal display devices, the bottom gate transistor can be adopted.

**[0246]** In the liquid crystal display device according to this embodiment mode, or in the liquid crystal display device in any of Embodiment Modes 1 to 12, of which transistor for driving the pixel is a bottom gate transistor having a structure similar to this embodiment mode, the gate insulating layer 103 over the substrate 100 may be removed except in a portion around the gate electrode

104a before the polysilicon film is formed over the gate insulating layer 103. In this case, the first electrode 102c is formed directly on the substrate 100.

**[0247]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 12 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 12 can be applied to or combined with this embodiment mode.

**[0248]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 14]

**[0249]** FIG. 19A is a cross-sectional view illustrating a structure of a liquid crystal display device according to Embodiment Mode 14 in the present invention. The cross-sectional view corresponds to a cross section A-B and a cross section C-D of FIGS. 12A and 12B. A structure of this embodiment mode is similar to that of the FFS mode liquid crystal display device in Embodiment Mode 5, except that all parts of the second electrode 108 are provided over the first interlayer insulating film 106a and a part of the drain wiring 107b is provided over the second electrode 108. In this embodiment mode, the drain wiring 107b is formed after the second electrode 108 is formed. Breakage of the second electrode 108 can be prevented by such a structure. That is, if the second electrode 108 is formed over the drain wiring 107b as shown in Embodiment Mode 5, the drain wiring 107b is often made thicker than the second electrode 108, so that breakage of the second electrode 108 might be caused at an end portion of the drain wiring 107b. On the other hand, when the second electrode 108 is formed under the drain wiring 107b as shown in this embodiment mode, the breakage of the second electrode 108 can be prevented. Note that since the drain wiring 107b is often formed to be thick, breakage of the drain wiring 107b is unlikely to be caused.

**[0250]** In addition, a manufacturing method of the liquid crystal display device according to this embodiment mode is generally similar to that of Embodiment Mode 5. Therefore, the description in Embodiment mode 5 can be applied to this embodiment mode. Hereinafter, a component same as Embodiment Mode 5 is denoted by the same reference numeral and description thereof is omitted. Note that although the opening pattern 112 included in the second electrode 108 can have a shape shown in any of Embodiment Modes 1 to 4 and 7, it is not limited thereto.

**[0251]** According to this embodiment mode, an effect similar to Embodiment Mode 5 can be obtained. Note that an opening pattern parallel to the opening pattern 112 included in the second electrode 108 may be formed in the first electrode 102c, so that the IPS mode liquid crystal display device can be realized. The opening pat-

tern can have a shape shown in any of Embodiment Modes 1 to 4 and 7. Note that the opening pattern in the first electrode 102c and the opening pattern 112 are required to be arranged so that the first electrode 102c and the second electrode 108 are alternately arranged and generally in parallel except in the peripheral portions when seen from the direction perpendicular to the substrate 100 of the liquid crystal display device.

**[0252]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 13 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 13 can be applied to or combined with this embodiment mode.

**[0253]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 15]

**[0254]** FIG. 19B is a cross-sectional view illustrating a structure of a liquid crystal display device according to Embodiment Mode 15 in the present invention. The cross-sectional view corresponds to a cross section A-B and a cross section C-D of FIGS. 7A and 7B. A structure of this embodiment mode is similar to that of the FFS mode liquid crystal display device in Embodiment Mode 1, except that a second drain wiring 116 is formed over the second interlayer insulating film 106b and the second electrode 108 is formed so as to cover the second drain wiring 116. Note that the second electrode 108 may partially overlap the second drain wiring 116. In addition, a manufacturing method of the liquid crystal display device according to this embodiment mode is generally similar to that of Embodiment Mode 1. Therefore, the description in Embodiment mode 1 can be applied to this embodiment mode. Hereinafter, a component same as Embodiment Mode 1 is denoted by the same reference numeral and description thereof is omitted. Note that although the opening pattern 112 included in the second electrode 108 can have a shape shown in any of Embodiment Modes 1 to 4 and 7, it is not limited thereto.

**[0255]** According to this embodiment mode, an effect similar to Embodiment Mode 1 can be obtained. Note that the opening pattern parallel to the opening pattern 112 included in the second electrode 108 may be formed in the first electrode 102c, so that the IPS mode liquid crystal display device can be realized. The opening pattern can have a shape shown in any of Embodiment Modes 1 to 4 and 7. Note that the opening pattern in the first electrode 102c and the opening pattern 112 are required to be arranged so that the first electrode 102c and the second electrode 108 are alternately arranged and generally in parallel except in the peripheral portions when seen from the direction perpendicular to the substrate 100 of the liquid crystal display device.

**[0256]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 14 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 14 can be applied to or combined with this embodiment mode.

**[0257]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 16]

**[0258]** FIG. 20 is a cross-sectional view illustrating a structure of a pixel portion in an FFS mode liquid crystal display device according to Embodiment Mode 16 in the present invention. A structure of the pixel portion of the liquid crystal display device according to this embodiment mode is generally similar to that of the liquid crystal display device in Embodiment Mode 1, except that a red color filter 130r, a green color filter 130g, and a blue color filter 130b are provided instead of the first interlayer insulating film 106a. Therefore, the description in Embodiment mode 1 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 1 is denoted by the same reference numeral and description thereof is omitted. Note that since the insulating film 105 is provided between the semiconductor film 102f and the color filters 130r, 130g, and 130b, it also functions to suppress diffusion of impurities from each color filter to the semiconductor film 102f.

**[0259]** A manufacturing method of the liquid crystal display device according to this embodiment mode is similar to that of Embodiment Mode 1, except that a step of forming the color filters 130r, 130g, and 130b is added instead of a step of forming the first interlayer insulating film 106a. The color filters 130r, 130g, and 130b are formed by repeating the following steps three times: a step of forming a color filter layer, a step of forming a resist pattern over the color filter layer, and a step of selectively dry-etching the color filter layer with use of the resist pattern as a mask. Note that the second interlayer insulating film 106b is embedded in a space which is generated between color filters. Alternatively, the color filters 130r, 130g, and 130b can be formed by using a droplet discharging method (such as an ink-jet method).

**[0260]** Accordingly, the number of manufacturing steps can be reduced. Further, since the color filter is provided on the substrate 100 side, reduction in an aperture ratio can be suppressed even when misalignment with the opposite substrate is caused, as compared with a case where a color filter is provided on the opposite substrate side. That is, a margin for the misalignment of the opposite substrate is increased.

**[0261]** Note that colors of the color filter may be a color other than red, blue, and green; or may be more than three colors, for example, four colors or six colors. For

example, yellow, cyan, magenta, or white may be added. Further, a black matrix (also called a black mask) may be provided in addition to the color filters.

**[0262]** FIG 21A is a plan view of the liquid crystal display device shown in FIG. 20. As shown in FIG 21A, in the liquid crystal display device, a source line driver circuit 160 and a gate line driver circuit 170, which are peripheral driver circuits, are provided in the periphery of a pixel portion 150. The red color filter 130r is provided over each of the source line driver circuit 160 and the gate line driver circuit 170. By provision of the red color filter 130r, light degradation of an active layer in a thin film transistor included in the source line driver circuit 160 and the gate line driver circuit 170 is prevented, and planarization is realized.

**[0263]** FIG 21B is an enlarged view of a part of the pixel portion 150 (three rows x three columns) in FIG 21A. In the pixel portion 150, the red color filter 130r, the blue color filter 130b, and the green color filter 130g are alternately arranged in stripes. Further, the red color filter 130r is provided over a thin film transistor included in each pixel.

**[0264]** Since a source wiring (not shown) and a gate wiring (not shown) are arranged so as to overlap with the space between each color filter, light leakage is suppressed.

**[0265]** Since the color filter 130r functions as a black mask in this manner, a step of forming a black mask, which is conventionally required, can be omitted.

**[0266]** As described above, according to this embodiment mode, an effect similar to Embodiment Mode 1 can be obtained. Further, since the color filters 130r, 130b, and 130g are provided instead of the first interlayer insulating film 106a, the number of manufacturing steps of the liquid crystal display device can be reduced. Moreover, reduction in an aperture ratio can be suppressed even when misalignment with the opposite substrate is caused, as compared with a case where the color filter is provided on the opposite substrate side. That is, a margin for the misalignment of the opposite substrate is increased.

**[0267]** Note that in the FFS mode or the IPS mode liquid crystal display devices shown in Embodiment Modes 2 to 4, 6 to 13, and 15, the color filters 130r, 130b, and 130g may be provided instead of the first interlayer insulating film 106a similar to this embodiment mode. In this case, an effect similar to this embodiment mode can be obtained.

**[0268]** Note that although a color filter may be provided between the gate electrode and the source wiring, it is not limited thereto. The color filter may be provided between the source wiring and the second electrode 108.

**[0269]** Further, a black matrix may be provided in addition to a color filter.

**[0270]** Note that an insulating film of an inorganic material may be provided between the color filter and the source wiring, or between the color filter and the second electrode 108. The inorganic material is formed of an

insulating substance containing oxygen or nitride, such as silicon oxide ( $\text{SiO}_x$ ), silicon nitride ( $\text{SiN}_x$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y$  :  $x > y$ ), or silicon nitride oxide ( $\text{SiN}_x\text{O}_y$  :  $x > y$ ). In order to block intrusion of impurities, a material containing a large amount of nitrogen is preferably employed.

**[0271]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 15 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 15 can be applied to or combined with this embodiment mode.

**[0272]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 17]

**[0273]** FIG. 22A is a plan view illustrating a structure of an FFS mode liquid crystal display device according to Embodiment Mode 17 in the present invention. FIG 22B is an enlarged view illustrating a structure of a pixel portion in FIG 22A. A structure of the liquid crystal display device according to this embodiment mode is similar to that of Embodiment Mode 16, except for the layout of the color filters 130r, 130b, and 130g. Therefore, the description in Embodiment mode 16 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Mode 16 is denoted by the same reference numeral and description thereof is omitted.

**[0274]** In this embodiment mode, the pixels provided with the color filter 130r, 130b, or 130g are arranged in matrix so that the color filters 130r, 130b, and 130g are alternately arranged. Specifically, the red color filter 130r is provided so as to fill a gap between the blue color filter 130b and the green color filter 130g. Further, the red color filter 130r is also provided over the source line driver circuit 160 and the gate line driver circuit 170, which are peripheral driver circuits; and provided in spaces between the pixel portion 150 and each of the source line driver circuit 160 and the gate line driver circuit 170. Therefore, generation of a space between color filters is suppressed.

**[0275]** According to this embodiment mode, an effect similar to Embodiment Mode 16 can be obtained. Note that after the first interlayer insulating film 106a is formed, the color filters 130r, 130b, and 130g may be provided instead of the second interlayer insulating film 106b. In this case, an effect similar to this embodiment mode can be obtained.

**[0276]** Note that in the FFS mode or the IPS mode liquid crystal display devices shown in Embodiment Modes 2 to 4, 6 to 13, and 15, the color filters 130r, 130b, and 130g may be provided instead of the first interlayer insulating film 106a similar to this embodiment mode. In this case, an effect similar to this embodiment mode can

be obtained.

**[0277]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 16 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 16 can be applied to or combined with this embodiment mode.

**[0278]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

#### [Embodiment Mode 18]

**[0279]** FIG. 23 is a cross-sectional view illustrating a structure of an FFS mode liquid crystal display device according to Embodiment Mode 18 in the present invention. A structure of the liquid crystal display device according to this embodiment mode is similar to that in Embodiment Mode 5, except that the color filters 130r, 130b, and 130g are provided instead of the first interlayer insulating film 106a. The layout of the color filters 130r, 130b, and 130g in this embodiment mode is similar to that of Embodiment Mode 17. Therefore, the description in Embodiment modes 5 and 17 can be applied to this embodiment mode. Hereinafter, the component similar to that of Embodiment Modes 5 and 17 is denoted by the same reference numeral and description thereof is omitted.

**[0280]** According to this embodiment mode, an effect similar to Embodiment Mode 17 can be obtained. Note that in the FFS mode liquid crystal display devices shown in Embodiment Mode 14, the color filters 130r, 130b, and 130g may be provided instead of the first interlayer insulating film 106a similar to this embodiment mode. In this case, an effect similar to this embodiment mode can be obtained.

**[0281]** Note that the layout of the color filters 130r, 130b, and 130g is not limited to those shown in Embodiment Modes 16 to 18, and various layouts such as a triangle mosaic arrangement, an RGBG four pixel arrangement, or an RGBW four pixel arrangement may be employed. In these cases, the red color filter 130r is preferably provided above an active layer of a thin film transistor.

**[0282]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 17 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 17 can be applied to or combined with this embodiment mode.

**[0283]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

#### [Embodiment Mode 19]

**[0284]** Each of FIGS. 24A to 24D is a plan view illustrating a structure of an electrode of an FFS mode liquid crystal display device according to Embodiment Mode 19 in the present invention. Since a structure shown in each drawing is similar to the FFS mode liquid crystal display device according to Embodiment Mode 1, except for a shape of the second electrode 108, components other than the first electrode 102c and the second electrode 108 are not shown in the drawing.

**[0285]** In FIG 24A, the second electrode 108 has a comb shape. A space between each comb-tooth functions as the opening pattern 112 shown in Embodiment Mode 1.

**[0286]** In FIG 24B, the second electrode 108 has a shape in which a plurality of electrodes each having a shape along a circumference of a circle, of which radius is different from each other, are arranged in a concentric pattern and is connected to each other. A space between each electrode functions as the opening pattern 112 shown in Embodiment Mode 1.

**[0287]** In FIG 24C, the second electrode 108 has a shape in which a plurality of linear electrodes extended in a long side direction of the rectangular first electrode 102c are arranged over the first electrode 102c so as not to overlap with each other; and each of the linear electrodes has its upper portion connected to an upper portion of an adjacent linear electrode and its lower end portion connected to a lower end portion of the other adjacent linear electrode. That is, the second electrode 108 has a shape in which an elongated electrode is led up and down repeatedly over the first electrode 102c, and its one end portion is arranged nearest to one long side of the first electrode 102c (in FIG 24C, a long side on the right side) and is connected nowhere. Further, a space between each linear electrode functions as the opening pattern 112 shown in Embodiment Mode 1.

**[0288]** In FIG. 24D, the second electrode 108 has a shape in which in the second electrode 108 shown in FIG 24C, the end portion nearest to one long side of the first electrode 102c (in FIG 24C, the long side on the right side) is further extended and led along a short side of the first electrode 102c (in FIG 24D, a short side on the upper side), and connected to a portion nearest to the other long side of the first electrode 102c (in FIG 24C, the long side on the left side). Since both the end portions of the second electrode 108 are connected to each other, a potential of the second electrode 108 can be easily kept constant as compared with the shape shown in FIG 24C.

**[0289]** A manufacturing method of the liquid crystal display device according to this embodiment mode is generally similar to that of Embodiment Mode 1 in each case. Therefore, the description in Embodiment mode 1 can be applied to this embodiment mode.

**[0290]** According to this embodiment mode, an effect similar to Embodiment Mode 1 can be obtained. Note that in Embodiment Modes 2, 5, and 13 to 18, the second

electrode 108 may have a shape shown in any of FIGS. 24A to 24D.

**[0291]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 18 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 18 can be applied to or combined with this embodiment mode.

**[0292]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 20]

**[0293]** Each of FIGS. 25A to 25D is a plan view illustrating a structure of an electrode of an IPS mode liquid crystal display device according to Embodiment Mode 20 in the present invention. Since a structure of this embodiment mode is similar to that of Embodiment Mode 3, except for the shape of the first electrode 102c and the second electrode 108, components other than the first electrode 102c and the second electrode 108 are not shown in the drawing.

**[0294]** In FIG 25A, each of the first electrode 102c and the second electrode 108 has a comb shape, and is arranged to face opposite directions from each other. Comb-teeth are alternately arranged.

**[0295]** In FIG. 25B, the first electrode 102c has a shape in which the circular opening pattern 115 is provided at the center of its rectangular body; and in the opening pattern 115, a plurality of electrodes each having a shape along a circumference of a circle, of which radius are different from each other, are arranged concentrically with the opening pattern 115 and each electrode having a shape along the circumference of the circle is connected to the body by one linear electrode. The second electrode 108 has a shape in which the circular opening pattern 112 is provided at the center of the rectangular body; and in the opening pattern 112, an electrode having a shape along the circumference of the circle is arranged concentrically with the opening pattern 112 and the electrode and the body are connected by a linear electrode. Note that the electrode having a shape along the circumference of the circle included in the second electrode 108 may be plural.

**[0296]** Since the opening patterns 112 and 115 are concentric with each other, the electrode having a shape along the circumference of the circle included in the first electrode 102c and the electrode having a shape along the circumference of the circle included in the second electrode 108 are concentric with each other. Note that the electrode having a shape along the circumference of the circle included in the first electrode 102c and the electrode having a shape along the circumference of the circle included in the second electrode 108 have different radii from each other, so that they are alternately ar-

ranged in parallel with each other.

**[0297]** In FIG. 25C, the first electrode 102c has a shape in which a plurality of linear electrodes extended up and down in the drawing are arranged in parallel with each other and each of upper end portions or lower end portions thereof is connected by a linear electrode extended in the lateral direction in the drawing. The second electrode 108 has a comb shape, and comb-teeth are provided in a space between the linear electrodes forming the first electrode 102c.

**[0298]** In FIG 25D, the first electrode 102c and the second electrode 108 have a shape in which a plurality of linear electrodes extended up and down in the drawing are arranged in parallel with each other so as not to overlap with each other; and each of the linear electrodes has its upper portion connected to an upper portion of an adjacent linear electrode and its lower end portion connected to a lower end portion of the other adjacent linear electrode. That is, the second electrode 108 has a shape in which an elongated electrode is led up and down repeatedly over the first electrode 102c. Further, in the first electrode 102c and the second electrode 108, portions extended up and down in the drawing are alternately arranged in parallel with each other, and portions extended in the lateral direction do not overlap with each other.

**[0299]** A manufacturing method of the liquid crystal display device according to this embodiment mode is generally similar to that of Embodiment Mode 3 in each case. Therefore, the description in Embodiment mode 3 can be applied to this embodiment mode.

**[0300]** According to this embodiment mode, an effect similar to Embodiment Mode 3 can be obtained. Note that in Embodiment Modes 4, and 6 to 12, the first electrode 102c and the second electrode 108 may have a shape shown in any of FIGS. 25A to 25D.

**[0301]** In addition, in each embodiment mode described above, another semiconductor film (for example, an organic semiconductor film or an amorphous silicon film) may be used instead of the semiconductor film 102f. In this case, the first electrode 102c may also be formed of the aforementioned another semiconductor film.

**[0302]** Note that this embodiment mode shows an example in a case where the description in Embodiment Modes 1 to 19 is partially changed, improved, transformed, or is described from a different perspective. Therefore, the description in Embodiment Modes 1 to 19 can be applied to or combined with this embodiment mode.

**[0303]** In addition, description is made with reference to various drawings. One drawing includes various components. Therefore, another structure can be made by combining components selected from different drawings.

[Embodiment Mode 21]

**[0304]** FIGS. 32A and 32B are cross-sectional views illustrating a structure of an inorganic EL element using the present invention. The inorganic EL element accord-

ing to the present invention has a structure using a bottom gate transistor, and the structure is similar to the liquid crystal display device according to Embodiment Mode 13 in that the first electrode 102c and the second electrode 108 are used. A structure of a transistor, an electrode, or the like is not limited to that shown in this embodiment mode; and a top gate transistor or a structure of an electrode shown in another embodiment mode may be used. Although only one transistor is shown in the cross-sectional views shown in this embodiment mode, a structure where a plurality of transistors, such as a driving transistor, a selection transistor, or a transistor for controlling current, are included in one pixel may be employed. As a material to be used for the second electrode, one or more elements selected from aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), neodymium (Nd), chromium (Cr), nickel (Ni), platinum (Pt), gold (Au), silver (Ag), copper (Cu), magnesium (Mg), scandium (Sc), cobalt (Co), zinc (Zn), niobium (Nb), silicon (Si), phosphorus (P), boron (B), arsenic (As), gallium (Ga), indium (In), and tin (Sn); a compound or an alloy material containing one or more of the aforementioned elements (such as indium tin oxide (ITO), indium zinc oxide (IZO), indium tin oxide doped with silicon oxide (ITSO), zinc oxide (ZnO), aluminum neodymium (Al-Nd), or magnesium silver (Mg-Ag)); a substance obtained by combining such compounds; or the like may be employed. Alternatively, a compound (silicide) of silicon and the aforementioned material (such as aluminum silicon, molybdenum silicon, or nickel silicide) or a compound of nitride and the aforementioned material (such as titanium nitride, tantalum nitride, or molybdenum nitride) can be used. Note that silicon (Si) may contain a large amount of n-type impurities (phosphorus or the like) or p-type impurities (boron or the like).

**[0305]** Inorganic EL elements are classified into a dispersion-type inorganic EL element and a thin-film type inorganic EL element, according to the structure of the element. These differ in that the former includes a layer including a light emitting material, in which particles of the light emitting material are dispersed in a binder, and the latter includes a layer including a light emitting material formed as a thin film. However, the dispersion-type inorganic EL element and the thin-film type inorganic EL element are common in that electrons accelerated by a high electric field are required. In this embodiment mode, a layer 501 including a light emitting material is provided above the second electrode 108. In a case of a dispersion-type inorganic EL element, a structure where the layer 501 including the light emitting material is provided on and in contact with the second electrode 108 (see FIG 32A) is preferably employed; however, it is not limited thereto. In a case of a thin-film type inorganic EL element, a structure where a dielectric 502 is formed over the second electrode 108 and the layer 501 including the light emitting material is provided over the dielectric 502 (see FIG 32B) is preferably employed; however, it is not limited thereto.

**[0306]** As a mechanism of light emission, donor-acceptor recombination emission in which a donor level and an acceptor level are utilized, and local emission in which inner shell electron transition in a metal ion is utilized are known. Generally, the dispersion-type inorganic EL element typically employs donor-acceptor recombination emission and the thin-film type inorganic EL element typically employs local emission.

**[0307]** The layer 501 including the light emitting material includes a base material and an impurity element to be a luminescent center. By change of the impurity element to be included, various colors of light emission can be obtained. As a manufacturing method of the light emitting material, a spraying thermal decomposition method, a double decomposition method, a method by thermal decomposition reaction of a precursor, a reversed micelle method, a method in which these methods and high temperature firing are combined, a freeze-drying method, or the like can be used.

**[0308]** The solid phase method is a method in which a compound including a base material and an impurity element or a compound including the impurity element are weighed, mixed in a mortar, heated in an electric-furnace, and baked to react so that the impurity element is included in the base material. The baking temperature is preferably 700 to 1500 °C. This is because solid-phase reaction does not proceed when the temperature is too low, and the base material is decomposed when the temperature is too high. Note that although baking may be performed in a powder state, it is preferably performed in a pellet state. It is suitable for mass-production since it is a simple method with high productivity even though baking at a comparatively high temperature is required.

**[0309]** The liquid phase method (the coprecipitation method) is a method in which a base material or a compound including the base material, and an impurity element or a compound including the impurity element are reacted in a solution, dried, and then baked. The particles of the light emitting material are dispersed uniformly, and the reaction can be advanced even if the particles are small and baking temperature is low.

**[0310]** As the base material to be used for the light emitting material, a sulfide, an oxide, or a nitride can be used. As a sulfide, zinc sulfide (ZnS), cadmium sulfide (CdS), calcium sulfide (CaS), yttrium sulfide (Y<sub>2</sub>S<sub>3</sub>), gallium sulfide (Ga<sub>2</sub>S<sub>3</sub>), strontium sulfide (SrS), barium sulfide (BaS), or the like can be used, for example. As an oxide, zinc oxide (ZnO), yttrium oxide (Y<sub>2</sub>O<sub>3</sub>), or the like can be used, for example.

**[0311]** In addition, as a nitride, aluminum nitride (AlN), gallium nitride (GaN), indium nitride (InN), or the like can be used, for example. Alternatively, zinc selenide (ZnSe), zinc telluride (ZnTe), or the like; or a ternary mixed crystal such as calcium sulfide-gallium (CaGa<sub>2</sub>S<sub>4</sub>), strontium sulfide-gallium (SrGa<sub>2</sub>S<sub>4</sub>), or barium sulfide-gallium (BaGa<sub>2</sub>S<sub>4</sub>) may be used.

**[0312]** As a luminescent center of local emission, manganese (Mn), copper (Cu), samarium (Sm), terbium (Tb),

erbium (Er), thulium (Tm), europium (Eu), cerium (Ce), praseodymium (Pr), or the like can be used. For charge compensation, a halogen element such as fluorine (F) or chlorine (Cl) may be added.

**[0313]** On the other hand, as a luminescent center of donor-acceptor recombination emission, a light emitting material including a first impurity element forming a donor level and a second impurity element forming an acceptor level can be used. As the first impurity element, fluorine (F), chlorine (Cl), aluminum (Al), or the like can be used, for example. As the second impurity element, copper (Cu), silver (Ag), or the like can be used, for example.

**[0314]** Note that in the inorganic EL light emitting element, a voltage is applied between a pair of electrodes so that light emission can be obtained. In this embodiment mode, AC drive is preferably used since an electric field formed by the first electrode 102c and the second electrode 108 is used for light emission in the inorganic EL light emitting element shown in this embodiment mode. Note that the electric field formed for light emission is similar to the electric field in the liquid crystal display device shown in other embodiment modes.

**[0315]** As a binder which can be used in this embodiment mode, an organic or inorganic insulating material, or a mixed material of an organic material and an inorganic material can be used. As the organic insulating material, the following resin can be used: a polymer having a comparatively high dielectric constant such as a cyanoethyl cellulose based resin; or a resin such as polyethylene, polypropylene, a polystyrene based resin, a silicone resin, an epoxy resin, or vinylidene fluoride. Further, a heat-resistant high-molecular material such as aromatic polyamide or polybenzimidazole, or a siloxane resin may also be used.

**[0316]** Alternatively, the following resin material may also be used: a vinyl resin such as polyvinyl alcohol or polyvinylbutyral, a phenol resin, a novolac resin, an acrylic resin, a melamine resin, a urethane resin, an oxazole resin (polybenzoxazole), or the like. Further, a photo-curable resin or the like can be used. Fine particles having a high dielectric constant such as barium titanate ( $\text{BaTiO}_3$ ) or strontium titanate ( $\text{SrTiO}_2$ ) may be mixed to these resins as appropriate, so that a dielectric constant can be adjusted.

**[0317]** As the inorganic material used for the binder, silicon oxide ( $\text{SiO}_x$ ), silicone nitride ( $\text{SiN}_x$ ), silicon containing oxygen and nitrogen, aluminum nitride (AlN), aluminum containing oxygen and nitrogen, aluminum oxide ( $\text{Al}_2\text{O}_3$ ), titanium oxide ( $\text{TiO}_2$ ),  $\text{BaTiO}_3$ ,  $\text{SrTiO}_3$ , lead titanate ( $\text{PbTiO}_3$ ), potassium niobate ( $\text{KNbO}_3$ ), lead niobate ( $\text{PbNbO}_3$ ), tantalum oxide ( $\text{Ta}_2\text{O}_5$ ), barium tantalate ( $\text{BaTa}_2\text{O}_6$ ), lithium tantalate ( $\text{LiTaO}_3$ ), yttrium oxide ( $\text{Y}_2\text{O}_3$ ), zirconium oxide ( $\text{ZrO}_2$ ), ZnS, or a material selected from a substance including other inorganic materials can be employed. By adding the inorganic material having a high dielectric constant in the organic material (by doping or the like), the dielectric constant of a layer including a light emitting substance formed of the light

emitting material and the binder can be controlled, and the dielectric constant can be further increased.

**[0318]** As shown in this embodiment mode, an electrode containing silicon is used as an electrode of the inorganic EL element, so that the inorganic EL element can be manufactured at low cost. By the structure shown in this embodiment mode, various electrode materials can be applied since attenuation by the electrode is not required to be considered. For example, the second electrode may be formed using a metal material so as to be thick. Further, since a layer including a light emitting material is not required to be provided between the first electrode and the second electrode, luminance as a display device can be improved; a load for the EL element can be reduced; and deterioration of the element can be reduced.

[Embodiment Mode 22]

**[0319]** FIG 33 is a cross-sectional view illustrating a structure of an organic EL element which uses an electrode containing silicon in the present invention. The organic EL element according to this embodiment mode has a structure where a bottom gate transistor 600 is used. In this embodiment mode, a layer 601 including an organic compound is interposed between the first electrode 102c and a second electrode 602. A structure of a transistor is not limited to that shown in this embodiment mode, and a top gate transistor may be used. As a material used for the second electrode, one or more elements selected from aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), neodymium (Nd), chromium (Cr), nickel (Ni), platinum (Pt), gold (Au), silver (Ag), copper (Cu), magnesium (Mg), scandium (Sc), cobalt (Co), zinc (Zn), niobium (Nb), silicon (Si), phosphorus (P), boron (B), arsenic (As), gallium (Ga), indium (In), tin (Sn), and oxygen (O); a compound or an alloy material containing one or more of the aforementioned elements (such as indium tin oxide (ITO), indium zinc oxide (IZO), indium tin oxide doped with silicon oxide (ITSO), zinc oxide (ZnO), aluminum neodymium (Al-Nd), or magnesium silver (Mg-Ag)); a substance obtained by combining such compounds; or the like may be employed. Alternatively, a compound (silicide) of silicon and the aforementioned material (such as aluminum silicon, molybdenum silicon, or nickel silicide) or a compound of nitride and the aforementioned material (such as titanium nitride, tantalum nitride, or molybdenum nitride) can be used. Note that silicon (Si) may contain a large amount of n-type impurities (phosphorus or the like) or p-type impurities (boron or the like).

**[0320]** The layer 601 including the organic compound includes at least a layer (light emitting layer) including a material with a high light emitting property. There is no particular limitation on the light emitting layer; however, a layer functioning as the light emitting layer has roughly two modes. One is a host-guest type layer which includes a light emitting substance dispersed in a layer formed of



a material (host material) having an energy gap larger than an energy gap of a substance (light emitting substance or guest material) to be a luminescent center. The other is a layer in which a light emitting layer includes only a light emitting material. The former is preferable since concentration quenching hardly occurs. As the light emitting substance, the following can be employed: 4-dicyanomethylene-2-methyl-6-(1,1,7,7-tetramethyljulolidyl-9-enyl)-4*H*-pyran (abbreviation: DCJT); 4-dicyanomethylene-2-*t*-butyl-6-(1,1,7,7-tetramethyljulolidyl-9-enyl)-4*H*-pyran; perflanthene; 2,5-dicyano-1,4-bis[2-(10-methoxy-1,1,7,7-tetramethyljulolidyl-9-enyl)]benzene; *N,N*'-dimethylquinacridone (abbreviation: DMQd); coumarin 6; coumarin 545T; tris(8-quinolinolato)aluminum (abbreviation: Alq<sub>3</sub>); 9,9'-bianthryl; 9,10-diphenylanthracene (abbreviation: DPA); 9,10-bis(2-naphthyl)anthracene (abbreviation: DNA); 2,5,8,11-tetra-*t*-butylperylene (abbreviation: TBP); or the like. As the host material, the following can be used: an anthracene derivative such as 9,10-di(2-naphthyl)-2-*tert*-butylanthracene (abbreviation: t-BuDNA); a carbazole derivative such as 4,4'-bis(*N*-carbazolyl)biphenyl (abbreviation: CBP); or a metal complex such as tris(8-quinolinolato)aluminum (abbreviation: Alq<sub>3</sub>), tris(4-methyl-8-quinolinolato)aluminum (abbreviation: Alm<sub>q3</sub>); bis(10-hydroxybenzo[*h*]-quinolinato)beryllium (abbreviation: BeBq<sub>2</sub>); bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (abbreviation: BALq); bis[2-(2-hydroxyphenyl)pyridinato]zinc (abbreviation: Znpp<sub>2</sub>); or bis[2-(2-hydroxyphenyl)benzoxazolate]zinc (abbreviation: ZnBOX). As a material which is a light transmitting substance capable of forming the light emitting layer alone, tris(8-quinolinolato)aluminum (abbreviation: Alq<sub>3</sub>), 9,10-bis(2-naphthyl)anthracene (abbreviation: DNA), bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (abbreviation: BALq), or the like can be used. Note that as a layer including an organic compound, a layer such as a hole injecting layer, a hole transporting layer, an electron transporting layer, or an electron injecting layer may be included.

**[0321]** Note that an organic EL light emitting element can obtain light emission when a voltage is applied between a pair of electrodes. In the organic EL light emitting element shown in this embodiment mode, light is emitted by a current generated by the first electrode 102c and the second electrode 602.

**[0322]** As shown in this embodiment mode, the electrode containing silicon is used as an electrode of the organic EL element, so that the organic EL element can be manufactured at low cost.

[Embodiment Mode 23]

**[0323]** FIGS. 34A to 34D are cross-sectional views illustrating a reflection type liquid crystal display device using a single crystalline silicon substrate, and a manufacturing method thereof. Hereinafter, the manufacturing method is briefly described. First, oxygen ions are im-

planted into a single crystalline silicon substrate 700 with constant acceleration (see FIG 34A). Thereafter, by heating at a high temperature, a silicon oxide layer 702 is formed, while a single crystalline silicon layer 701 remains on a surface of the single crystalline silicon substrate 700 (see FIG 34B). Next, the single crystalline silicon layer 701 is etched into an island shape so as to form a transistor 703. In this case, the first electrode 102c is formed at the same time (see FIG 34C). Note that an impurity element is added to source and drain regions 704 of the transistor 703 so as to have conductivity. As the impurity element, elements shown in other embodiment modes can be used. Further, an electrode, a wiring, or the like can be formed using a material shown in other embodiment modes.

**[0324]** Next, an interlayer insulating film 705 is formed (see FIG 34C). Since the interlayer insulating film can be formed using a material shown in other embodiment modes and embodiments, detailed description is omitted here. Note that in this embodiment mode, although the interlayer insulating film has a single-layer structure, it may have a stacked-layer structure of two or more layers. After the interlayer insulating film 705 is formed, a contact hole is formed and a second electrode 706 to be a pixel electrode is formed (see FIG 34D). In this embodiment mode, as a material for the second electrode 706, a material having high visible light reflectivity is preferably used since a reflection type liquid crystal display device is formed; it is not limited thereto. As a material having high reflectivity, a metal material such as aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), neodymium (Nd), chromium (Cr), nickel (Ni), platinum (Pt), gold (Au), silver (Ag), copper (Cu), magnesium (Mg), scandium (Sc), cobalt (Co), zinc (Zn), niobium (Nb), silicon (Si), phosphorus (P), boron (B), arsenic (As), gallium (Ga), indium (In), or tin (Sn) can be taken as an example. Note that a wiring 707 for connection is preferably formed at the same time as the electrode 706.

**[0325]** Thereafter, an alignment film, a liquid crystal, an opposite substrate, and the like are provided so that the reflection type liquid crystal display device is completed. In the liquid crystal display device in this embodiment mode, light from an upper surface (on an opposite substrate side) is reflected by the first electrode 102c or the second electrode 706 so that an image is seen. Therefore, a material having high reflectivity is preferably used for the second electrode 706. Crystal silicon which is a material of the first electrode 102c has, depending on a state of a surface thereof, reflectivity higher than a certain value; therefore, it can be used as a reflective film of the reflection type liquid crystal display device. Note that a structure of a reflection type liquid crystal display device is not limited to that of this embodiment mode, and various structures can be used. For example, in this embodiment mode, a top gate transistor is used as the transistor 703; however, a bottom gate transistor may be used. Further, an electrode formed of a metal material may be employed as the first electrode 102c.

**[0326]** As shown in this embodiment mode, by use of a single crystalline silicon substrate, a liquid crystal display device suitable for usage requiring high-speed operation can be manufactured. That is, a driver circuit can be manufactured directly on a substrate, and high-speed operation of the driver circuit and the like can be achieved. Needless to say, not only the driver circuit but also other circuits can be formed using single crystalline silicon, so that a display device in which all circuits are mounted on one substrate can be formed.

[Embodiment 1]

**[0327]** Embodiment 1 of the present invention is described with reference to FIGS. 26A to 28B. In a liquid crystal display module according to this embodiment, a pixel portion has a structure similar to that of the liquid crystal display device shown in any of Embodiment Modes 1 to 20. Therefore, manufacturing cost can be lowered as compared with a conventional device.

**[0328]** First, as shown in FIG 26A, a base film 802 is formed over a substrate 801. The substrate 801 is a glass substrate, a quartz substrate, a substrate formed of an insulator such as alumina, a plastic substrate with enough heat resistance to withstand a processing temperature of subsequent steps, a silicon substrate, or a metal plate. Further, the substrate 801 may be a substrate in which an insulating film of silicon oxide, silicon nitride, or the like is formed over a surface of a metal substrate such as a stainless steel substrate or a surface of a semiconductor substrate. Note that when a plastic substrate is used for the substrate 801, plastic with a comparatively high glass transition point, such as PC (polycarbonate), PES (polyethersulfone), PET (polyethylene terephthalate), or PEN (polyethylene naphthalate) is preferably used.

**[0329]** The base film 802 has a stacked-layer structure where a silicon oxide ( $\text{SiO}_x$ ) film is formed over a silicon nitride ( $\text{SiN}_x$ ) film, for example; other insulators (such as silicon oxynitride ( $\text{SiO}_x\text{N}_y$ ) ( $x > y > 0$ ) or silicon nitride oxide ( $\text{SiN}_x\text{O}_y$ ) ( $x > y > 0$ )) may also be used. Alternatively, the base film 802 may be formed by high-density plasma treatment on a surface of the substrate 801. High-density plasma is generated by using a microwave at, for example, 2.45 GHz, and has electron density of  $1 \times 10^{11}$  to  $1 \times 10^{13} / \text{cm}^3$ , electron temperature of 2 eV or less, and ion energy of 5 eV or less. Such high-density plasma has low kinetic energy of active species, and a film with less plasma damage and fewer defects compared with conventional plasma treatment can be formed. The distance between the substrate 801 and an antenna for generating the microwave is set to 20 to 80 mm, preferably 20 to 60 mm.

**[0330]** The surface of the substrate 801 can be nitrided by performing the aforementioned high-density plasma treatment in a nitrogen atmosphere, for example, in an atmosphere including nitrogen and a rare gas, an atmosphere including nitrogen, hydrogen, and a rare gas, or

an atmosphere including ammonia and a rare gas. When a glass substrate, a quartz substrate, a silicon wafer, or the like is used as the substrate 801 and nitriding treatment is performed by the aforementioned high-density plasma, a nitride film formed on the surface of the substrate 801 contains silicon nitride as its main component, so that the nitride film can be used as the base film 802. A silicon oxide film or a silicon oxynitride film may be formed over the nitride film by a plasma CVD method so that the base film 802 includes a plurality of layers.

**[0331]** In addition, a nitride film can be formed on a surface of the base film 802 including a silicon oxide film, a silicon oxynitride film, or the like by similarly performing nitriding treatment with high-density plasma on the surface of the base film 802. The nitride film can suppress diffusion of impurities from the substrate 801 and can be formed to be very thin; therefore, influence of stress upon a semiconductor layer to be formed thereover can be reduced.

**[0332]** Next, as shown in FIG 26B, a crystalline semiconductor film (such as a polysilicon film) is formed over the base film 802. As a forming method of the crystalline semiconductor film, a method in which the crystalline semiconductor film is formed directly on the base film 802, and a method in which an amorphous semiconductor film is formed over the base film 802 and subsequently crystallized can be taken as an example.

**[0333]** As a method of crystallizing the amorphous semiconductor film, the following can be used: a crystallization method by laser light irradiation; a crystallization method by heating using an element (for example, a metal element such as nickel) which promotes crystallization of the semiconductor film; or a crystallization method by heating using an element which promotes crystallization of the semiconductor film and subsequently irradiating the semiconductor film with laser light. Needless to say, a method of thermally crystallizing the amorphous semiconductor film without using the aforementioned element can be used as well. However, in this case, the substrate is required to be a quartz substrate, a silicon wafer, or the like which can withstand the high temperature.

**[0334]** When laser irradiation is used, a continuous wave laser beam (CW laser beam) or a pulsed laser beam (pulse laser beam) can be used. Here, a laser beam emitted from one or plural kinds of a gas laser such as an Ar laser, a Kr laser, or an excimer laser; a laser using, as a medium, single crystalline YAG,  $\text{YVO}_4$ , forsterite ( $\text{Mg}_2\text{SiO}_4$ ),  $\text{YAlO}_3$ , or  $\text{GdVO}_4$ , or polycrystalline (ceramic) YAG,  $\text{Y}_2\text{O}_3$ ,  $\text{YVO}_4$ ,  $\text{YAlO}_3$ , or  $\text{GdVO}_4$  doped with one or more of Nd, Yb, Cr, Ti, Ho, Er, Tm, and Ta as a dopant; a glass laser; a ruby laser; an alexandrite laser; a Ti:sapphire laser; a copper vapor laser; and a gold vapor laser can be used. By irradiation with a laser beam having a fundamental wave of such laser beams or one of the second to fourth harmonics of the fundamental wave, a crystal with a large grain size can be obtained. For example, the second harmonic (532 nm)

or the third harmonic (355 nm) of an Nd:YVO<sub>4</sub> laser (fundamental wave of 1064 nm) can be used. In this case, the energy density of approximately 0.01 to 100 MW/cm<sup>2</sup> (preferably, 0.1 to 10 MW/cm<sup>2</sup>) is required for the laser. The scanning rate is set at approximately 10 to 2000 cm/sec to irradiate the semiconductor film.

**[0335]** Note that a laser using, as a medium, single crystalline YAG, YVO<sub>4</sub>, forsterite (Mg<sub>2</sub>SiO<sub>4</sub>), YAlO<sub>3</sub>, or GdVO<sub>4</sub>, or polycrystalline (ceramic) YAG, Y<sub>2</sub>O<sub>3</sub>, YVO<sub>4</sub>, YAlO<sub>3</sub>, or GdVO<sub>4</sub> doped with one or more of Nd, Yb, Cr, Ti, Ho, Er, Tm, and Ta as a dopant; an Ar ion laser; and a Ti:sapphire laser are capable of continuous oscillation. Further, pulse oscillation thereof can be performed at a repetition rate of 10 MHz or more by carrying out Q switch operation or mode locking. When a laser beam is emitted at a repetition rate of 10 MHz or more, a semiconductor film is irradiated with a next pulse after being melted by the laser beam and before being solidified. Therefore, unlike a case of using a pulsed laser with a low repetition rate, a solid-liquid interface can be continuously moved in the semiconductor film; therefore, crystal grains which continuously grow in a scanning direction can be obtained.

**[0336]** When ceramic (polycrystal) is used as a medium, the medium can be formed to have a desired shape for a short time and at low cost. When a single crystalline is used, a columnar medium with several mm in diameter and several tens of mm in length is used. When the ceramic is used, a medium larger than the case of using the single crystalline can be formed.

**[0337]** A concentration of a dopant such as Nd or Yb in a medium, which directly contributes to light emission, cannot be changed largely in either case of the single crystalline or the polycrystal; therefore, there is some limitation on improvement in output of a laser by increasing the concentration of the dopant. However, in the case of ceramic, the size of a medium can be significantly increased as compared with the case of the single crystalline; therefore, drastic improvement in output of a laser can be expected.

**[0338]** Further, in the case of ceramic, a medium with a parallelepiped shape or a rectangular parallelepiped shape can be easily formed. When a medium having such a shape is used and oscillated light is made travel in a zigzag manner inside the medium, a path of the oscillated light can be made long. Therefore, amplification is increased and a laser beam can be oscillated at high output. Furthermore, since a cross section of a laser beam emitted from the medium having such a shape has a quadrangular shape, it has an advantage over a circular beam in being shaped into a linear beam. By shaping a laser beam emitted in the aforementioned manner by using an optical system, a linear beam having a length of 1 mm or less on a lateral side and a length of several mm to several m on a longitudinal side can be easily obtained. In addition, when a medium is uniformly irradiated with excited light, energy distribution of a linear beam becomes uniform in a longitudinal direction.

**[0339]** A semiconductor film is irradiated with this linear beam, so that the whole surface of the semiconductor film can be annealed more uniformly. When uniform annealing is required from one end to the other end of the linear beam, ingenuity such as arrangement in which slits are provided in ends of the linear beam to shield light at a portion where energy is attenuated is required.

**[0340]** When a semiconductor film is annealed using the thus obtained linear beam having uniform intensity and an electronic appliance is manufactured by using this semiconductor film, characteristics of the electronic appliance are good and uniform.

**[0341]** As the method for crystallizing the amorphous semiconductor film by heating with an element which promotes crystallization of the semiconductor film, a technique described in Japanese Published Patent Application No. H8-78329 can be used. In the technique in the patent application publication, an amorphous semiconductor film (also referred to as an amorphous silicon film) is doped with a metal element which promotes crystallization of the semiconductor film, and then heat treatment is performed so that the amorphous semiconductor film is crystallized with the doped region as a nucleus.

**[0342]** Alternatively, an amorphous semiconductor film can be crystallized by performing irradiation with strong light instead of heat treatment. In this case, one of or a combination of infrared light, visible light, and ultraviolet light can be used. Typically, light emitted from a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp is used. A lamp light source is lighted for 1 to 60 seconds, preferably 30 to 60 seconds, and such lighting is repeated 1 to 10 times, preferably 2 to 6 times. The light emission intensity of the lamp light source is arbitrary, but the semiconductor film is required to be instantaneously heated up to approximately 600 to 1000 °C. Note that if necessary, heat treatment may be performed in order to discharge hydrogen contained in the amorphous semiconductor film having an amorphous structure before the irradiation with the strong light. Alternatively, crystallization may be performed by both heat treatment and irradiation with strong light.

**[0343]** After the heat treatment, in order to increase the degree of crystallinity of the crystalline semiconductor film (rate of area occupied by crystalline components against the whole volume of the film) and to correct defects which remain in crystalline grains, the crystalline semiconductor film may be irradiated with the laser light in the atmospheric air or an oxygen atmosphere. The laser light may be selected from the aforementioned laser light.

**[0344]** The doped elements are required to be removed from the crystalline semiconductor film, and the method is described below. First, a surface of the crystalline semiconductor film is treated with a solution containing ozone (typically, ozone water), so that a barrier layer formed of an oxide film (called chemical oxide) is formed on the surface of the crystalline semiconductor

film to have a thickness of 1 to 10 nm. The barrier layer functions as an etching stopper when only a gettering layer is selectively removed in a subsequent step.

**[0345]** Then, a gettering layer containing a rare gas element is formed as a gettering site over the barrier layer. Here, a semiconductor film containing a rare gas element is formed as the gettering layer by a CVD method or a sputtering method. When the gettering layer is formed, the sputtering conditions are controlled as appropriate so that a rare gas element is added to the gettering layer. The rare gas element may be one or more of helium (He), neon (Ne), argon (Ar), krypton (Kr), or xenon (Xe).

**[0346]** Note that when the gettering layer is formed by using a source gas containing phosphorus which is an impurity element or by using a target containing phosphorus, gettering can be performed by utilizing the coulomb force of phosphorus in addition to the gettering using the rare gas element. In gettering, a metal element (such as nickel) tends to move to a region having a high concentration of oxygen; therefore, the concentration of oxygen contained in the gettering layer is preferably set at, for example,  $5 \times 10^{18}/\text{cm}^3$  or higher.

**[0347]** Next, the crystalline semiconductor film, the barrier layer, and the gettering layer are subjected to thermal treatment (such as heat treatment or irradiation with strong light), and thereby the metal element (such as nickel) is gettered, so that the metal element in the crystalline semiconductor film is lowered in concentration or removed.

**[0348]** Next, a known etching method is performed using the barrier layer as an etching stopper so that only the gettering layer is selectively removed. After that, the barrier layer formed of an oxide film is removed, for example, using an etchant containing hydrofluoric acid.

**[0349]** Here, impurity ions may be added in consideration of threshold characteristics of a TFT to be manufactured.

**[0350]** Next, a photo resist film (not shown) is applied over the crystalline semiconductor film, and is exposed to light and developed. Therefore, a resist pattern is formed over the crystalline semiconductor film. Next, the crystalline semiconductor film is etched using the resist pattern as a mask. Therefore, a crystalline semiconductor film 803 to be included in a thin film transistor and a crystalline semiconductor film 803a to be a common electrode are formed over the base film 802.

**[0351]** Next, after surfaces of the crystalline semiconductor films 803 and 803a are cleaned with an etchant containing hydrofluoric acid, a gate insulating film 804 is formed to have a thickness of 10 to 200 nm over the crystalline semiconductor film 803. The gate insulating film 804 is formed of an insulating film containing silicon as a main component, such as a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or a silicon nitride oxide film. Further, the gate insulating film may have a single layer or a stacked-layer film. Note that the gate insulating film 804 is also formed over the crystalline

semiconductor film 803a and the base film 802.

**[0352]** Next, as shown in FIG. 26C, after the gate insulating film 804 is cleaned, a first conductive film and a second conductive film are formed in this order over the gate insulating film 804. For example, the first conductive film is a tungsten film and the second conductive film is a tantalum nitride film.

**[0353]** Next, a photo resist film (not shown) is applied over the second conductive film, and is exposed to light and developed. Therefore, a resist pattern is formed over the second conductive film. Next, by using the resist pattern as a mask, the first conductive film and the second conductive film are etched under a first condition, and further, the second conductive film is etched under a second condition. Thus, first gate electrodes 805a and 805b and second gate electrodes 806a and 806b are formed over the crystalline semiconductor film 803. The first gate electrodes 805a and 805b are separated from each other. The second gate electrode 806a is provided over the first gate electrode 805a, and the second gate electrode 806b is provided over the first gate electrode 806b. Inclined angles of side surfaces of each of the first gate electrodes 805a and 805b are more moderate than inclined angles of side surfaces of each of the second gate electrodes 806a and 806b.

**[0354]** By the etching treatment, a first wiring 807 and a second wiring 808 provided over the first wiring 807 are formed near the crystalline semiconductor film 803a. Here, each of the aforementioned gate electrodes and wirings is preferably led so as to have a round corner when seen from a direction perpendicular to the substrate 801. By making the corners round, dust or the like can be prevented from remaining at the corners of the wiring; therefore, the number of defects generated due to dust can be reduced and yield can be improved. Thereafter, the photo resist film is removed.

**[0355]** Next, as shown in FIG. 26D, a first conductivity type (for example, n-type) impurity element (for example, phosphorus) is injected into the crystalline semiconductor film 803 by using the first gate electrodes 805a and 805b and the second gate electrodes 806a and 806b as masks. Therefore, first impurity regions 810a, 810b, and 810c are formed in the crystalline semiconductor film 803. The first impurity region 810a is provided in a region to be a source of the thin film transistor. The first impurity region 810c is provided in a region to be a drain of the thin film transistor. The impurity region 810b is provided between the first gate electrodes 805a and 805b.

**[0356]** Note that in this treatment, the first conductivity type impurity element is also injected into the crystalline semiconductor film 803a to be a common electrode to lower resistance.

**[0357]** Next, as shown in FIG. 26E, a photo resist film is applied over the whole surface including over the first gate electrodes 805a and 805b and the second gate electrodes 806a and 806b, and is exposed to light and developed. Therefore, each of top surfaces of the first gate electrode 805a and the second gate electrode 806a and

their surroundings are covered with a resist pattern 812a, and each of top surfaces of the first gate electrode 805b and the second gate electrode 806b and their surroundings are covered with a resist pattern 812b. Next, by using the resist patterns 812a and 812b as masks, a first conductivity type impurity element 811 (for example, phosphorus) is injected into the crystalline semiconductor film 803. Therefore, the first conductivity type impurity element 811 is further injected into a part of each of the first impurity regions 810a, 810b, and 810c, so that second impurity regions 813a, 813b, and 813c are formed.

**[0358]** Further, the first conductivity type impurity element is further injected into the crystalline semiconductor film 803a to be the common electrode to lower resistance. Note that the other parts of the first impurity regions 810a, 810b, and 810c remain as third impurity regions 814a, 814b, 814c, and 814d.

**[0359]** Thereafter, as shown in FIG 27A, the resist patterns 812a and 812b are removed. Next, an insulating film (not shown) covering almost all surface is formed. The insulating film is, for example, a silicon oxide film formed by a plasma CVD method.

**[0360]** Next, heat treatment is performed on the crystalline semiconductor films 803 and 803a to activate the impurity elements doped therewith. The heat treatment is performed by a rapid thermal annealing method (RTA method) using a lamp light source, irradiation of a YAG laser or an excimer laser from the back surface, or heat treatment using a furnace, or by a combination of a plurality of these methods.

**[0361]** By the aforementioned treatment, the impurity elements are activated, and simultaneously the element (for example, a metal element such as nickel), which is used as a catalyst for crystallizing the crystalline semiconductor film 803, is gettered in the second impurity regions 813a to 813c including a high concentration impurity (such as phosphorus), and a nickel concentration mainly in a region to be a channel forming region of the crystalline semiconductor film 803 is reduced. As a result, crystallinity of the channel forming region is improved. Accordingly, an off-current value of a TFT is reduced and high electron field-effect mobility can be obtained. Therefore, a TFT having favorable characteristics can be obtained.

**[0362]** Next, an insulating film 815 is formed over the whole surface including above the crystalline semiconductor films 803 and 803a. The insulating film 815 is, for example, a silicon nitride film formed by a plasma CVD method. Next, a planarizing film to be an interlayer insulating film 816 is formed over the insulating film 815. As the interlayer insulating film 816, a light-transmitting inorganic material (silicon oxide, silicon nitride, silicon nitride containing oxygen, or the like); a photosensitive or non-photosensitive organic material (polyimide, acrylic, polyamide, polyimide amide, a resist, or benzocyclobutene); a stacked-layer structure thereof; or the like is used. Alternatively, as another light-transmitting film used for the planarizing film, an insulating film formed of

a  $\text{SiO}_x$  film containing an alkyl group obtained by a coating method, for example, an insulating film using silica glass, alkyl siloxane polymers, alkylsilsesquioxane polymers, hydrogen silsesquioxane polymers, hydrogen alkylsilsesquioxane polymers, or the like can be used. As an example of siloxane-based polymers, there are coating insulating film materials such as PSB-K1 and PSB-K31 (product of Toray industries, Inc.) and ZRS-5PH (product of Catalysts & Chemicals Industries Co., Ltd.). The interlayer insulating film may be a single-layer film or a multi-layer film.

**[0363]** Next, a photo resist film (not shown) is applied over the interlayer insulating film 816, and is exposed to light and developed. Therefore, a resist pattern is formed over the interlayer insulating film 816. Next, the interlayer insulating film 816, the insulating film 815, and the gate insulating film 804 are etched using the resist pattern as a mask. Therefore, contact holes 817a, 817b, 817c, and 817d are formed in the interlayer insulating film 816, the insulating film 815, and the gate insulating film 804. The contact hole 817a is provided over the second impurity region 813a, which is the source of the transistor. The contact hole 817b is provided over the second impurity region 813c, which is the drain of the transistor. The contact hole 817c is provided over the second wiring 808. The contact hole 817d is provided over the crystalline semiconductor film 803a, which is the common electrode. Thereafter, the resist pattern is removed.

**[0364]** Next, as shown in FIG 27B, a first conductive film 818 is formed in each of the contact holes 817a to 817d and over the interlayer insulating film 816. The first conductive film 818 is a light-transmitting conductive film, such as an ITO film, a film of indium tin oxide containing a Si element, or a film of IZO (indium zinc oxide) formed by using a target in which zinc oxide (ZnO) of 2 to 20 wt% is mixed with indium oxide. Next, a second conductive film 819 is formed over the first conductive film 818. The second conductive film 819 is, for example, a metal film.

**[0365]** Next, a photo resist film 820 is applied over the conductive film 819. Next, a reticle 840 is provided above the photo resist film 820. The reticle 840 has a structure where semi-transmitting film patterns 842a, 842b, 842c, and 842d are formed over a glass substrate and light shielding patterns 841a, 841b, and 841c are formed over a part of the semi-transmitting film patterns 842a to 842d. The semi-transmitting film pattern 842a and the light shielding pattern 841a are provided above the contact hole 817a. The semi-transmitting film pattern 842b and the light shielding pattern 841b are provided above the contact hole 817b. The semi-transmitting film pattern 842c and the light shielding pattern 841c are provided above the contact holes 817c and 817d. The semi-transmitting film pattern 842d is provided above the crystalline semiconductor film 803a.

**[0366]** Next, the photo resist film 820 is exposed to light using the reticle 840 as a mask. Therefore, the photo resist film 820 is exposed to light except for a portion below the light shielding patterns 841a to 841c and a

lower layer of a portion below the semi-transmitting film patterns 842a to 842d. Note that portions which are not exposed to light are denoted by reference numerals 821a, 821b, 821c, and 821d.

**[0367]** Next, as shown in FIG 27C, the photo resist film 820 is developed. Therefore, portions exposed to light in the photo resist film 820 are removed, and resist patterns 822a, 822b, 822c, and 822d are formed. The resist pattern 822a is provided above the contact hole 817a. The resist pattern 822b is provided above and around the contact hole 817b. The resist pattern 822c is provided above and between the contact holes 817c and 817d. The resist pattern 822d is provided above the crystalline semiconductor film 803a to be the common electrode. Note that portions of the resist pattern 822b, except for a portion above the contact hole 817b, and the resist pattern 822d are thinner than other resist patterns.

**[0368]** Next, as shown in FIG 27D, the first conductive film 818 and the second conductive film 819 are etched using the resist patterns 822a to 822d as masks. Thus, the first conductive film 818 and the second conductive film 819 in regions which are not covered with the resist patterns 822a to 822d are removed.

**[0369]** Further, since the resist patterns 822a to 822d are also gradually etched, in the etching treatment, a thin portion (specifically, the portions of the resist pattern 822b, except for a portion above the contact hole 817b, and the resist pattern 817d) of the resist pattern is removed. Therefore, in each of regions below the portion of the resist pattern 822b except for a portion above the contact hole 817b, and the resist pattern 817d, the second conductive film 819 is removed and only the first conductive film 818 remains. Thereafter, the resist patterns 822a to 822c are removed.

**[0370]** As described above, with one resist pattern and one etching treatment, source wirings 823a and 824a, drain wiring 823b and 824b, connection wirings 823c and 824c, and a pixel electrode 823d are formed. The source wirings 823a and 824a and the drain wiring 823b and 824b form a thin film transistor 825 along with the crystalline semiconductor film 803, impurity regions formed in the crystalline semiconductor film 803, the gate insulating film 804, the first gate electrodes 805a and 805b, and the second gate electrodes 806a and 806b. The connection wirings 823c and 824c connect the second wiring 808 and the crystalline semiconductor film 803a.

**[0371]** Thereafter, a first alignment film 826 is formed. Thus, an active matrix substrate is formed. Note that with the treatments shown in FIGS. 26A to 27D, thin film transistors 827 and 829 (shown in FIG 28B) are formed in a gate signal line driver circuit region 854 of a liquid crystal display device shown in FIGS. 28A and 28B. Further, with the treatments shown in FIGS. 27B to 27D, a first terminal electrode 838a and a second terminal electrode 838b (shown in FIG 28B) which connect the active matrix substrate and the outside are formed.

**[0372]** Thereafter, as shown in a plan view of FIG 28A and a cross-sectional view along a line K-L of FIG. 28B,

an organic resin film such as an acrylic resin film is formed over the active matrix substrate, and patterning is performed on the organic resin film. Thus, a columnar spacer 833 is formed over the active matrix substrate. Next, after a sealing material 834 is formed in a sealing region 853, a liquid crystal is dropped on the active matrix substrate. Before the liquid crystal is dropped, a protective film may be formed over the sealing material to prevent the sealing material and the liquid crystal from reacting with each other.

**[0373]** Thereafter, an opposite substrate 830 provided with a color filter 832 and a second alignment film 831 is provided opposed to the active matrix substrate, and these two substrates are attached by the sealing material 834. In this case, the active matrix substrate and the opposite substrate 830 are attached by the spacer 833 to have a uniformed space. Next, the space between the substrates is completely sealed. Thus, the liquid crystal is sealed between the active matrix substrate and the opposite substrate.

**[0374]** Next, if required, one or both the active matrix substrate and the opposite substrate are cut into a desired shape. Further, polarizing plates 835a and 835b are provided. Next, a flexible printed circuit (hereinafter referred to as an FPC) 837 is connected to the second terminal electrode 838b provided in an external terminal connection region 852, through an anisotropy conductive film 836.

**[0375]** A structure of the liquid crystal display module formed in this manner is described. A pixel region 856 is provided at the center of the active matrix substrate. A plurality of pixels are formed in the pixel region 856. In FIG 28A, the gate signal line driver circuit regions 854 for driving a gate signal line are provided above and below the pixel region 856. A source signal line driver circuit region 857 for driving a source signal line is provided in a region between the pixel region 856 and the FPC 837. The gate signal line driver circuit region 854 may be provided either above and below the pixel region 856, which may be selected by a designer as appropriate in accordance with substrate size in the liquid crystal display module, or the like. Note that when operation reliability, efficiency of driving, and the like of the circuits are considered, the gate signal line driver circuit regions 854 are preferably provided symmetrically with the pixel region 856 therebetween. Signals to each driver circuit are inputted from the FPC 837.

#### [Embodiment 2]

**[0376]** A liquid crystal display module according to Embodiment 2 of the present invention is described with reference to FIGS. 29A to 30B. In each drawing, a structure of a pixel portion 930 is similar to that of the pixel region 856 shown in Embodiment 1, and a plurality of pixels are formed over the substrate 100.

**[0377]** FIG. 29A is a schematic plan view of a liquid crystal display module. FIG 29B is a diagram illustrating

a circuit structure of a source driver 910. As an example of FIGS. 29A and 29B, both a gate driver 920 and the source driver 910 are formed over the substrate 100 same as the pixel portion 930 as shown in FIG 29A. The source driver 910 includes a plurality of thin film transistors 912 for selecting the source signal line to which an inputted video signal is transmitted; and a shift register 911 for controlling the plurality of thin film transistors 912.

**[0378]** FIG. 30A is a schematic plan view of a liquid crystal display module. FIG 30B is a diagram illustrating a circuit structure of a source driver. As an example of FIGS. 30A and 30B, the source driver includes a thin film transistor group 940 formed over the substrate 100; and an IC 950 formed separately from the substrate 100. The IC 950 and the thin film transistor group 940 are electrically connected by an FPC 960, for example.

**[0379]** The IC 950 is formed using a single crystalline silicon substrate, for example. The IC 950 controls the thin film transistor group 940 and inputs a video signal to the thin film transistor group 940. The thin film transistor group 940 selects the source signal line to which an inputted video signal is transmitted, based on a control signal from the IC.

**[0380]** According to Embodiment 2, manufacturing cost of a liquid crystal display module can be reduced.

[Embodiment 3]

**[0381]** An electric appliance according to Embodiment 3 of the present invention is described with reference to FIGS. 31A to 31H. An electric appliance includes a light emitting device of the present invention and is provided with a module such as examples shown in the aforementioned embodiments.

**[0382]** The electronic appliances include cameras such as a video camera and a digital camera, a goggle-type display (head mounted display), a navigation system, an audio reproducing device (such as a car audio component stereo), a computer, a game machine, a portable information terminal (such as a mobile computer, a mobile phone, a mobile game machine, and an electronic book), an image reproducing device provided with a recording medium (specifically, a device for reproducing a recording medium such as a digital versatile disc (DVD) and having a display for displaying the reproduced image) and the like. FIGS. 31A to 31H show specific examples of these electric appliances.

**[0383]** FIG 31A shows a monitor of a television receiving device or a personal computer, which includes a housing 2001, a supporting base 2002, a display portion 2003, a speaker portion 2004, a video input terminal 2005, and the like. As the display portion 2003, the liquid crystal display device shown in any of Embodiment Modes 1 to 20 is used. Since the monitor of the television receiving device or the personal computer includes the liquid crystal display device, manufacturing cost thereof can be reduced.

**[0384]** FIG 31B shows a digital camera. An image re-

ceiving portion 2103 is provided in the front side of a main body 2101. A shutter 2106 is provided at the upper portion of the main body 2101. A display portion 2102, operation keys 2104, and an external connection port 2105 are provided at the backside of the main body 2101. As the display portion 2103, the liquid crystal display device shown in any of Embodiment Modes 1 to 20 is used. Since the digital camera includes the liquid crystal display device, manufacturing cost thereof can be reduced.

**[0385]** FIG 31C shows a notebook computer. A main body 2201 is provided with a keyboard 2204, an external connection port 2205, and a pointing device 2206. A housing 2202 including a display portion 2203 is attached to the main body 2201. As the display portion 2203, the liquid crystal display device shown in any of Embodiment Modes 1 to 20 is used. Since the notebook computer includes the liquid crystal display device, manufacturing cost thereof can be reduced.

**[0386]** FIG 31D shows a mobile computer, which includes a main body 2301, a display portion 2302, a switch 2303, operation keys 2304, an infrared port 2305, and the like. An active matrix display device is provided for the display portion 2302. As the display portion 2303, the liquid crystal display device shown in any of Embodiment Modes 1 to 20 is used. Since the mobile computer includes the liquid crystal display device, manufacturing cost thereof can be reduced.

**[0387]** FIG 31E shows an image reproducing device. A main body 2401 is provided with a display portion B 2404, a recording medium reading portion 2405, and an operation key 2406. A housing 2402 including a speaker portion 2407 and a display portion A 2403 is attached to the main body 2401. As each of the display portion A 2403 and the display portion B 2404, the liquid crystal display device shown in any of Embodiment Modes 1 to 20 is used. Since the image reproducing device includes the liquid crystal display device, manufacturing cost thereof can be reduced.

**[0388]** FIG. 31F shows an electronic book. A main body 2501 is provided with an operation key 2503. A plurality of display portions 2502 are attached to the main body 2501. As the display portions 2502, the liquid crystal display device shown in any of Embodiment Modes 1 to 20 is used. Since the electronic book includes the liquid crystal display device, manufacturing cost thereof can be reduced.

**[0389]** FIG 31G shows a video camera. A main body 2601 is provided with an external connection port 2604, a remote control receiving portion 2605, an image receiving portion 2606, a battery 2607, an audio input portion 2608, operation keys 2609, and an eyepiece portion 2610. A housing 2603 including a display portion 2602 is attached to the main body 2601. As the display portions 2602, the liquid crystal display device shown in any of Embodiment Modes 1 to 20 is used. Since the video camera includes the liquid crystal display device, manufacturing cost thereof can be reduced.

**[0390]** FIG. 31H shows a mobile phone, which includes

a main body 2701, a housing 2702, a display portion 2703, an audio input portion 2704, an audio output portion 2705, an operation key 2706, an external connection port 2707, an antenna 2708, and the like. As the display portions 2703, the liquid crystal display device shown in any of Embodiment Modes 1 to 20 is used. Since the mobile phone includes the liquid crystal display device, manufacturing cost thereof can be reduced.

**[0391]** As described above, the application range of the present invention is so wide that the present invention can be applied to electronic appliances of various fields.

**[0392]** This application is based on Japanese Patent Application serial No. 2006-105618 filed in Japan Patent Office on April 6th, 2006, the entire contents of which are hereby incorporated by reference.

## Claims

1. A liquid crystal display device comprising:

a first substrate (100);

a semiconductor film (102f) comprising a channel formation region (102a) over the first substrate (100);

a pixel electrode (108) over the first substrate (100);

a conductive film (107b) on and in contact with the pixel electrode (108), the conductive film (107b) being electrically connected to the pixel electrode (108) and to the semiconductor film (102f);

a common electrode (102c) over the first substrate;

an insulating film (106a) interposed between the pixel electrode (108) and the common electrode (102c);

a liquid crystal layer (110) provided over the pixel electrode (108) and the common electrode (102c); and

a second substrate (111) over the liquid crystal layer (110).

2. The liquid crystal display device according to claim 1, wherein the conductive film (107b) comprises molybdenum.

3. The liquid crystal display device according to claim 1 or claim 2, wherein the insulating film (106a) comprises silicon nitride.

4. The liquid crystal display device according to any of claims 1 to 3, wherein the electrode amongst the two electrodes which is the closest to the liquid crystal layer (111) comprises indium tin oxide.

5. The liquid crystal display device according to any of claims 1 to 4, wherein the liquid crystal display device

is configured to control orientation of a liquid crystal of the liquid crystal layer (110) via an electric field generated by a voltage applied between the pixel electrode (108) and the common electrode (102c).

6. The liquid crystal display device according to any of claims 1 to 5, wherein the channel formation region (102a) does not overlap the pixel electrode (108).

7. The liquid crystal display device according to any of claims 1 to 6, further comprising a second insulating film (105) interposed between the pixel electrode (108) and the common electrode (102c).

8. An electronic device comprising the liquid crystal display device according to any of claim 1 to 6.

9. A mobile computer comprising the liquid crystal display device (2302) according to any of claim 1 to 7.



FIG. 1A

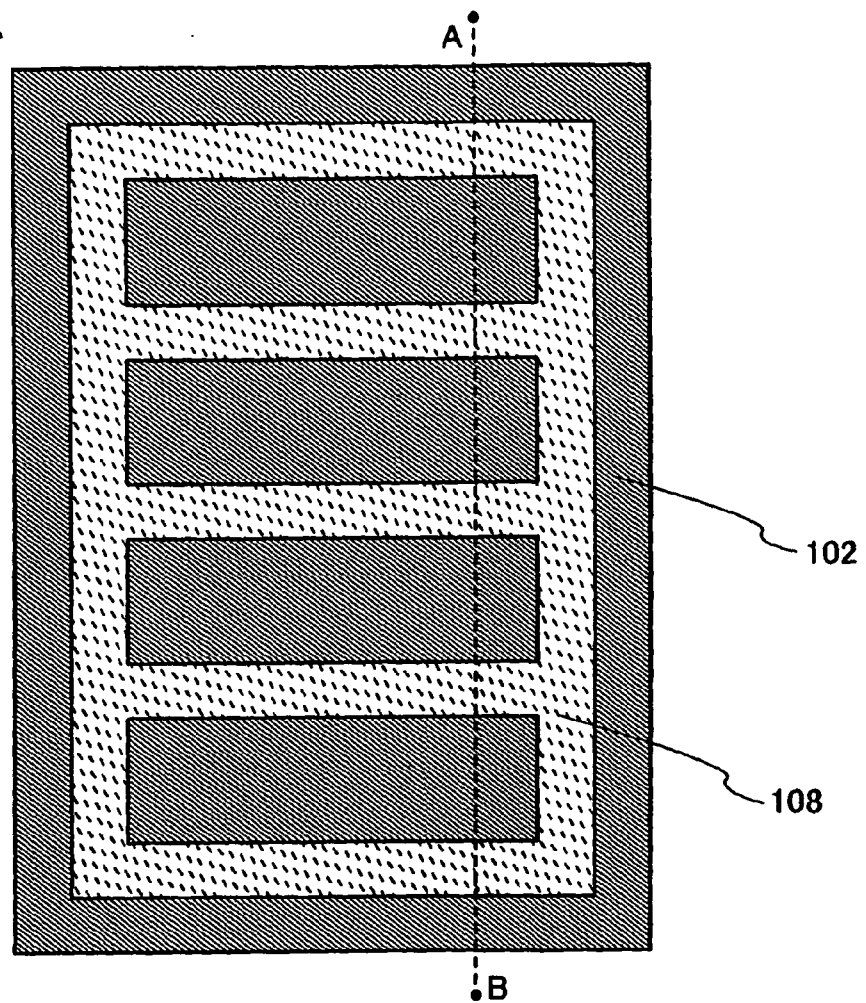


FIG. 1B

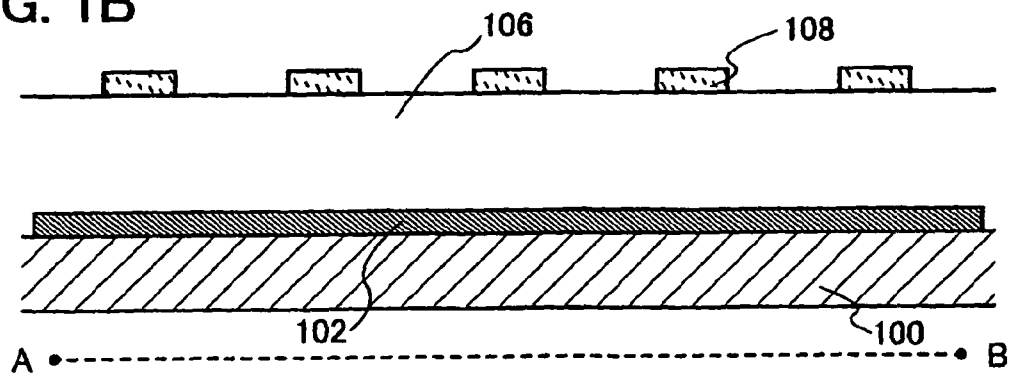


FIG. 2A

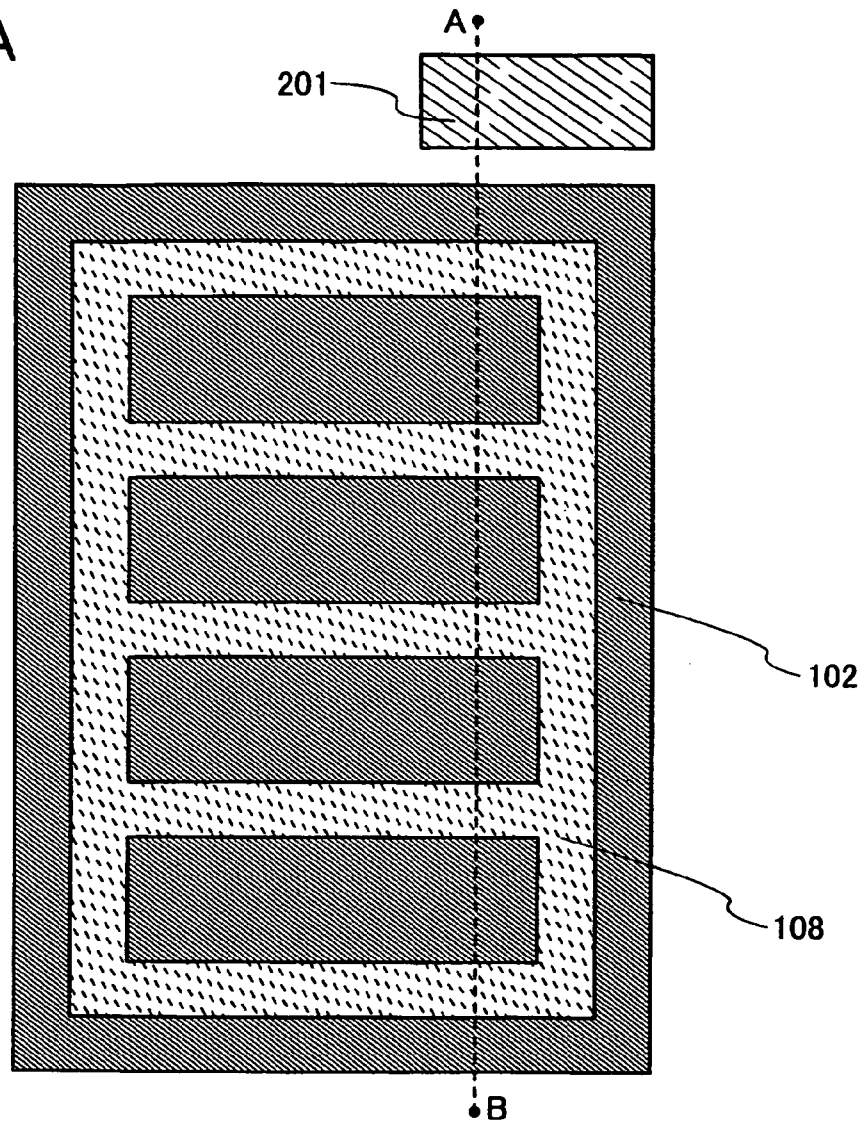


FIG. 2B

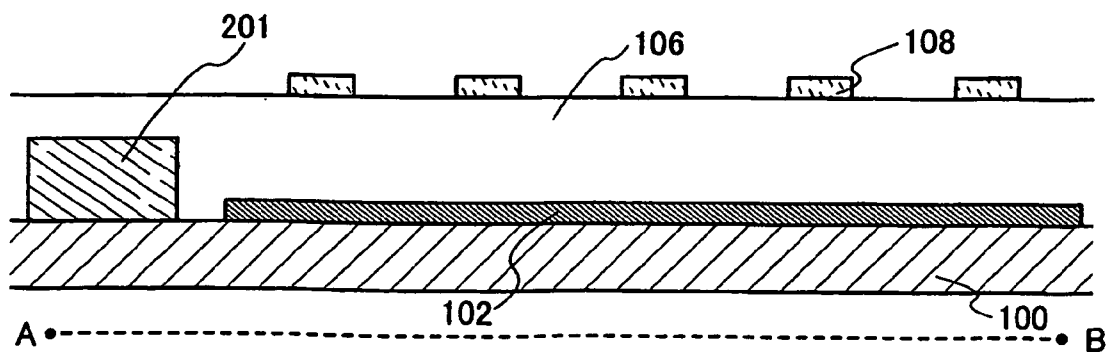


FIG. 3A

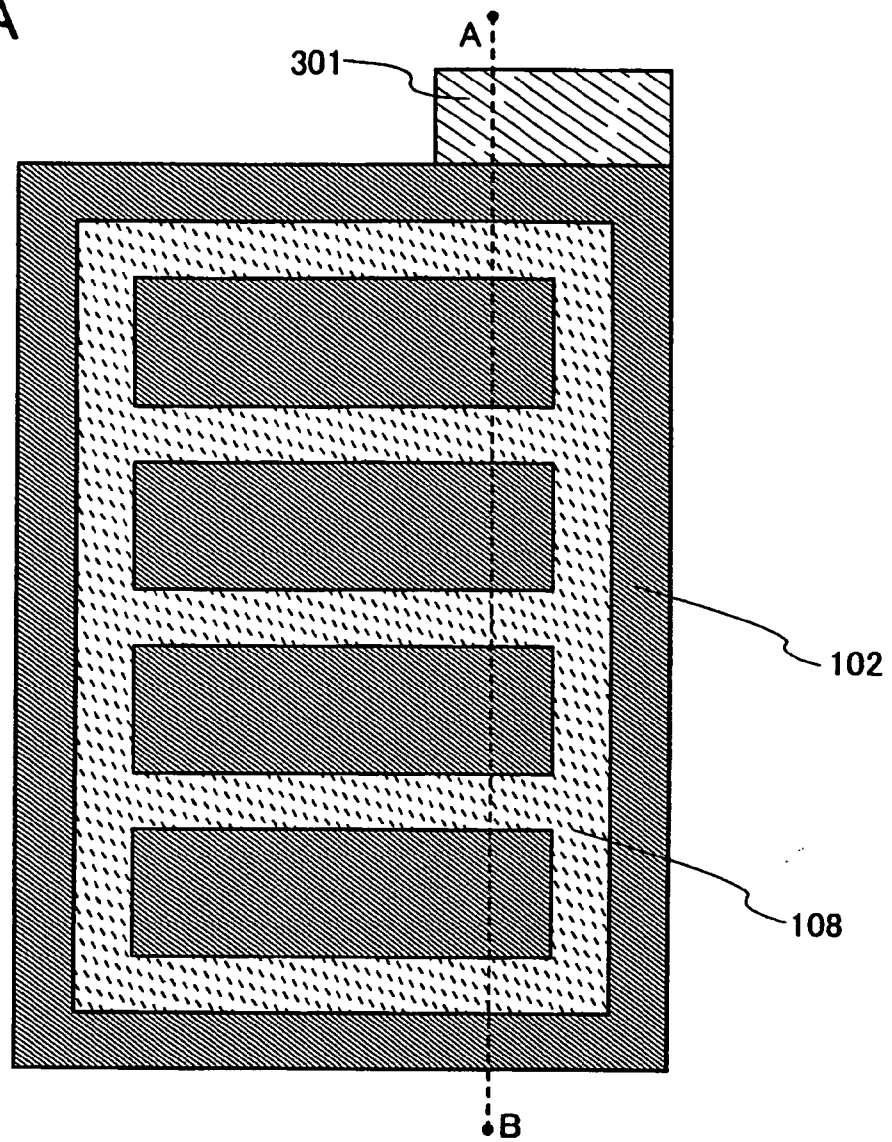


FIG. 3B

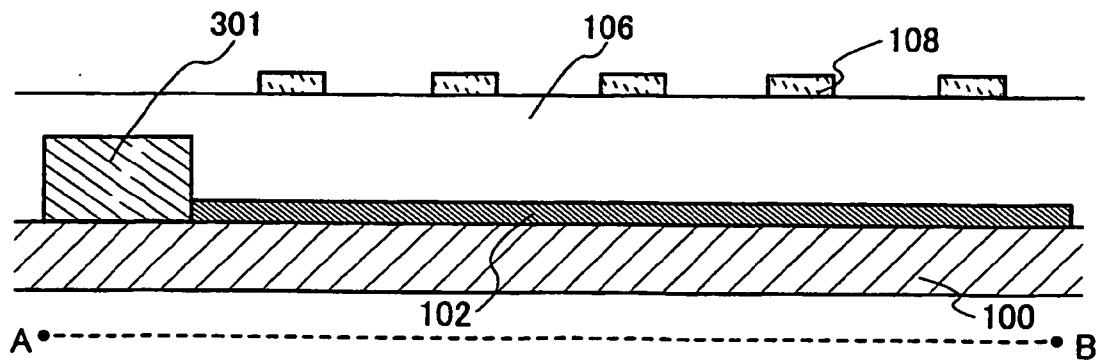


FIG. 4A

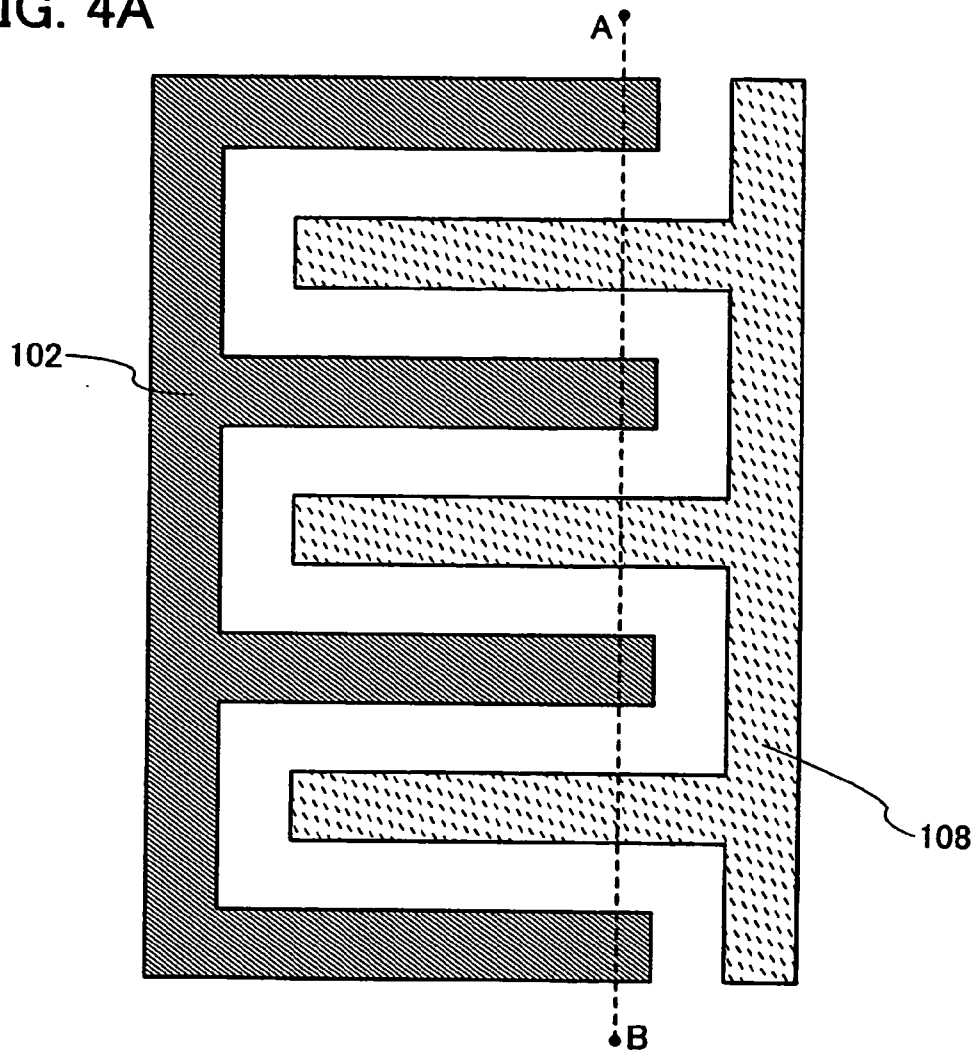


FIG. 4B

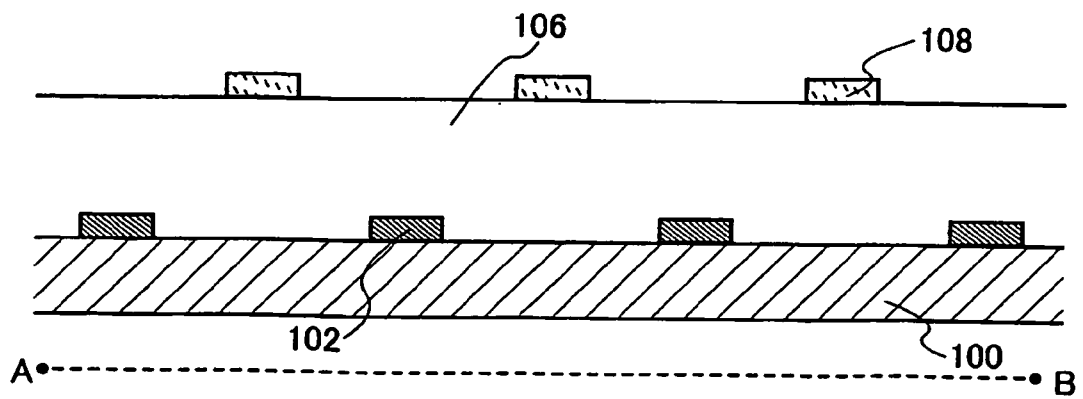


FIG. 5A

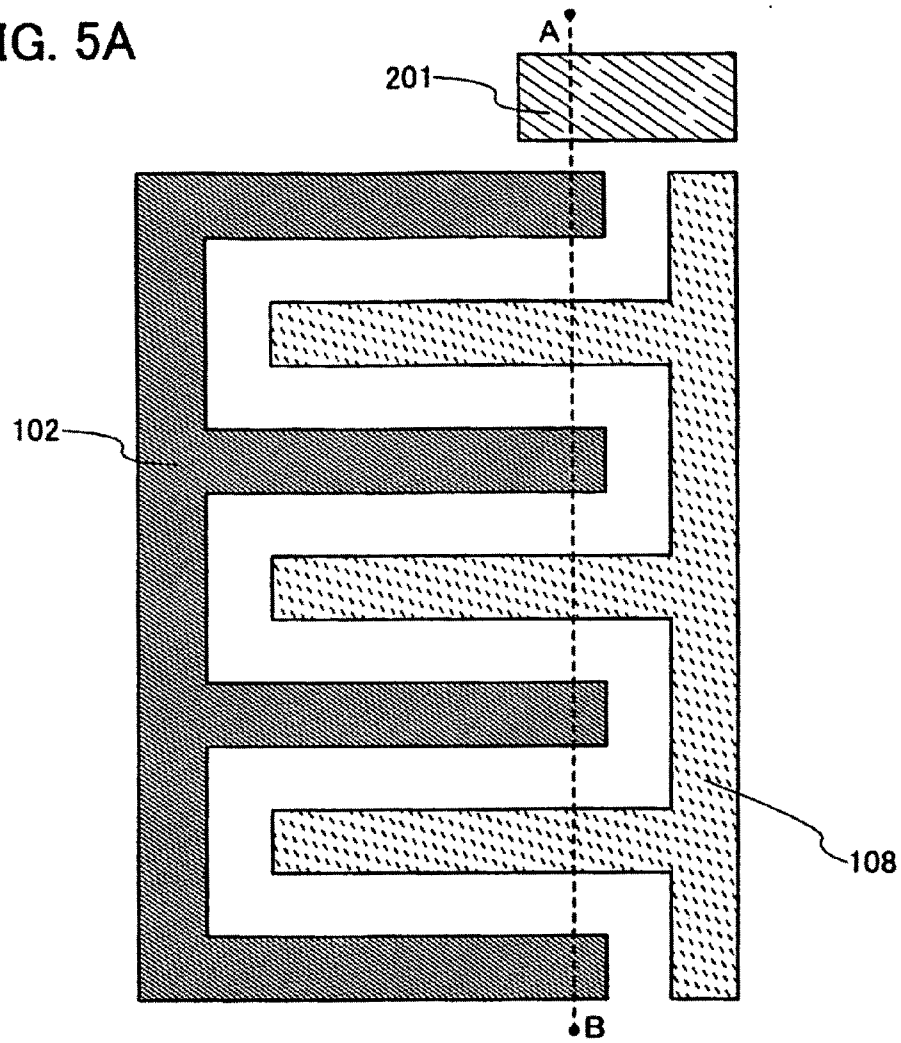


FIG. 5B

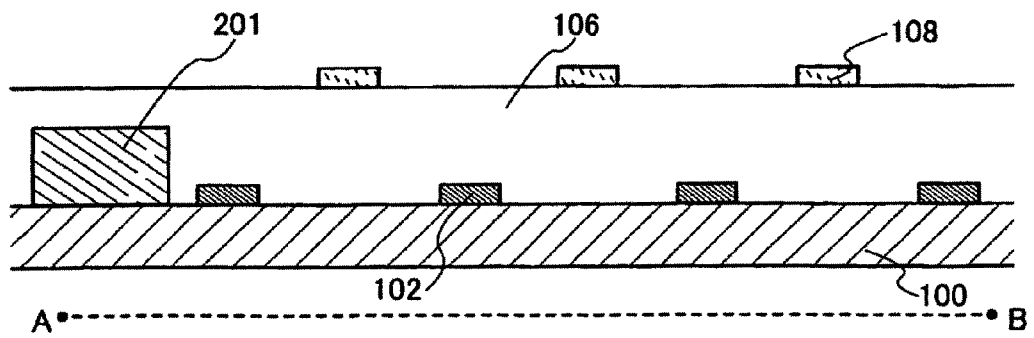


FIG. 6A

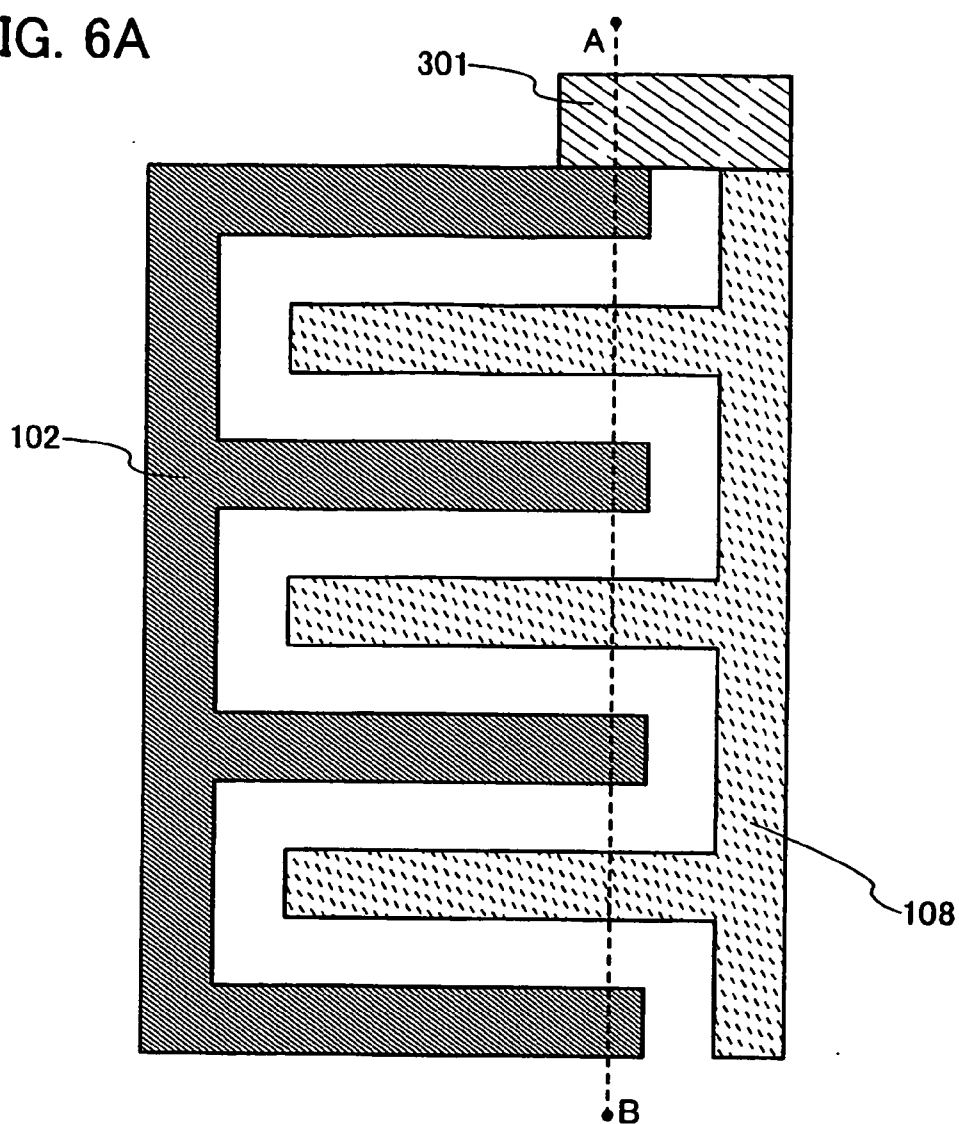


FIG. 6B

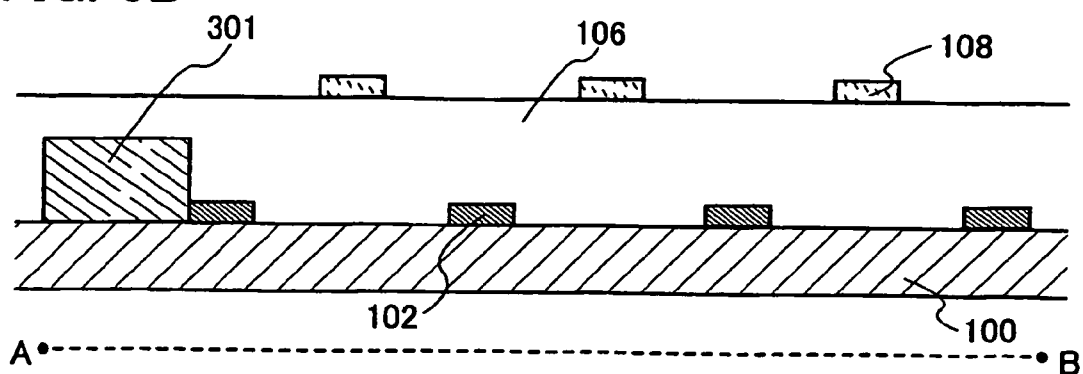


FIG. 7A

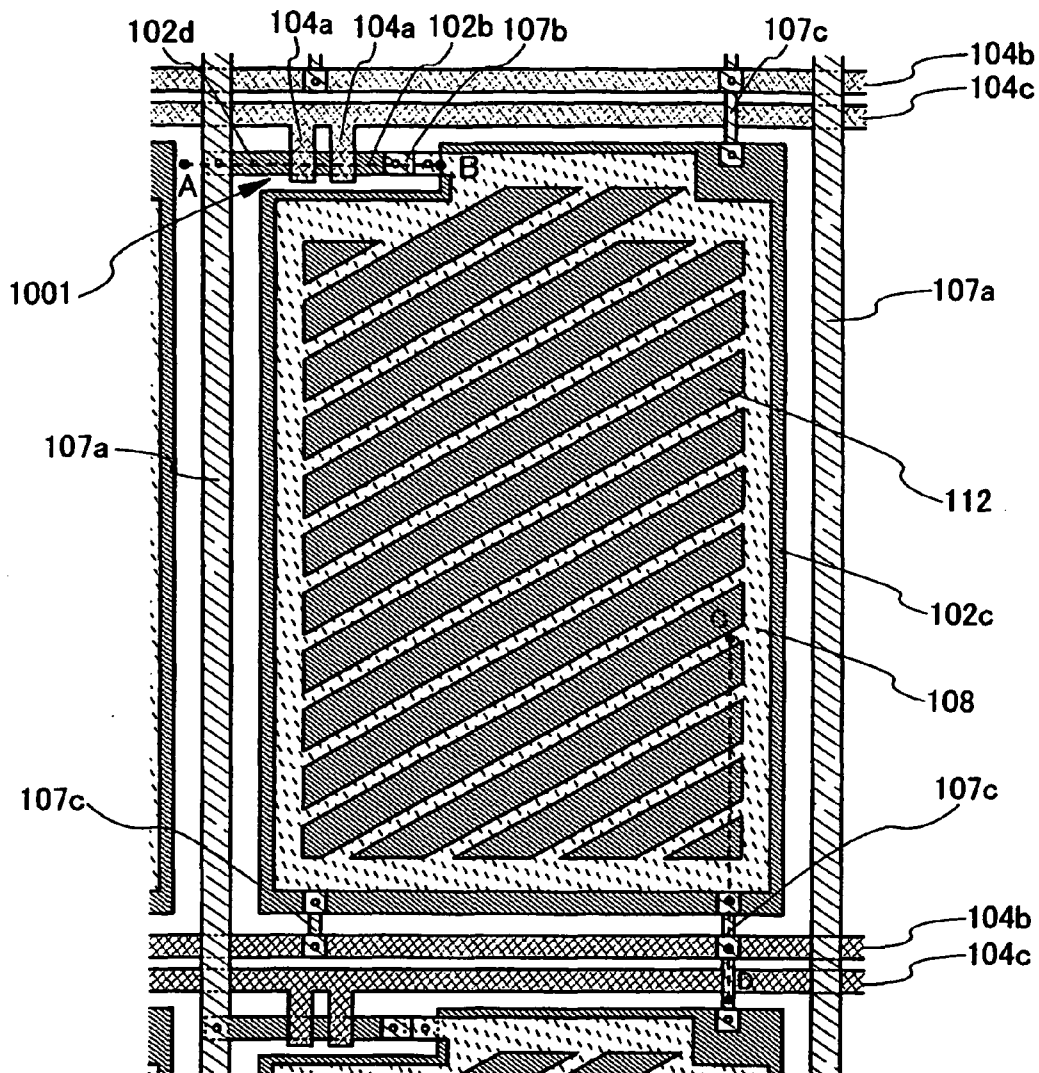


FIG. 7B

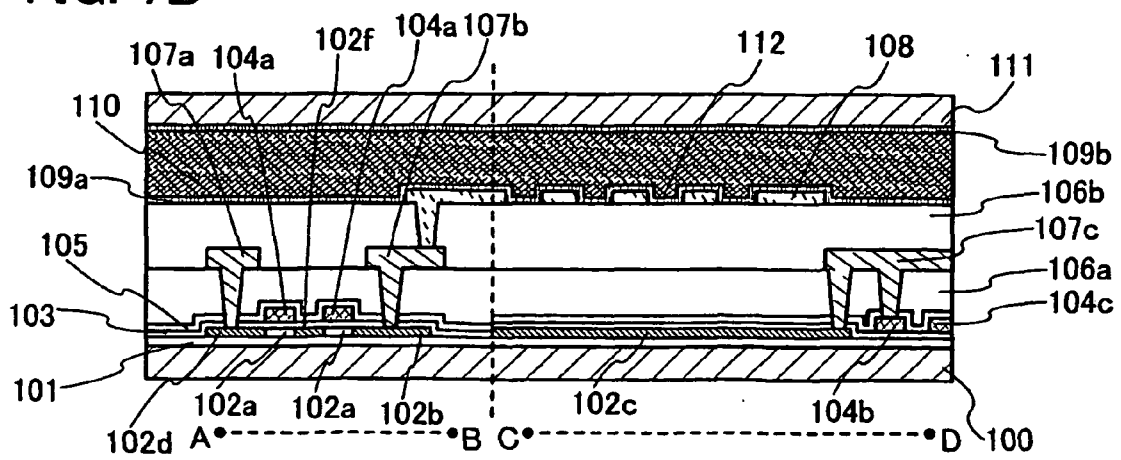


FIG. 8

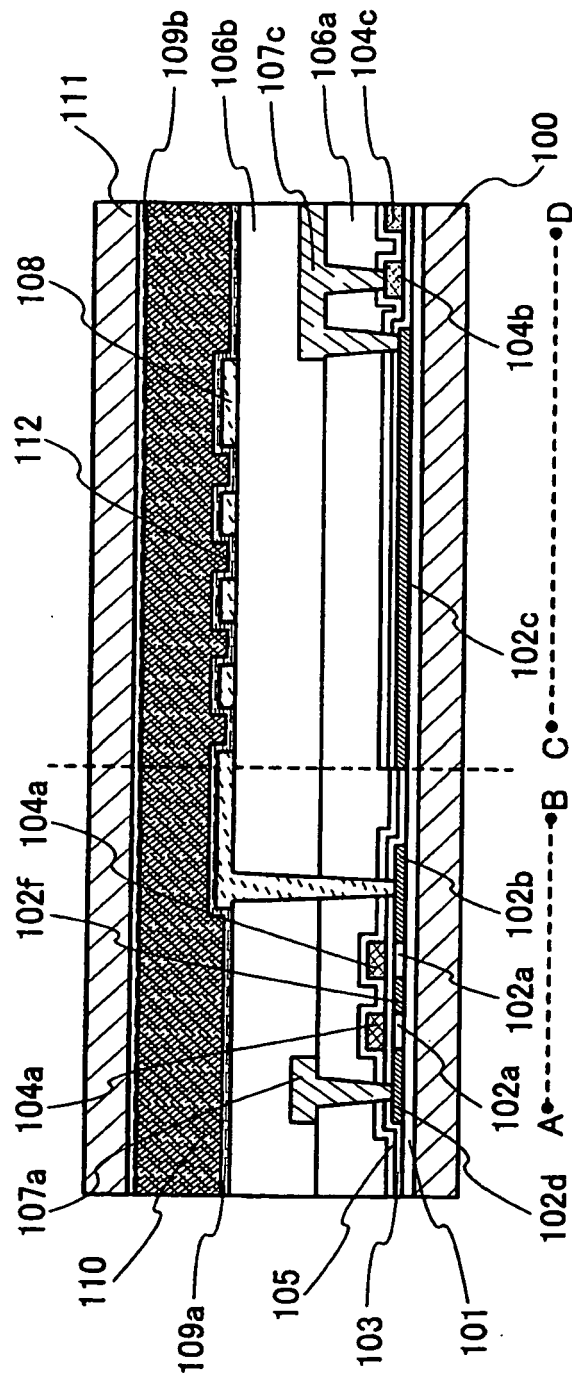




FIG. 9A

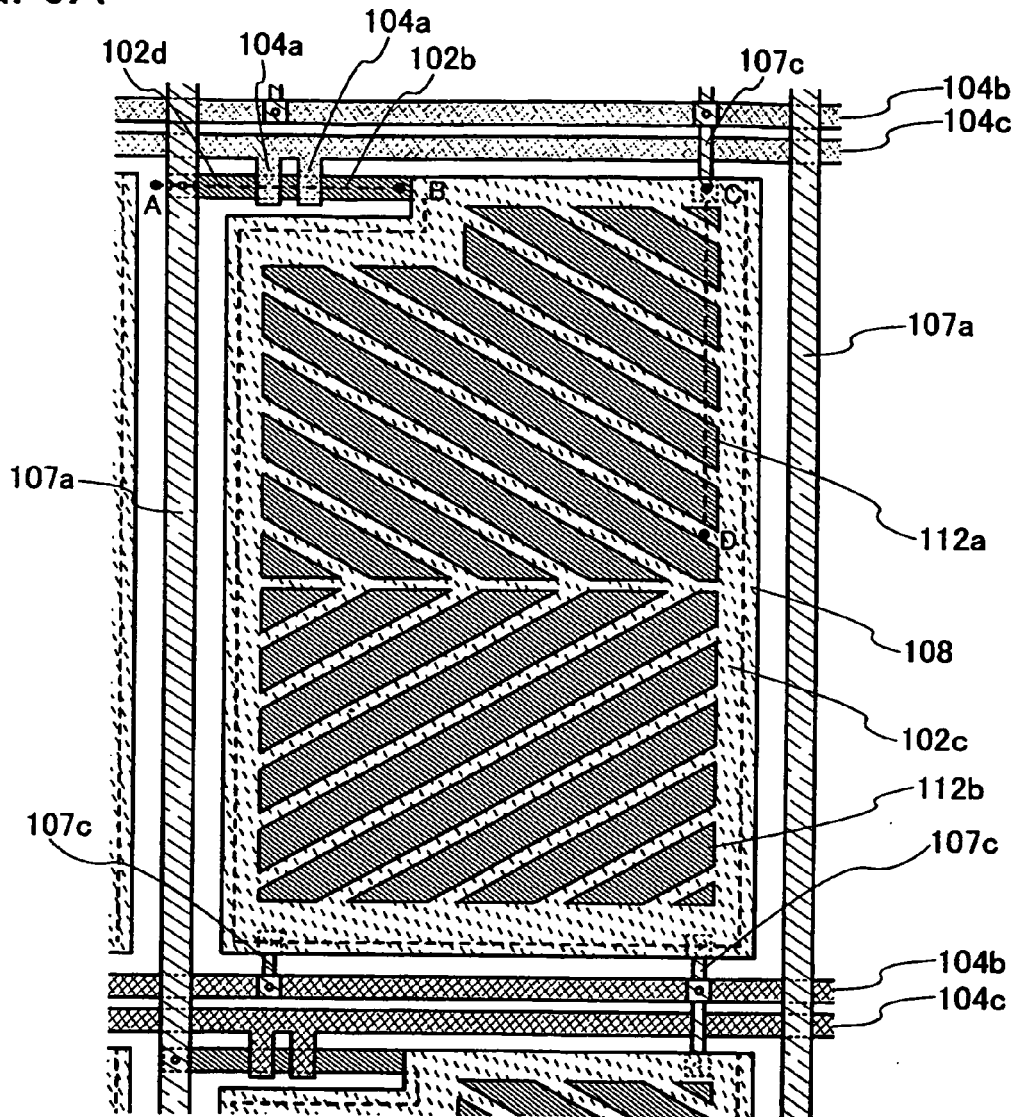


FIG. 9B

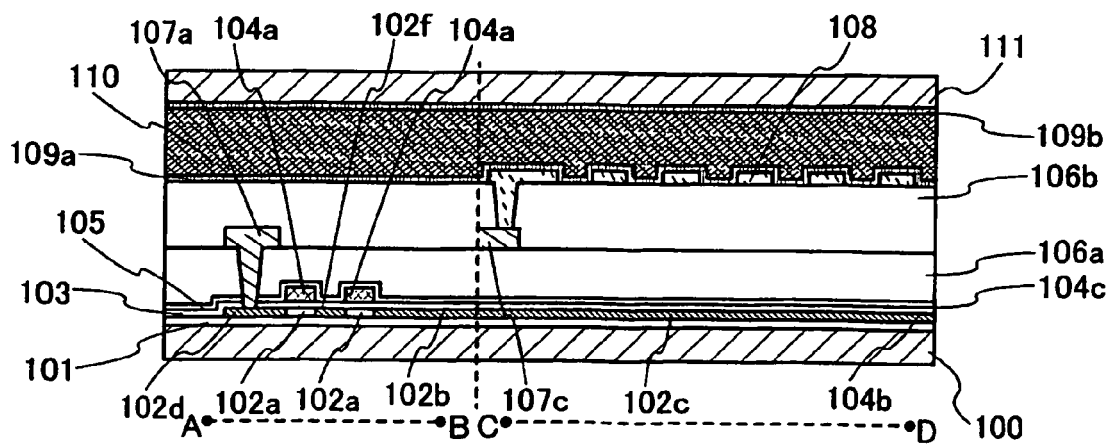


FIG. 10A

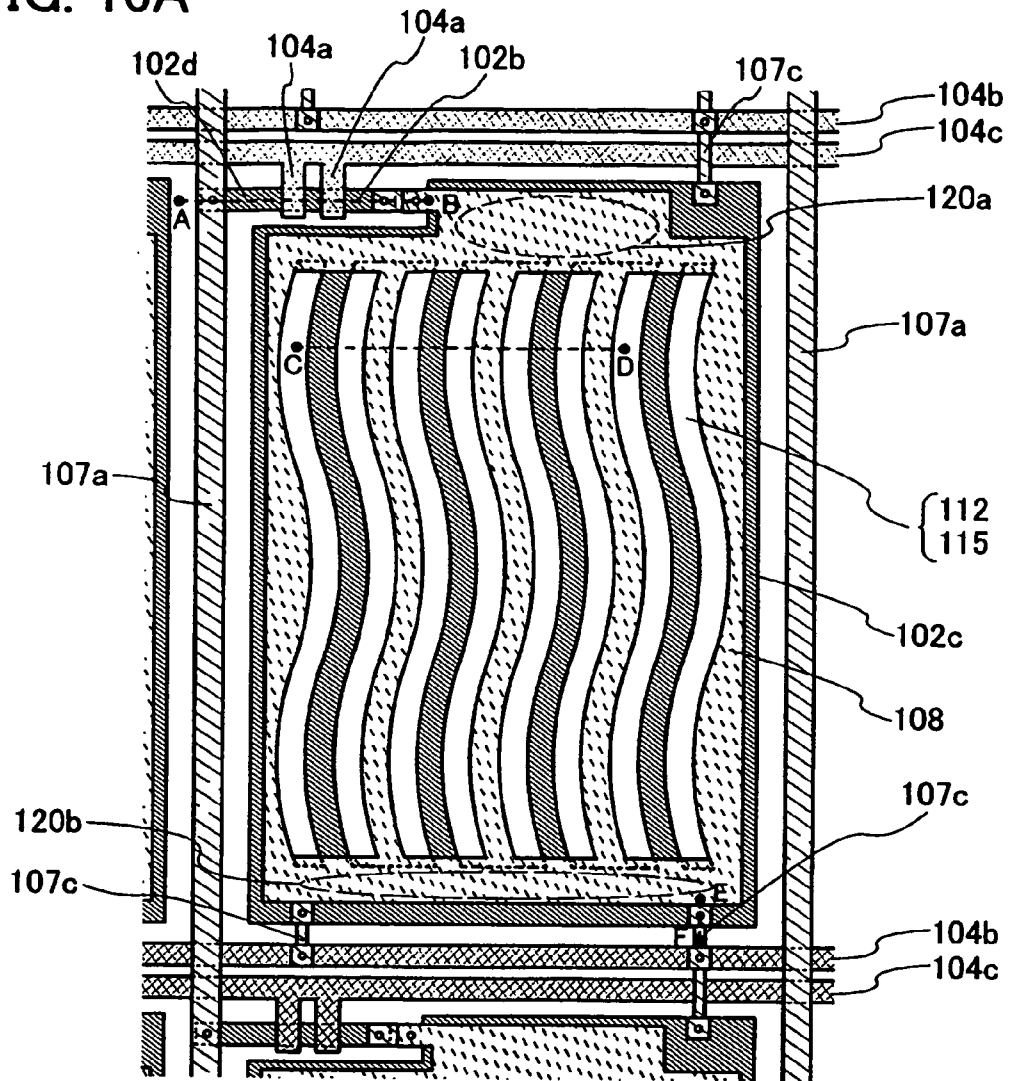


FIG. 10B

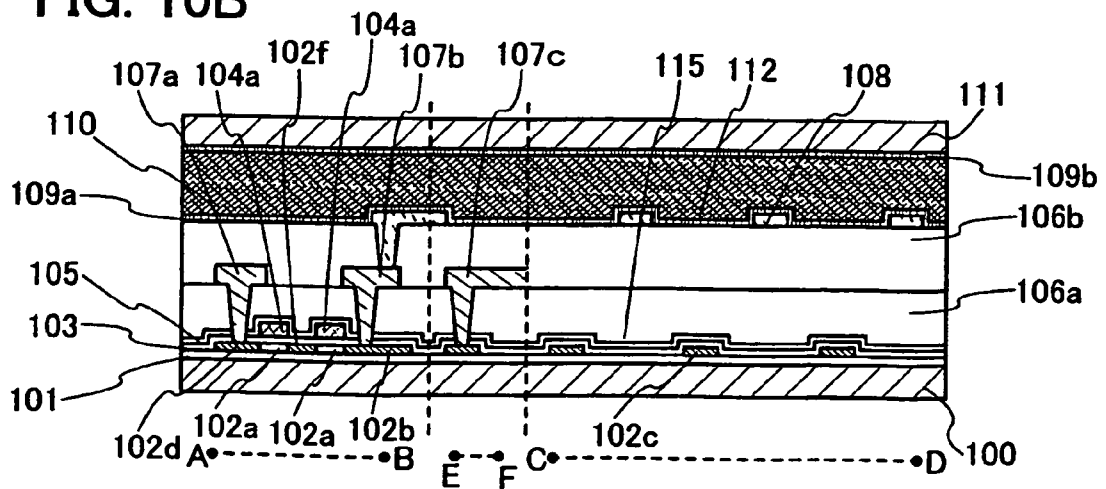


FIG. 11A

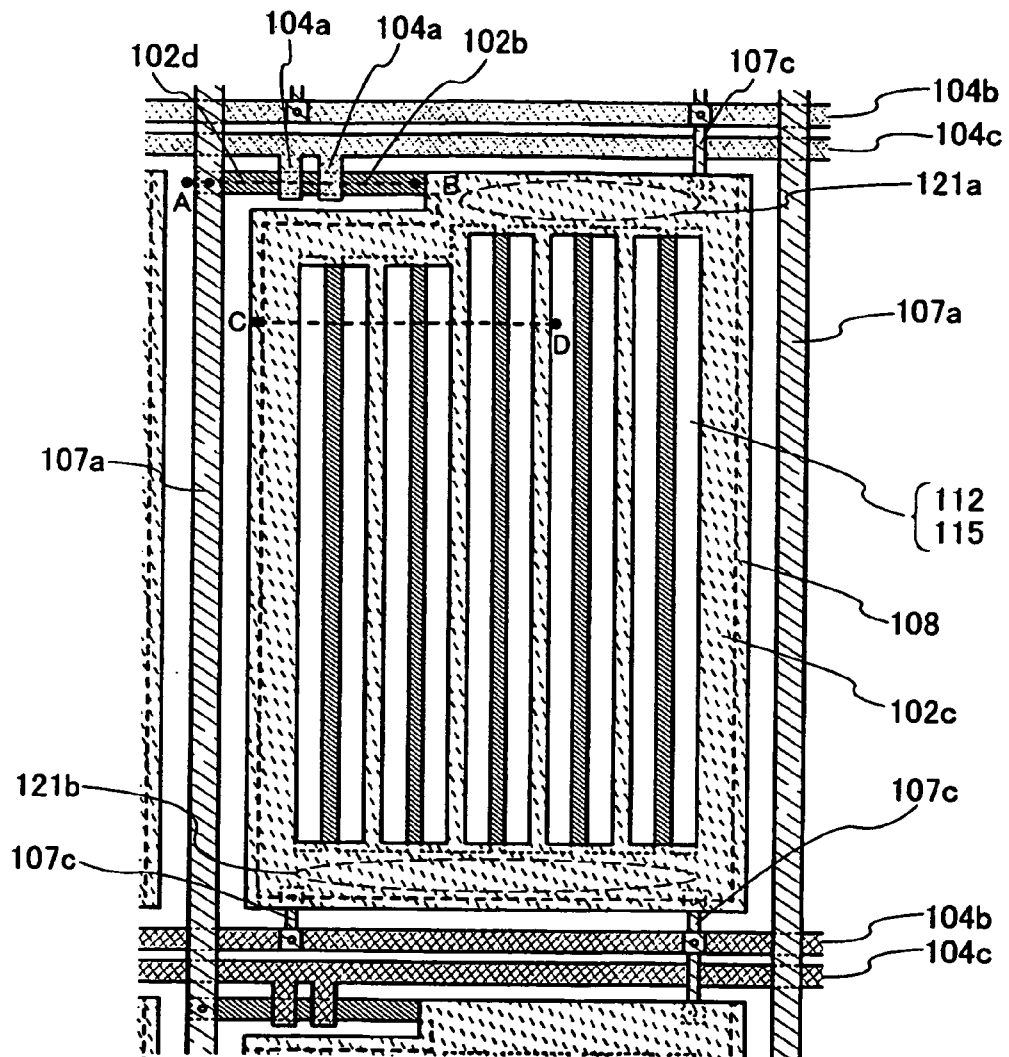


FIG. 11B

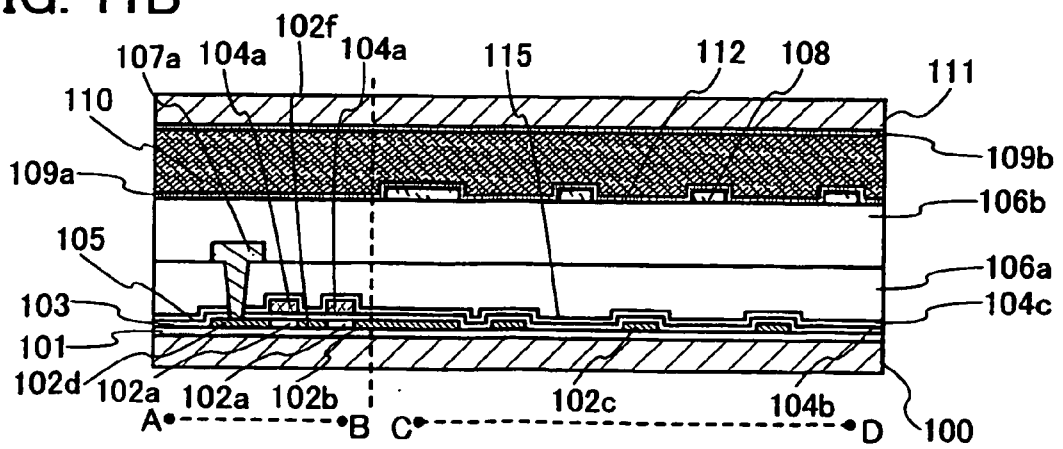


FIG. 12A

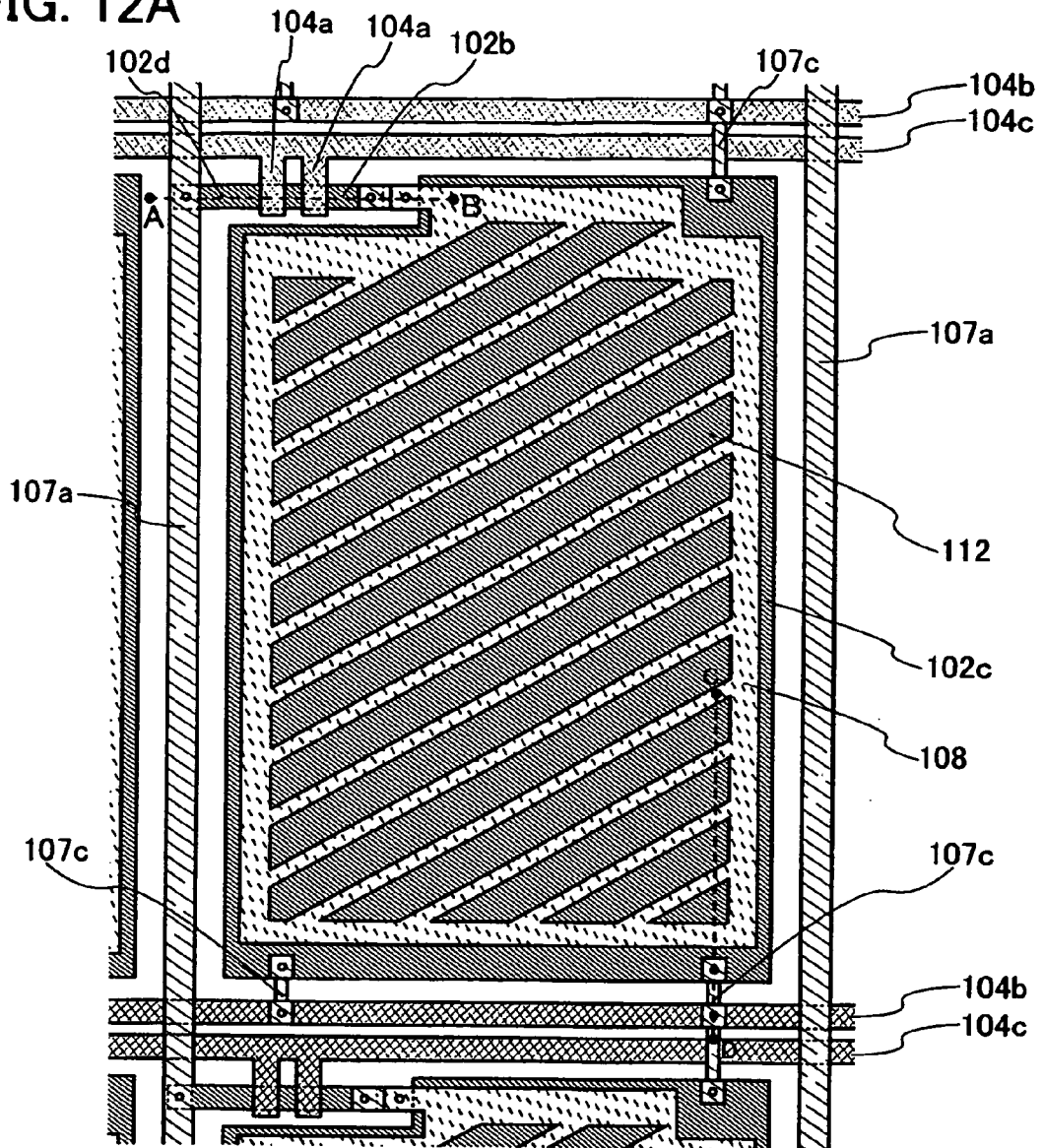


FIG. 12B

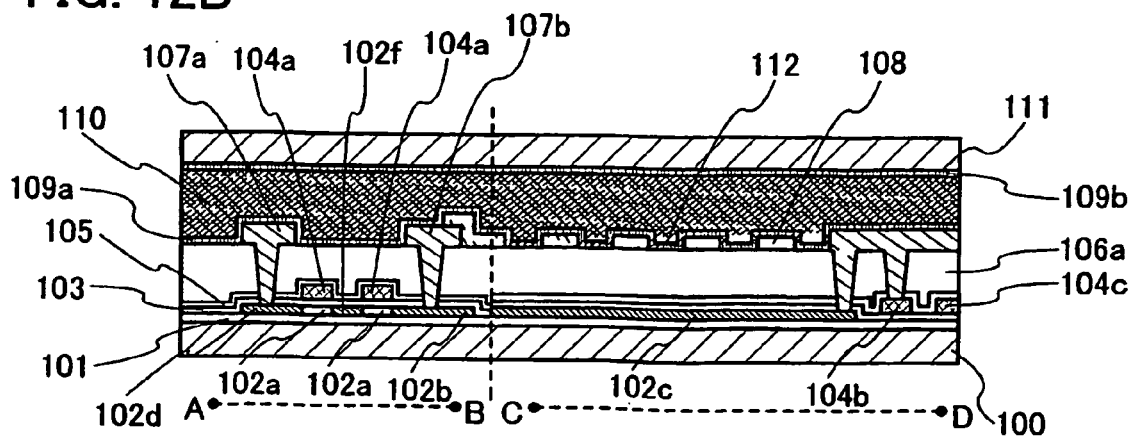


FIG. 13A

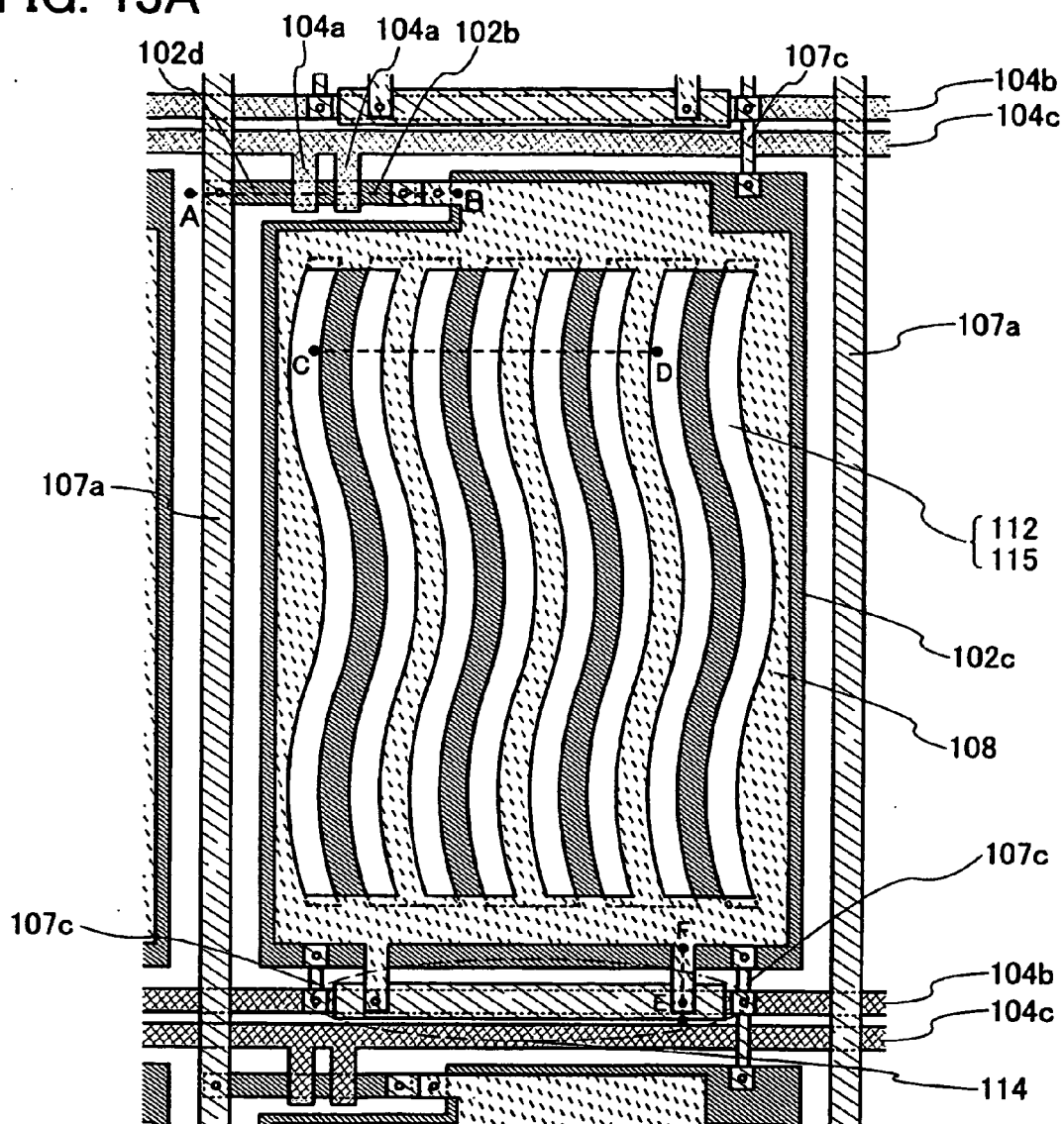


FIG. 13B

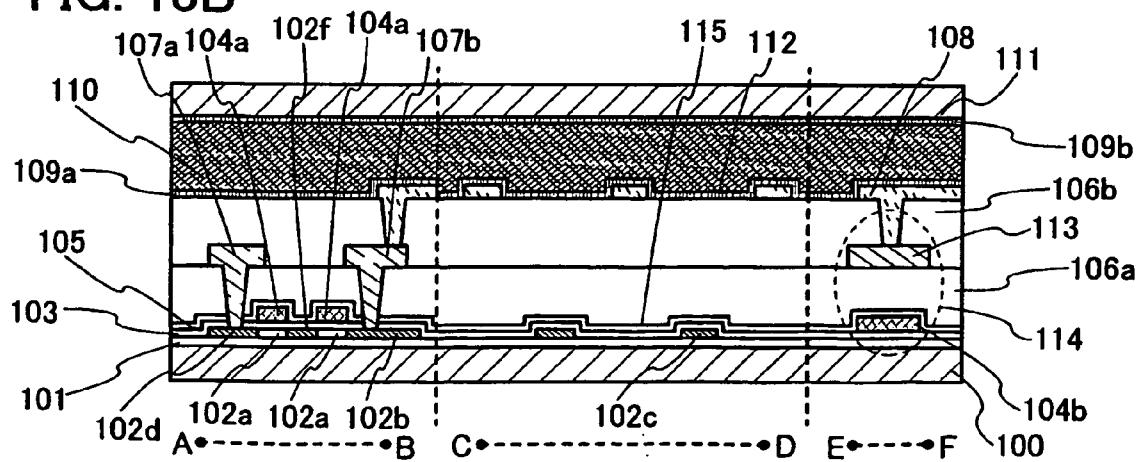


FIG. 14A

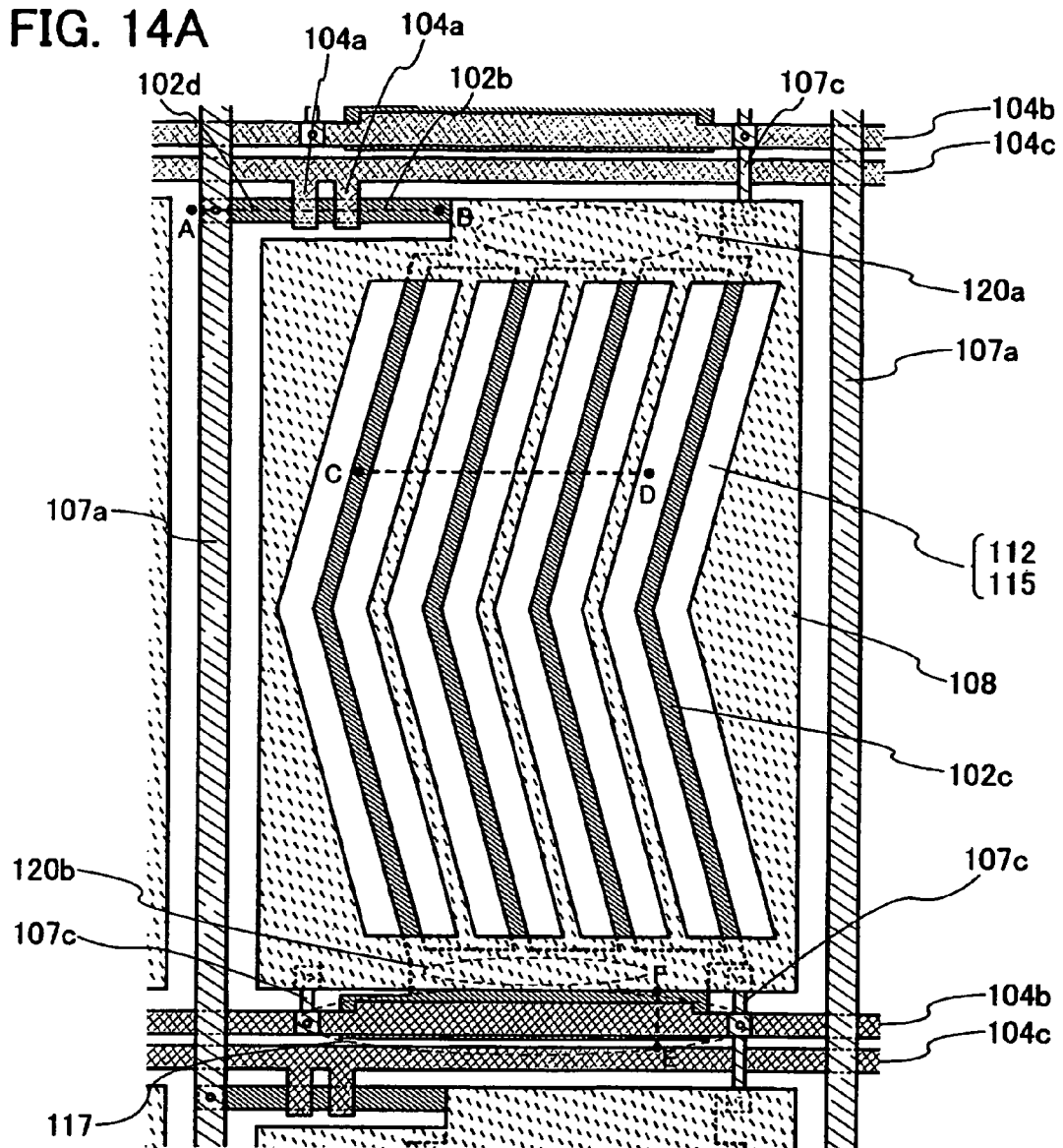


FIG. 14B

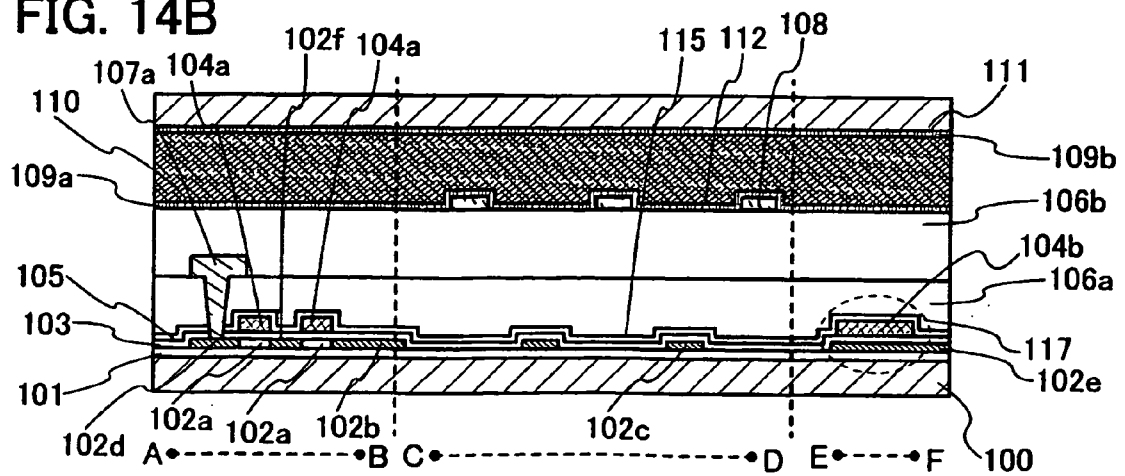


FIG. 15A

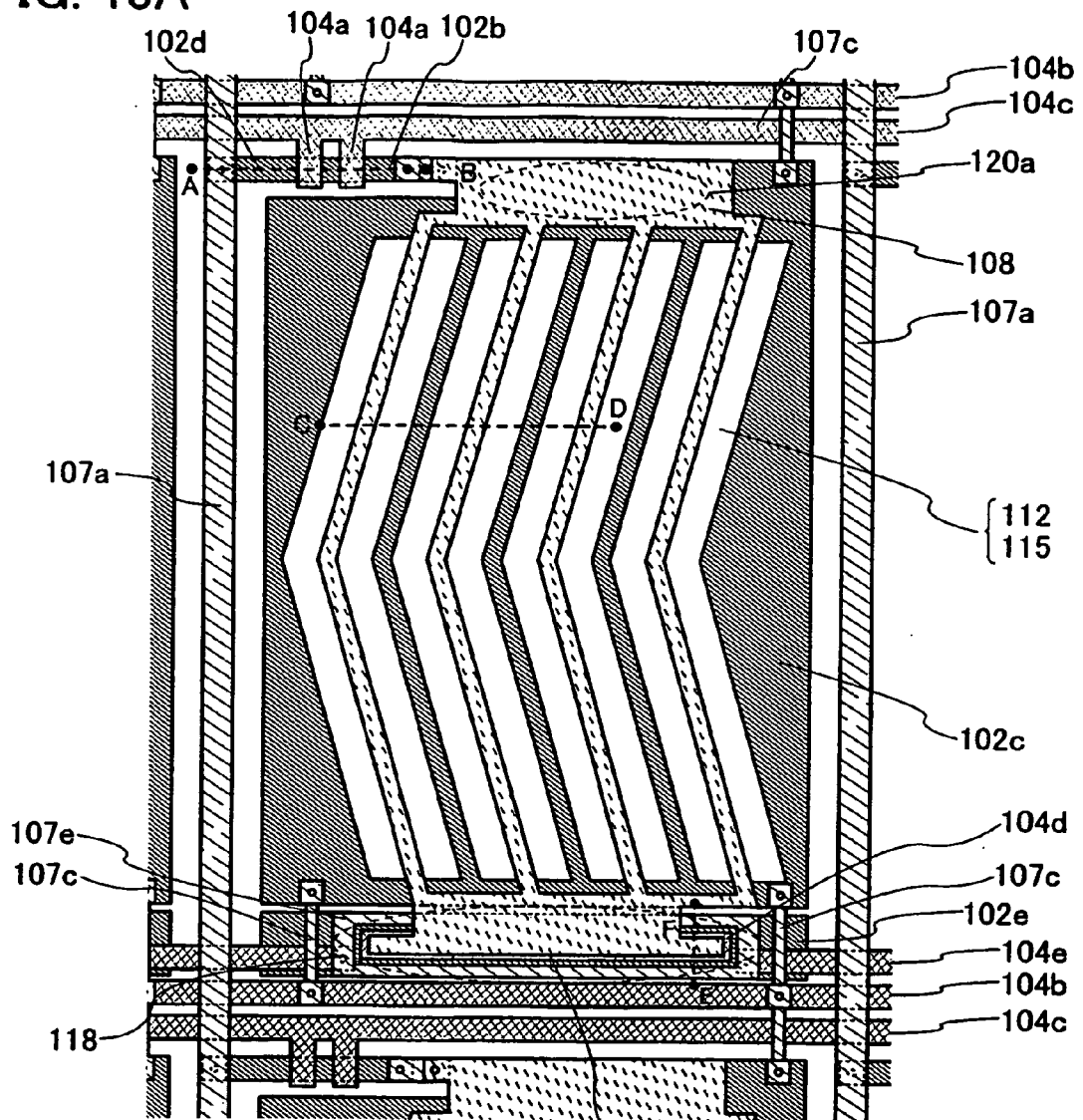


FIG. 15B

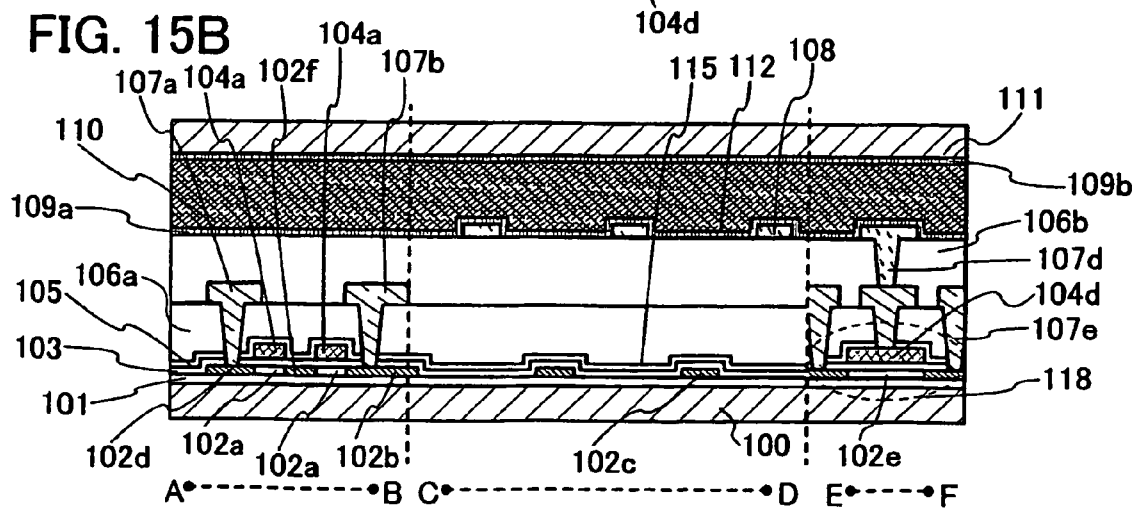


FIG. 16A

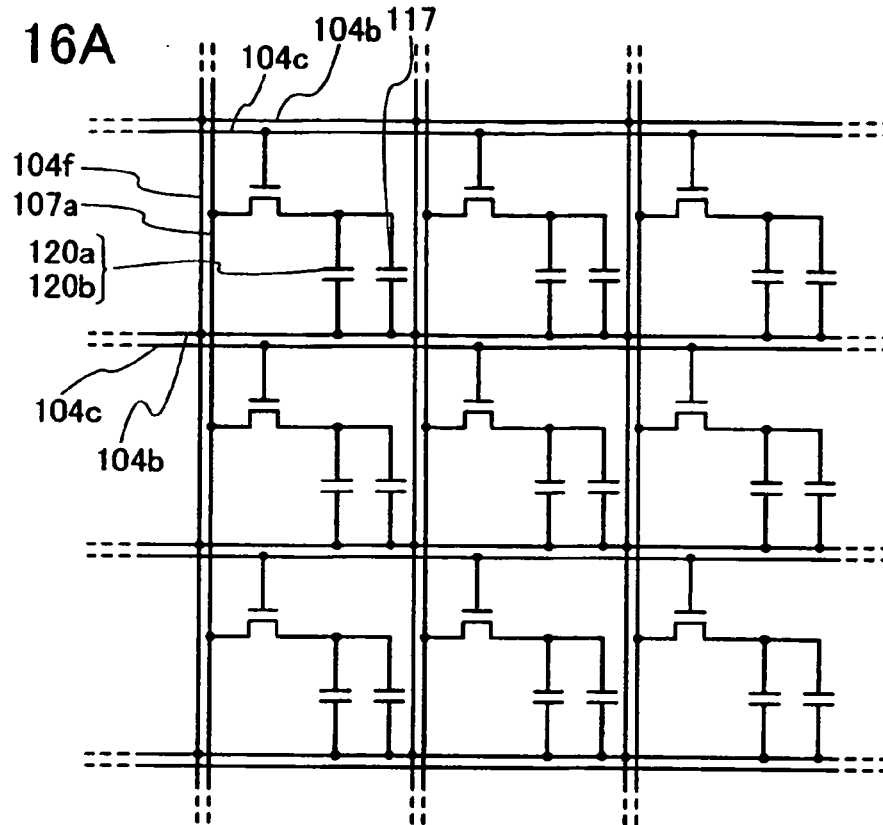


FIG. 16B

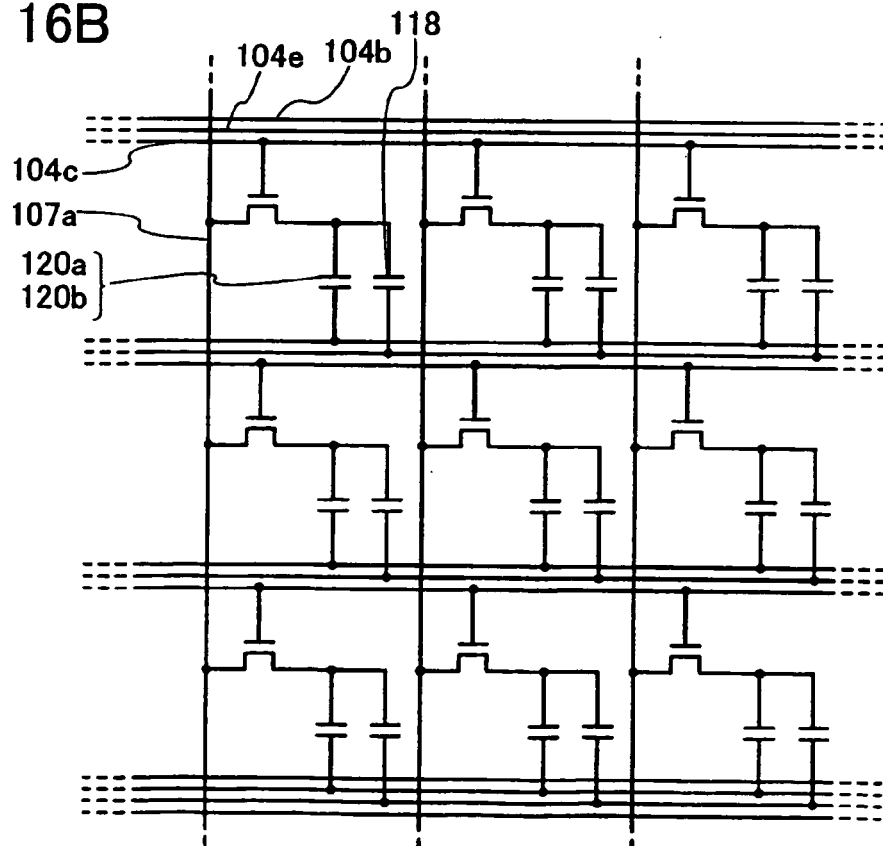




FIG. 17A

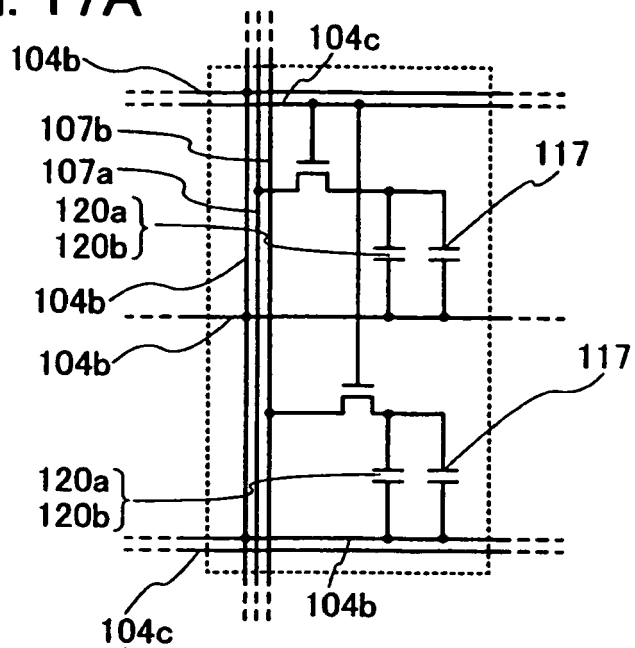


FIG. 17B

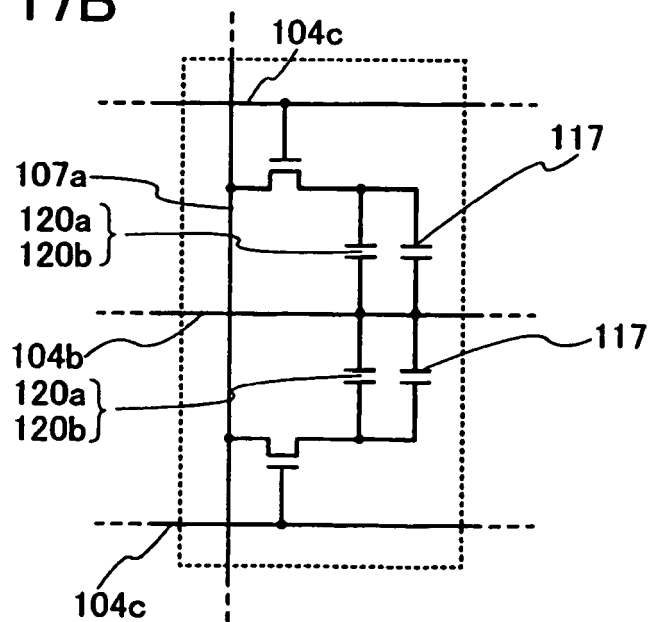


FIG. 18A

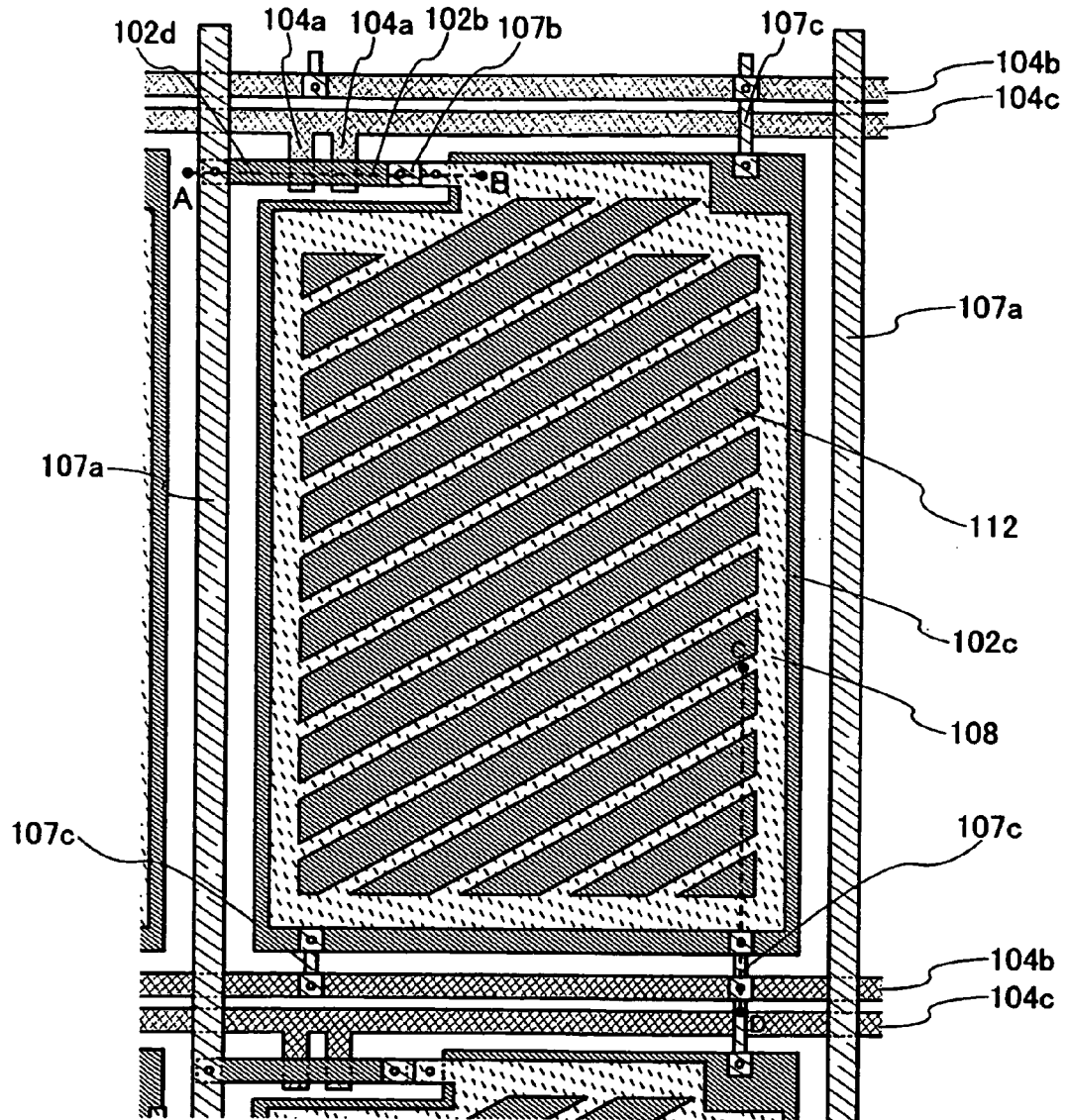


FIG. 18B

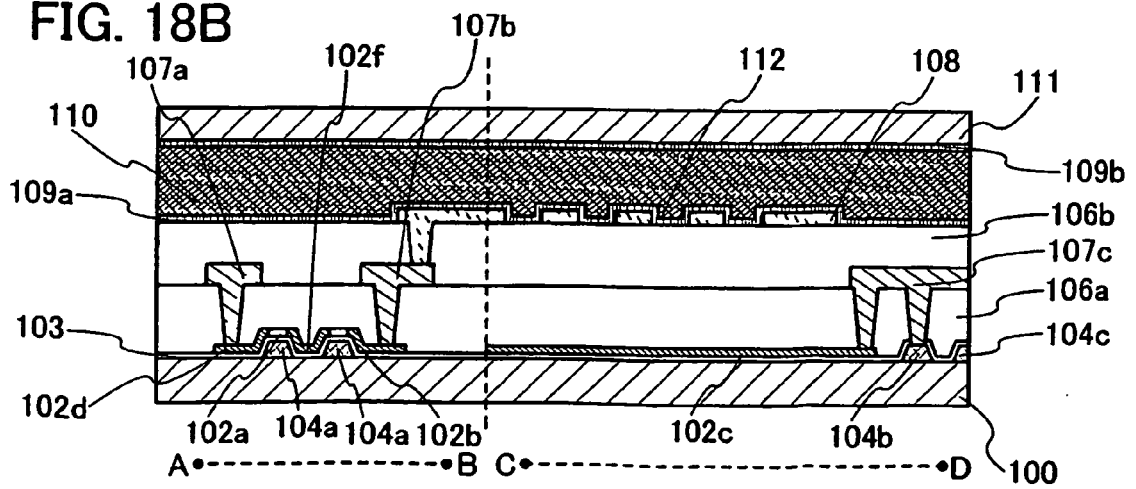


FIG. 19A

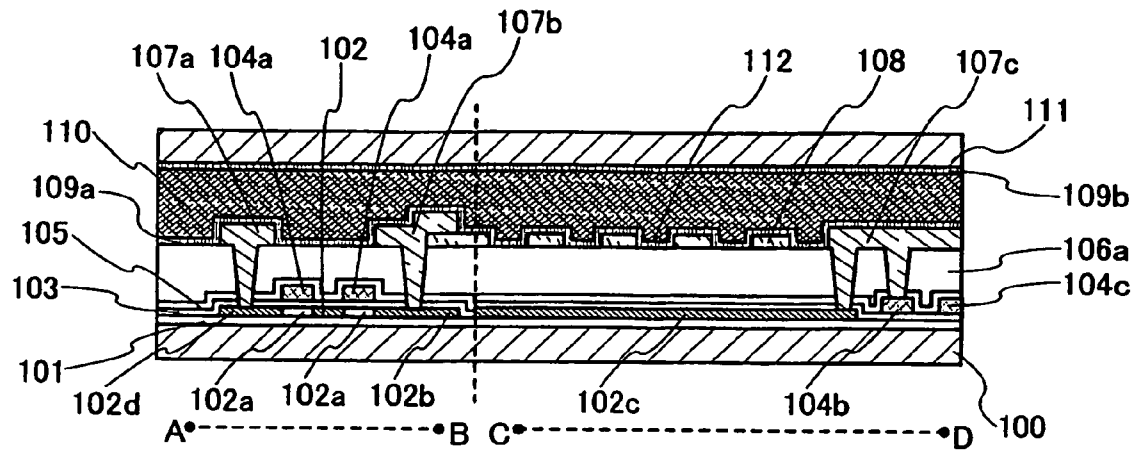
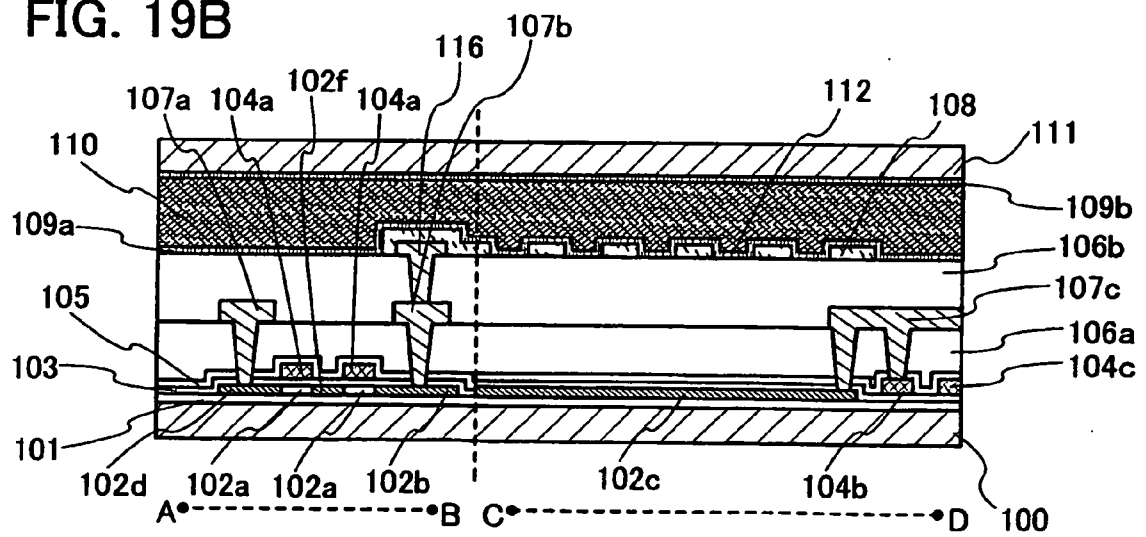


FIG. 19B



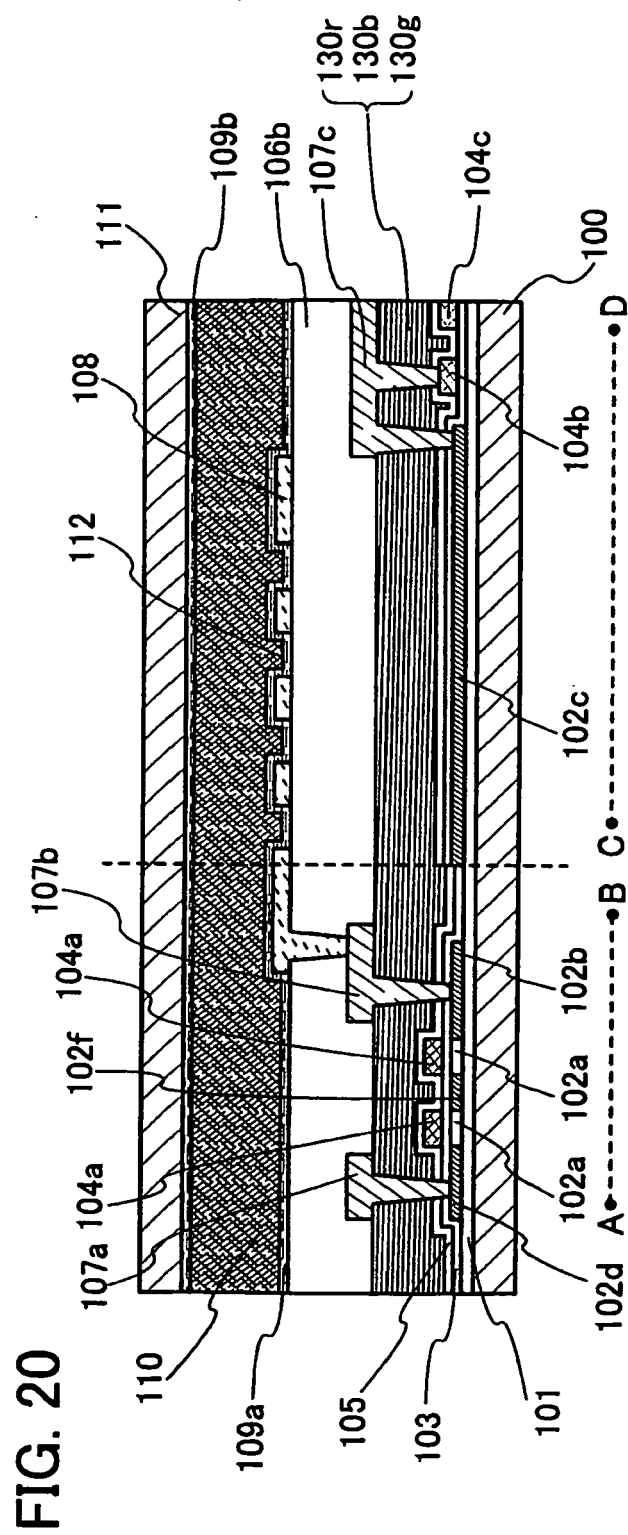


FIG. 21A

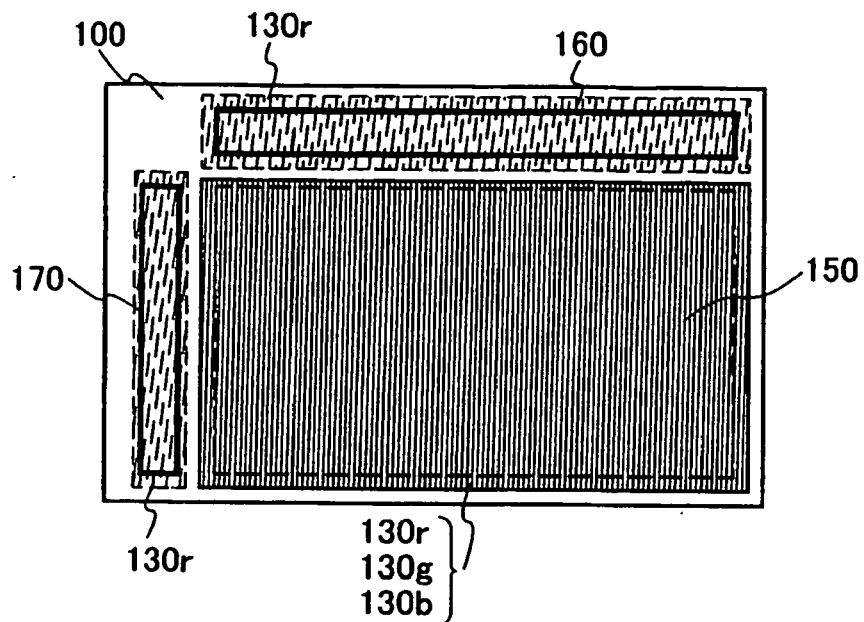


FIG. 21B

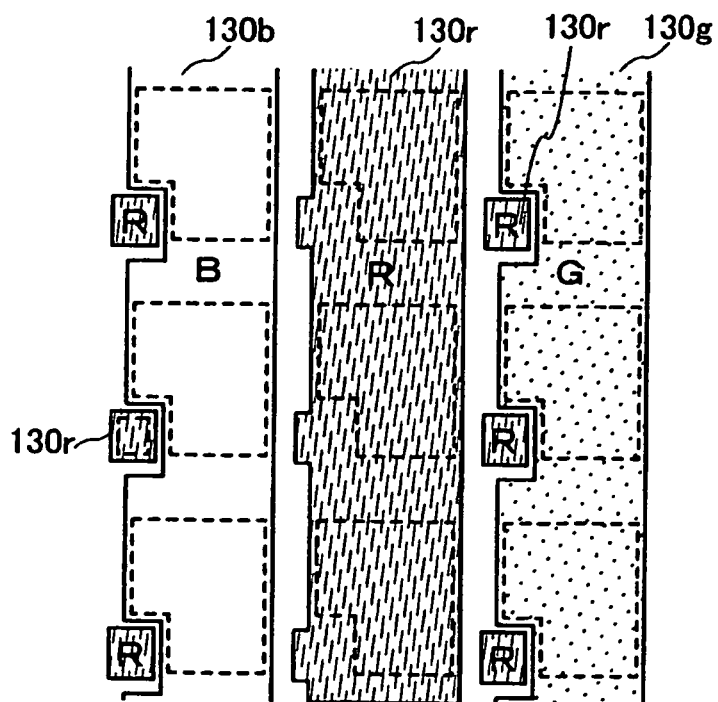


FIG. 22A

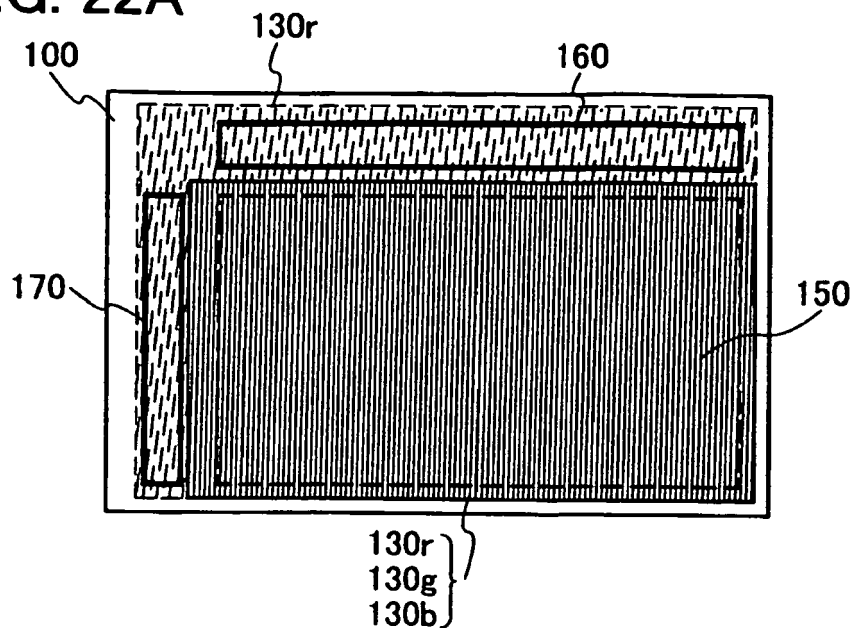
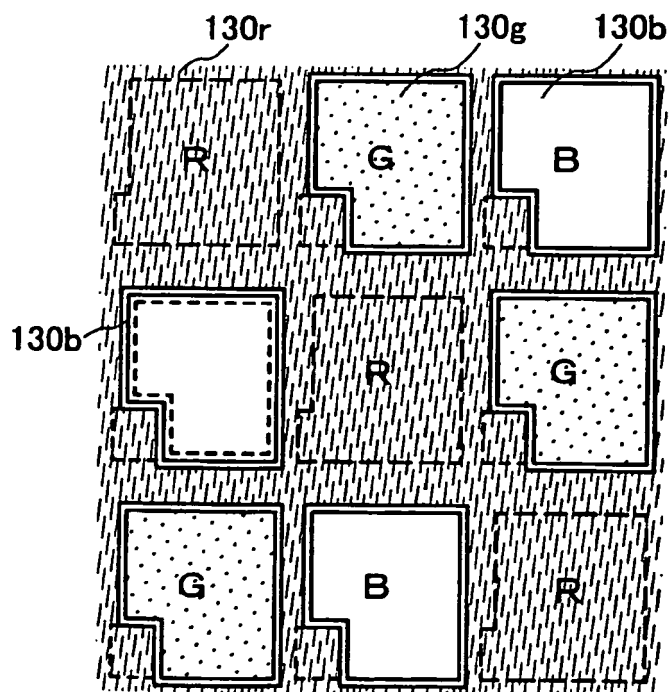


FIG. 22B



**FIG. 23**

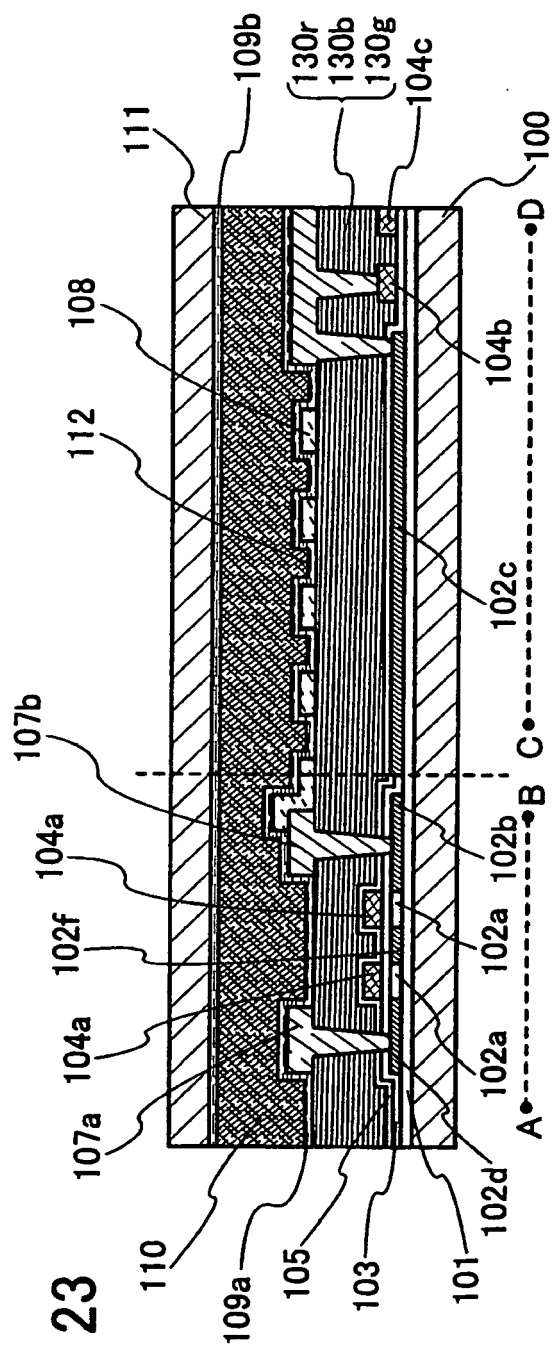


FIG. 24A

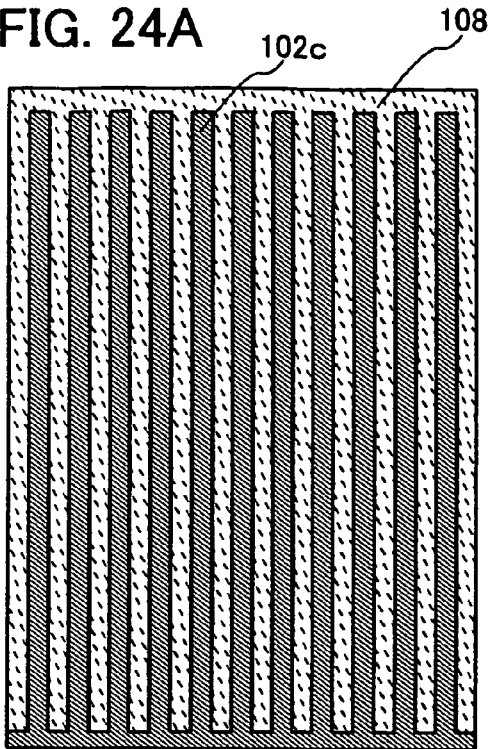


FIG. 24B

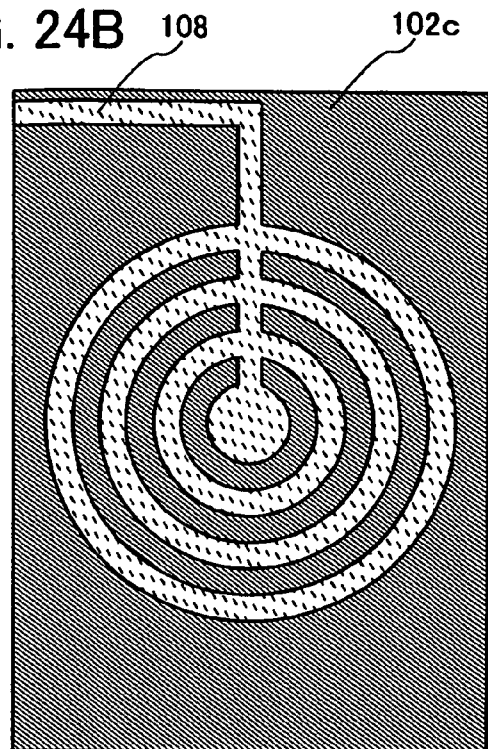


FIG. 24C

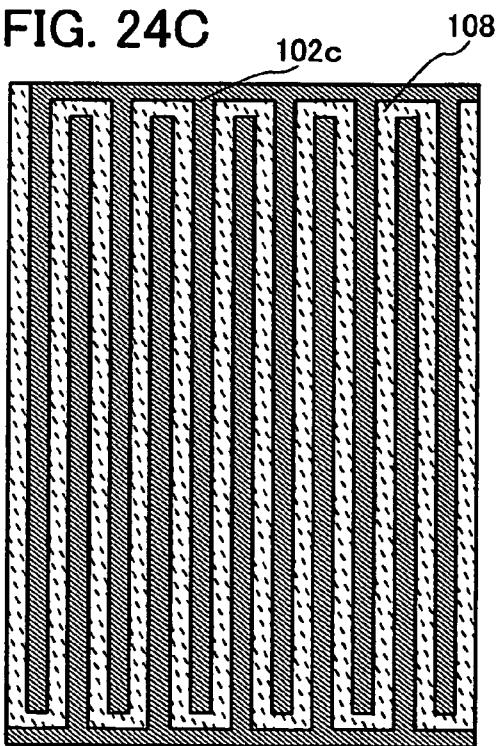
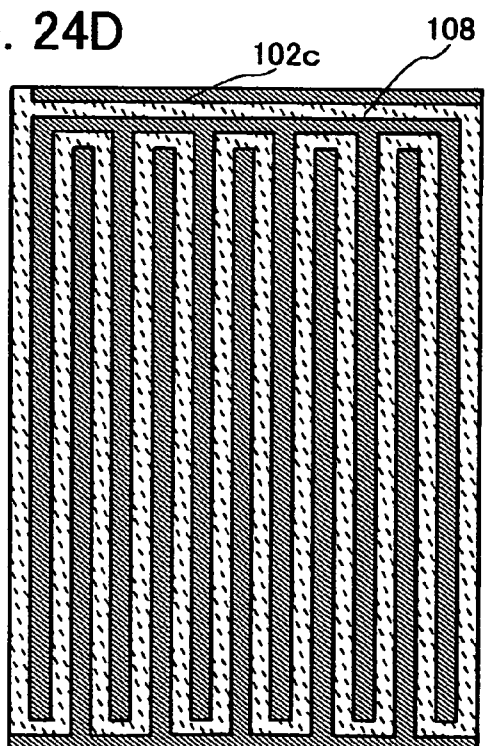


FIG. 24D





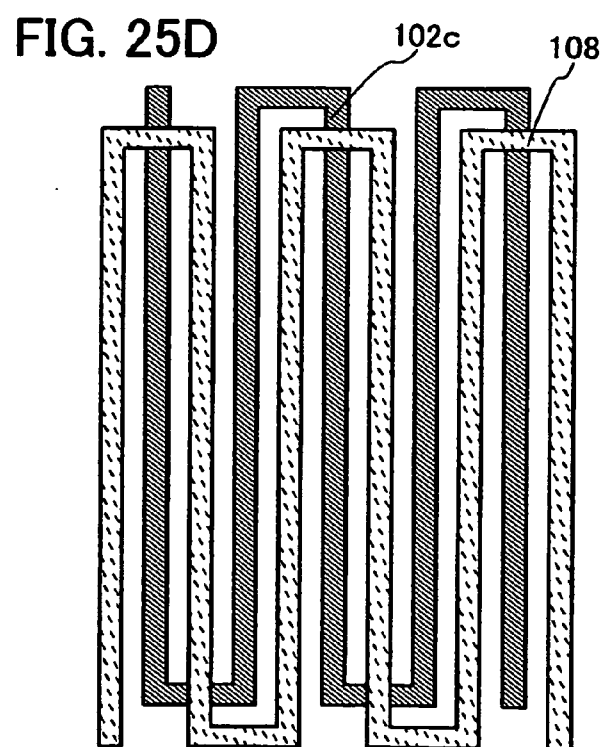
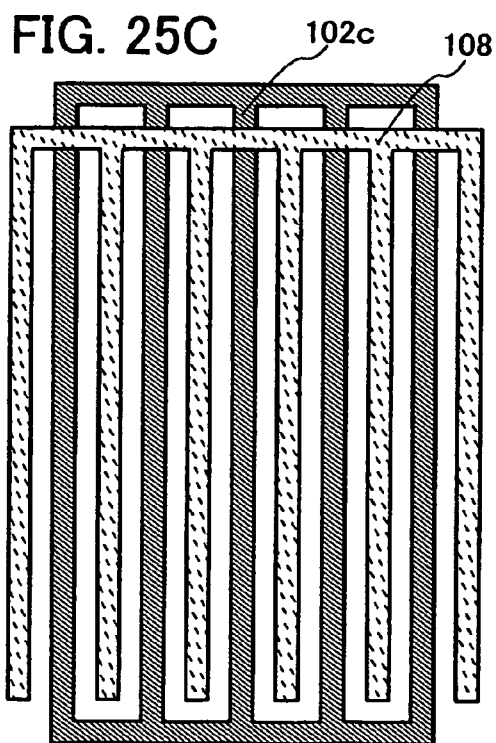
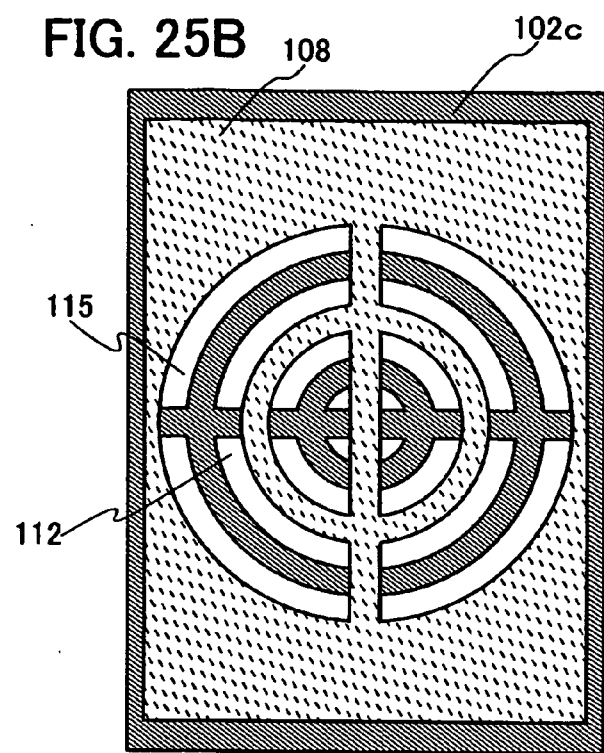
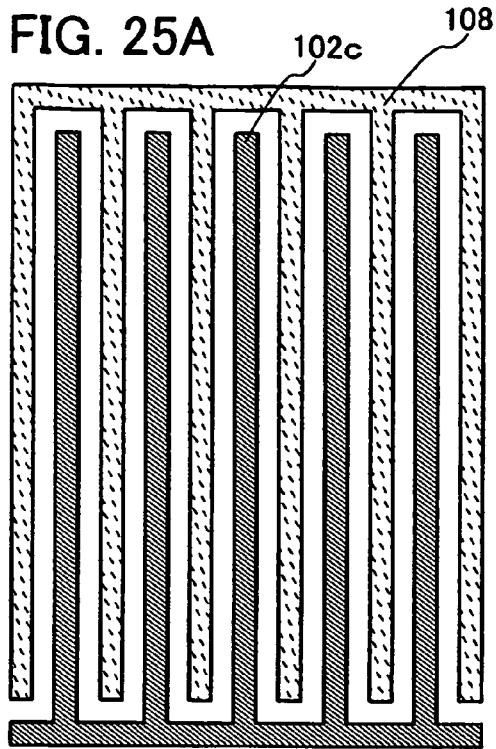


FIG. 26A

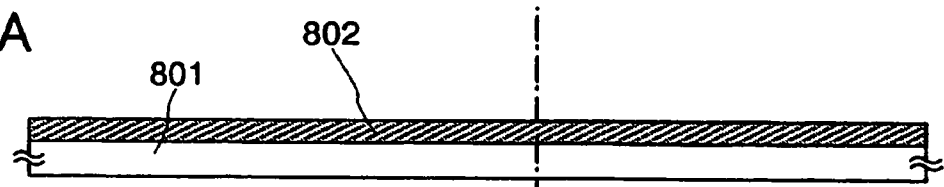


FIG. 26B

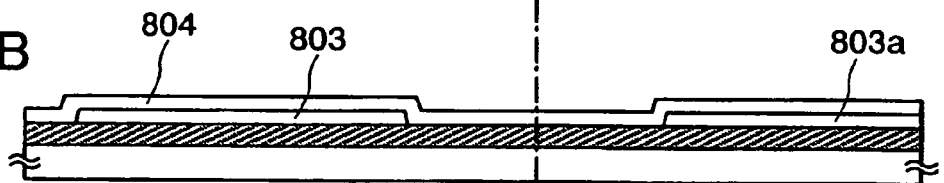


FIG. 26C

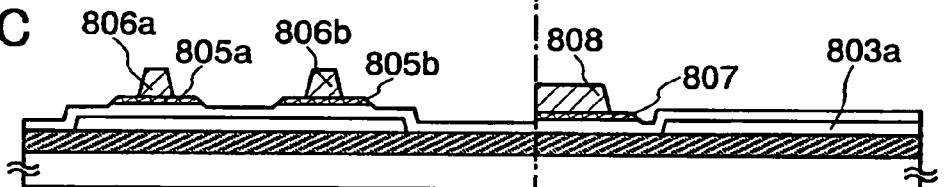


FIG. 26D

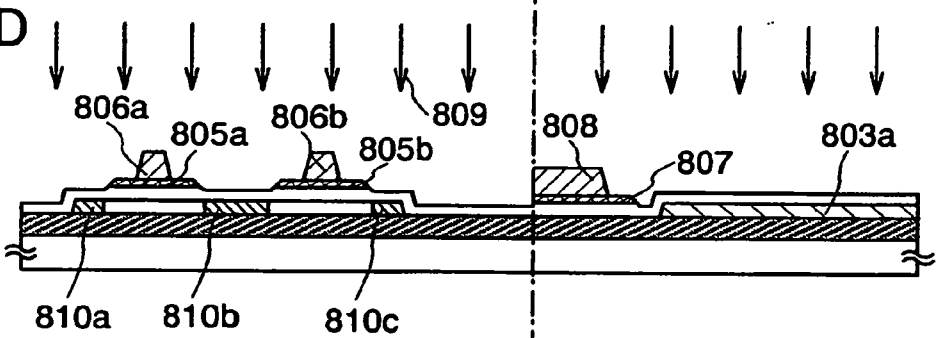


FIG. 26E

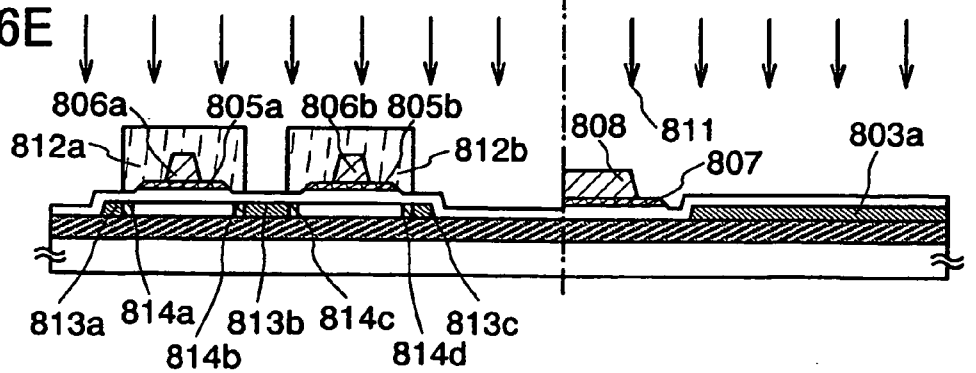


FIG. 27A

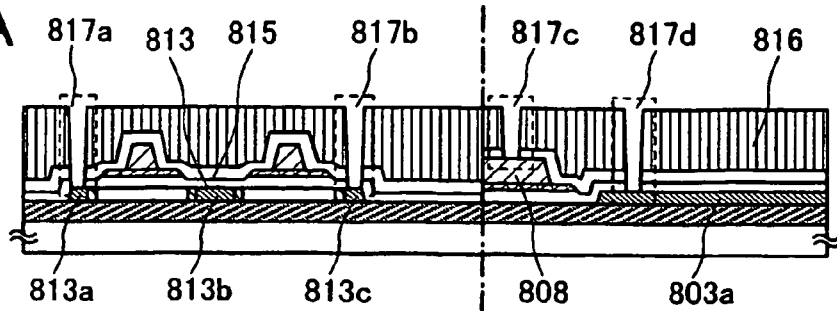


FIG. 27B

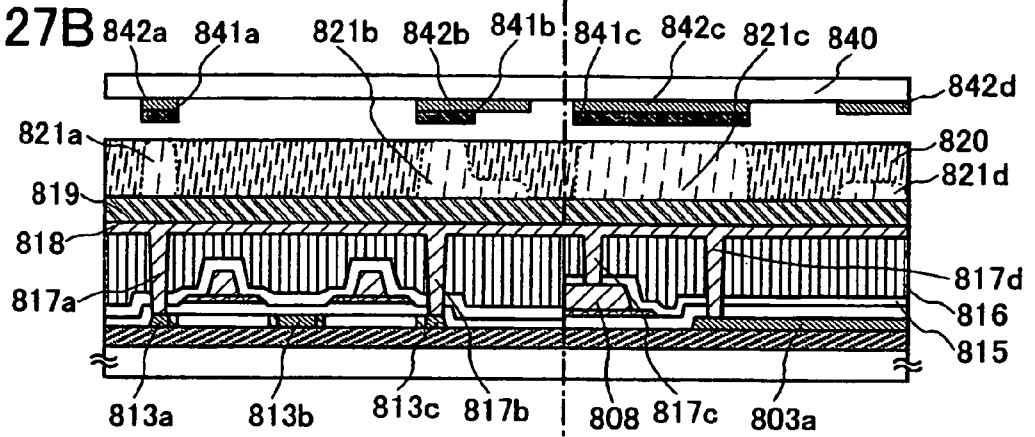


FIG. 27C

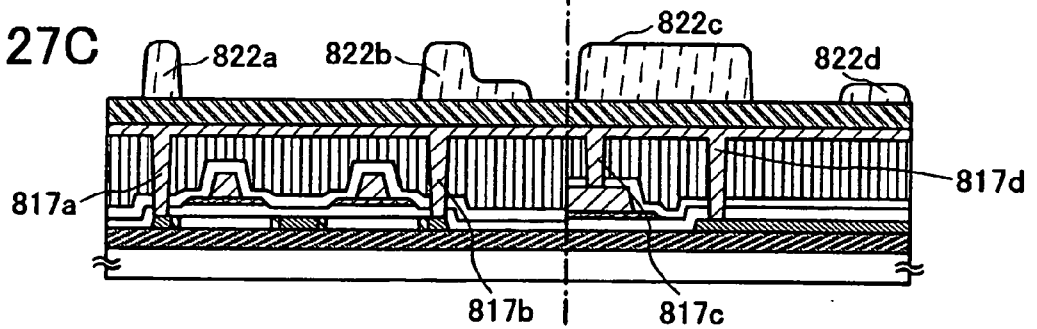


FIG. 27D

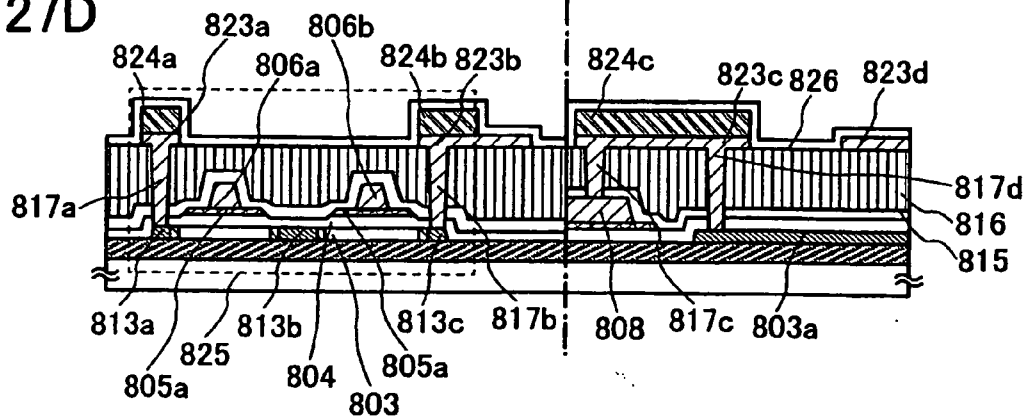


FIG. 28A

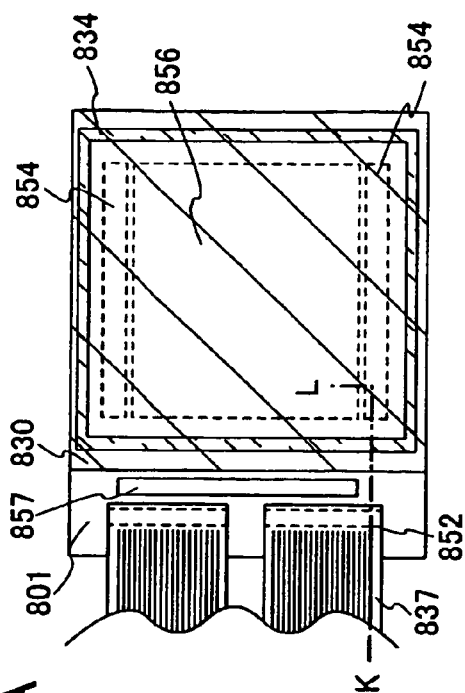


FIG. 28B

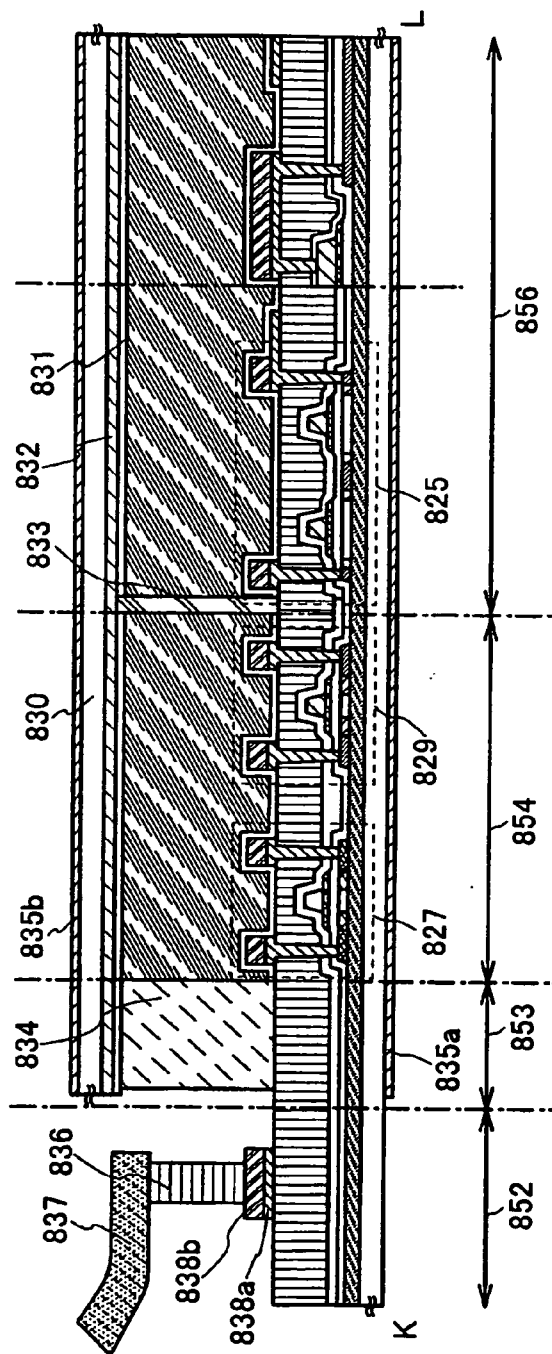


FIG. 29A

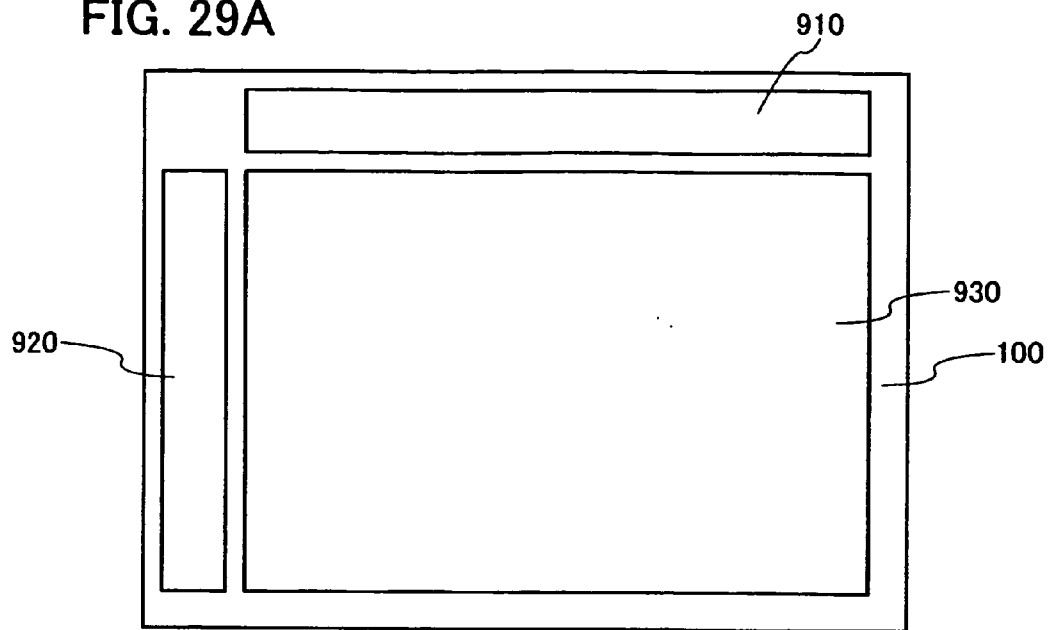


FIG. 29B

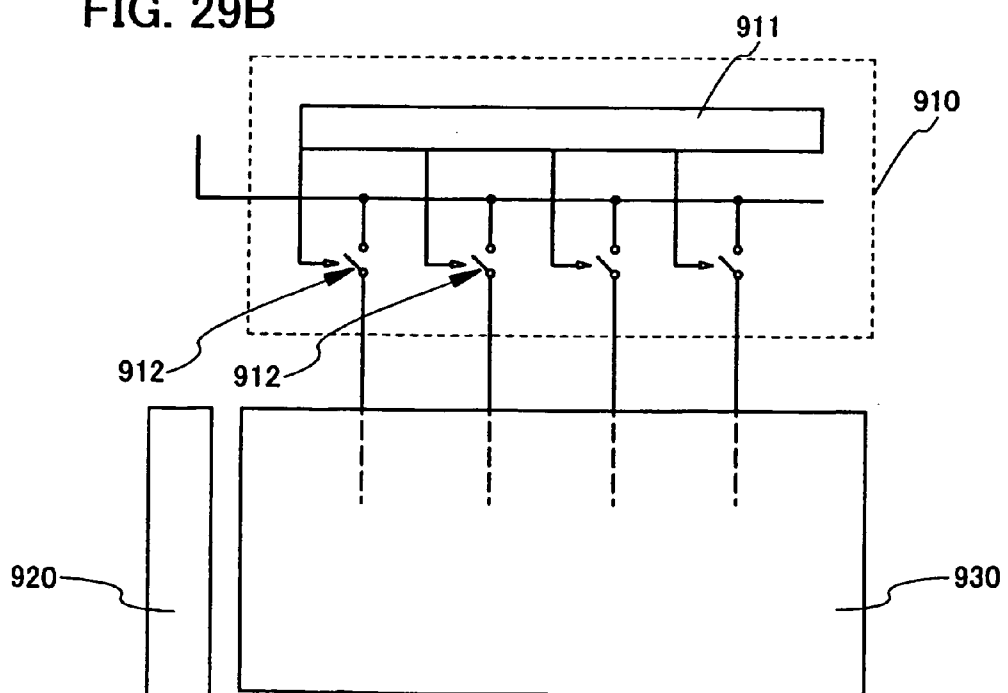


FIG. 30A

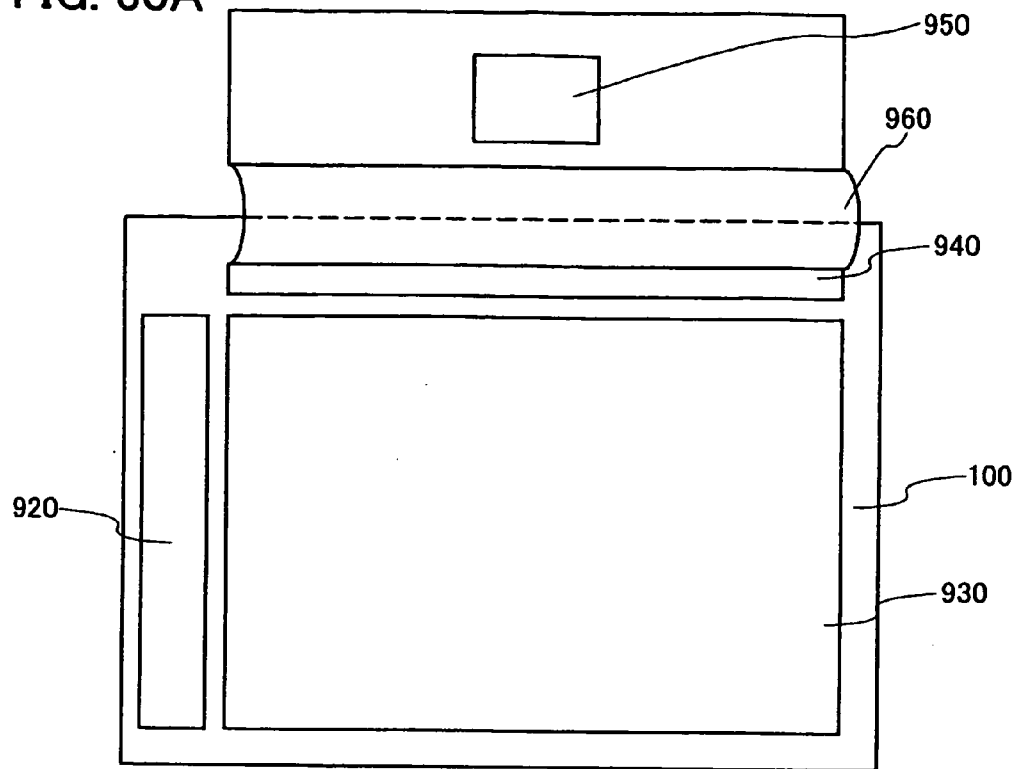


FIG. 30B

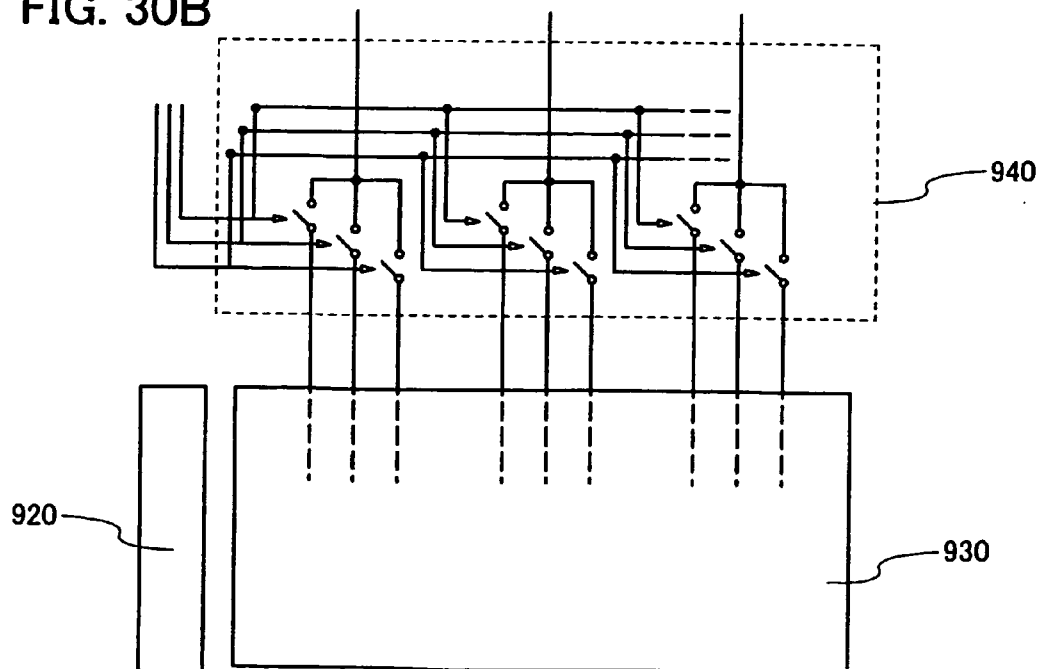


FIG. 31A

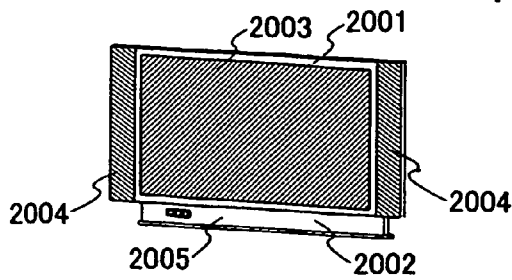


FIG. 31B

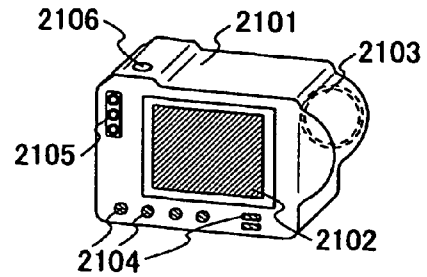


FIG. 31C

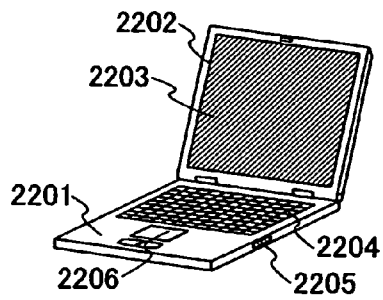


FIG. 31D

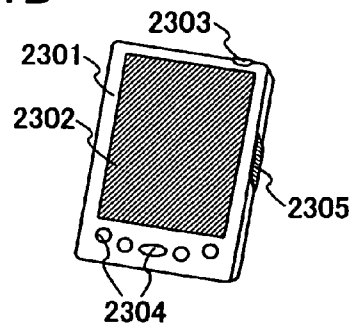


FIG. 31E

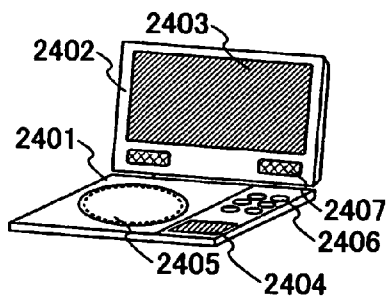


FIG. 31F

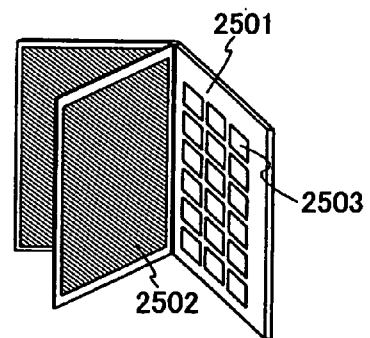


FIG. 31G

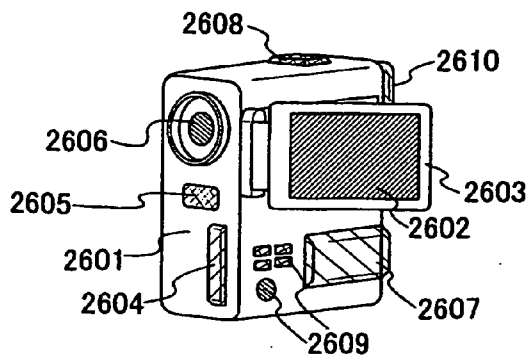


FIG. 31H

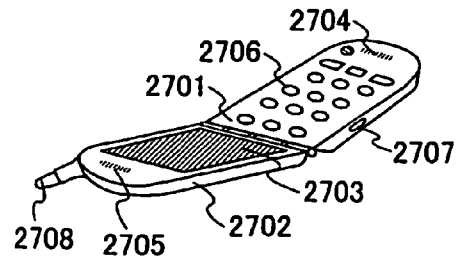


FIG. 32A

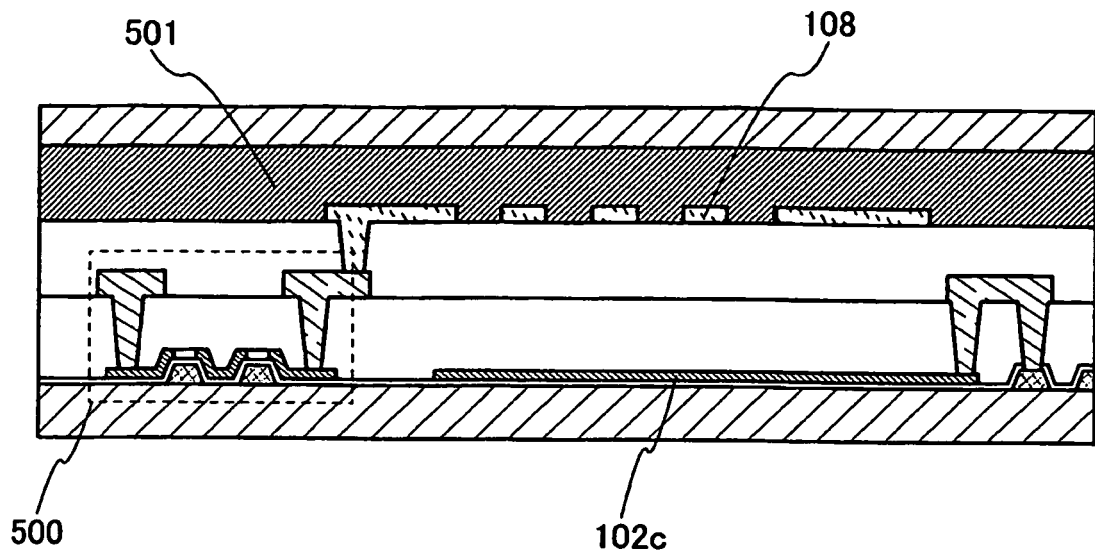
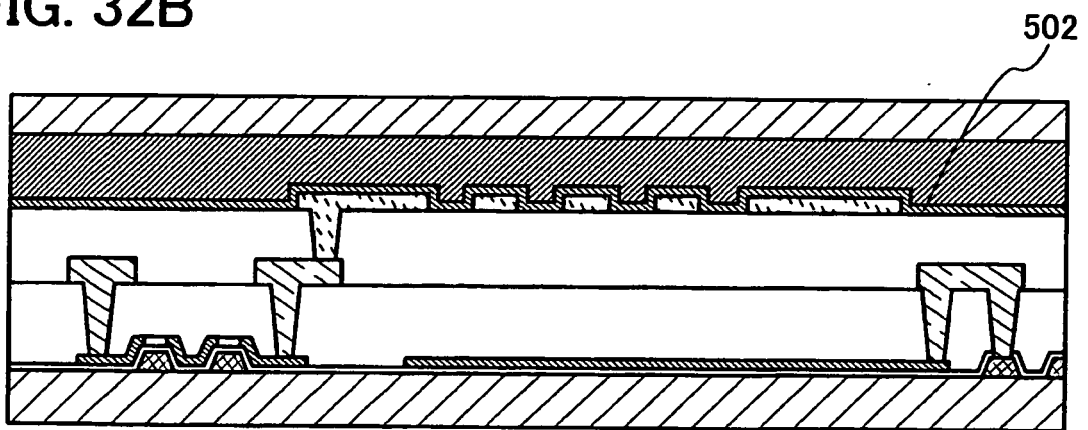


FIG. 32B





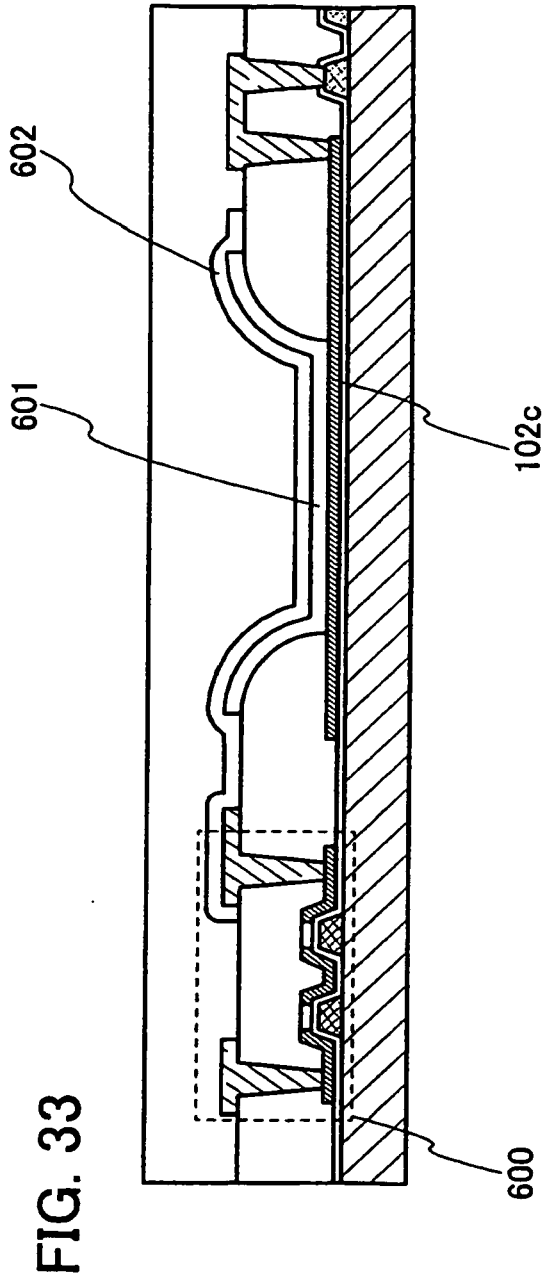


FIG. 34A

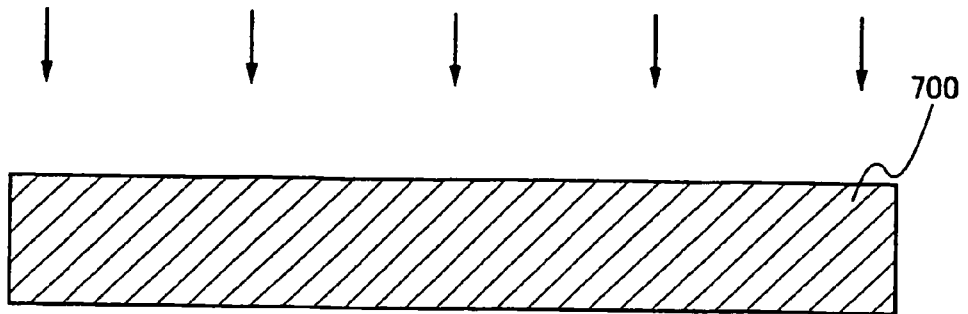


FIG. 34B

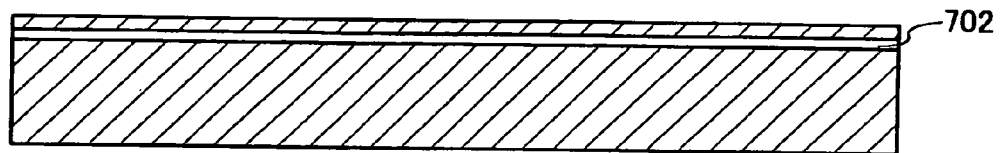


FIG. 34C

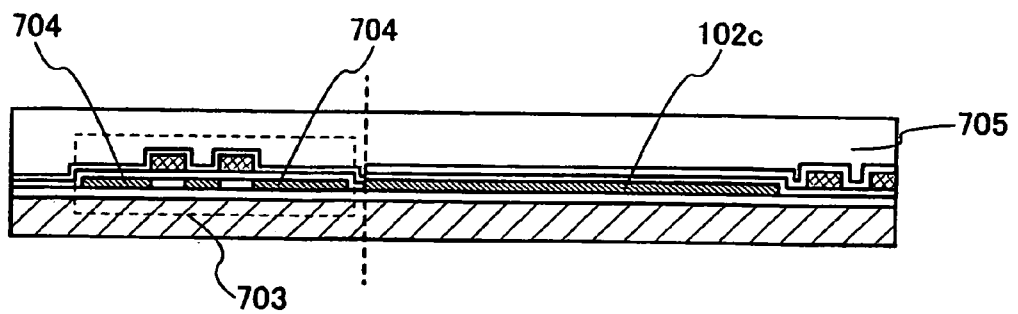
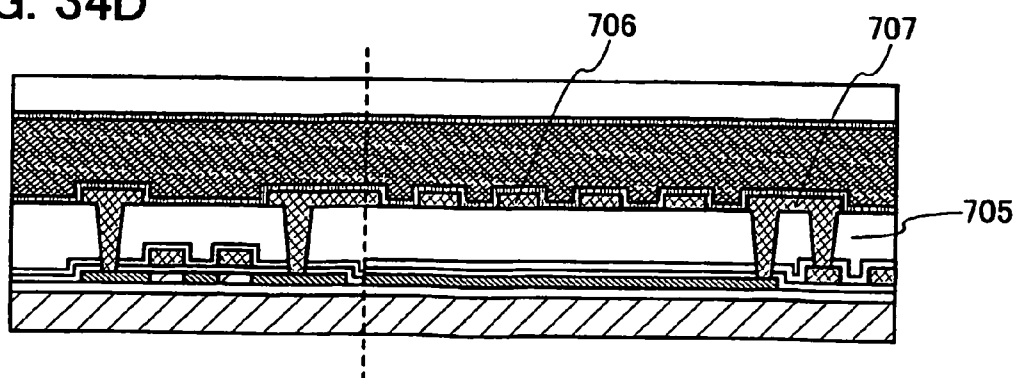


FIG. 34D





## EUROPEAN SEARCH REPORT

Application Number  
EP 10 01 0225

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	KR 2004 012 208 A (BOE HYDIS TECHNOLOGY CO LTD) 11 February 2004 (2004-02-11) * abstract * * figures 2,3a-3e *	1-9	INV. G02F1/1343 H01L27/00
Y	EP 0 685 757 A (MATSUSHITA ELECTRIC IND CO LTD [JP]) 6 December 1995 (1995-12-06) * column 4, line 4 - line 20 * * column 7, line 13 - line 31 * * figures 1A,1B *	1-9	ADD. G02F1/1362
Y	US 6 507 383 B1 (ABE MAKOTO [JP] ET AL) 14 January 2003 (2003-01-14) * figure 21 * * column 31, line 11 - line 33 *	1-9	
Y	US 2001/025958 A1 (YAMAZAKI SHUNPEI [JP] ET AL) 4 October 2001 (2001-10-04) * figures 4A-4C *	1-9	
Y	JP H08 78329 A (SEMICONDUCTOR ENERGY LAB) 22 March 1996 (1996-03-22) * abstract; figure 3 *	1-9	TECHNICAL FIELDS SEARCHED (IPC)
A	KR 2000 0057644 A (HITACHI LTD) 25 September 2000 (2000-09-25) * figure page 2 *	1-9	G02F H01L
A	WO 01/33292 A (HITACHI LTD [JP]; SATO TAKESHI [JP]; KAWACHI GENSHIRO [JP]; MIKAMI YOS) 10 May 2001 (2001-05-10) * abstract * * figure 25 *	1-9	
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 9 June 2015	Examiner Girardin, François
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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## EUROPEAN SEARCH REPORT

Application Number  
EP 10 01 0225

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	US 2004/183978 A1 (JEOUNG HUN [KR] JEOUNG HNN [KR]) 23 September 2004 (2004-09-23) * figures 4,5 * * figures 8,9 * * paragraph [0076] - paragraph [0080] *	1-9	
A	GB 2 166 276 A (SONY CORP) 30 April 1986 (1986-04-30) * the whole document *	1-9	
			TECHNICAL FIELDS SEARCHED (IPC)
The present search report has been drawn up for all claims			
Place of search <b>Munich</b>		Date of completion of the search <b>9 June 2015</b>	Examiner <b>Girardin, François</b>
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons &amp; : member of the same patent family, corresponding document</p>			

 1  
EPO FORM 1503 03.82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 10 01 0225

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The members are as contained in the European Patent Office EDP file on  
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

09-06-2015

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 2004012208 A	11-02-2004	NONE	
EP 0685757 A	06-12-1995	EP 0685757 A2 JP H07325323 A TW 401525 B US 5680190 A	06-12-1995 12-12-1995 11-08-2000 21-10-1997
US 6507383 B1	14-01-2003	JP 3695393 B2 TW 513588 B US 6507383 B1 WO 0171417 A1	14-09-2005 11-12-2002 14-01-2003 27-09-2001
US 2001025958 A1	04-10-2001	JP 2001175198 A US 2001025958 A1 US 2005040400 A1	29-06-2001 04-10-2001 24-02-2005
JP H0878329 A	22-03-1996	JP 3464287 B2 JP H0878329 A	05-11-2003 22-03-1996
KR 20000057644 A	25-09-2000	NONE	
WO 0133292 A	10-05-2001	NONE	
US 2004183978 A1	23-09-2004	KR 20040082796 A US 2004183978 A1 US 2007013820 A1	30-09-2004 23-09-2004 18-01-2007
GB 2166276 A	30-04-1986	CA 1269161 A1 CN 85108619 A DE 3538065 A1 FR 2572569 A1 GB 2166276 A JP H0543095 B2 JP S61102628 A NL 8502881 A	15-05-1990 10-04-1986 10-07-1986 02-05-1986 30-04-1986 30-06-1993 21-05-1986 16-05-1986

**REFERENCES CITED IN THE DESCRIPTION**

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**Patent documents cited in the description**

- JP 2000089255 A [0003]
- JP H878329 B [0341]
- JP 2006105618 A [0392]

专利名称(译)	液晶显示装置，半导体装置和电子设备		
公开(公告)号	<a href="#">EP2924498A1</a>	公开(公告)日	2015-09-30
申请号	EP2010010225	申请日	2007-03-20
[标]申请(专利权)人(译)	株式会社半导体能源研究所		
申请(专利权)人(译)	半导体能源研究所CO.，LTD.		
当前申请(专利权)人(译)	半导体能源研究所CO.，LTD.		
[标]发明人	KIMURA HAJIME		
发明人	KIMURA, HAJIME		
IPC分类号	G02F1/1343 H01L27/00 G02F1/1362		
CPC分类号	G02F1/1303 G02F1/1343 G02F1/134363 G02F1/1362 G02F2001/134372 G02F2001/136231 H01L23/48 H01L27/1214 H01L29/40 G02F1/13439 H01L27/124 H01L2924/0002 H01L2924/00 G02F1/133345 G02F1/133514 G02F1/1337 G02F1/134309 G02F1/136213 G02F1/136286 G02F1/1368 H01L27/1225 H01L27/1255 H01L29/7869 H01L29/78696		
优先权	2006105618 2006-04-06 JP		
外部链接	<a href="#">Espacenet</a>		

#### 摘要(译)

液晶显示装置包括岛状第一半导体膜102，其形成在基底绝缘膜101上，并且其中形成源极102d，沟道形成区102a和漏极102b；第一电极102c，由与第一半导体膜102相同的材料形成，作为源极102d或漏极102b，形成在基底绝缘膜101上；第二电极108，形成在第一电极102c上方并包括第一开口图案112；在第二电极108上提供液晶110。漏电极（102b）和第二电极之间的电接触由导电膜（107b）提供，导电膜（107b）在第二电极（108）上并与之接触。

FIG. 19A

