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(54) DRIVE DEVICE FOR LIQUID CRYSTAL DISPLAY DEVICE

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Description

TECHNICAL FIELD

[0001] The present invention relates to a drive device for liquid crystal display device.

BACKGROUND ART

[0002] In general, a liquid crystal display device of the active matrix system using TFTs (Thin Film Transistors) is constructed with a liquid crystal being interposed between a common electrode and a plurality of pixel electrodes arranged in a matrix pattern.

Then, a desired image is displayed by controlling an applied voltage to the liquid crystal between the common electrode and each pixel electrode.

[0003] The liquid crystal display device of the active matrix system using TFTs is provided with source lines for respective columns of the pixel electrodes arranged in the matrix pattern and with gate lines for respective rows of the pixel electrodes. A TFT is provided for each pixel electrode. Each individual pixel electrode is connected to a TFT and the TFT is connected to a source line and to a gate line. Fig. 9 is an explanatory drawing showing a connection example of a pixel electrode, a TFT, a source line, and a gate line. Fig. 9 illustrates the pixel electrode connected to the gate line G_i of the i -th row and the source line S_k of the k -th column, out of the plurality of pixel electrodes arranged in the matrix pattern. The pixel electrode 21 is connected to a TFT 22 and the TFT 22 is connected to the gate line G_i and to the source line S_k . Specifically, the pixel electrode 21 is connected to the drain 22_b of the TFT 22. Furthermore, the gate 22_a of the TFT 22 is connected to the gate line G_i and the source 22_c of the TFT 22 is connected to the source line S_k . Fig. 9 shows one pixel electrode, and connection forms of the TFT, gate line and source line in the other pixel electrodes are also the same.

[0004] Each gate line is selected in a line-sequential manner, a selected gate line is set at a selected-period potential, and the nonselected gate lines are set at a non-selected-period potential. When a certain gate line is selected, the source lines are set at respective potentials according to image data for a row of the selected gate line. In the TFT 22 arranged for each pixel electrode, when the gate 22_a turns to the selected-period potential, the drain 22_b and the source 22_c become electrically conductive; when the gate 22_a turns to the nonselected-period potential, the drain 22_b and the source 22_c become electrically nonconductive. Therefore, the pixel electrodes in the selected row are set at their respective potentials according to the image data for the row. A potential of the common electrode 30 (see Fig. 9) opposed to each pixel electrode through the liquid crystal (not shown) is also controlled to a predetermined potential. As a consequence of this, voltages according to the image data for the row are applied to the liquid crystal in the selected

row. By sequentially selecting the gate lines, an image according to the image data can be displayed. The potential of the common electrode will be denoted below by V_{COM} .

[0005] In some parts of the description hereinafter, a value of the selected-period potential will be denoted by V_{GH} and a value of the nonselected-period potential by V_{GL} .

[0006] A state in which the potential of a pixel electrode is higher than the potential of the common electrode will be referred to as positive polarity. Moreover, a state in which the potential of a pixel electrode is lower than the potential of the common electrode will be referred to as negative polarity.

[0007] As an example of modes for switching the positive and negative polarities, there is a mode of switching the polarities every two rows in each column, while making the polarities different from each other between adjacent columns. This mode will be referred to hereinafter as two-line dot inversion drive. Fig. 10 shows an example of the polarities of respective pixels in the two-line dot inversion drive. In the description hereinafter, the first column is defined as the leftmost column when viewed from the viewer side of the liquid crystal display device and the columns are counted from the left. In the drawings including Fig. 10 and others, "+" indicates the positive polarity and "-" the negative polarity. In the two-line dot inversion drive, when attention is focused on each individual row in a certain frame, as shown in Fig. 10, the polarities of the pixels are different between adjacent columns. For example, with focus on the first row, the pixels in the first row have different polarities between adjacent pixels. In this manner, while the polarities are made different between adjacent pixels in each individual row, the polarities of the pixels in each column are switched every two rows. As a result, for example, in the first column, the pixels in the first row and the second row have the positive polarity and the pixels in the third row and the fourth row have the negative polarity. Furthermore, for example, in the second column, the pixels in the first row and the second row have the negative polarity and the pixels in the third row and the fourth row have the positive polarity.

[0008] Fig. 11 is a timing chart showing an example of the potential changes in gate lines and a source line in the two-line dot inversion drive. In Fig. 11, G_1 to G_4 refer to the gate lines of the respective rows from the first row to the fourth row. Furthermore, S_1 refers to the source line of the first column. As shown in Fig. 11, each of the gate lines is selected starting from the gate line G_1 and the gate line selected is set at the selected-period potential V_{GH} . Latch pulses (which will be referred to hereinafter as LP) shown in Fig. 11 are a pulse signal to define start timing of potential setting for the source lines. At a falling edge of LP, each source line is set to a potential according to each pixel in the selected row.

[0009] As shown in Fig. 11, the source line S_1 is set to potentials higher than the common electrode potential

V_{COM} during selected periods of the gate lines of the first row and the second row, and is set to potentials lower than the common electrode potential V_{COM} during selected periods of the gate lines of the third row and the fourth row. Thereafter, the source line is alternately switched between potentials higher than V_{COM} and potentials lower than V_{COM} every two rows in the same manner. The same also applies to the source lines of the other odd-numbered columns. Each of the source lines of the even-numbered columns, which are omitted from the illustration in Fig. 11, is set to potentials lower than V_{COM} during selected periods of the first row and the second row and is set to potentials higher than V_{COM} during selected periods of the third row and the fourth row. Thereafter, the source line is alternately switched between potentials lower than V_{COM} and potentials higher than V_{COM} every two rows in the same manner. This example shows a case where with LP at a high level, each source line is kept in a high impedance state.

[0010] As the potentials of the respective gate lines and the respective source lines are set as described above, the polarities of the respective pixels become as illustrated in Fig. 10. In the next frame, the liquid crystal display device is driven so as to invert the polarities of the respective pixels.

[0011] There is another mode for switching the polarities every row in each column, while making the polarities different between adjacent columns. This mode will be referred to hereinafter as one-line dot inversion drive. Fig. 12 shows an example of polarities of respective pixels in the one-line dot inversion drive. In the one-line dot inversion drive, as shown in Fig. 12, the polarities are different between adjacent pixels in each of directions of the columns and rows.

[0012] Concerning the one-line dot inversion drive, there is a known drive method of, prior to a selected period of a gate line of a certain row, setting a potential of the gate line to the selected-period potential VGH in advance. This drive method is also called a double gate method. In the double gate method, for example, the potentials of the gate lines of the first row and the third row are simultaneously set to the selected-period potential VGH in the selected period of the first row, and the potentials of the gate lines of the third row and the fifth row are simultaneously set to the selected-period potential VGH in the selected period of the third row. In this case, the gate line of the third row, together with the first row, is set to the selected-period potential VGH during the selected period of the first row, prior to a start of the selected period of the gate line of the third row itself. The same also applies to the rows other than the third row. In this manner, prior to a selected period of the gate line of a certain row, the potential of the gate line is set to the selected-period potential VGH in advance, whereby the pixels in that row can be subjected to precharge, which can reduce power consumption.

[0013] Fig. 13 is a timing chart showing an example of the potential changes in gate lines and a source line in

the case where the double gate method is adopted in the one-line dot inversion drive. As shown in Fig. 13, in the selected period of the gate line G_1 of the first row, not only the gate line G_1 but also the gate line G_3 are set to the selected-period potential VGH. In the selected period of the gate line G_1 , duration during which the gate lines G_1 and G_3 are set at the selected-period potential VGH are identical. Thereafter, in the selected period of the gate line G_n of the n-th row, not only the gate line G_n but also the gate line G_{n+2} are set to the selected-period potential VGH in the same manner. In the selected period of the gate line G_n , duration during which the gate lines G_n and G_{n+2} are set at the selected-period potential VGH are identical.

[0014] As shown in Fig. 13, the source line S_1 is set to a potential higher than the common electrode potential V_{COM} during the selected period of the gate line G_1 of the first row and is set to a potential lower than the common electrode potential V_{COM} during the selected period of the gate line G_2 of the second row. Thereafter, the source line is alternately switched between a potential higher than V_{COM} and a potential lower than V_{COM} every row in the same manner. The same also applies to the source lines of the other odd-numbered columns. Each of the source lines of the even-numbered columns, which are omitted from the illustration in Fig. 13, is set to a potential lower than the common electrode potential V_{COM} during the selected period of the gate line G_1 and is set to a potential higher than the common electrode potential V_{COM} during the selected period of the gate line G_2 . Thereafter, the source line is alternately switched between a potential lower than V_{COM} and a potential higher than V_{COM} every row in the same manner. With LP at the high level, each source line is kept in a high impedance state.

[0015] As the potentials of the respective gate lines and the respective source lines are set in this manner, the polarities of the respective pixels become as shown in Fig. 12. The double gate method can reduce power consumption when compared to the simple line-sequential drive.

[0016] The double gate method is described, for example, in Patent Documents 1, 2 and others. Patent Document 1 discloses that a preliminary on-signal is set at least two lines prior to a regular on-signal. The pulse duration of the regular on-signal is the same as the pulse duration of the preliminary on-signal.

[0017] Patent Document 2 discloses that when H represents the selected period of each gate line, the gate line of the N-th row is again set to the selected-period potential with a lapse of 4H since a time of a start of the selected period of the gate line of the N-th row. Duration during which the gate line of the N-th row is again set at the selected-period potential is also H. Furthermore, Patent Document 2 discloses that the potentials of the source lines are switched between potentials in the positive polarity and potentials in the negative polarity every 2H, to realize the switching of polarities as exemplified in Fig.

10.

[0018] Patent Document 3 discloses that a gate drive waveform is kept continuous for at least two clocks.

[0019] Patent documents 4 and 5 each disclose respective settings of the gate line of an even numbered row at a selected period potential with a delay of a first predetermined time from timing when the gate line of the odd-numbered row is set at the selected period potential.

[0020] Patent document 6 discloses the selecting of one gate line, and a subsequent gate line that is a gate line of a row after the next to the one gate line.

PRIOR ART DOCUMENTS

PATENT DOCUMENTS

[0021]

Patent Document 1: JP-A-4-67122 (Page 3, Fig. 1)

Patent Document 2: JP-A-2001-249643 (Paragraphs 0016-0024, Fig. 4)

Patent Document 3: JP-A-2001-195043 (Page 1)

Patent Document 4: US2006/208984 (Paragraphs 0159-0161, Figs. 8A, 8B)

Patent Document 5: US2007/262310 (Paragraph 0045, Fig. 4)

Patent Document 6: US2010/0231617 (Paragraphs 0151-0156, Figs. 8, 9)

DISCLOSURE OF INVENTION

TECHNICAL PROBLEM

[0022] In the two-line dot inversion drive, it is preferable to make power consumption as low as possible.

[0023] In the one-line dot inversion drive, it is also preferable to make power consumption as low as possible.

[0024] It is therefore an object of the present invention to provide a drive device for liquid crystal display device that can realize the one-line dot inversion drive with less power consumption.

SOLUTION TO PROBLEM

[0025] A drive device for liquid crystal display device according to an example is a drive device for liquid crystal display device, which drives a liquid crystal display device including source lines arranged along columns of pixels formed in a matrix pattern and gate lines arranged along rows of the pixels formed in the matrix pattern, the drive device for liquid crystal display device comprising: a gate driver (e.g., gate driver 3) which selects a gate line of an odd-numbered row and a gate line of an even-numbered row subsequent thereto, which sets the gate line of the even-numbered row at a selected-period potential with a delay of a first predetermined time (e.g., t) from timing when the gate line of the odd-numbered row is set at the selected-period potential (e.g., VGH), and which there-

after sets the gate line of the odd-numbered row at a nonselected-period potential (e.g., VGL); and a source driver (e.g., source driver 4 in the example) which switches polarities of the pixels in each column every two rows and which sets potentials of the respective source lines to potentials according to image data of respective pixels for one row, while making the polarities of the pixels in adjacent columns opposite to each other.

[0026] The drive device for liquid crystal display device according to the example may be configured as follows: it comprises: control means (e.g., timing controller 2) which feeds to the gate driver, a switching signal (e.g., CKV in the example) to indicate switching of gate lines to be selected, an output enable signal for an odd-numbered row to indicate a duration during which the gate line of the odd-numbered row selected is kept at the selected-period potential, and an output enable signal for an even-numbered row to indicate duration during which the gate line of the even-numbered row selected is kept at the selected-period potential, and which feeds to the source driver, a source line potential setting indication signal (e.g., LP) to indicate that the potentials of the respective source lines are to be set to potentials according to image data of the respective pixels for one row, and a polarity control signal (e.g., POL_2 in the example) to make the polarities of the pixels in each column switched every two rows; the control means operates as follows: the control means feeds a signal changed to a first level (e.g., a high level) and a second level (e.g., a low level) in a predetermined period, as the switching signal to the gate driver; the control means raises the source line potential setting indication signal at timing when the switching signal is changed to the first level, and defines a period of the source line potential setting indication signal as half of the period of the switching signal; the control means feeds to the gate driver, the output enable signal for odd-numbered row (e.g., OE_{odd}) to indicate as the duration during which the gate line of the odd-numbered row is kept at the selected-period potential, a duration of H-s from a change of a level of the switching signal to the first level when $2H$ represents the period of the switching signal, t represents the first predetermined time, and s represents a second predetermined time, and the output enable signal for an even-numbered row (e.g., OE_{even}) to indicate as the duration during which the gate line of the even-numbered row is kept at the selected-period potential, duration from a point of time when t has elapsed since the change of the level of the switching signal to the first level, to a point of time when $2H-s$ has elapsed since the change of the level of the switching signal to the first level; the gate driver operates as follows: the gate driver selects a gate line of an odd-numbered row and a gate line of an even-numbered row subsequent thereto, every switching of the switching signal to the first level, and sets the selected gate line of the odd-numbered row to the selected-period potential in accordance with the output enable signal for an odd-numbered row and the selected gate line of the even-numbered row to the

selected-period potential in accordance with the output enable signal for an even-numbered row; and the source driver sets the potentials of the respective source lines to potentials according to image data of respective pixels for one row in synchronism with a falling edge of the source line potential setting indication signal.

[0027] In the drive device for liquid crystal display device according to the example, the first predetermined time is preferably a time that is at least the sum of a time needed to change the potentials of the source lines from a minimum to a maximum of set potentials for the source lines, and a time needed to change the source line potential setting indication signal to a high level.

[0028] A drive device for liquid crystal display device according to an aspect of the present invention is a drive device for liquid crystal display device, which drives a liquid crystal display device including source lines arranged along columns of pixels formed in a matrix pattern and gate lines arranged along rows of the pixels formed in the matrix pattern, the drive device for liquid crystal display device comprising: a gate driver (e.g., gate driver 3_a) which selects a gate line; and a source driver (e.g., source driver 4 in the embodiment of the present invention) which switches polarities of the pixels in each column every row and which sets potentials of the respective source lines to potentials according to image data of respective pixels for one row, while making the polarities of the pixels in adjacent columns opposite to each other, wherein the gate driver selects one gate line, and a subsequent gate line that is a gate line of a row after the next to the one gate line, sets the subsequent gate line to a selected-period potential with a delay of a first predetermined time (e.g., t) from timing when the one gate line is set at the selected-period potential (e.g., VGH), and sets the one gate line and the subsequent gate line to a non-selected-period potential (e.g., VGL), prior to selection of the gate line next to the one gate line.

[0029] The drive device for liquid crystal display device according to the present invention may be configured as follows: it comprises: control means (e.g., timing controller 2_a) which feeds to the gate driver, a switching signal (e.g., CKV in the embodiment of the present invention) to indicate switching of a gate line to be selected, and an output enable signal for each row to, when a gate line is selected by the gate driver, indicate duration during which the gate line is kept at the selected-period potential, and which feeds to the source driver, a source line potential setting indication signal (e.g., LP) to indicate that potentials of the respective source lines are to be set to potentials according to image data of respective pixels for one row, and a polarity control signal (e.g., POL₂ in the embodiment of the present invention) to make the polarities of the pixels in each column switched every row; the control means operates as follows: the control means feeds a signal changed to a first level and a second level in a predetermined period, as the switching signal to the gate driver; the control means raises the source line potential setting indication signal at timing when the switching sig-

nal is changed to the first level, defines a period of the source line potential setting indication signal to be the same period as the period of the switching signal, and feeds to the gate driver, the output enable signal to indicate as the duration during which the one gate line selected by the gate driver is kept at the selected-period potential, duration of H-s from a change of a level of the switching signal to the first level when H represents the period of the switching signal, t represents the first predetermined time, and s represents a second predetermined time, and the output enable signal to indicate as the duration during which the subsequent gate line to the one gate line is kept at the selected-period potential, duration from a point of time when t has elapsed since the change of the level of the switching signal to the first level, to a point of time when H-s has elapsed since the change of the level to the switching signal to the first level; the gate driver operates as follows: the gate driver switches the one gate line and the subsequent gate line selected, every switching of the switching signal to the first level, and sets the selected gate line and subsequent gate line to the selected-period potential in accordance with the output enable signal; and the source driver sets the potentials of the respective source lines to potentials according to image data of respective pixels for one row in synchronism with a falling edge of the source line potential setting indication signal.

[0030] In the drive device for liquid crystal display device according to the present invention, the first predetermined time is preferably a time that is at least the sum of a time needed to change the potentials of the source lines from a minimum to a maximum of set potentials for the source lines, and a time needed to change the source line potential setting indication signal to a high level.

ADVANTAGEOUS EFFECTS OF INVENTION

[0031] The present invention enables achievement of the two-line dot inversion drive with less power consumption. The present invention also enables achievement of the one-line dot inversion drive with less power consumption.

BRIEF DESCRIPTION OF DRAWINGS

[0032]

Fig. 1 is an explanatory drawing showing a configuration example of the drive device for liquid crystal display device according to an example being helpful to understand the present invention.

Fig. 2 is an explanatory drawing showing changes of POL₁ and POL₂ in the example of Fig. 1.

Fig. 3 is a timing chart showing input timing of each of STH and CLK to a source driver 4 in the beginning of a frame in the example of Fig. 1.

Fig. 4 is a timing chart showing STV and CKV input to a gate driver, an operation of the gate driver 3,

and others in the example of Fig. 1.

Fig. 5 is a timing chart showing potential changes in pixel electrodes and others in the example of Fig. 1.

Fig. 6 is an explanatory drawing showing a method of determining a predetermined duration in the example of Fig. 1.

Fig. 7 is an explanatory drawing showing a configuration example of the drive device for liquid crystal display device according to an embodiment of the invention.

Fig. 8 is a timing chart showing an example of operation according to the embodiment of the present invention.

Fig. 9 is an explanatory drawing showing a connection example of a pixel electrode, a TFT, a source line, and a gate line in the embodiment of the present invention.

Fig. 10 is a schematic drawing showing an example of polarities of respective pixels in the two-line dot inversion drive.

Fig. 11 is a timing chart showing an example of potential changes in gate lines and a source line in the line dot inversion drive

Fig. 12 is a schematic drawing showing an example of polarities of respective pixels in the one-line dot inversion drive.

Fig. 13 is a timing chart showing an example of potential changes in gate lines and a source line in a case where the double gate method is adopted in the one-line dot inversion drive.

DESCRIPTION OF AN EXAMPLE AND AN EMBODIMENT OF THE INVENTION

[0033] An example, which is helpful to understand the present invention, and an embodiment of the present invention will be described below with reference to the drawings.

[Example]

[0034] Fig. 1 is an explanatory drawing showing a configuration example of the drive device for liquid crystal display device according to an example being helpful to understand the invention. The drive device 1 of the present example drives a liquid crystal display device 7 of the active matrix system using TFTs.

[0035] The liquid crystal display device 7, as exemplified in Fig. 9, is provided with a common electrode 30 and pixel electrodes 21 arranged for respective pixels. Fig. 9 shows one pixel electrode, but the liquid crystal display device 7 is provided with a plurality of pixel electrodes 21 arranged in a matrix pattern. Furthermore, the liquid crystal display device 7 is provided with a plurality of source lines arranged along columns of the plurality of pixel electrodes 21 arranged in the matrix pattern and a plurality of gate lines arranged along rows of the plurality of pixel electrodes 21. An example will be described

herein using a case where the source lines are arranged for the respective columns of the pixel electrodes and where the gate lines are arranged for the respective rows of the pixel electrodes. Namely, the example to be explained is a case where the source lines and the respective columns are in one-to-one correspondence and where the gate lines and the respective rows are in one-to-one correspondence.

[0036] The liquid crystal display device 7 is also provided with a TFT 22 for each individual pixel electrode, as exemplified in Fig. 9. Therefore, combinations, each of which includes a TFT 22 and a pixel electrode 21, are arranged in the matrix pattern. Then, the gate 22_a of each individual TFT 21 is connected to a gate line corresponding to a row in which the TFT is arranged. The drain 22_b of each individual TFT 21 is connected to a pixel electrode corresponding to the TFT. The source 22_c of each individual TFT 21 is connected to a source line corresponding to a column in which the TFT is arranged.

[0037] The drive device 1 is provided with a timing controller 2, a gate driver 3, a source driver 4, and a common electrode potential setting circuit 5. It is noted that an illustration of a power generating circuit for liquid crystal is omitted.

[0038] The common electrode potential setting circuit 5 sets a potential of the common electrode of the liquid crystal display device 7 to a predetermined potential V_{COM} .

[0039] The gate driver 3 operates in accordance with the timing controller 2 to perform scanning of the gate lines while selecting each gate line, to set the potential of a selected gate line to a selected-period potential V_{GH} and to set the potential of nonselected gate lines to a nonselected-period potential V_{GL} . A period during which the potential of the gate line is set at the selected-period potential V_{GH} will be referred to as a selected-period potential set period.

[0040] After a lapse of a predetermined time since a start of the selected-period potential set period for a gate line of an odd-numbered row, the gate driver 3 starts the selected-period potential set period for a gate line of an even-numbered row immediately subsequent to the foregoing row. This predetermined time will be represented by t . The time t is shorter than the selected-period potential set period for the gate line of the odd-numbered row. Therefore, before an end of the selected-period potential set period for the gate line of the odd-numbered row, the selected-period potential set period for the gate line of the subsequent row is started, and thus the selected-period potential set periods for the odd-numbered row and the subsequent row overlap in part.

[0041] The gate driver 3 ends the selected-period potential set period for the gate line of the even-numbered row and then starts the selected-period potential set period for a gate line of an odd-numbered row immediately subsequent to the foregoing row. Therefore, there is no overlap of the selected-period potential set periods between the even-numbered row and the subsequent row.

[0042] The gate driver 3 includes a potential output unit 31 and an output control unit 32.

[0043] The potential output unit 31 has potential output terminals corresponding to the respective gate lines. When k represents an integer of at least 1, a set is defined as a couple of two potential output terminals corresponding to a $(2k-1)$ -th gate line and a $(2k)$ -th gate line and the selected-period potential VGH is sequentially output from each set of two potential output terminals. The nonselected-period potential VGL is output from the potential output terminals other than those outputting the selected-period potential VGH. That the potential output unit 31 outputs VGH from a set of two potential output terminals means that the gate driver 3 selects the gate lines corresponding to the two potential output terminals (the gate line of the odd-numbered row and the gate line of the subsequent even-numbered row). The timing controller 2 feeds a control signal (gate start pulses, which will be represented by STV) to indicate sequential selection of the gate lines, to the potential output unit 31. In the present example, STV is used to instruct the potential output unit 31 to sequentially output the selected-period potential VGH starting from the first set of potential output terminals (i.e., a set of potentials output terminals corresponding to the gate lines of the first row and the second row). The potential output unit 31 outputs the selected-period potential VGH for each set of potential output terminals, sequentially from the first set of potential output terminals, according to STV and below-described CKV. The timing controller 2 feeds a control signal (gate shift clocks, which will be represented by CKV) to indicate switching of selected gate lines, to the potential output unit 31. In the present example, CKV is used to instruct the potential output unit 31 to switch the set of potential output terminals to output the selected-period potential VGH, to the next set. The potential output unit 31 switches the set of potential output terminals to output the selected-period potential VGH, to the next set, according to CKV input from the timing controller 2.

[0044] The output control unit 32 has potential input terminals and potential output terminals corresponding to the respective gate lines. The potentials output from the potential output unit 31 are input to the respective potential input terminals of the output control unit 32. Therefore, the selected-period potential VGH from the potential output unit 31 is sequentially input to each set of odd-numbered and subsequent even-numbered potential input terminals, starting from the set of potential input terminals corresponding to the gate lines of the first row and the second row. The nonselected-period potential VGL from the potential output unit 31 is input to the potential input terminals to which the selected-period potential VGH is not input.

[0045] The potential output terminals of the output control unit 32 are connected to the corresponding gate lines, respectively. The output control unit 32 outputs the selected-period potential VGH, according to output enable signals input from the timing controller 2, from the poten-

tial output terminals (potential output terminals of the output control unit 32) corresponding to two potential input terminals to which the selected-period potential VGH is input from the potential output unit 31. The output control unit 32 receives the output enable signal to define a potential output from the odd-numbered $((2k-1)$ -th) potential output terminal from the first (which will be denoted by OE_{odd}) and the output enable signal to define a potential output from the even-numbered $(2k)$ -th potential output terminal from the first (which will be denoted by OE_{even}), out of the two potential output terminals corresponding to the two potential input terminals to which the selected-period potential VGH is input. With OE_{odd} being at a high level, the output control unit 32 outputs VGH from the odd-numbered potential output terminal from the first, out of the two potential output terminals corresponding to the two potential input terminals to which the selected-period potential VGH is input. Similarly, with OE_{even} being at a high level, it outputs VGH from the even-numbered potential output terminal from the first, out of the two potential output terminals corresponding to the two potential input terminals to which the selected-period potential VGH is input. For example, let us assume that the selected-period potential VGH is input from the potential output unit 31 to the first and second potential input terminals. Then, the output control unit 32 outputs the selected-period potential VGH from the first potential output terminal for duration during which OE_{odd} is at the high level. It also outputs the selected-period potential VGH from the second potential output terminal for duration during which OE_{even} is at the high level.

[0046] The output control unit 32 outputs the nonselected-period potential VGL from the potential output terminals other than the potential output terminals outputting the selected-period potential VGH. Since the potential output terminals of the output control unit 32 are connected to the respective corresponding gate lines, each gate line is set at the output potential of the corresponding potential output terminal of the output control unit 32.

[0047] The potential output terminal of the potential output unit 31 corresponding to an arbitrary n -th gate line will be denoted by O_n' . The potential output terminal of the output control unit 32 corresponding to an arbitrary n -th gate line will be denoted by O_n .

[0048] The source driver 4 has potential output terminals corresponding to the respective source lines. The source driver 4 reads image data in accordance with control of the timing controller 2. Then the source driver 4 sets potentials of the respective source lines connected to the respective potential output terminals, to potentials according to image data of pixels in a row corresponding to a selected gate line. Specifically, the timing controller 2 feeds to the source driver 4, a control signal to indicate a start of read of image data for one row (source start pulse, which will be denoted by STH), a clock signal to indicate read of image data of one pixel in one row (dot clock, which will be denoted by CLK), and LP (latch pulse) to indicate output of potentials according to already-read

image data. The periods of STH and LP are half of the period of CKV and, when detecting a falling edge of LP, the source driver 4 sets the potentials of the respective source lines of the liquid crystal display device 7 to potentials according to the read image data. It is, however, noted that an example described below is a case where the source driver 4 keeps each potential output terminal in a high impedance state, for duration during which LP is at a high level.

[0049] The timing controller 2 feeds to the source driver 4, two types of control signals (which will be denoted by POL_1 and POL_2) for defining polarities of the respective pixels. Fig. 2 is an explanatory drawing showing changes in POL_1 and POL_2 . The timing controller 2 alternately switches POL_1 between a high level and a low level, frame by frame (see Fig. 2). The timing controller 2 also changes POL_2 in the period of twice the period of CKV. In the example, the period of CKV will be defined below as 2H. Therefore, the period of POL_2 is 4H. Then the timing controller 2 alternately switches the level of POL_2 between a high level and a low level at intervals of 2H. The timing controller 2 changes POL_2 so that POL_2 turns to the high level at the first falling edge of LP in a frame.

[0050] When POL_1 and POL_2 both are at the high level, the source driver 4 sets the odd-numbered source lines to potentials higher than the common electrode potential V_{COM} and sets the even-numbered source lines to potentials lower than the common electrode potential V_{COM} .

[0051] When POL_1 is at the high level and POL_2 is at the low level, the source driver 4 sets the odd-numbered source lines to potentials lower than the common electrode potential V_{COM} and sets the even-numbered source lines to potentials higher than the common electrode potential V_{COM} .

[0052] When POL_1 is at the low level and POL_2 is at the high level, the source driver 4 sets the odd-numbered source lines to potentials lower than the common electrode potential V_{COM} and sets the even-numbered source lines to potentials higher than the common electrode potential V_{COM} .

[0053] When POL_1 and POL_2 both are at the low level, the source driver 4 sets the odd-numbered source lines to potentials higher than the common electrode potential V_{COM} and sets the even-numbered source lines to potentials lower than the common electrode potential V_{COM} .

[0054] 2H is twice the period of LP. Therefore, in each frame, the polarities of the pixels in each column are switched every two rows. Since the polarities in the odd-numbered columns are always different from those in the even-numbered columns, the two-line dot inversion drive is carried out in the present example. For duration during (which POL_1 is at the high level, the polarities of the respective pixels are the same as those of the respective pixels shown in Fig. 10. For duration during which POL_1 is at the low level, the polarities of the respective pixels are opposite to those of the respective pixels shown in Fig. 10.

[0055] The timing controller 2 feeds STV and CKV to

the potential output unit 31 of the gate driver 3 and feeds OE_{odd} and OE_{even} to the output control unit 32 of the gate driver 3. Furthermore, the timing controller 2 feeds STH, CLK, LP, POL_1 , and POL_2 to the source driver 4. Concerning POL_1 and POL_2 , the timing controller 2 may feed only POL to the source driver 4. Namely, the timing controller 2 may feed one signal (denoted by POL) as a signal for controlling the polarities, to the source driver 4. In this case, the timing controller 2 can be configured to feed a signal indicative of Exclusive OR (XOR) of POL_1 and POL_2 described above, as POL to the source driver 4.

[0056] An operation will be described below.

[0057] Fig. 3 is a timing chart showing input timing of each of STH and CLK to the source driver 4 in the beginning of a frame. In the beginning of the frame, the timing controller 2 changes STH to the high level. At this time, the timing controller 2 keeps LP at the low level and also keeps each of the signals STV, CKV, OE_{odd} , and OE_{even} (not shown in Fig. 3) to be input to the gate driver 3, at the low level.

[0058] The timing controller 2 alternately changes CLK between the high level and the low level on a periodic basis. However, it changes CLK so as to place a rising edge of CLK in duration during which STH is at the high level. The timing controller 2 turns STH to the high level, then turns CLK to the high level in duration of STH at the high level, and turns STH to the low level. When detecting a rising edge of CLK in the duration of STH at the high level, the source driver 4 reads and retains image data for one pixel at every detection of a rising edge of CLK, starting from the next rising edge of CLK (see Fig. 3).

[0059] The timing controller 2 raises STH to the high level in the period of half of CKV (not shown in Fig. 3). Then the timing controller 2 feeds the image data for one row to the source driver 4 in each duration from a falling edge to a rising edge of STH. In the beginning of a frame, the timing controller 2 feeds the image data of the first row to the source driver 4. The source driver 4 reads and retains the image data input from the timing controller 2, pixel by pixel, at every rising edge of CLK.

[0060] When first turning CKV to the high level in the frame, the timing controller 2 changes LP to the high level and then changes LP back to the low level. Thereafter, the timing controller 2 raises LP to the high level in the period of half of CKV. Moreover, the timing controller 2 matches the timing of each rising edge of LP with a level switching timing of CKV. When detecting a falling edge of LP, the source driver 4 sets potentials of the respective source lines of the liquid crystal display device 7, to potentials according to the retained image data of the respective pixels in one row.

[0061] Therefore, in one frame, as shown in Fig. 3, the source driver 4 reads and retains the image data of the first row in duration from the first rising edge of STH to the falling edge of STH, and sets the potentials of the respective source lines to potentials according to the image data of the respective pixels in the first row, at the first falling edge of LP in the frame. An example to be

described below is a case where POL_1 is at the high level and the polarities of the respective pixels are set as shown in Fig. 10.

[0062] Thereafter, in the same manner as above, the source driver 4 periodically repeats the operation of reading the image data for one row and setting the potentials of the respective source lines to potentials according to the image data, in accordance with STH , CLK , and LP .

[0063] Fig. 4 is a timing chart showing STV and CKV input to the gate driver, the operation of the gate driver 3, and others. Fig. 5 is a timing chart showing changes in potentials of the pixel electrodes and others.

[0064] The timing controller 2 changes STV to the high level at a start of sequential selection from the gate line of the first row, changes CKV to the high level in duration of STV at the high level, and thereafter changes STV to the low level (see Fig. 4). The timing controller 2 turns LP to be input to the source driver 4, to the high level in synchronism with this rising edge of CKV (see Fig. 4). It is, however, noted that the controller may turn LP to the high level with a delay of several ten to several hundred pulses of CLK , without synchronism with the rising edge of CKV .

[0065] The period of CKV is $2H$; when duration H has elapsed since the rising edge of CKV , the timing controller 2 changes CKV to the low level; when another duration H has elapsed, it again changes CKV to the high level. Thereafter, the timing controller 2 changes CKV in the same manner.

[0066] When detecting the rising edge of CKV in the duration of STV at the high level, the potential output unit 31 (see Fig. 1) of the gate driver 3 outputs the selected-period potential VGH from the potential output terminals O_1' , O_2' corresponding to the gate lines of the first row and the second row (see Fig. 4) and outputs the nonselected-period potential VGL from each of the other potential output terminals. Thereafter, the potential output unit 31 switches the set of potential output terminals outputting the selected-period potential VGH , at every rising edge of CKV (in other words, in the period of $2H$), to output the selected-period potential VGH from the potential output terminal O_{2k-1}' corresponding to an odd-numbered row and the potential output terminal O_{2k}' corresponding to an even-numbered row. Furthermore, it outputs the nonselected-period potential VGL from each of the other potential output terminals.

[0067] The timing controller 2 raises OE_{odd} to the high level at the same timing as the rising edge of CKV . Furthermore, it raises OE_{even} to the high level when a predetermined time t has elapsed since the rising edge of OE_{odd} . It changes OE_{odd} to the low level when duration H -s has elapsed since the rising edge of OE_{odd} . Then it turns OE_{even} to the low level when duration $2H$ -s has elapsed since the rising edge of OE_{odd} . The timing controller 2 changes OE_{odd} and OE_{even} in this manner at every rise of CKV to the high level. The lengths of the times t and s are determined in advance.

[0068] The output control unit 32 outputs the selected-

period potential VGH from the potential output terminal O_1 corresponding to the gate line of the first row for duration during which the selected-period potential VGH is input from the potential output terminals O_1' , O_2' of the electron output unit 31 and during which OE_{odd} is at the high level, to set the potential of the gate line G_1 of the first row to VGH . Namely, the output control unit 32 sets the potential of the gate line G_1 at VGH for the duration of H -s from the rising edge of OE_{odd} (see Fig. 4).

[0069] The output control unit 32 outputs the selected-period potential VGH from the potential output terminal O_2 corresponding to the gate line of the second row for a duration during which the selected-period potential VGH is input from the potential output terminals O_1' , O_2' of the electron output unit 31 and during which OE_{even} is at the high level, to set the potential of the gate line G_2 of the second row to VGH . Namely, the output control unit 32 sets the potential of the gate line G_2 at VGH for the duration from a point of time when the predetermined time t has elapsed since the rising edge of OE_{odd} to a point of time when $2H$ -s has elapsed since the rising edge of OE_{odd} (see Fig. 4).

[0070] When detecting the first falling edge of LP after the start of the frame, the source driver 4 sets the potentials of the respective source lines to the potentials according to the respective pixels in the first row. Fig. 5 shows potentials of the potential output terminal of the source driver 4 corresponding to the first source line S_1 from the left, and potential changes in the pixel electrodes in the first row and the second row in the first column from the left.

[0071] At the first falling edge of LP after the frame start, POL_2 is at the high level. It is assumed that in this frame POL_1 is also at the high level. Therefore, when detecting the first falling edge of LP after the frame start, the source driver 4 sets the potentials of the odd-numbered source lines from the left, such as the source line S_1 , to potentials higher than V_{COM} (see Fig. 5). The source driver 4 also sets the potentials of the even-numbered source lines from the left to potentials lower than V_{COM} .

[0072] Describing an example of the pixel electrodes in the first row and the second row in the first column from the left, these two pixel electrodes are set at a potential (0 V in the example shown in Fig. 5) lower than V_{COM} in the preceding frame. It is assumed in this example that $0\text{ V} < V_{COM} < V_{max}$, that 0 V is a potential corresponding to the maximum gray level in the negative polarity, and that V_{max} is a potential corresponding to the maximum gray level in the positive polarity. Furthermore, $V_{max} - V_{COM} = V_{COM} - 0$. When the source driver 4 sets the potential of the source line S_1 to a potential higher than V_{COM} , since the output control unit 32 has set the gate line G_1 of the first row to the selected-period potential VGH , the pixel electrode in the first row in the first column from the left is changed to the potential equal to that of the source line S_1 (see Fig. 5). Then, it becomes equipotential to the source line S_1 before the predetermined

time t has elapsed from the rising edge of OE_{odd} . When H -s has elapsed since the rising edge of OE_{odd} , the potential of the gate line G_1 is switched to the nonselected-period potential V_{GL} ; however, the pixel electrode in the first row in the first column maintains the potential at that point.

[0073] Furthermore, when the predetermined time t has elapsed since the output of the selected-period potential V_{GH} from the potential output terminal O_1 , the output control unit 32 outputs the selected-period potential V_{GH} from the potential output terminal O_2 to set the potential of the gate line G_2 in the second row to V_{GH} . As a consequence of this, the pixel electrode in the second row in the first column from the left also changes so as to approach the potential of the source line S_1 (see Fig. 5). However, since each source line is changed into the high impedance state with a change of LP to the high level, the potential change stops.

[0074] When detecting the next falling edge of LP , the source driver 4 sets the potentials of the respective source lines to potentials according to the image data of the respective pixels in the second row. Since at this time POL_2 is also at the high level, the source driver 4 sets the potentials of the odd-numbered source lines from the left, such as the source line S_1 , to potentials higher than V_{COM} (see Fig. 5). The source driver 4 also sets the potentials of the even-numbered source lines from the left to potentials lower than V_{COM} .

[0075] At this time, the output control unit 32 is outputting the selected-period potential V_{GH} from the potential output terminal O_2 and the potential of the gate line G_2 of the second row is V_{GH} . Therefore, the pixel electrode in the second row in the first column from the left varies to the potential of the source line S_2 , so as to become equipotential to the source line S_2 .

[0076] In this frame, the pixel electrodes in the first row and in the second row in the first column from the left are set both to the potentials in the positive polarity (i.e., the potentials higher than V_{COM}). Furthermore, the pixel electrode in the second row in the first column from the left starts changing toward the potential higher than V_{COM} , prior to the second falling edge of LP after the frame start. This means that the pixel in the second row in the first column from the left is subjected to precharge. This example described the example of the first column from the left but the precharge is also performed in the same manner for the pixel in the second row in each of the other odd-numbered columns from the left. In each of the even-numbered columns from the left, the pixel electrode in the second row is set at a potential lower than V_{COM} and starts changing toward the potential lower than V_{COM} , prior to the second falling edge of LP after the frame start. This means that the precharge is also performed for the pixel in the second row in each of the even-numbered columns.

[0077] Thereafter, the operation of the gate driver 3 (the potential output unit 31 and the output control unit 32) with change of CKV to the high level is the same as

the above operation, except for switching of the gate lines to be set at the selected-period potential V_{GH} . Therefore, the precharge is also performed for the pixels in the even-numbered rows, out of the pixels in each of the third and subsequent rows.

[0078] Since the present example involves execution of the precharge for each pixel in the even-numbered rows in this manner, it can reduce power consumption.

[0079] In the present example, the duration P (see Fig. 4) from the point of time when the predetermined time t has elapsed from the rising edge of OE_{odd} to the next rising edge of LP is set to be the duration of execution of the precharge. Therefore, the entire selected-period potential set period of the odd-numbered gate line is not used as the duration of execution of the precharge, which enhances the effect of a reduction in power consumption.

[0080] Namely, the present example can realize the two-line dot inversion drive with less power consumption.

[0081] How to determine the predetermined duration t will be described below. Fig. 6 is an explanatory drawing showing a method of determining the predetermined duration t . A time needed to change a potential of a source line from the minimum to the maximum of set potentials for the source lines is defined as R . A time needed to change a potential of a source line from the maximum to the minimum of set potentials for the source lines is also R . The minimum of the set potentials for the source lines is the potential corresponding to the maximum gray level in the negative polarity and, in the present example, it is 0 V. The maximum of the set potentials for the source lines is the potential corresponding to the maximum gray level in the positive polarity and, in the present example, it is V_{MAX} . In the present example, therefore, R may be determined to be a time necessary for a change of the potential of the source line from 0 V to V_{MAX} . The predetermined time t may be determined to be at least a value obtained by adding a duration Q of LP at the high level to R . Namely, t can be determined to satisfy $t \geq Q+R$. LP is changed to the high level in synchronism with the rising edge of OE_{odd} and from the falling edge of LP , the source lines are set to potentials according to image data. Therefore, when t is determined to satisfy $t \geq Q+R$, the potential of each source line can be changed from any potential in the negative polarity to any desired potential in the positive polarity within the predetermined time t . Likewise, the potential of each source line can be changed from any potential in the positive polarity to any desired potentials in the negative polarity within the predetermined time t .

[Embodiment of the present invention]

[0082] According to an embodiment of the present invention, explanation will be made of a drive device that realizes the one-line dot inversion drive. Fig. 7 is an explanatory drawing showing a configuration example of the drive device for liquid crystal display device according to the embodiment of the present invention. The same

elements as those in the previously described example will be denoted by the same reference signs as in Fig. 1, while omitting the description thereof.

[0083] The liquid crystal display device 7 is the same as the liquid crystal display device 7 according to the previously described example.

[0084] The drive device 1_a according to the present embodiment is provided with a timing controller 2_a, a gate driver 3_a, a source driver 4, and a common electrode potential setting circuit 5.

[0085] The timing controller 2_a feeds STH, CLK, LP, POL₁, and POL₂ to the source driver 4. In the present embodiment, however, the periods of STH, LP, and POL₂ are the same as the period of CKV input from the timing controller 2_a to the gate driver 3_a. In the present embodiment, the periods of CKV, STH, LP, and POL₂ will be defined below as H. The operation of the source driver 4 in accordance with STH, CLK, LP, POL₁, and POL₂ is the same as in the previously described example. Concerning POL₁ and POL₂, the timing controller 2_a may feed only POL to the source driver 4. Namely, the timing controller 2_a may feed one signal (POL) as a signal for controlling the polarities, to the source driver 4. In this case, the timing controller 2_a can feed a signal indicative of Exclusive OR (XOR) of POL₁ and POL₂ described above, as POL to the source driver 4.

[0086] When selecting a gate line of an odd-numbered row, the gate driver 3_a also selects a gate line of the next odd-numbered row. However, the gate driver 3_a first sets the first gate line to the selected-period potential VGH, out of the two gate lines, and when the predetermined time t has elapsed, the gate driver 3_a sets the second gate line to the selected-period potential VGH. Then, after completion of selection of the gate lines of the two odd-numbered rows, the gate driver 3_a selects gate lines of even-numbered rows. The predetermined time t may be determined in the same manner as in the previously described example.

[0087] Similarly, when selecting a gate line of an even-numbered row, the gate driver 3_a also selects a gate line of the next even-numbered row. However, the gate driver 3_a first sets the first gate line to the selected-period potential VGH, out of the two gate lines, and when the predetermined time t has elapsed, the gate driver 3_a sets the second gate line to the selected-period potential VGH. After completion of selection of the gate lines of the two even-numbered rows, the gate driver 3_a selects gate lines of odd-numbered rows.

[0088] In the embodiment according to the present invention, therefore, there is an overlap of the selected-period potential set periods between gate lines of odd-numbered rows or between gate lines of even-numbered rows, but there is no overlap of the selected-period potential set periods between odd-numbered and even-numbered rows.

[0089] The gate driver 3_a has a potential output unit 31_a and an output control unit 32_a. The potential output unit 31_a has potential output terminals corresponding to

the respective gate lines. Furthermore, the output control unit 32_a has potential input terminals and potential output terminals corresponding to the respective gate lines. The potentials output from the corresponding potential output terminals of the potential output unit 31_a are input to the potential input terminals of the output control unit 32_a. As in the previously described example, the potential output terminals of the potential output unit 31_a will be denoted by O_n', and the potential output terminals of the output control unit 32_a will be denoted by O_n.

[0090] When detecting a rising edge of CKV in a duration during which STV input from the timing controller 2_a is at the high level, the potential output unit 31_a outputs the selected-period potential VGH from the first potential output terminal. Then the potential output unit 31_a shifts the potential output terminal to output the selected-period potential VGH, by one at every detection of a rising edge of CKV. As described below, the timing controller 2_a turns STV to the high level twice in the beginning of a frame. Time duration between the two rising edges of STV is twice the period (H) of CKV. Therefore, the potential output unit 31_a starts the operation of outputting the selected-period potential VGH in order from the first potential output terminal, and thereafter, in synchronism with the operation, it again outputs the selected-period potential VGH in order from the first potential output terminal. Therefore, the potential output unit 31_a outputs the selected-period potential VGH from two potential output terminals and sequentially shifts the potentials output terminals to output VGH. Specifically, the potential output unit 31_a outputs VGH from the potential output terminals O₁', O₃', then outputs VGH from the potential output terminals O₂', O₄', and thereafter sequentially shifts the potential output terminals to output VGH, in the same manner.

[0091] The potential output unit 31_a outputs the non-selected-period potential VGL from the potential output terminals not to output VGH.

[0092] The output control unit 32_a outputs the selected-period potential VGH in accordance with an output enable signal input from the timing controller 2_a, starting from the potential output terminals (potential output terminals of the output control unit 32_a) corresponding to two potential input terminals to which the selected-period potential VGH is input from the potential output unit 31_a. In the present embodiment, the timing controller 2_a feeds to the output control unit 32_a, the output enable signal corresponding to each potential output terminal of the output control unit 32_a. The output enable signal corresponding to the n-th potential output terminal will be denoted by OE_n.

[0093] When VGH from the potential output unit 31_a is input to two odd-numbered potential input terminals, the output control unit 32_a outputs VGH for duration during which the output enable signal corresponding to each potential output terminal is at the high level, from two potential output terminals corresponding to the two potential input terminals. For example, in a case where VGH

is input from the potential output unit 31_a to the (2j+1)-th and (2j+3)-th potential input terminals, VGH is output for duration of OE_{2j+1} at the high level from the (2j+1)-th potential output terminal. VGH is output for duration of OE_{2j+3} at the high level from the (2j+3)-th potential output terminal. It is noted that j is an integer of at least 0.

[0094] When VGH from the potential output unit 31_a is input to two even-numbered potential input terminals, the output control unit 32_a outputs VGH for duration during which the output enable signal corresponding to each potential output terminal is at the high level, from two potential output terminals corresponding to the two potential input terminals. For example, in a case where VGH is input from the potential output unit 31_a to the (2j+2)-th and (2j+4)-th potential input terminals, VGH is output for duration of OE_{2j+2} at the high level from the (2j+2)-th potential output terminal. VGH is output for a duration of OE_{2j+4} at the high level from the (2j+4)-th potential output terminal.

[0095] The timing controller 2_a feeds STV and CKV to the potential output unit 31_a. In the present embodiment, as described above, the period of CKV is set to H. In the beginning of a frame, STV is changed to the high level and then back to the low level, and thereafter, when 2H has elapsed since a rising edge thereof, STV is again changed to the high level and back to the low level. Then it controls CKV so that one rising edge of CKV appears in duration during which STV is at the high level.

[0096] The timing controller 2_a feeds each output enable signal to the output control unit 32_a. The output enable signal OE_n corresponding to the n-th potential output terminal is controlled as follows. Namely, the timing controller 2_a changes OE_n to the high level at a point of time when the predetermined time t has elapsed since the rising edge of CKV to output VGH from the (n-2)-th potential output part in the potential output unit 31_a, and changes OE_n to the low level at a point of time when H-s has elapsed since the rising edge of CKV. Furthermore, it changes OE_n to the high level at the rising edge of CKV to output VGH from the (n)-th potential output part in the potential output unit 31_a, and changes OE_n to the low level at a point of time when H-s has elapsed since the rising edge of CKV. The length of the time s may be determined in advance.

[0097] However, concerning OE₁ corresponding to the first potential output terminal, OE₁ may be controlled to be changed to the high level at the rising edge of CKV to output VGH from the first potential output part in the potential output unit 31_a and then to the low level at a point of time when H-s has elapsed since the rising edge of CKV. Concerning OE₂ corresponding to the second potential output terminal, OE₂ may be controlled to be changed to the high level at the rising edge of CKV to output VGH from the second potential output part in the potential output unit 31_a and then to the low level at a point of time when H-s has elapsed since the rising edge of CKV.

[0098] The timing controller 2_a feeds STH, CLK, LP,

POL₁, and POL₂ to the source driver 4. As described previously, the periods of STH, LP, and POL₂ are the same as the period H of CKV.

[0099] Next, an operation will be described.

[0100] Fig. 8 is a timing chart showing an example of operation in the embodiment of the present invention. The timing controller 2_a changes STV to the high level in the beginning of a frame, changes CKV to the high level in duration of STV at the high level, and then changes STV back to the low level. The timing controller 2_a alternately switches the level of CKV between the high level and the low level at every lapse of a time of H/2 (see Fig. 8). As a consequence of this, the period of CKV becomes H. At this time, the timing controller 2_a maintains each OE_n at the low level.

[0101] When detecting a rising edge of CKV in duration of STV at the high level, the potential output unit 31_a outputs the selected-period potential VGH from the first potential output terminal O₁' and thereafter, switches the potential output terminal to output VGH, at every detection of a rising edge of CKV.

[0102] At this time, since each output enable signal is at the low level, the output potential of each potential output terminal of the output control unit 32_a is VGL.

[0103] When 2H (twice the period of CKV) has elapsed since the first rising edge of STV in the frame, the timing controller 2_a again changes STV to the high level and then back to the low level. At this time, the timing controller 2_a also changes CKV to the high level in the duration of STV at the high level (see Fig. 8). Therefore, the potential output unit 31_a again detects a rising edge of CKV in the duration of STV at the high level. For this reason, the potential output unit 31_a outputs the selected-period potential VGH from the first potential output terminal O₁' and thereafter switches the potential output terminal to output VGH, at every detection of a rising edge of CKV. Namely, the potential output unit 31_a outputs the potential VGH from the potential output terminals O₁' and O₃' and, when detecting a rising edge of CKV, it outputs the potential VGH from the potential output terminals O₂' and O₄'. Furthermore, when detecting a rising edge of CKV, it outputs the potential VGH from the potential output terminals O₃' and O₅'. In this manner, the potential output unit 31_a sequentially switches the potential output terminals to output VGH.

[0104] The timing controller 2_a changes OE₁ corresponding to the first potential output terminal O₁ of the output control unit 32_a to the high level in synchronism with a rising edge of CKV in the second duration of STV at the high level. Furthermore, the timing controller 2_a changes OE₃ corresponding to the third potential output terminal O₃ of the output control unit 32_a when the predetermined time t has elapsed since the rising edge of CKV. Then the timing controller 2_a changes OE₁ and OE₂ to the low level when the time H-s has elapsed since the rising edge of CKV.

[0105] Therefore, the output control unit 32_a outputs VGH from the potential output terminal O₁ to keep the

potential of the first-row gate line G_1 at VGH during the time H-s from the rising edge of CKV in the second duration of STV at the high level.

[0106] The timing controller 2_a changes LP to the high level in synchronism with the rising edge of CKV and then changes LP back to the low level. Up to this point, LP is maintained at the low level. The timing controller 2_a may output STH so that the source driver 4 can complete read of the image data for the first row before the first rising edge of LP. The operation for the source driver 4 to read the image data in synchronism with STH and CLK is the same as in the previously described example. It is also possible to change LP to the high level with a delay of several ten to several hundred pulses of CLK, without synchronism with the rising edge of CKV.

[0107] The source driver 4 sets the potentials of the respective source lines to potentials according to the image data of the respective pixels in the first row, at the first falling edge of LP. At this time, since the potential of the first-row gate line G_1 is VGH, each pixel electrode in the first row changes so as to become equipotential to the source line of the corresponding column.

[0108] It is assumed that in this frame POL_1 is at the high level and POL_2 also has been changed to the high level at the first falling edge of LP. Therefore, the source driver 4 sets the odd-numbered source lines to potentials higher than the common electrode potential V_{COM} and sets the even-numbered source lines to potentials lower than the common electrode potential V_{COM} . Accordingly, among the pixel electrodes in the first row, the pixel electrodes in the odd-numbered columns are changed to the potentials higher than V_{COM} and the pixel electrodes in the even-numbered columns are changed to the potentials lower than V_{COM} .

[0109] Since each pixel electrode is set at a potential in the opposite polarity to that in the preceding frame, the potential is changed across V_{COM} . Since the predetermined time t is defined as the same as in the previously described example, each pixel electrode in the first row becomes equipotential to the corresponding source line before the predetermined time t has elapsed from the rising edge of CKV.

[0110] As described previously, the timing controller 2_a changes OE_3 to the high level at the point of time when the predetermined time t has elapsed since the rising edge of CKV. Then the output control unit 32_a also outputs VGH from the potential output terminal O_3 corresponding to the third row, to change the potential of the third-row gate line G_3 to VGH. As a consequence of this, each pixel electrode in the third row also starts changing toward the potential of the corresponding source line. The timing controller 2_a changes OE_3 to the low level when the time of H-s has elapsed since the rising edge of CKV, and the output control unit 32_a stops the output of VGH from the potential output terminals O_1 and O_3 . Therefore, the potential of each pixel electrode in the third row changes up to this point and the change of potential stops at this point.

[0111] In the present embodiment, the period of POL_2 is the same as the period of CKV, and in each column, the pixels in the odd-numbered rows have the same polarity and the pixels in the even-numbered rows also have the same polarity. However, the polarity of the pixels in the odd-numbered rows is opposite to that of the pixels in the even-numbered rows in each column.

[0112] Therefore, each pixel electrode in the third row changes to a potential in the polarity of each pixel in the third row in the present frame in the duration of OE_3 at the high level. Namely, the pixels in the third row are subjected to precharge.

[0113] Subsequently, the potential output unit 31_a switches the potential output terminals to output VGH, from O_1, O_3 to O_2, O_4 , at the next rising edge of CKV. The timing controller 2_a changes OE_2 corresponding to the second potential output terminal O_2 of the output control unit 32_a to the high level, in synchronism with the rising edge of CKV. Furthermore, the timing controller 2_a changes OE_4 corresponding to the fourth potential output terminal O_4 of the output control unit 32_a to the high level when the predetermined time t has elapsed since the rising edge of CKV. Then the timing controller 2_a changes OE_2 and OE_4 to the low level when the time H-s has elapsed since the rising edge of CKV.

[0114] The output control unit 32_a outputs VGH from the potential output terminal O_2 during the time H-s from the rising edge of CKV, to keep the potential of the second-row gate line G_2 at VGH.

[0115] The timing controller 2_a changes LP to the high level in synchronism with the rising edge of CKV and then changes LP back to the low level. The source driver 4 sets the potentials of the respective source lines to potentials according to the image data for the pixels in the second row, at the falling edge of LP. Since the potential of the second-row gate line G_2 is VGH, each pixel electrode in the second row changes to become equipotential to the source line of the corresponding column. Since POL_2 is at the low level at this time, the source driver 4 sets the odd-numbered source lines to potentials lower than the common electrode potential V_{COM} and sets the even-numbered source lines to potentials higher than the common electrode potential V_{COM} . Therefore, among the pixel electrodes in the second row, the pixel electrodes in the odd-numbered columns change to the potentials lower than V_{COM} and the pixel electrodes in the even-numbered columns change to the potentials higher than V_{COM} . As in the case of the pixel electrodes in the first row, the pixel electrodes in the second row change across V_{COM} but each pixel electrode in the second row becomes equipotential to the corresponding source line before the predetermined time t has elapsed since the rising edge of CKV.

[0116] As described previously, the timing controller 2_a changes OE_4 to the low level at the point of time when the predetermined time t has elapsed since the rising edge of CKV. Then the output control unit 32_a also outputs VGH from the potential output terminal O_4 corre-

sponding to the fourth row, to change the potential of the fourth-row gate line G_4 to VGH. As a consequence of this, each pixel electrode in the fourth row also starts changing toward the potential of the corresponding source line. The timing controller 2_a stops the output of VGH from the potential output terminals O_2 and O_4 when the time of H-s has elapsed since the rising edge of CKV. Therefore, the potential of each pixel electrode in the fourth row changes up to this point and the change of potential stops at this point.

[0117] Therefore, each pixel electrode in the fourth row changes to a potential in the polarity of the pixel in the fourth row in the present frame in the duration of OE_4 at the high level. Namely, the pixels in the fourth row are subjected to precharge.

[0118] Furthermore, the potential output unit 31_a switches the potential output terminals to output VGH, from O_2' , O_4' to O_3' , O_5' , at the next rising edge of CKV. The timing controller 2_a changes OE_3 corresponding to the third potential output terminal O_3 of the output control unit 32_a to the high level, in synchronism with the rising edge of CKV. Furthermore, the timing controller 2_a changes OE_5 corresponding to the fifth potential output terminal O_5 of the output control unit 32_a to the high level when the predetermined time t has elapsed since the rising edge of CKV. Then the timing controller 2_a changes OE_3 and OE_5 to the low level when the time H-s has elapsed since the rising edge of CKV.

[0119] The output control unit 32_a outputs VGH from the potential output terminal O_3 during the time H-s from the rising edge of CKV, to keep the potential of the third-row gate line G_3 at VGH.

[0120] The timing controller 2_a changes LP to the high level in synchronism with the rising edge of CKV and then changes LP back to the low level. The source driver 4 sets the potentials of the respective source lines to potentials according to the image data for the respective pixels in the third row, at the falling edge of LP. Since the potential of the third-row gate line G_3 is VGH, each pixel electrode in the third row changes to become equipotential to the source line of the corresponding column. Here, each pixel in the third row has been precharged when the source driver 4 outputs the potentials according to the image data for the first row. Therefore, power consumption needed to make each pixel electrode in the third row equipotential to the source line of each column is reduced.

[0121] As in the case of the precharge for each pixel electrode in the third row, each pixel electrode in the fifth row is subjected to precharge in the duration of OE_5 at the high level.

[0122] The drive device 1_a repeats the same operation in this frame thereafter.

[0123] In the present embodiment, as described above, when the potential of the gate line G_n is changed to VGH by changing OE_n corresponding to the n -th row to the high level at the rising edge of CKV, OE_{n+2} is also changed to the high level to precharge the pixel elec-

trodes in the $(n+2)$ -th row, at the point of time when the time t has elapsed since the rising edge of CKV. Therefore, power consumption can be reduced. In the present embodiment, when OE_n is changed to the high level, OE_{n+2} is set to the high level during a time shorter by t than the duration of OE_n at the high level, which enhances the effect of a reduction in power consumption.

[0124] In this manner, the present embodiment can realize the one-line dot inversion drive with less power consumption.

[0125] The liquid crystal display device 7 driven by the drive device in the foregoing example and embodiment may be a liquid crystal display device of the in-plane switching drive system. The liquid crystal display device of the in-plane switching drive system is also provided with the source lines for respective columns and the gate lines for respective rows.

INDUSTRIAL APPLICABILITY

[0126] The present invention is suitably applied, for example, to driving of TFT liquid crystal display devices and others.

Claims

1. A drive device for a liquid crystal display device (7), the liquid crystal display device including source lines arranged along columns of pixels formed in a matrix pattern and gate lines arranged along rows of the pixels formed in the matrix pattern, the drive device for the liquid crystal display device comprising:

a gate driver (3_a , 31_a , 32_a) which selects a gate line; and

a source driver (4) which switches polarities of the pixels in each column every row and which sets potentials of the respective source lines to potentials according to image data of respective pixels for one row, while making the polarities of the pixels in adjacent columns opposite to each other,

wherein the gate driver selects one gate line (O_1), and a subsequent gate line that is a gate line (O_3) of a row after the next to the one gate line, sets the subsequent gate line to a selected-period potential with a delay of a first predetermined time from timing when the one gate line is set at the selected-period potential, and sets the one gate line and the subsequent gate line to a nonselected-period potential, prior to selection (LP) of the gate line next to the one gate line.

2. The drive device for a liquid crystal display device according to Claim 1, comprising:

control means (2_a) which feeds to the gate driver, a switching signal (CKV) to indicate switching of a gate line to be selected (O_1 - O_4), and an output enable signal (OE_1 - OE_4) for each row to, when a gate line is selected by the gate driver, indicate duration during which the gate line is kept at the selected-period potential, and which feeds to the source driver, a source line potential setting indication signal to indicate that potentials of the respective source lines are to be set to potentials according to image data of respective pixels for one row, and a polarity control signal to make the polarities of the pixels in each column switched every row, wherein the control means operates as follows:

the control means feeds a signal changed to a first level and a second level in a predetermined period, as the switching signal to the gate driver;
the control means raises the source line potential setting indication signal at timing when the switching signal is changed to the first level, defines a period of the source line potential setting indication signal to be the same as the period of the switching signal, and feeds to the gate driver, the output enable signal to indicate as the duration during which the one gate line selected by the gate driver is kept at the selected-period potential, duration of H-s from a change of a level of the switching signal to the first level when H represents the period of the switching signal, t represents the first predetermined time, and s represents a second predetermined time, and the output enable signal to indicate as the duration during which the subsequent gate line to the one gate line is kept at the selected-period potential, duration from a point of time when t has elapsed since the change of the level of the switching signal to the first level, to a point of time when H-s has elapsed since the change of the level of the switching signal to the first level,

wherein the gate driver operates as follows:

the gate driver switches the one gate line and the subsequent gate line selected, every switching of the switching signal to the first level, and sets the selected gate line and subsequent gate line to the selected-period potential in accordance with the output enable signal, and wherein the source driver sets the potentials of the respective source lines to potentials according to image data of respective pixels

for one row in synchronism with a falling edge of the source line potential setting indication signal.

3. The drive device for a liquid crystal display device according to Claim 2, wherein the first predetermined time is a time that is at least the sum of a time needed to change the potentials of the source lines from a minimum to a maximum of set potentials for the source lines, and a time needed to change the source line potential setting indication signal to a high level.

15 Patentansprüche

1. Antriebsvorrichtung für eine Flüssigkristallanzeigevorrichtung (7), wobei die Flüssigkristallanzeigevorrichtung Source-Leitungen, die entlang Spalten von Pixeln angeordnet sind, die in einer Matrixstruktur gebildet sind, und Gate-Leitungen umfasst, die entlang Zeilen der in der Matrix-Struktur gebildeten Pixeln angeordnet sind, wobei die Antriebsvorrichtung für die Flüssigkristallanzeigevorrichtung Folgendes umfasst:

einen Gate-Treiber (3_a , 31_a , 32_a), der eine Gate-Leitung auswählt; und
einen Source-Treiber (4), der jede Zeile Polaritäten der Pixel in jeder Spalte umschaltet und der Potentiale der entsprechenden Source-Leitungen gemäß Bilddaten von entsprechenden Pixeln für eine Zeile auf Potentiale einstellt, während er die Polaritäten der Pixel in benachbarten Spalten einander entgegengesetzt macht, wobei der Gate-Treiber eine Gate-Leitung (O_1) und eine darauffolgende Gate-Leitung auswählt, die eine Gate-Leitung (O_3) einer Zeile nach derjenigen neben der einen Gate-Leitung ist, die darauffolgende Gate-Leitung mit einer Verzögerung von einer ersten vorbestimmten Zeit von dem Zeitpunkt, an dem die eine Gate-Leitung auf das Potential für die ausgewählte Periode eingestellt wurde, auf ein Potential für die ausgewählte Periode einstellt und die eine Gate-Leitung und die darauffolgende Gate-Leitung vor der Auswahl (LP) der Gate-Leitung neben der einen Gate-Leitung auf ein Potential für die nicht ausgewählte Periode einstellt.

2. Antriebsvorrichtung für eine Flüssigkristallanzeigevorrichtung nach Anspruch 1, die Folgendes umfasst:

ein Steuermittel (2_a), das in den Gate-Treiber ein Schaltsignal (CKV) zum Angeben des Umschaltens einer auszuwählenden Gate-Leitung (O_1 - O_4) und ein Ausgangsfreigabesignal

(OE₁-OE₄) für jede Zeile einspeist, um, wenn eine Gate-Leitung durch den Gate-Treiber ausgewählt wird, die Dauer anzugeben, während der die Gate-Leitung auf dem Potential für die ausgewählte Periode gehalten wird, und das in den Source-Treiber ein Source-Leitungspotential-Einstellungsangabesignal, um anzugeben, dass Potentiale der entsprechenden Source-Leitungen gemäß Bilddaten von entsprechenden Pixeln für eine Zeile auf Potentiale einzustellen sind, und ein Polaritätssteuersignal einspeist, um die Polaritäten der Pixel in jeder Spalte jede Zeile umzuschalten, wobei das Steuermittel wie folgt betrieben wird:

das Steuermittel speist ein Signal, das sich in einer vorbestimmten Periode auf einen ersten Pegel und einen zweiten Pegel geändert hat, als das Schaltsignal an den Gate-Treiber ein;
das Steuermittel erhöht das Source-Leitungspotential-Einstellungsangabesignal an dem Zeitpunkt, an dem das Schaltsignal auf den ersten Pegel geändert wird, definiert eine Periode des Source-Leitungspotential-Einstellungsangabesignals, um gleich der Periode des Schaltsignals zu sein, und speist das Ausgangsfreigabesignal, um als die Dauer, während der die eine durch den Gate-Treiber ausgewählte Gate-Leitung auf dem Potential für die ausgewählte Periode gehalten wird, die Dauer von H-s von einer Änderung eines Pegels des Schaltsignals auf den ersten Pegel anzugeben, wobei H die Periode des Schaltsignals darstellt, t die erste vorbestimmte Zeit darstellt und s eine zweite vorbestimmte Zeit darstellt, und das Ausgangsfreigabesignal, um als die Dauer, während der die auf die eine Gate-Leitung folgende Gate-Leitung auf dem Potential für die ausgewählte Periode gehalten wird, die Dauer von einem Zeitpunkt anzugeben, an dem t seit der Änderung des Pegels des Schaltsignals auf den ersten Pegel bis zu einem Zeitpunkt verstrichen ist, an dem H-s seit der Änderung des Pegels des Schaltsignals auf den ersten Pegel verstrichen ist, in den Gate-Treiber ein,

wobei der Gate-Treiber wie folgt betrieben wird:

der Gate-Treiber schaltet die eine Gate-Leitung und die darauffolgende ausgewählte Gate-Leitung bei jedem Schalten des Schaltsignals auf den ersten Pegel und stellt die ausgewählte Gate-Leitung und die darauffolgende Gate-Leitung gemäß dem

Ausgangsfreigabesignal auf das Potential für die ausgewählte Periode ein, und wobei der Source-Treiber die Potentiale der entsprechenden Source-Leitungen gemäß Bilddaten von entsprechenden Pixeln für eine Zeile synchron mit einer abfallenden Flanke des Source-Leitungspotential-Einstellungsangabesignals auf Potentiale einstellt.

3. Antriebsvorrichtung für eine Flüssigkristallanzeige nach Anspruch 2, wobei die erste vorbestimmte Zeit eine Zeit ist, die mindestens die Summe einer Zeit, die benötigt wird, um die Potentiale der Source-Leitungen von einem Minimum auf ein Maximum von eingestellten Potentialen für die Source-Leitungen zu ändern, und einer Zeit ist, die erforderlich ist, um das Source-Leitungspotential-Einstellungsangabesignal auf einen hohen Pegel zu ändern.

Revendications

1. Dispositif d'attaque pour un dispositif d'affichage à cristaux liquides (7), le dispositif d'affichage à cristaux liquides comprenant des lignes source disposées le long de colonnes de pixels formés selon un motif de matrice et des lignes de grille disposées le long de rangées constituées des pixels formés selon le motif de matrice, le dispositif d'attaque pour le dispositif d'affichage à cristaux liquides comprenant :

un circuit d'attaque de grille (3_a, 31_a, 32_a) qui sélectionne une ligne de grille ; et
un circuit d'attaque de source (4) qui commute les polarités des pixels de chaque colonne à chaque rangée et qui règle les potentiels des lignes source respectives sur des potentiels conformes aux données d'image de pixels respectifs pour une rangée, tout en rendant les polarités des pixels dans les colonnes adjacentes opposées les unes aux autres, dans lequel le circuit d'attaque de grille sélectionne une première ligne de grille (O₁) et une ligne de grille ultérieure qui est une ligne de grille (O₃) d'une rangée venant après celle située à côté de la première ligne de grille, règle la ligne de grille ultérieure sur un potentiel de période sélectionnée avec un retard d'un premier temps prédéfini par rapport au moment où la première ligne de grille est réglée sur le potentiel de période sélectionnée, puis règle la première ligne de grille et la ligne de grille ultérieure sur un potentiel de période non sélectionnée, préalable à la sélection (LP) de la ligne de grille située près de la première ligne de grille.

2. Dispositif d'attaque pour un dispositif d'affichage à

cristaux liquides selon la revendication n° 1, comprenant :

un moyen de commande (2_a) qui envoie au circuit d'attaque de grille un signal de commutation (CKV) afin d'indiquer la commutation d'une ligne de grille à sélectionner (O₁-O₄) et un signal d'activation de sortie (OE₁-OE₄) pour chaque rangée pour indiquer, lorsqu'une ligne de grille est sélectionnée par le circuit d'attaque de grille, la durée pendant laquelle la ligne de grille est maintenue au potentiel de période sélectionnée et qui envoie au circuit d'attaque de source un signal d'indication de réglage du potentiel de ligne source pour indiquer que les potentiels des lignes source respectives doivent être réglés sur des potentiels conformes aux données d'image de pixels respectifs pour une rangée et un signal de commande de polarité pour que les polarités des pixels de chaque colonne soient commutées à chaque rangée, le moyen de commande fonctionnant comme suit :

le moyen de commande envoie un signal modifié sur un premier niveau et un second niveau au cours d'une période prédéfinie en tant que signal de commutation au circuit d'attaque de grille ;

le moyen de commande élève le signal d'indication de réglage du potentiel de ligne source au moment où le signal de commutation est modifié sur le premier niveau, il définit une période du signal d'indication de réglage du potentiel de ligne source pour qu'elle soit identique à la période du signal de commutation et envoie au circuit d'attaque de grille le signal d'activation de sortie pour indiquer la durée au cours de laquelle la première ligne de grille sélectionnée par le circuit d'attaque de grille est maintenue au potentiel de période sélectionnée, la durée de H-s provenant d'un changement d'un niveau du signal de commutation sur le premier niveau lorsque H représente la période du signal de commutation, t représente le premier moment prédéfini et s représente un second moment prédéfini, et le signal d'activation de sortie en tant que durée pendant laquelle la ligne de grille ultérieure à la première ligne de grille est maintenue au potentiel de période sélectionnée, durée partant d'un point dans le temps où t s'est écoulé depuis le changement du niveau du signal de commutation vers le premier niveau à un point dans le temps où H-s s'est écoulé depuis le changement du niveau du signal de commutation sur le premier niveau,

dans lequel le circuit d'attaque de grille fonctionne comme suit :

le circuit d'attaque de grille commute la première ligne de grille et la ligne de grille ultérieure sélectionnée, chaque commutation du signal de commutation se faisant sur le premier niveau, et il règle la ligne de grille sélectionnée et la ligne de grille ultérieure sur le potentiel de période sélectionnée conformément au signal d'activation de sortie,

dans lequel le circuit d'attaque de source règle les potentiels des lignes source respectives sur les potentiels conformes aux données d'images de pixels respectifs pour une rangée en synchronisation avec un bord descendant du signal d'indication de réglage du potentiel de ligne source.

3. Dispositif d'attaque pour un dispositif d'affichage à cristaux liquides selon la revendication n° 2, dans lequel la première durée prédéfinie est une durée qui représente au moins la somme d'un temps nécessaire pour modifier les potentiels des lignes source, d'un minimum à un maximum de potentiels de consigne pour les lignes source, et d'un temps nécessaire pour modifier le signal d'indication de réglage de potentiel de ligne source sur un niveau supérieur.

Fig. 1

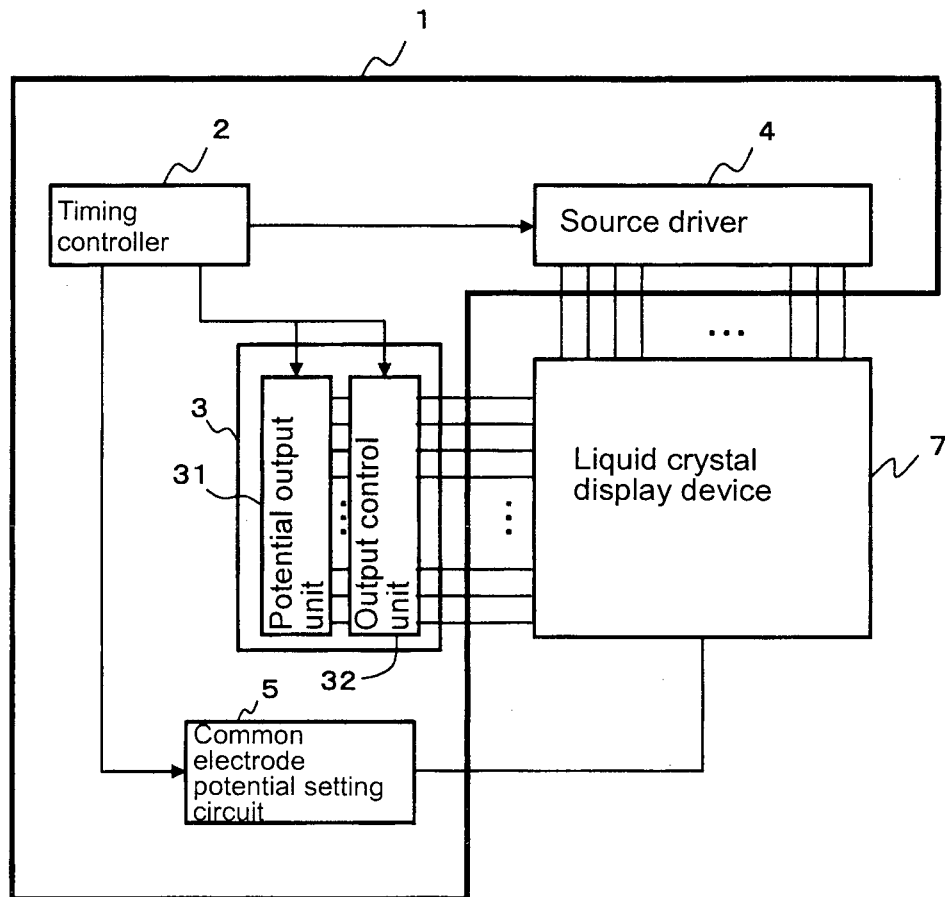


Fig. 2

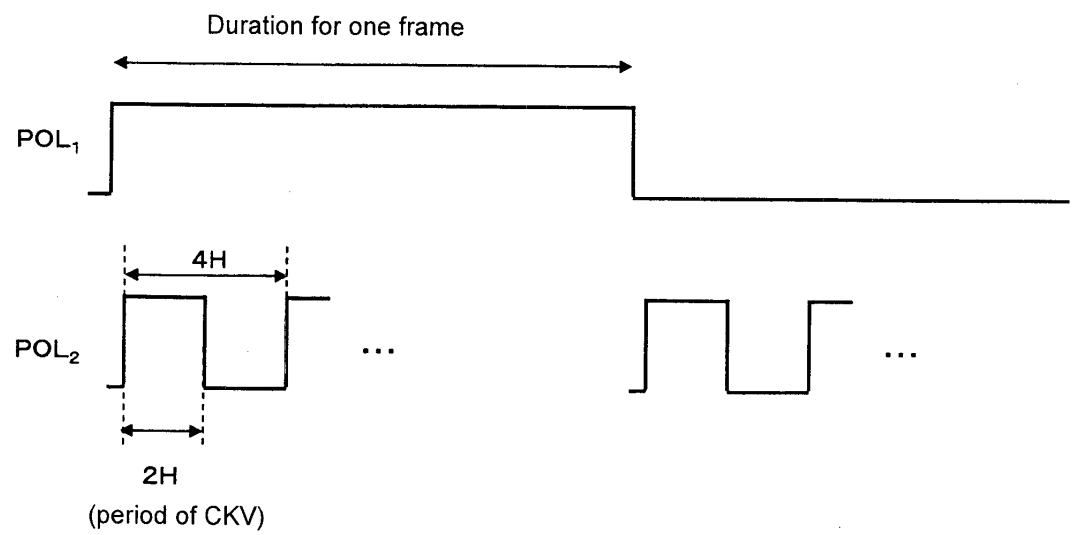


Fig. 3

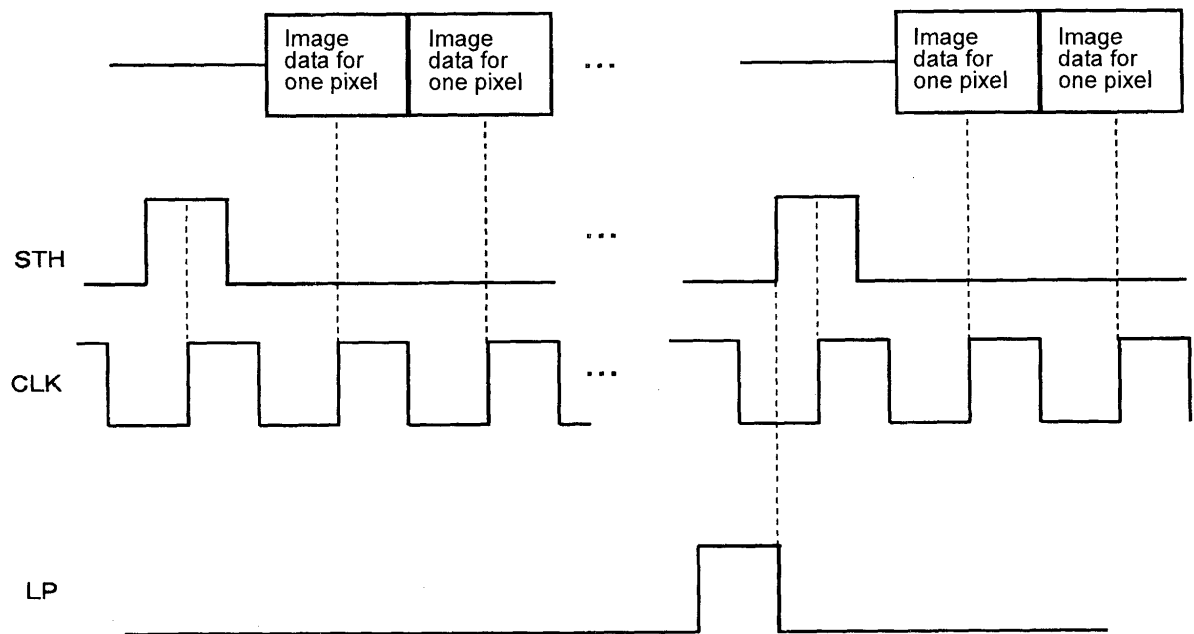
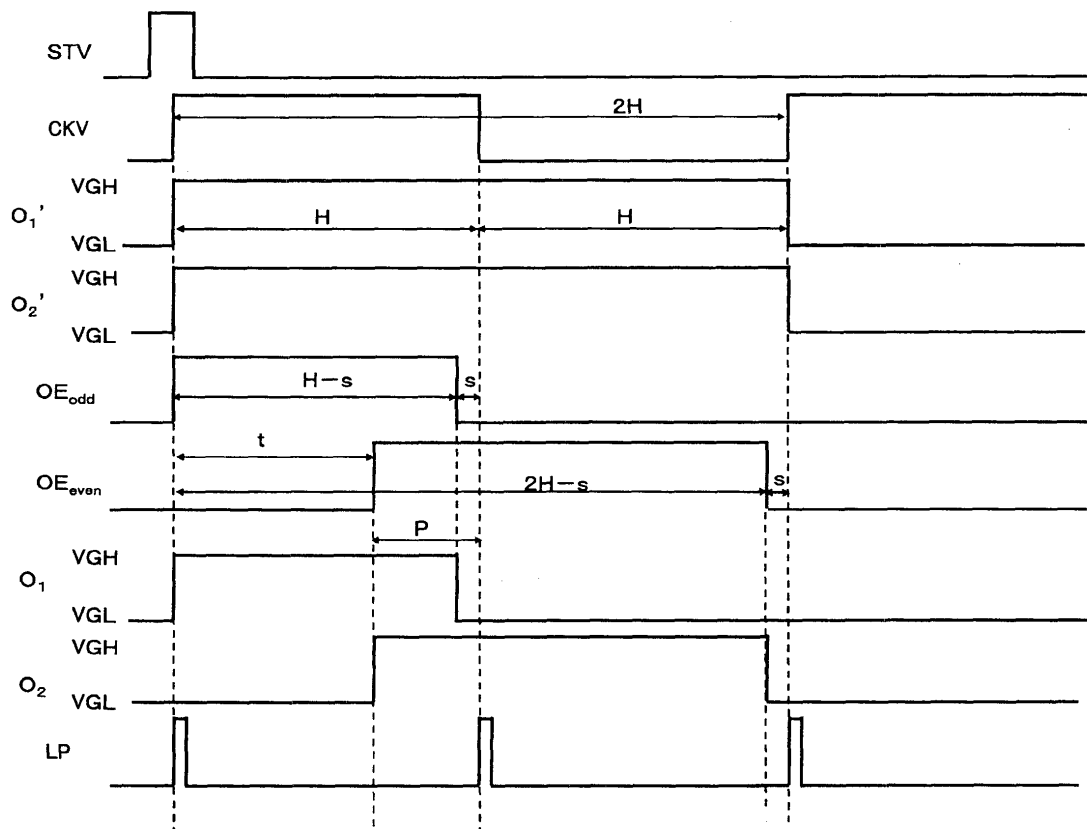


Fig. 4



P: Duration used for precharge of pixel in even-numbered row

Fig. 5

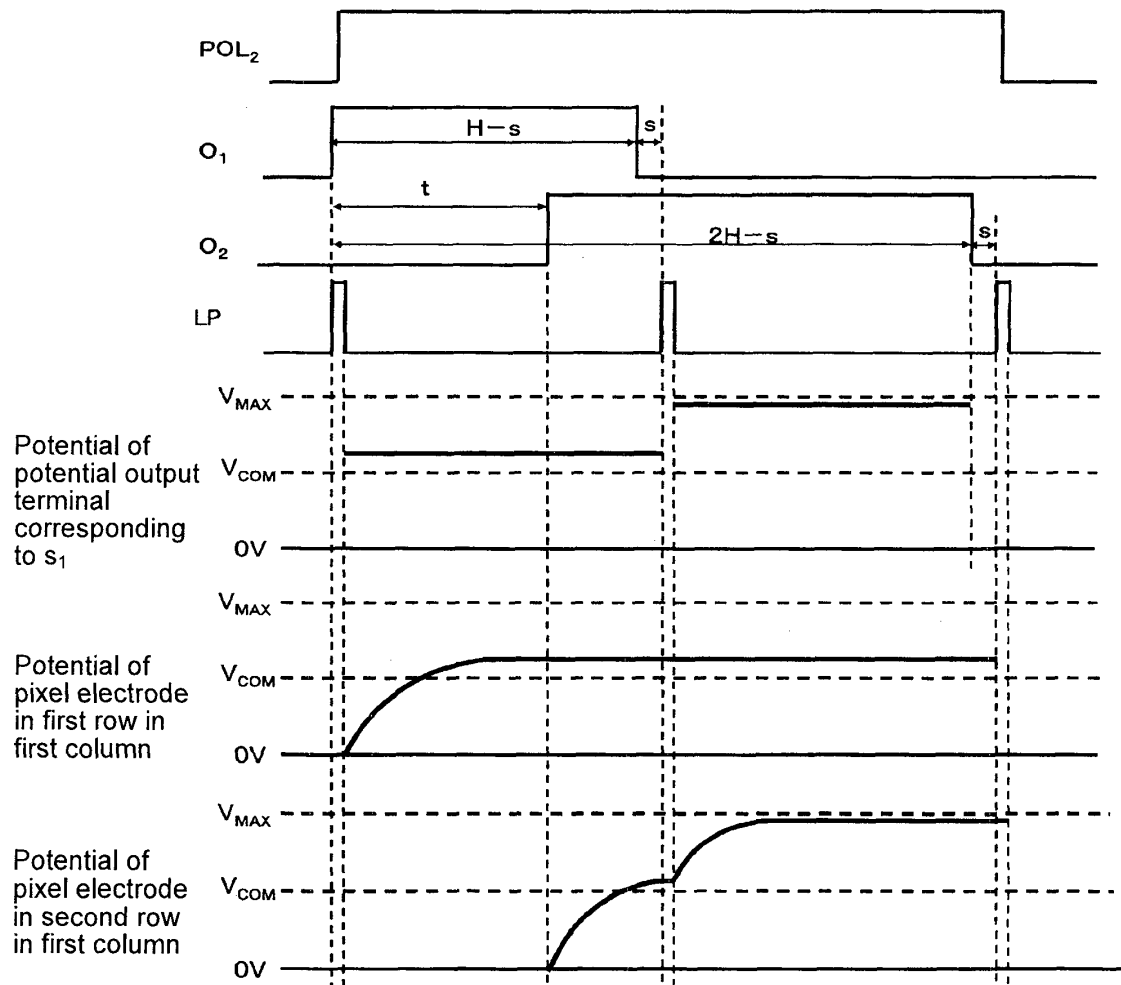


Fig. 6

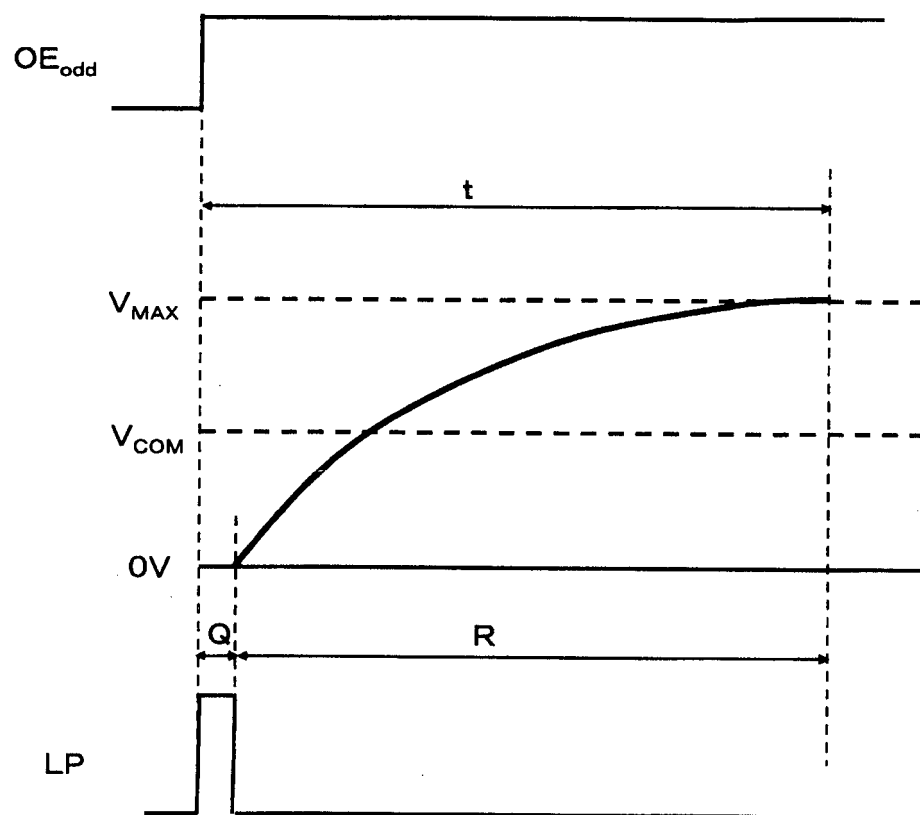


Fig. 7

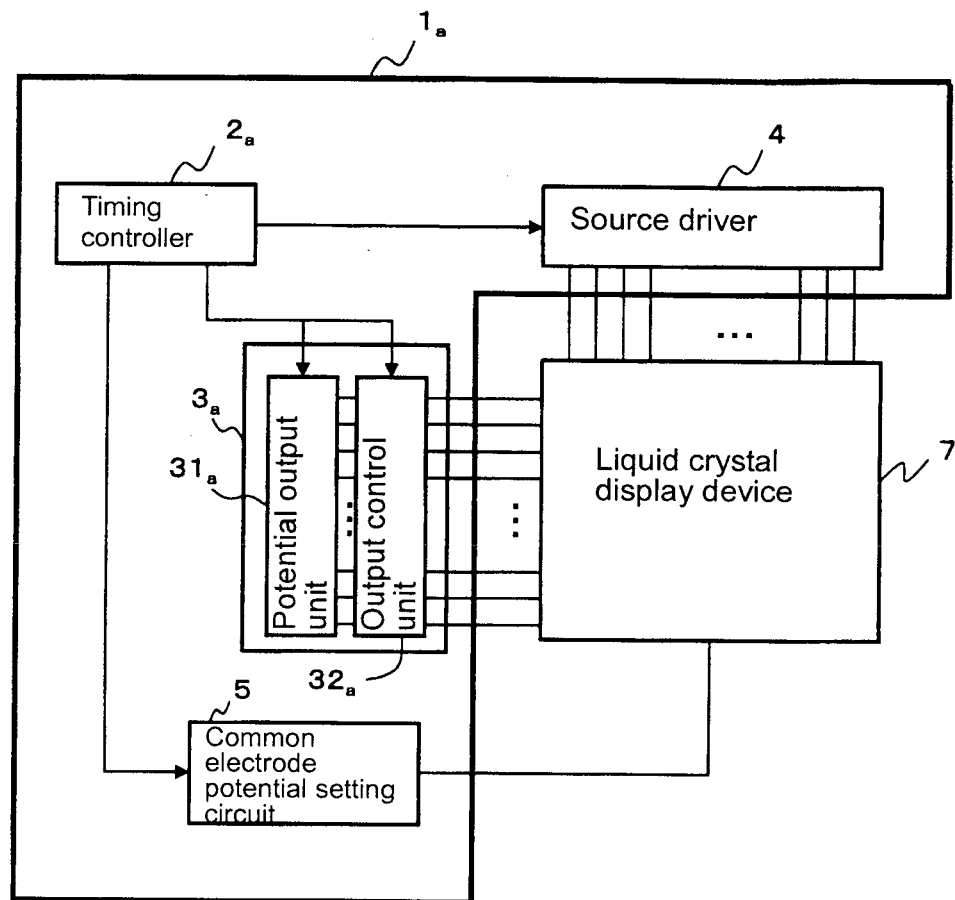


Fig. 8

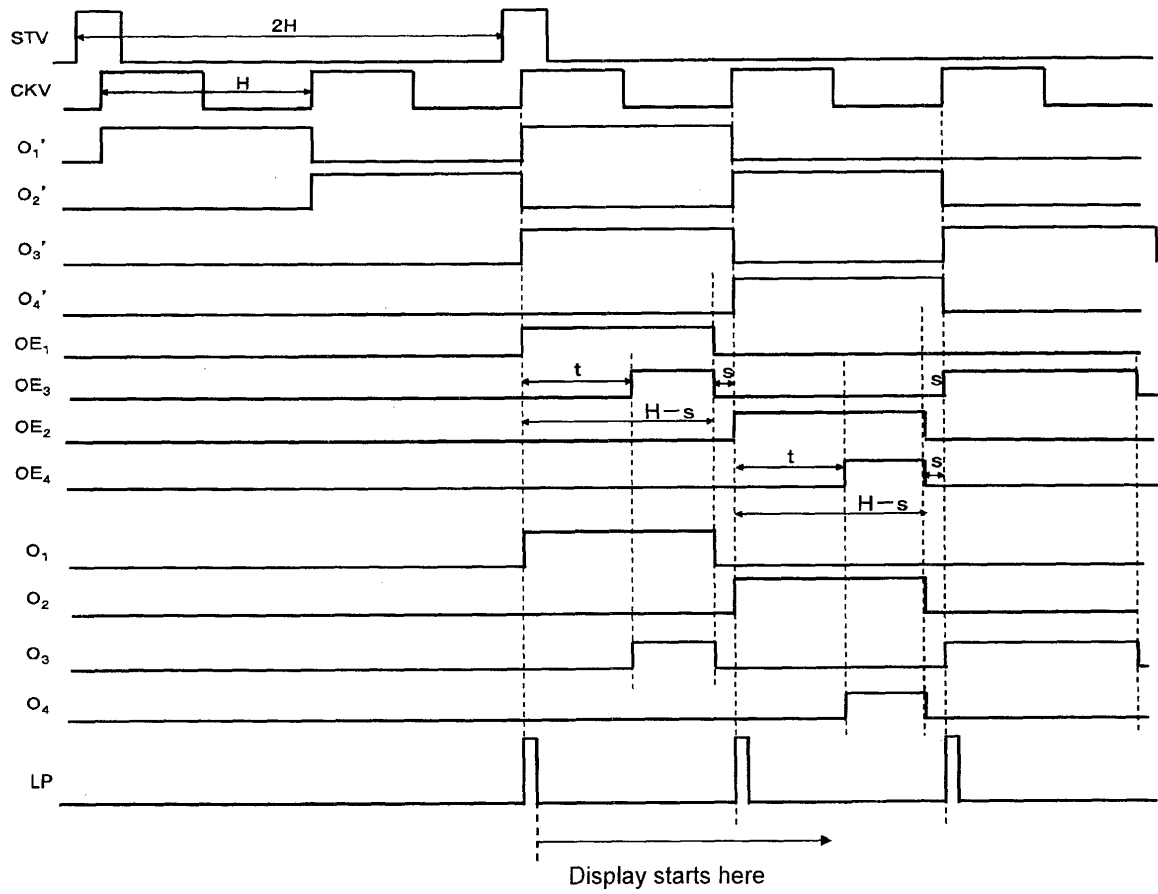


Fig. 9

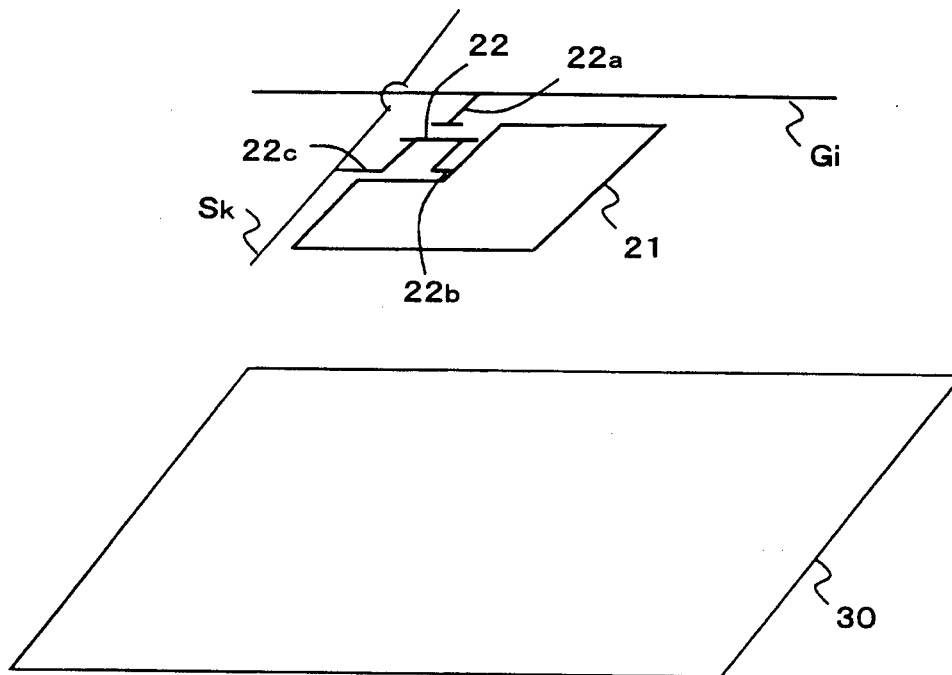


Fig. 10

	1st column	2nd column	3rd column	4th column	5th column	
1st row	+	-	+	-	+	-
2nd row	+	-	+	-	+	-
3rd row	-	+	-	+	-	+
4th row	-	+	-	+	-	+
						

⋮

Fig. 11

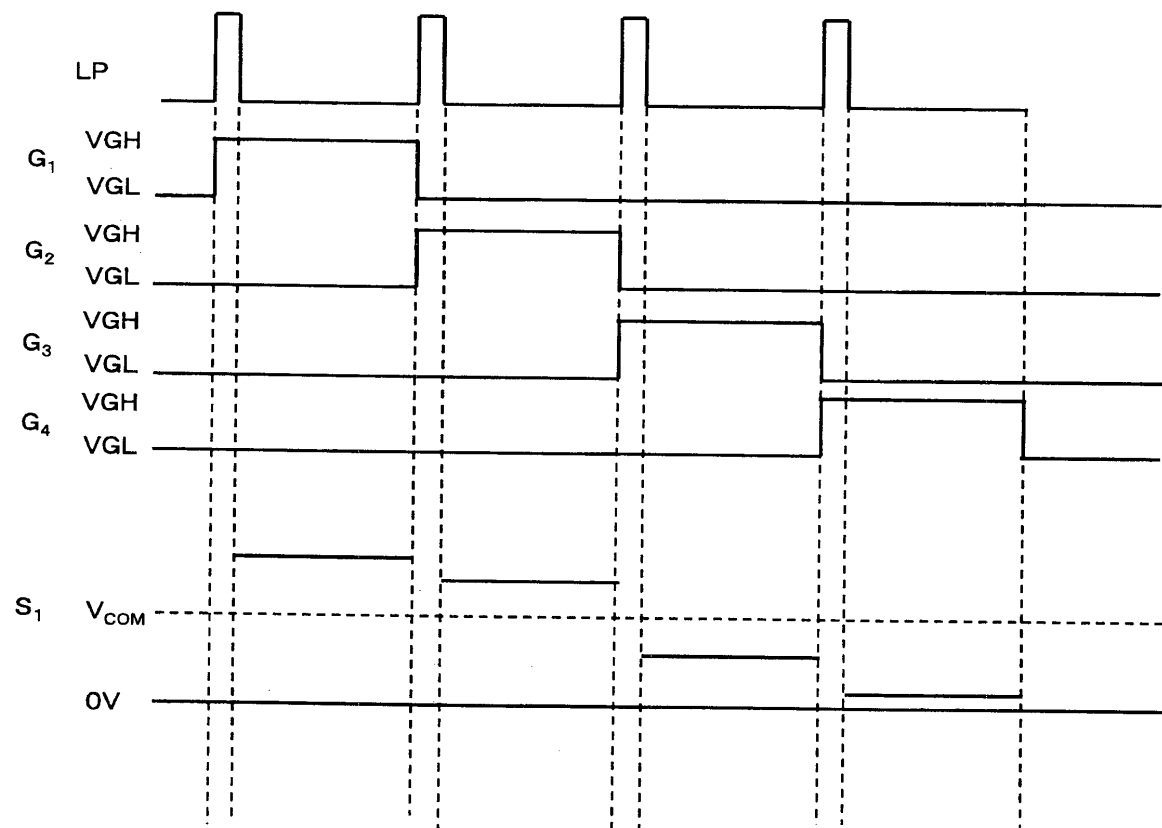
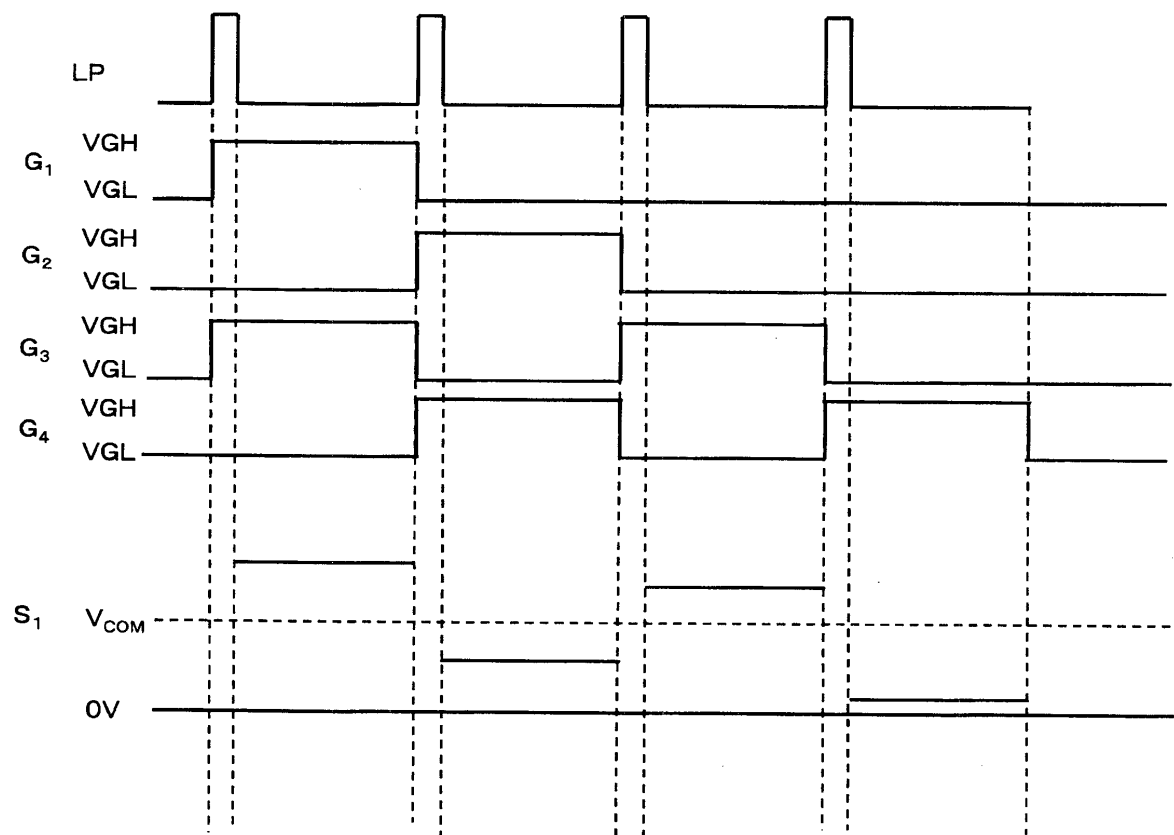


Fig. 12

	1st column	2nd column	3rd column	4th column	5th column	6th column	
1st row	+	−	+	−	+	−	
2nd row	−	+	−	+	−	+	
3rd row	+	−	+	−	+	−	
4th row	−	+	−	+	−	+	
							

Fig. 13



REFERENCES CITED IN THE DESCRIPTION

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申请(专利权)人(译)	京瓷显示器公司		
当前申请(专利权)人(译)	京瓷显示器公司		
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外部链接	Espacenet		

摘要(译)

栅极驱动器选择奇数行的栅极线和随后的偶数行的栅极线，并将偶数行的栅极线设置为具有预定时间延迟的选定周期电位。将奇数行的栅极线设置为选择周期电位的定时。之后，栅极驱动器将设置在选定周期电位的栅极线的电位设置为非选择周期电位。源极驱动器每两行切换每列中的像素的极性，并且根据一行的各个像素的图像数据将各个源极线的电位设置为电位，同时使相邻列中的像素的极性彼此相反。

Fig. 1

