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(54) **COLUMN ELECTRODE DRIVING CIRCUIT AND VOLTAGE GENERATING CIRCUIT FOR A LIQUID CRYSTAL DISPLAY**

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CIRCUIT DE COMMANDE D'ELECTRODE COLONNE ET CIRCUIT GENERATEUR DE TENSION
POUR AFFICHEUR A CRISTAUX LIQUIDES

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Description

1. Field of the Invention

[0001] The present invention relates to a display device, and in particular to a column electrode driving circuit used for a display device that can perform multi-gray-scale displaying or multicolored displaying.

2. Description of the Related Art

[0002] In a liquid crystal display device, for example, many pixels (pixel areas) are provided over an entire display area in a matrix or in an array equivalent thereto, and row and column electrodes are provided for applying parts of a liquid crystal medium corresponding to these pixels with the respective electric fields according to the pixel information. The row electrodes are electrically conductive patterns that extend in a horizontal direction in the display area and the column electrodes are electrically conductive patterns that extend in a vertical direction in the same area.

[0003] Most active matrix type liquid crystal display devices are provided with, for example, TFTs (thin film transistors) as active elements to individually drive parts of the liquid crystal medium for each pixel, wherein the row electrodes are connected to the gates of the TFTs and the column electrodes are connected to the sources of the TFTs. Usually, one of the row electrodes corresponding to so-called scanning lines is selected for each horizontal scanning period of an image signal, and a gate voltage is supplied to the selected row electrode for simultaneously activating a group of TFTs connected to the selected row electrode. On the other hand, source voltages (pixel information signals) according to an image of the line are supplied to the activated TFTs to display the image of the line. Driving circuits for performing voltage-application to the row and column electrodes are provided, respectively.

[0004] There is one typical type of column electrode driving circuit which generates a number of gray-scale voltages necessary for different gray-scale levels required for the display device, and selects any of the gray-scale voltages in accordance with the pixel information for each pixel information signal so as to supply the selected gray-scale voltage to the corresponding column electrode. This driving circuit is arranged in such a manner that all gray-scale voltages are outputted via amplifiers. There is also a type of column electrode driving circuit that has amplifiers whose outputs are connected to the column electrodes, respectively.

[0005] The present inventor has noticed that the former would cause the amplifiers and their peripheral circuits to have an enormous power consumption. The present inventor has also conceived that the latter would have a feature of constantly operating quite a large number of amplifiers corresponding in number to dots for one line of the displayed image and again having an enormous

power consumption, whereby it can be estimated that power consumption will increase further considering an increase in the number of dots based on a tendency to increase resolution in the future.

[0006] With the advent of portable devices or wearable devices such as cellular phones whose display functions have been unprecedentedly enhanced, there is a perception that notably the latest electronics devices are required not only to allow a long time operation with a limited battery capacity but also to have high-level display performance.

[0007] Document US 5,343,221 discloses a prior art column electrode driving circuit for a display device.

15 SUMMARY OF THE INVENTION

[0008] It is an object of the present invention to provide a column electrode driving circuit with a reduced power consumption. The invention is defined by the independent claims. The dependent claims define advantageous embodiments.

[0009] In particular, the invention relates to a column electrode driving circuit for a display device having a matrix of rows and columns of display segments, a display segment comprising at least one pixel capable of gray-scale displaying, the driving circuit comprising:

gray-scale voltage producing means including amplifiers, each amplifier having a first input for receiving one value of a range of a plurality of gradually increasing gray-scale voltage values, and having an amplifier output for delivering an output signal in proportion to the voltage level at the input; and selecting means having inputs coupled to the outputs of the amplifiers for selecting and outputting any of the output signals of the amplifiers for each display segment in a row that is being addressed in accordance with an image signal indicative of a gray-scale level to be generated by the display segment, the driving circuit characterised in that it can operate in a predetermined mode, wherein the gray-scale voltage producing means power on a predetermined number of amplifiers, which correspond to a predetermined number of predetermined gray-scale values within the range and power off the other amplifiers, and the selecting means select the output signals of the amplifiers which are powered on.

[0010] Alternatively, the invention relates to a column electrode driving circuit for a display device capable of gray-scale displaying, comprising:

gray-scale voltage producing means including amplifiers which relay a plurality of gray-scale voltages having values that are gradually level-shifted, respectively, and potential divider circuits coupled between outputs of the amplifiers for dividing their out-

put voltages to produce finer gray-scale voltages;
 and
 selecting means for selecting and outputting any of
 the gray-scale voltages for each pixel or each pre-
 determined displayed unit in accordance with an im-
 age signal indicative of a gray-scale level for the pixel
 or displayed unit,
 the driving circuit characterised in that it can operate
 in a predetermined mode, wherein
 the gray-scale voltage producing means output-dis-
 ables any potential divider circuits that produce a
 predetermined number of gray-scale voltages which
 correspond to predetermined gray-scale levels by
 electrically isolating the subject potential divider cir-
 cuit from corresponding amplifiers or from one of the
 amplifiers, thereby avoiding an output current of that
 amplifier from flowing through the fine potential di-
 vider circuits,
 and the selecting means selecting any of effective
 voltages during the predetermined mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] These and other aspects of the invention will
 be further elucidated and described with reference to the
 drawings, in which:

Fig. 1 is a block diagram showing a general consti-
 tution of a matrix addressing circuit applied with the
 present invention;
 Fig. 2 is a block diagram showing a configuration of
 a source driver according to the present invention;
 Fig. 3 is a time chart showing an operation of a data
 conversion circuit in the source driver of Fig. 1;
 Fig. 4 is a diagram showing one structural example
 of a gray-scale voltage producing circuit in the source
 driver of Fig. 1;
 Fig. 5 is a schematic illustration showing an arrange-
 ment of a pixel data block in an image data signal
 and relations between values of the block and the
 corresponding gray-scale voltages;
 Fig. 6 is a schematic illustration showing one exam-
 ple of arrangement of a pixel data block in an image
 data signal and relations between values of the block
 and the corresponding gray-scale voltages during
 16-gray-scale displaying;
 Fig. 7 is an illustration showing a structural example
 of a pixel data block when 6-bit image data are en-
 tered in a forced mode;
 Fig. 8 is a diagram showing a modification of the
 arrangement of Fig. 4;
 Fig. 9 is a schematic illustration showing another ex-
 ample of arrangement of a pixel data block in an
 image data signal and relations between values of
 the block and the corresponding gray-scale voltages
 during 16-gray-scale displaying, which are used for
 the arrangement of Fig. 8;
 Fig. 10 is an illustration showing a structural example

of a pixel data block when 6-bit image data are en-
 tered in a forced mode, which is used for the arrange-
 ment of Fig. 8;

Fig. 11 is a graph showing relations between values
 of gray-scale voltages and their ranking for compar-
 ing one arrangement example and the other arrange-
 ment example of an image data block;

Fig. 12 is a diagram showing a modification of the
 arrangement of Fig. 4, which is used instead of the
 arrangement of Fig. 8;

Fig. 13 is a schematic illustration showing the other
 example of arrangement of a pixel data block in an
 image data signal and relations between values of
 the block and the corresponding gray-scale voltages
 during 16-gray-scale displaying, which are used for
 the arrangement of Fig. 12;

Fig. 14 is an illustration showing a structural example
 of a pixel data block when 6-bit image data are en-
 tered in a forced mode, which is used for the arrange-
 ment of Fig. 12;

Fig. 15 is a block diagram showing one example of
 processing way for a pixel data block;

Fig. 16 is a block diagram showing another example
 of processing way for a pixel data block;

Fig. 17 is a diagram showing the other structural ex-
 ample of gray-scale voltage producing circuit in the
 source driver;

Fig. 18 is a diagram showing a modification of a con-
 stitution of Fig. 17;

Fig. 19 is a schematic illustration showing an ar-
 rangement of a pixel data block and relations be-
 tween values of the block and the corresponding
 gray-scale voltages during a 3-bit displaying mode;

Fig. 20 is a schematic illustration showing an ar-
 rangement of a pixel data block and relations be-
 tween values of the block and the corresponding
 gray-scale voltages during a 2-bit displaying mode;

Fig. 21 is a schematic illustration showing an ar-
 rangement of a pixel data block and relations be-
 tween values of the block and the corresponding
 gray-scale voltages during a 1-bit displaying mode;

Fig. 22 is a block diagram showing a schematic con-
 struction of the upper part of one example of multi-
 stage switching type gray-scale voltage producing
 circuit according to the present invention;

Fig. 23 is a block diagram showing a schematic con-
 struction of the lower part of one example of multi-
 stage switching type gray-scale voltage producing
 circuit according to the present invention;

Fig. 24 is a table showing defined contents of control
 signals used in the gray-scale voltage producing cir-
 cuit of Figs. 22 and 23;

Fig. 25 is a block diagram showing a schematic con-
 struction of the upper part of another example of mul-
 ti-stage switching type gray-scale voltage producing
 circuit according to the present invention;

Fig. 26 is a block diagram showing a schematic con-
 struction of the lower part of another example of mul-

ti-stage switching type gray-scale voltage producing circuit according to the present invention;

Fig. 27 is a block diagram showing a schematic construction of the other embodiment of gray-scale voltage producing circuit according to the present invention;

Fig. 28 is a block diagram showing a schematic construction of a further embodiment of gray-scale voltage producing circuit according to the present invention; and

Fig. 29 is a block diagram showing a schematic construction of a yet further embodiment of gray-scale voltage producing circuit according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT (S)

[0012] The embodiments of the present invention will be hereinbelow explained in more detail with reference to the accompanying drawings.

[0013] Fig. 1 shows a general constitution of a matrix addressing circuit of a liquid crystal display device according to an embodiment of the present invention.

[0014] In Fig. 1, this matrix addressing circuit 10 is arranged to drive a display panel 20 of an active matrix liquid crystal display (LCD) device on which, for example, field-effect thin film transistors (TFTs) 21 are placed in correspondence with pixels as active elements for driving pixels within a predetermined display area.

[0015] On the display panel 20, the TFTs 21 are arranged in Y rows X columns of a matrix. Gate electrodes of the TFTs 21 are connected, on a row basis, to gate bus lines running across the display area for each row horizontally and in parallel with each other, and source electrodes of the TFTs 21 are connected, on a column basis, to source bus lines running across the display area for each column vertically and in parallel with each other. Drain electrodes of the TFTs 21 are connected to their respective pixel electrodes 23, and individual pixel areas are basically determined by these pixel electrodes 23.

[0016] The display panel 20 is further provided with a common electrode 25 placed opposite to the pixel electrodes with a gap. This gap is filled with a liquid crystal medium (not shown), and the common electrode 25 extends over the entire display area in this example. The TFTs 21 are selectively turned on row by row by a gate control signal supplied through the gate bus line. The TFTs which are turned on are brought in a driving state based on pixel information signals supplied through the source bus lines. The pixel electrodes 23 are given a potential according to such a driving state by the drain electrodes. The orientation of the liquid crystal medium is controlled for each pixel electrode by an electric field determined by a difference between this given pixel electrode potential and a level of the voltage supplied to the common electrode 25. Thus, the liquid crystal medium can modulate the light originating from a backlight system

(not shown) and passing through the medium to the front side (or the reflection of incident light from a front light system) in accordance with the pixel information for each pixel. Since such configurations and operations of the liquid crystal display panel are well known they are not explained further here.

[0017] The driving circuit 10 is provided with a signal control section 30, a reference voltage producing section 40, a source driver 50 as column driving means and a gate driver 60 as row driving means.

[0018] The signal control section 30 receives image data signals in the form of red (R), green (G) and blue (B) color components of the image data, dot clock signal CLK and synchronization signals SYNC including horizontal and vertical synchronization signals from signal supply means (not shown). The signal control section 30 transfers the image data signals R,G,B, also referred to as "data", in accordance with timings of the clock signal CLK and synchronization signals SYNC, to the source driver 50. Furthermore, the signal control section 30 generates a source control signal St to control the source driver 50 and a gate control signal Gc to control the gate driver 60 in accordance with the clock signal CLK and synchronization signals SYNC.

[0019] The voltage producing section 40 produces and supplies supply voltages V_s , V_p necessary for the source driver 50 and the supply voltage V_g for the gate driver 60 on the basis of a supply voltage V from a power supply system (not shown). The voltage producing section 40 further produces and supplies a voltage signal Vcom to the common electrode 25 on the display panel 20 based on the supply voltage V.

[0020] The source driver 50 is provided with a digital-analog converter for each of the color components R, G and B of the image data signals. For each pixel in a horizontal line of the display panel 20, an analog signal is generated. The level of this analog signal is corresponding to the gray level to be displayed by that pixel in accordance with the image data signals. The voltage level of each analog signal is kept constant from the beginning of one horizontal scanning cycle until the next horizontal scanning cycle starts and is supplied to the respective corresponding source bus lines. The source control signal St supplied to the source driver 50 constitutes a basis for determining timings such as a horizontal scanning cycle, timing of the digital to analog R conversion, voltage level application to the source bus lines and the like.

[0021] The gate driver 60 selectively activates the gate bus lines of the display panel 20 in accordance with the gate control signal Gc for example, selectively supplies a predetermined high voltage to the bus lines sequentially. The activated gate bus line turns on the respective TFTs connected thereto, while at the same time these TFT sources are supplied with the above-described analog signals. Therefore each TFT transfers a potential corresponding to the level of the analog signal to the corresponding part of the liquid crystal medium through its drain and pixel electrode, so as to modulate the electric

field and molecular orientation state of the medium. Thus, all pixels on the corresponding line or row are optically modulated simultaneously in accordance with the analog signals for that line as described above.

[0022] The display panel 20 is generally "alternate-driven" by means of the control of the source driver 50 and gate driver 60 and of the common voltage signal Vcom, but to simplify the explanation, it will not be further mentioned here. However, it should be noted that such alternate-driving mode is included in the scope of the invention.

[0023] Fig. 2 shows a functional block diagram illustrating a schematic configuration of the source driver 50. Supply voltages V_s and V_p are supplied from the voltage producing section 40 to the gray-scale voltage producing circuit 2. The gray-scale voltage producing circuit 2 is designed to generate a maximum number (64 in this example) of gray-scale voltages (hereinafter represented as "#0 to #63") required by the display panel and the details thereof will be described later. The gray-scale voltage producing circuit 2 is also supplied with an operating mode control signal 4_s as an operating mode signal according to the number of gray-scale levels to be represented during displaying (that is, the number of gray-scale levels necessary for a current display operation). The gray-scale voltage producing circuit 2 is further supplied with a forced mode control signal 4_f according to the number of gray-scale levels which is to be forcibly represented irrespective of the current display operation.

[0024] Gray-scale voltages #0, #1, ..., #63 outputted from the gray-scale voltage producing circuit 2 are supplied to the respective input terminals 30, 31, ..., 3x of data decoding and voltage selection circuits (hereinafter referred to as "decoding and selection circuits"), where "x" denotes the number of column electrodes of the display panel 20. The decoding and selection circuits 30, 31, ..., 3x are further supplied with "serial-parallel converted" image data signals from the data conversion circuit 1 as their respective selection control signals. The decoding and selection circuits each select any one of the gray-scale voltages in accordance with this selection control signal and supply the selected voltage to the corresponding column electrode.

[0025] The data conversion circuit (S/P) 1 performs the function of serially receiving and capturing the input image data signal "data" and of, at the same time outputting in parallel the data signal for each horizontal scanning cycle. More specifically, as shown in Fig. 3, the input image data signal has a form in which a group of pixel data blocks $D_0, D_1, D_2, \dots, D_x$ (x corresponds to the number of the predetermined displayed units for one line or the number of column electrodes of the display panel 20) each consisting of 6 bits as information of one pixel arrive consecutively and sequentially on the time series. The data conversion circuit 1 holds this pixel data block group for every horizontal scanning cycle (H) based on the timing signal St while updating and outputting each of the pixel data blocks for the one horizontal scanning

cycle at the same time. Therefore, the 6-bit pixel data blocks $D_0, D_1, D_2, \dots, D_x$ are outputted to the decoding and selection circuits 30, 31, 32, ..., 3x simultaneously or in parallel, as shown in "output of S/P1" of Fig. 3.

[0026] Each of the decoding and selection circuits selects the corresponding gray-scale voltage in accordance with the parallel output of the 6-bit pixel data block. One pixel data block represents any one of 64 kinds of information, and therefore each decoding and selection circuit can decode the information and select any one of the gray-scale voltages #0, #1, ..., #63 corresponding to the decoding result. The manner of such decoding and selection will be described later.

[0027] Thus, gray-scale voltages according to the image data signal "data" are updated for every horizontal scanning cycle while being supplied to the column electrodes in line sequence.

[0028] Fig. 4 schematically illustrates an internal configuration of the gray-scale voltage producing circuit 2.

[0029] In Fig. 4, the basic gray-scale voltage V_s from the (preceding) voltage producing section 40 (see Fig. 1) is divided by a potential divider circuit based on series circuits of resistors R_0 to R_{63} formed between a power supply point and a grounding point. As shown in the figure, these potential divider resistors are tapped at the common connection points and grounding point, and the divisional voltages V_0 to V_{63} are obtained from the tap outputs. These divisional voltages are inputs of buffer amplifiers A_0 to A_{63} , respectively. These amplifiers perform predetermined amplification on the input divisional voltages (with input-output ratio of 1.0 in this example) while securing impedance matching with the column electrodes and supply outputs to the column electrodes as gray-scale voltages #0, #1, ..., #63.

[0030] The gray-scale voltage producing circuit 2 according to this embodiment is characterized in that a predetermined number of amplifiers of these amplifiers serve as specific amplifiers and take fixed forms whereby the amplifiers are supplied with the amplifier supply voltage V_p from the voltage producing section 40, while the remainder of the amplifiers serve as unspecified amplifiers which are interruptible amplifiers corresponding to predetermined gray-scale levels to be omissible, the remainder being supplied with the supply voltage V_p selectively. As is apparent from Fig. 4, the specific amplifiers $A_0, A_4, \dots, A_{55}, A_{59}, A_{63}$ are connected to the power line in a fixed manner, while the remaining unspecified amplifiers A_1 to $A_3, \dots, A_{56}$ to A_{58} , and A_{60} to A_{62} are connected to the power line via switching circuits SW_1 to $SW_3, \dots, SW_{56}$ to SW_{58} , and SW_{60} to SW_{62} , respectively. Then, these switching circuits are constructed to be controlled to ON/OFF by a common control signal C_0 . This control signal C_0 is obtained from the output of an AND gate 201 that carries out the logical AND between the above described operating mode signal 4_s and the inverted output of the above described forced mode signal 4_f through an inversion gate 200.

[0031] In this example, the number of the specific am-

plifiers whose power supplies are fixed is 16 and these are selected amplifiers whose inputs are applied with the divisional voltages (specific gray-scale voltages) V_0 , V_4 , ..., V_{55} , V_{59} , V_{63} ranked in substantially equal intervals in the voltage range from voltage V_0 to V_{63} . On the other hand, the remaining 48 unspecified amplifiers are selectively supplied with power and these are the amplifiers whose inputs are applied with the divisional voltages (unspecific gray-scale voltages or intermediate gray-scale voltages) V_1 to V_3 , ..., V_{56} to V_{58} , V_{60} to V_{62} representing intermediate values corresponding to the omisable gray-scale levels between the specific gray-scale voltages in the voltage range.

[64-gray-scale displaying]

[0032] In this gray-scale voltage producing circuit 2, in the case where the number of gray-scale levels specified in a display operation when the forced mode signal 4f does not show the forced mode and is at a low level is 64, which is a maximum number of gray-scale levels of the display panel 20, the control signal C_0 is active by the control signal 4s that represents a state corresponding to this case (here, a high level) and the switching circuits attached to the selective power supply type amplifiers turn ON. This causes all the amplifiers of the gray-scale voltage producing circuit to be brought into operation, whereby all gray-scale voltages, that is, not only gray-scale voltages #0, #4, ..., #55, #59, #63 but also gray-scale voltages #1 to #3, ..., #56 to #58, #60 to #62 voltages based on the voltages V_1 to V_3 , ..., V_{56} to V_{58} , V_{60} to V_{62} are outputted validly.

[16-gray-scale displaying]

[0033] On the other hand, in the case where the number of gray-scale levels specified in a display operation when the forced mode signal 4f does not indicate a forced mode and is at a low level is 16, the control signal C_0 is inactive by the control signal 4s representing a state corresponding to this case (here, low level) and the switching circuits attached to the selective power supply type amplifiers turn OFF. This causes the amplifiers to be electrically isolated (the gray-scale voltage lines are substantially opened), thereby bringing only the persistent power supply type amplifiers A_0 , A_4 , ..., A_{55} , A_{59} , A_{63} into operation. Thus, only the 16 specific gray-scale voltages #0, #4, ..., #55, #59, #63 are outputted validly.

[0034] When the forced mode signal 4f indicates a forced mode and is at a high level, the control signal C_0 is inactive and the switching circuits are turned OFF irrespective of the number of gray-scale levels specified during the display operation, so that only the 16 specific gray-scale voltages are outputted validly alike.

[0035] With the gray-scale voltage producing circuit 2 having such a configuration and in cooperation with the decoding and selection circuits 30 to 3x, the source driver 50 shown in Fig. 2 performs the following unique opera-

tions.

[0036] In the case of normal 64-gray-scale displaying, the pixel data signal "data" arrives with all 6 bits per pixel being enabled. At this time, the format of one pixel data block Dn can be expressed as shown in Fig. 5. That is, six bits Q_0 , Q_1 , Q_2 , Q_3 , Q_4 and Q_5 each having an arbitrary binary value are arranged from the LSB to the MSB sequentially. As shown in a more detailed example in Fig. 5, a relationship between the values that these bits can take and the gray-scale voltages is defined. In this example, the binary values shown by the bit trains are directly used as ranking numbers of the gray-scale voltages.

[0037] As described above, in the case of 64-gray-scale displaying, all amplifiers of the gray-scale voltage producing circuit 2 are operated and all gray-scale voltages are effectively outputted and supplied to the decoding and selection circuits 30 to 3x. Correspondingly, the decoding and selection circuits 30 to 3x also decode the pixel data block Dn based on the relationship shown in Fig. 5 so as to determine which corresponds to the content of the data and select any of the gray-scale voltages #0 to #63 supplied thereto. Since all the pixel data blocks for to one horizontal scanning cycle may designate all 64 kinds of gray-scale voltages, full shades of gray-scale displaying of image data in the format of 6 bits per pixel is achieved with all gray-scale voltages being outputted validly and by selecting any one of these gray-scale voltages for each column electrode.

[0038] Unlike the above, in the case of normal 16-gray-scale displaying, the pixel data signal "data" arrives with 4 bits per pixel being enabled as shown at the top of Fig. 6. The format of one pixel data block Dn at this time can be set as shown on the middle row of Fig. 6. In this example, basically without destroying the block format during the above described 64-gray-scale displaying, four bits Q_3 , Q_2 , Q_1 and Q_0 each having an arbitrary binary value are sequentially arranged from the MSB in the block and at the same time two higher-order bits Q_3 and Q_2 of the bit train are repeatedly located in the two bit positions on the LSB side in the block (higher-order bit relocation format). The third row of Fig. 6 shows the further details of this mode and a relationship between the values that these bits can take and gray-scale voltages is defined.

[0039] On the other hand, in the case of forced 16-gray-scale displaying, the pixel data signal "data" may arrive with all 6 bits per pixel being enabled as shown at the top of Fig. 7. The format of one pixel data block Dn at this time can be set as shown on the middle row of Fig. 7. In this example, basically without destroying the block format during the above-described 64-gray-scale displaying, four bits Q_5 , Q_4 , Q_3 and Q_2 each having an arbitrary binary value are sequentially arranged from the MSB in the block and at the same time two higher-order bits Q_5 and Q_4 of the original bit train instead of the original two bits Q_1 and Q_0 are repeatedly located in the two bit positions on the LSB side in the block (higher-order bit relocation format). The third row of Fig. 7 shows the fur-

ther details of this mode and a relationship between the values that these bits can take and gray-scale voltages is defined.

[0040] In the case of forced 16-gray-scale displaying, when the pixel data signal "data" arrives with 4 bits per pixel being enabled as shown at the top of Fig. 6, the two higher-order bits Q_3 and Q_2 are copied to the lower-order bits as in the case of the normal 16-gray-scale displaying described above.

[0041] As a result, in both cases of 6-bit data input and 4-bit data input, the same 16-gray-scale voltages can be designated.

[0042] As described above, in the case of normal/forced 16-gray-scale displaying, only some amplifiers A_0 , A_4 , ..., A_{55} , A_{59} , A_{63} of the gray-scale voltage producing circuit 2 operate and only gray-scale voltages limited to 16 kinds of #0, #4, #8, #12, #17, #21, #25, #29, #34, #38, #42, #46, #51, #55, #59 and #63 are outputted efficiently and supplied to the decoding and selection circuits. Correspondingly, the decoding and selection circuits 30 to 3x also decode the pixel data block D_n based on the relationship shown in Figs. 6 and 7 so as to decide which corresponds to the content of the data and select any one of the gray-scale voltages #0, #4, #8, #12, #17, #21, #25, #29, #34, #38, #42, #46, #51, #55, #59 and #63 supplied. Since only these 16 kinds of gray-scale voltages can be designated even for all the pixel data blocks for one horizontal scanning cycle, selecting any one of them for each column electrode allows gray-scale displaying of image data in the format of 4 bits per pixel to be implemented appropriately.

[0043] According to the source driver 50 as described above, in the case of a display mode with fewer gray-scale levels, it is possible to electrically isolate amplifiers that output unnecessary gray-scale voltages, thus reducing power consumption. This advantage becomes noticeable for a display device whose number of intermediate tones to be displayed is variable. For example, in the case of so-called mobile or wearable devices, represented by a cellular phone, there are not so many chances where the user operates the devices, and rather the time of waiting operations is overwhelmingly long. Such devices often have a variety of functions from an operating mode requiring high display quality to an operating mode only requiring two-tone display. Thus, saving unnecessary power in such a waiting operation and display mode with a small-number of intermediate tones is suitable for an actual operation and reasonable, without forcing any sacrifice of the actual operation, etc. and is therefore quite desirable.

[0044] As is apparent from the relationship between the bit trains and gray-scale voltages shown in Figs. 6 and 7, the minimum gray-scale voltage #0 and the maximum gray-scale voltage #63 are used even for this 16-gray-scale displaying just as with the 64-gray-scale displaying. Then, gray-scale voltages are selected in such a way as to be ranked in substantially the same intervals between the minimum gray-scale voltage and the maxi-

mum gray-scale voltage. This embodiment realizes selections (ranking) of such gray-scale voltages in the above described higher-order 2-bit relocation format. Adopting such a format makes it possible to use both the maximum and minimum gray-scale voltages, and to make full use of the whole width of the gray-scale voltage range efficiently, thereby simply selecting gray-scale voltages ranked in substantially the same intervals in the voltage range.

[0045] This embodiment is intended to select gray-scale voltages during 16-gray-scale displaying in the higher-order 2-bit relocation format, but there are also other selection methods. Fig. 8 shows a configuration of a gray-scale voltage producing circuit 2' according to such a modified selection method, wherein the same components as those in Fig. 4 are assigned the same reference symbols.

[0046] The configuration in Fig. 8 differs from that in Fig. 4 in that an amplifier A_{63} is selected as an amplifier to be constantly powered so as to provide constant output of the maximum voltage V_{63} and further amplifiers to be constantly powered are selected every four voltage lines using the amplifier A_{63} as the reference. This difference is made clear in Figs. 9 and 10.

[0047] As in the cases of Figs. 6 and 7, Figs. 9 and 10 show the format of a pixel data block D_n with an example of gray-scale voltages to be selected and a decoding rule of the decoding and selection circuit. In Fig. 9, basically without destroying the above-described block format during the 64-gray-scale displaying, four bits Q_3 , Q_2 , Q_1 , and Q_0 each having an arbitrary binary value are sequentially located from the MSB side in the block and at the same time a fixed value "11" is assigned to the two bit positions on the LSB side in the same block (maximum-base lower-order bit fixed format). Fig. 10 shows data processing carried out when six bits Q_5 , Q_4 , Q_3 , Q_2 , Q_1 and Q_0 are supplied as the input pixel data block in the case of forced 16-gray-scale displaying. In the processing, the original higher-order bit train Q_5 , Q_4 , Q_3 and Q_2 remains unchanged, while a fixed value "11" is assigned to the lower bits instead of the lower-order bit train Q_1 and Q_0 (maximum-base lower-order bit fixed format, again).

[0048] According to this, when the higher-order 4-bit train indicates a maximum value, the 6-bit block indicates a maximum value, but even if the higher-order 4-bit train indicates a minimum value, the 6-bit block does not indicate a minimum value. Furthermore, as in the cases of Figs. 6 and 7, during the forced 16-gray-scale displaying, the same 16-gray-scale voltages can be designated for both cases of 6-bit data input and 4-bit data input as a result.

[0049] As is apparent from these examples, the gray-scale voltages whose ranking diminishes just every 4 steps from the maximum gray-scale voltage #63 downward are selected. For a comparison between this case and the cases in Figs. 6 and 7, seeing Fig. 11 is desired. Fig. 11 shows ranking of gray-scale voltages within the

overall gray-scale voltage range (this is an example where the gray-scale voltage changes completely linearly). Black bullets indicate gray-scale voltages according to the higher-order 2-bit relocation format in Figs. 6 and 7, white bullets gray-scale voltages according to the maximum-base two lower-order bit fixed format in Figs. 9 and 10. As is apparent from this, the former adopts both the maximum value and minimum value within the gray-scale voltage range for the gray-scale voltages, and selects gray-scale voltages positioned in substantially the same intervals within the range as the other gray-scale voltages. In contrast, the latter adopts the maximum value as the gray-scale voltage, and selects gray-scale voltages positioned in completely equal intervals within the voltage range from the maximum value using the maximum value as the reference as the other gray-scale voltages.

[0050] The former is more advantageous in the sense that a certain limited voltage range is effectively used and no gray-scale display range is sacrificed (allowing a more comprehensive intermediate tone expression as a result). However, depending on the system applied, there is also a possibility that relocation processing of the higher-order two bits in the former may complicate the configuration, for example, require a memory function specific to that processing, and therefore the latter may also be advantageous in terms of simplification of data processing. Furthermore, in the latter, intermediate tone displaying corresponding to the gray-scale voltages #0, #1 and #2 is discarded during the 16-gray-scale displaying, but the lowest gray-scale voltage #3 is as low as negligible and switching from the 64-gray-scale displaying to the 16-gray-scale displaying would originally mean that the intermediate tone to be displayed becomes rougher, and therefore this discarding does not matter in many cases.

[0051] Furthermore, as a further modification example instead of the configuration in Fig. 8, the amplifier A_0 may be selected as an amplifier to be constantly powered so as to keep the fixed output of the minimum voltage V_0 as a specific gray-scale voltage and amplifiers which are constantly powered and output other specific gray-scale voltages may be selected for every four voltage lines using the amplifier A_0 as the reference.

[0052] Fig. 12 shows a configuration of a gray-scale voltage producing circuit 2" according to such a modification example and the same components as those in Fig. 4 are assigned the same reference symbols.

[0053] In Fig. 12, the amplifier A_0 is selected as the amplifier to be constantly powered so as to make the fixed output of the minimum voltage V_0 instead of the maximum voltage V_{63} and amplifiers which are constantly powered are selected for every four voltage lines using the amplifier A_0 as the reference. This is made clear in Figs. 13 and 14.

[0054] As in the cases of Figs. 6 and 7 or Figs. 9 and 10, Figs. 13 and 14 show a format of a pixel data block D_n , with an example of gray-scale voltages to be selected

and a decoding rule of the decoding and selection circuit. In Fig. 13, basically without destroying the above-mentioned block format during the 64-gray-scale displaying, four bits of Q_3 , Q_2 , Q_1 and Q_0 each having an arbitrary binary value are sequentially located from the MSB side in the block and at the same time a fixed value "00" is assigned to the two bit positions on the LSB side in the same block (minimum-base lower-order bit fixed format). Fig. 14 shows data processing carried out when six bits of Q_5 , Q_4 , Q_3 , Q_2 , Q_1 and Q_0 are supplied as the input pixel data block in the case of forced 16-gray-scale displaying, wherein and while the original higher-order bit train Q_5 , Q_4 , Q_3 and Q_2 remains unchanged, a fixed value "00" is now assigned instead of the lower-order bit train Q_1 , Q_0 (minimum-base lower-order bit fixed format, again).

[0055] According to this, when the higher-order 4-bit train indicates a minimum value, the 6-bit block indicates a minimum value, but even if the higher-order 4-bit train indicates a maximum value, the 6-bit block does not indicate a maximum value. Furthermore, as in the case of the foregoing examples, during the forced 16-gray-scale displaying, the same 16-gray-scale voltages can be designated for both cases of 6-bit data input and 4-bit data input as a result.

[0056] According to this example, gray-scale voltages whose ranking increases just every 4 steps from the minimum gray-scale voltage #0 upward are selected. In reference to Fig. 11, all white bullets in the cases of Figs. 8 to 10 are shifted 4 steps toward the origin on the straight line.

[0057] Therefore, this is advantageous in simplifying data processing as in the cases of Figs. 8 to 10. Furthermore, intermediate tone displaying corresponding to the gray-scale voltages #63, #62 and #61 is discarded during the 16-gray-scale displaying, but the highest gray-scale voltage #60 is sufficiently high and these voltages can be ignored, and therefore this example is sufficiently practical.

[0058] The explanations so far have described examples where the lower-order bits are fixed to "11" and "00" in the lower-order bit fixed format, but other values such as "01" and "10" can also be fixed as the lower-order bits. That is, with these lower-order bits of "01" and "10", neither the maximum-base nor the minimum-base as described above is obtained, but a format is provided wherein a value slightly deviating from the maximum value or minimum value is the reference. This means a common feature in respect that specific gray-scale voltages are selected in equal intervals by determining one reference value so that much the same effects and advantages can be obtained.

[0059] The data arrangement processing in the above-described higher-order bit relocation format and lower-order bit fixed format can be carried out with appropriate means provided on the supply source side of the data sequence "data".

[0060] Fig. 15 illustrates such an example, wherein a

data processing circuit 9 whose input is applied with the data sequence "data" is provided before the data conversion circuit 1. The data processing circuit 9 basically receives the control signals 4s and 4f, then processes the 6-bit train or 4-bit train of the input data train "data" in the higher-order bit relocation format or lower-order bit fixed format in accordance with these control signals to always generate a 6-bit output data train and to transfer the data train to the data conversion circuit 1. This has an advantage that the data conversion circuit 1 and the selection circuits 30 to 3x are not required to change according to the present invention.

[0061] Alternatively, since the decoding rule itself of the selection circuits 30 to 3x is certain, it is also possible to provide an arrangement immediately before the selection circuit, which, for example, switches to a mechanism to make up 2 missing bits for a 6-bit selection control signal in the case of 4-bit data in response to the control signal 4s, thus implementing equivalent data processing.

[0062] Fig. 16 shows such an example and illustrates part of a system implementing data processing in the higher-order bit relocation format of Figs. 6 and 7. Here, the system is provided with selectors 91 and 92 which receive the LSB side 2 bits of the 6 bits of the output of the data conversion circuit 1 as their inputs, respectively and receive the MSB side 2 bits as their other inputs, respectively and further receive the above-described control signal C_0 as their control inputs. Furthermore, the higher-order 4-bit outputs of the data conversion circuit 1 are directly coupled with the higher-order 4-bit inputs for selection control of the selection circuit on one hand, and the outputs of the selectors 91 and 92 are supplied to the lower-order 2-bit inputs for selection control of the selection circuit, respectively, on the other. The selectors 91 and 92 can select and output either one input according to the above-described control signal C_0 , and can thereby select and output the MSB side 2 bits of the output 6 bits of the data conversion circuit 1 during the normal/forced 16-gray-scale displaying and attain the higher-order bit relocation.

[0063] By the way, Fig. 16 only illustrates the configuration of one selection circuit (the first selection circuit 30), but the same configuration applies to other selection circuits. Furthermore, in the case of the lower-order bit fixed format, predetermined fixed bits such as "11" bits, etc. may be used as the other inputs of the selectors 91 and 92.

[0064] There may be a number of other embodiments for adapting the selection circuits to changes in the output fashion of the gray-scale voltage producing circuit 2 due to the switching of the number of displayed gray-scale (e.g., data processing, etc. in the data conversion circuit 1).

[0065] Fig. 17 shows a gray-scale voltage producing circuit 2A used for the source driver of another embodiment according to the present invention.

[0066] In Fig. 17, the base gray-scale voltage V_s from the (preceding) voltage producing section 40 (see Fig.

1) is divided by coarse potential divider circuits based on series circuits of resistors R_{63} , R_{62-59} , R_{58-55} , ..., R_{3-0} formed between the power supply point and grounding point. As shown in Fig. 17, the common connection points of these potential dividing resistors and the grounding point are led out as taps and 16 coarsely divisional voltages (basic gray-scale voltages) V_0 , V_4 , ..., V_{55} , V_{59} , V_{63} are obtained from these tap outputs, respectively. These coarsely divisional voltages are inputted to 16 buffer amplifiers A_0' , A_4' , ..., A_{55}' , A_{59}' , A_{63}' , respectively. These amplifiers perform predetermined amplification on the input divisional voltages while securing impedance matching with the corresponding column electrodes as with the above-mentioned embodiments, and supply outputs as gray-scale voltages #0, #4, ..., #55, #59, #63.

[0067] Fine control potential divider circuits D_{4-0} , ..., D_{59-55} , D_{63-59} based on series circuits made up of 4 or 5 resistors are formed between an output line of one buffer amplifier and that of the next buffer amplifier. Furthermore, both ends of these fine potential divider circuits are connected to the output lines of the amplifiers through switching circuits SW_0 , SW_{4L} , SW_{4H} , ..., SW_{55L} , SW_{55H} , SW_{59L} , SW_{59H} and SW_{63} . Each switching circuit is controlled to ON/OFF by a control signal C_0 which may be equivalent to the control signal in the foregoing embodiment.

[0068] When the respective switching circuits are closed, the gray-scale voltages #4, ..., #55, #59 and #63 are divided by the fine potential divider circuits. As shown in Fig. 17, the common connection points of these potential divider resistors in the fine divider circuits are led out as taps, and the finely divisional voltages (intermediate gray-scale voltages) #1 to #3, ..., #56 to #58, #60 to #62 each having a value between the above-described coarsely divisional voltages are obtained from these tap outputs, respectively. These finely divisional voltages are supplied to the column electrodes together with the outputs #0, #4, ..., #55, #59 and #63 of the above-described coarsely divisional voltages V_0 , V_4 , ..., V_{55} , V_{59} , and V_{63} .

[0069] This embodiment is intended to directly supply the outputs of the amplifiers to the column electrodes for the predetermined 16 gray-scale voltages, and to obtain other gray-scale voltages by (more finely) dividing the predetermined gray-scale voltages while electrically isolating the fine potential divider circuits from this gray-scale voltage producing circuit using the switching circuits when the other gray-scale voltages are unnecessary.

[0070] According to such configuration, turning OFF the switching circuits prevents the fine potential divider circuits from being load on the amplifiers during 16-gray-scale displaying, and therefore the amplifiers need not supply currents to the fine potential divider circuits. This allows the effect of reducing power consumption to be exhibited as in the case of the aforementioned embodiments.

[0071] This embodiment is also based on the aforementioned higher-order bit relocation format. That is,

specific gray-scale voltages outputted through the amplifiers are gray-scale voltages with the ranking numbers shown in Figs. 6 and 7 and other gray-scale voltages are based on the divisional outputs of the fine potential divider circuits corresponding to the other ranking numbers.

[0072] The configuration of this embodiment may also be modified to a configuration based on the maximum-base lower-order bit fixed format mentioned already. Fig. 18 shows a gray-scale voltage producing circuit 2A' according to this modification. The configuration in Fig. 18 complies with the maximum-base lower-order 2-bit fixed format shown in Figs. 9 and 10, but instead of this format, not only the minimum-base lower-order 2-bit fixed format shown in Figs. 13 and 14 but also other formats as based on the lower-order bit fixed format may be used. Those configurations are obvious for those skilled in the art from the above description.

[0073] In the above embodiment, the control signal 4s as an operating mode signal can be received, e.g. by providing an external input terminal for the driving circuit as means for supplying the signal 4s. This makes it possible to introduce therein a signal being obtained from the CPU or the like in the display device and being indicative of a state corresponding to the number of gray-scale levels to be displayed.

[0074] Furthermore, the control signal 4f as a forced mode signal can also be received in the same manner and the user can perform input operation to set, for example, a simple display (power-saving) mode to determine a state of the signal 4f. Alternatively or in addition, when the CPU or the like in the display device determines that the amount of its battery charge is equal to or lower than a predetermined level, it may make this control signal 4f active so as to automatically change the operating mode to a forced simple display (power-saving) mode.

[0075] Up to this point, representative embodiments and their modifications have been described, but the present invention is not limited to them and it goes without saying that a variety of modified embodiments can also be found. For example, the gray-scale voltages need not follow the pattern as shown in Fig. 11, but can also take values having a predetermined compensation characteristic and the present invention is applicable not only to a case of 64- and 16-gray-scale voltages but also to a case where the different number of gray-scale voltages are generated.

[0076] The present invention is not limited to two kinds of display modes and may be intended to electrically isolate output circuits for similarly appropriate gray-scale voltages for the respective display modes of, for example, 64-gray-scale levels, 32-gray-scale levels and 16-gray-scale levels, etc. In this case, such electrical isolation is performed hierarchically.

[0077] Fig. 19 shows an arrangement of the data block Dn in displaying of 3-bit pixel data according to the higher-order bit relocation format, that is, the 8-gray-scale displaying and the resultant ranking numbers for the specific gray-scale voltages. In this example, all three input bits

are assigned to the three bits which are missing in the six bits that make displaying the maximum number of gray-scale levels in the display device. Fig. 20 also shows an arrangement of the data block Dn in displaying of 2-bit pixel data according to the same higher-order bit relocation format, that is, the 4-gray-scale displaying and the resultant ranking numbers for the specific gray-scale voltages. In this example, two input bits are assigned to the missing four bits twice repeatedly. Fig. 21 further shows an arrangement of the data block Dn in displaying of 1-bit pixel data according to yet the same higher-order bit relocation format, that is, the 2-gray-scale displaying and the resultant ranking numbers of the specific gray-scale voltages. In this example, one input bit is assigned to all the five bits which are missing. Not only the higher-order bit relocation format but also the lower-order bit fixed format may be adopted for each display mode.

[0078] Figs. 22 and 23 shows a specific example of the gray-scale voltage producing circuit supporting multi-stepwise displaying.

[0079] This configuration supports the switching between different numbers of steps with 6-, 4-, 3- and 1-bit pixel data and a forced power-saving display mode. This configuration is also an expansion of the previously mentioned configuration in Fig. 4 and adopts the higher-order bit relocation format.

[0080] This gray-scale voltage producing circuit 2m uses control signals C₆, C₄, C₃ and C₁ which become active for the display manners of 6-, 4-, 3- and 1-bit pixel data, respectively and a control signal C_x which becomes active in the forced display mode. These control signals are prescribed as in the table shown in Fig. 24. This table expresses the followings: any one of the control signals C₆, C₄, C₃ and C₁ becomes active (high level) in correspondence with the number of gray-scale levels to be represented in a normal display mode (when the control signal C_x is non-active); and the control signal C_x becomes active (high level) in a forced display mode, indicating that the number of gray-scale levels to be represented should be set to 2 irrespective of states of the other control signals.

[0081] Figs. 22 and 23 show the case where only amplifiers necessary for a display mode specified are operated according to those control signals. Verification of Figs. 6, 19 and 21 is helpful to understand. By the way, pixel data are processed in order to obtain appropriate control signals for the selection circuits 30 to 3x in the forced mode, too. This is apparent from the above descriptions.

[0082] Thus, even if the gray-scale levels to be represented are divided into three or more stages, it is possible to realize appropriate (fine) power-saving according to each stage.

[0083] The configuration in Figs. 22 and 23 may be replaced by a configuration shown in Figs. 25 and 26.

[0084] This configuration supports multi-stepwise switching of the number of gray-scale levels with 6-, 4-, 3- and 1-bit pixel data and a forced power-saving display

mode. This configuration is an expansion of the configuration in Fig. 17 mentioned above, and adopts the higher-order bit relocation format.

[0085] This gray-scale voltage producing circuit 2mA also uses the similar control signals C_6 , C_4 , C_3 , C_1 and C_x , and supplies outputs of amplifiers on the upstream side only to potential divider circuits necessary for the specified display mode. This example should also be understood together with Figs. 6, 19, 21 and 24.

[0086] In the above embodiments, if pixel data with e.g. a full number of bits are inputted in the forced mode, the processing as shown in Figs. 7, 10 and 14 (processing of decimating values indicated by the train of a greater number of bits) is performed to reduce the number of gray-scale levels to be selected while the gray-scale voltage producing circuit electrically isolates circuit elements for producing gray-scale voltages other than those to be selected. However, a forced mode for appropriate power-saving can be accomplished even without performing such decimation processing.

[0087] Fig. 27 shows a configuration to realize such a forced mode. This gray-scale voltage producing circuit 2B is worth that obtained by modifying the configuration in Fig. 17. According to this configuration, a control signal 4s for specifying a normal display mode is one input for an OR gate 202 and an AND gate 203, while a control signal 4f for specifying a forced display mode is the other input for the OR gate 202 and supplied to the other input of the AND gate 203 through an inverting gate 204. The output of the OR gate 202 is supplied to control inputs of upstream switching circuits SW_{4L} , ..., SW_{55L} , SW_{59L} , SW_{63} to which a higher potential of the respective fine potential divider circuits is applied. The output of the AND gate 203 is supplied to control inputs of downstream switching circuits SW_{0L} , SW_{4H} , ..., SW_{55H} , SW_{59H} to which a lower potential of the respective fine potential divider circuits is applied.

[0088] In such a configuration, the output of the gate 202 becomes active (high level) when the control signal 4f becomes active (high level) and the upstream switching circuits turn ON, while the output of the gate 203 becomes non-active (low level) and the downstream switching circuits turn OFF. In this condition, each of the potential divider circuit no longer functions as the original potential divider circuit, and even if the upstream side switching circuits close a possible conducting path between the amplifier outputs, the downstream side switching circuits open the path, which prevents a current (due to the effect of potential division) from flowing through the fine potential divider circuits between the outputs of the amplifiers. And at this time, all the potential divisional output ends of the respective fine potential divider circuits will represent a voltage almost equal to the supply voltage on the upstream side. This is generally attributable to the fact that the divisional potential output ends are coupled with the column electrodes of the display device through the selection circuits 30 to 3x, while the capacitance component constitutes the main part of the load on the signal

route including the column electrodes and the dividing resistor component of the fine potential divider circuits is negligible.

[0089] For example, consider a case where a bit train of the input pixel data is "000001" in a forced mode. In this case, the corresponding selection circuit selects the voltage #1, but the downstream switch SW_0 is opened and the upstream switch SW_{4L} is closed in the potential divider circuit D_{4-0} corresponding to the value of the bit train, and therefore the output of #1 is output which has been passed through the resistors R_3 , R_2 and R_1 from the output of the amplifier A_4' . In contrast to this, the corresponding selection circuit performs a selection of the data "000001" without the decimation, and therefore selects the output of #1 as usual. However, this output #1 is coupled with a column electrode which extends much long in the display area through the selection circuit, so that a load of the conditions as described above is caused, whereby the resistors R_3 , R_2 and R_1 do not substantially form a potential divider circuit, and the voltage of #1 will be a voltage having nearly the same value as that of the output voltage of the amplifier A_4' . The partial drawing pointed by an arrow (i) in Fig. 27 shows this appearance. Likewise, a voltage having nearly the same value as that of the outputted voltage of the amplifier A_4' is outputted when the voltage of #2 or #3 is selected.

[0090] Thus, the selection circuit outputs the specific gray-scale voltage of #4 not only for data "000010" (corresponding to #4), but also for "000001" (corresponding to #1), "000010" (corresponding to #2) and "000011" (corresponding to #3). For other fine potential divider circuits, the specific gray-scale voltage on the upstream side is likewise outputted as an output divisional voltage. Hence, an appropriate forced display mode is attained without depending on the aforementioned decimation processing.

[0091] By the way, the same switching control may also be performed and the decimation processing may be omitted not only in the forced mode, but also in a normal 4-bit display mode. Such a modification example is shown in Figs. 28 and 29.

[0092] Fig. 28 shows a first example of a gray-scale voltage producing circuit 2C provided with only upstream side switching circuits and Fig. 29 shows a second example of a gray-scale voltage producing circuit 2D provided with only downstream side switching circuits. According to the first example, the upstream side switching circuits are opened in both the forced mode and the normal 4-bit display mode, and a low potential given to the potential divider circuit appears at their respective potential divider output ends at almost the same level. According to the other example, the downstream side switching circuits are opened in both the forced mode and the normal 4-bit display mode, and a high potential given to the potential divider circuit appears at their respective potential divider output ends at almost the same level. Moreover, neither of the two examples requires the decimation processing.

[0093] It goes without saying that the feature of setting the potential divider output ends to either the upstream side or downstream side specific gray-scale voltage is also applicable to the configuration in Fig. 18 and those in Figs. 25 and 26, and more.

[0094] Furthermore, the foregoing embodiments have been described only to the effect that gray-scale voltages are ranked in equal intervals, but the present invention is not limited to this. The extent of "substantially equal intervals" should be interpreted in a wider sense.

[0095] Furthermore, the foregoing embodiments have taken as examples cases where pixel signals are updated and outputted to the column electrodes for each row, that is, in line-sequence, but the present invention is not limited to the examples and they may be modified to a configuration in which the pixel signals are updated and outputted for each pixel or each predetermined displayed unit, that is, in dot-sequence. For example, in a part of source driver or an ancillary circuit coupled therewith in the display panel on which LTPS (low-temperature polysilicon)-based TFTs are formed, it goes without saying that in synchronization with or in response to serial input having a form in which a sequence of pixel information pieces as shown in "Input of S/P1" of Fig. 3 is supplied, serial output may be done in the same form of a sequence of pixel information pieces so as to drive the column electrodes in column-sequence. In this case, the data conversion circuit 1 may be unnecessary.

[0096] As an additional remark, the configuration of the gray-scale voltage producing circuit has been described as having two types; one based on operation/non-operation of amplifiers and the other based on output-enabling/disabling of potential divider circuits, but these two types can also be combined as appropriate.

[0097] As a further remark, the foregoing explanations have made for the case where an amplifier intervenes in the line of gray-scale voltage #0, but this amplifier may be omitted. Therefore, note that the present invention does not exclude such a case.

[0098] In addition, those skilled in the art can create any modifications for the present invention without departing from the scope of the protection described in the claims thereof.

[0099] It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item

of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. A column electrode driving circuit (50) for a display device having a matrix (20) of rows and columns of display segments, a display segment comprising at least one pixel (23) capable of gray-scale displaying, the driving circuit comprising:

gray-scale voltage producing means (2) including amplifiers ($A_0, A_1, A_2 \dots A_{63}$), each amplifier having a first input for receiving one value of a range of a plurality of gradually increasing gray-scale voltage values, and having an amplifier output for delivering an output signal in proportion to the voltage level at the input; and selecting means (30, 31 ... 3x) having inputs coupled to the outputs of the amplifiers for selecting and outputting any of the output signals of the amplifiers for each display segment in a row that is being addressed in accordance with an image signal indicative of a gray-scale level to be generated by the display segment, the driving circuit being **characterized in that** it can operate in a predetermined mode, wherein the gray-scale voltage producing means (2) power on a predetermined number of amplifiers, which correspond to a predetermined number of predetermined gray-scale values within the range, and power off the other amplifiers, and the selecting means select the output signals of the amplifiers which are powered on.

2. The column electrode driving circuit as defined in claim 1, wherein the predetermined mode includes a plurality of sub-modes, and the amplifiers to be powered on are determined for each sub-mode by the gray-scale voltage producing means.

3. The column electrode driving circuit as defined in claim 1 or 2, further comprising means for receiving a control signal for designating a content of the predetermined mode, the gray-scale voltage producing means performing power control on a power supply of the amplifiers in accordance with the control signal.

4. The column electrode driving circuit as defined in any of the preceding claims, wherein specific gray-scale voltage values applied to amplifiers to be powered on are assigned gray-scale voltage values within the range of voltage values between a minimum gray-scale voltage value and a maximum gray-scale

voltage value, which have been selected in accordance with the predetermined mode.

5. The column electrode driving circuit as defined in claim 4, wherein the specific gray-scale voltage values include the maximum gray-scale voltage value and/or the minimum gray-scale voltage value. 5
6. The column electrode driving circuit as defined in claim 4, wherein the specific gray-scale voltage values are assigned gray-scale voltage values which are a subset of the range of voltage values having substantially an equal difference between two subsequent values of the subset. 10
7. The column electrode driving circuit as defined in any of the preceding claims, further comprising data processing means for converting an input bit train comprising a sequence of groups of bits, each group of bits determining a gray level of an image point of the image, for each display segment a corresponding image point being present, of an input image signal into a new bit train having only groups of bits corresponding to the predetermined gray-scale values designated by the predetermined mode; the selecting means performing selection based on the image signal, being the new bit train. 15
8. The column electrode driving circuit as defined in claim 7, **characterized in that** the data processing means form the new bit train using a content of at least one higher-order bit of the input bit train for its lower-order bit. 20
9. The column electrode driving circuit as defined in claim 7, **characterized in that** the data processing means form the new bit train using a fixed value of at least one bit for its lowerorder bit. 25
10. A driving circuit as defined in claim 8, **characterized in that** the data processing means form the new bit train such that the bit train can have a value capable of designating a maximum gray-scale voltage and/or a minimum gray-scale voltage. 30
11. A column electrode driving circuit (50) for a display device (20) capable of gray-scale displaying, comprising: 35

gray-scale voltage producing means (30) including amplifiers (A_0' , A_1' , A_2' ... A_{63}') which relay a plurality of gray-scale voltages having values that are gradually level-shifted, respectively, and potential divider circuits (R_0 , R_1 ... R_{63}) coupled between outputs of the amplifiers for dividing their output voltages to produce finer gray-scale voltages; and selecting means (30, 31 ... 3x) for selecting and

outputting any of the gray-scale voltages for each pixel or each predetermined displayed unit in accordance with an image signal indicative of a gray-scale level for the pixel or displayed unit, the driving circuit being **characterized in that** it can operate in a predetermined mode, wherein the gray-scale voltage producing means output-disables any potential divider circuits that produce a predetermined number of gray-scale voltages which correspond to predetermined gray-scale levels by electrically isolating the subject potential divider circuit from corresponding amplifiers or from one of the amplifiers, thereby avoiding an output current of that amplifier from flowing through the fine potential divider circuits, and the selecting means selecting any of effective voltages during the predetermined mode.

12. The column electrode driving circuit as defined in claim 11, **characterized in that** the predetermined mode includes a plurality of sub-modes, and the potential divider circuits to be output-enabled are determined for each sub-mode in the gray-scale voltage producing means. 40
13. The column electrode driving circuit as defined in claim 11 or 12, **characterized in that** the driving circuit comprises means for receiving a control signal for designating a content of the predetermined mode, and the gray-scale voltage producing means perform output-disablement/enablement control on the potential divider circuits in accordance with the control signal. 45
14. The column electrode driving circuit as defined in any of claims 11 to 13, **characterized in that** the divider circuits have a first connection end given a higher potential and a second connection end given a lower potential for dividing a potential difference between the first and second connection ends, the connection ends being coupled between output lines of the amplifiers, at least one of the connection ends being coupled to the output line via a switching circuit that causes a conducting path between the output lines to be opened or closed, the switching circuit performing open-control on the path at the time when output of the divider circuit is disabled. 50
15. The column electrode driving circuit as defined in any of claims 11 to 14, **characterized in that** the divider circuits have a first connection end given a higher potential and a second connection end given a lower potential for dividing a potential difference between the first and second connection ends, the connection ends being coupled between output lines of the amplifiers, only one of the connection ends being coupled to the output line via a switching circuit 55

that causes a conducting path between the output lines to be opened or closed, the switching circuit performing open-control on the path at the time when output of the divider circuit is disabled.

16. The column electrode driving circuit as defined in claim 1, **characterized in that** the predetermined mode has at least one mode to represent a less number of gray-scale levels than the maximum number of gray-scale levels.
17. The column electrode driving circuit as defined in claim 16, **characterized in that** the predetermined mode includes a mode to represent a necessary number of gray-scale levels for display operation and a mode to represent gray-scale levels forcedly designated.
18. A display device comprising a display panel; and a column electrode driving circuit (50) as defined in any of the preceding claims.
19. The display device according to claim 18, wherein contents of the predetermined mode are defined in accordance with a waiting state of the display device, that is if the display device is in an active state, using all available gray scale levels or if the display device is in a waiting state, using a reduced number of gray scales.

Patentansprüche

1. Spaltenelektroden - Treiberschaltung (50) für eine Displayeinrichtung mit einer Matrix (20) aus Zeilen und Spalten von Displaysegmenten, wobei ein Displaysegment zumindest ein Pixel (23) umfasst, das zu einer Grauwertanzeige in der Lage ist, welche Treiberschaltung umfasst:

Grauwertspannungs-Erzeugungsmittel (2) mit Verstärkern ($A_0, A_1, A_2, \dots, A_{63}$), wobei jeder Verstärker einen ersten Eingang, um einen Wert aus einem Bereich einer Mehrzahl von allmählich ansteigenden Grauwertspannungswerten zu empfangen, und einen Verstärkerausgang aufweist, um ein Ausgangssignal im Verhältnis zu dem Spannungspegel am Eingang abzugeben; und
Auswahlmittel (30, 31, ... 3x), die Eingänge aufweisen, die mit den Ausgängen der Verstärker verbunden sind, um irgendeines der Ausgangssignale der Verstärker für jedes Displaysegment in einer gerade adressierten Zeile in Entsprechung zu einem Bildsignal, das einen von dem Displaysegment zu erzeugenden Grauwertpegel bezeichnet, auszuwählen und auszugeben,

wobei die Treiberschaltung **dadurch gekennzeichnet ist, dass**

diese in einem vorbestimmten Modus betrieben werden kann, in welchem die Grauwertspannungs-Erzeugungsmittel (2) eine vorbestimmte Anzahl von Verstärkern anschalten, die einer vorbestimmten Anzahl von vorbestimmten Grauwertwerten innerhalb des Bereiches entsprechen, und die anderen Verstärker ausschalten, und
die Auswahlmittel die Ausgangssignale der Verstärker auswählen, die angeschaltet werden.

2. Spaltenelektroden-Treiberschaltung nach Anspruch 1, wobei die vorbestimmte Betriebsart eine Mehrzahl von Unterbetriebsarten umfasst, und die anzuschaltenden Verstärker für jede Unterbetriebsart von den Grauwertspannungs-Erzeugungsmitteln festgelegt werden.
3. Spaltenelektroden-Treiberschaltung nach Anspruch 1 oder 2, weiterhin umfassend Mittel, um ein Steuersignal zum Bestimmen des Inhalts der vorbestimmten Betriebsart zu empfangen, wobei die Grauwertspannungs-Erzeugungsmittel auf eine Spannungsversorgung der Verstärker in Entsprechung zu dem Steuersignal eine Spannungssteuerungs-Kontrolle ausüben.
4. Spaltenelektroden-Treiberschaltung nach einem der vorhergehenden Ansprüche, wobei bestimmte Grauwertspannungswerte, die an die anzuschaltenden Verstärker angelegt werden, Grauwertspannungswerten innerhalb des Bereichs von Spannungswerten zwischen einem minimalen Grauwertspannungswert und einem maximalen Grauwertspannungswert zugeordnet sind, die in Entsprechung zu der vorbestimmten Betriebsart ausgewählt wurden.
5. Spaltenelektroden-Treiberschaltung nach Anspruch 4, wobei die bestimmten Grauwertspannungswerte den maximalen Grauwertspannungswert und/oder den minimalen Grauwertspannungswert umfassen.
6. Spaltenelektroden-Treiberschaltung nach Anspruch 4, wobei die bestimmten Grauwertspannungswerte Grauwertspannungswerten zugeordnet sind, bei denen es sich um einen Untersatz aus dem Bereich von Spannungswerten handelt, bei denen eine im Wesentlichen gleiche Differenz zwischen zwei aufeinander folgenden Werten des Untersatzes vorliegt.
7. Spaltenelektroden-Treiberschaltung nach einem der vorhergehenden Ansprüche, weiterhin umfassend ein Datenverarbeitungsmittel, um eine Eingangsbitfolge, die eine Sequenzfolge von Gruppen von Bits umfasst, wobei jede Gruppe von Bits einen

Grauepegel eines Bildpunktes des Bildes festlegt, und zwar für jedes Displaysegment eines entsprechenden vorliegenden Bildpunktes, eines Eingangsbildsignal in eine neue Bitfolge umwandelt, die nur Bits von Gruppen aufweist, die den vorbestimmten Grauwertwerten entsprechen, die von der vorbestimmten Betriebsart zugewiesen werden; wobei das Auswahlmittel eine Auswahl basierend auf dem Bildsignal vornimmt, welches die neue Bitfolge ist.

8. Spaltenelektroden-Treiberschaltung nach Anspruch 7, **dadurch gekennzeichnet, dass** das Datenverarbeitungsmittel die neue Bildfolge unter Verwendung des Inhalts von zumindest einem Bit höherer Ordnung der Eingangsbitfolge für deren Bit niedrigerer Ordnung bildet.

9. Spaltenelektroden-Treiberschaltung nach Anspruch 7, **dadurch gekennzeichnet, dass** das Datenverarbeitungsmittel die neue Bitfolge unter Verwendung eines Festwerts von zumindest einem Bit für ihr Bit niedrigerer Ordnung bildet.

10. Spaltenelektroden-Treiberschaltung nach Anspruch 8, **dadurch gekennzeichnet, dass** das Datenverarbeitungsmittel die neue Bitfolge so bildet, dass die Bitfolge einen Wert aufweisen kann, der eine maximale Grauwertspannung und/oder eine minimale Grauwertspannung zuweisen kann.

11. Spaltenelektroden-Treiberschaltung (50) für eine Displayeinrichtung (20), die zu einer Grauwertanzeige in der Lage ist, umfassend:

Grauwertspannungs-Erzeugungsmittel (30) mit Verstärkern ($A_0', A_1', A_2', \dots, A_{63}'$), die eine Mehrzahl von Grauwertspannungen weitergeben, die Werte aufweisen, die jeweils allmählich im Pegel verschoben sind, sowie Spannungsteilerschaltungen ($R_0, R_1, R_2, \dots, R_{63}$) die zwischen die Ausgänge der Verstärker geschaltet sind, um deren Ausgangsspannungen zu teilen, um feiner geteilte Grauwertspannungen zu erzeugen; und

Auswahlmittel (30, 31, ..., 3x), um irgendeine der Grauwertspannungen für jedes Pixel oder jede vorbestimmte angezeigte Einheit in Entsprechung zu einem Bildsignal, das einen Grauwertpegel für das Pixel oder die angezeigte Einheit bezeichnet, auszuwählen und auszugeben, wobei die Treiberschaltung **dadurch gekennzeichnet ist, dass** diese in einer vorbestimmten Betriebsart betrieben werden kann, wobei die Grauwertspannungs-Erzeugungsmittel beliebige Spannungsteilerschaltungen im Ausgang sperren, die eine vorbestimmte Anzahl von Grauwertspannungen erzeugen, die vorbe-

stimmten Grauwertpegeln entsprechen, und zwar durch elektrisches Trennen der in Betracht kommenden Spannungsteilerschaltungen von entsprechenden Verstärkern oder von einem der Verstärker, um so zu vermeiden, dass ein Ausgangsstrom dieses Verstärkers durch die feineren Spannungsteilerschaltungen fließt, und die Auswahlmittel irgendeine der tatsächlichen Spannungen während der vorbestimmten Betriebsart auswählen.

12. Spaltenelektroden-Treiberschaltung nach Anspruch 11, **dadurch gekennzeichnet, dass** die vorbestimmte Betriebsart eine Mehrzahl von Unterbetriebsarten umfasst und die im Ausgang zu sperrenden Spannungsteilerschaltungen für jede Unterbetriebsart in den Grauwertspannungs-Erzeugungsmitteln bestimmt werden.

13. Spaltenelektroden-Treiberschaltung nach Anspruch 11 oder 12, **dadurch gekennzeichnet, dass** die Treiberschaltung Mittel umfasst, um ein Steuer- bzw. Kontrollsignal zu empfangen, um einen Inhalt der vorbestimmten Betriebsart fest zu bestimmen, und die Grauwertspannungs-Erzeugungsmittel eine Steuerung bzw. Kontrolle zum Ausgangssperren bzw. zur Ausgangsfreigabe auf die Spannungsteilerschaltungen in Entsprechung zu dem Steuer- bzw. Kontrollsignal ausüben.

14. Spaltenelektroden-Treiberschaltung nach einem der Ansprüche 11 bis 13, **dadurch gekennzeichnet, dass** die Treiberschaltungen ein erstes Verbindungsende, dem eine höhere Spannung zugewiesen ist, und ein zweites Verbindungsende, dem eine niedrigere Spannung zugewiesen ist, aufweisen, um eine Potentialdifferenz zwischen dem ersten und zweiten Verbindungsende zu teilen, wobei die Verbindungsenden zwischen Ausgangsleitungen der Verstärker geschaltet sind, zumindest eines der Verbindungsenden über einen Schaltkreis mit der Ausgangsleitung verbunden ist, welcher eine leitende Bahn zwischen den zu öffnenden oder zu schließenden Ausgangsleitungen bewirkt, wobei der Schaltkreis die Öffnungssteuerung auf der Bahn zu demjenigen Zeitpunkt ausübt, wenn ein Ausgang der Teilerschaltung gesperrt ist.

15. Spaltenelektroden-Treiberschaltung nach einem der Ansprüche 11 bis 14, **dadurch gekennzeichnet, dass** die Teilerschaltungen ein erstes Verbindungsende, dem eine höhere Spannung zugeordnet ist, und ein zweites Verbindungsende, dem eine niedrigere Spannung zugeordnet ist, aufweisen, um eine Spannungsdifferenz zwischen dem ersten und dem zweiten Verbindungsende zu teilen, wobei die Verbindungsenden zwischen Ausgangsleitungen

der Verstärker geschaltet sind, wobei nur eines der Verbindungsenden über einen Schaltkreis mit dem Verbindungsende verbunden ist, welcher eine leitende Bahn zwischen den zu öffnenden oder zu schließenden Ausgangsleitungen bewirkt, wobei der Schaltkreis eine Öffnungssteuerung auf der Bahn zu demjenigen Zeitpunkt bewirkt, wenn ein Ausgang der Teilerschaltung gesperrt ist.

16. Spaltenelektroden-Treiberschaltung nach Anspruch 1, **dadurch gekennzeichnet, dass** die vorbestimmte Betriebsart zumindest eine Betriebsart aufweist, um eine niedrigere Anzahl von Grauwertpegeln als die maximale Anzahl von Grauwertpegeln abzubilden. 5
17. Spaltenelektroden-Treiberschaltung nach Anspruch 16, **dadurch gekennzeichnet, dass** die vorbestimmte Betriebsart eine Betriebsart umfasst, um eine notwendige Anzahl von Grauwertpegeln für einen Anzeigevorgang abzubilden, sowie eine Betriebsart, um erzwungen bestimmte Grauwertpegel abzubilden. 10
18. Anzeigeeinrichtung mit einem Anzeigefeld; und einer Spaltenelektroden-Treiberschaltung (50) nach einem der vorhergehenden Ansprüche. 15
19. Anzeigeeinrichtung nach Anspruch 18, bei der Inhalte der vorbestimmten Betriebsart in Entsprechung zu einem Wartezustand der Anzeigeeinrichtung definiert sind, dass heißt dann, wenn sich die Anzeigeeinrichtung in einem aktiven Zustand befindet, sämtliche zur Verfügung stehender Grauwertpegel verwendet werden, oder dann, wenn sich die Anzeigeeinrichtung in einem Wartezustand befindet, eine reduzierte Anzahl an Grauwertwerten verwendet wird. 20

Revendications

1. Un circuit de commande d'électrode colonne (50) pour un afficheur ayant une matrice (20) de rangées et de colonnes de segments d'affichage, un segment d'affichage comportant au moins un pixel (23) capable d'afficher en niveaux de gris, le circuit de commande comprenant : 25
- des moyens (2) de génération de potentiels de niveaux de gris comprenant des amplificateurs ($A_0, A_1, A_2, \dots, A_{63}$), chaque amplificateur ayant une première entrée recevant une valeur d'une gamme d'une pluralité de valeurs graduellement croissantes de potentiels de niveaux de gris, et ayant une sortie d'amplificateur pour générer un signal de sortie en rapport avec le niveau de tension à l'entrée ; et 30

des moyens de sélection (30, 31, ... 3x) disposant d'entrées connectées aux sorties des amplificateurs afin de sélectionner et d'extraire n'importe lequel des signaux de sortie des amplificateurs pour chacun des segments d'affichage d'une rangée qui est adressée suivant un signal d'image représentatif d'un niveau de gris devant être produit par le segment d'affichage; le circuit de commande étant **caractérisé en ce qu'il** opère suivant un mode prédéterminé dans lequel les moyens (2) de génération de potentiels de niveaux de gris alimentent un nombre prédéterminé d'amplificateurs correspondant à un nombre prédéterminé de valeurs de niveaux de gris au sein de la gamme, et éteignent les autres amplificateurs ; et 35

les moyens de sélection sélectionnent les signaux de sorties des amplificateurs qui sont alimentés.

2. Le circuit de commande d'électrode colonne selon la revendication 1, dans lequel le mode prédéterminé comporte une pluralité de sous-modes, et les amplificateurs devant être alimentés sont déterminés pour chaque sous-mode par les moyens de génération de potentiels de niveaux de gris. 40
3. Le circuit de commande d'électrode colonne selon la revendication 1 ou 2, comportant en outre des moyens de réception d'un signal de commande pour désigner le contenu d'un mode prédéterminé, les moyens de génération de potentiels de niveaux de gris assurent la commande de l'alimentation des amplificateurs suivant le signal de commande. 45
4. Le circuit de commande d'électrode colonne selon l'une quelconque des revendications précédentes, dans lequel des valeurs spécifiques de potentiels de niveaux de gris qui sont appliquées aux amplificateurs à alimenter se voient affectées à des valeurs de potentiels de niveaux de gris au sein de la gamme de tensions entre une valeur minimale de potentiels de niveaux de gris et une valeur maximale de potentiels de niveaux de gris, lesquelles ont été sélectionnées suivant le mode prédéterminé. 50
5. Le circuit de commande d'électrode colonne selon la revendication 4, dans lequel les valeurs spécifiques de potentiels de niveaux de gris comporte la valeur maximale de potentiels de niveaux de gris et/ou la valeur minimale de potentiels de niveaux de gris. 55
6. Le circuit de commande d'électrode colonne selon la revendication 4, dans lequel les valeurs spécifiques de potentiels de niveaux de gris se voient affectées des valeurs de potentiels de niveaux de gris qui constituent un sous-ensemble de la gamme des

valeurs de potentiels dans lequel deux valeurs consécutives présentent un écart sensiblement constant.

7. Le circuit de commande d'électrode colonne selon l'une quelconque des revendications précédentes, comportant en outre des moyens de traitement de données pour la conversion d'un train de bit d'entrée comportant une séquence de groupes de bits, chacun des groupes de bits déterminant un niveau de gris d'un point image de l'image, un point image étant présent pour chaque segment d'affichage, d'un signal d'image d'entrée en un nouveau train de bits disposant uniquement de groupes de bits correspondant aux valeurs de gris prédéterminés identifiés par le mode prédéterminé ;
les moyens de sélection assurant la sélection sur la base du signal d'image qui est le nouveau train de bits. 5
10
15
20
8. Le circuit de commande d'électrode colonne selon la revendication 7, **caractérisé en ce que** les moyens de traitement de données génèrent le nouveau train de bits au moyen du contenu d'au moins un bit d'ordre le plus élevé du train de bit d'entrée pour son bit d'ordre le plus faible. 25
9. Le circuit de commande d'électrode colonne selon la revendication 7, **caractérisé en ce que** les moyens de traitement de données génèrent le nouveau train de bits en utilisant une valeur fixe d'un bit au moins de son bit d'ordre le plus faible. 30
10. Un circuit de commande tel que défini dans la revendication 8, **caractérisé en ce que** les moyens de traitement de données génèrent le nouveau train de bits de telle manière que le train de bits comporte une valeur permettant de désigner le potentiel maximum de niveau de gris et/ou le potentiel minimum de niveaux de gris. 35
40
11. Un circuit de commande d'électrode colonne (50) pour un afficheur (20) capable d'afficher en niveaux de gris, comportant :
des moyens (30) de génération de potentiels de niveaux de gris comprenant des amplificateurs (A'_0 , A'_1 , A'_2 , ... A'_{63}) qui relaient une pluralité de potentiels de niveaux de gris présentant des valeurs graduellement décalées, respectivement, et des circuits de diviseur de tension (R_0 , R_1 , R_2 , ... R_{63}) connectés entre les sorties des amplificateurs afin de diviser leur potentiel de sortie pour générer des potentiels de niveaux de gris plus fins ; et
des moyens de sélection (30, 31, ... 3x) pour sélectionner et extraire n'importe lequel des potentiels de niveaux de gris ou chaque unité pré- 45
50
55

déterminée qui est affichée en fonction d'un signal d'image représentatif d'un niveau de gris pour le pixel ou l'unité affichée, le circuit de commande étant **caractérisé en ce qu'il** peut fonctionner suivant un mode prédéterminé, dans lequel

les moyens de génération de potentiels de niveaux de gris désactivent la sortie des circuits diviseurs de tension qui produisent un nombre prédéterminé de potentiels de niveaux de gris correspondant à des niveaux de gris prédéterminés en isolant électriquement le diviseur de tension concerné des amplificateurs correspondants ou de l'un des amplificateurs, permettant ainsi d'éviter l'écoulement d'un courant de sortie de cet amplificateur dans les circuits fins de division de tension ; et

les moyens de sélection sélectionnent n'importe lesquels des potentiels effectifs dans le mode prédéterminé.

12. Le circuit de commande d'électrode colonne selon la revendication 11, dans lequel le mode prédéterminé comporte une pluralité de sous-modes, et les circuits diviseurs de tension à activer en sortie sont déterminés pour chaque sous-mode par les moyens de génération de potentiels de niveaux de gris.
13. Le circuit de commande d'électrode colonne selon la revendication 11 ou 12, comportant en outre des moyens de réception d'un signal de commande pour désigner le contenu d'un mode prédéterminé, les moyens de génération de potentiels de niveaux de gris assurent l'activation/désactivation en sortie des diviseurs de tension suivant le signal de commande.
14. Le circuit de commande d'électrode colonne selon l'une quelconque des revendications 11 à 13, **caractérisé en ce que** les circuits diviseurs présentent une première électrode de connexion supérieure recevant un potentiel élevé et une seconde électrode de connexion inférieure recevant un potentiel faible, afin de diviser la différence de potentiel entre les deux électrodes, les électrodes de connexion étant connectés aux lignes de sortie des amplificateurs, une au moins des électrodes de connexion étant connectée à la ligne de sortie via un circuit de commutation assurant un chemin de conduction entre les lignes de sortie devant être ouvertes ou fermées, le circuit de commutation assurant la commande d'ouverture du chemin au moment où la sortie du circuit diviseur est désactivée.
15. Le circuit de commande d'électrode colonne selon la revendication 11 à 14, **caractérisé en ce que** les circuits diviseurs présentent une première électrode de connexion supérieure recevant un potentiel élevé et une seconde électrode de connexion inférieure

recevant un potentiel faible, afin de diviser la différence de potentiel entre les deux électrodes, les électrodes de connexion étant connectés aux lignes de sortie des amplificateurs, une seule seulement des électrodes de connexion étant connectée à la ligne de sortie via un circuit de commutation assurant un chemin de conduction entre les lignes de sortie devant être ouvertes ou fermées, le circuit de commutation assurant la commande d'ouverture du chemin au moment où la sortie du circuit diviseur est désactivée.

16. Le circuit de commande d'électrode colonne selon la revendication 1, **caractérisé en ce que** le mode prédéterminé comporte au moins d'un mode de représentation d'un nombre inférieur de niveaux de gris que le nombre maximum de niveaux de gris. 5
17. Le circuit de commande d'électrode colonne selon la revendication 16, **caractérisé en ce que** le mode prédéterminé comporte un mode pour représenter un nombre nécessaire de niveaux de gris pour une opération d'affichage et un mode pour représenter des niveaux de gris désignés par défaut. 10 20
18. Un dispositif d'affichage comportant un panneau d'affichage, et un circuit de commande d'électrode colonne (50) tel que défini dans l'une quelconque des revendications précédentes. 25 30
19. Le dispositif d'affichage selon la revendication 18, dans lequel les contenus du mode prédéterminé sont définis selon un état d'attente du dispositif d'affichage, à savoir si le dispositif d'affichage est dans un état d'attente, utilisant tous les niveaux de gris disponibles, ou si le dispositif d'affichage est dans un état d'attente utilisant un nombre réduit de niveaux de gris. 35 40

40

45

50

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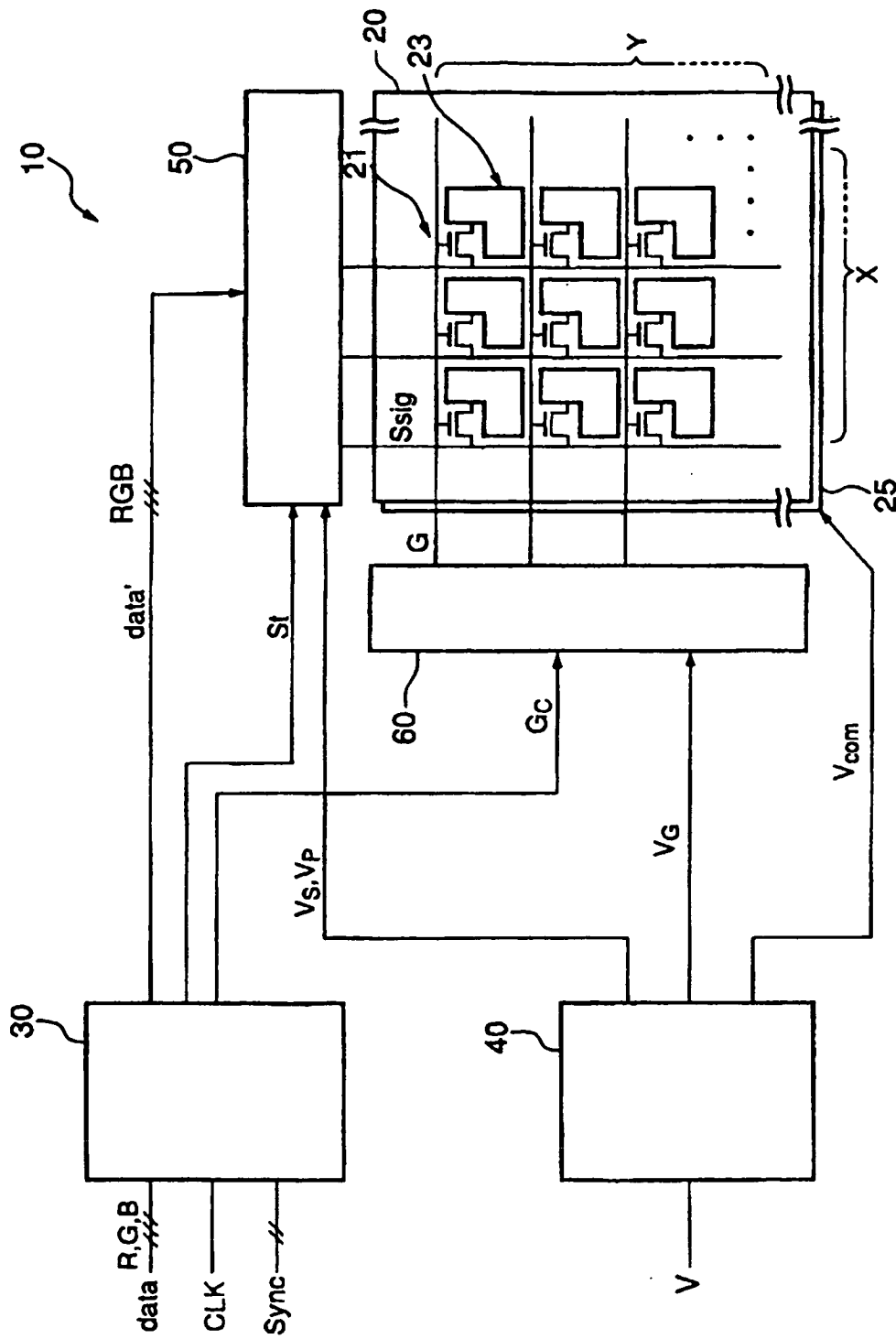


FIG.1

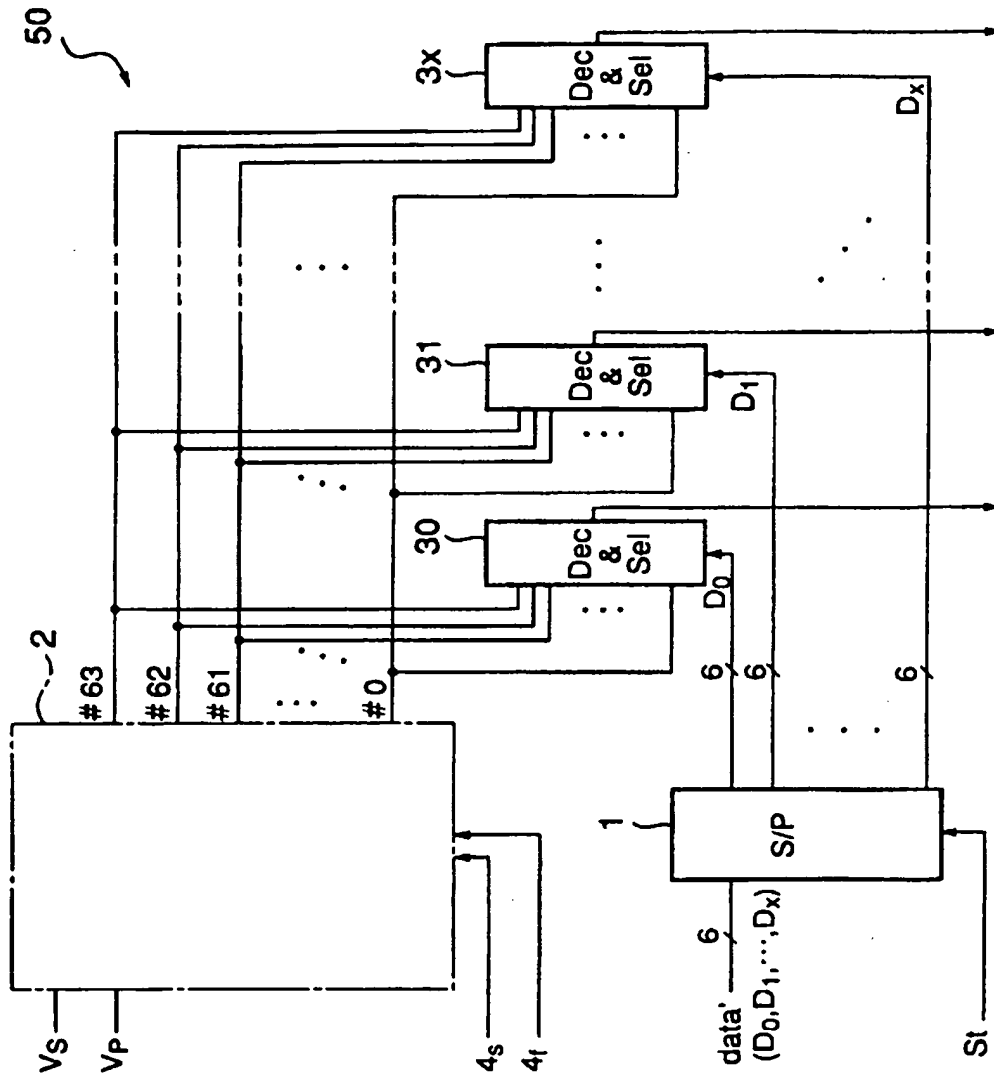


FIG. 2

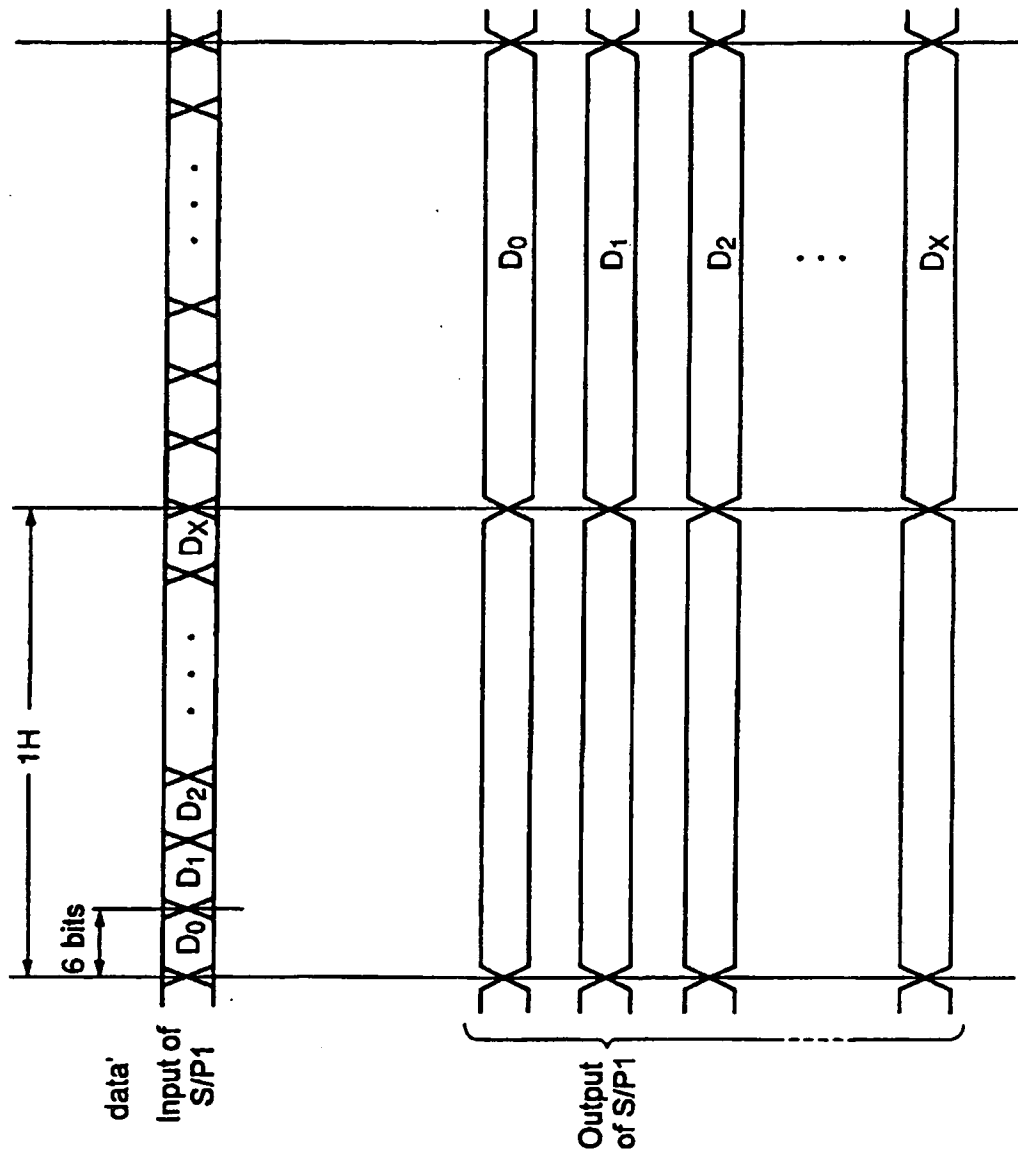


FIG.3

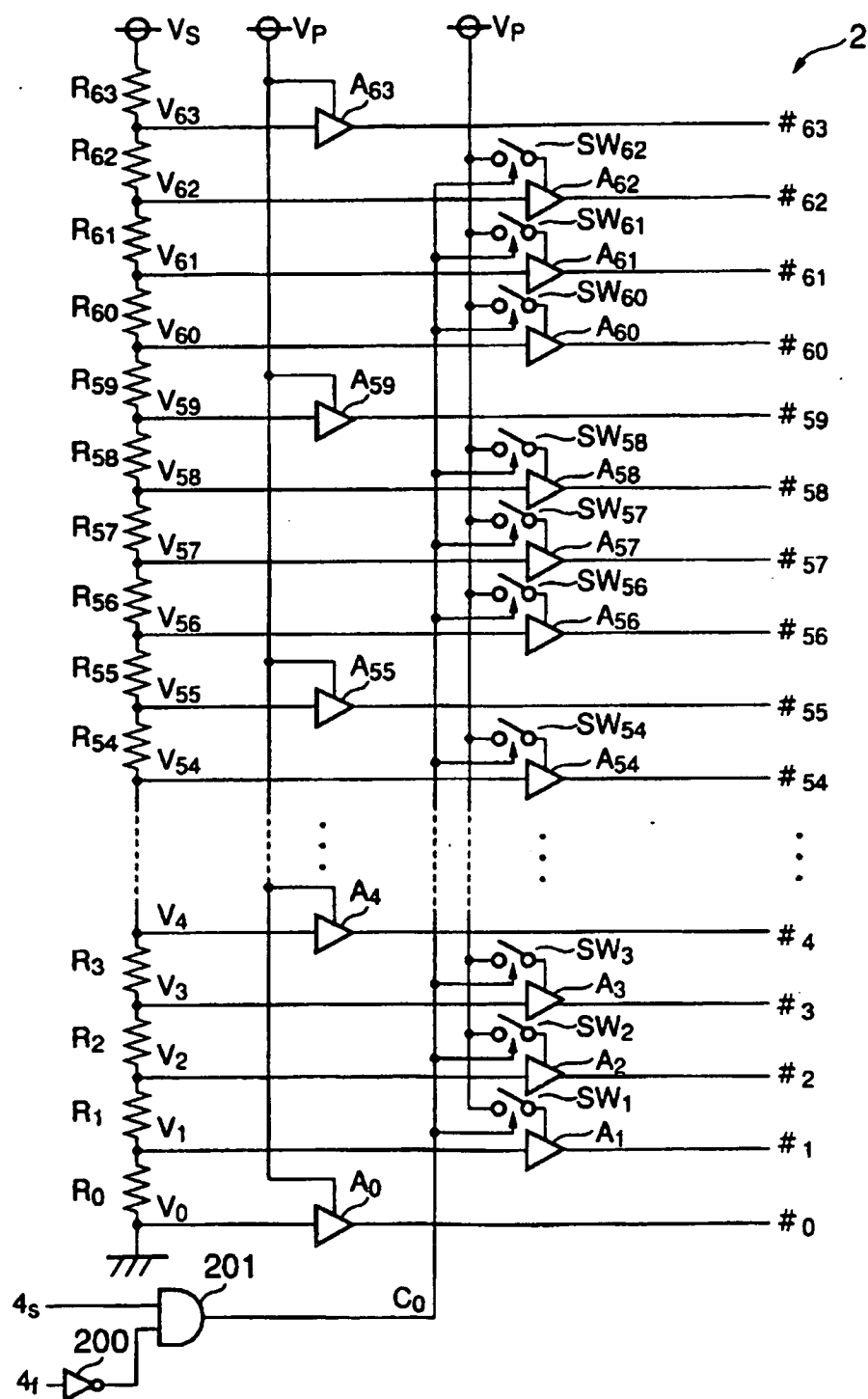
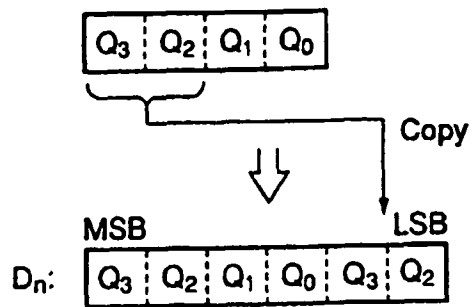


FIG. 4

D _n :	MSB			LSB			
	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀	
	0	0	0	0	0	0	#0
	0	0	0	0	0	1	#1
	0	0	0	0	1	0	#2
	0	0	0	0	1	1	#3
				.			.
				.			.
				.			.
	1	1	1	1	0	1	#61
	1	1	1	1	1	0	#62
	1	1	1	1	1	1	#63

FIG.5

4-bit Displaying



0	0	0	0	0	0	#0
0	0	0	1	0	0	#4
0	0	1	0	0	0	#8
0	0	1	1	0	0	#12
0	1	0	0	0	1	#17
0	1	0	1	0	1	#21
0	1	1	0	0	1	#25
0	1	1	1	0	1	#29
1	0	0	0	1	0	#34
1	0	0	1	1	0	#38
1	0	1	0	1	0	#42
1	0	1	1	1	0	#46
1	1	0	0	1	1	#51
1	1	0	1	1	1	#55
1	1	1	0	1	1	#59
1	1	1	1	1	1	#63

FIG.6

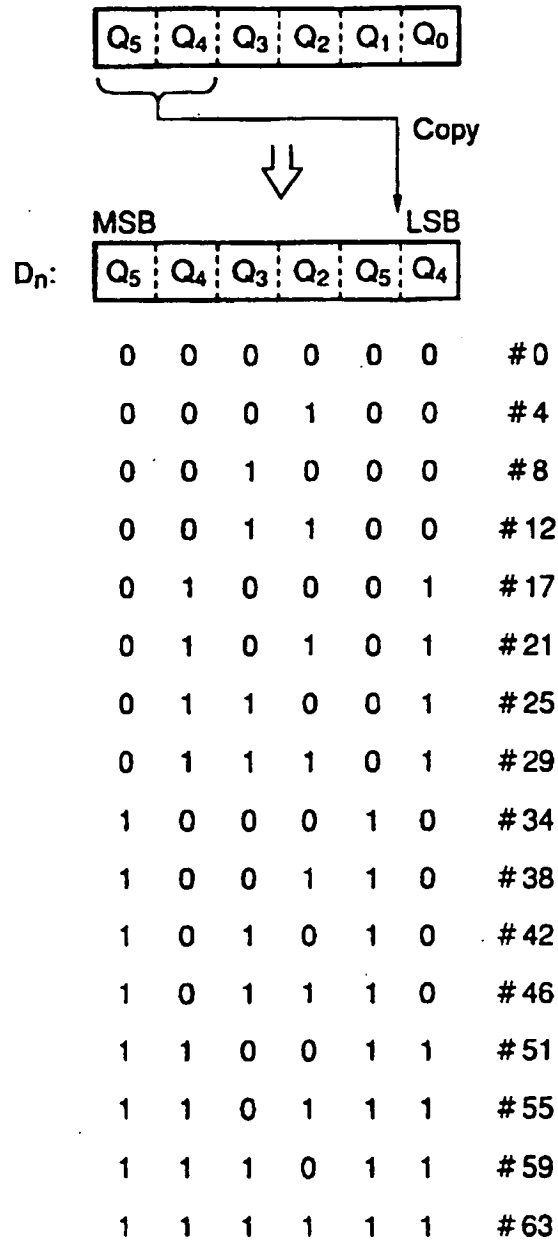


FIG.7

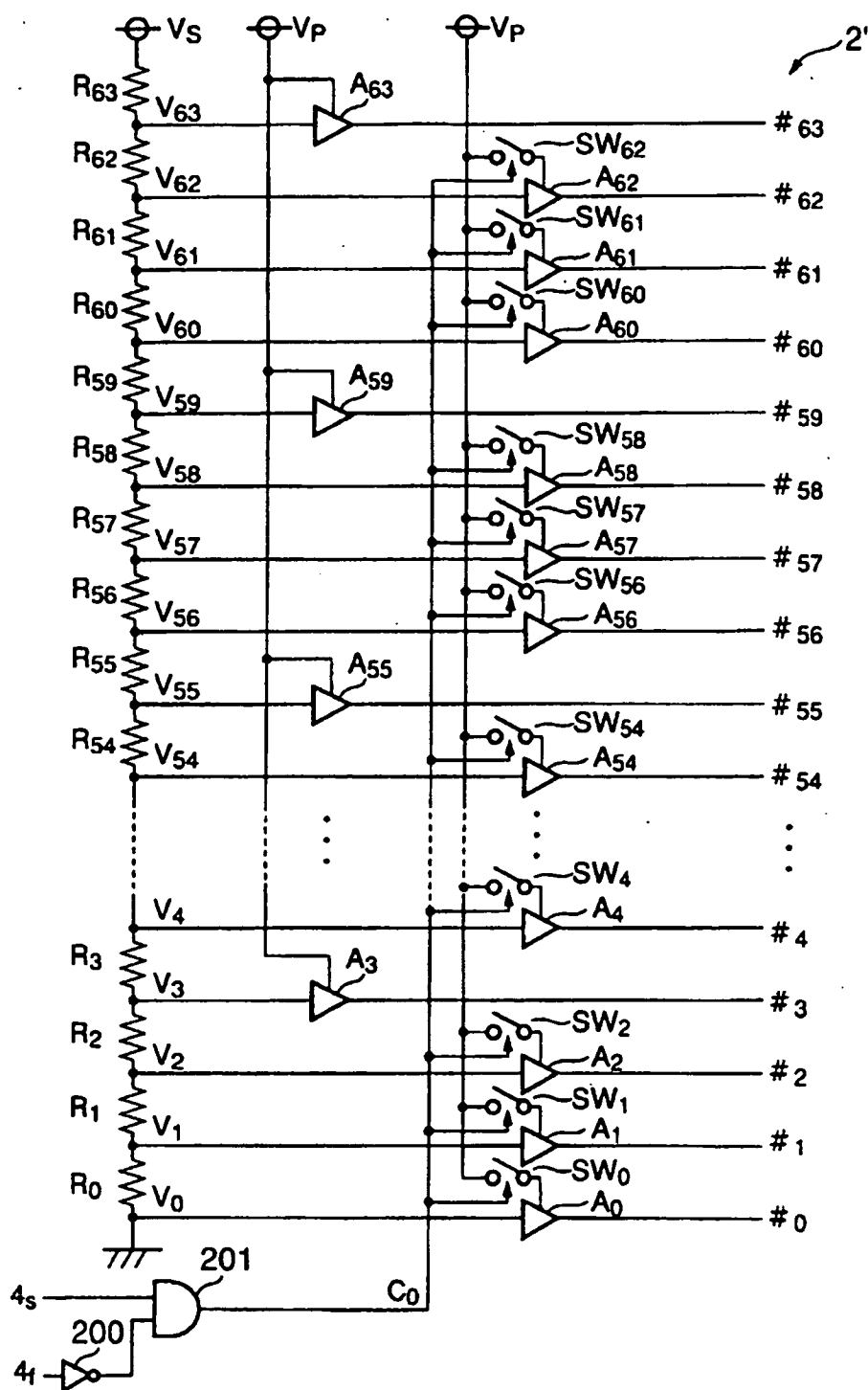


FIG. 8

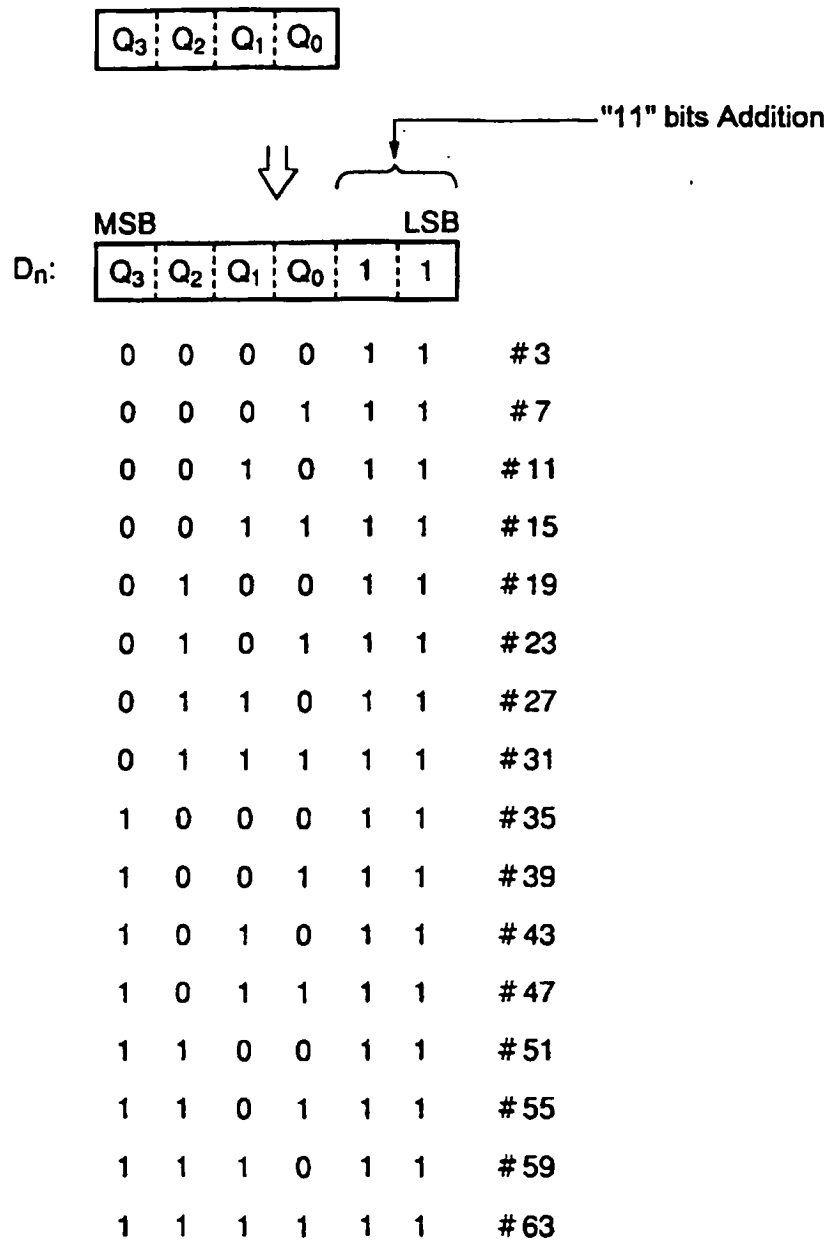


FIG.9

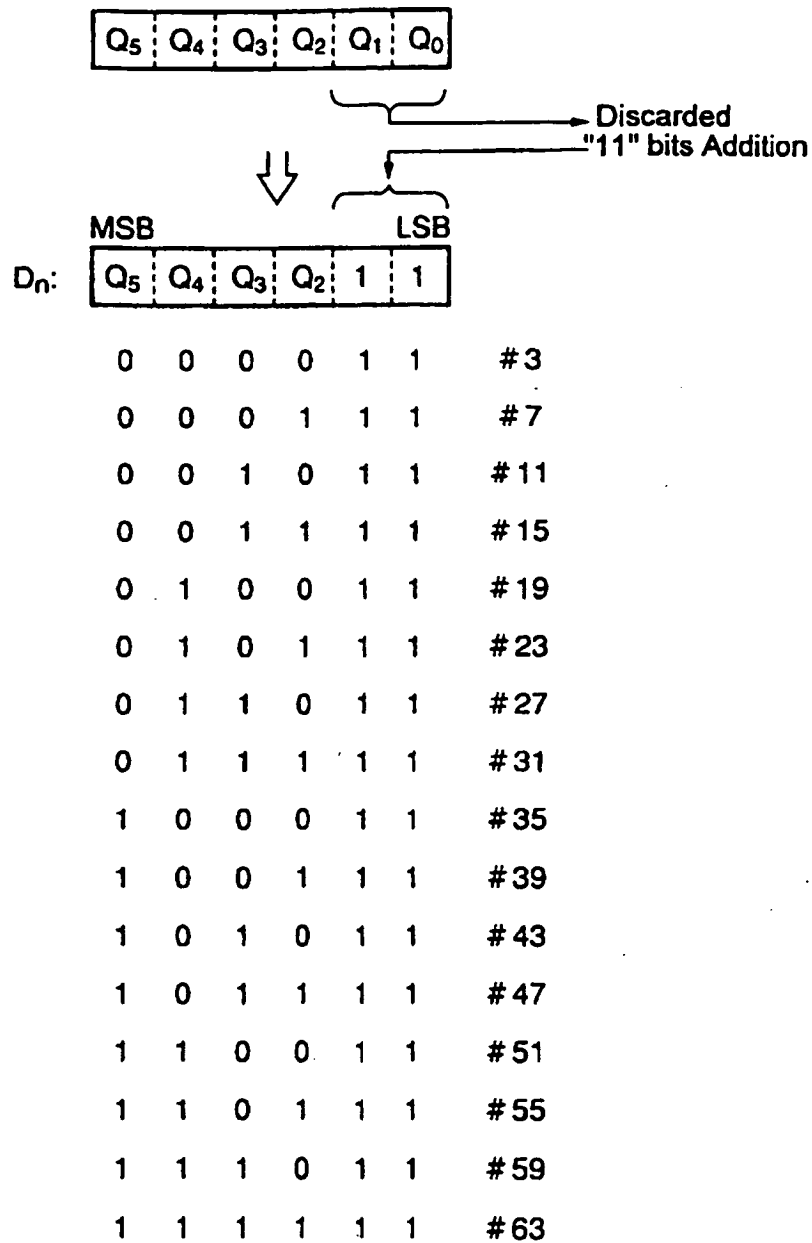


FIG.10

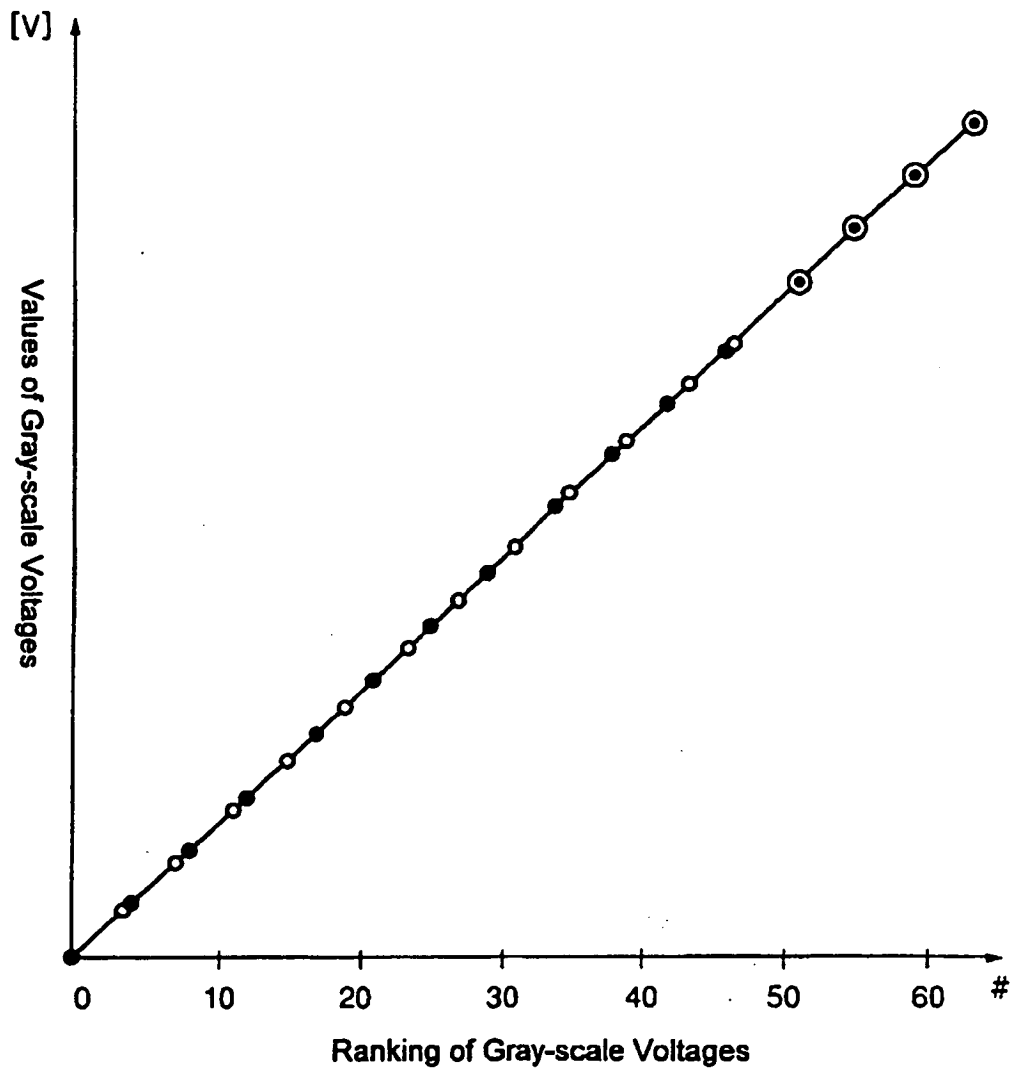


FIG.11

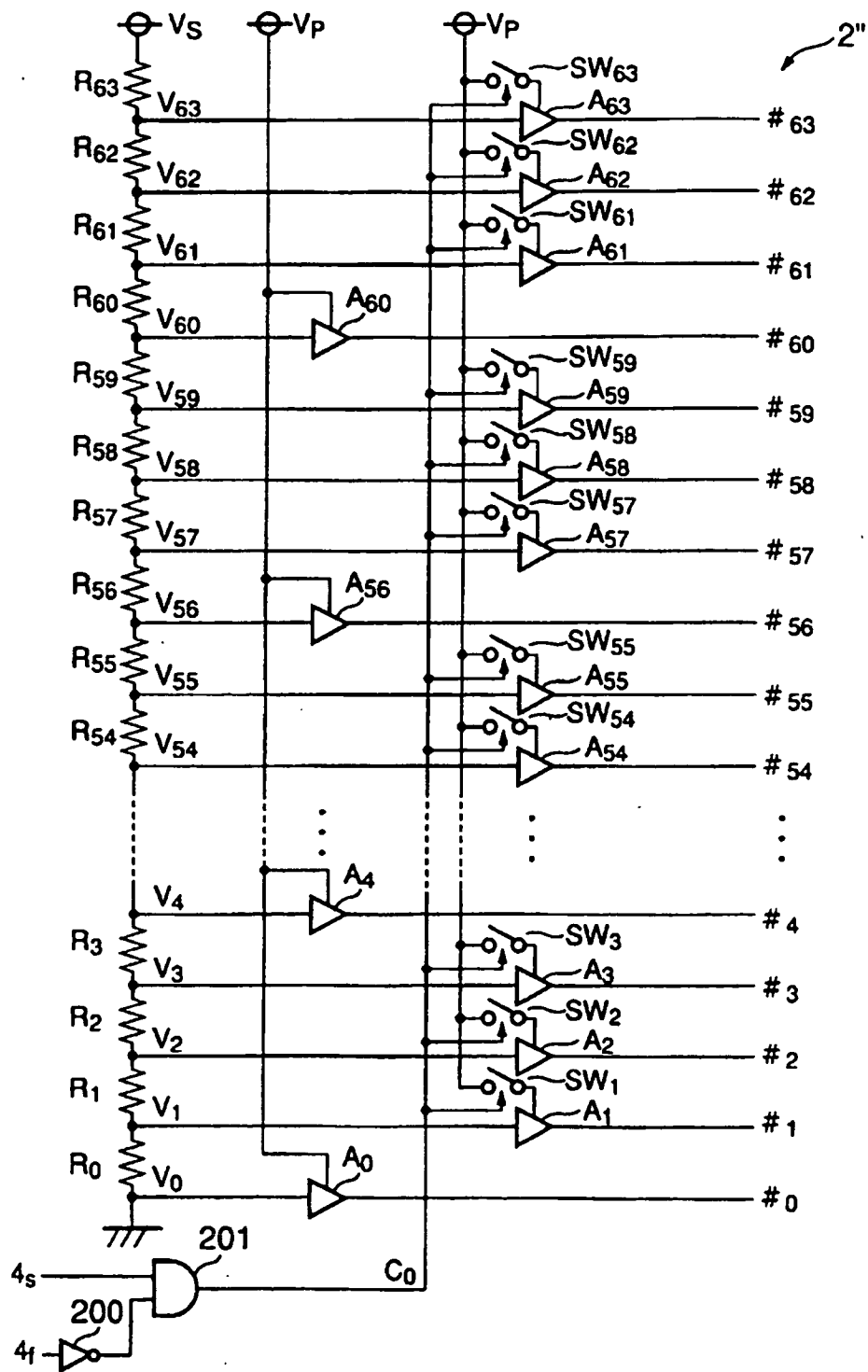


FIG.12

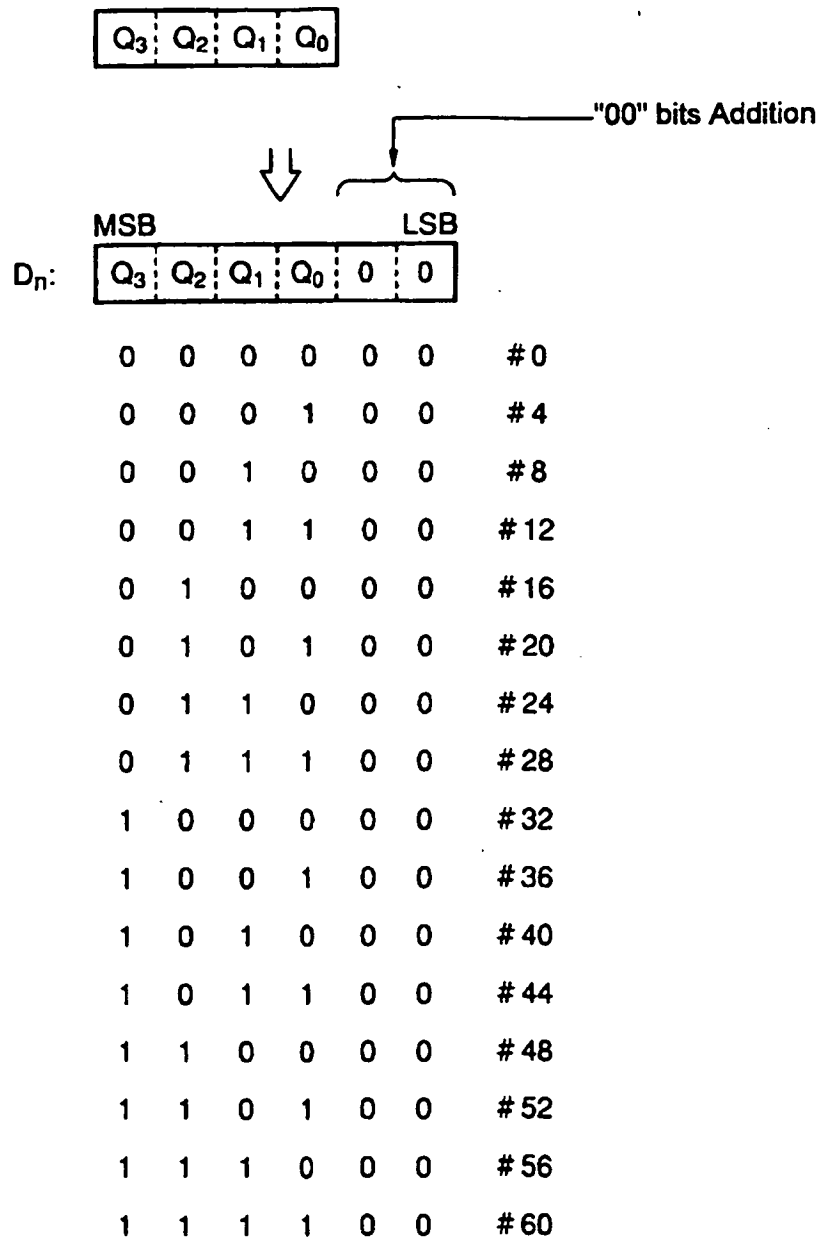


FIG.13

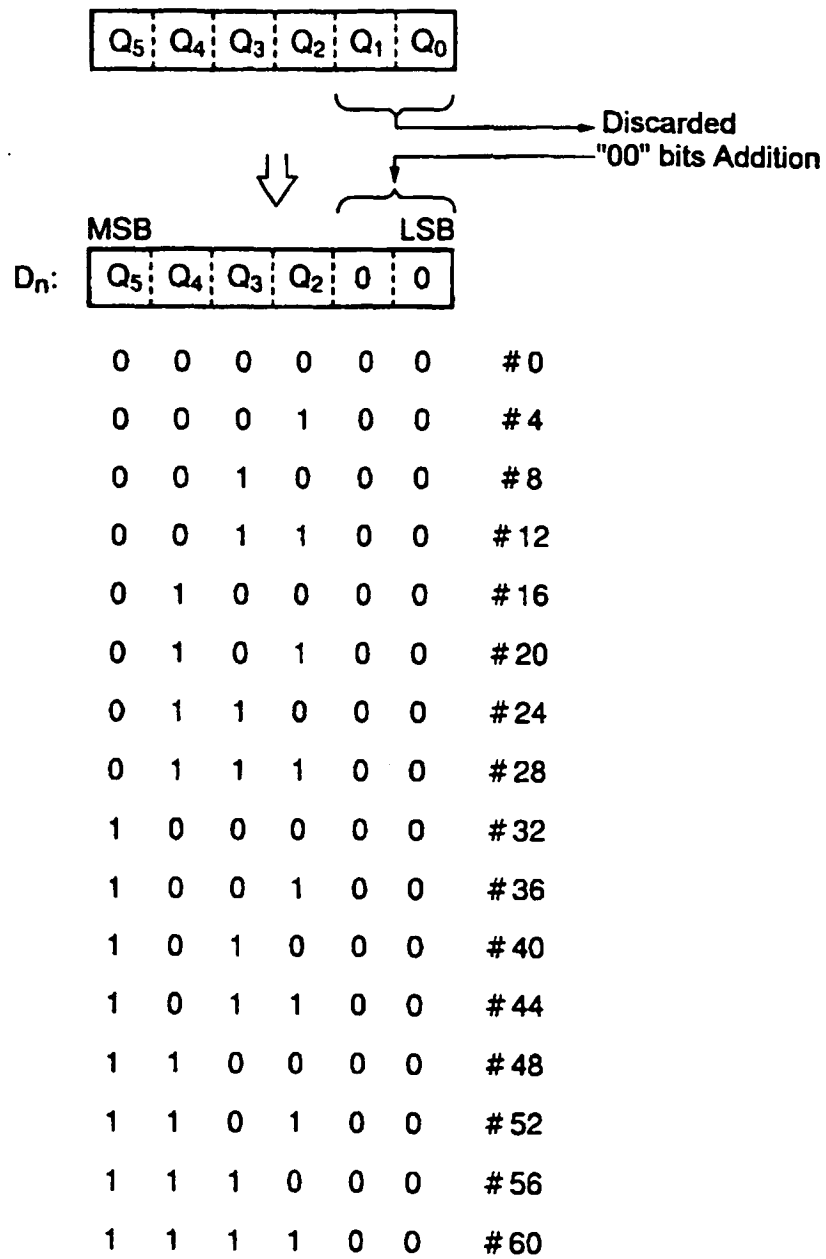


FIG.14

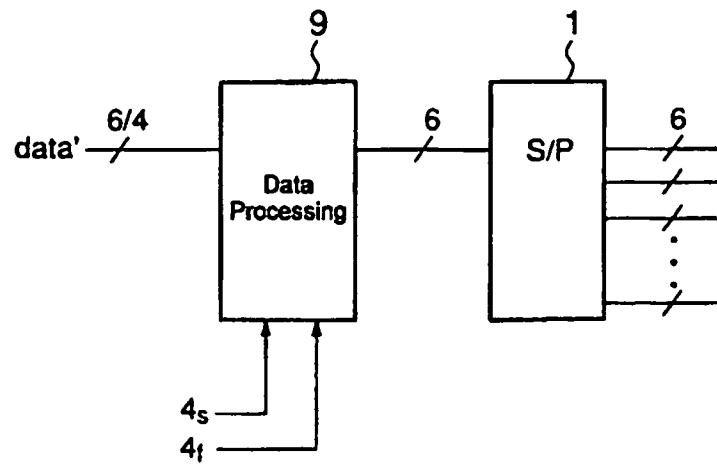


FIG15

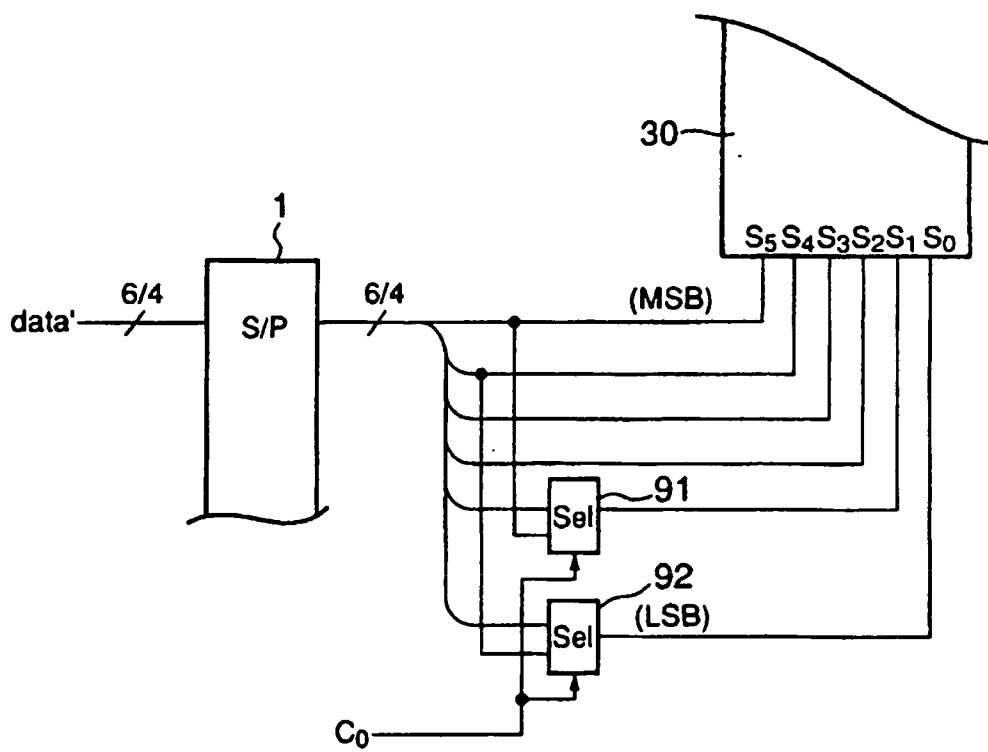


FIG16

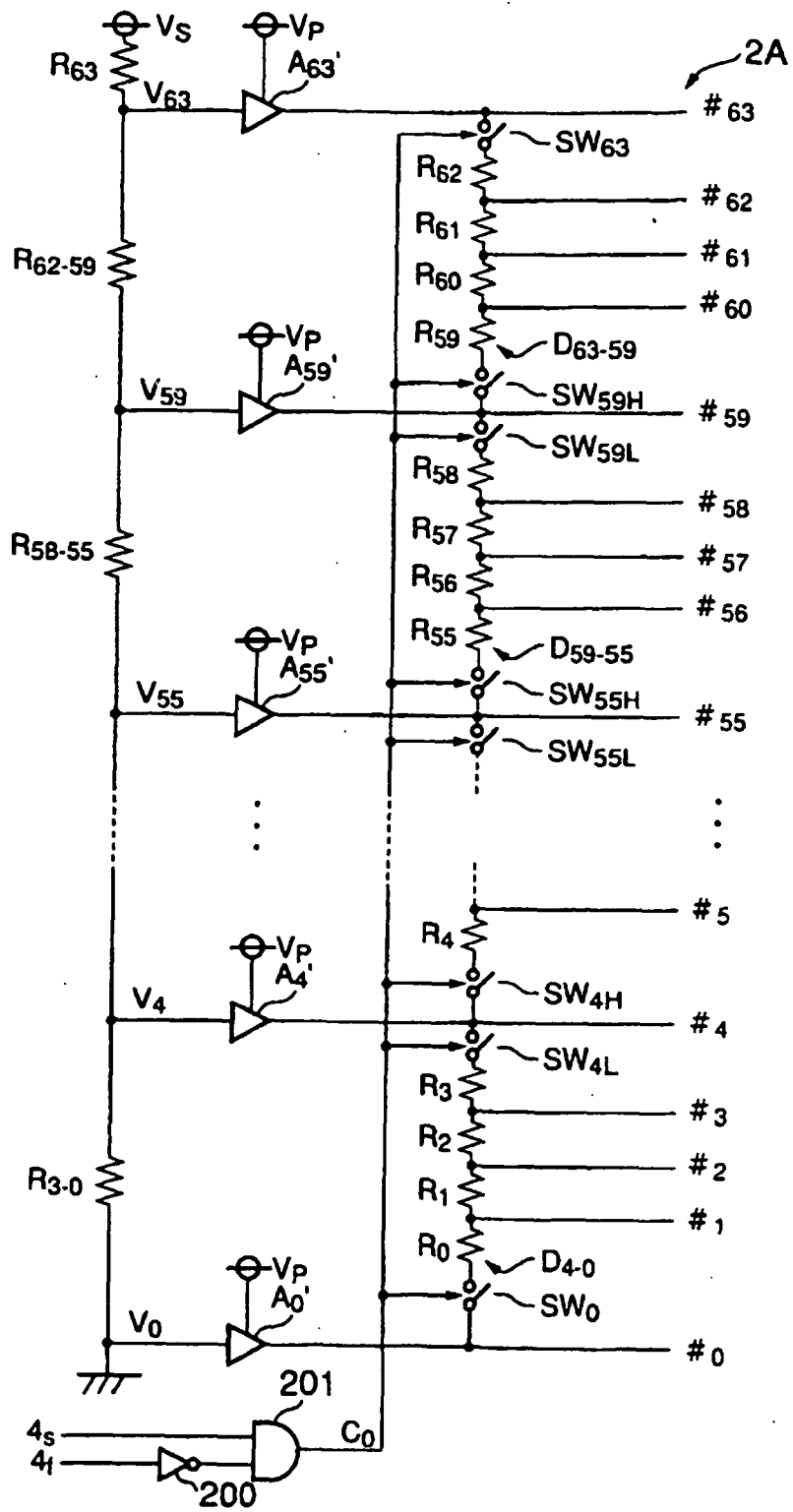


FIG.17

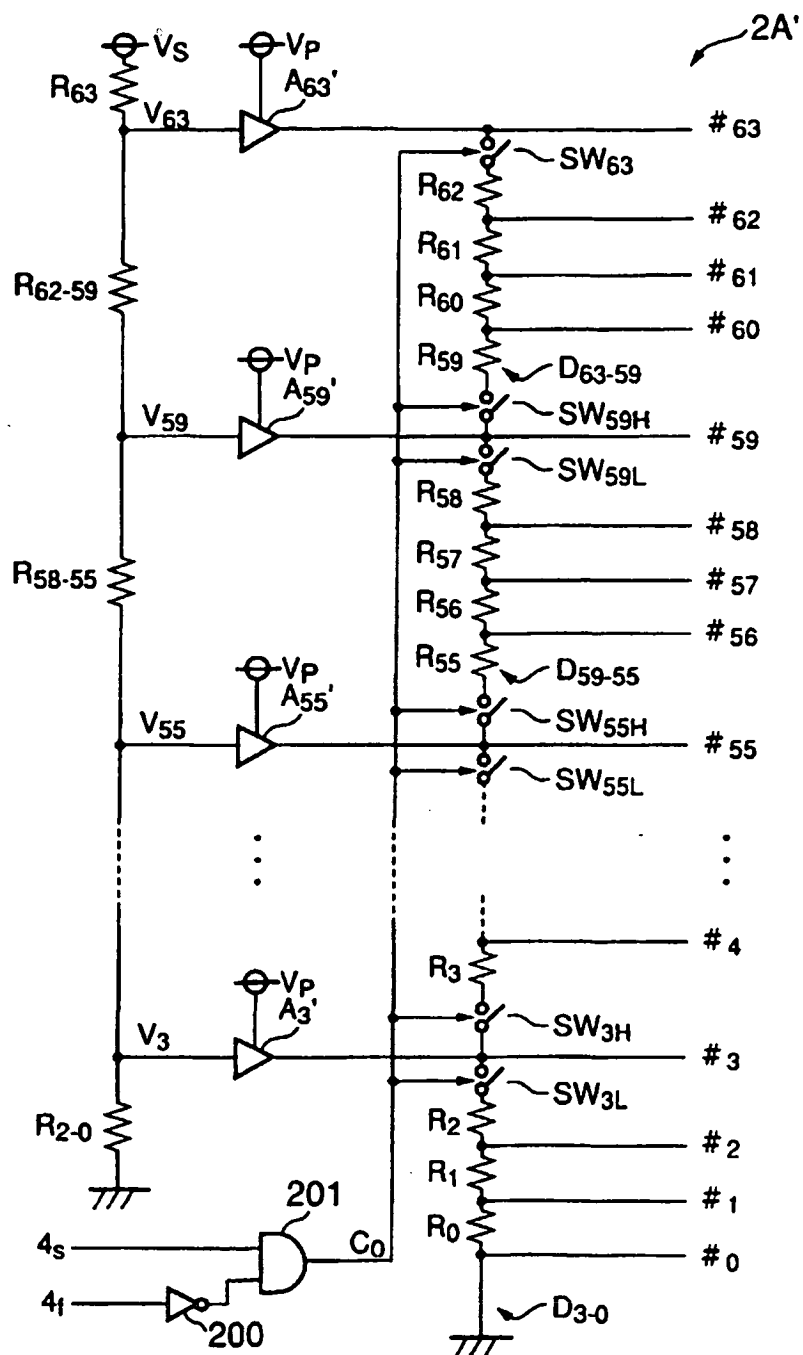


FIG.18

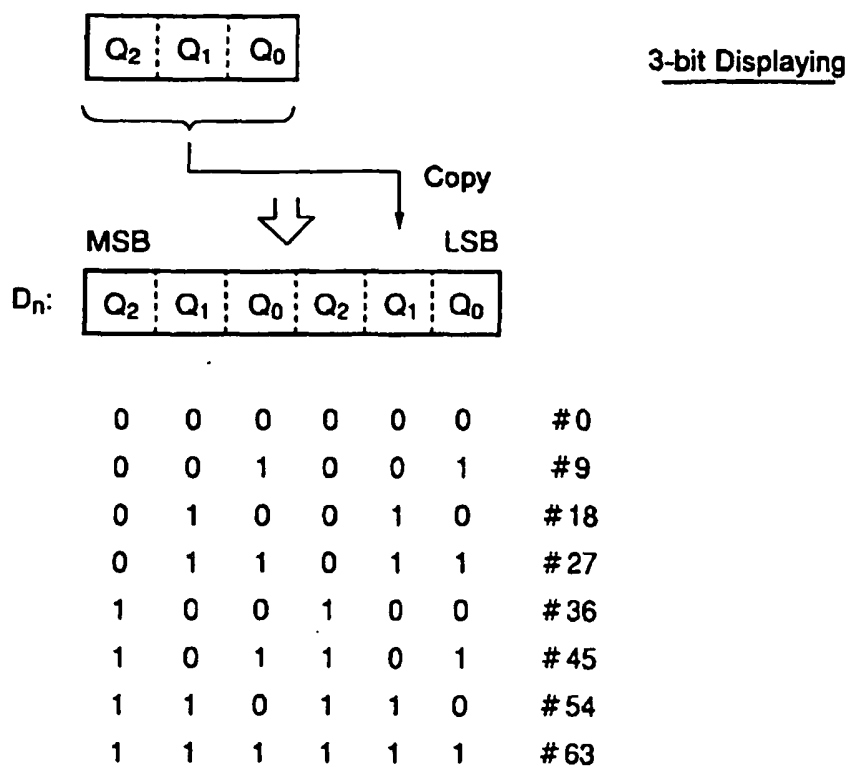


FIG.19

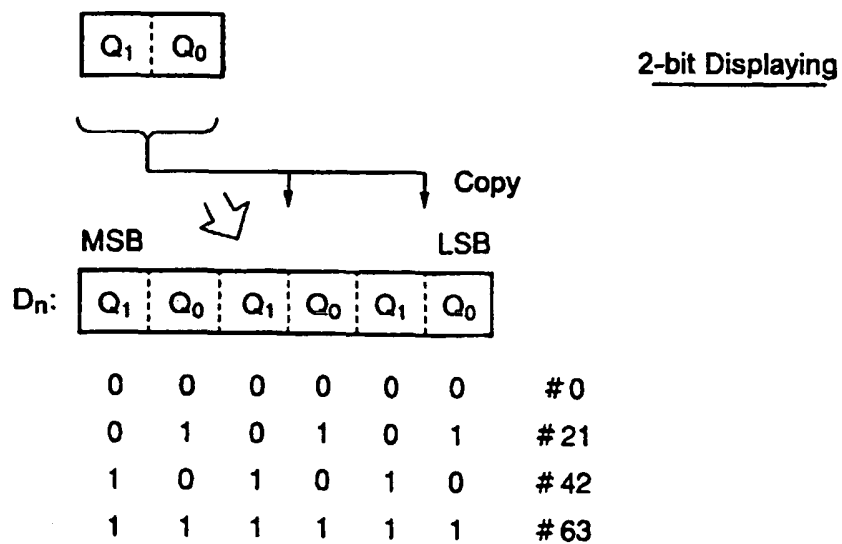


FIG.20

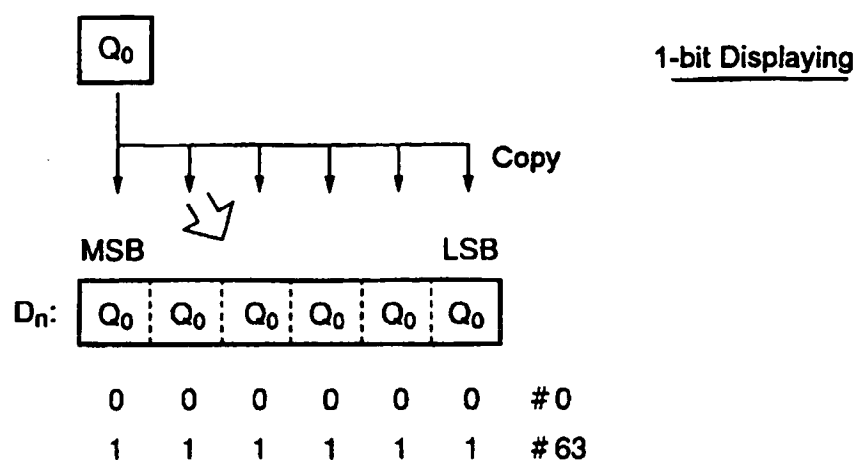


FIG.21

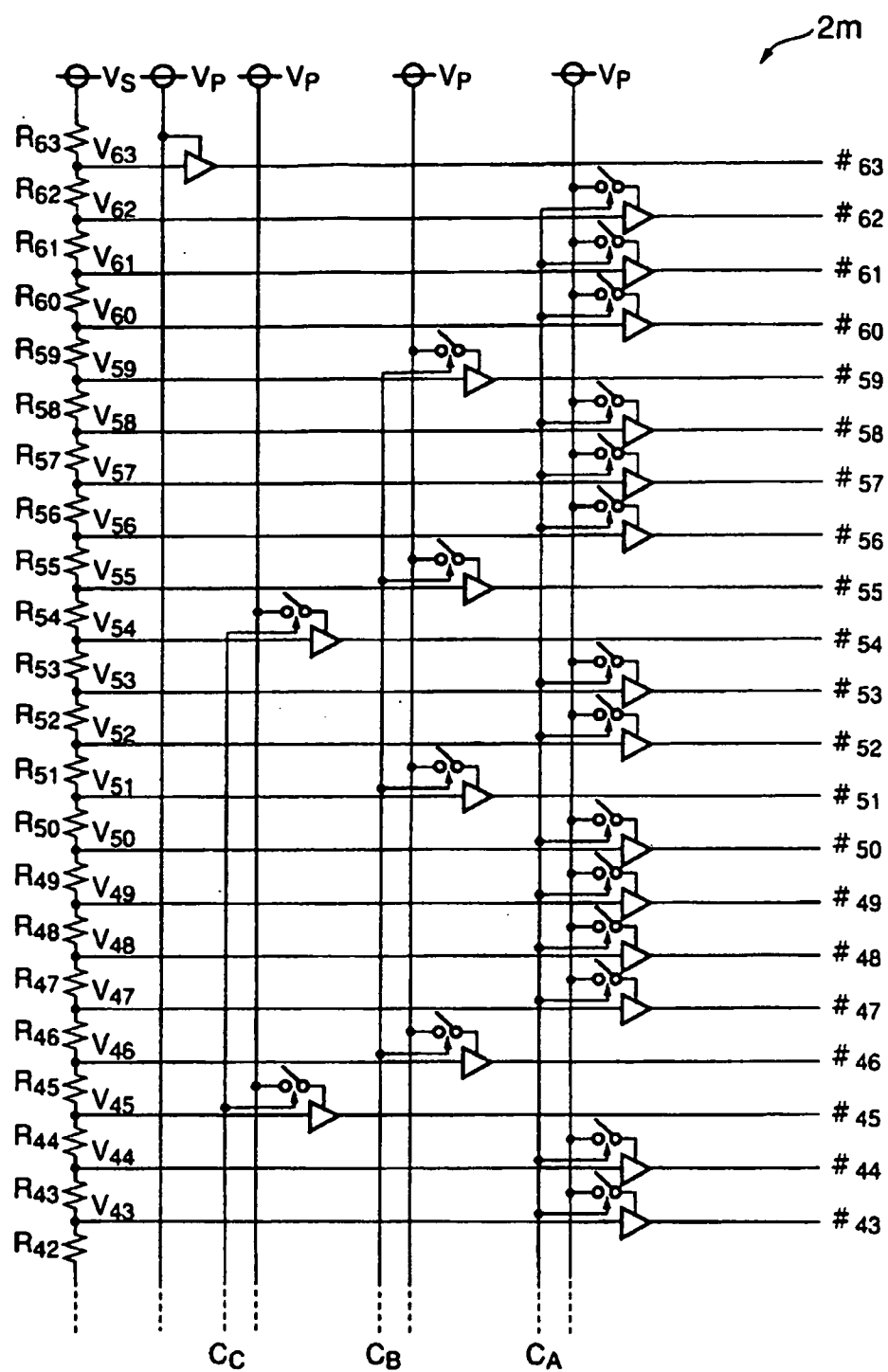


FIG.22

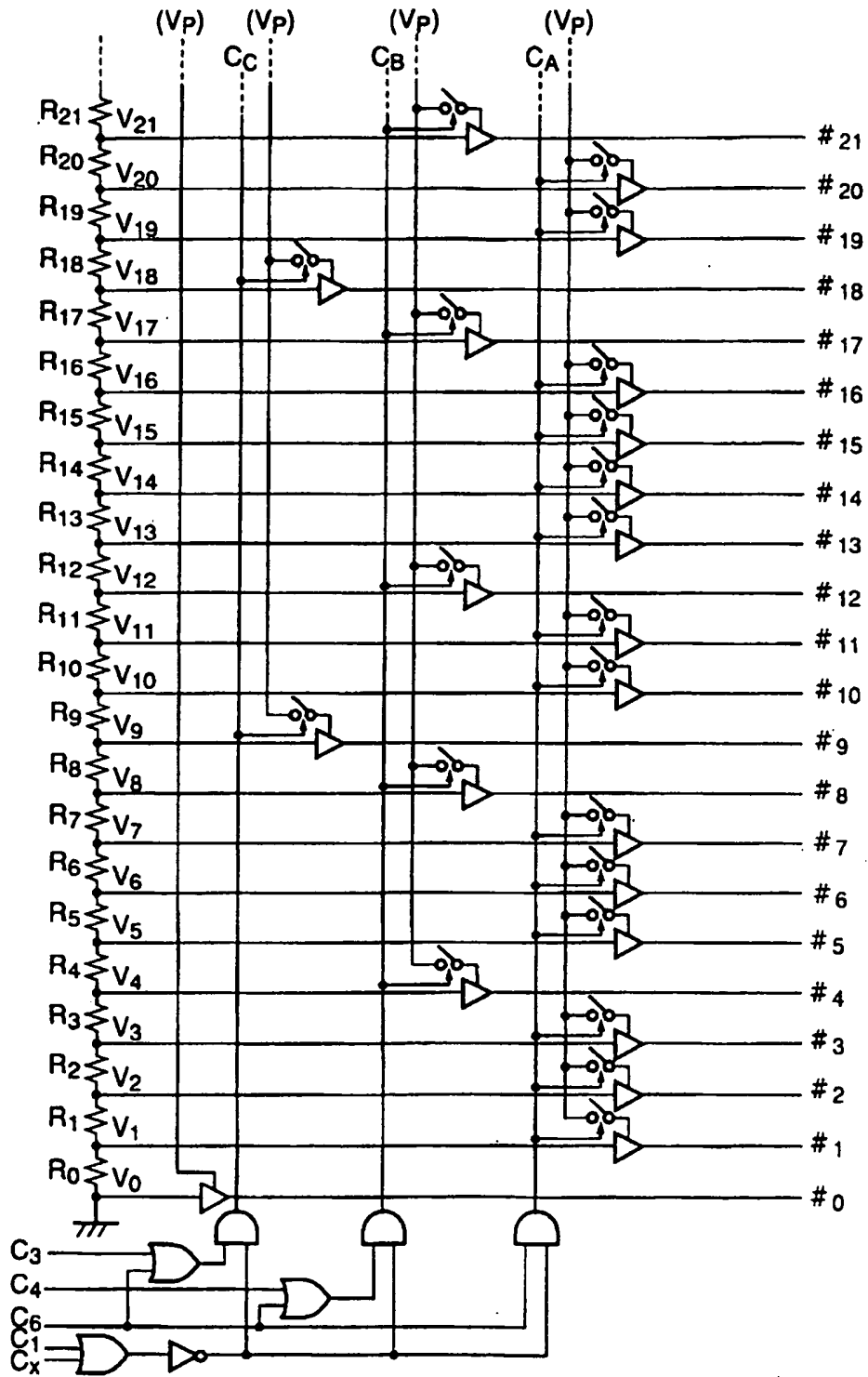


FIG.23

Control Singal		Number of Presented Gray-scale Levels					
Mode	Control Singal	C ₆	C ₄	C ₃	C ₁	C _x	
		C ₆	C ₄	C ₃	C ₁	C _x	
Normal	6-bit Displaying	H	L	L	L	L	64
	4-bit Displaying	L	H	L	L	L	16
	3-bit Displaying	L	L	H	L	L	8
	1-bit Displaying	L	L	L	H	L	2
Forced		X	X	X	X	H	2

FIG.24

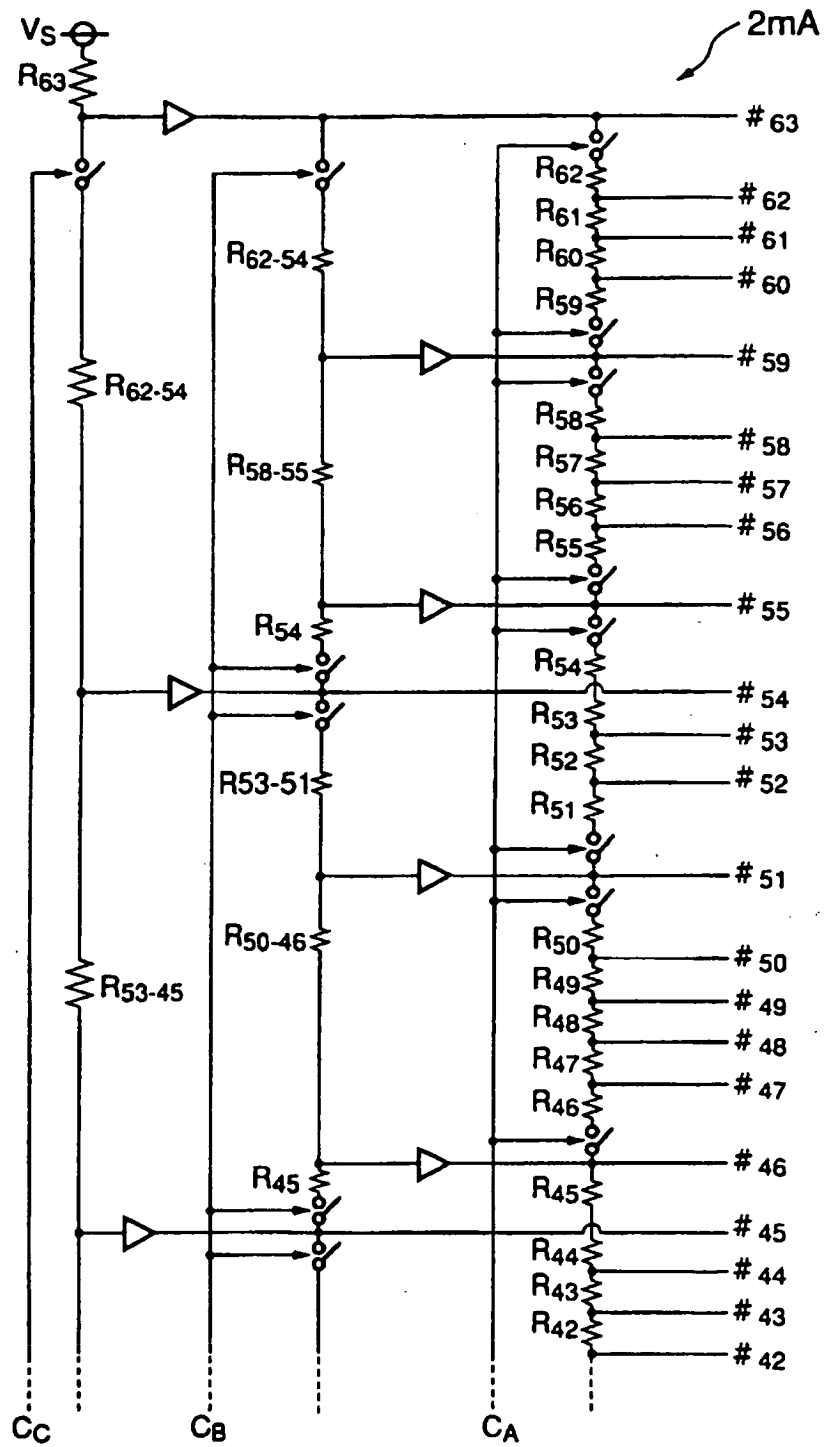


FIG.25

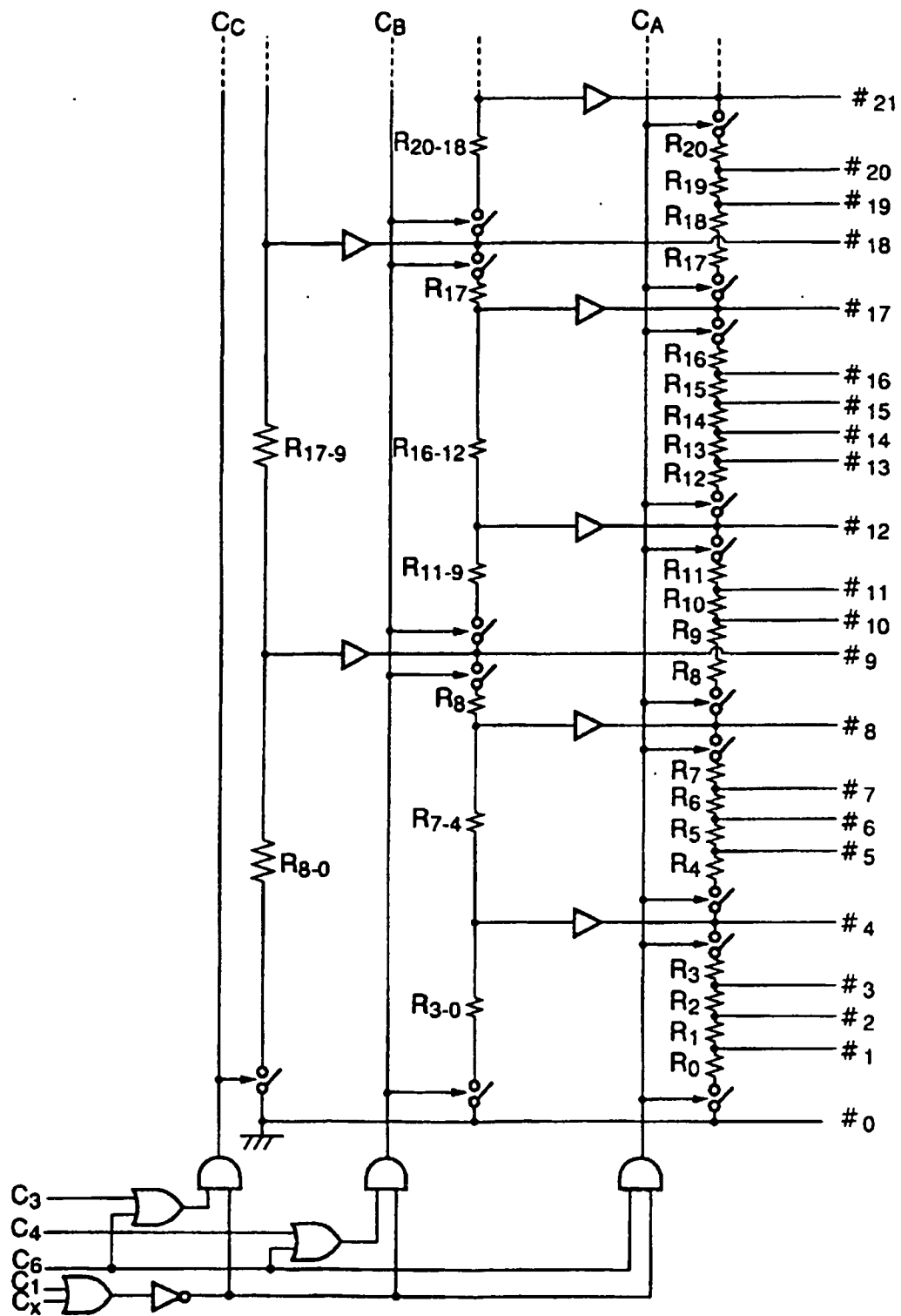


FIG.26

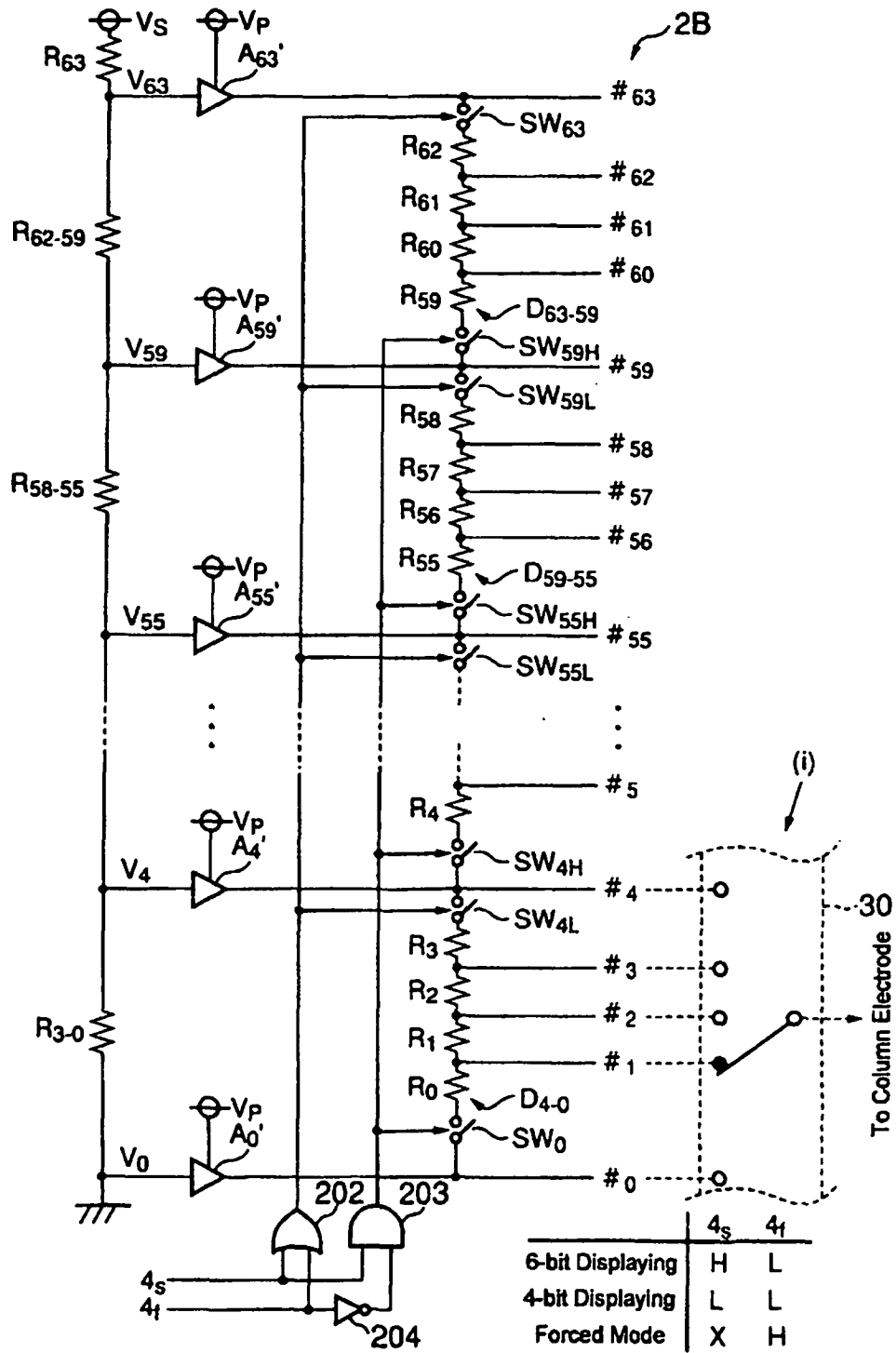


FIG.27

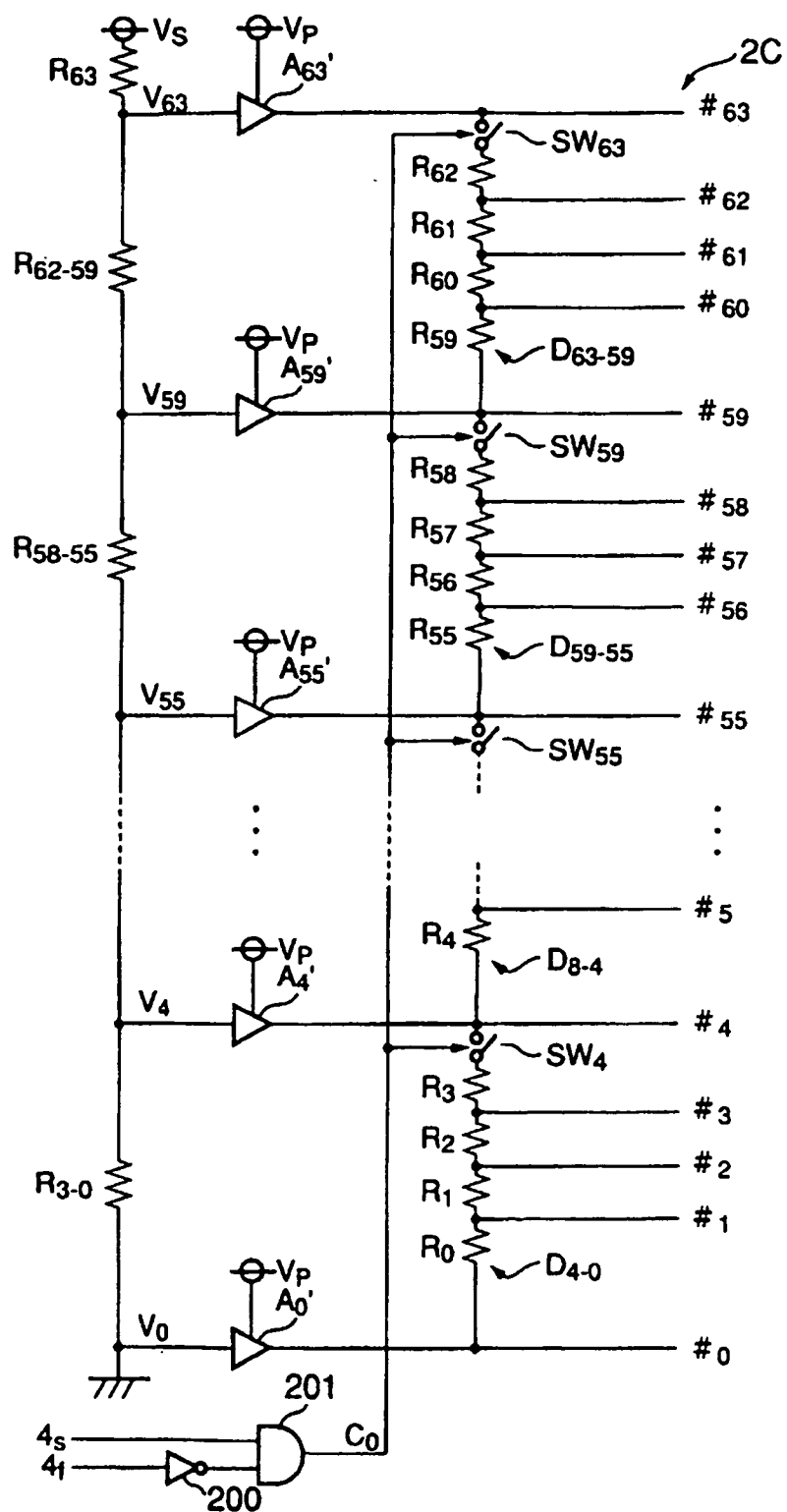


FIG.28

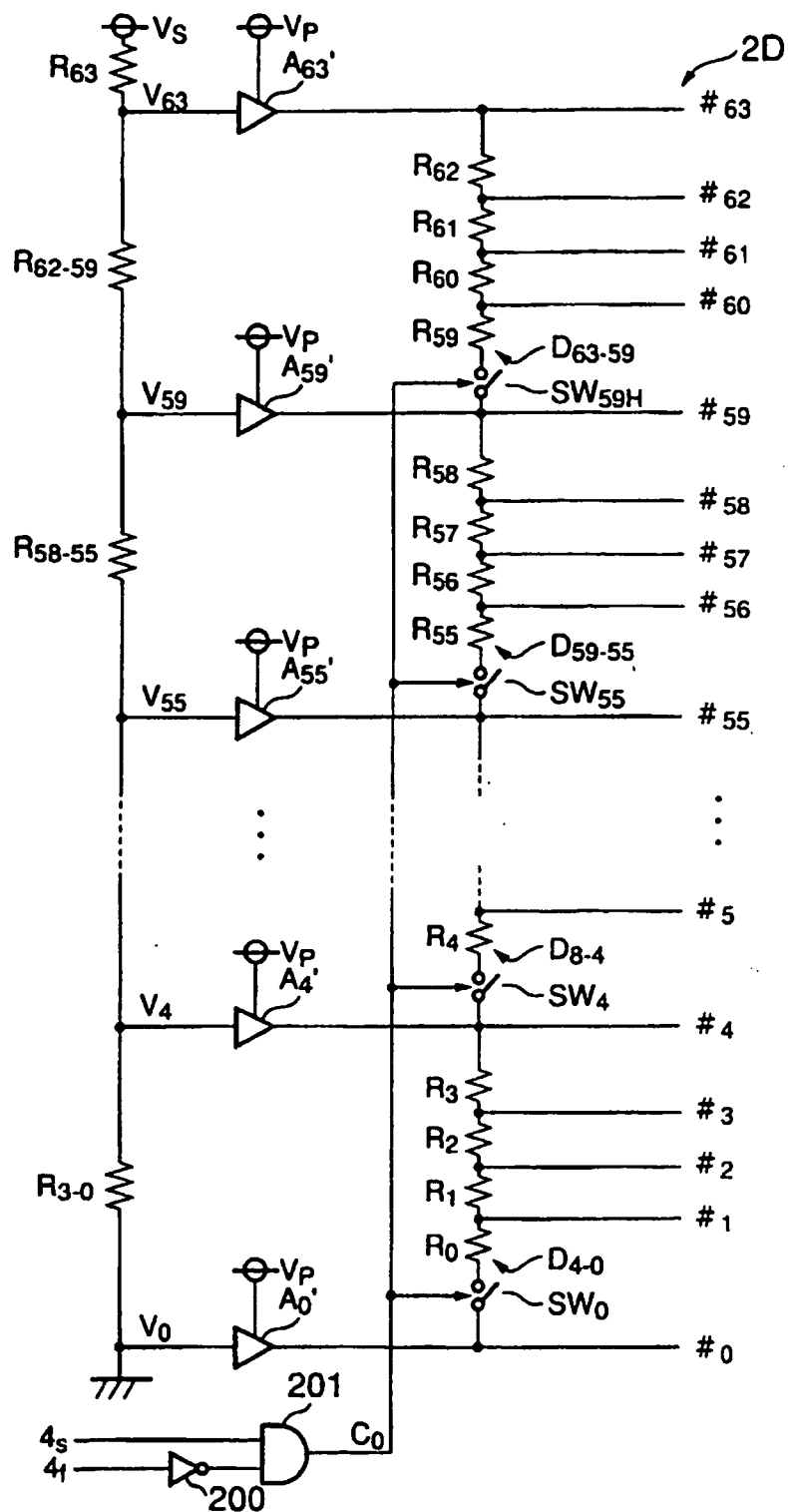


FIG.29

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 5343221 A [0007]

专利名称(译)	用于液晶显示器的列电极驱动电路和电压产生电路		
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摘要(译)

本发明的目的是提供一种列电极驱动电路和使用它的显示装置，其可以降低功耗。用于能够进行灰度显示的显示装置的列电极驱动电路50。该电路50包括：灰度电压产生装置（2），包括放大器（A63-A0），其输入分别施加有多个灰度电压（V63-V0）；选择装置（30-3x），用于根据表示灰度的图像信号为每个像素或每个预定的显示单元选择和输出放大器（A63-A0）的任何输出信号（#63-#0）。像素或显示单位的比例级别。灰度电压产生装置2使得对应于预定数量的预定灰度级的放大器的任何放大器（A1-A3，...，A56-A58，A60-A62）断电并且在预定模式期间使其它放大器（A0，A4，.....，A55，A59，A63）通电，选择装置（30-3x）选择在预定模式期间通电的放大器的任何输出信号。还公开了基于分压器电路的另一种结构。

