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(54) **Field effect transistor and method of manufacturing the same as well as liquid crystal display using the same as well as method of manufacturing the same**

(57) A gate-overlap-drain structure is obtained by a single pair of a single impurity implantation process and a single laser anneal process, wherein the improved gate-overlap-drain structure includes lightly activated high impurity concentration regions exhibiting substantially the same function as the lightly doped drain re-

gions, wherein the lightly activated high impurity concentration regions are bounded with high impurity concentration regions serving as source and drain regions. The boundaries are self-aligned to edges of a gate electrode. Side regions of the gate electrode overlap the lightly activated high impurity concentration regions.

**FIG. 1A prior art**

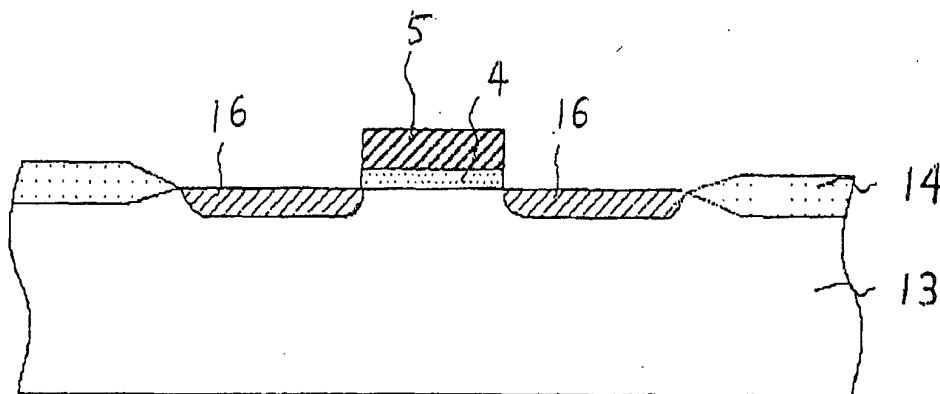


FIG. 1B prior art

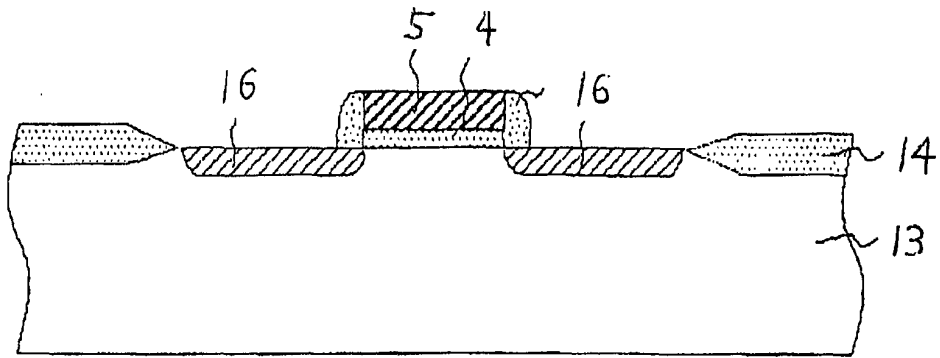
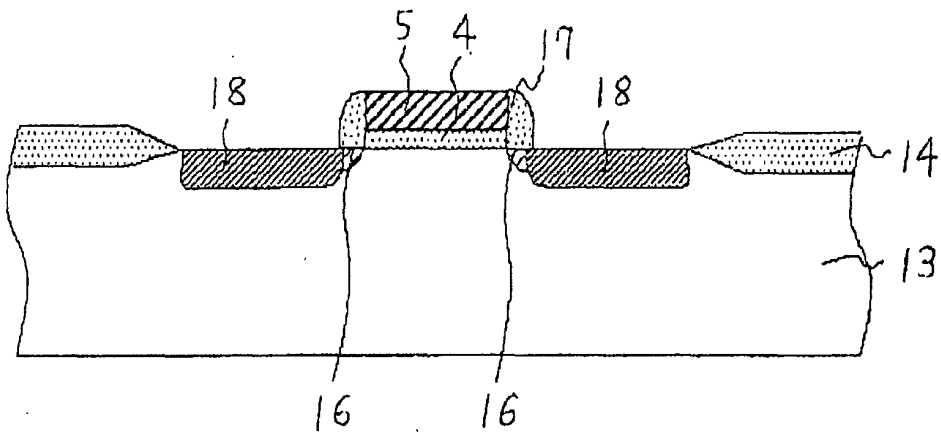


FIG. 1C prior art



## Description

**[0001]** The present invention relates to a field effect transistor with an improved gate overlap drain structure and a method of manufacturing the same by utilizing a laser beam irradiation technique as well as a liquid crystal display using the same and a method of manufacturing the same.

**[0002]** All of patents, patent applications, patent publications, scientific articles and the like, which will hereinafter be cited or identified in the present application, will, hereby, be incorporated by references in their entirety in order to describe more fully the state of the art, to which the present invention pertains.

**[0003]** In recent years, shrinkage of the semiconductor device causes shortening a gate width of a field effect transistor. The shortened gate width may cause short channel effects and hot carrier injections, thereby resulting in deterioration of reliability of the field effect transistor. The short channel effects and the hot carrier injections may cause an extensively high field in the vicinity of the drain region of the transistor. In order to avoid the above undesired problems, it is effective to reduce or relax an extensively high field in the vicinity of the drain region of the transistor. In order to reduce or relax an extensively high field, a lightly doped drain (LLD) structure is effective, which has been known in the art, to which the present invention pertains. In accordance with the lightly doped drain (LLD) structure, off-set gate layers having lower impurity concentration are selectively formed in selected substrate regions between source/drain regions and a channel region under a gate electrode. The off-set gate layers contribute to relax undesired extensively high fields in the selected substrate regions between the source/drain regions and the channel region under the gate electrode. The off-set gate layers thus contribute to increase the withstand voltages, for example, a punch-through voltage and a hot carrier withstand voltage.

**[0004]** A method of forming a typical example of a conventional lightly doped drain structure will be described with reference to FIGS. 1A through 1C. As shown in FIG. 1A, an isolation oxide film 14 is selectively formed over a silicon substrate 13 by a local oxidation of silicon method, thereby to define a field region which is surrounded by the isolation oxide film 14. A gate oxide film 4 is formed on the field region by a thermal oxidation. A polysilicon film is then deposited by a low pressure chemical vapor deposition method over the gate oxide film 4 and the isolation oxide film 14. A photo-lithography and a subsequent dry etching process are then carried out to form a gate electrode 5. A first ion-implantation is then carried out at a low impurity concentration by use of the gate electrode 5 and the isolation oxide film 14 as masks for subsequent anneal under predetermined conditions to form low impurity concentration regions 16.

**[0005]** As shown in FIG. 1B, a silicon oxide film is de-

posited by a low pressure chemical vapor deposition method over the gate electrode 5 and the isolation oxide film 14 as well as the low impurity concentration regions 16. An anisotropic etching such as a dry etching is then carried out to etch-back the silicon oxide film, thereby to selectively form side wall oxide films 17 on opposite side walls of the gate electrode 5.

**[0006]** As shown in FIG. 1C, a second ion-implantation is carried out at a high impurity concentration by use of the gate electrode 5, the side wall oxide films 17 and the isolation oxide film 14 as masks for subsequent anneal under predetermined conditions to form high impurity concentration regions 18, while the low impurity concentration regions 16 remain only under the side wall oxide films 17, wherein boundaries between the high impurity concentration regions 18 and the low impurity concentration regions 16 are self-aligned to the outside edges of the side wall oxide films 17. The high impurity concentration regions 18 serve as source and drain regions, while the remaining low impurity concentration regions 16 under the side wall oxide films 17 serve as the off-set gate layers. The above lightly doped drain structure is, indeed, effective to relax the expensively high field concentration. Further high degree of shrinkage of the semiconductor device causes a further high degree of shortening the gate width which defines the channel width, namely of shortening the channel width. Increase in the degree of shortening the channel width may cause an undesired phenomenon that hot carriers generated in the vicinity of the drain region are trapped into side regions of the gate oxide film in the vicinity of the lightly doped drain regions or the low impurity concentration regions 16. The trapped hot carriers may cause an undesired inversion in the conductivity type of the lightly doped drain regions 16. The inversion in the conductivity type of the lightly doped drain regions 16 may cause an undesired variation in threshold voltage of the transistor and also an undesired drop of the punch-through withstand voltage.

**[0007]** In the meantime, it has been known in the art, to which the present invention pertains, a thin film transistor as typical one of the field effect transistors is used as a switching device for a liquid crystal display. In accordance with a basic structure of a polycrystal silicon thin film transistor used as a pixel switching transistor in the liquid crystal display, the lightly doped drain structure is effective to suppress or reduce a leakage of current, which may be a dark current. This lightly doped drain structure and the channel region of the polycrystal silicon thin film transistor have an disadvantage in possible increase in leakage of current or dark current upon incidence of light into the channel region, namely an off-leak current upon incidence of light into the channel region. In order to reduce such undesired off-leak current upon incidence of light into the channel region, a pair of top and bottom light shielding layers is provided, wherein the top light shielding layer overlies the transistor, while the bottom light shielding layer underlies the tran-

sistor. As described above, in accordance with the lightly doped drain structure, the low impurity concentration regions are not covered by the gate electrode. This structure allows a light reflected by respective layers in an active matrix substrate of the display to become incident into the low impurity concentration regions, even the top and bottom optical shielding layers are provided. Namely, it is difficult to avoid the undesirable leakage of light or possible incidence of light into the low impurity concentration regions unless the low impurity concentration regions are completely covered by the gate electrode. This problem will be remarkable in a light valve active matrix liquid crystal display for liquid crystal light projection. In order to have attempted to solve the above problems with the undesired possible trap of the hot carriers into the gate oxide film and with the undesired possible light incidence into the low impurity concentration regions, a gate-overlap-drain structure was proposed, wherein laminations of a gate insulation film and a gate electrode extend over the lightly doped drain structure, or over the low impurity concentration regions. This gate-overlap-drain structure is disclosed in Japanese laid-open patent publications Nos. 8-153875 and 8-222736. This gate-overlap-drain structure will be described.

**[0008]** FIGS. 2A through 2D are fragmentary cross sectional elevation views of field effect transistors in sequential steps involved in a typical example of a conventional method of forming a gate-overlap-drain structure. As shown in FIG. 2A, an isolation oxide film 14 is selectively formed over a silicon substrate 13 by a local oxidation of silicon method, thereby to define a field region which is surrounded by the isolation oxide film 14. A gate oxide film 4 is formed on the field region by a thermal oxidation. A resist pattern 10 is selectively formed in the field region, wherein the resist pattern 10 has a smaller size than an intended size of a gate electrode to be formed in later. A first ion-implantation is then carried out at a low impurity concentration by use of the resist pattern 10 and the isolation oxide film 14 as masks for subsequent anneal under predetermined conditions to form low impurity concentration regions 16. After the first ion-implantation is completed, then the used resist pattern 10 is removed.

**[0009]** As shown in FIG. 2B, a polysilicon film is then deposited by a low pressure chemical vapor deposition method over the gate oxide film 4 and the isolation oxide film 14. A photo-lithography and a subsequent dry etching process are then carried out to form a gate electrode 5 which has a larger size than the above-described resist pattern 10 which was already been removed, so that side regions of the gate electrode 5 overlap inside regions of the low impurity concentration regions 16.

**[0010]** As shown in FIG. 2C, a second ion-implantation is carried out at a high impurity concentration by use of the gate electrode 5 and the isolation oxide film 14 as masks for subsequent anneal under predetermined conditions to form high impurity concentration regions

18, while the low impurity concentration regions 16 remain only under the overlap side regions of the gate electrode 5, wherein boundaries between the high impurity concentration regions 18 and the low impurity concentration regions 16 are self-aligned to the outside edges of the gate electrode 5. The high impurity concentration regions 18 serve as source and drain regions, while the remaining low impurity concentration regions 16 under the side regions of the gate electrode 5 serve as the off-set gate layers. The side regions of the gate electrode 5 overlap the remaining low impurity concentration regions 16, thereby forming a gate-overlap-drain structure.

**[0011]** As shown in FIG. 2D, an inter-layer insulator 6 is deposited over the gate electrode 5, the gate oxide film 4 and the isolation oxide film 14. Contact holes are selectively formed in the inter-layer insulator 6 and over the high impurity concentration regions 18 serving as the source and drain regions. Source and drain electrodes 7 are selectively formed within the contact holes and over the inter-layer insulator 6, so that the source and drain electrodes 7 are in contact with the high impurity concentration regions 18 serving as the source and drain regions, thereby forming a field effect transistor including a gate-overlap-drain structure.

**[0012]** FIGS. 3A through 3D are fragmentary cross sectional elevation views of field effect transistors in sequential steps involved in another typical example of a conventional method of forming another gate-overlap-drain structure. This conventional technique is disclosed in Japanese laid-open patent publication No. 8-153875. As shown in FIG. 3A, an isolation oxide film 14 is selectively formed over a silicon substrate 13 by a local oxidation of silicon method, thereby to define a field region which is surrounded by the isolation oxide film 14. A gate oxide film 4 is formed on the field region by a thermal oxidation. A polysilicon film is then deposited by a low pressure chemical vapor deposition method over the gate oxide film 4 and the isolation oxide film 14. A photo-lithography and a subsequent dry etching process are then carried out to form a gate electrode 5. A first ion-implantation is then carried out at a low impurity concentration by use of the gate electrode 5 and the isolation oxide film 14 as masks for subsequent anneal under predetermined conditions to form low impurity concentration regions 16.

**[0013]** As shown in FIG. 3B, a silicon-based film is entirely formed over the gate electrode 5 and the isolation oxide film 14 as well as the low impurity concentration regions 16. An anisotropic etching is then carried out to etch-back the silicon oxide film, thereby to selectively form side wall conductive films 19 on opposite side walls of the gate electrode 5. The side wall silicon-based films 19 are electrically conductive, for which reason the side wall conductive films 19 serve as part of the gate electrode in cooperation with the gate electrode 5.

**[0014]** As shown in FIG. 3C, a second ion-implantation is carried out at a high impurity concentration by use

of the gate electrode 5, the side wall conductive films 19 and the isolation oxide film 14 as masks for subsequent anneal under predetermined conditions to form high impurity concentration regions 18, while the low impurity concentration regions 16 remain only under the side wall conductive films 19, wherein boundaries between the high impurity concentration regions 18 and the low impurity concentration regions 16 are self-aligned to boundaries between the side wall conductive films 19 and the gate electrode 5. The high impurity concentration regions 18 serve as source and drain regions, while the remaining low impurity concentration regions 16 under the side wall conductive films 19 serve as the off-set gate layers, thereby forming a gate-overlap-drain structure.

**[0015]** As shown in FIG. 3D, an inter-layer insulator 6 is deposited over the gate electrode 5, the side wall conductive films 19, the gate oxide film 4 and the isolation oxide film 14. Contact holes are selectively formed in the inter-layer insulator 6 and over the high impurity concentration regions 18 serving as the source and drain regions. Source and drain electrodes 7 are selectively formed within the contact holes and over the inter-layer insulator 6, so that the source and drain electrodes 7 are in contact with the high impurity concentration regions 18 serving as the source and drain regions, thereby forming a field effect transistor including a gate-overlap-drain structure.

**[0016]** In accordance with the above described conventional gate-overlap-drain structure, the side regions of the gate electrode overlap the lightly doped drain regions. This conventional gate-overlap-drain structure may prevent the above-described undesired influence of the hot carriers generated in the vicinity of the drain region. Further, the lightly doped drain regions are covered by the side regions of the gate electrode, wherein the side regions of the gate electrode serve as light shielding regions and improves a light-shieldability. Namely, the conventional gate-overlap-drain structure reduces the above problem with the light leakage. The above-described conventional method for forming the conventional gate-overlap-drain structure, however, need at least two ion-implantation processes and further additional processes for forming the lightly doped drain regions under the side regions of the gate electrode. This results in complicated necessary processes for forming the conventional gate-overlap-drain structure.

**[0017]** Further, the anneal is carried out after the impurity has been selectively implanted, wherein the anneal reduces or relaxes an abruptness of the impurity concentration profile. This abruptness of the impurity concentration profile may cause an expensive highly field concentration, for which reason the reduction or the relaxation of the abruptness of the impurity concentration profile is effective to reduce or relax the expensive highly field concentration. FIG. 4 is a diagram of an impurity concentration profile across the channel region, the low impurity concentration region and the high im-

purity concentration region of the field effect transistor having the gate-overlap drain structure. As shown in FIG. 4, the impurity concentration profile includes two step-like variations in the impurity concentration at respective boundaries between the channel region and the low impurity concentration region and between the low impurity concentration region and the high impurity concentration region. Lager variation in the impurity concentration may cause a high field concentration. This impurity concentration profile with the two step-like variations makes it difficult to achieve a sufficient relaxation of the field concentration.

**[0018]** Furthermore, the above impurity concentration profile includes the abrupt step-like variation in impurity concentration at the boundary between the low impurity concentration region and the high impurity concentration region. This abrupt step-like variation in impurity concentration causes an undesirable abrupt and large variation in energy level at the boundary between the low impurity concentration region and the high impurity concentration region. Such abrupt and large variation in energy level promotes an undesired carrier trap, and a carrier re-combination, resulting in a shortened carrier life time. In the above circumstances, the development of a novel field effect transistor free from the above problems is desirable.

**[0019]** Accordingly, it is an object of the present invention to provide a novel field effect transistor with an improved gate overlap drain structure free from the above problems.

**[0020]** It is a further object of the present invention to provide a novel field effect transistor with an improved gate overlap drain structure which may be formed in a reduced number of processes.

**[0021]** It is a still further object of the present invention to provide a novel field effect transistor with an improved gate overlap drain structure which provides such a relatively gentle effective impurity concentration profile free of any step-like abrupt variation in impurity concentration as relaxing a high field concentration.

**[0022]** It is yet a further object of the present invention to provide a novel field effect transistor with an improved gate overlap drain structure which provides such a relatively gentle effective impurity concentration profile as avoiding any shortened carrier life-time.

**[0023]** It is another object of the present invention to provide a novel method of forming an improved gate overlap drain structure of a field effect transistor, which is free from the above problems.

**[0024]** It is further another object of the present invention to provide a novel method of forming an improved gate overlap drain structure of a field effect transistor, which may be formed in a reduced number of processes.

**[0025]** It is still further another object of the present invention to provide a novel method of forming an improved gate overlap drain structure of a field effect transistor, which provides such a relatively gentle effective

impurity concentration profile free of any step-like abrupt variation in impurity concentration as relaxing a high field concentration.

**[0026]** It is yet further another object of the present invention to provide a novel method of forming an improved gate overlap drain structure of a field effect transistor, which provides such a relatively gentle effective impurity concentration profile as avoiding any shortened carrier life-time.

**[0027]** It is an additional object of the present invention to provide a novel liquid crystal display including a field effect transistor with an improved gate overlap drain structure, which is free from the above problems.

**[0028]** It is a further additional object of the present invention to provide a novel liquid crystal display including a field effect transistor with an improved gate overlap drain structure, which may be formed in a reduced number of processes.

**[0029]** It is a still further additional object of the present invention to provide a novel liquid crystal display including a field effect transistor with an improved gate overlap drain structure, which provides such a relatively gentle effective impurity concentration profile free of any step-like abrupt variation in impurity concentration as relaxing a high field concentration.

**[0030]** It is yet a further additional object of the present invention to provide a novel liquid crystal display including a field effect transistor with an improved gate overlap drain structure, which provides such a relatively gentle effective impurity concentration profile as avoiding any shortened carrier life-time.

**[0031]** It is moreover additional object of the present invention to provide a novel method of forming a liquid crystal display including a field effect transistor with an improved gate overlap drain structure, which is free from the above problems.

**[0032]** It is further more additional object of the present invention to provide a novel method of forming a liquid crystal display including a field effect transistor with an improved gate overlap drain structure, which may be formed in a reduced number of processes.

**[0033]** It is still more additional object of the present invention to provide a novel method of forming a liquid crystal display including a field effect transistor with an improved gate overlap drain structure, which provides such a relatively gentle effective impurity concentration profile free of any step-like abrupt variation in impurity concentration as relaxing a high field concentration.

**[0034]** It is yet more additional object of the present invention to provide a novel method of forming a liquid crystal display including a field effect transistor with an improved gate overlap drain structure, which provides such a relatively gentle effective impurity concentration profile as avoiding any shortened carrier life-time.

**[0035]** The present invention provides an improved gate-overlap-drain structure for a field effect transistor by a single pair of a single impurity implantation process and a single laser anneal process, wherein the improved

gate-overlap-drain structure includes lightly activated high impurity concentration regions exhibiting substantially the same function as the lightly doped drain regions, wherein the lightly activated high impurity concentration regions are bounded with high impurity concentration regions serving as source and drain regions. The boundaries are self-aligned to edges of a gate electrode. Side regions of the gate electrode overlap the lightly activated high impurity concentration regions. After a selective ion-implantation is carried out to form a high impurity concentration region, then a selective laser beam irradiation is carried out to a selected region of the high impurity concentration region for causing complete activation of the impurity in the laser-irradiated region of the high impurity concentration region, while causing incomplete activation of the impurity in the remaining heat-diffused region free from the laser irradiation in the high impurity concentration region. The completely or heavily activated region of the high impurity concentration region serve as the source/drain regions, while the incompletely or lightly activated region of the high impurity concentration region serve as the lightly doped drain regions. The lightly activated region has the same high impurity concentration as the source and drain regions, for which reason the lightly activated region is distinctly different from the lightly doped drain region which has a lower impurity concentration than the source and drain regions. The lightly activated high impurity concentration region, however, has a low concentration of effectively activated impurity which contributes to electrical conductivity because of the incomplete or light activation. Namely, only part of the actually implanted impurity is effectively activated and serves as effective carrier, while the remaining part of the actually implanted impurity does not serve as the carrier. The above and other objects, features and advantages of the present invention will be apparent from the following descriptions. Preferred embodiments according to the present invention will be described in detail with reference to the accompanying drawings.

**[0036]** FIGS. 1A through 1C are fragmentary cross sectional elevation views of field effect transistors in sequential steps involved in a conventional method of forming a typical example of a conventional lightly doped drain structure.

**[0037]** FIGS. 2A through 2D are fragmentary cross sectional elevation views of field effect transistors in sequential steps involved in a typical example of a conventional method of forming a gate-overlap-drain structure.

**[0038]** FIGS. 3A through 3D are fragmentary cross sectional elevation views of field effect transistors in sequential steps involved in another typical example of a conventional method of forming another gate-overlap-drain structure.

**[0039]** FIG. 4 is a diagram of an impurity concentration profile across the channel region, the low impurity concentration regions and the high impurity concentra-

tion regions of the field effect transistor having the gate-overlap drain structure.

**[0040]** FIG. 5 is a fragmentary cross sectional elevation view of a novel thin film field effect transistor with an improved gate-overlap-drain structure in accordance with the first embodiment of the present invention.

**[0041]** FIGS. 6A through 6I are fragmentary cross sectional elevation views of thin film field effect transistors with the improved gate-overlap-drain structure in sequential steps involved in a novel method of forming the transistor in accordance with the first embodiment of the present invention.

**[0042]** FIG. 7 is a diagram of an impurity concentration profile across the channel region, the lightly activated high impurity concentration layers and the sufficiently activated high impurity concentration layers of the field effect transistor having the improved gate-overlap drain structure shown in FIG. 5.

**[0043]** FIG. 8 is a fragmentary cross sectional elevation view of a novel thin film field effect transistor with an improved gate-overlap-drain structure in accordance with the second embodiment of the present invention.

**[0044]** FIGS. 9A through 9I are fragmentary cross sectional elevation views of thin film field effect transistors with the improved gate-overlap-drain structure in sequential steps involved in a novel method of forming the transistor in accordance with the third embodiment of the present invention.

**[0045]** FIGS. 10A through 10I are fragmentary cross sectional elevation views of thin film field effect transistors with the improved gate-overlap-drain structure in sequential steps involved in a novel method of forming the transistor in accordance with the fourth embodiment of the present invention.

**[0046]** FIGS. 11A through 11I are fragmentary cross sectional elevation views of thin film field effect transistors with the improved gate-overlap-drain structure in sequential steps involved in a novel method of forming the transistor in accordance with the fifth embodiment of the present invention.

**[0047]** FIG. 12 is a fragmentary cross sectional elevation view of a novel thin film field effect transistor with an improved gate-overlap-drain structure in accordance with the sixth embodiment of the present invention.

**[0048]** A first aspect of the present invention is a semiconductor structure in a field effect transistor. The structure comprises : a semiconductor layer ; an insulating layer overlying the semiconductor layer; and a gate electrode for controlling an electric field applied to at least a part of the semiconductor layer. The semiconductor layer further includes : at least a lightly activated high impurity concentration layer and at least a sufficiently activated high impurity concentration layer. The lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than the first implanted-impurity concentration value. The sufficiently activated high impurity

concentration layer is bounded with the lightly activated high impurity concentration layer. The sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as the first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than the first effectively-activated-impurity concentration range.

**[0049]** It is also preferable that the lightly activated high impurity concentration layer is positioned under the gate electrode. Further, preferably, a boundary between the lightly activated high impurity concentration layer and the sufficiently activated high impurity concentration layer is aligned to an edge of the gate electrode. Furthermore, it is preferable that the lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in the first effectively-activated-impurity concentration range as a distance from the sufficiently activated high impurity concentration layer is increased. It is further preferable that the sufficiently activated high impurity concentration layer is sufficiently activated by a laser beam irradiation, while the lightly activated high impurity concentration layer is insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layer. It is also preferable that the sufficiently activated high impurity concentration layer serves as a drain region, while the lightly activated high impurity concentration layer serves as a field concentration relaxation region. As a typical example, it is possible that the semiconductor layer comprises : a channel region ; the lightly activated high impurity concentration layers adjacent to opposite sides of the channel region ; and the sufficiently activated high impurity concentration layers adjacent to opposite outsides of the lightly activated high impurity concentration layers. The sufficiently activated high impurity concentration layers serve as source and drain regions. Respective boundaries between the lightly activated high impurity concentration layers and the sufficiently activated high impurity concentration layers are aligned to opposite side edges of the gate electrode.

**[0050]** A second aspect of the present invention is a semiconductor structure in a field effect transistor. The structure comprises : a semiconductor layer ; an insulating layer overlying the semiconductor layer; and a gate electrode for controlling an electric field applied to at least a part of the semiconductor layer. The semiconductor layer further includes : at least a sufficiently activated high impurity concentration layer and at least a lightly activated high impurity concentration layer. The sufficiently activated high impurity concentration layer is sufficiently activated by a laser beam irradiation. The lightly activated high impurity concentration layer is bounded with the sufficiently activated high impurity concentration layer. The lightly activated high impurity concentration layer is insufficiently activated by a thermal diffusion from the sufficiently activated high impurity

concentration layer.

**[0051]** It is preferable that the lightly activated high impurity concentration layer is positioned under the gate electrode. It is further preferable that a boundary between the lightly activated high impurity concentration layer and the sufficiently activated high impurity concentration layer is aligned to an edge of the gate electrode. It is furthermore preferable that the lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value as a distance from the sufficiently activated high impurity concentration layer is increased. It is moreover preferable that the lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than the first implanted-impurity concentration value, and that the sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as the first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than the first effectively-activated-impurity concentration range. It is also preferable that the sufficiently activated high impurity concentration layer serves as a drain region, while the lightly activated high impurity concentration layer serves as a field concentration relaxation region. As a typical example, it is possible that the semiconductor layer comprises : a channel region ; the lightly activated high impurity concentration layers adjacent to opposite sides of the channel region ; and the sufficiently activated high impurity concentration layers adjacent to opposite out-sides of the lightly activated high impurity concentration layers. The sufficiently activated high impurity concentration layers serve as source and drain regions. Respective boundaries between the lightly activated high impurity concentration layers and the sufficiently activated high impurity concentration layers are aligned to opposite side edges of the gate electrode.

**[0052]** A third aspect of the present invention is a field effect transistor including : a substrate ; a gate insulating film over the substrate ; a gate electrode over the gate insulating film ; and source/drain regions over and substrate and under the gate insulating film. The drain region further includes : at least a lightly activated high impurity concentration layer and at least a sufficiently activated high impurity concentration layer. The lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than the first implanted-impurity concentration value. The sufficiently activated high impurity concentration layer is bounded with the lightly activated high impurity concentration layer. The sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as the first implanted-impurity concentration value, and a second effectively-activated-impurity concentration

value which is higher than the first effectively-activated-impurity concentration range.

**[0053]** It is preferable that the lightly activated high impurity concentration layer is positioned under the gate electrode. It is further preferable that a boundary between the lightly activated high impurity concentration layer and the sufficiently activated high impurity concentration layer is aligned to an edge of the gate electrode. It is further more preferable that the lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in the first effectively-activated-impurity concentration range as a distance from the sufficiently activated high impurity concentration layer is increased. It is moreover preferable that the sufficiently activated high impurity concentration layer is sufficiently activated by a laser beam irradiation, while the lightly activated high impurity concentration layer is insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layer. It is also preferable that the source region has the same structure as the drain region.

**[0054]** A fourth aspect of the present invention is a field effect transistor including : a substrate ; a gate insulating film over the substrate ; a gate electrode over the gate insulating film ; and source/drain regions over and substrate and under the gate insulating film. The drain region further includes : at least a sufficiently activated high impurity concentration layer and at least a lightly activated high impurity concentration layer. The sufficiently activated high impurity concentration layer is sufficiently activated by a laser beam irradiation. The lightly activated high impurity concentration layer is bounded with the sufficiently activated high impurity concentration layer. The lightly activated high impurity concentration layer is insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layer. It is preferable that the lightly activated high impurity concentration layer is positioned under the gate electrode. It is further preferable that a boundary between the lightly activated high impurity concentration layer and the sufficiently activated high impurity concentration layer is aligned to an edge of the gate electrode. It is further more preferable that the lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value as a distance from the sufficiently activated high impurity concentration layer is increased. It is moreover preferable that the lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than the first implanted-impurity concentration value ; and that the sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as the first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than the first effectively-activated-impurity concentra-

tion range. It is also preferable that the source region has the same structure as the drain region.

**[0055]** A fifth aspect of the present invention is a field effect transistor including : a substrate ; a gate insulating film over the substrate ; a gate electrode over the gate insulating film ; and source/drain regions over and substrate and under the gate insulating film. Each of the source/drain regions further includes : at least a lightly activated high impurity concentration layer and at least a sufficiently activated high impurity concentration layer. The lightly activated high impurity concentration layer is positioned under the gate electrode. The lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than the first implanted-impurity concentration value. The sufficiently activated high impurity concentration layer is bounded with the lightly activated high impurity concentration layer. A boundary between the lightly activated high impurity concentration layer and the sufficiently activated high impurity concentration layer is aligned to an edge of the gate electrode. The sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as the first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than the first effectively-activated-impurity concentration range. The lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in the first effectively-activated-impurity concentration range as a distance from the sufficiently activated high impurity concentration layer is increased. It is preferable that the sufficiently activated high impurity concentration layer is sufficiently activated by a laser beam irradiation, while the lightly activated high impurity concentration layer is insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layer. It is also preferable that the field effect transistor is a thin film field effect transistor.

**[0056]** A sixth aspect of the present invention is a liquid crystal display including a plurality of pixels, each pixel having a liquid crystal cell and a switching device. The switching device further comprises : a thin film field effect transistor including : a substrate ; a gate insulating film over the substrate ; a gate electrode over the gate insulating film ; and source/drain regions over and substrate and under the gate insulating film. Each of the source/drain regions further includes : at least a lightly activated high impurity concentration layer and at least a sufficiently activated high impurity concentration layer. The lightly activated high impurity concentration layer is positioned under the gate electrode. The lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than the first implanted-impurity concentration value.

The sufficiently activated high impurity concentration layer is bounded with the lightly activated high impurity concentration layer. A boundary between the lightly activated high impurity concentration layer and the sufficiently activated high impurity concentration layer is aligned to an edge of the gate electrode. The sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as the first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than the first effectively-activated-impurity concentration range. The lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in the first effectively-activated-impurity concentration range as a distance from the sufficiently activated high impurity concentration layer is increased.

**[0057]** A seventh aspect of the present invention is a method of forming a semiconductor structure in a field effect transistor. The method comprises the following steps. A resist pattern is selectively formed over a first selected region of a semiconductor layer. A selective impurity-implantation is then carried out by use of the resist pattern as a mask for selectively implanting an impurity into the semiconductor layer except under the resist pattern at a first implanted-impurity concentration, to define at least an impurity-implanted region in the semiconductor layer. The resist pattern is then removed from the semiconductor layer. A gate electrode is selectively formed over a second selected region of the semiconductor layer. The second selected region completely encompasses the first selected region and also encompasses an outside region adjacent to a periphery of the first selected region. At least a gate-overlapped part of then impurity-implanted region is covered by the gate electrode, while a remaining non-overlapped part of then impurity-implanted region is not covered by the gate electrode. A selective laser beam irradiation to the remaining non-overlapped part is carried out by use of the gate electrode as a mask. The remaining non-overlapped part is sufficiently activated upon the selective laser beam irradiation. The remaining non-overlapped part becomes at least a sufficiently activated high impurity concentration layer. The gate-overlapped part is insufficiently activated by a thermal diffusion from the remaining non-overlapped part. The gate-overlapped part becomes at least a lightly activated high impurity concentration layer.

**[0058]** It is preferable that the lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than the first implanted-impurity concentration value ; and that the sufficiently activated high impurity concentration layer is bounded with the lightly activated high impurity concentration layer, and the sufficiently activated high impurity concentration layer has a second implanted-impurity

concentration value which is substantially the same as the first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than the first effectively-activated-impurity concentration range.

**[0059]** It is further preferable that a boundary between the lightly activated high impurity concentration layer and the sufficiently activated high impurity concentration layer is aligned to an edge of the gate electrode. It is further more preferable that the lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in the first effectively-activated-impurity concentration range as a distance from the sufficiently activated high impurity concentration layer is increased.

**[0060]** As a typical example, it is possible that a dummy layer is additionally formed over at least an entirety of the semiconductor layer before selectively forming a resist pattern over the dummy layer for selectively implanting the impurity through the dummy layer into the semiconductor layer in the selective impurity implantation. The dummy layer may be removed in addition to the removal of the resist pattern before a gate insulating film is formed prior to the step of selectively forming the gate electrode over the gate insulating film. The dummy layer may remain as the gate insulating film, so that the gate electrode is selectively formed over the dummy layer as the gate insulating film.

**[0061]** An eighth aspect of the present invention is a method of forming a semiconductor structure in a field effect transistor, comprising the following steps. A selective impurity-implantation is carried out for selectively implanting an impurity into a semiconductor layer, to define at least an impurity-implanted region in the semiconductor layer. A selective laser beam irradiation to at least a selected part of then impurity-implanted region is then carried out, whereby the selected part of then impurity-implanted region is sufficiently activated upon the selective laser beam irradiation, and the selected part becomes at least a sufficiently activated high impurity concentration layer. On the other hand, a remaining non-selected part of then impurity-implanted region is insufficiently activated by a thermal diffusion from the selected part, and the remaining non-selected part becomes at least a lightly activated high impurity concentration layer.

**[0062]** It is preferable that the lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than the first implanted-impurity concentration value, and also that the sufficiently activated high impurity concentration layer is bounded with the lightly activated high impurity concentration layer, and the sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as the first implanted-impurity concentration value, and a second effectively-activated-impurity concen-

tration value which is higher than the first effectively-activated-impurity concentration range.

**[0063]** It is further preferable that a boundary between the lightly activated high impurity concentration layer and the sufficiently activated high impurity concentration layer is aligned to an edge of the gate electrode. It is further more preferable that the lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in the first effectively-activated-impurity concentration range as a distance from the sufficiently activated high impurity concentration layer is increased.

**[0064]** In accordance with the present invention, the above-described improved gate-overlap-drain structure is obtained by a single pair of a single impurity implantation process and a single laser anneal process, wherein the improved gate-overlap-drain structure includes lightly activated high impurity concentration regions exhibiting substantially the same function as the lightly doped drain regions, wherein the lightly activated high impurity concentration regions are bounded with high impurity concentration regions serving as source and drain regions. The boundaries are self-aligned to edges of a gate electrode. Side regions of the gate electrode overlap the lightly activated high impurity concentration regions.

**[0065]** As described above, in accordance with the conventional gate-overlap-drain structure, the lightly doped drain regions are positioned under the side regions of the gate electrode to suppress hot carrier traps in the vicinity of the drain region and also to reduce the light leakage. The conventional gate-overlap-drain structure is, however, disadvantage in the necessary complicated manufacturing process.

**[0066]** In the meantime, the manufacturing processes for the field effect transistors may generally include heat treatments such as activation anneals for activating the implanted impurity and silicidation anneals for causing silicidation reactions to form silicide layers over the source and drain regions. Those anneals may include, but not limited to, a furnace anneal using an electric furnace, a rapid thermal anneal using an infrared ray lamp, and a laser anneal using a laser beam.

**[0067]** For example, an excited-dimer laser may be used for the activation anneal.

**[0068]** The excited-dimer laser is a pulse laser having a short width of one-shot-pulse, for which reason a laser energy is likely to be absorbed in a relatively shallow region. This means it easy to control a depth of the activation region. Therefore, the excited-dimer laser anneal is suitable for activation of the low impurity concentration region of the lightly doped drain structure. In general, the purpose of the activation anneal is to cause a complete activation of the implanted impurity into the laser-irradiated region. The present inventor, however, proposed for utilizing a phenomenon that there is a difference in degree of activation between a laser-irradiated region having received a laser irradiation and a heat-

diffused region having received a thermal diffusion from the laser irradiation, but not received the laser irradiation.

**[0069]** The furnace anneal and the rapid thermal anneal cause non-localized and non-selected heat supply to the entirety of the substrate, for which reason those anneals are incapable of controlling the degree of the activation of the implanted impurity for respective regions. In contrast, the laser anneal is advantageous in that the laser energy is absorbed in the relatively shallow region, and also the thermal diffusion is limited within a relatively narrow region. This allows a highly localized control of the degree of activation of the implanted impurity. After a selective ion-implantation is carried out to form a high impurity concentration region, then a selective laser beam irradiation is carried out to a selected region of the high impurity concentration region for causing complete activation of the impurity in the laser-irradiated region of the high impurity concentration region, while causing incomplete activation of the impurity in the remaining heat-diffused region free from the laser irradiation in the high impurity concentration region. The completely or heavily activated region of the high impurity concentration region serve as the source/drain regions, while the incompletely or lightly activated region of the high impurity concentration region serve as the lightly doped drain regions.

**[0070]** The lightly activated region has the same high impurity concentration as the source and drain regions, for which reason the lightly activated region is distinctly different from the lightly doped drain region which has a lower impurity concentration than the source and drain regions. The lightly activated high impurity concentration region, however, has a low concentration of effectively activated impurity which contributes to electrical conductivity because of the incomplete or light activation. Namely, only part of the actually implanted impurity is effectively activated and serves as effective carrier, while the remaining part of the actually implanted impurity does not serve as the carrier. For this reason, the lightly activated high impurity concentration region may exhibit substantially the same function as the lightly doped drain region.

**[0071]** The following embodiments are typical examples for practicing the foregoing aspects of the present invention. Although the subject matters of the present invention have been described in details, the following additional descriptions in one or more typical preferred embodiments or examples will be made with reference to the drawings for making it easy to understand the typical modes for practicing the foregoing aspects of the present invention.

#### FIRST EMBODIMENT:

**[0072]** A first embodiment according to the present invention will be described in detail with reference to the drawings. FIG. 5 is a fragmentary cross sectional ele-

vation view of a novel thin film field effect transistor with an improved gate-overlap-drain structure in accordance with the first embodiment of the present invention. A thin film field effect transistor is provided over a glass substrate 1. An under-coat layer 2 overlies the glass substrate 1. A semiconductor layer 3 is selectively provided over the under-coat layer 2. Typically, the semiconductor layer 3 may be made of polysilicon. The semiconductor layer 3 further comprises a channel layer 3a, lightly activated high impurity concentration layers 3b in contact directly with opposite sides of the channel layer 3a, and sufficiently activated high impurity concentration layers 3c in contact directly with outsides of the lightly activated high impurity concentration layers 3b. A gate insulating film 4 extends over the semiconductor layer 3 and the under-coat layer 2. A gate electrode 5 is selectively provided over the gate insulating film 4. The lightly activated high impurity concentration layers 3b are positioned under the gate electrode 5, so that the lightly activated high impurity concentration layers 3b are covered by the gate electrode 5.

**[0073]** The sufficiently activated high impurity concentration layers 3c are positioned under outsides of the gate electrode 5, so that the sufficiently activated high impurity concentration layers 3c are not covered by the gate electrode 5. Respective boundaries between the sufficiently activated high impurity concentration layers 3c and the lightly activated high impurity concentration layers 3b are self-aligned to the opposite side-edges of the gate electrode 5. An inter-layer insulator 6 extends over the gate electrode 5 and the gate insulating film 4. Contact holes are provided in laminations of the gate insulating film 4 and the inter-layer insulator 6 but over the sufficiently activated high impurity concentration layers 3c. Source/drain electrodes 7 are selectively provided in the contact holes and over the inter-layer insulator 6, so that the source/drain electrodes 7 are in contact with the sufficiently activated high impurity concentration layers 3c. The sufficiently activated high impurity concentration layers 3c serve as source/drain regions. In addition, the transistor has a pair of top and bottom light shielding layers 9b and 9a, wherein the top light shielding layer 9b overlies the transistor, while the bottom light shielding layer 9a underlies the glass substrate 1 of the transistor. The lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c have the same impurity concentration. The impurity implanted in the sufficiently activated high impurity concentration layers 3c are sufficiently activated by direct laser beam irradiation in the laser anneal process. The impurity implanted in the lightly activated high impurity concentration layers 3b are lightly or insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layers 3c. The lightly activated high impurity concentration layers 3b have not received any laser irradiation. Namely, the activation energy for the lightly activated high impurity concentration layers 3b depends

on the thermal diffusion from the sufficiently activated high impurity concentration layers 3c, for which reason the activation is insufficient. This insufficient activation depending on the thermal diffusion gives rise to a lower concentration of the effectively activated impurity than the implanted-impurity concentration. The effectively activated impurity only may contribute to provide an electrical conductivity. For those reasons, the lightly activated high impurity concentration layers 3b exhibits substantially the same function as the lightly doped drain regions. Further, the thermal diffusion into the lightly activated high impurity concentration layers 3b is directed inwardly from the sufficiently activated high impurity concentration layers 3c which have received the laser irradiation in the laser anneal process. For this reason, the heat energy absorbed into the lightly activated high impurity concentration layers 3b may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Therefore, the degree of the activation of the impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Namely, the concentration profile of the effectively activated impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Accordingly, the concentration profile of the effectively activated impurity across the channel region 3a, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c are free of any step-like variation or any other abrupt and rapid variation, whereby no extensively high field concentration is caused.

**[0074]** FIGS. 6A through 6I are fragmentary cross sectional elevation views of thin film field effect transistors with the improved gate-overlap-drain structure in sequential steps involved in a novel method of forming the transistor in accordance with the first embodiment of the present invention. As shown in FIG. 6A, a transparent insulating substrate 1 such as a glass substrate 1 is prepared. An under-coat layer 2 is formed over the transparent insulating substrate 1. The under-coat layer 2 may typically have a thickness in the range of 100-500 nm and more preferably about 300 nm. The under-coat layer 2 is provided in order to prevent any further impurity diffusion from the substrate 1 to any overlying layers, for example, a semiconductor layer 3. The under-coat layer 2 is not necessarily needed if the above impurity diffusion is not problem. The under-coat layer 2 may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method, a sputtering method and a dipping method. The under-coat layer

2 may typically comprise, but not limited to, any one of a silicon oxide layer, a silicon nitride layer, and laminations thereof.

**[0075]** As shown in FIG. 6B, a polycrystal silicon layer 3 is formed over the under-coat layer 2. A typical example of forming the polycrystal silicon layer 3 is that an amorphous silicon layer as a precursor is first formed over the under-coat layer 2, before the amorphous silicon layer is then crystallized by a laser irradiation. The amorphous silicon layer may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method and a sputtering method. A typical thickness of the amorphous silicon layer may be in the range of 50-100 nm. Instead of the laser irradiation for crystallization, a solid-state growth method may also be available.

**[0076]** As shown in FIG. 6C, a resist pattern is selectively formed over the polycrystal silicon layer 3 by use of the known lithography technique. The polycrystal silicon layer 3 is then patterned into an island shape by an anisotropic etching technique using the resist pattern as a mask. The used resist pattern is then removed.

**[0077]** As shown in FIG. 6D, another resist pattern 10 is also selectively formed over the patterned polycrystal silicon layer 3. A selective impurity-implantation process is carried out by use of the resist pattern 10 as a mask, so that impurity ions 11 are selectively implanted into the patterned polycrystal silicon layer 3 except under the resist pattern 10, thereby to form high impurity concentration regions 3a in the patterned polycrystal silicon layer 3, except under the resist pattern 10. The impurity may, for example, be phosphorous but not limited thereto. A size of the resist pattern 10 is smaller than an intended gate electrode formation region by a size of lightly activated high impurity concentration layers. A typical example of the doping conditions is that an acceleration voltage is approximately 20 keV, and a dose is in the range of  $8E14$  /cm<sup>2</sup> through  $3E15$  /cm<sup>2</sup>. Whereas the above typical example of the doping conditions has been shown, the acceleration voltage and the dose are not limited to the above value and range, but should rather be decided by taking into account the correlation to the laser anneal process to be described below. The used resist pattern 10 is then removed.

**[0078]** As shown in FIG 6E, a gate insulating film 4 is then formed over the semiconductor layer 3 and the under-coat layer 2. The gate insulating film 4 may comprise any available insulating film including but not limited to silicon oxide and silicon nitride. The gate insulating film 4 may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method and a sputtering method. The thickness of the gate insulating film 4 may advantageously be decided by taking into account a driving condition of the device and a driving voltage. A typical example of the thickness of the gate insulating film 4 may be in the range of 30-200 nm,

and preferably 50-100 nm.

**[0079]** As shown in FIG. 6F, a conductive film is deposited over the gate insulating film 4. The conductive film may comprise any available conductive film, for example, a silicide film, a metal film, and an impurity-doped silicon film. The deposition may typically be made by a plasma enhanced chemical vapor deposition method. A typical example of the thickness of the conductive film may be in the range of 200-400 nm. A resist pattern is selectively formed over the conductive film by the know lithography technique. An anisotropic etching process is then carried out by use of the resist pattern as a mask to define the conductive film into a gate electrode 5. Since the resist pattern overlaps predetermined inside regions of the high impurity concentration regions 3a of the semiconductor layer 3, then the gate electrode 5 also overlaps predetermined inside regions of the high impurity concentration regions 3a of the semiconductor layer 3. In this typical example, the above overlap appears symmetrically both the source and drain sides, but it should be noted that the above overlap is needed at least in the drain side. Namely, it is possible that the above overlap appears only in the drain side, or also possible that the above overlap appears asymmetrically both in the source and drain sides. It should also be noted that if the transistor is for the switching transistor utilizing the inversion between the source and drain regions, then the above overlap should appear symmetrically in both the source and drain sides.

**[0080]** As shown in FIG. 6G, a selective laser irradiation process is then carried out by use of the gate electrode 5 as a mask, so that a laser beam 12 is irradiated through the gate insulating film 4 to the semiconductor layer 3, except under the gate electrode 5 for the purpose of selective activation of the semiconductor layer 3, except under the gate electrode 5. The non-overlapped regions of the semiconductor layer 3 do receive the laser beam irradiation, whereby the non-overlapped regions become sufficiently activated high impurity concentration layers 3c. The impurity in the non-overlapped regions or the sufficiently activated high impurity concentration layers 3c is sufficiently activated and the most of the impurity becomes effectively activated impurity which contributes to the electrical conductivity. On the other hand, the gate-overlapped regions of the semiconductor layer 3 do not receive the laser beam irradiation but do receive a thermal diffusion from the non-overlapped regions, whereby the gate-overlapped regions become lightly activated high impurity concentration layers 3b. The impurity in the gate-overlapped regions or the lightly activated high impurity concentration layers 3b is insufficiently activated and the minority of the impurity becomes effectively activated impurity which contributes to the electrical conductivity. Namely, the lightly activated high impurity concentration layers 3b has a lower concentration of the effectively activated impurity, which contributes to the electrical conductivity, than the concentration of the implanted-impurity.

**[0081]** Namely, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c have the same impurity concentration. The impurity implanted in the sufficiently activated high impurity concentration layers 3c are sufficiently activated by direct laser beam irradiation in the laser anneal process. The impurity implanted in the lightly activated high impurity concentration layers 3b are lightly or insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layers 3c. The lightly activated high impurity concentration layers 3b have not received any laser irradiation. Namely, the activation energy for the lightly activated high impurity concentration layers 3b depends on the thermal diffusion from the sufficiently activated high impurity concentration layers 3c, for which reason the activation is insufficient. This insufficient activation depending on the thermal diffusion gives rise to a lower concentration of the effectively activated impurity than the implanted-impurity concentration. The effectively activated impurity only may contribute to provide an electrical conductivity. For those reasons, the lightly activated high impurity concentration layers 3b exhibits substantially the same function as the lightly doped drain regions. Further, the thermal diffusion into the lightly activated high impurity concentration layers 3b is directed inwardly from the sufficiently activated high impurity concentration layers 3c which have received the laser irradiation in the laser anneal process. For this reason, the heat energy absorbed into the lightly activated high impurity concentration layers 3b may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Therefore, the degree of the activation of the impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Namely, the concentration profile of the effectively activated impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Accordingly, the concentration profile of the effectively activated impurity across the channel region free of impurity implantation, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c are free of any step-like variation or any other abrupt and rapid variation, whereby no extensively high field concentration is caused. The energy of the laser irradiation may be decided by taking into account respective thicknesses of the semiconductor layer 3 and the gate insulating film 4 as well as respective surface reflectivities thereof, and also with reference to an energy which causes semiconductor or silicon of the semiconductor layer 3 to be melt.

A typical example of the laser irradiation energy may be in the range of 250-300 mJ, but not limited thereto.

**[0082]** As shown in FIG. 6H, an inter-layer insulator 6 is deposited over the gate electrode 5 and the gate insulating film 4. Contact holes 8 are selectively formed in the inter-layer insulator 6 and the gate insulating film 4 and over the sufficiently activated high impurity concentration layers 3c serving as source and drain regions.

**[0083]** As shown in FIG. 6I, a metal film is also deposited over the inter-layer insulator 6 and within the contact holes 8, so that the metal film is made into contact with the sufficiently activated high impurity concentration layers 3c. The deposition may be made by any available method, for example, a sputtering method. A typical example of the thickness of the metal film may be in the range of 300-1000 nm, but not limited thereto. A typical example of material for the metal film may be aluminum, but not limited thereto. The metal film is then patterned into source and drain electrodes 7 by use of a known lithography technique and a subsequent anisotropic etching process, thereby forming the thin film field effect transistor including the improved gate-overlap-drain structure. As described above, the above novel method for forming the improved gate-overlap-drain structure utilizes a single pair of the above-described single impurity implantation process and the above-described single laser anneal process. The improved gate-overlap-drain structure includes the lightly activated high impurity concentration regions 3b exhibiting substantially the same function as the lightly doped drain regions. The lightly activated high impurity concentration regions 3b are bounded with the sufficiently activated high impurity concentration layers 3c serving as source and drain regions. The boundaries are self-aligned to opposite side edges of the gate electrode 5. Side regions of the gate electrode 5 overlap the lightly activated high impurity concentration regions 3b. After the above-described selective ion-implantation is carried out to form a high impurity concentration region 3a, then the above-described selective laser beam irradiation is carried out to the non-overlapped regions of the high impurity concentration region 3a for causing sufficient activation of the impurity in the laser-irradiated regions 3c of the high impurity concentration region 3a, while causing in sufficient activation of the impurity in the remaining heat-diffused regions 3b free from the laser irradiation in the high impurity concentration region 3a. The completely or highly activated regions 3c of the high impurity concentration region 3a serve as the source/drain regions, while the incompletely or lightly activated regions 3b of the high impurity concentration region 3a serve as the lightly doped drain regions. The lightly activated high impurity concentration layers 3b have the same high impurity concentration as the source and drain regions or the sufficiently activated high impurity concentration layers 3c, for which reason the lightly activated high impurity concentration layers 3b are distinctly different from

the lightly doped drain region which has a lower impurity concentration than the source and drain regions. The lightly activated high impurity concentration layers 3b, however, have a low concentration of the effectively activated impurity which contributes to electrical conductivity because of the incomplete or light activation depending only upon the thermal diffusion from the sufficiently activated high impurity concentration layers 3c.

**[0084]** FIG. 7 is a diagram of an effectively activated impurity concentration profile across the channel region, the lightly activated high impurity concentration layers and the sufficiently activated high impurity concentration layers of the field effect transistor having the improved gate-overlap drain structure shown in FIG. 5. The thermal diffusion into the lightly activated high impurity concentration layers 3b is directed inwardly from the sufficiently activated high impurity concentration layers 3c which have received the laser irradiation in the laser anneal process. For this reason, the heat energy absorbed into the lightly activated high impurity concentration layers 3b may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Therefore, the degree of the activation of the impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Namely, the concentration profile of the effectively activated impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c.

**[0085]** Accordingly, as shown in FIG. 7, the concentration profile of the effectively activated impurity across the channel region 3a, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c are free of any step-like variation or any other abrupt and rapid variation, whereby no extensively high field concentration is caused. Namely, the above-improved gate-overlap-drain structure provides a highly effective controllability to hot carriers and also allow a long carrier life-time due to no traps of the hot carriers. The above-described thin film field effect transistor may be applicable to a variety of transistors, typically, for example, a switching transistor acting for ON-OFF of each pixel included in a display device such as an active matrix liquid crystal display. Further, the transistor may be applicable to a variety of display devices and semiconductor devices. As described above, in accordance with the improved gate-overlap-drain structure, the lightly activated high impurity concentration layers 3b are covered by the gate electrode 5. This structure prevents an incidence of light reflected by respective layers in an active matrix substrate of the display into the lightly activated high impu-

urity concentration layers 3b. Namely, it is ensured to avoid the undesirable leakage of light or possible incidence of light into the lightly activated high impurity concentration layers 3b. In accordance with the above-described typical example, the transistor is formed over the glass substrate as the transparent insulating substrate. The present invention is of course applicable to when the transistor is formed over a variety of substrate, for example, a semiconductor substrate such as a silicon substrate.

#### SECOND EMBODIMENT:

[0086] A second embodiment according to the present invention will be described in detail with reference to the drawings. FIG. 8 is a fragmentary cross sectional elevation view of a novel thin film field effect transistor with an improved gate-overlap-drain structure in accordance with the second embodiment of the present invention. A thin film field effect transistor is provided over a silicon substrate 13. Isolation insulating films 14 are selectively provided over the silicon substrate 13 to define a field region of the silicon substrate 13. A gate insulating film 4 is provided over the field region of the silicon substrate 13. A gate electrode is selectively provided over the gate insulating film 4. Lightly activated high impurity concentration layers 3b are selectively provided in the silicon substrate 13, wherein the lightly activated high impurity concentration layers 3b are adjacent to opposite sides of a channel layer. Further, sufficiently activated high impurity concentration layers 3c are also selectively provided in the silicon substrate 13, wherein the sufficiently activated high impurity concentration layers 3c are adjacent to outsides of the lightly activated high impurity concentration layers 3b. The lightly activated high impurity concentration layers 3b are positioned under the gate electrode 5, so that the lightly activated high impurity concentration layers 3b are covered by the gate electrode 5. The sufficiently activated high impurity concentration layers 3c are positioned under outsides of the gate electrode 5, so that the sufficiently activated high impurity concentration layers 3c are not covered by the gate electrode 5. Respective boundaries between the sufficiently activated high impurity concentration layers 3c and the lightly activated high impurity concentration layers 3b are self-aligned to the opposite side-edges of the gate electrode 5. An inter-layer insulator 6 extends over the gate electrode 5 and the gate insulating film 4. Contact holes are provided in laminations of the gate insulating film 4 and the inter-layer insulator 6 but over the sufficiently activated high impurity concentration layers 3c. Source/drain electrodes 7 are selectively provided in the contact holes and over the inter-layer insulator 6, so that the source/drain electrodes 7 are in contact with the sufficiently activated high impurity concentration layers 3c. The sufficiently activated high impurity concentration layers 3c serve as source/drain regions. The lightly ac-

tivated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c have the same impurity concentration. The impurity implanted in the sufficiently activated high impurity concentration layers 3c are sufficiently activated by direct laser beam irradiation in the laser anneal process. The impurity implanted in the lightly activated high impurity concentration layers 3b are lightly or insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layers 3c. The lightly activated high impurity concentration layers 3b have not received any laser irradiation. Namely, the activation energy for the lightly activated high impurity concentration layers 3b depends on the thermal diffusion from the sufficiently activated high impurity concentration layers 3c, for which reason the activation is insufficient. This insufficient activation depending on the thermal diffusion gives rise to a lower concentration of the effectively activated impurity than the implanted-impurity concentration. The effectively activated impurity only may contribute to provide an electrical conductivity. For those reasons, the lightly activated high impurity concentration layers 3b exhibits substantially the same function as the lightly doped drain regions. Further, the thermal diffusion into the lightly activated high impurity concentration layers 3b is directed inwardly from the sufficiently activated high impurity concentration layers 3c which have received the laser irradiation in the laser anneal process. For this reason, the heat energy absorbed into the lightly activated high impurity concentration layers 3b may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Therefore, the degree of the activation of the impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Namely, the concentration profile of the effectively activated impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Accordingly, the concentration profile of the effectively activated impurity across the channel region, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c are free of any step-like variation or any other abrupt and rapid variation, whereby no extensively high field concentration is caused. The above improved gate-overlap-drain structure may be formed by a single pair of a single impurity implantation process and a later single laser anneal process for selective activation. The impurity implantation process is carried out by using a resist pattern having a smaller size than the gate electrode 5 as a mask to form high impurity concentration regions which include both the

lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c. After the gate electrode 5 is formed, then the single laser anneal process is carried out by using the gate electrode as a mask for selective activation of the high impurity concentration regions, whereby the laser-irradiated regions non-overlapped and non-covered by the gate electrode 5 are sufficiently activated and become the sufficiently activated high impurity concentration layers 3c, while the laser-irradiation-free regions overlapped and covered by the gate electrode 5 are insufficiently activated by the thermal diffusion from the laser-irradiated regions and become the lightly activated high impurity concentration layers 3b.

### THIRD EMBODIMENT:

**[0087]** A third embodiment according to the present invention will be described in detail with reference to the drawings. This third embodiment is different from the first embodiment but only parts of the processes for forming the transistor, for which reason the following descriptions will focus on the sequential processes. FIGS. 9A through 9I are fragmentary cross sectional elevation views of thin film field effect transistors with the improved gate-overlap-drain structure in sequential steps involved in a novel method of forming the transistor in accordance with the third embodiment of the present invention. As shown in FIG. 9A, a transparent insulating substrate 1 such as a glass substrate 1 is prepared. An under-coat layer 2 is formed over the transparent insulating substrate 1. The under-coat layer 2 may typically have a thickness in the range of 100-500 nm and more preferably about 300 nm. The under-coat layer 2 is provided in order to prevent any further impurity diffusion from the substrate 1 to any overlying layers, for example, a semiconductor layer 3. The under-coat layer 2 is not necessarily needed if the above impurity diffusion is not problem. The under-coat layer 2 may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method, a sputtering method and a dipping method. The under-coat layer 2 may typically comprise, but not limited to, any one of a silicon oxide layer, a silicon nitride layer, and laminations thereof.

**[0088]** As shown in FIG. 9B, a polycrystal silicon layer 3 is formed over the under-coat layer 2. A typical example of forming the polycrystal silicon layer 3 is that an amorphous silicon layer as a precursor is first formed over the under-coat layer 2, before the amorphous silicon layer is then crystallized by a laser irradiation. The amorphous silicon layer may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method and a sputtering method. A typical thickness of the amorphous silicon layer may be in the range of 50-100 nm. Instead of the laser irradiation

for crystallization, a solid-state growth method may also be available.

**[0089]** As shown in FIG. 9C, a resist pattern is selectively formed over the polycrystal silicon layer 3 by use of the known lithography technique. The polycrystal silicon layer 3 is then patterned into an island shape by an anisotropic etching technique using the resist pattern as a mask. The used resist pattern is then removed. In the above-described first embodiment, the polycrystal silicon layer 3 is directly subjected to the impurity implantation. This direct exposure to the impurity implantation may allow the polycrystal silicon layer 3 to be damaged in crystal structure. In order to avoid the polycrystal silicon layer 3 from the possibility of damage in the crystal structure, the following addition process is carried out.

**[0090]** As shown in FIG. 9D, a dummy oxide film 15 is additionally formed over the polycrystal silicon layer 3 and the under-coat layer 2, before another resist pattern 10 is also selectively formed over the dummy oxide film 15. A selective impurity-implantation process is carried out by use of the resist pattern 10 as a mask, so that impurity ions 11 are selectively implanted through the dummy oxide film 15 into the patterned polycrystal silicon layer 3 except under the resist pattern 10, thereby to form high impurity concentration regions 3a in the patterned polycrystal silicon layer 3, except under the resist pattern 10. The impurity may, for example, be phosphorous but not limited thereto. A size of the resist pattern 10 is smaller than an intended gate electrode formation region by a size of lightly activated high impurity concentration layers.

**[0091]** As shown in FIG. 9E, the used resist pattern 10 is then removed. Further, the used dummy oxide film 15 is also removed.

**[0092]** As shown in FIG. 9F, a gate insulating film 4 is then formed over the semiconductor layer 3 and the under-coat layer 2. The gate insulating film 4 may comprise any available insulating film including but not limited to silicon oxide and silicon nitride. The gate insulating film 4 may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method and a sputtering method. The thickness of the gate insulating film 4 may advantageously be decided by taking into account a driving condition of the device and a driving voltage. A typical example of the thickness of the gate insulating film 4 may be in the range of 30-200 nm, and preferably 50-100 nm. Further, a conductive film is deposited over the gate insulating film 4. The conductive film may comprise any available conductive film, for example, a silicide film, a metal film, and an impurity-doped silicon film. The deposition may typically be made by a plasma enhanced chemical vapor deposition method. A typical example of the thickness of the conductive film may be in the range of 200-400 nm. A resist pattern is selectively formed over the conductive film by the known lithography technique. An anisotropic etching process is then carried out by use of the resist pattern as a mask

to define the conductive film into a gate electrode 5. Since the resist pattern overlaps predetermined inside regions of the high impurity concentration regions 3a of the semiconductor layer 3, then the gate electrode 5 also overlaps predetermined inside regions of the high impurity concentration regions 3a of the semiconductor layer 3. In this typical example, the above overlap appears symmetrically both the source and drain sides, but it should be noted that the above overlap is needed at least in the drain side. Namely, it is possible that the above overlap appears only in the drain side, or also possible that the above overlap appears asymmetrically both in the source and drain sides. It should also be noted that if the transistor is for the switching transistor utilizing the inversion between the source and drain regions, then the above overlap should appear symmetrically in both the source and drain sides.

**[0093]** As shown in FIG. 9G, a selective laser irradiation process is then carried out by use of the gate electrode 5 as a mask, so that a laser beam 12 is irradiated through the gate insulating film 4 to the semiconductor layer 3, except under the gate electrode 5 for the purpose of selective activation of the semiconductor layer 3, except under the gate electrode 5. The non-overlapped regions of the semiconductor layer 3 do receive the laser beam irradiation, whereby the non-overlapped regions become sufficiently activated high impurity concentration layers 3c. The impurity in the non-overlapped regions or the sufficiently activated high impurity concentration layers 3c is sufficiently activated and the most of the impurity becomes effectively activated impurity which contributes to the electrical conductivity. On the other hand, the gate-overlapped regions of the semiconductor layer 3 do not receive the laser beam irradiation but do receive a thermal diffusion from the non-overlapped regions, whereby the gate-overlapped regions become lightly activated high impurity concentration layers 3b. The impurity in the gate-overlapped regions or the lightly activated high impurity concentration layers 3b is insufficiently activated and the minority of the impurity becomes effectively activated impurity which contributes to the electrical conductivity. Namely, the lightly activated high impurity concentration layers 3b has a lower concentration of the effectively activated impurity, which contributes to the electrical conductivity, than the concentration of the implanted-impurity. Namely, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c have the same impurity concentration. The impurity implanted in the sufficiently activated high impurity concentration layers 3c are sufficiently activated by direct laser beam irradiation in the laser anneal process. The impurity implanted in the lightly activated high impurity concentration layers 3b are lightly or insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layers 3c. The lightly activated high impurity concentration layers 3b have not received any laser irradiation. Namely, the

activation energy for the lightly activated high impurity concentration layers 3b depends on the thermal diffusion from the sufficiently activated high impurity concentration layers 3c, for which reason the activation is insufficient. This insufficient activation depending on the thermal diffusion gives rise to a lower concentration of the effectively activated impurity than the implanted-impurity concentration. The effectively activated impurity only may contribute to provide an electrical conductivity. For those reasons, the lightly activated high impurity concentration layers 3b exhibits substantially the same function as the lightly doped drain regions. Further, the thermal diffusion into the lightly activated high impurity concentration layers 3b is directed inwardly from the sufficiently activated high impurity concentration layers 3c which have received the laser irradiation in the laser anneal process. For this reason, the heat energy absorbed into the lightly activated high impurity concentration layers 3b may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Therefore, the degree of the activation of the impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Namely, the concentration profile of the effectively activated impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Accordingly, the concentration profile of the effectively activated impurity across the channel region free of impurity implantation, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c are free of any step-like variation or any other abrupt and rapid variation, whereby no extensively high field concentration is caused. The energy of the laser irradiation may be decided by taking into account respective thicknesses of the semiconductor layer 3 and the gate insulating film 4 as well as respective surface reflectivities thereof, and also with reference to an energy which causes semiconductor or silicon of the semiconductor layer 3 to be melt. A typical example of the laser irradiation energy may be in the range of 250-300 mJ, but not limited thereto.

**[0094]** As shown in FIG. 9H, an inter-layer insulator 6 is deposited over the gate electrode 5 and the gate insulating film 4. Contact holes 8 are selectively formed in the inter-layer insulator 6 and the gate insulating film 4 and over the sufficiently activated high impurity concentration layers 3c serving as source and drain regions.

**[0095]** As shown in FIG. 9I, a metal film is also deposited over the inter-layer insulator 6 and within the contact holes 8, so that the metal film is made into contact with

the sufficiently activated high impurity concentration layers 3c. The deposition may be made by any available method, for example, a sputtering method. A typical example of the thickness of the metal film may be in the range of 300-1000 nm, but not limited thereto. A typical example of material for the metal film may be aluminum, but not limited thereto. The metal film is then patterned into source and drain electrodes 7 by use of a known lithography technique and a subsequent anisotropic etching process, thereby forming the thin film field effect transistor including the improved gate-overlap-drain structure.

#### FOURTH EMBODIMENT :

**[0096]** A fourth embodiment according to the present invention will be described in detail with reference to the drawings. This fourth embodiment is different from the first embodiment but only parts of the processes for forming the transistor, for which reason the following descriptions will focus on the sequential processes. FIGS. 10A through 10I are fragmentary cross sectional elevation views of thin film field effect transistors with the improved gate-overlap-drain structure in sequential steps involved in a novel method of forming the transistor in accordance with the fourth embodiment of the present invention. As shown in FIG. 10A, a transparent insulating substrate 1 such as a glass substrate 1 is prepared. An under-coat layer 2 is formed over the transparent insulating substrate 1. The under-coat layer 2 may typically have a thickness in the range of 100-500 nm and more preferably about 300 nm. The under-coat layer 2 is provided in order to prevent any further impurity diffusion from the substrate 1 to any overlying layers, for example, a semiconductor layer 3. The under-coat layer 2 is not necessarily needed if the above impurity diffusion is not problem. The under-coat layer 2 may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method, a sputtering method and a dipping method. The under-coat layer 2 may typically comprise, but not limited to, any one of a silicon oxide layer, a silicon nitride layer, and laminations thereof.

**[0097]** As shown in FIG. 10B, a polycrystal silicon layer 3 is formed over the under-coat layer 2. A typical example of forming the polycrystal silicon layer 3 is that an amorphous silicon layer as a precursor is first formed over the under-coat layer 2, before the amorphous silicon layer is then crystallized by a laser irradiation. The amorphous silicon layer may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method and a sputtering method. A typical thickness of the amorphous silicon layer may be in the range of 50-100 nm. Instead of the laser irradiation for crystallization, a solid-state growth method may also be available.

**[0098]** As shown in FIG. 10C, a resist pattern is selectively formed over the polycrystal silicon layer 3 by use of the known lithography technique. The polycrystal silicon layer 3 is then patterned into an island shape by an anisotropic etching technique using the resist pattern as a mask. The used resist pattern is then removed. In the above-described first embodiment, the polycrystal silicon layer 3 is directly subjected to the impurity implantation. This direct exposure to the impurity implantation may allow the polycrystal silicon layer 3 to be damaged in crystal structure. In order to avoid the polycrystal silicon layer 3 from the possibility of damage in the crystal structure, the following addition process is carried out.

**[0099]** As shown in FIG. 10D, a dummy oxide film 15 is additionally formed over the polycrystal silicon layer 3 and the under-coat layer 2. The dummy oxide film 15 is then selectively removed, so that the dummy oxide film 15 extends only over the polycrystal silicon layer 3. Subsequently, another resist pattern 10 is also selectively formed over the dummy oxide film 15. A selective impurity-implantation process is carried out by use of the resist pattern 10 as a mask, so that impurity ions 11 are selectively implanted through the dummy oxide film 15 into the patterned polycrystal silicon layer 3 except under the resist pattern 10, thereby to form high impurity concentration regions 3a in the patterned polycrystal silicon layer 3, except under the resist pattern 10. The impurity may, for example, be phosphorous but not limited thereto. A size of the resist pattern 10 is smaller than an intended gate electrode formation region by a size of lightly activated high impurity concentration layers.

**[0100]** As shown in FIG. 10E, the used resist pattern 10 is then removed, while the used dummy oxide film 15 remains over the semiconductor layer 3.

**[0101]** As shown in FIG. 10F, a gate insulating film 4 is then formed over the dummy oxide film 15 and the under-coat layer 2. The gate insulating film 4 may comprise any available insulating film including but not limited to silicon oxide and silicon nitride. The gate insulating film 4 may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method and a sputtering method. The thickness of the gate insulating film 4 may advantageously be decided by taking into account a driving condition of the device and a driving voltage. A typical example of the thickness of the gate insulating film 4 may be in the range of 30-200 nm, and preferably 50-100 nm. Further, a conductive film is deposited over the gate insulating film 4. The conductive film may comprise any available conductive film, for example, a silicide film, a metal film, and an impurity-doped silicon film. The deposition may typically be made by a plasma enhanced chemical vapor deposition method. A typical example of the thickness of the conductive film may be in the range of 200-400 nm. A resist pattern is selectively formed over the conductive film by the known lithography technique. An ani-

sotropic etching process is then carried out by use of the resist pattern as a mask to define the conductive film into a gate electrode 5. Since the resist pattern overlaps predetermined inside regions of the high impurity concentration regions 3a of the semiconductor layer 3, then the gate electrode 5 also overlaps predetermined inside regions of the high impurity concentration regions 3a of the semiconductor layer 3. In this typical example, the above overlap appears symmetrically both the source and drain sides, but it should be noted that the above overlap is needed at least in the drain side. Namely, it is possible that the above overlap appears only in the drain side, or also possible that the above overlap appears asymmetrically both in the source and drain sides. It should also be noted that if the transistor is for the switching transistor utilizing the inversion between the source and drain regions, then the above overlap should appear symmetrically in both the source and drain sides.

**[0102]** As shown in FIG. 10G, a selective laser irradiation process is then carried out by use of the gate electrode 5 as a mask, so that a laser beam 12 is irradiated through the gate insulating film 4 and the dummy oxide film 15 to the semiconductor layer 3, except under the gate electrode 5 for the purpose of selective activation of the semiconductor layer 3, except under the gate electrode 5. The non-overlapped regions of the semiconductor layer 3 do receive the laser beam irradiation, whereby the non-overlapped regions become sufficiently activated high impurity concentration layers 3c. The impurity in the non-overlapped regions or the sufficiently activated high impurity concentration layers 3c is sufficiently activated and the most of the impurity becomes effectively activated impurity which contributes to the electrical conductivity. On the other hand, the gate-overlapped regions of the semiconductor layer 3 do not receive the laser beam irradiation but do receive a thermal diffusion from the non-overlapped regions, whereby the gate-overlapped regions become lightly activated high impurity concentration layers 3b. The impurity in the gate-overlapped regions or the lightly activated high impurity concentration layers 3b is insufficiently activated and the minority of the impurity becomes effectively activated impurity which contributes to the electrical conductivity. Namely, the lightly activated high impurity concentration layers 3b has a lower concentration of the effectively activated impurity, which contributes to the electrical conductivity, than the concentration of the implanted-impurity. Namely, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c have the same impurity concentration. The impurity implanted in the sufficiently activated high impurity concentration layers 3c are sufficiently activated by direct laser beam irradiation in the laser anneal process. The impurity implanted in the lightly activated high impurity concentration layers 3b are lightly or insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layers 3c. The lightly activated high

impurity concentration layers 3b have not received any laser irradiation. Namely, the activation energy for the lightly activated high impurity concentration layers 3b depends on the thermal diffusion from the sufficiently activated high impurity concentration layers 3c, for which reason the activation is insufficient. This insufficient activation depending on the thermal diffusion gives rise to a lower concentration of the effectively activated impurity than the implanted-impurity concentration. The effectively activated impurity only may contribute to provide an electrical conductivity. For those reasons, the lightly activated high impurity concentration layers 3b exhibits substantially the same function as the lightly doped drain regions. Further, the thermal diffusion into the lightly activated high impurity concentration layers 3b is directed inwardly from the sufficiently activated high impurity concentration layers 3c which have received the laser irradiation in the laser anneal process. For this reason, the heat energy absorbed into the lightly activated high impurity concentration layers 3b may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Therefore, the degree of the activation of the impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Namely, the concentration profile of the effectively activated impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Accordingly, the concentration profile of the effectively activated impurity across the channel region free of impurity implantation, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c are free of any step-like variation or any other abrupt and rapid variation, whereby no extensively high field concentration is caused. The energy of the laser irradiation may be decided by taking into account respective thicknesses of the semiconductor layer 3 and the gate insulating film 4 as well as respective surface reflectivities thereof, and also with reference to an energy which causes semiconductor or silicon of the semiconductor layer 3 to be melt. A typical example of the laser irradiation energy may be in the range of 250-300 mJ, but not limited thereto.

**[0103]** As shown in FIG. 10H, an inter-layer insulator 6 is deposited over the gate electrode 5 and the gate insulating film 4. Contact holes 8 are selectively formed in the inter-layer insulator 6, the gate insulating film 4 and the dummy oxide film 15 but over the sufficiently activated high impurity concentration layers 3c serving as source and drain regions.

**[0104]** As shown in FIG. 10I, a metal film is also de-

posited over the inter-layer insulator 6 and within the contact holes 8, so that the metal film is made into contact with the sufficiently activated high impurity concentration layers 3c. The deposition may be made by any available method, for example, a sputtering method. A typical example of the thickness of the metal film may be in the range of 300-1000 nm, but not limited thereto. A typical example of material for the metal film may be aluminum, but not limited thereto. The metal film is then patterned into source and drain electrodes 7 by use of a known lithography technique and a subsequent anisotropic etching process, thereby forming the thin film field effect transistor including the improved gate-overlap-drain structure.

#### FIFTH EMBODIMENT:

**[0105]** A fifth embodiment according to the present invention will be described in detail with reference to the drawings. This fifth embodiment is different from the first embodiment but only parts of the processes for forming the transistor, for which reason the following descriptions will focus on the sequential processes. FIGS. 11A through 11I are fragmentary cross sectional elevation views of thin film field effect transistors with the improved gate-overlap-drain structure in sequential steps involved in a novel method of forming the transistor in accordance with the fifth embodiment of the present invention. As shown in FIG. 11A, a transparent insulating substrate 1 such as a glass substrate 1 is prepared. An under-coat layer 2 is formed over the transparent insulating substrate 1. The under-coat layer 2 may typically have a thickness in the range of 100-500 nm and more preferably about 300 nm. The under-coat layer 2 is provided in order to prevent any further impurity diffusion from the substrate 1 to any overlying layers, for example, a semiconductor layer 3. The under-coat layer 2 is not necessarily needed if the above impurity diffusion is not problem. The under-coat layer 2 may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method, a sputtering method and a dipping method. The under-coat layer 2 may typically comprise, but not limited to, any one of a silicon oxide layer, a silicon nitride layer, and laminations thereof.

**[0106]** As shown in FIG. 11B, a polycrystal silicon layer 3 is formed over the under-coat layer 2. A typical example of forming the polycrystal silicon layer 3 is that an amorphous silicon layer as a precursor is first formed over the under-coat layer 2, before the amorphous silicon layer is then crystallized by a laser irradiation. The amorphous silicon layer may be formed by one of any available methods such as a low pressure chemical vapor deposition method, a plasma enhanced chemical vapor deposition method and a sputtering method. A typical thickness of the amorphous silicon layer may be in the range of 50-100 nm. Instead of the laser irradiation

for crystallization, a solid-state growth method may also be available.

**[0107]** As shown in FIG. 11C, a resist pattern is selectively formed over the polycrystal silicon layer 3 by use of the known lithography technique. The polycrystal silicon layer 3 is then patterned into an island shape by an anisotropic etching technique using the resist pattern as a mask. The used resist pattern is then removed. In the above-described first embodiment, the polycrystal silicon layer 3 is directly subjected to the impurity implantation. This direct exposure to the impurity implantation may allow the polycrystal silicon layer 3 to be damaged in crystal structure. In order to avoid the polycrystal silicon layer 3 from the possibility of damage in the crystal structure, an additional dummy oxide film is formed which may act as a gate oxide film.

**[0108]** As shown in FIG. 11D, a dummy oxide film 15 is additionally formed over the polycrystal silicon layer 3 and the under-coat layer 2. Subsequently, another resist pattern 10 is also selectively formed over the dummy oxide film 15. A selective impurity-implantation process is carried out by use of the resist pattern 10 as a mask, so that impurity ions 11 are selectively implanted through the dummy oxide film 15 into the patterned polycrystal silicon layer 3 except under the resist pattern 10, thereby to form high impurity concentration regions 3a in the patterned polycrystal silicon layer 3, except under the resist pattern 10. The impurity may, for example, be phosphorous but not limited thereto. A size of the resist pattern 10 is smaller than an intended gate electrode formation region by a size of lightly activated high impurity concentration layers.

**[0109]** As shown in FIG. 11E, the used resist pattern 10 is then removed, while the used dummy oxide film 15 remains over the semiconductor layer 3 because the used dummy oxide film 15 will act as a gate insulating film, for which reason the dummy oxide film 15 will hereinafter referred to as a gate insulating film 15.

**[0110]** As shown in FIG. 11F, a conductive film is deposited over the gate insulating film 15. The conductive film may comprise any available conductive film, for example, a silicide film, a metal film, and an impurity-doped silicon film. The deposition may typically be made by a plasma enhanced chemical vapor deposition method. A typical example of the thickness of the conductive film may be in the range of 200-400 nm. A resist pattern is selectively formed over the conductive film by the known lithography technique. An anisotropic etching process is then carried out by use of the resist pattern as a mask to define the conductive film into a gate electrode 5. Since the resist pattern overlaps predetermined inside regions of the high impurity concentration regions 3a of the semiconductor layer 3, then the gate electrode 5 also overlaps predetermined inside regions of the high impurity concentration regions 3a of the semiconductor layer 3. In this typical example, the above overlap appears symmetrically both the source and drain sides, but it should be noted that the above overlap is needed at

least in the drain side. Namely, it is possible that the above overlap appears only in the drain side, or also possible that the above overlap appears asymmetrically both in the source and drain sides. It should also be noted that if the transistor is for the switching transistor utilizing the inversion between the source and drain regions, then the above overlap should appear symmetrically in both the source and drain sides.

**[0111]** As shown in FIG. 11G, a selective laser irradiation process is then carried out by use of the gate electrode 5 as a mask, so that a laser beam 12 is irradiated through the gate insulating film 15 and the dummy oxide film 15 to the semiconductor layer 3, except under the gate electrode 5 for the purpose of selective activation of the semiconductor layer 3, except under the gate electrode 5. The non-overlapped regions of the semiconductor layer 3 do receive the laser beam irradiation, whereby the non-overlapped regions become sufficiently activated high impurity concentration layers 3c. The impurity in the non-overlapped regions or the sufficiently activated high impurity concentration layers 3c is sufficiently activated and the most of the impurity becomes effectively activated impurity which contributes to the electrical conductivity. On the other hand, the gate-overlapped regions of the semiconductor layer 3 do not receive the laser beam irradiation but do receive a thermal diffusion from the non-overlapped regions, whereby the gate-overlapped regions become lightly activated high impurity concentration layers 3b. The impurity in the gate-overlapped regions or the lightly activated high impurity concentration layers 3b is insufficiently activated and the minority of the impurity becomes effectively activated impurity which contributes to the electrical conductivity. Namely, the lightly activated high impurity concentration layers 3b has a lower concentration of the effectively activated impurity, which contributes to the electrical conductivity, than the concentration of the implanted-impurity. Namely, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c have the same impurity concentration. The impurity implanted in the sufficiently activated high impurity concentration layers 3c are sufficiently activated by direct laser beam irradiation in the laser anneal process. The impurity implanted in the lightly activated high impurity concentration layers 3b are lightly or insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layers 3c. The lightly activated high impurity concentration layers 3b have not received any laser irradiation. Namely, the activation energy for the lightly activated high impurity concentration layers 3b depends on the thermal diffusion from the sufficiently activated high impurity concentration layers 3c, for which reason the activation is insufficient. This insufficient activation depending on the thermal diffusion gives rise to a lower concentration of the effectively activated impurity than the implanted-impurity concentration. The effectively activated impurity only may contribute to pro-

vide an electrical conductivity. For those reasons, the lightly activated high impurity concentration layers 3b exhibits substantially the same function as the lightly doped drain regions. Further, the thermal diffusion into the lightly activated high impurity concentration layers 3b is directed inwardly from the sufficiently activated high impurity concentration layers 3c which have received the laser irradiation in the laser anneal process. For this reason, the heat energy absorbed into the lightly activated high impurity concentration layers 3b may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Therefore, the degree of the activation of the impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Namely, the concentration profile of the effectively activated impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Accordingly, the concentration profile of the effectively activated impurity across the channel region free of impurity implantation, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c are free of any step-like variation or any other abrupt and rapid variation, whereby no extensively high field concentration is caused. The energy of the laser irradiation may be decided by taking into account respective thicknesses of the semiconductor layer 3 and the gate insulating film 15 as well as respective surface reflectivities thereof, and also with reference to an energy which causes semiconductor or silicon of the semiconductor layer 3 to be melt. A typical example of the laser irradiation energy may be in the range of 250-300 mJ, but not limited thereto.

**[0112]** As shown in FIG. 11H, an inter-layer insulator 6 is deposited over the gate electrode 5 and the gate insulating film 15. Contact holes 8 are selectively formed in the inter-layer insulator 6 and the gate insulating film 15 but over the sufficiently activated high impurity concentration layers 3c serving as source and drain regions.

**[0113]** As shown in FIG. 11I, a metal film is also deposited over the inter-layer insulator 6 and within the contact holes 8, so that the metal film is made into contact with the sufficiently activated high impurity concentration layers 3c. The deposition may be made by any available method, for example, a sputtering method. A typical example of the thickness of the metal film may be in the range of 300-1000 nm, but not limited thereto. A typical example of material for the metal film may be aluminum, but not limited thereto. The metal film is then patterned into source and drain electrodes 7 by use of

a known lithography technique and a subsequent anisotropic etching process, thereby forming the thin film field effect transistor including the improved gate-overlap-drain structure. In accordance with the present embodiment, since the dummy oxide film 15 used in the impurity-implantation process is further re-used as the gate insulating film 15, for which reason no process for forming the gate insulating film is needed.

#### SIXTH EMBODIMENT:

**[0114]** A sixth embodiment according to the present invention will be described in detail with reference to the drawings. FIG. 12 is a fragmentary cross sectional elevation view of a novel thin film field effect transistor with an improved gate-overlap-drain structure in accordance with the sixth embodiment of the present invention. In the first, third, fourth and fifth embodiments, the planer-structured thin film field effect transistors have been provided. In this sixth embodiment, however, a staggered thin film field effect transistor is provided, wherein source and drain electrodes underlie the source and drain regions, above which a gate electrode is positioned.

**[0115]** A staggered thin film field effect transistor is provided over a glass substrate 1. An under-coat layer 2 overlies the glass substrate 1. Source/drain electrodes 20 are selectively provided over the under-coat layer 2. A semiconductor layer 3 is selectively provided over the source/drain electrodes 20 and also over the under-coat layer 2 but between the source/drain electrodes 20 and in the vicinity of the outside edges of the source/drain electrodes 20. The semiconductor layer further comprises an amorphous silicon channel layer 21, lightly activated high impurity concentration layers 3b in contact directly with opposite sides of the amorphous silicon channel layer 21, and sufficiently activated high impurity concentration layers 3c in contact directly with outsides of the lightly activated high impurity concentration layers 3b. A gate insulating film 4 extends over the semiconductor layer 3 and the under-coat layer 2.

**[0116]** A gate electrode 5 is selectively provided over the gate insulating film 4. The lightly activated high impurity concentration layers 3b are positioned under the gate electrode 5, so that the lightly activated high impurity concentration layers 3b are covered by the gate electrode 5. The sufficiently activated high impurity concentration layers 3c are positioned under outsides of the gate electrode 5, so that the sufficiently activated high impurity concentration layers 3c are not covered by the gate electrode 5. Respective boundaries between the sufficiently activated high impurity concentration layers 3c and the lightly activated high impurity concentration layers 3b are self-aligned to the opposite side-edges of the gate electrode 5.

**[0117]** An inter-layer insulator 6 extends over the gate electrode 5 and the gate insulating film 4. Contact holes are provided in laminations of the sufficiently activated

high impurity concentration layers 3c, the gate insulating film 4 and the inter-layer insulator 6 but over the source/drain electrodes 20. Source/drain electrodes 7 are selectively provided in the contact holes and over the inter-layer insulator 6, so that the source/drain electrodes 7 are in contact with the source/drain electrodes 20. The sufficiently activated high impurity concentration layers 3c serve as source/drain regions.

**[0118]** The lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c have the same impurity concentration. The impurity implanted in the sufficiently activated high impurity concentration layers 3c are sufficiently activated by direct laser beam irradiation in the laser anneal process. The impurity implanted in the lightly activated high impurity concentration layers 3b are lightly or insufficiently activated by a thermal diffusion from the sufficiently activated high impurity concentration layers 3c. The lightly activated high impurity concentration layers 3b have not received any laser irradiation. Namely, the activation energy for the lightly activated high impurity concentration layers 3b depends on the thermal diffusion from the sufficiently activated high impurity concentration layers 3c, for which reason the activation is insufficient. This insufficient activation depending on the thermal diffusion gives rise to a lower concentration of the effectively activated impurity than the implanted-impurity concentration. The effectively activated impurity only may contribute to provide an electrical conductivity. For those reasons, the lightly activated high impurity concentration layers 3b exhibits substantially the same function as the lightly doped drain regions.

**[0119]** Further, the thermal diffusion into the lightly activated high impurity concentration layers 3b is directed inwardly from the sufficiently activated high impurity concentration layers 3c which have received the laser irradiation in the laser anneal process. For this reason, the heat energy absorbed into the lightly activated high impurity concentration layers 3b may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Therefore, the degree of the activation of the impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Namely, the concentration profile of the effectively activated impurity may gently or gradually decrease from the outside position near the sufficiently activated high impurity concentration layers 3c to the inside position far from the sufficiently activated high impurity concentration layers 3c. Accordingly, the concentration profile of the effectively activated impurity across the channel region 3a, the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c are free of any step-like variation or any other abrupt

and rapid variation, whereby no extensively high field concentration is caused. This concentration profile of the effectively activated impurity prevents traps of the hot carriers and thus allow a long carrier life-time.

[0120] Similarly to the foregoing embodiments, the above improved gate-overlap-drain structure may also be formed by a single pair of a single impurity implantation process and a later single laser anneal process for selective activation. The impurity implantation process is carried out by using a resist pattern having a smaller size than the gate electrode 5 as a mask to form high impurity concentration regions which include both the lightly activated high impurity concentration layers 3b and the sufficiently activated high impurity concentration layers 3c. After the gate electrode 5 is formed, then the single laser anneal process is carried out by using the gate electrode as a mask for selective activation of the high impurity concentration regions, whereby the laser-irradiated regions non-overlapped and non-covered by the gate electrode 5 are sufficiently activated and become the sufficiently activated high impurity concentration layers 3c, while the laser-irradiation-free regions overlapped and covered by the gate electrode 5 are insufficiently activated by the thermal diffusion from the laser-irradiated regions and become the lightly activated high impurity concentration layers 3b.

[0121] In the foregoing embodiments, the entirety of the substrate is subjected to the laser anneal. It is, of course, possible to irradiate the laser beam onto one or more selected or localized regions. It is also possible to utilize laser anneal processes under various conditions for causing a variety of the activation degree.

[0122] Although the invention has been described above in connection with several preferred embodiments therefor, it will be appreciated that those embodiments have been provided solely for illustrating the invention, and not in a limiting sense. Numerous modifications and substitutions of equivalent materials and techniques will be readily apparent to those skilled in the art after reading the present application, and all such modifications and substitutions are expressly understood to fall within the true scope and spirit of the appended claims.

## Claims

1. A semiconductor structure in a field effect transistor, said structure comprising:

a semiconductor layer;  
 an insulating layer overlying said semiconductor layer ; and  
 a gate electrode for controlling an electric field applied to at least a part of said semiconductor layer ;

**characterized in that** said semiconductor

layer further includes :

at least a lightly activated high impurity concentration layer having a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than said first implanted-impurity concentration value; and

at least a sufficiently activated high impurity concentration layer being bounded with said at least a lightly activated high impurity concentration layer, and said at least a sufficiently activated high impurity concentration layer having a second implanted-impurity concentration value which is substantially the same as said first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than said first effectively-activated-impurity concentration range.

2. The semiconductor structure as claimed in claim 1, **characterized in that** said at least a lightly activated high impurity concentration layer is positioned under said gate electrode.
3. The semiconductor structure as claimed in claim 2, **characterized in that** a boundary between said at least a lightly activated high impurity concentration layer and said at least a sufficiently activated high impurity concentration layer is aligned to an edge of said gate electrode.
4. The semiconductor structure as claimed in claim 3, **characterized in that** said at least a lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in said first effectively-activated-impurity concentration range as a distance from said at least a sufficiently activated high impurity concentration layer is increased.
5. The semiconductor structure as claimed in claim 4, **characterized in that** said at least a sufficiently activated high impurity concentration layer is sufficiently activated by a laser beam irradiation, while said at least a lightly activated high impurity concentration layer is insufficiently activated by a thermal diffusion from said at least a sufficiently activated high impurity concentration layer.
6. The semiconductor structure as claimed in claim 1, **characterized in that** said at least a sufficiently activated high impurity concentration layer serves as a drain region, while said at least a lightly activated high impurity concentration layer serves as a field concentration relaxation region.

7. The semiconductor structure as claimed in claim 1, **characterized in that** said semiconductor layer comprises :

a channel region;  
 said lightly activated high impurity concentration layers adjacent to opposite sides of said channel region ; and  
 said sufficiently activated high impurity concentration layers adjacent to opposite outsides of said lightly activated high impurity concentration layers, and said sufficiently activated high impurity concentration layers serve as source and drain regions, and respective boundaries between said lightly activated high impurity concentration layers and said sufficiently activated high impurity concentration layers are aligned to opposite side edges of said gate electrode.

8. A semiconductor structure in a field effect transistor, said structure comprising:

a semiconductor layer;  
 an insulating layer overlying said semiconductor layer; and  
 a gate electrode for controlling an electric field applied to at least a part of said semiconductor layer ;

**characterized in that** said semiconductor layer further includes :

at least a sufficiently activated high impurity concentration layer being sufficiently activated by a laser beam irradiation, and  
 at least a lightly activated high impurity concentration layer being bounded with said at least a sufficiently activated high impurity concentration layer, and said at least a lightly activated high impurity concentration layer being insufficiently activated by a thermal diffusion from said at least a sufficiently activated high impurity concentration layer.

9. The semiconductor structure as claimed in claim 8, **characterized in that** said at least a lightly activated high impurity concentration layer is positioned under said gate electrode.

10. The semiconductor structure as claimed in claim 9, **characterized in that** a boundary between said at least a lightly activated high impurity concentration layer and said at least a sufficiently activated high impurity concentration layer is aligned to an edge of said gate electrode.

11. The semiconductor structure as claimed in claim

10, **characterized in that** said at least a lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value as a distance from said at least a sufficiently activated high impurity concentration layer is increased.

12. The semiconductor structure as claimed in claim 11, **characterized in that** said at least a lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than said first implanted-impurity concentration value ; and

**characterized in that** said at least a sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as said first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than said first effectively-activated-impurity concentration range.

13. The semiconductor structure as claimed in claim 8, **characterized in that** said at least a sufficiently activated high impurity concentration layer serves as a drain region, while said at least a lightly activated high impurity concentration layer serves as a field concentration relaxation region.

14. The semiconductor structure as claimed in claim 8, **characterized in that** said semiconductor layer comprises :

a channel region;  
 said lightly activated high impurity concentration layers adjacent to opposite sides of said channel region ; and  
 said sufficiently activated high impurity concentration layers adjacent to opposite outsides of said lightly activated high impurity concentration layers, and said sufficiently activated high impurity concentration layers serve as source and drain regions, and respective boundaries between said lightly activated high impurity concentration layers and said sufficiently activated high impurity concentration layers are aligned to opposite side edges of said gate electrode.

15. A field effect transistor including :

a substrate;  
 a gate insulating film over said substrate ;  
 a gate electrode over said gate insulating film; and  
 source/drain regions over and substrate and under said gate insulating film,

**characterized in that** said drain region further includes :

at least a lightly activated high impurity concentration layer having a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than said first implanted-impurity concentration value ; and  
 at least a sufficiently activated high impurity concentration layer being bounded with said at least a lightly activated high impurity concentration layer, and said at least a sufficiently activated high impurity concentration layer having a second implanted-impurity concentration value which is substantially the same as said first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than said first effectively-activated-impurity concentration range.

16. The field effect transistor as claimed in claim 15, **characterized in that** said at least a lightly activated high impurity concentration layer is positioned under said gate electrode.
17. The field effect transistor as claimed in claim 16, **characterized in that** a boundary between said at least a lightly activated high impurity concentration layer and said at least a sufficiently activated high impurity concentration layer is aligned to an edge of said gate electrode.
18. The field effect transistor as claimed in claim 17, **characterized in that** said at least a lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in said first effectively-activated-impurity concentration range as a distance from said at least a sufficiently activated high impurity concentration layer is increased.
19. The field effect transistor as claimed in claim 18, **characterized in that** said at least a sufficiently activated high impurity concentration layer is sufficiently activated by a laser beam irradiation, while said at least a lightly activated high impurity concentration layer is insufficiently activated by a thermal diffusion from said at least a sufficiently activated high impurity concentration layer.
20. The field effect transistor as claimed in claim 15, **characterized in that** said source region has the same structure as said drain region.
21. A field effect transistor including :

a substrate;  
 a gate insulating film over said substrate;  
 a gate electrode over said gate insulating film ;  
 and  
 source/drain regions over and substrate and under said gate insulating film,

**characterized in that** said drain region further includes :

at least a sufficiently activated high impurity concentration layer being sufficiently activated by a laser beam irradiation, and  
 at least a lightly activated high impurity concentration layer being bounded with said at least a sufficiently activated high impurity concentration layer, and said at least a lightly activated high impurity concentration layer being insufficiently activated by a thermal diffusion from said at least a sufficiently activated high impurity concentration layer.

22. The field effect transistor as claimed in claim 21, **characterized in that** said at least a lightly activated high impurity concentration layer is positioned under said gate electrode.
23. The field effect transistor as claimed in claim 22, **characterized in that** a boundary between said at least a lightly activated high impurity concentration layer and said at least a sufficiently activated high impurity concentration layer is aligned to an edge of said gate electrode.
24. The field effect transistor as claimed in claim 23, **characterized in that** said at least a lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value as a distance from said at least a sufficiently activated high impurity concentration layer is increased.
25. The field effect transistor as claimed in claim 24, **characterized in that** said at least a lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than said first implanted-impurity concentration value ; and  
**characterized in that** said at least a sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as said first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than said first effectively-activated-impurity concentration range.

26. The field effect transistor as claimed in claim 21, **characterized in that** said source region has the same structure as said drain region.

27. A field effect transistor including :

a substrate;  
a gate insulating film over said substrate ;  
a gate electrode over said gate insulating film;  
and  
source/drain regions over and substrate and under said gate insulating film,

**characterized in that** each of said source/drain regions further includes:

at least a lightly activated high impurity concentration layer being positioned under said gate electrode, and said at least a lightly activated high impurity concentration layer having a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than said first implanted-impurity concentration value; and  
at least a sufficiently activated high impurity concentration layer being bounded with said at least a lightly activated high impurity concentration layer, and a boundary between said at least a lightly activated high impurity concentration layer and said at least a sufficiently activated high impurity concentration layer being aligned to an edge of said gate electrode, and said at least a sufficiently activated high impurity concentration layer having a second implanted-impurity concentration value which is substantially the same as said first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than said first effectively-activated-impurity concentration range, and

**characterized in that** said at least a lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in said first effectively-activated-impurity concentration range as a distance from said at least a sufficiently activated high impurity concentration layer is increased.

28. The field effect transistor as claimed in claim 27, **characterized in that** said at least a sufficiently activated high impurity concentration layer is sufficiently activated by a laser beam irradiation, while said at least a lightly activated high impurity concentration layer is insufficiently activated by a thermal diffusion from said at least a sufficiently activated high impurity concentration layer.

29. The field effect transistor as claimed in claim 27, **characterized in that** said field effect transistor is a thin film field effect transistor.

5 30. A liquid crystal display including a plurality of pixels, each pixel having a liquid crystal cell and a switching device, and said switching device further comprising : a thin film field effect transistor including :

a substrate;  
a gate insulating film over said substrate;  
a gate electrode over said gate insulating film;  
and  
source/drain regions over and substrate and under said gate insulating film,

**characterized in that** each of said source/drain regions further includes:

at least a lightly activated high impurity concentration layer being positioned under said gate electrode, and said at least a lightly activated high impurity concentration layer having a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than said first implanted-impurity concentration value; and  
at least a sufficiently activated high impurity concentration layer being bounded with said at least a lightly activated high impurity concentration layer, and a boundary between said at least a lightly activated high impurity concentration layer and said at least a sufficiently activated high impurity concentration layer being aligned to an edge of said gate electrode, and said at least a sufficiently activated high impurity concentration layer having a second implanted-impurity concentration value which is substantially the same as said first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than said first effectively-activated-impurity concentration range, and

**characterized in that** said at least a lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in said first effectively-activated-impurity concentration range as a distance from said at least a sufficiently activated high impurity concentration layer is increased.

31. A method of forming a semiconductor structure in a field effect transistor, comprising the steps of:

selectively forming a resist pattern over a first selected region of a semiconductor layer;

carrying out a selective impurity-implantation by use of said resist pattern as a mask for selectively implanting an impurity into said semiconductor layer except under said resist pattern at a first implanted-impurity concentration, to define at least an impurity-implanted region in said semiconductor layer;  
 removing said resist pattern from said semiconductor layer ;  
 selectively forming a gate electrode over a second selected region of said semiconductor layer, and said second selected region completely encompassing said first selected region and also encompassing an outside region adjacent to a periphery of said first selected region, and at least a gate-overlapped part of said at least an impurity-implanted region being covered by said gate electrode, while a remaining non-overlapped part of said at least an impurity-implanted region being not covered by said gate electrode; and  
 carrying out a selective laser beam irradiation to said remaining non-overlapped part by use of said gate electrode as a mask, whereby said remaining non-overlapped part is sufficiently activated upon said selective laser beam irradiation and said remaining non-overlapped part becomes at least a sufficiently activated high impurity concentration layer, while said at least a gate-overlapped part is insufficiently activated by a thermal diffusion from said remaining non-overlapped part, and said at least a gate-overlapped part becomes at least a lightly activated high impurity concentration layer.

32. The method as claimed in claim 31, **characterized in that** said at least a lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than said first implanted-impurity concentration value ; and

said at least a sufficiently activated high impurity concentration layer is bounded with said at least a lightly activated high impurity concentration layer, and said at least a sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as said first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than said first effectively-activated-impurity concentration range.

33. The method as claimed in claim 32, **characterized in that** a boundary between said at least a lightly activated high impurity concentration layer and said at least a sufficiently activated high impurity con-

centration layer is aligned to an edge of said gate electrode.

34. The method as claimed in claim 33, **characterized in that** said at least a lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in said first effectively-activated-impurity concentration range as a distance from said at least a sufficiently activated high impurity concentration layer is increased.

35. The method as claimed in claim 31, further including the step of forming a dummy layer over at least an entirety of said semiconductor layer before selectively forming a resist pattern over said dummy layer for selectively implanting said impurity through said dummy layer into said semiconductor layer in said selective impurity implantation.

36. The method as claimed in claim 35, further including the steps of :

removing said dummy layer in addition to said removal of said resist pattern; and  
 forming a gate insulating film prior to said step of selectively forming said gate electrode over said gate insulating film.

37. The method as claimed in claim 35, further including the step of having said dummy layer remain as said gate insulating film, so that said gate electrode is selectively formed over said dummy layer as said gate insulating film.

38. A method of forming a semiconductor structure in a field effect transistor, comprising the steps of:

carrying out a selective impurity-implantation for selectively implanting an impurity into a semiconductor layer, to define at least an impurity-implanted region in said semiconductor layer; and

carrying out a selective laser beam irradiation to at least a selected part of said at least an impurity-implanted region, whereby said at least a selected part of said at least an impurity-implanted region is sufficiently activated upon said selective laser beam irradiation, and said at least a selected part becomes at least a sufficiently activated high impurity concentration layer, while a remaining non-selected part of said at least an impurity-implanted region is insufficiently activated by a thermal diffusion from said at least a selected part, and said remaining non-selected part becomes at least a lightly activated high impurity concentration layer.

**39.** The method as claimed in claim 38, **characterized in that** said at least a lightly activated high impurity concentration layer has a first implanted-impurity concentration value, and a first effectively-activated-impurity concentration range which is lower than said first implanted-impurity concentration value; and

said at least a sufficiently activated high impurity concentration layer is bounded with said at least a lightly activated high impurity concentration layer, and said at least a sufficiently activated high impurity concentration layer has a second implanted-impurity concentration value which is substantially the same as said first implanted-impurity concentration value, and a second effectively-activated-impurity concentration value which is higher than said first effectively-activated-impurity concentration range.

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**40.** The method as claimed in claim 39, **characterized in that** a boundary between said at least a lightly activated high impurity concentration layer and said at least a sufficiently activated high impurity concentration layer is aligned to an edge of said gate electrode.

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**41.** The method as claimed in claim 40, **characterized in that** said at least a lightly activated high impurity concentration layer has a gentle decrease in a first effectively-activated-impurity concentration value ranged in said first effectively-activated-impurity concentration range as a distance from said at least a sufficiently activated high impurity concentration layer is increased.

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FIG. 1A prior art

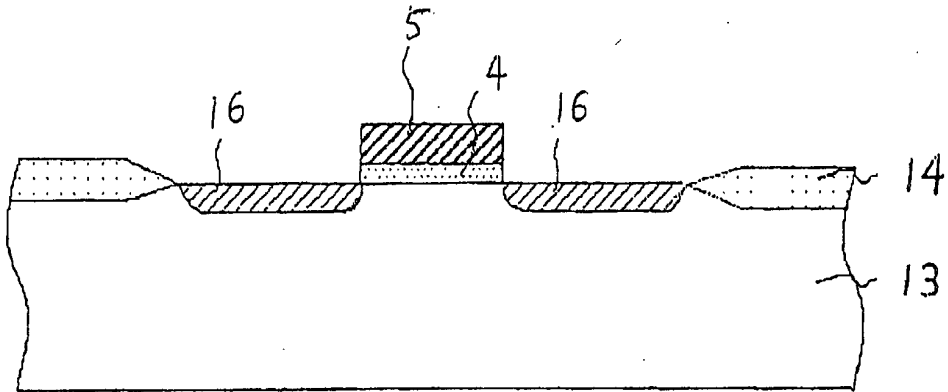


FIG. 1B prior art

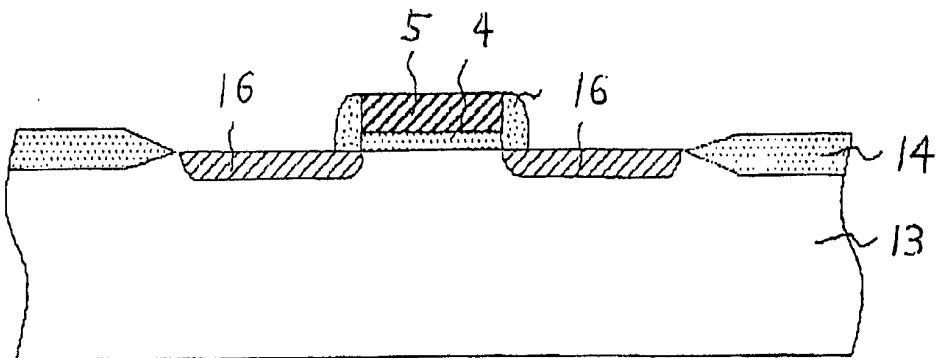


FIG. 1C prior art

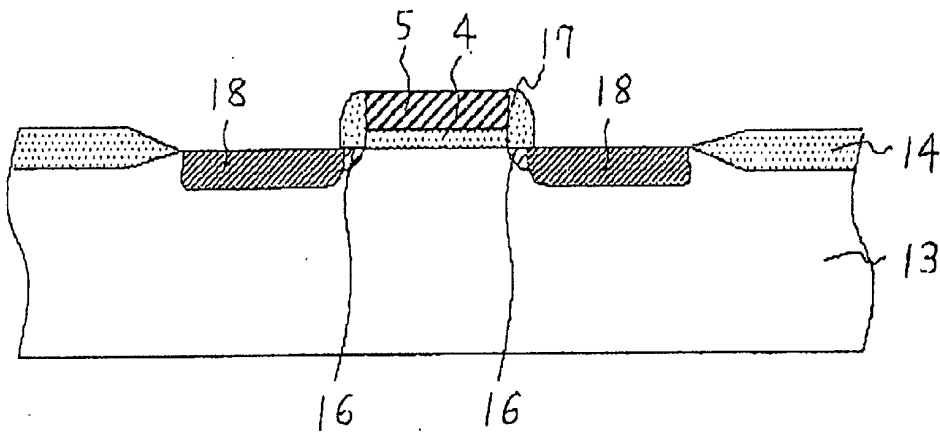


FIG. 2A prior art

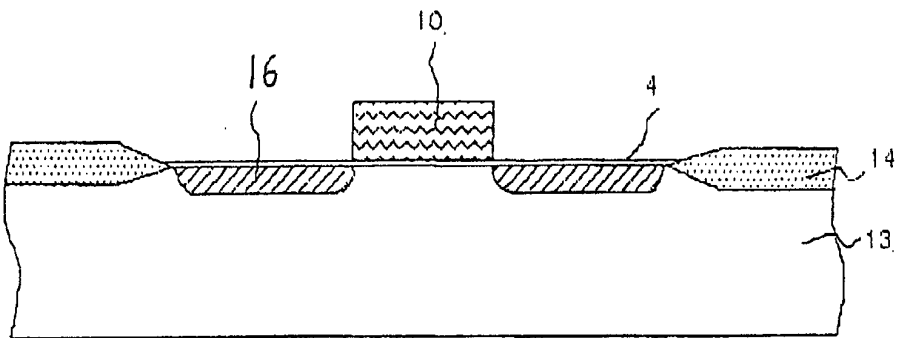


FIG. 2B prior art

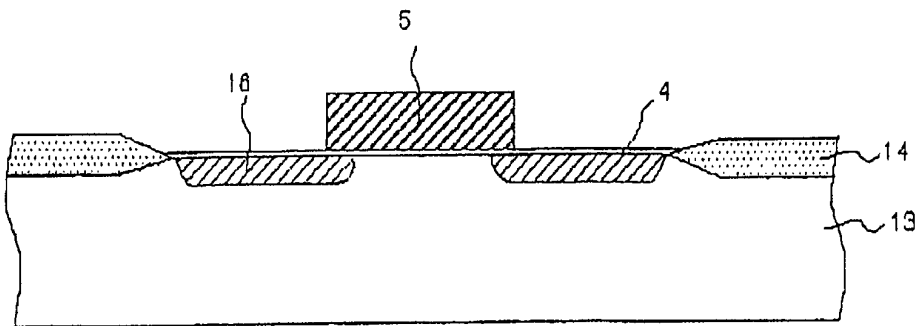


FIG. 2C prior art

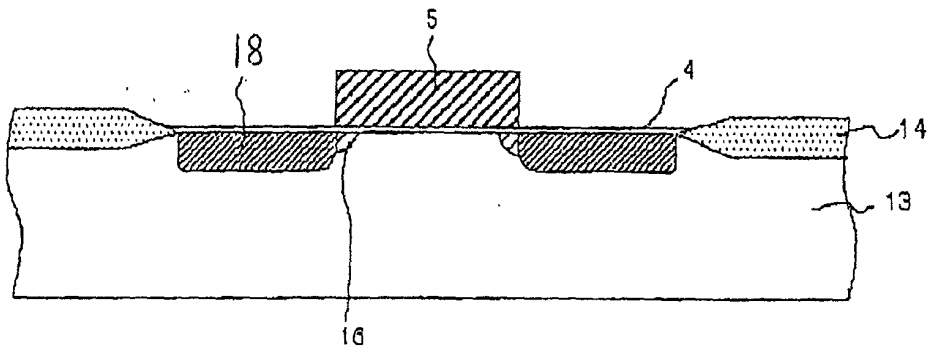


FIG. 2D prior art

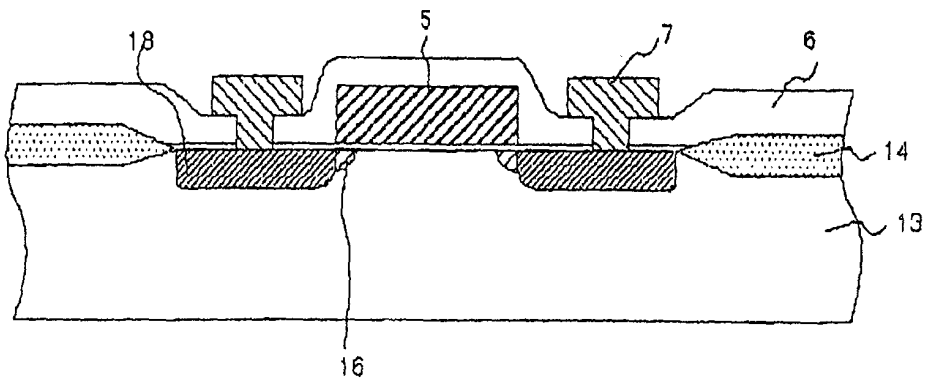


FIG. 3A prior art

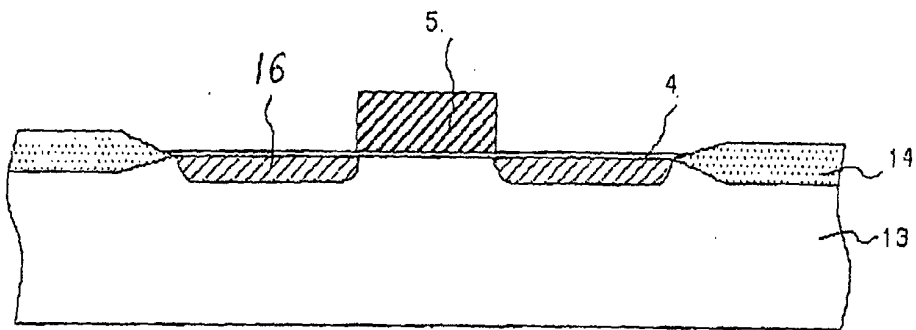


FIG. 3B prior art

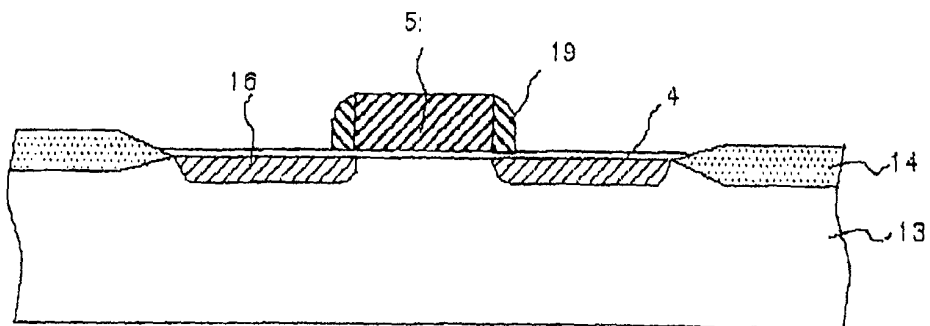


FIG. 3C prior art

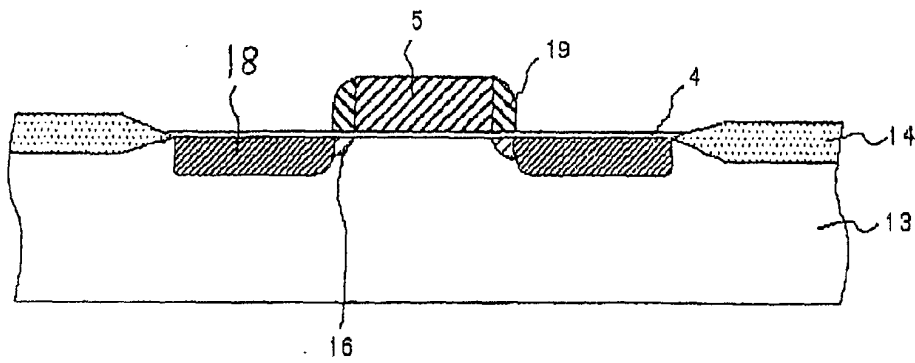


FIG. 3D prior art

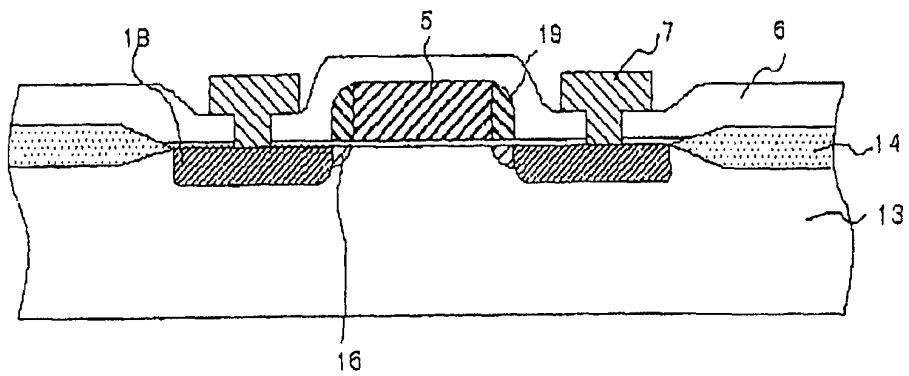
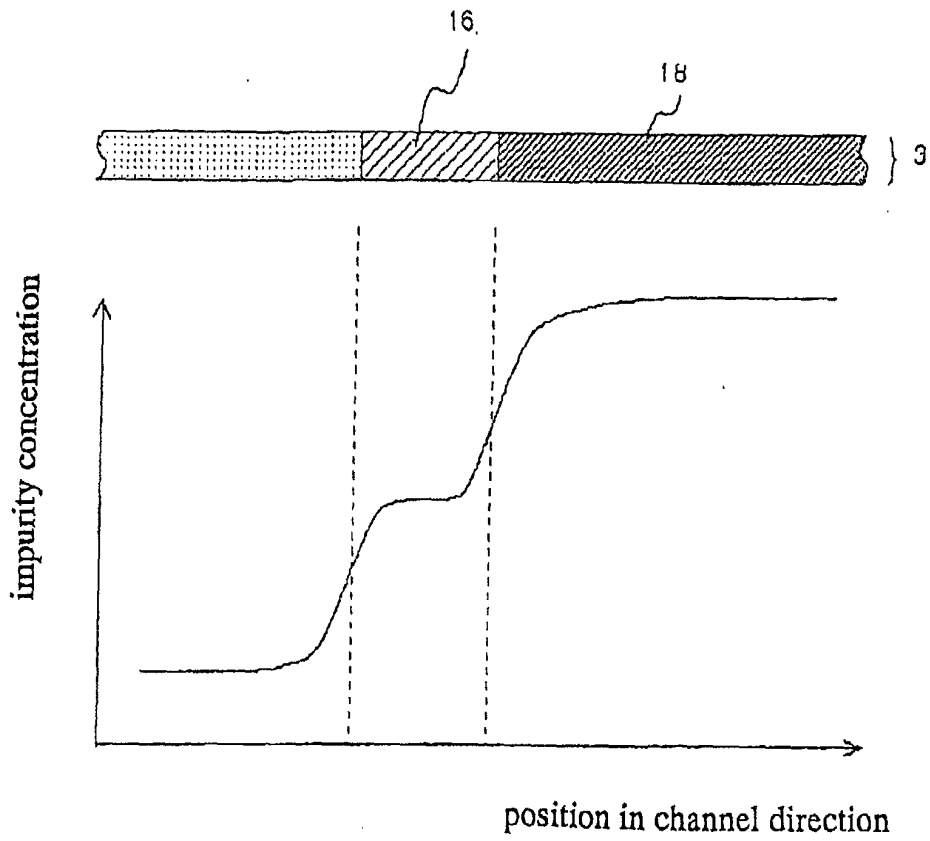


FIG. 4 prior art



conventional gate-overlap-drain structure

FIG. 5

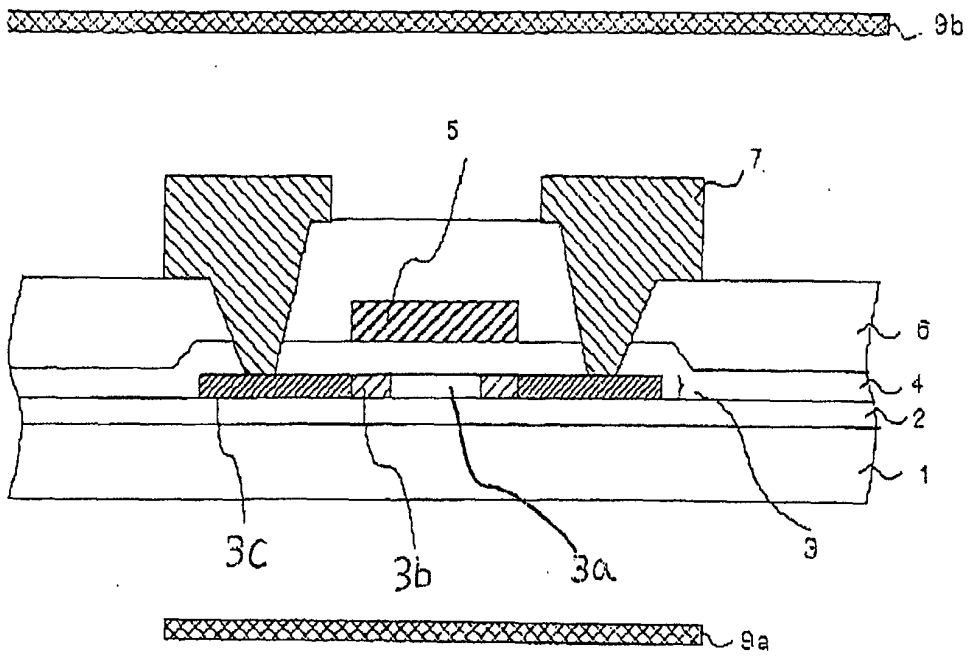


FIG. 6A

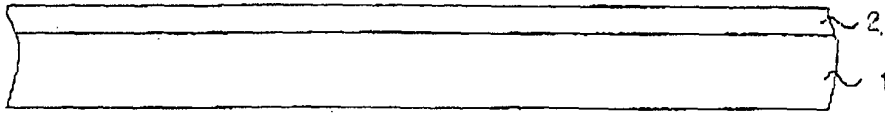


FIG. 6B

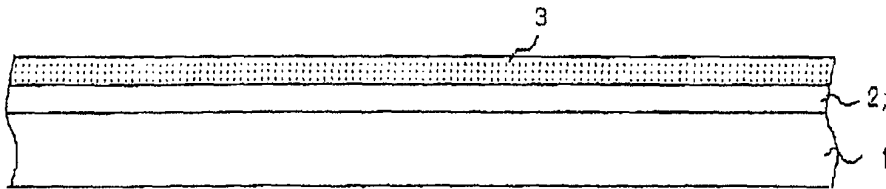


FIG. 6C

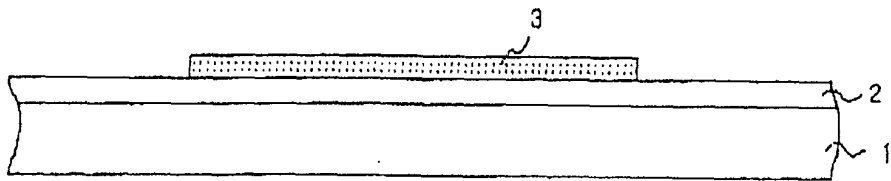


FIG. 6D

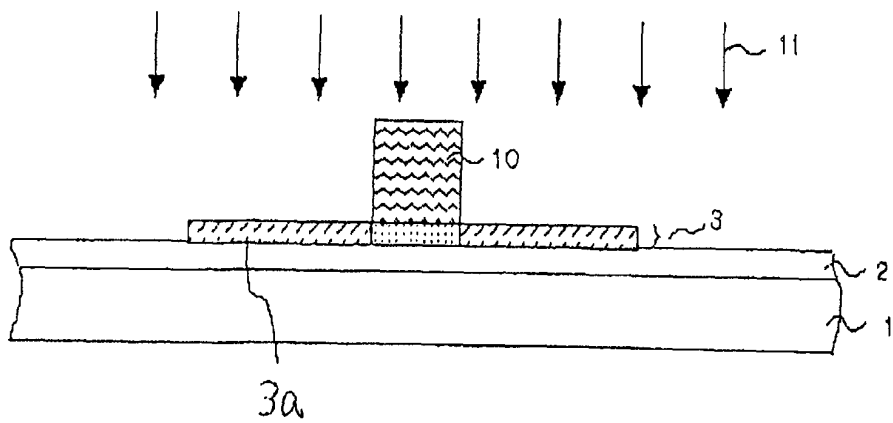


FIG. 6E

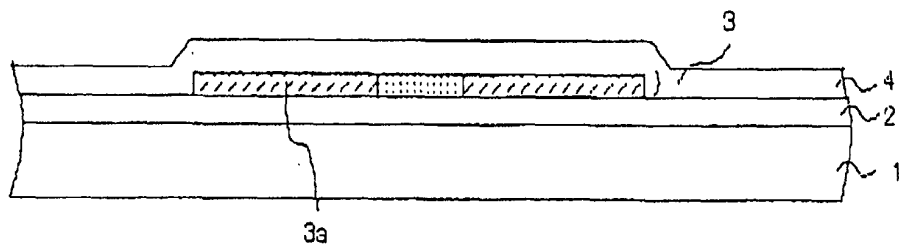


FIG. 6F

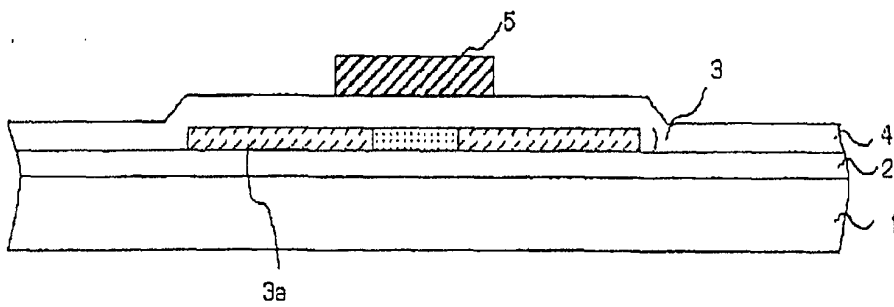


FIG. 6G

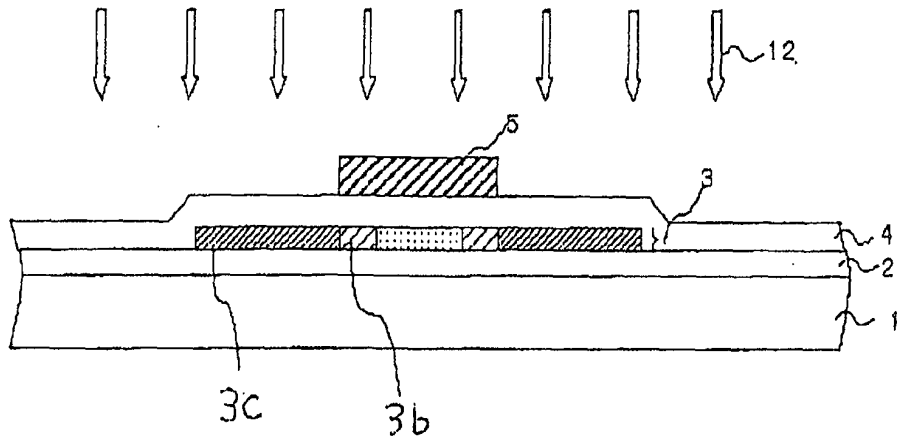


FIG. 6H

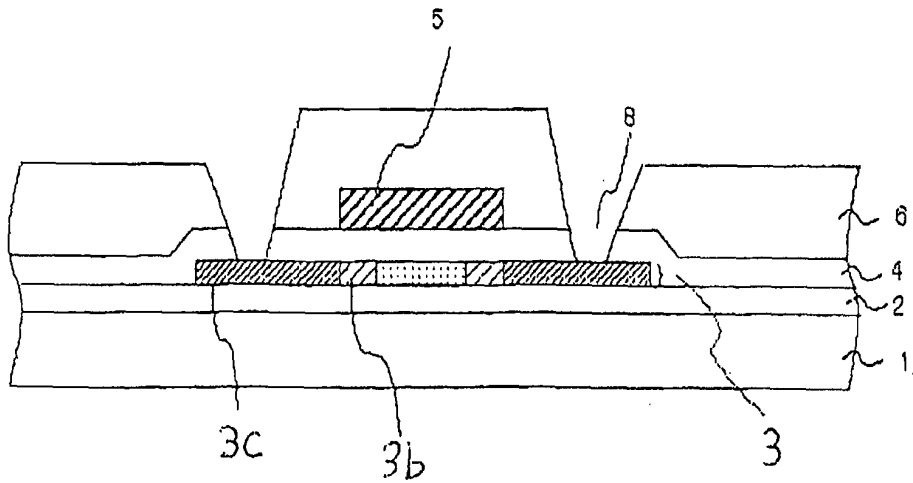


FIG. 6I

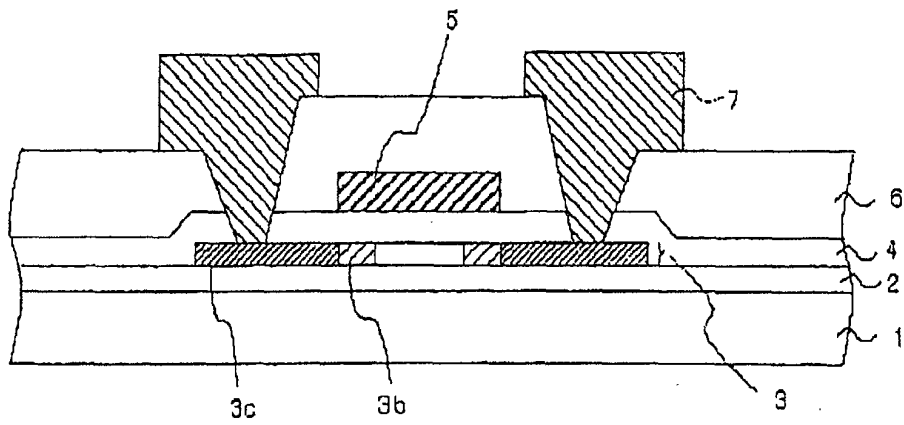
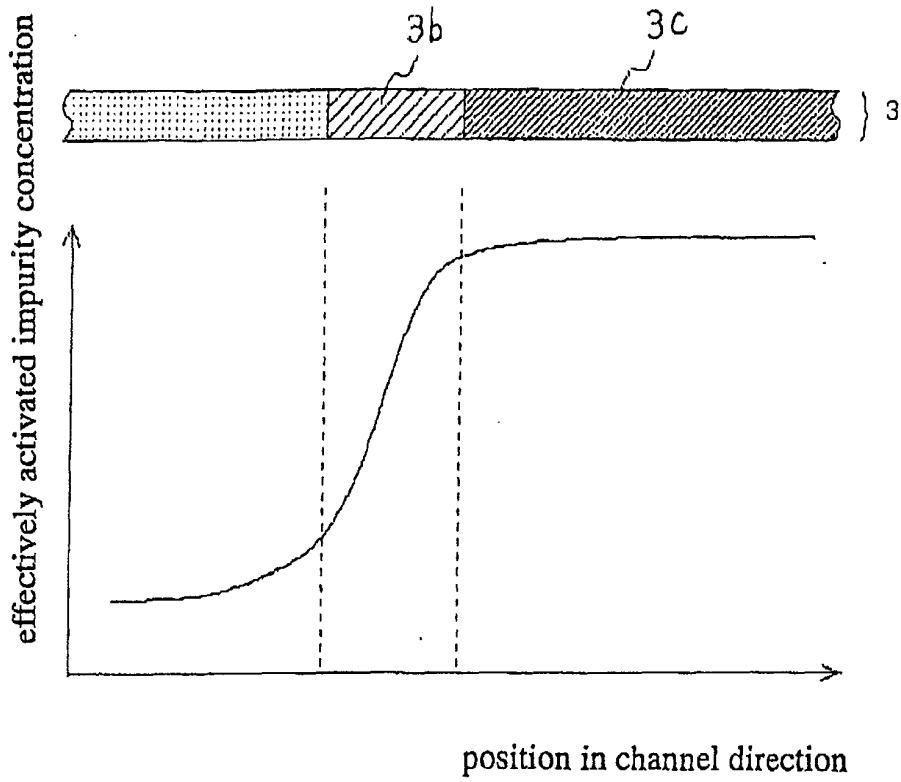


FIG. 7



improved gate-overlap-drain structure

FIG. 8

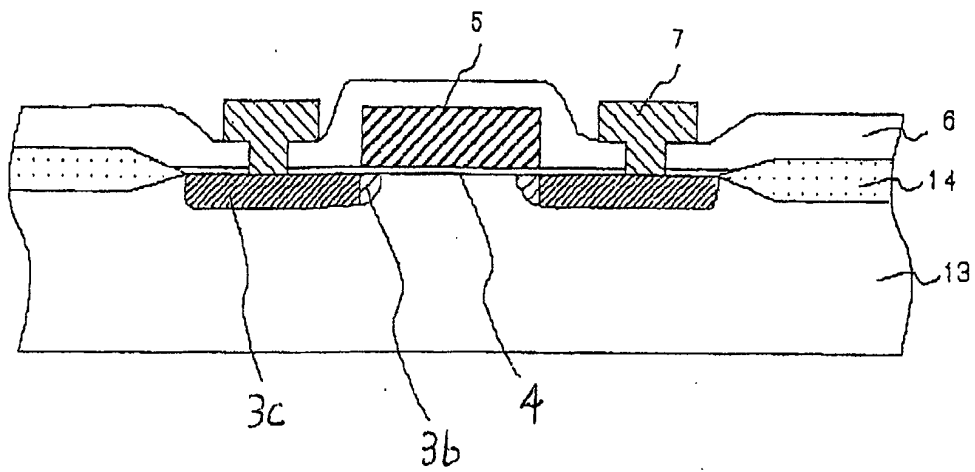


FIG. 9A

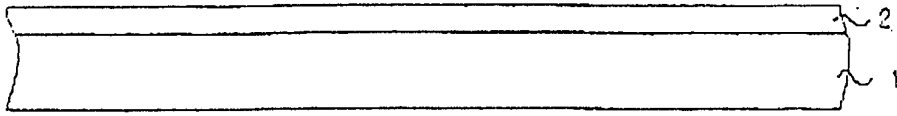


FIG. 9B

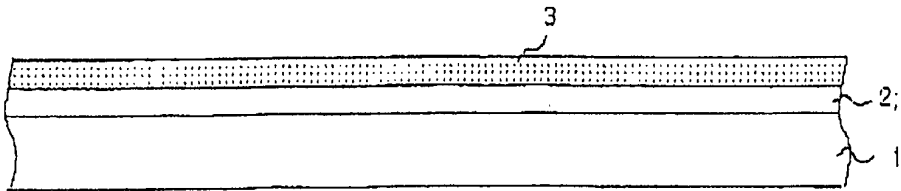


FIG. 9C

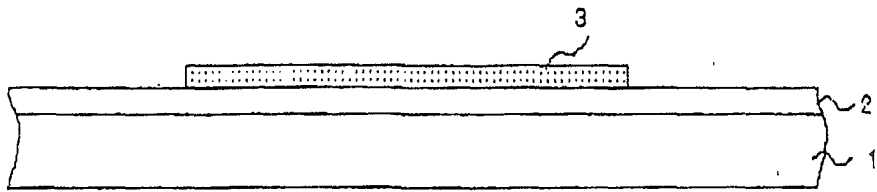


FIG. 9D

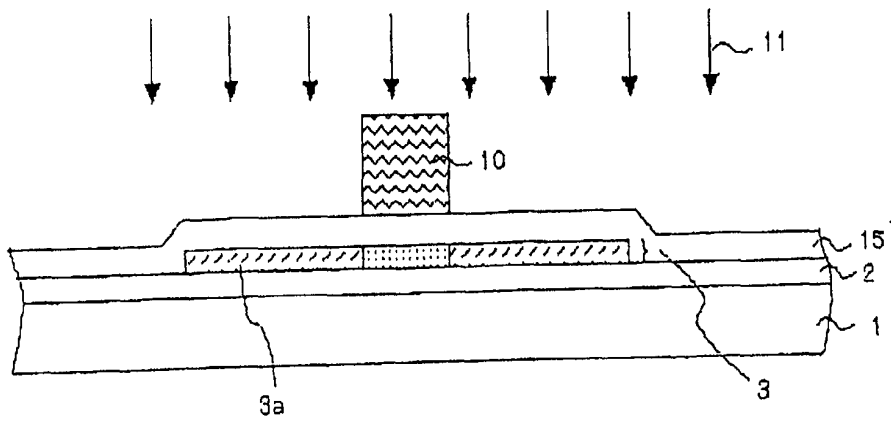


FIG. 9E

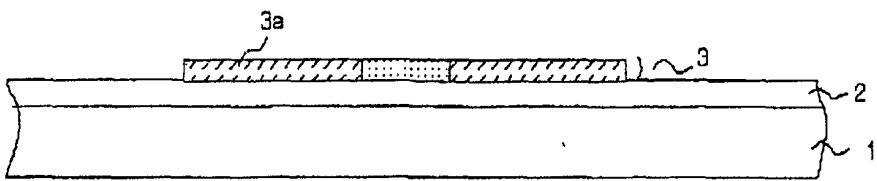


FIG. 9F

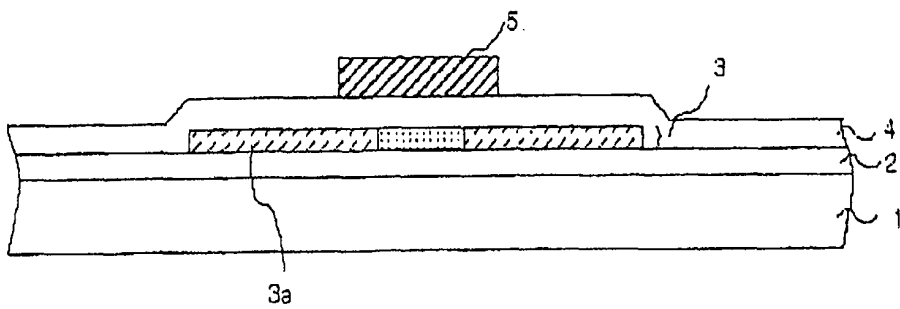


FIG. 9G

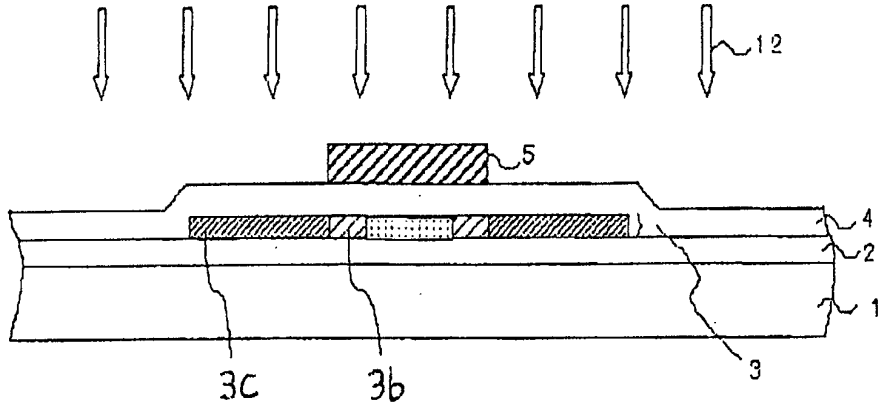


FIG. 9H

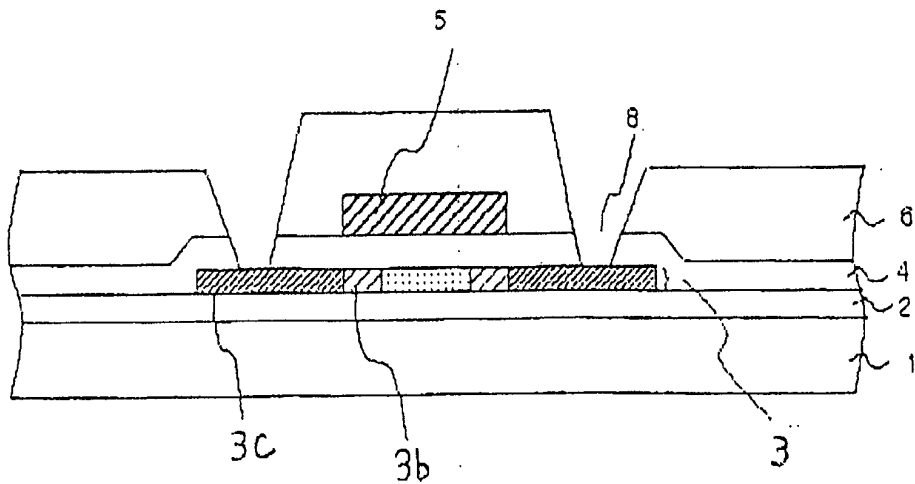


FIG. 9I

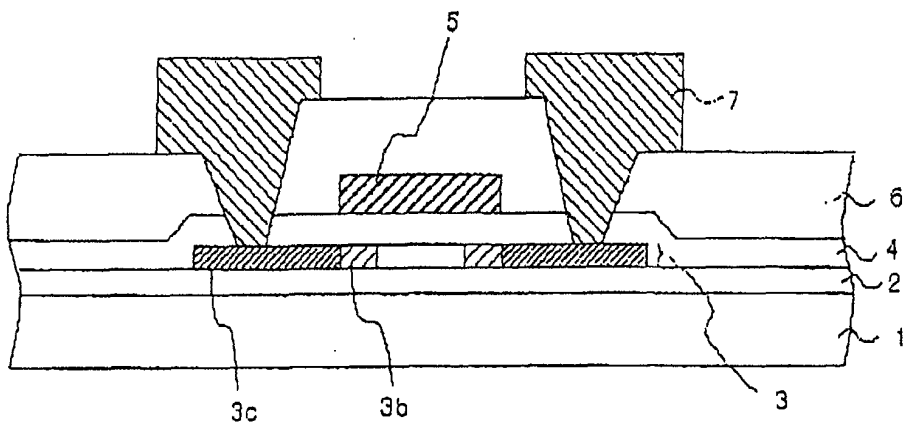


FIG. 10A



FIG. 10B

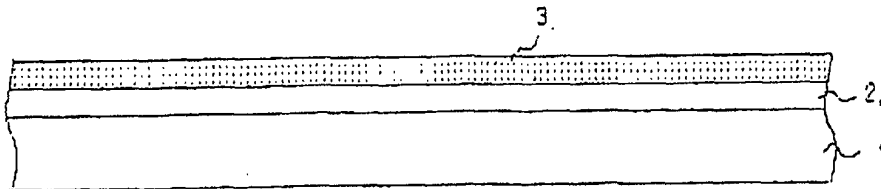


FIG. 10C

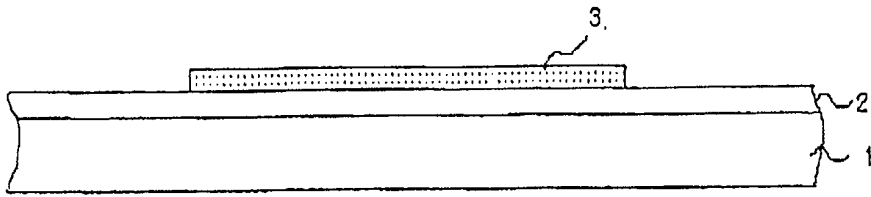


FIG. 10D

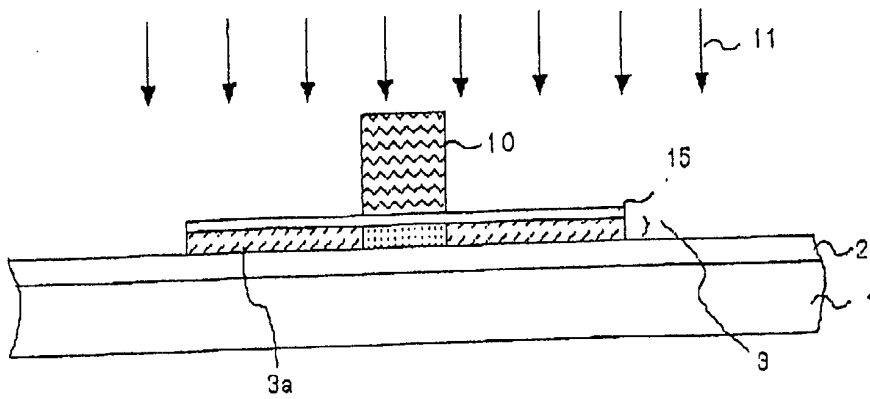


FIG. 10E

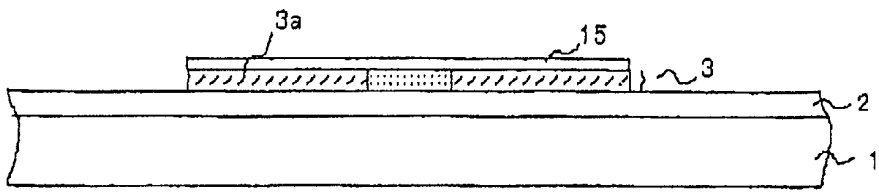


FIG. 10F

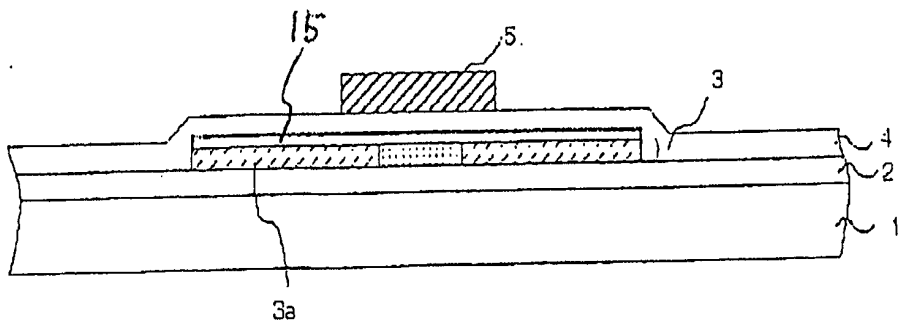


FIG. 10G

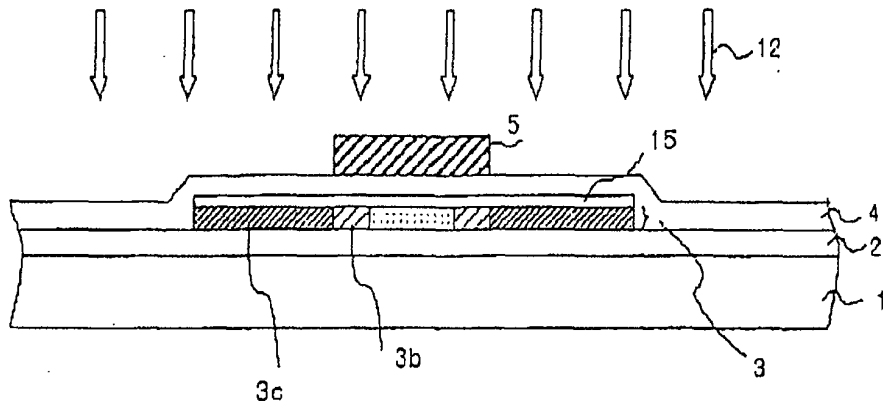


FIG. 10H

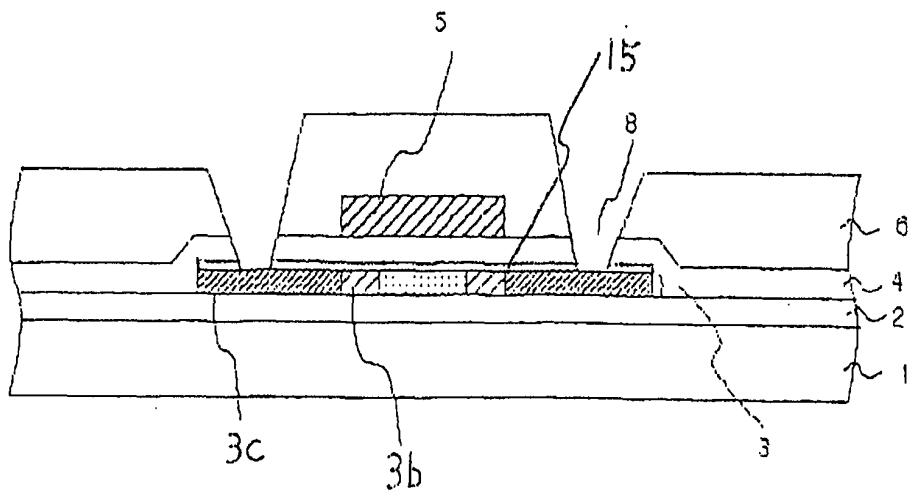


FIG. 10I

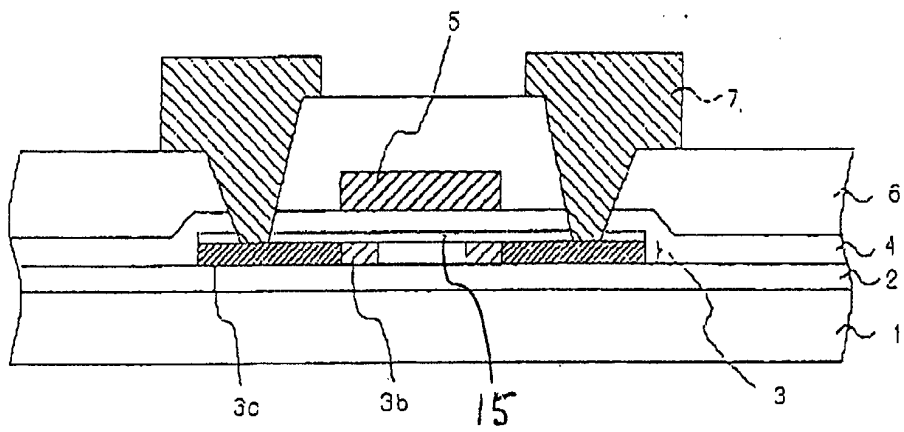


FIG. 11A

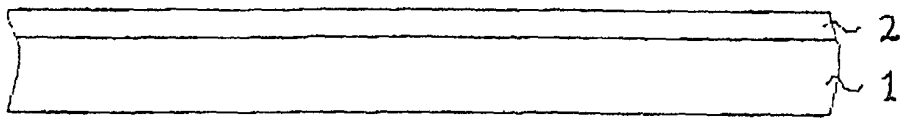


FIG. 11B

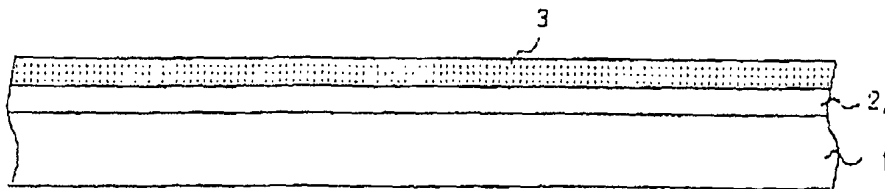


FIG. 11C

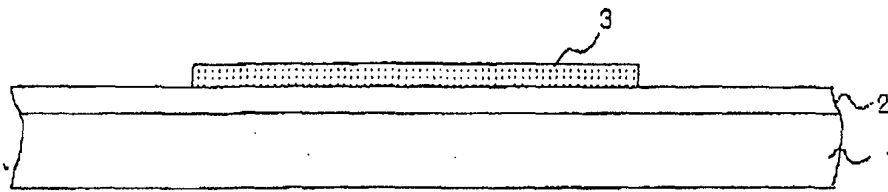


FIG. 11D

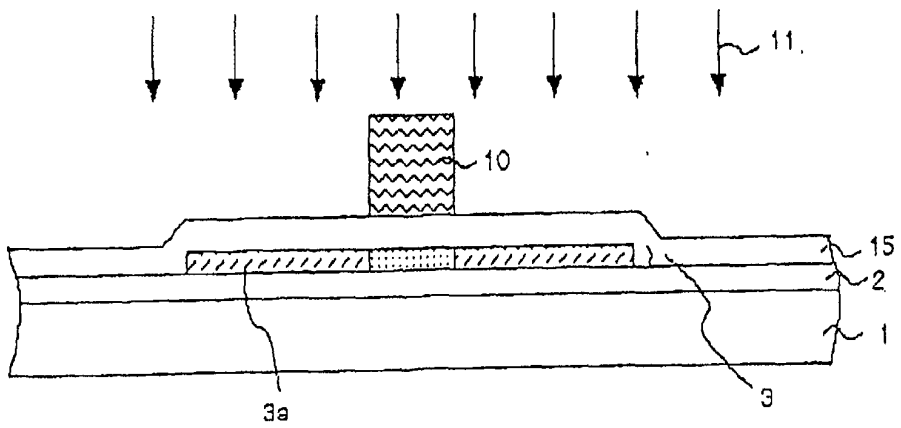


FIG. 11E

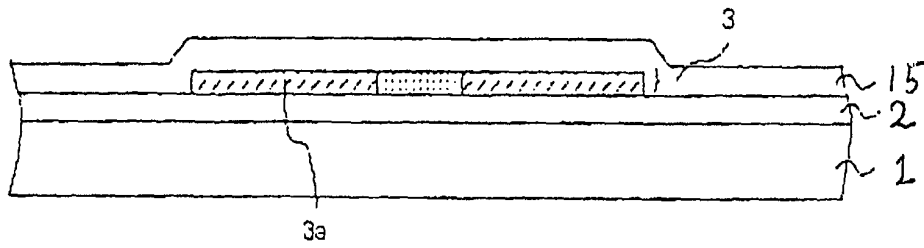


FIG. 11F

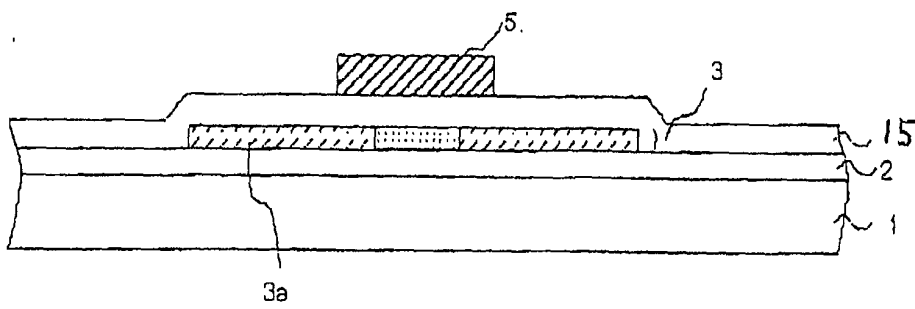


FIG. 11G

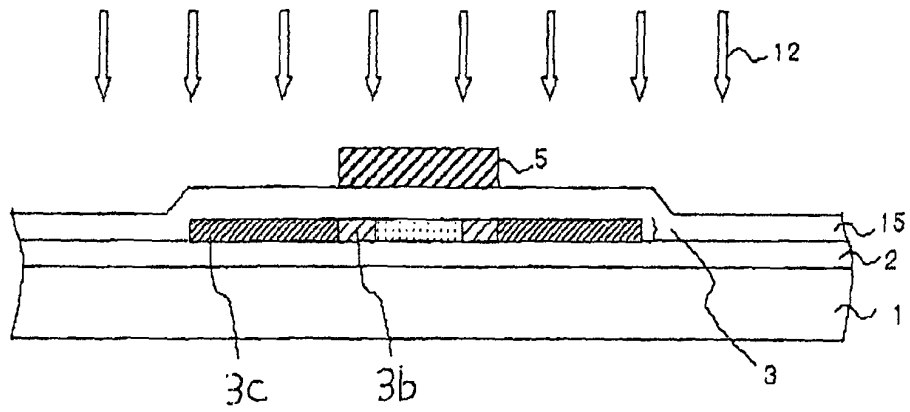


FIG. 11H

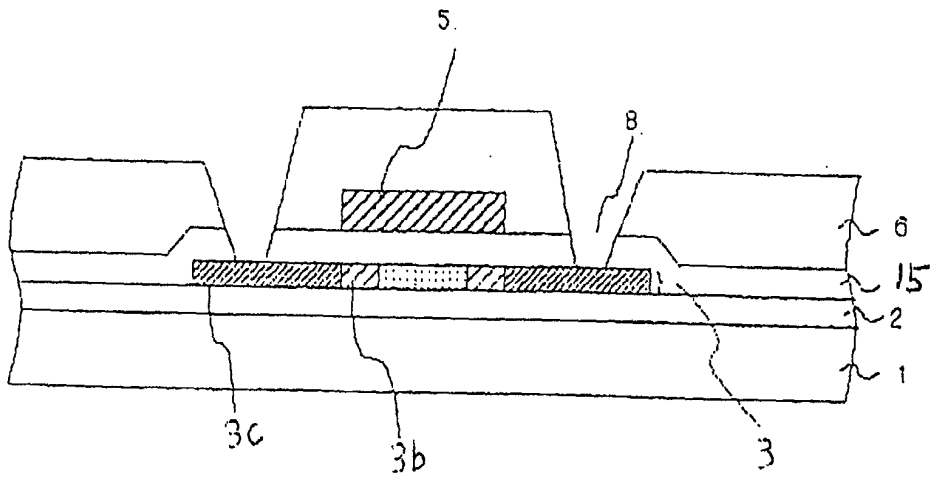


FIG. 11I

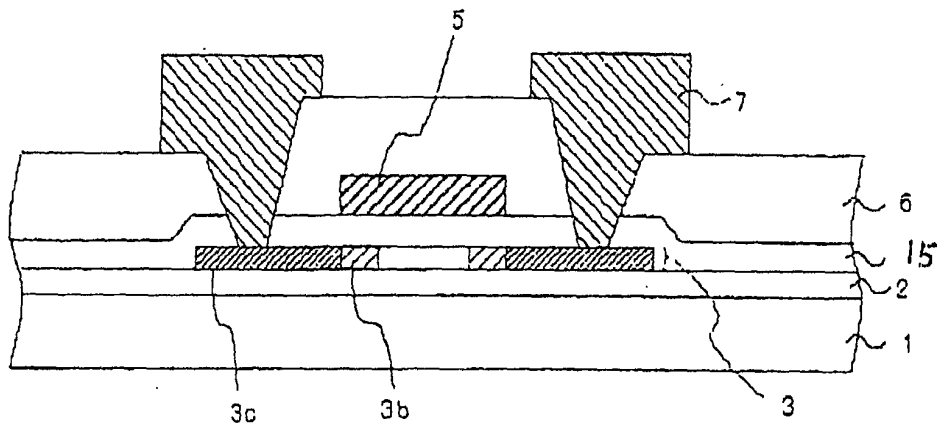
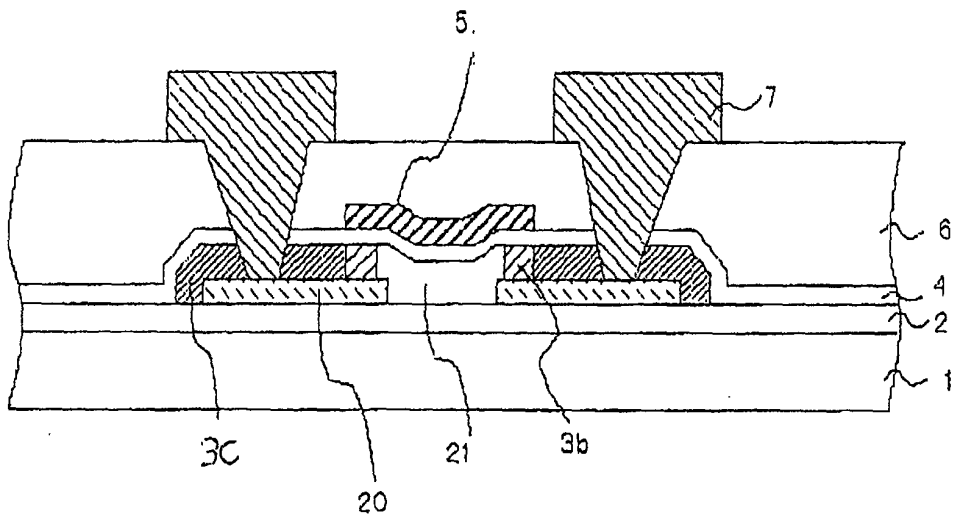


FIG. 12



专利名称(译)	场效应晶体管及其制造方法以及使用该场效应晶体管的液晶显示器及其制造方法		
公开(公告)号	<a href="#">EP1282173A2</a>	公开(公告)日	2003-02-05
申请号	EP2002017240	申请日	2002-07-31
申请(专利权)人(译)	NEC公司		
当前申请(专利权)人(译)	GETNER FOUNDATION LLC		
[标]发明人	SERA KENJI		
发明人	SERA, KENJI		
IPC分类号	G02F1/1368 H01L21/268 H01L21/336 H01L29/417 H01L29/78 H01L29/786		
CPC分类号	H01L29/66757 H01L21/268 H01L29/41733 H01L29/4908 H01L29/78621 H01L29/78627 H01L29/78666 H01L2029/7863		
优先权	2001233256 2001-08-01 JP		
其他公开文献	EP1282173A3		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

通过单对单杂质注入工艺和单激光退火工艺获得栅极 - 重叠 - 漏极结构，其中改进的栅极 - 重叠 - 漏极结构包括轻微激活的高杂质浓度区域，其显示出与轻微相同的功能。掺杂漏极区域，其中轻微激活的高杂质浓度区域与用作源极和漏极区域的高杂质浓度区域界定。边界与栅电极的边缘自对准。栅电极的侧区与轻微激活的高杂质浓度区重叠。

FIG. 1A prior art

