



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 1 249 819 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:

16.10.2002 Bulletin 2002/42

(51) Int Cl.⁷: **G09G 3/36**

(21) Application number: **02008318.4**

(22) Date of filing: **11.04.2002**

(84) Designated Contracting States:

**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE TR**

Designated Extension States:

AL LT LV MK RO SI

(72) Inventor: **Tsutsui, Yusuke**

Hashima-shi, Gifu-ken 501-6257 (JP)

(74) Representative: **Glawe, Delfs, Moll & Partner
Patentanwälte**

**Rothenbaumchaussee 58
20148 Hamburg (DE)**

(30) Priority: **11.04.2001 JP 2001112724**

(71) Applicant: **Sanyo Electric Co., Ltd.**

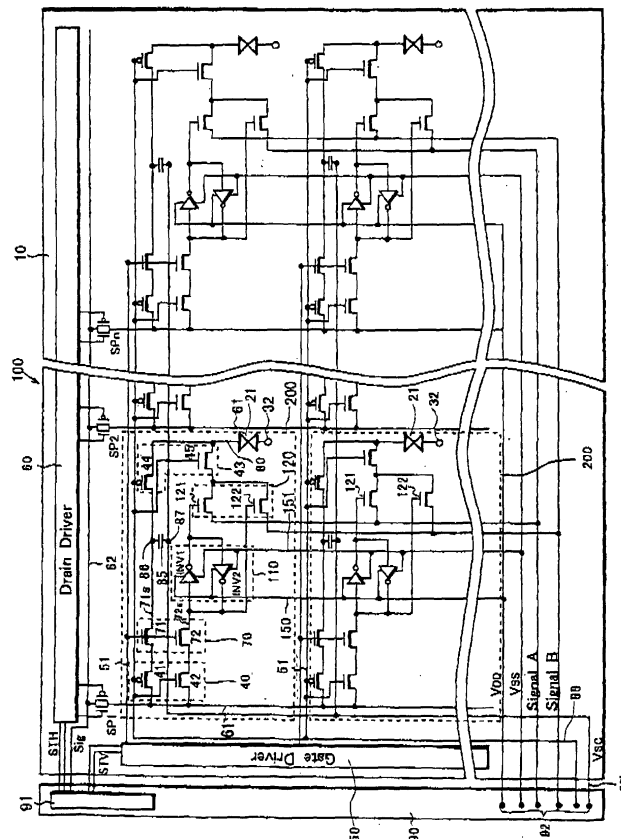
Moriguchi-shi, Osaka-fu 570-8677 (JP)

(54) Display device

(57) A display device, under a digital display mode, performs writing of digital image signals into a static memory circuit while a power voltage of about 3V is applied to the static memory with a panel drive frequency

reduced from 60 Hz to 20-30 Hz. It is, thus, possible to output the digital image signal from a frame memory directly to a liquid crystal display panel without using a level shifter.

Fig.3



EP 1 249 819 A2

Description

Background of the Invention

Field of the Invention

[0001] This invention relates to a display device, specifically to a display device which is incorporated into a portable communication and computing device.

Description of the Related Art

[0002] There has been a great demand in the market for portable communication and computing devices such as a portable TV and a cellular phone. All these devices need a small, lightweight and low-power consumption display device, and efforts have been made accordingly.

[0003] Fig. 5 shows a circuit diagram corresponding to a single pixel element of a conventional liquid crystal display device. A gate signal line 51 and a drain signal line 61 are placed on an insulating substrate (not shown) perpendicular to each other. A thin-film transistor (TFT) 72 connected to two signal lines 51, 61, is formed near the intersection of the two signal lines 51, 61. A source 11s of the TFT 65 is connected to a display electrode 80 of a liquid crystal 21.

[0004] A storage capacitor element 85 holds the voltage of the display electrode 80 during one field period. One terminal 86 of the storage capacitor 85 is connected to the source 11s of the TFT 72 and the other terminal 87 is provided with a voltage common among all the pixel elements.

[0005] When a scanning signal is applied to the gate signal line 51, the TFT 72 turns to an on-state. Accordingly, an analog image signal from the drain signal line 61 is applied to the display electrode 80, and the storage capacitor 85 holds the voltage. The voltage of the image signal is applied to the liquid crystal 21 through the display electrode 80, and the liquid crystal 21 aligns in response to the applied voltage for providing a liquid crystal display image.

[0006] Therefore, this configuration is capable of showing both moving images and still images. There is a need for the display to show both a moving image and a still image within a single display. One such example is to show a still image of a battery within an area of a moving image of a cellular phone display to show the remaining amount of the battery power.

[0007] However, the configuration shown in Fig. 6 requires a continuous rewriting of each pixel element with the same image signal at each scanning in order to provide a still image. This is basically to show a still-like image in a moving image mode, and the scanning signal needs to activate the TFT 72 at each scanning.

[0008] Accordingly, it is necessary to operate a driver circuit which generates a driver signal for the scanning signals and the image signals, and an external LSI

which generates various signals for controlling the timing of the driver circuit, resulting in a significant electric power consumption. This is a considerable drawback when such a configuration is used in a cellular phone device which has only a limited power source. That is, the time a user can use the telephone under one battery charge is considerably decreased.

[0009] Japanese Laid-Open Patent Publication No. Hei 8-194205 discloses another configuration for a display device suitable for portable applications. This display device has a static memory for each of the pixel elements, as shown in Fig. 6. A static memory, in which two inverters INV1 and INV2 are positively fed back to each other, holds the image signal. This results in reduced power consumption.

[0010] In this configuration, a switching element 24 controls the resistance between a reference line and a display electrode 80 in response to the divalent digital image signal held by the static memory in order to adjust the biasing of the liquid crystal 21. The common electrode, on the other hand, receives an AC signal Vcom. Ideally, this configuration does not need to refresh the memory when the image stays still for a period of time.

[0011] As described above, the conventional liquid crystal display device is suitable for displaying a full color moving picture in response to the analog image signal. On the other hand, the liquid crystal display device with a static memory for retaining the digital image signal is suitable for displaying a still picture with low-depth with low-energy consumption.

[0012] However, two liquid crystal display devices described above have different sources for image signals, thus, it is impossible to have both images within single display device. It is an object of the invention to provide a display device that overcomes this drawback.

Summary of the Invention

[0013] The invention lies in the features of the independent claims and preferably in those of the dependent claims. The invention provides a display device including a display panel and an image memory outputting a digital image signal. A plurality of pixel elements are disposed in the display panel. A plurality of static memory circuits are disposed for the corresponding pixel elements. The device has a panel drive circuit supplying a panel drive signal for controlling a timing of writing the digital image signal into the static memory circuits. In this configuration, an image is displayed based on the digital image signal retained in the static memory circuits, and the digital image signal is written into the static memory circuits from the image memory by reducing the frequency of the panel drive signal without a use of a level-shifter for raising the level of the digital image signal.

[0014] The invention also provides a display device including a display panel and an image memory outputting a digital image signal. The device also has a DA

converter converting the digital image signal outputted from the image memory into an analog image signal and a signal selection element selecting the analog image signal from the DA converter or the digital image signal outputted from the image memory. The selected signal is supplied to the display panel. A timing control circuit supplies a panel drive signal to the display panel. A plurality of pixel elements are disposed in the display pane. A plurality of first display circuits are disposed for the corresponding pixel elements and display an analog image in response to the analog image signal inputted based on the panel drive signal. A plurality of second display circuits are disposed for the corresponding pixel elements and display a digital image in response to the digital image signal. Each of the second display circuits has a static memory circuit which receives the digital image signal based on the panel drive signal. In this configuration, the first display circuit or the second display circuit is selected for displaying the analog image or the digital image, respectively, and the timing control circuit reduces the frequency of the panel drive signal so that the digital image signal is written into the static memory circuit from the image memory without a use of a level-shifter for raising the level of the digital image signal.

[0015] The invention further provides methods having the features of claim 6 and 7.

Brief Description of the Drawings

[0016]

Fig. 1 is a circuit block chart of a liquid crystal display device of an embodiment of this invention.

Fig. 2 is a block chart of the amplifier 4 of Fig. 1.

Fig. 3 is a circuit diagram of the liquid crystal display device of the embodiment of this invention.

Fig. 4 is a timing chart of the liquid crystal display device under the digital display mode.

Fig. 5 is a circuit diagram of a conventional liquid crystal display device.

Fig. 6 is a circuit diagram of another conventional liquid crystal display device.

Fig. 7 is a block chart of an amplifier of a liquid crystal display device which forms a basis of this invention.

Detailed Description of the Invention

[0017] This invention is directed to a display device, which can alternate between two kinds of display modes, an analog display mode and a digital display mode, as described in commonly owned copending U.

S. Patent Application Serial No. 09/953,233 and the parallel European Patent Application No. 01 122 308.8, entitled "DISPLAY DEVICE AND ITS CONTROL METHOD." The disclosure of U.S. Patent Application Serial No. 09/953,233 is in its entirety incorporated herein by reference.

[0018] Based on a display mode switching signal, the liquid crystal display panel receives either an analog image signal or a digital image signal. Under an analog display mode, the analog image signal is inputted into the first display circuit having a storage capacitance element, and under a digital display mode, the digital image signal is written into a static memory disposed for each of the display pixel elements in the liquid crystal display panel. In this configuration, an amplifier for amplifying the amplitude of these signals is required and the amplified signals is supplied to the liquid crystal display panel.

[0019] In Fig. 7 shows a configuration of such an amplifier. The analog amplifier 10 amplifies the inputted analog image signal. The level shifter 11 raises the amplitude of the inputted digital image signal. Usually, the inputted digital image signal has a voltage amplitude of 3Vp-p. However, about 6V is required as a source voltage of the static memory circuit in order for the digital image signal to be written into the static memory circuit disposed for each of the pixel elements in the liquid crystal display panel under an ordinary panel driver frequency (60Hz). Therefore, the level shifter, which raises the voltage amplitude of the inputted digital image signal (3Vp-p) to about 6V, is required.

[0020] Then, the switching element 12 is switched based on the display mode switching signal MD. Therefore, under the ordinary display mode (analog display mode), the analog image signal amplified by the analog amplifier 10 is outputted to the liquid crystal display panel, and under the digital display mode, the digital image signal amplified by the level shifter 11 is outputted to the liquid crystal display panel.

[0021] Fig. 1 shows a circuit block chart of a display device of an embodiment of this invention.

[0022] The signal processing circuit 1 performs the various signal processing tasks such as contrast adjustment and brightness adjustment for a digital image signal inputted through a CPU interface. The processed digital image signal is temporarily stored in the frame memory 2. The frame memory 2 is one type of image memory and comprises DRAM or flash memory.

[0023] Image signal outputted at certain timing from the frame memory 2 are converted into the analog image signal by the DA converter 3, and then inputted to the amplifier 4.

[0024] As seen in Fig. 2, the analog amplifier 10 disposed in the amplifier 4 amplifies the analog image signal. On the other hand, the digital image signal (voltage amplitude 3Vp-p) outputted from the frame memory 2 is directly inputted to a switch 12 without passing through a level shifter. The switch 12 performs the switching

based on a display mode-switching signal MD.

[0025] Therefore, under the normal display mode (analog display mode), the analog image signal amplified by the analog amplifier 10 is outputted to the liquid crystal display panel 100, and under the digital display mode, the digital image signal with the voltage amplitude of 3Vp-p is outputted to the liquid crystal display panel 100.

[0026] The timing control circuit 6 outputs control signals for controlling the panel drive signal PC, signal processing circuit 1, frame memory 2, and DA converter 3 based on the system clock CLK, horizontal synchronization signal Hsync and the vertical synchronization signal Vsync from the oscillator 5.

[0027] In the configuration of Fig. 7, in order to write the digital image signal into a static memory disposed for each of the display pixel elements of the liquid crystal display panel 100 under the ordinary panel drive frequency (60 Hz), 6V is necessary as the power voltage of the static memory circuit. The level shifter 11 is needed for this purpose. A panel drive frequency is a frequency of the sampling pulse, as described later.

[0028] However, in this embodiment, by reducing the panel drive frequency from 60 Hz to 20-30 Hz, a power voltage of about 3 V can be used to write a digital signal in the static memory.

[0029] Therefore, the digital image signal outputted from the frame memory 2 can be directly outputted to the liquid crystal display panel 100 without passing through a level shifter.

[0030] As shown in Fig. 1, the white/black voltage generating circuit 7, based on the signal from the timing control circuit 6, outputs the white signal (signal A, as described later) and the black signal (signal B, as described later) to the liquid crystal display panel 100. Also, the reference numeral 8 denotes the amplifier that amplifies the common electrode drive signal of the liquid crystal.

[0031] Next, the configuration of the liquid crystal display device, especially the detailed configuration of the liquid crystal display panel 100 will be explained in reference to the circuit diagram in Fig. 3.

[0032] On an insulating board 10, a plurality of gate signal lines 51 connected to a gate driver 50 supplying a scanning signal are disposed in one direction. A plurality of drain signal lines 61 are disposed in the direction perpendicular to the gate signal line 51.

[0033] In response to the timing of a sampling pulse outputted from a drain driver 60, the respective sampling transistors SP1, SP2, --- SPn sequentially turn on, supplying the data signal (analog image signal or digital image signal) of a data signal line 62 to the drain signal line 61.

[0034] On a liquid crystal display panel 100, a plurality of pixel elements are disposed in a matrix configuration, which are selected by the scanning signal fed from the gate signal line 51 and which are provided with the data signal fed from the drain signal line 61.

[0035] The detailed configuration of a pixel element 200 will be explained hereinafter. Near the crossing of the gate signal line 51 and drain signal line 61, a circuit selection circuit 40 comprising a P channel TFT 41 and an N channel TFT 42 is formed. Both drains of the TFTs 41 and 42 are connected to the drain signal line 61 and both gates of these TFTs are connected to a circuit selection signal line 88. Either one of TFTs 41 or 42 turns on based on the selection signal from the circuit selection signal line 88. Also, as explained later, a circuit selection circuit 43 is formed, making a pair with the circuit selection circuit 40.

[0036] Therefore, selecting as well as the changing between the analog display mode (full color moving image) and the digital display mode (low energy consumption, still image) is possible. Also, a pixel element selection circuit 70 having an N channel TFT 71 and an N channel TFT 72 is formed adjacent to the circuit selection circuit 40. The pixel element selection TFTs 71 and 72 are connected to the circuit selection TFTs 41 and 42 of the circuit selection circuit 40 in the vertical direction, respectively. Also, both gates of the TFTs 71, 72 are connected to the gate signal line 51. Both of the TFTs 71 and 72 turn on simultaneously in response to the scanning signal fed from the gate signal line 51.

[0037] A storage capacitance element 85 holds the analog image signal under the analog mode. One electrode 86 of the storage capacitance element 85 is connected to the source 71s of the TFT 71. Another electrode 87 is connected to a common storage capacitance line CSL carrying a bias voltage VCS. When the analog image signal is applied to a liquid crystal 21 after the opening of the TFT gates of the circuit selection circuit 70, the voltage of the applied signal may decrease even during a one-field period, resulting in a loss of homogeneity of the display image. The storage capacitance element 85 maintains the applied voltage at the initial level during one field period for eliminating the problem above.

[0038] A P channel TFT 44 of the circuit selection circuit 43 is placed between the storage capacitance element 85 and the liquid crystal 21, and turns on and off in synchronization with the switching of the TFT 41 of the circuit selection circuit 43. A static memory circuit 110 and a signal selection circuit 120 are placed between the TFT 72 of the pixel element selection circuit 70 and a display electrode 80 of the liquid crystal 21.

[0039] The static memory circuit 110 has two inverter circuits, the first and second inverter circuits, which are positively fed back to each other. The source 72s of the pixel element selection TFT 72 is connected to an input terminal of the first inverter circuit INV1, and its output is inputted to the second inverter circuit INV2. Also, an output terminal of the second inverter circuit INV2 is connected to the input terminal of the first inverter circuit INV1.

[0040] Under the digital display mode, when the voltage of the circuit selection signal line 88 is "H", and when

the scanning signal of the gate signal line 51 also is "H", the writing into the static memory circuit 110 is possible.

[0041] The signal selection circuit 120 is the circuit selecting the signal based on the digital image signal retained in the static memory circuit 110 and comprises two N-channel TFTs 121, and 122. To the gates of the TFTs 121, 122, the output signal is complementarily supplied from the static memory circuit 110 and thus, the TFTs 121, 122 complementarily turn on and off.

[0042] Here, the AC drive signal (signal B) is selected when the TFT 122 turns on, and the common electrode signal VCOM (signal A) is selected when the TFT 121 turns on. The selected signal is then applied to the display electrode 80, which supplied the voltage to the liquid crystal 21, through the TFT 45 of the circuit selection circuit 43.

[0043] The liquid crystal panel 100 has peripheral circuit as well. An LSI 91 for driver scanning is mounted on an external circuit board 90 retrofitted to the insulating substrate 10 of the liquid crystal panel 100, and sends a vertical start signal STV and a horizontal start signal STH to the gate driver 50 and the drain driver 60, respectively. The panel driver LSI also feeds the image signal to a data line 62.

[0044] The driving method of the display device described above will be explained hereinafter in reference to Figs. 3 and 4. Fig. 4 shows a timing chart when the liquid crystal display device is set to operate under the digital display mode.

(1) Analog Display Mode.

[0045] When the analog display mode is selected in response to the mode switching signal MD, the analog image signal is outputted to the data signal line 62 from the DA converter 3. Also, the voltage applied to the circuit selection signal line 88 changes to "L", so that the TFTs 41, 44 of the circuit selection circuits 40, 43 turn on.

[0046] The sampling transistor SP turns on in response to the sampling signal based on the horizontal start signal STH so that the analog image signal of the data signal line 62 is supplied to the drain signal line 61. The sampling signal corresponds to the panel drive signal and its frequency is 60 Hz under the analog display mode.

[0047] Also, the scanning signal is supplied to the gate signal line 51 in accordance with the vertical start signal STV. When the TFT 71 turns on in response to the scanning signal, the analog image signal Sig is applied, through the drain signal line 61, to the display electrode 80 and the storage capacitance element 85, which holds the applied voltage. The liquid crystal 21 aligns itself in accordance with the image signal voltage applied to the liquid crystal 21 fed from the display electrode 80, to form a display image.

[0048] The analog display mode is suitable for showing a full color moving picture.

(2) Digital Display Mode

[0049] When the digital display mode is selected in response to the mode switching signal MD, the data signal line 62 is set to receive the digital image signal outputted from the frame memory 2. At the same time, the voltage of the circuit selection signal line 88 turns to "H", and the static memory circuit 110 is set to be operable. Further, the TFTs 41, 44 of the circuit selection circuits 40, 43 turn off and the TFTs 42, 45 turn on.

[0050] The LSI 91 for driver scanning on the external circuit board 90 sends start signals STV, STH to the gate driver 50 and the drain driver 60 respectively. In response to the start signals, the sampling signals are sequentially generated and turn on the respective sampling transistors SP1, SP2, --- SPn sequentially, which sample the digital image signal Sig and send it to each of the drain signal lines 61.

[0051] The operation of the first row of the matrix, or the operation of the gate signal line 51, which receives the scanning signal G1, will be described below. First, the scanning signal G1 turns on each TFT of the pixel elements, P11, P12, --- P1n connected to the gate signal line 51, for one horizontal scanning period.

[0052] In the pixel element P11 located at the upper left corner of the matrix, the sampling signal SP 1 allows an intake of the digital image signal S11 and feeds it to the drain signal line 61. The scanning signal G1 becomes "H", turning the TFT 70 on. Thus, the drain signal D1 is written into the static memory circuit 110.

[0053] Under the digital display mode, the frequency of the sampling signal is reduced to 20 - 30 Hz by the timing control circuit 6 described above. Therefore, it is possible to write the signal into the static memory circuit 110 without amplifying it using a level shifter

[0054] The signal retained by the static memory circuit 110 is then fed to the signal selection circuit 120, and the signal selection circuit 120 selects one of the signal A and signal B. The selected signal is then applied to the liquid crystal 21 through the display electrode 80. Thus, upon a completion of a scanning from the first gate signal line 51 on the top row of the matrix to the last gate signal line 51 on the bottom row of the matrix, a full display frame scan (one field scan) is completed.

[0055] Then, the display in accordance with the data held in the static memory circuit 110 (still picture display) appears. Under this digital display mode, the supply of the power voltage to the circuits such as the gate driver 50, the drain driver 60 and the external LSI 91 for driver scanning is halted. In the meantime, the static memory circuit 110 continuously receives the voltages VDD, VSS. Also, the common electrode 32 receives the common electrode voltage and the signal selection circuit 120 receives the signal A and the signal B.

[0056] That is, when the static memory circuit 110 receives the VDD, VSS for its operation and when the common electrode voltage VCOM (signal A) is applied to the common electrode, the liquid crystal display panel

100 is in the normally-white (NW) mode. In this mode, the same voltage as the common electrode 32 is applied to the signal A and only the AC drive voltage (for example 60Hz) for driving the liquid crystal is applied to the signal B.

[0057] In this way, the data for one still picture is retained and displayed. Other circuits such as the gate driver 50, the drain driver 60 and the external LSI 91 for driver scanning do not receive voltage.

[0058] When the static memory circuit 110 receives the digital image signal of "H (high)" through the drain signal line 61, the first TFT 121 of the signal selection circuit 120 receives an "L" signal and accordingly turns off, and the second TFT 122 receives an "H" signal and turns on.

[0059] In this case, the signal B is selected and the liquid crystal 21 receives the signal B having a phase opposite to the signal A applied to the common electrode 32, resulting in the rearrangement of the liquid crystal 21. Since the display panel is in a NW mode, a black image results.

[0060] When the static memory circuit 110 receives the digital image signal of "L" through the drain signal line 61, the first TFT 121 of the signal selection circuit 120 receives an "H" signal and accordingly turns on, and the second TFT 122 receives an "L" signal and turns off. In this case, the signal A is selected and the liquid crystal 21 receives the signal A, which has the same voltage applied to the common electrode 32. As a result, there is no change in the arrangement of the liquid crystal 21 and the pixel element stays white.

[0061] In the explanation about the above embodiment, one-bit digital data signal is inputted in the digital display mode. However, this invention is not limited to that embodiment, and is also applicable to multiple-bit data signal system. In such a configuration, a multiple-level image representation is possible. Also, in such a configuration, it is necessary to provide the retaining circuits and the signal selection circuits in accordance with the number of the bits used in the system.

[0062] In the display device of this invention, the digital image signal can be written into the static memory circuit from the image memory without shifting the amplitude of the signal by reducing the frequency of the panel drive signal. That is, the level shifter for amplifying the digital image signal fed from the image memory is not needed, leading to the reduction of the circuit size. It is also possible to put the analog signal processing element and the digital signal processing circuit together on one chip.

[0063] The above is a detailed description of the particular embodiment of the invention which is not intended to limit the invention to the embodiment described. It is recognized that modifications within the scope of the invention will occur to a person skilled in the art. Such modifications and equivalents of the invention are intended for inclusion within the scope of this invention.

Claims

1. A display device comprising:

- a display panel (100);
- an image memory (2) outputting a digital image signal;
- a plurality of pixel elements (200) disposed in the display panel (100);
- a plurality of static memory circuits (110) disposed for corresponding pixel elements (200); and
- a panel drive circuit (6) supplying a panel drive signal for controlling a timing of writing the digital image signal into the static memory circuits (110);

wherein an image is displayed based on the digital image signal retained in the static memory circuits (110), and the digital image signal is written into the static memory circuits (110) from the image memory (2) by reducing a frequency of the panel drive signal without a use of a level-shifter for raising a level of the digital image signal.

2. A display device comprising:

- a display panel (100);
- an image memory (2) outputting a digital image signal;
- a DA converter (3) converting the digital image signal outputted from the image memory (2) into an analog image signal;
- a signal selection element (12) selecting the analog image signal from the DA converter (3) or the digital image signal outputted from the image memory (2), the selected signal being supplied to the display panel (100);
- a timing control circuit (6) supplying a panel drive signal to the display panel (100);
- a plurality of pixel elements (200) disposed in the display panel (100);
- a plurality of first display circuits disposed for corresponding pixel elements (200) and displaying an analog image in response to the analog image signal inputted based on the panel drive signal; and

- a plurality of second display circuits disposed for corresponding pixel elements and displaying a digital image in response to the digital image signal, each of the second display circuits having a static memory circuit (110) which receives the digital image signal based on the panel drive signal;

wherein the first display circuit or the second display circuit is selected for displaying the analog image or the digital image, respectively, and the timing control circuit (6) reduces a frequency of the panel drive signal so that the digital image signal is written into the static memory circuit (110) from the image memory (2) without a use of a level-shifter for raising a level of the digital image signal.

3. The display device of claim 2, wherein the reduced frequency of the panel drive signal which is used when one of the second display circuits is selected is lower than a frequency of the panel drive signal which is used when one of the first display circuits is selected.
4. The display device of claims 1 or 3, wherein the static memory circuit (110) comprises a first inverter circuit (INV1) and a second inverter circuit (INV2) positively feeding back to each other.
5. The display device of claim 4, wherein the first inverter circuit (INV1) and the second inverter circuit (INV2) comprise a thin film transistor.
6. Method for displaying a digital image signal on a display device comprising:
 - a display panel (100),
 - an image memory (2) outputting a digital image signal;
 - a plurality of pixel elements (200) disposed in the display panel (100);
 - a plurality of static memory circuits (110) disposed for corresponding pixel elements (200); and
 - a panel drive circuit (6) supplying a panel drive signal for controlling a timing of writing the digital image signal into the static memory circuits (110);

wherein an image is displayed based on the digital image signal retained in the static memory circuits (110),

characterized in that

the digital image signal is written into the static

memory circuits (110) from the image memory (2) by reducing a frequency of the panel drive signal without a use of a level-shifter for raising a level of the digital image signal.

7. Method for displaying a digital image signal on a display comprising a display panel,

- a display panel (100);
- an image memory (2) outputting a digital image signal;
- a DA converter (3) converting the digital image signal outputted from the image memory (2) into an analog image signal;
- a signal selection element (12) selecting the analog image signal from the DA converter (3) or the digital image signal outputted from the image memory (2), the selected signal being supplied to the display panel (100);
- a timing control circuit (6) supplying a panel drive signal to the display panel (100);
- a plurality of pixel elements (200) disposed in the display panel (100);
- a plurality of first display circuits disposed for corresponding pixel elements (200) and displaying an analog image in response to the analog image signal inputted based on the panel drive signal; and
- a plurality of second display circuits disposed for corresponding pixel elements and displaying a digital image in response to the digital image signal, each of the second display circuits having a static memory circuit (110) which receives the digital image signal based on the panel drive signal;

wherein the first display circuit or the second display circuit is selected for displaying the analog image or the digital image, respectively,

characterized in that

the timing control circuit (6) reduces a frequency of the panel drive signal so that the digital image signal is written into the static memory circuit (110) from the image memory (2) without a use of a level-shifter for raising a level of the digital image signal.

Fig.1

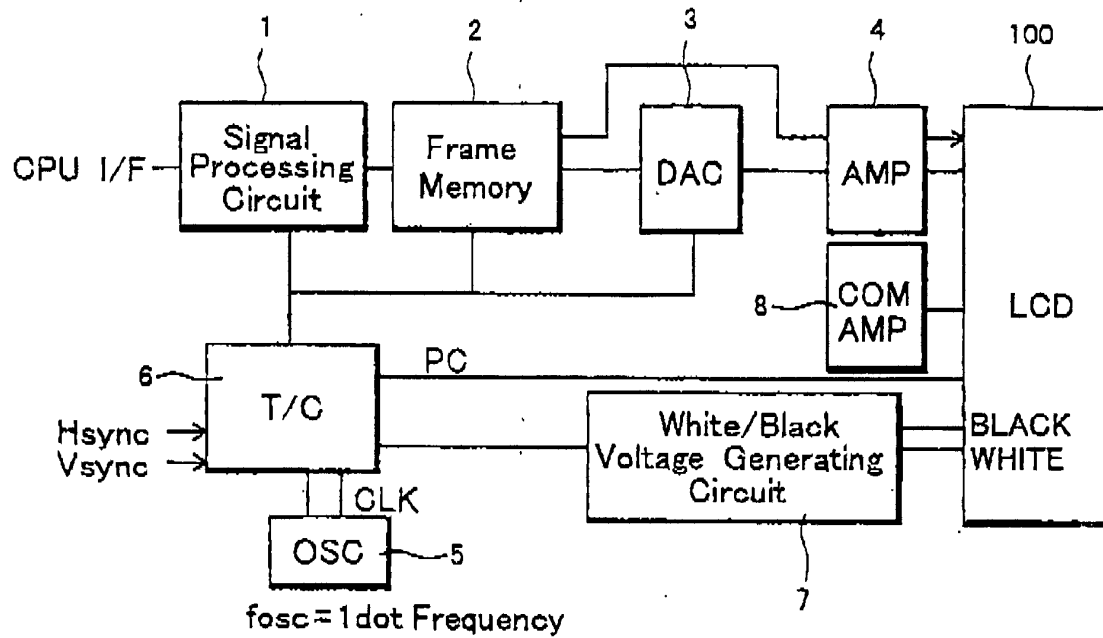


Fig.2

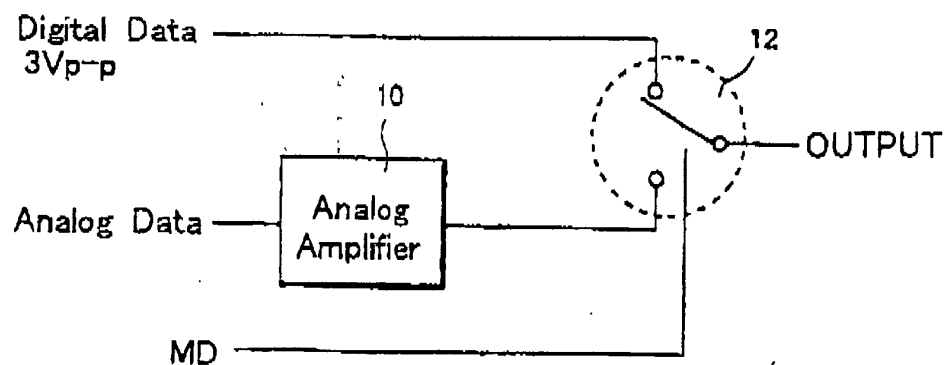


Fig.3

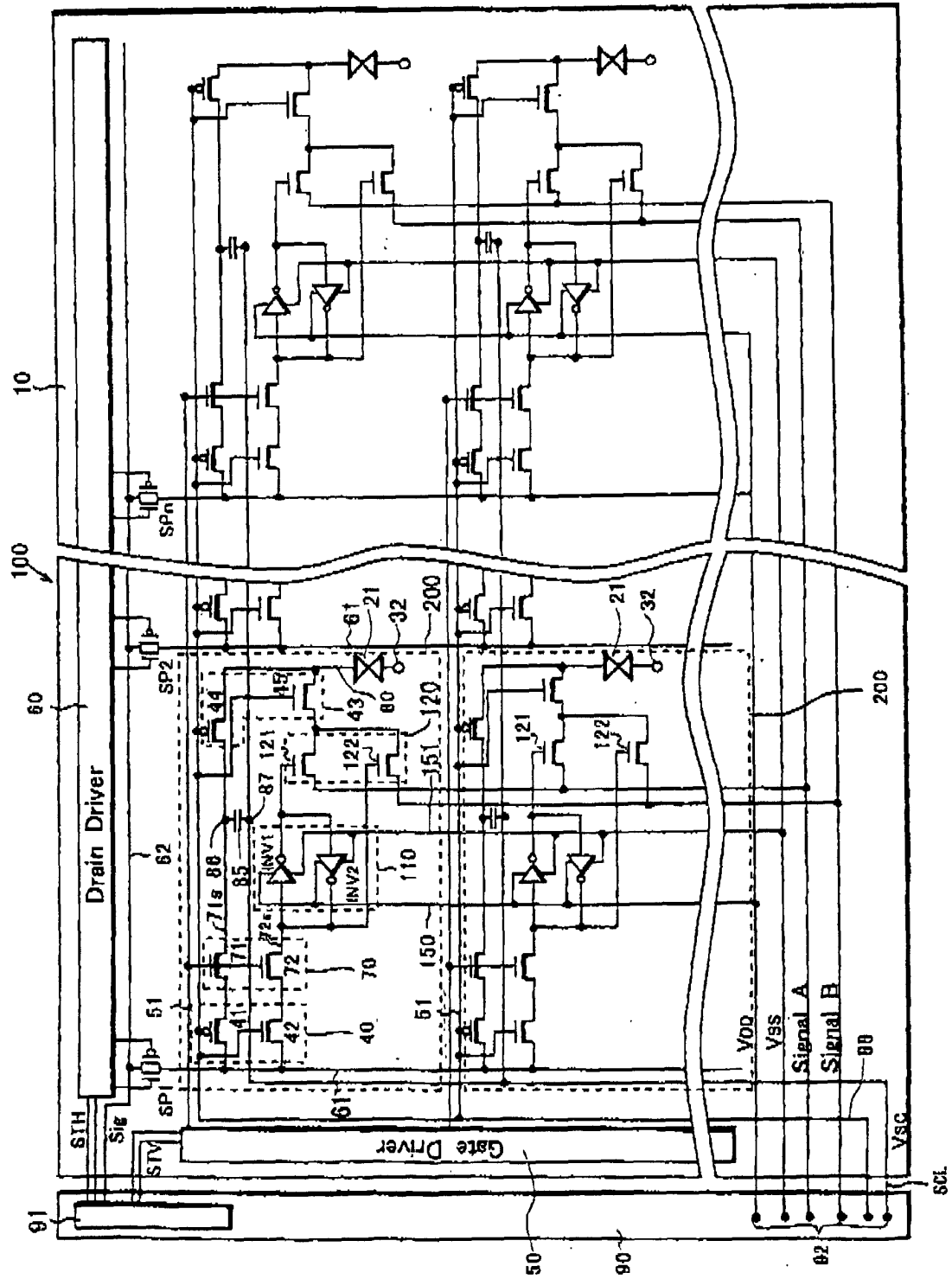


Fig.4

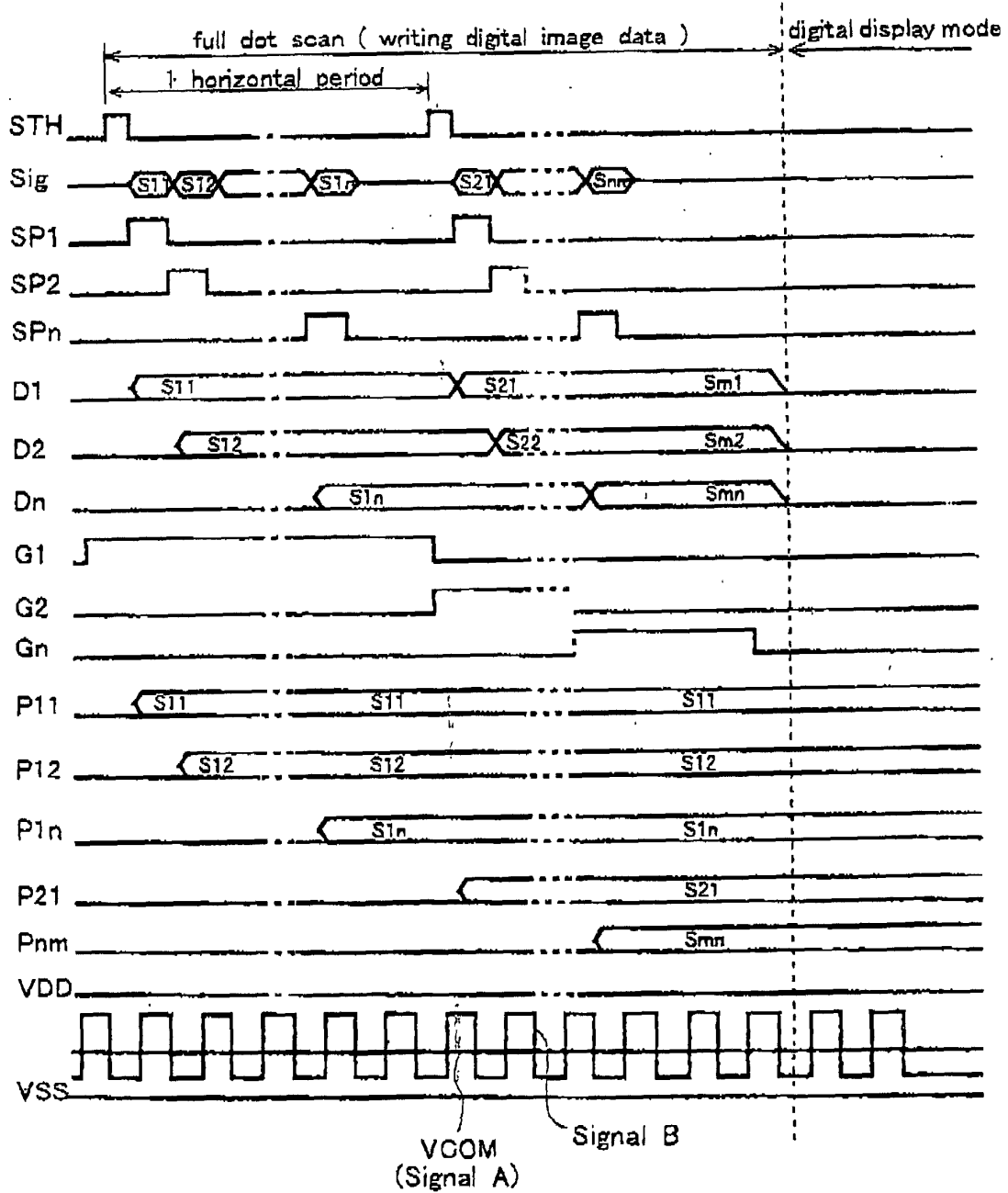


Fig.5

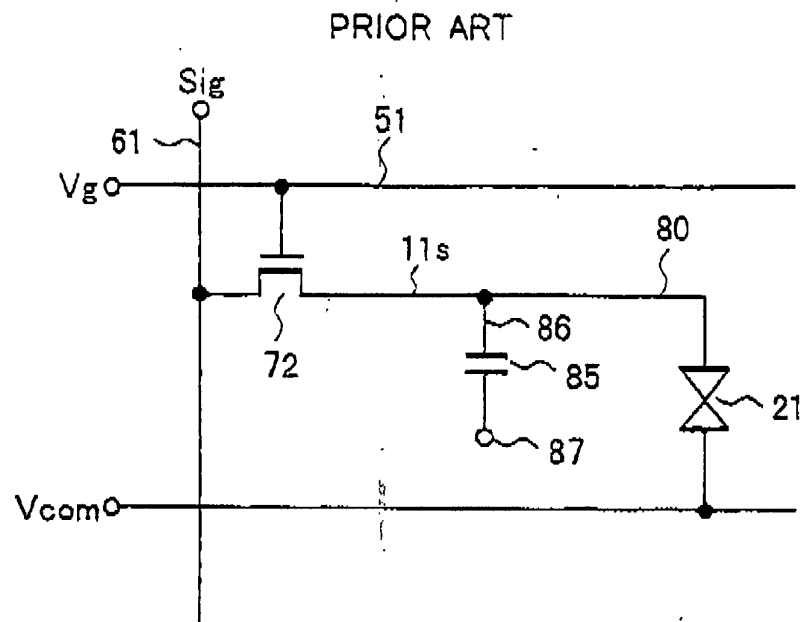


Fig.6

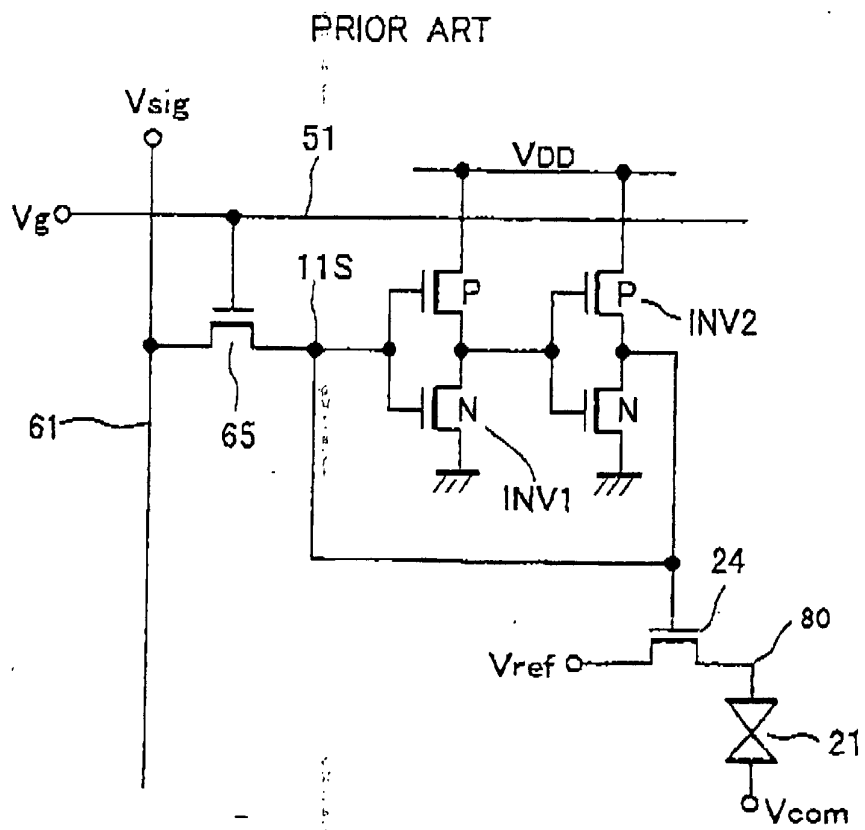
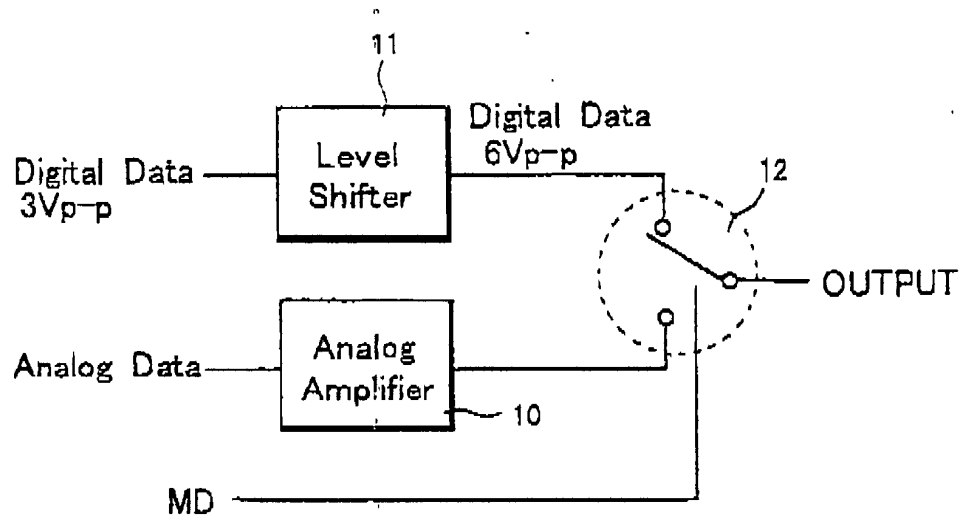


Fig.7



专利名称(译)	显示设备		
公开(公告)号	EP1249819A2	公开(公告)日	2002-10-16
申请号	EP2002008318	申请日	2002-04-11
[标]申请(专利权)人(译)	三洋电机株式会社		
申请(专利权)人(译)	SANYO ELECTRIC CO. , LTD.		
当前申请(专利权)人(译)	SANYO ELECTRIC CO. , LTD.		
[标]发明人	TSUTSUI YUSUKE		
发明人	TSUTSUI, YUSUKE		
IPC分类号	G02F1/133 G09F9/30 G09G3/20 G09G3/36		
CPC分类号	G09G3/3648 G09G2300/0842 G09G2300/0857 G09G2330/02		
优先权	2001112724 2001-04-11 JP		
其他公开文献	EP1249819A3		
外部链接	Espacenet		

摘要(译)

在数字显示模式下，显示装置执行将数字图像信号写入静态存储电路，同时将约3V的电源电压施加到静态存储器，其中面板驱动频率从60Hz降低到20-30Hz。因此，可以在不使用电平移位器的情况下将数字图像信号从帧存储器直接输出到液晶显示板。

Fig.3

