



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
10.08.2011 Bulletin 2011/32

(51) Int Cl.:
G09G 3/36 ^(2006.01)

(21) Application number: **10010671.5**

(22) Date of filing: **25.09.2010**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR
Designated Extension States:
BA ME RS

(72) Inventor: **Koo, Bon-Yong**
Asan-si
Chungcheongnam-do (KR)

(74) Representative: **Weitzel, Wolfgang**
Dr. Weitzel & Partner
Patent- und Rechtsanwälte
Friedenstrasse 10
89522 Heidenheim (DE)

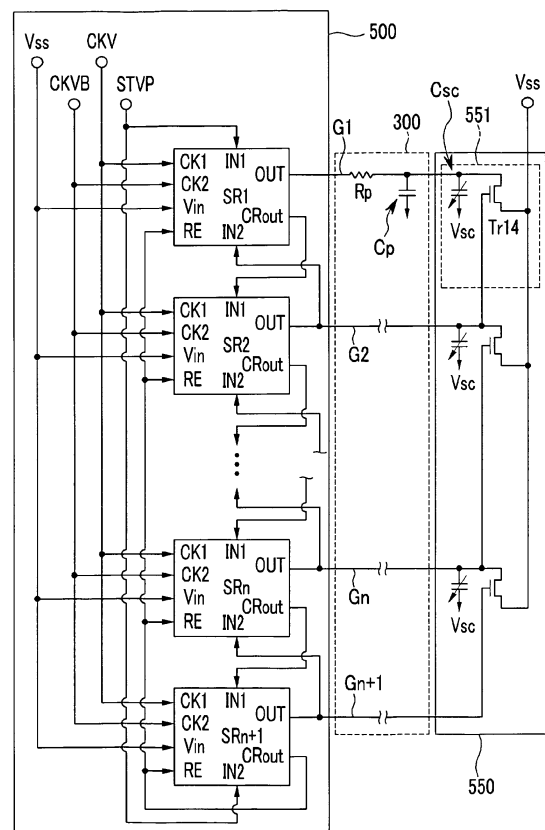
(30) Priority: **14.12.2009 KR 20090124219**

(71) Applicant: **Samsung Electronics Co., Ltd**
Yeongtong-gu
Suwon-city, Gyeonggi-do
442-742 (JP)

(54) **Scanning circuit for active matrix liquid crystal display**

(57) A display panel has an amorphous silicon gate driver. A scanning circuit (500) at one side of the display panel has attached thereto a gate line (G1-Gn+1) at the output of each stage (SR1-SRn+1). A variable capacitor (Vsc) is formed at the other end of the gate line to prevent the deterioration of display quality due to high temperature noise. A predetermined level of capacitance is provided to the variable capacitor to reduce ripple of gate voltage and eliminate the high temperature noise. Further included at the end of each gate line is a circuit for discharging charge to a low level, the discharging being controlled by the voltage applied to the next gate line.

FIG.2



Description

BACKGROUND

(a) Technical Field

[0001] The present disclosure relates to display panels and in particular, to a display panel that has a gate driver integrated in the display panel.

(b) Discussion of the Related Art

[0002] Among display panels, the liquid crystal display is one of the flat panel displays that are currently widely used and includes two display panels in which field generating electrodes, such as a pixel electrode and a common electrode, are formed with a liquid crystal layer disposed therebetween. The liquid crystal display has voltages applied to the field generating electrodes to generate an electric field in the liquid crystal layer, such that the direction of liquid crystal molecules of the liquid crystal layer is determined and polarization of incident light is controlled, thereby displaying images. Display panels also include organic light emitting devices, plasma display devices, and electrophoretic displays.

[0003] Each display device typically includes a gate driver and a data driver. The gate driver is typically patterned along with gate lines, data lines, and thin film transistors, to be able to be integrated on the panel. The integrated gate driver does not need a separate gate driving chip, thereby making it possible to reduce manufacturing costs. However, the characteristics of a semiconductor (in particular, an amorphous semiconductor) of thin film transistors implemented in integrated gate drivers can change as a function of temperature. As a result, the gate voltage output at high temperature does not have a predetermined waveform and thus, noise can occur.

SUMMARY

[0004] According to an exemplary embodiment a display panel has an amorphous silicon gate driver. A variable capacitor is formed at one end of a gate line to prevent the deterioration of display quality due to high temperature noise. A predetermined level of capacitance is provided to the variable capacitor to reduce the ripple of gate voltage and eliminate high temperature noise.

[0005] According to an exemplary embodiment of the present invention a display panel includes a display area that includes a gate line. A main gate driver integrated on a substrate is connected to one end of the gate line and applies a gate on voltage to the gate line.

[0006] The variable capacitor may be connected to an other end of the gate line

[0007] One end of the variable capacitor may be connected to the gate line and the other end thereof may be connected to receive voltage from the outside.

[0008] The variable capacitor may have capacitance

that varies according to the voltage applied to the other end of the variable capacitor.

[0009] When more than two variable capacitors are included, the variable capacitors may be connected in parallel.

[0010] The display area may further include a data line that intersects the gate line.

[0011] One electrode of the variable capacitor may be made of the same material as the gate line,

[0012] The other electrode of the variable capacitor may be made of the same material as the data line.

[0013] A gate insulating layer may cover the gate line and be between the one electrode of the variable capacitor and the other electrode of the variable capacitor.

[0014] The sub gate driver may further include a gate voltage discharge transistor that discharges the voltage applied to the gate line.

[0015] The gate voltage discharge transistor may further include a control electrode connected to a gate line of a next stage, an input electrode connected to a gate line of a current stage, and an output electrode connected to low voltage.

[0016] The main gate driver may include a thin film transistor of amorphous silicon.

[0017] The main gate driver may include an input unit, a pull-up driver, a transmit signal generator, an output unit, and a pull-down driver.

[0018] The input unit may be responsive to an input voltage and have an output connected to the transfer signal generator, to the pull-down driver and to the output unit.

[0019] The pull-up driver may be responsive to clock signals and have an output connected to the pull-down driver.

[0020] The transfer signal generator may be responsive to the clock signals and have an output connected to a next stage for outputting a transfer signal to the next stage.

[0021] The output unit may be connected to the gate line for providing a gate on voltage and a gate off voltage to the gate line.

[0022] The pull-down driver may be responsive to a gate voltage of the next stage for changing a gate on voltage output from the output unit to a gate off voltage.

[0023] According to an exemplary embodiment of the present invention, when noise occurs in the gate voltage at high temperature, the capacitance having a predetermined size may be provided to the variable capacitor such that the size of the capacitance in the gate line is increased and a ripple occurring in the gate voltage is reduced, thereby removing noise occurring at high temperature. However, one terminal of the variable capacitor may be floated to remove the capacitance provided in the variable capacitor, thereby making it possible to control the capacitance in the gate line as needed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024]

FIG. 1 is a plan view of a display panel according to an exemplary embodiment of the present invention.

FIG. 2 is a block diagram showing in more detail the gate driver and the gate lines shown in FIG. 1.

FIG. 3 is a circuit diagram showing one stage, one gate line, one variable capacitor, and one gate voltage discharge transistor of the exemplary embodiment shown in FIG. 2.

FIG. 4 is a graph showing gate voltage after and before a variable capacitor is added in the gate driver according to an exemplary embodiment of the present invention.

FIGs. 5, 6, 7 and 8 are diagrams showing in more detail the structure of a sub gate driver in the display panel according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0025] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

[0026] In the drawings, the thickness of layers, films, panels, regions, etc., may be exaggerated for clarity. Like reference numerals designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0027] FIG. 1 is a plan view of a display panel according to an exemplary embodiment of the present invention. A display panel 100 includes a display area 300 that displays images and a gate driver (including a main gate driver 500 and a sub gate driver 550) that applies gate voltages to the gate lines of the display area 300. The data lines of the display area 300 are applied with data voltages from a driver IC 460 that is formed on a flexible printed circuit film (FPC) 450 attached to the display panel 100. The gate drivers 500, 550 and the data driver IC 460 are controlled by a signal controller 600. A printed circuit board (PCB) 400 is formed at an outer side of the flexible printed circuit film 450 to transmit signals from the signal controller 600 to the data driver IC 460 and to the gate drivers 500, 550. The signal controller 600 provides a first clock signal CKV, a second clock signal CK-

VB, a scan starting signal STVP, and signals that provide specific voltages Vss, Vcst, Vsc.

[0028] The display area 300 of FIG. 1 for a representative liquid crystal panel includes a plurality of thin film transistors Trsw, liquid crystal capacitors Clc, and maintaining capacitors Cst. A representative organic light emitting panel includes a plurality of thin film transistors and organic light emitting diodes. Other representative display panels include elements such as a thin film transistors and the like, thereby forming the display area 300. Hereinafter, an exemplary embodiment for a liquid crystal panel implementation will be described in more detail.

[0029] The display area 300 includes a plurality of gate lines G1, ... Gn+1 and a plurality of data lines D1, ... Dm, wherein the plurality of gate lines G1, ... Gn+1 and the plurality of data line D1, ... Dm are isolated from, but intersect with, each other.

[0030] Each pixel PX includes the thin film transistor Trsw, the liquid crystal capacitor Clc, and the maintaining capacitor Cst. A control terminal of the thin film transistor Trsw is connected to one gate line. An input terminal of the thin film transistor Trsw is connected to one data line. An output terminal of the thin film transistor Trsw is connected to one terminal of the liquid crystal capacitor Clc and one terminal of the maintaining capacitor Cst. The other terminal of the liquid crystal capacitor Clc is connected to a common electrode and the other terminal of the maintaining capacitor Cst is applied with a maintaining voltage Vcst from the signal controller 600.

[0031] Data voltages from the data driver IC 460 are applied to the plurality of data lines D1, ... Dm and gate voltages from the gate drivers 500, 550 are applied to the plurality of gate lines G1, ... Gn+1.

[0032] The data driver IC 460 is formed on the upper and lower sides of the display panel 100 and is connected to the data lines D1, ... Dm that extend in a vertical direction and the exemplary embodiment of FIG. 1 shows the case where the data driver IC 460 is disposed at the lower side of the display panel 100.

[0033] The gate drivers 500, 550 include the main gate driver 500 that applies the gate voltage to the gate lines G1, ... Gn+1 and the sub gate driver 550 that provides additional storage capacitance to the gate lines G1, ... Gn+1 or discharges the applied gate voltage.

[0034] The main gate driver 500 receives clock signals CKV, CKVB, scan starting signal STVP, and the low voltage Vss to generate gate voltages (gate-on and gate-off voltages) and sequentially applies the gate-on voltage to the gate lines G1, ... Gn+1.

[0035] The sub gate driver 550 performs (through a gate voltage discharge transistor Tr14 shown in FIG. 2) the role of lowering the gate-on voltage, which is applied to a gate line of the current stage, to the low voltage Vss (the gate-off voltage) when the gate on voltage is applied to the gate on voltage of the next stage and provides additional capacitance through the variable capacitor Csc (shown in FIG. 2) to reduce the ripple in the gate voltage, thereby performing the role of removing noise

occurring at high temperature. The capacitance of the variable capacitor Csc can vary according the voltage value that is applied to one end of the variable capacitor Csc and one end can float, such that the variable capacitor would not perform the role as a capacitor.

[0036] The sub gate driver 550 is included in each pixel PX and is applied with the maintaining voltage Vcst that is applied to one end of the maintaining capacitor Cst to maintain the applied data voltage for one frame.

[0037] The clock signals CKV, CKVB, the scan starting signal STVP, and the voltage Vss (the gate-off voltage), and the maintaining voltage Vcst that are applied to the main gate driver 500 and the sub gate driver 550 are applied to each gate driver 500, 550 through two flexible printed circuit films 450 that is positioned at the outermost side of the display panel 100. The signal is transmitted to the flexible printed circuit films 450 through the printed circuit board 400 from the signal controller 600.

[0038] The gate drivers 500, 550 and the gate lines G1, ... Gn+1 will now be described in more detail.

[0039] FIG. 2 is a block diagram showing in more detail the gate driver 500, the sub gate driver 550 and the gate lines G1, ... Gn+1 shown in FIG. 1. The main gate driver 500 includes plurality of stages SR1, SR2, ... SRn, SRn+1 that are connected to each other in a cascade form. Each stage SR1, SR2, ... SRn, SRn+1 includes two input terminals IN1, IN2, two clock input terminals CK1, CK2, a voltage input terminal Vin that is applied with the low voltage Vss, a reset terminal RE, an output terminal OUT, and a transfer signal output terminal CRout.

[0040] The first input terminal IN1 is connected to the transfer signal output terminal CRout of a previous stage to receive the transfer signal CR of the previous stage. The first stage receives the scan starting signal STVP to a first input terminal IN1 since there is no previous stage.

[0041] The second input terminal IN2 is connected to the output terminal OUT of the next stage to receive the gate voltage of the next stage. Herein, in the case of an n+1-th stage SRn+1 (dummy stage) that is formed last, it is applied with the scan starting signal STVP to a second input terminal IN2 since there is no next stage.

[0042] The first clock terminals CK1 of odd numbered stages of the plurality of stages are applied with the first clock CKV and the second clock terminal CK2 is applied with the second clock CKVB having an inverted phase. The first clock terminal CK1 of even numbered stages is applied with the second clock CKVB and the second clock terminal CK2 thereof is applied with the first clock CKV, such that the phase of the clock input to the same terminal is opposite to each other, as compared with the odd numbered stage.

[0043] The voltage input terminal Vin is applied with the low voltage Vss as the gate-off voltage and the reset terminal (RE) is connected to the transfer signal output terminal CRout of the dummy stage SRn+1 that is positioned last.

[0044] The dummy stage SRn+1 is a stage that generates and outputs the dummy gate voltage unlike other

stages SR1, SR2, ... SRn. In other words, the gate voltages output from other stages SR1, SR2, ... SRn are transferred through the gate line and the data voltage is applied to the pixel to display the images. However, the dummy stage SRn+1, even though it is connected to a gate line, may be connected to the gate line of a dummy pixel (not shown) that does not display the images image, such that it is not used to display images.

[0045] The operation of the main gate driver 500 will now be described in more detail.

[0046] First, the first stage SR1 is applied with the first and second clock signals CKV, CKVB through the first clock input terminal CK1 and the second clock input terminal CK2 from the outside and the scan starting signal STVP through the first input terminal IN1. The voltage input terminal Vin is applied with the low voltage Vss for the gate-off voltage, and receives the gate voltage (voltage output from an out terminal) provided from the second stage SR2 through the second input terminal IN2, respectively, to output the gate voltage to the first gate line through the output terminal OUT. The transfer signal output terminal CRout outputs the transfer signal CR, which is transferred to the first input terminal IN1 of the second stage SR2.

[0047] The second stage SR2 is applied with the first and second clock signals CKV, CKVB provided through the first and second clock input terminals CK1, CK2 from the outside, respectively, and the transfer signal CR of the first stage SR1 through the first input terminal IN1. The voltage input terminal Vin is applied with the voltage Vss, and receives the gate voltage provided from the third stage SR3 through the second input terminal IN2, respectively, to output the gate voltage of the second gate line through the output terminal OUT. The transfer signal output terminal CRout outputs the transfer signal CR, which is transferred to the first input terminal IN1 of the third stage SR3.

[0048] In the above-mentioned manner, the n stage SRn is applied with the first and second clock signals CKV, CKVB provided from the outside through the first and second clock input terminals CK1, CK2, respectively, and the transfer signal CR of the n-1 stage SRn-1 through the first input terminal IN1. The voltage input terminal Vin is applied with the voltage Vss, and receives the gate voltage provided from the n-1 stage SRn-1 through the second input terminal IN2, respectively, to output the gate voltage of the n-th gate line through the output terminal OUT. The transfer signal output terminal CRout outputs the transfer signal CR, which is transferred to the first input terminal IN1 of the n+1 dummy stage SRn+1.

[0049] The sub gate driver 550 includes the unit sub gate driver 551 corresponding to one gate line of the gate lines G1, ... Gn+1.

[0050] One unit sub gate driver 551 includes at least one variable capacitor Csc and at least one gate voltage discharge transistor T14.

[0051] One-to-one correspondence may be shown to exist between the gate voltage discharge transistor T14

and one gate line and a plurality of variable capacitors Csc, or only one variable capacitor, may be formed in one gate line according to the size of the required capacitance. The exemplary embodiment of FIGs. 5 to 9 is formed with two variable capacitors Csc.

[0052] As seen in FIG. 3, one end of the variable capacitor Csc is connected to the gate line and the other end thereof is connected to the variable capacitor voltage Vsc that is applied to the variable capacitor Csc. The variable capacitor Csc may have the capacitance changed according to the variable capacitor voltage Vsc and when the variable capacitor Csc is unnecessary, the end of the variable capacitor is disconnected from a portion that applies the voltage Vsc to float the end of the variable capacitor Csc, thereby, in essence, removing the variable capacitor Csc.

[0053] The gate voltage discharge transistor Tr14 includes the input terminal that is connected to the gate line of the current stage, a control terminal that is connected to the gate line of the next stage, and an output terminal that is applied with the low voltage Vss. In other words, when the gate-on voltage is applied to the gate line of the next stage, the voltage that is applied to the gate line of the current stage is discharged, thereby having the Vss voltage value that is the low voltage. As a result, even after the gate-off voltage is applied, the charge remaining in the gate line is removed, thereby making it possible to prevent the malfunction of the thin film transistor Trsw.

[0054] The structure of the gate driver that is connected to one gate line will be described in more detail with reference to FIG. 3 which is a circuit diagram showing one stage (SR), one gate line, and one unit sub gate driver 551 of FIG 2.

[0055] First, the structure of one stage SR will be described.

[0056] Referring to FIG. 3, each stage SR of the main gate driver 500 according to the present exemplary embodiment includes an input unit 510, a pull-up driver 511, a transfer signal generator 512, an output unit 513, and a pull-down driver 514.

[0057] The input unit 510 includes fourth transistor Tr4. The input terminal and control terminal of the fourth transistor Tr4 is commonly connected (diode-connected) to the first input terminal IN1, and the output terminal is connected to a Q contact. When the input unit 510 applies the high voltage to the first input terminal IN1, the input unit 510 performs a role of transferring the high voltage to the Q contact.

[0058] The pull-up driver 511 includes seventh transistor Tr7, twelfth transistor Tr12, second capacitor C2, and third capacitor C3. The input electrode is commonly connected to the control electrode of the twelfth transistor Tr12 such that it receives the first clock signal CKV or the second clock signal CKVB through the first clock terminal CK1 and the output electrode is connected to the pull-down driver 514. The input electrode of the seventh transistor Tr7 receives the first clock signal CKV or the

second clock signal CKVB through the first clock terminal CK1. The control terminal and the output terminal of the seventh transistor Tr7 is connected to the pull-down driver 514. The second capacitor C2 is connected between the input electrode and the control electrode of the seventh transistor Tr7 and the third capacitor C3 is connected between the control electrode and the output electrode of the seventh transistor Tr7.

[0059] The transfer signal generator 512 includes fifteenth transistor Tr15 and fourth capacitor C4. The input electrode of the fifteenth transistor Tr15 receives the first clock signal CKV or the second clock signal CKVB through the first clock terminal CK1 and the control electrode is connected to the output of the input unit 510. That is, the Q contact and the control electrode and the output electrode are connected to the fourth capacitor C4. The transfer signal generator 512 outputs the transfer signal CR according to the voltage at the Q contact and the first clock signal CKV.

[0060] The output unit 513 includes first transistor Tr1 and first capacitor C1. The control electrode of the first transistor Tr1 is connected to the Q contact. The input electrode receives the first clock signal CKV or the second clock signal CKVB through the first clock terminal CK1. The control electrode and the output electrode are connected to the first capacitor C1 and the output terminal is connected to the gate line. The output unit 513 outputs the gate voltage according to the voltage at the Q contact and the first clock signal CKV.

[0061] The pull-down driver 514 removes the charge existing on the stage SR to smoothly output the gate-off voltage Q, thereby lowering the potential of the gate line contact and lowering the voltage output to the gate line. The pull-down driver 514 includes second transistor Tr2, third transistor Tr3, fifth transistor Tr5, sixth transistor Tr6, eighth transistor Tr8, ninth transistor Tr9, tenth transistor Tr10, eleventh transistor Tr11, and thirteenth transistor Tr13.

[0062] The fifth transistor Tr5, the tenth transistor Tr10, and the eleventh transistor Tr11 are coupled in series between the first input terminal IN1 that is applied with the transfer signal CR of the previous stage SR and the voltage input terminal Vin that is applied with the low voltage Vss. The control terminals of the fifth and eleventh transistor Tr5, Tr11 receive the second clock signal CKVB or the first clock signal CKV through the second clock terminal CK2. The control terminal of the tenth transistor Tr10 receives the first clock signal CKV or the second clock signal CKVB through the first clock terminal CK1. In addition, the Q contact is connected between the eleventh transistor Tr11 and the tenth transistor Tr10 and the output terminal of the first transistor Tr1 of the output unit 513. That is, the gate line is connected between the tenth transistor Tr10 and the fifth transistor Tr5.

[0063] A pair of transistors Tr6, Tr9 are coupled in parallel between the Q contact and the low voltage Vss. The control terminal of the sixth transistor Tr6 receives the transfer signal CR of the dummy stage through the reset

terminal RE and the control terminal of the ninth transistor Tr9 receives the gate voltage of the next stage through the second input terminal IN2.

[0064] A pair of transistors Tr8, Tr13 are connected between the outputs of two transistors Tr7, Tr12 and the low potential level Vss, respectively. The control terminals of the eighth and the thirteenth transistor Tr8, Tr13 are commonly connected to the output terminal of the first transistor Tr1 of the output unit 513, that is, the gate line.

[0065] Finally, the pair of transistors Tr2, Tr3 are coupled in parallel between the output of the output unit 513 and the low potential level Vss. The control terminal of the third transistor Tr3 is connected to the output terminal of the seventh transistor Tr7 of the seventh transistor Tr7. The control terminal of the second transistor Tr2 receives the gate voltage of the next stage through the second input terminal IN2.

[0066] When the pull-down driver 514 receives the gate voltage of the next stage through the second input terminal IN2, it changes the voltage of the Q contact to the low voltage Vss through the ninth transistor Tr9 and change the voltage output to the gate line through the second transistor Tr2 to the low voltage Vss. In addition, when the transfer signal CR is applied with the transfer signal CR of the dummy stage through the reset terminal RE, the voltage of the Q contact is changed to the low voltage Vss through the sixth transistor Tr6 once more. When the high voltage is applied to the second clock terminal CK2 to which voltage having a phase opposite to the first clock terminal CK1, the voltage output to the gate line through the fifth transistor Tr5 is changed to the low voltage Vss.

[0067] As described with regard to FIG. 2, each stage of the main gate driver 500 receives the first and second clock signals CKV, CKVB and the first and second clock terminals CK1, CK2 are alternately input to the first and second clock signals CKV, CKVB for each stage.

[0068] The transistors Tr1, ... Tr13, Tr15 that are formed in the stage SR may be NMOS transistors.

[0069] The gate voltage output from the stage SR is transferred through the gate line. The gate line may be represented as having the resistance Rp and the capacitance Cp in a circuit, as shown in FIGs 2 and 3. These values are included in one gate line but one gate line may have different values according to the structure and characteristics of the display area 300.

[0070] The gate line that is extended passing through the display area 300 is connected to the sub gate driver 550 and is connected to the unit sub gate driver 551 in the sub gate driver 550.

[0071] The unit sub gate driver 551 includes at least one variable capacitor Cs and the gate voltage discharge transistor Tr14.

[0072] The variable capacitor Csc is connected to the capacitance Cp included in the gate line in parallel to increase the capacitance included in the gate line. As a result, the ripple of the gate voltage is reduced, thereby

making it possible to prevent noise from generating in the gate voltage. This can be confirmed in Experimental Example described below in conjunction with FIG. 4.

[0073] In the gate voltage discharge transistor Tr14 the extending line of the gate line is connected to the input terminal. The extending line of the gate line of the next stage is connected to the control terminal. The output terminal is connected to the low voltage Vss. As a result, when the gate-on voltage is applied to the gate line of the next stage, the gate voltage discharge transistor Tr14 is turned on to discharge the charge existing in the gate line of the current stage, thereby having the low voltage.

[0074] The waveform of the output gate voltage after and before the variable capacitor Csc is used will now be described with reference to FIGs. 4A and 4B which depict graphs showing gate voltage after and before a variable capacitor Csc is added in the gate driver according to an exemplary embodiment of the present invention. More particularly, FIG. 4A shows the case where the variable capacitor Csc does not serve as the capacitor by floating (F) one end of the variable capacitor Csc and shows the case of generating noise while the gate voltage of the main gate driver 500 is operated at the high temperature. FIG. 4B shows the case of operating the main gate driver 500 at high temperature after the entire capacitance value is included in the gate line so that the variable capacitor Csc has the capacitance by applying the predetermined voltage to one end of the variable capacitor Csc. As can be appreciated in FIG. 4B, the ripple of the gate voltage is reduced while increasing the capacitance included in the gate line. As a result, noise does not occur in the gate voltage output from the main gate driver 500 even though the main gate driver 500 is operated at high temperature. In the present exemplary embodiment, the capacitance of the added variable capacitor Csc is 20pF, but the exemplary embodiment forms the variable capacitor Csc of about 10 to 50pF, thereby making it possible to remove the occurrence of noise.

[0075] As can be appreciated in FIG. 4B, the variable capacitor Csc is added to the rear end of the gate line, thereby making it possible to remove the high temperature noise of the main gate driver 500. The variable capacitor Csc is not necessarily positioned at the rear end of the gate line, but the exemplary embodiment of the present invention shows the case where it is positioned at the rear end of the gate line. This is based upon the fact that the main gate driver 500 is formed at the front end of the gate line to limit the space in which the variable capacitor Csc will be formed. However, according to an exemplary embodiment, when the sufficient space in which the variable capacitor Csc will be formed is secured at the front end of the gate line, the variable capacitor Csc is not necessarily formed at the rear end of the gate line.

[0076] FIGs. 5 to 8 are diagrams showing in detail the structure of a sub gate driver in the display panel accord-

ing to an exemplary embodiment of the present invention.

[0077] FIG. 5 is a layout view showing a display panel based upon the structure of the sub gate driver 550 according to an exemplary embodiment of the present invention. FIG. 6 is a layout view showing wiring that is formed on the same layer as the gate line in the sub gate driver 550 according to the exemplary embodiment of FIG. 5. FIG. 7 is a diagram showing wiring formed on the same layer as the data line of the exemplary embodiment of FIG. 5. FIG. 8 is a cross-sectional view taken along the line VIII-VIII of FIG. 7.

[0078] As shown in FIGs. 5 to 7, the sub gate driver 550 includes the variable capacitor Csc, the gate voltage discharge transistor Tr14, wiring 175-1 that applies the low voltage Vss to the output terminal of the gate voltage discharge transistor Tr14, and wirings 131, 131-1 that apply the maintaining voltage Vcst to the maintaining capacitor Cst.

[0079] Referring first to FIG. 5, the right side (outer side) of the sub gate driver 550 is positioned with a region A printed with identification marks and a region B formed with a dummy pattern. The position of the wiring can be easily found in region A by eyesight and as an example of the dummy pattern of region B, there is a cell gap maintaining pattern, dot pattern, or the like.

[0080] The structure of the sub gate driver 550 according to an exemplary embodiment of the present invention will now be described in more detail with reference to FIGs. 6 to 8, wherein FIG. 6 shows sub gate driver 550 formed on the same layer as the gate line and FIGs. 7 and 8 show sub gate driver 550 formed on the same layer as the data line.

[0081] The sub gate driver 550 is extended from the gate line 121 and has two extended variable capacitor electrodes 125, 125-1 and includes the first extending region 122 formed to contact the upper wiring. The second extending region 123 is also formed to connect to the first extending region 122 of the next stage. The second extending region 123 is extended through the extending line 124-1 that protrudes in the extending direction of the gate line. The gate electrode 124 of the gate voltage discharge transistor Tr14 is formed while one end of the extending line 124-1 gate electrode 124 is extended.

[0082] The sub gate driver 550 is also formed with a storage electrode line 131 that applies voltage to the one end of the maintaining capacitor Cst and the storage electrode line 131 is extended to be bent according to the outer side of the variable capacitor electrodes 125, 125-1. In addition, the sub gate driver 550 is formed with a shorting bar 131-1 to be electrically connected to the storage electrode line 131.

[0083] A gate insulating layer 140 is formed on the gate line 121, the variable capacitor electrodes 125, 125-1, the first and second extending regions 122, 123, and the gate electrode 124 of the gate voltage discharge transistor Tr14. In particular, a semiconductor layer 150 that forms the channel of the gate voltage discharge transistor

Tr14 is formed on the gate insulating layer 140 that is formed on the gate electrode 124 of the gate voltage discharge transistor Tr14.

[0084] Electrodes 172, 172-1 of the other end of the variable capacitor are formed on the gate insulating layer 140 to overlap with each of the variable capacitor electrodes 125, 125-1 while extending in the vertical direction to the extending direction of the gate line in the same layer as the data line gate insulating layer 140. The variable capacitor electrodes 125, 125-1, the electrodes 172, 172-1 of the other end of the variable capacitor, and the gate insulating layer 140 therebetween each form the two variable capacitors Csc. When voltage is applied to the electrodes 172, 172-1 of the other end of the variable capacitor, the variable capacitor Csc has the capacitance and when the electrodes 172, 172-1 of the other end of the variable capacitor is floated, the variable capacitor Csc is not operated as the capacitor.

[0085] The first extending region 122 of the next stage and the second extending region 123 of the current end are connected to a connecting member 179. As a result, the gate-on voltage of the next stage is applied to the gate electrode 124 of the gate voltage discharge transistor Tr14 of the previous stage.

[0086] A source electrode having a plurality of grooves and a drain electrode 175 having a plurality of protruding portions are formed on the gate electrode 124 of the gate voltage discharge transistor Tr14 and on the semiconductor layer 150. The source electrode 173 is electrically connected to the connecting member 179 through the extending line 173-1 protruding from the connecting member of the current end. The drain electrode 175 is extended and is connected to the wiring 175-1 that applies the low voltage Vss. As a result, when the gate-on voltage is applied to the gate line of the next stage, the gate voltage discharge transistor Tr14 of the current end is turned on to discharge voltage from the source electrode 173 to the drain electrode 175, such that the gate line 121 has the low voltage Vss.

[0087] In the exemplary embodiment of FIGs. 6 to 8, the drain electrode 175 is configured to have the protruding portion, but in an exemplary embodiment of the present invention, the source electrode 173 can have the protruding portion.

[0088] While the present invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but is intended to also cover various modifications and equivalent arrangements, all of which are included within the spirit and scope of the appended claims.

Claims

1. A display panel, comprising:

a display area that includes a gate line;

- a main gate driver that is connected to one end of the gate line, that applies a gate on voltage to the gate line, and is integrated on a substrate; and
a sub gate driver that is connected to an other end of the gate line and includes at least one variable capacitor. 5
2. The display panel of claim 1, wherein the variable capacitor is connected to the other end of the gate line. 10
3. The display panel of claim 2, wherein one end of the variable capacitor is connected to the gate line and an other end of the variable capacitor receives voltage from the outside. 15
4. The display panel of claim 3, wherein the variable capacitor has a capacitance that varies according to the voltage applied to the other end of the variable capacitor. 20
5. The display panel of claim 4, wherein the display panel includes more than two variable capacitors connected in parallel. 25
6. The display panel of claim 4, wherein:
the display area further comprises a data line that intersects the gate line,
one electrode of the variable capacitor is made of the same material as the gate line,
the other electrode of the variable capacitor is made of the same material as the data line, and
a gate insulating layer covers the gate line and is between the one electrode of the variable capacitor and the other electrode of the variable capacitor. 30
7. The display panel of claim 6, wherein the sub gate driver further comprises a gate voltage discharge transistor that discharges the voltage applied to the gate line. 35
8. The display panel of claim 7, wherein the gate voltage discharge transistor comprises:
a control electrode that is connected to a gate line of a next stage,
an input electrode that is connected to a gate line of a current stage, and
an output electrode that is connected to low voltage. 40
9. The display panel of claim 8, wherein: 45
the main gate driver includes an input unit, a pull-up driver, a transmit signal generator, an output unit, and a pull-down driver;
the input unit is responsive to an input voltage and has an output connected to the transfer signal generator, to the pull-down driver and to the output unit;
the pull-up driver is responsive to clock signals and has an output connected to the pull-down driver;
the transfer signal generator is responsive to the clock signals and has an output connected to a next stage for outputting a transfer signal to the next stage;
the output unit is connected to the gate line for providing a gate on voltage and a gate off voltage to the gate line; and
the pull-down driver is responsive to a gate voltage of the next stage for changing a gate on voltage output from the output unit to a gate off voltage. 50
10. The display panel of claim 1, wherein one end of the variable capacitor is connected to the gate line and an other end of the variable capacitor receives voltage from the outside. 55
11. The display panel of claim 1, wherein the display panel includes more than two variable capacitors connected in parallel.
12. The display panel of claim 1, wherein:
the display area further comprises a data line that intersects the gate line,
one electrode of the variable capacitor is made of the same material as the gate line,
the other electrode of the variable capacitor is made of the same material as the data line, and
a gate insulating layer that covers the gate line and is between the one electrode of the variable capacitor and the other electrode of the variable capacitor. 60
13. The display panel of claim 1, wherein the sub gate driver includes a gate voltage discharge transistor that discharges the voltage applied to the gate line.
14. The display panel of claim 1, wherein the main gate driver includes a thin film transistor comprising amorphous silicon.
15. The display panel of claim 1, wherein:
the main gate driver includes an input unit, a pull-up driver, a transmit signal generator, an output unit, and a pull-down driver;
the input unit is responsive to an input voltage and has an output connected to the transfer signal generator, to the pull-down driver and to the output unit;
the pull-up driver is responsive to clock signals and has an output connected to the pull-down driver;
the transfer signal generator is responsive to the clock signals and has an output connected to a next stage for outputting a transfer signal to the next stage;
the output unit is connected to the gate line for providing a gate on voltage and a gate off voltage to the gate line; and
the pull-down driver is responsive to a gate voltage of the next stage for changing a gate on voltage output from the output unit to a gate off voltage. 65

output unit;
the pull-up driver is responsive to clock signals
and has an output connected to the pull-down
driver;
the transfer signal generator is responsive to the 5
clock signals and has an output connected to a
next stage for outputting a transfer signal to the
next stage;
the output unit is connected to the gate line for
providing a gate on voltage and a gate off voltage 10
to the gate line; and
the pull-down driver is responsive to a gate volt-
age of the next stage for changing a gate on
voltage output from the output unit to a gate off
voltage. 15

20

25

30

35

40

45

50

55

FIG.1

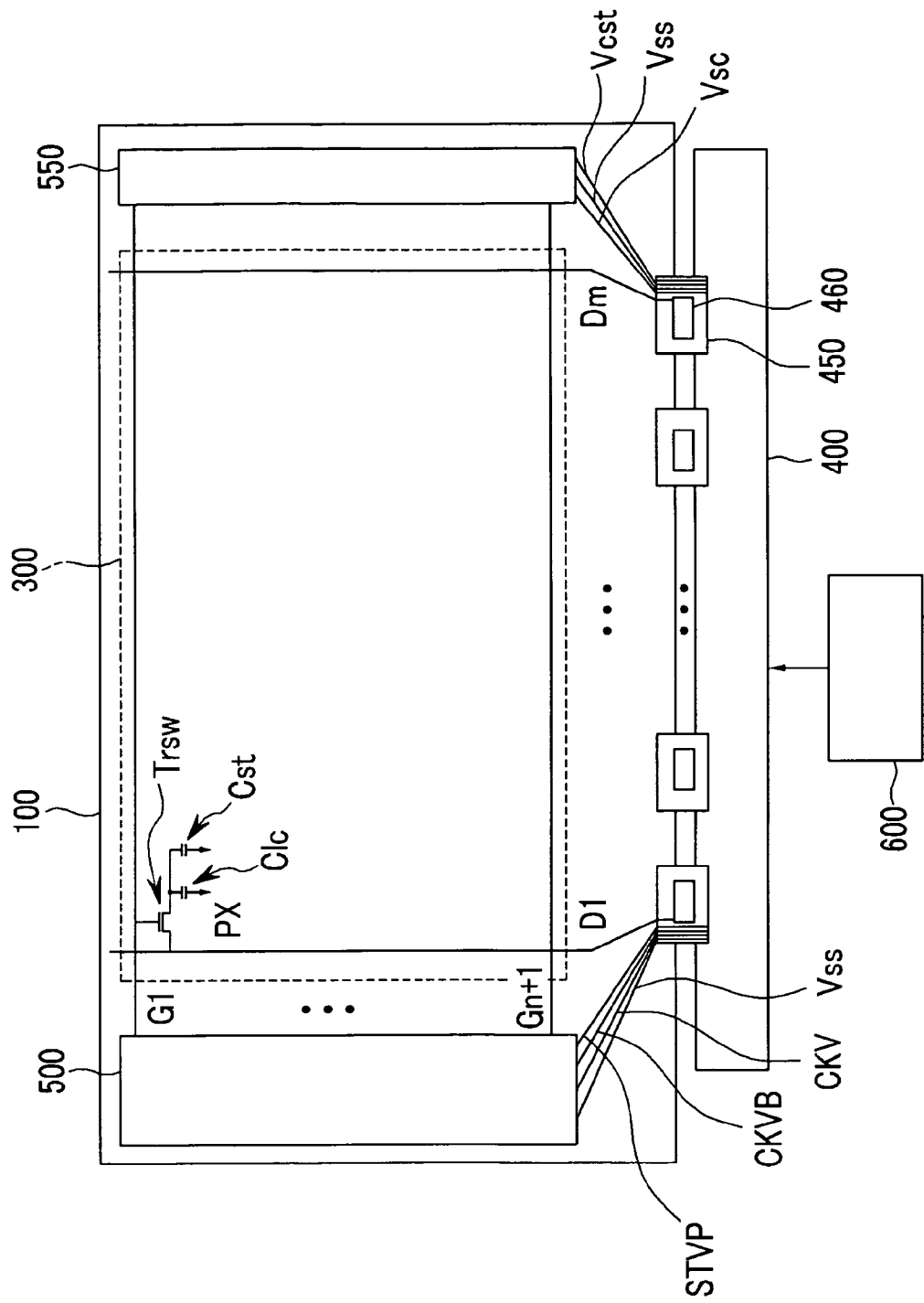


FIG.2

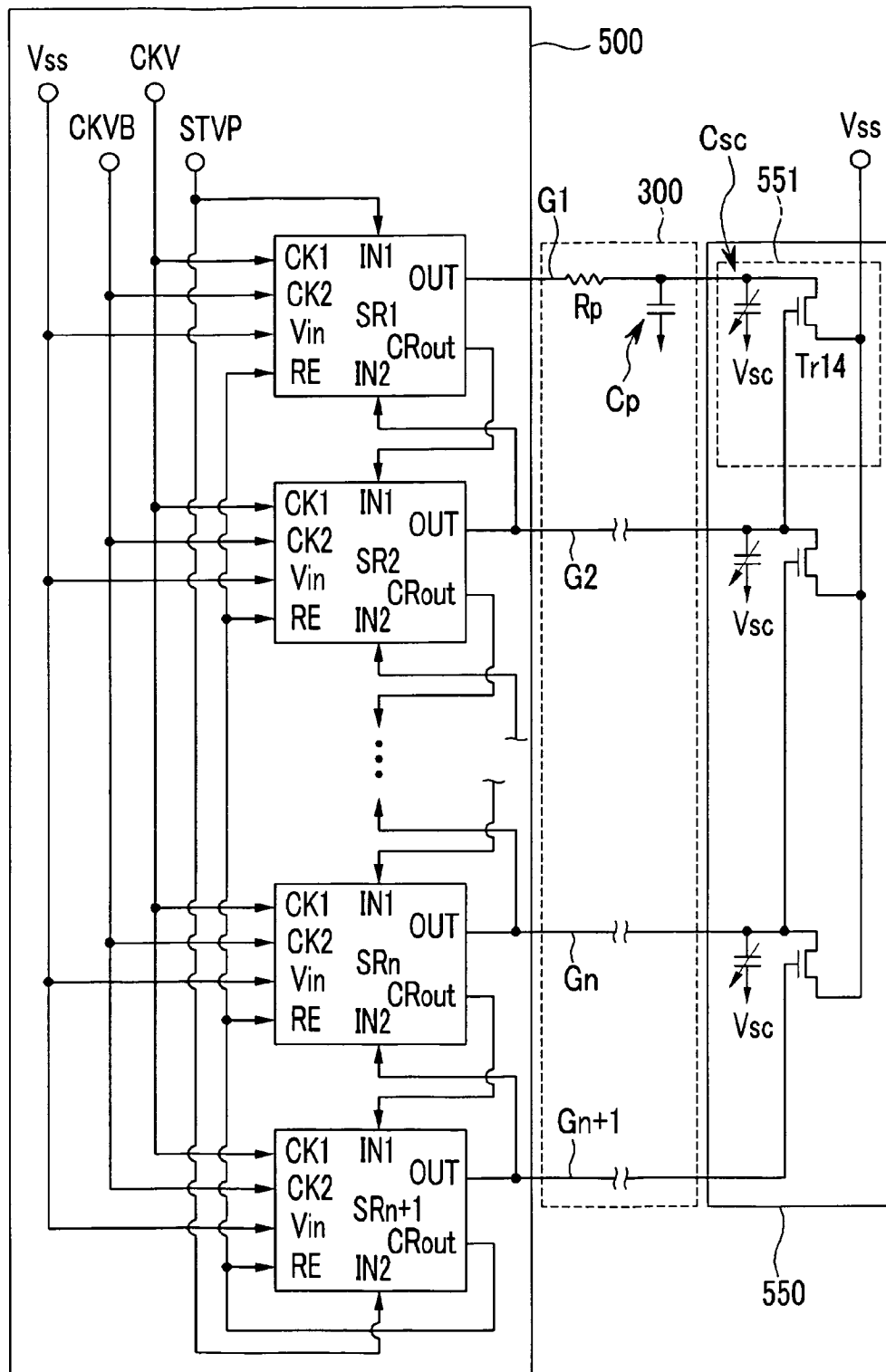


FIG.3

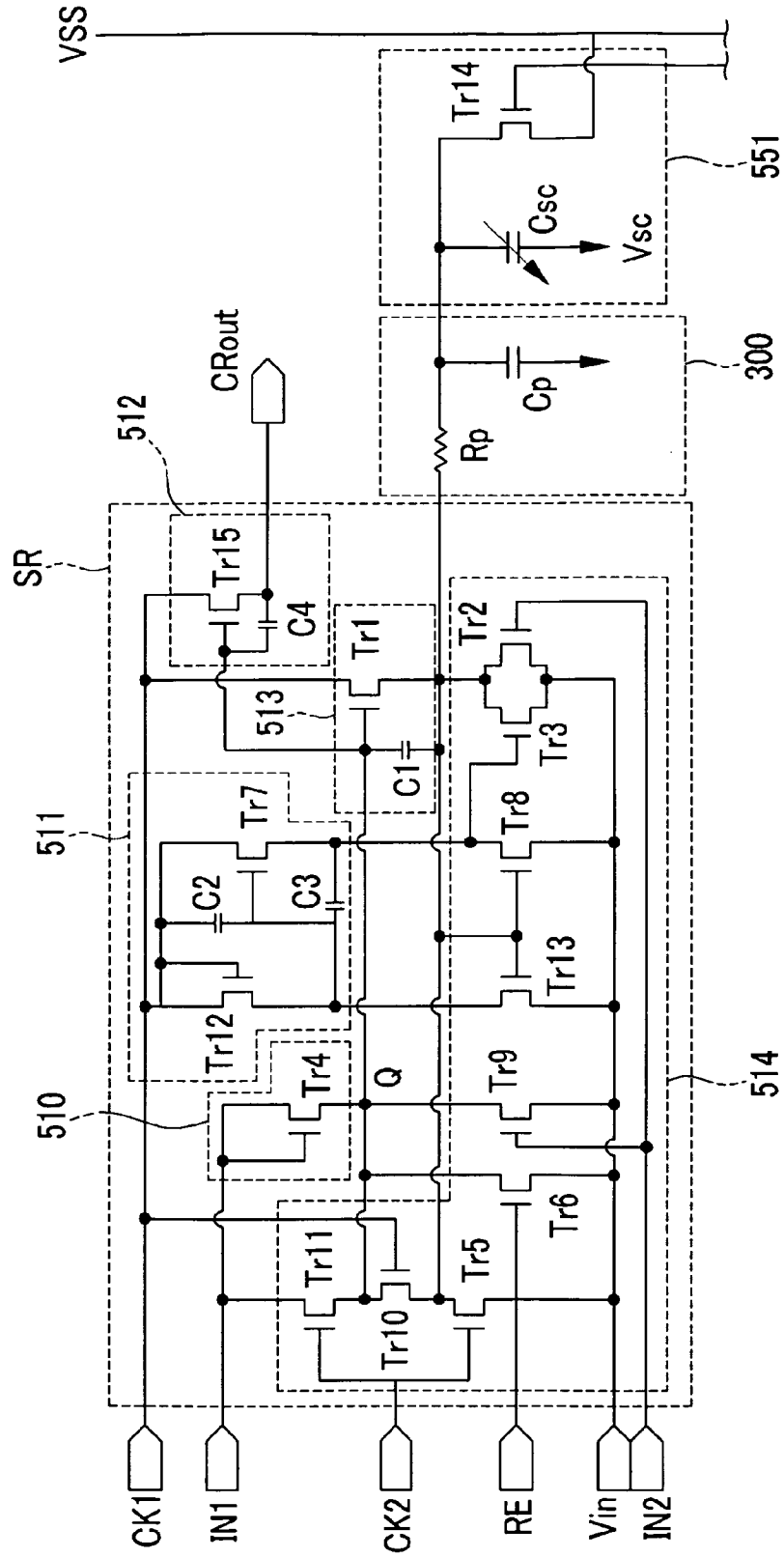


FIG.4A

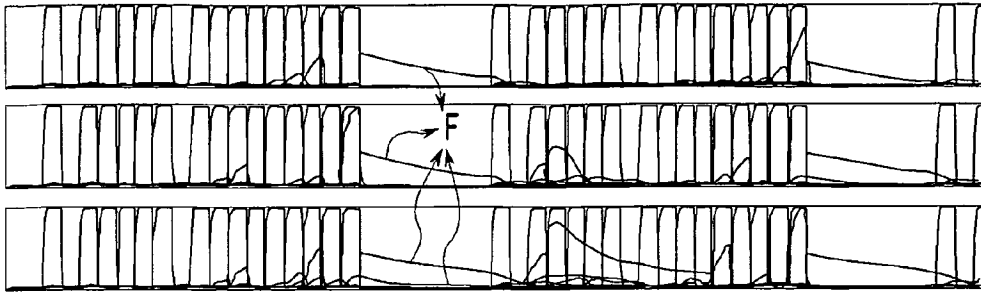


FIG.4B

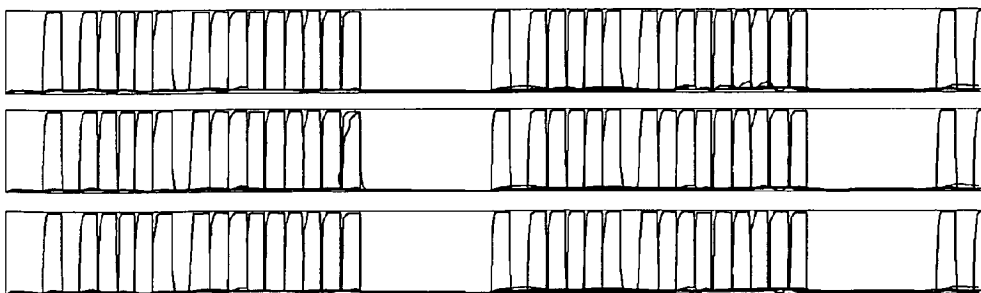


FIG. 5

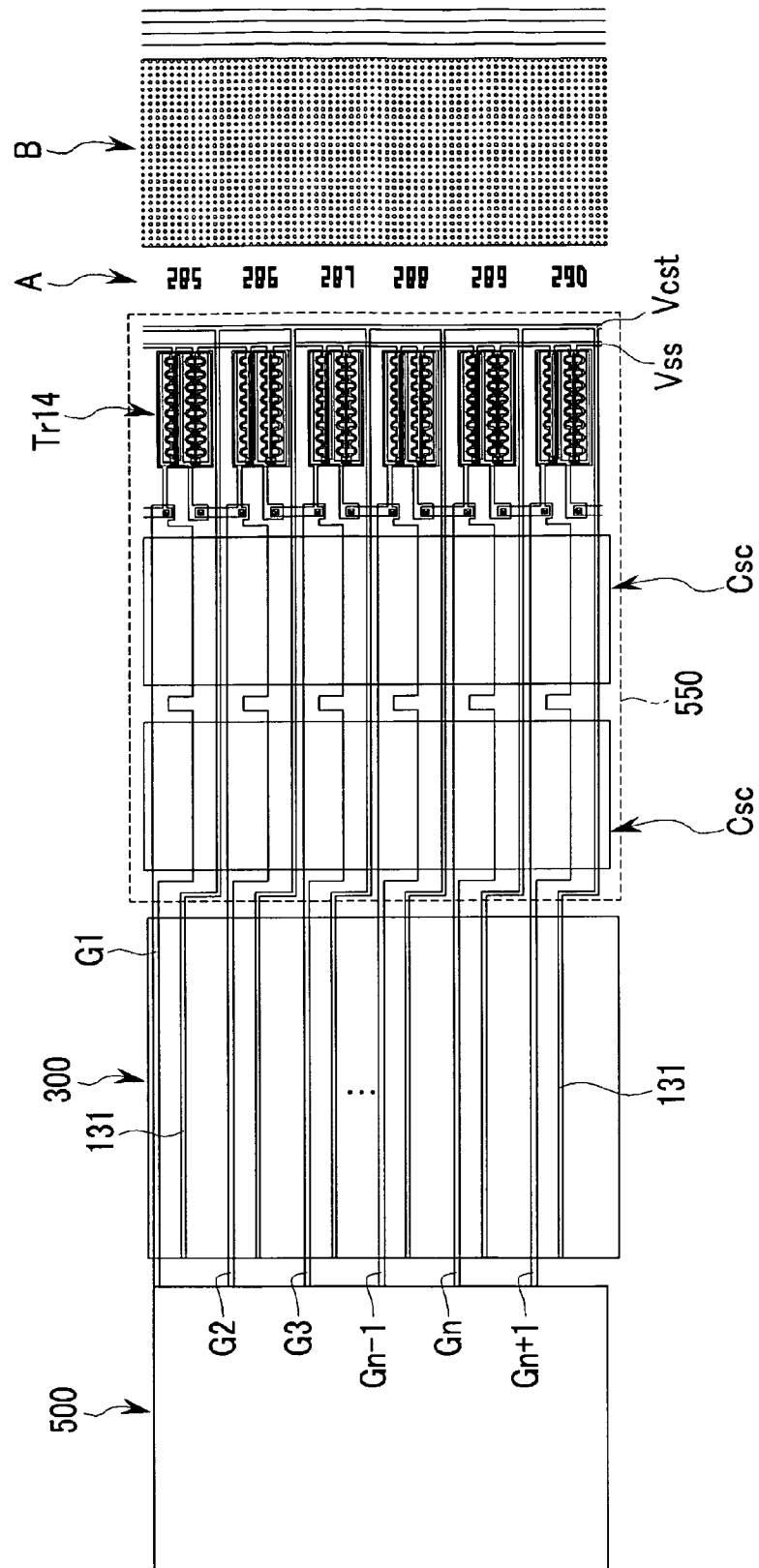


FIG.6

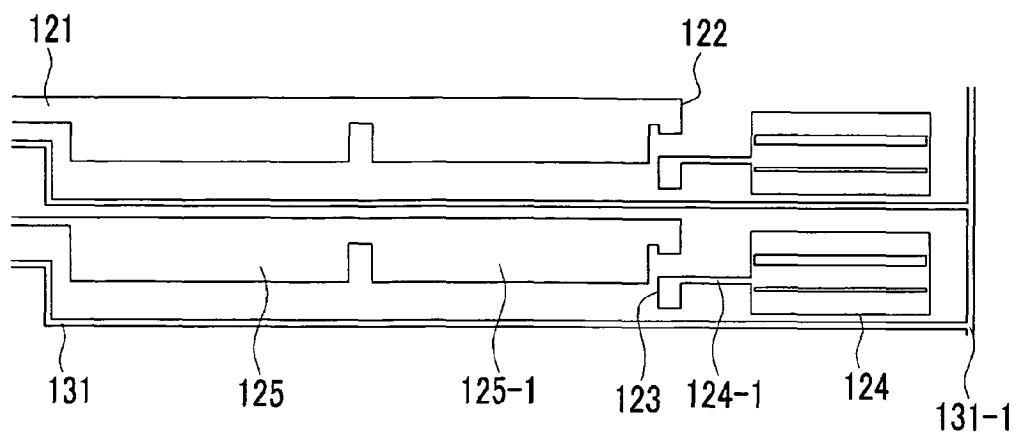


FIG.7

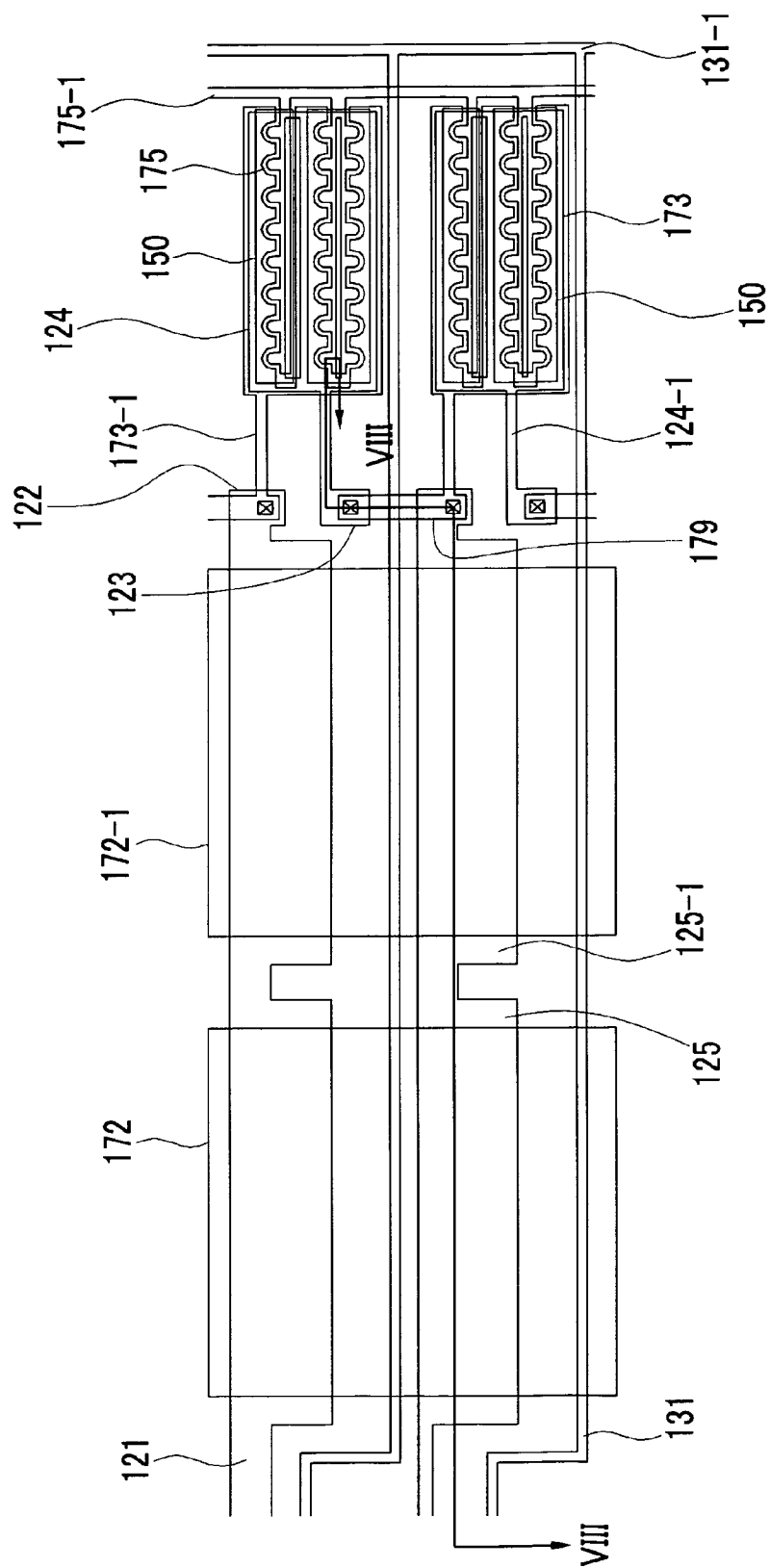
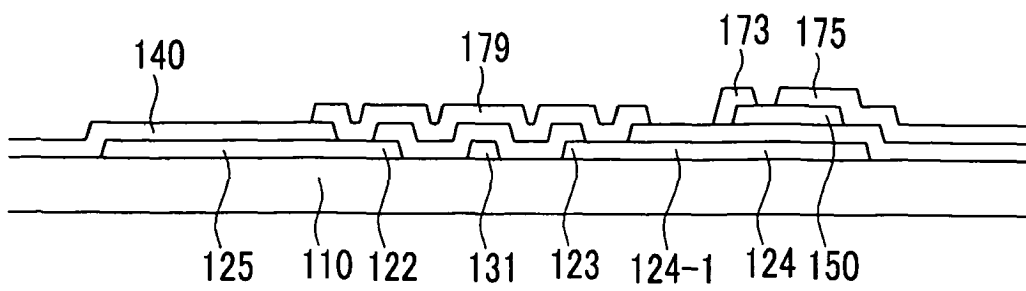


FIG.8





EUROPEAN SEARCH REPORT

Application Number
EP 10 01 0671

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 5 909 262 A (TOMOOKA TAKATOSHI [JP] ET AL) 1 June 1999 (1999-06-01)	1-6, 10-12	INV. G09G3/36
Y	* column 3, line 65 - column 5, line 55; figures 5-7 *	7-9, 13-15	
Y	----- US 2008/100560 A1 (NA BYOUNG-SUN [KR] ET AL) 1 May 2008 (2008-05-01) * paragraph [0049] - paragraph [0077]; figures 2, 3 *	7-9, 13-15	
X	----- US 2003/169242 A1 (NAKANISHI HAYATO [JP]) 11 September 2003 (2003-09-11) * paragraph [0056] - paragraph [0058]; figures 3,4 * * paragraph [0074] - paragraph [0080]; figures 3,4 *	1-15	TECHNICAL FIELDS SEARCHED (IPC) G09G
Y	----- US 2006/104152 A1 (MARTIN ERIC T [US] ET AL) 18 May 2006 (2006-05-18) * paragraph [0009] - paragraph [0018]; figures 1-3 *	1-15	
Y	----- US 2008/136756 A1 (YEO JANG-HYUN [KR] ET AL) 12 June 2008 (2008-06-12) * paragraph [0093] - paragraph [0110]; figures 5, 6 *	1-15	
A	----- GB 2 341 714 A (LG PHILIPS LCD CO LTD [KR]) 22 March 2000 (2000-03-22) * page 2, line 14 - page 3, line 30; figures 1, 2 * * page 10, line 5 - page 14, line 9; figures 6-8 * * page 20, line 1 - page 25, line 21; figures 18-20 * ----- -/--	1-15	
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 9 March 2011	Examiner Morris, David
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

 1
EPO FORM 1503 03/82 (P04C01)



EUROPEAN SEARCH REPORT

Application Number
EP 10 01 0671

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	US 2004/119675 A1 (WASHIO HAJIME [JP] ET AL) 24 June 2004 (2004-06-24) * paragraph [0067] - paragraph [0078]; figures 8,9 * -----	1-15	
			TECHNICAL FIELDS SEARCHED (IPC)
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 9 March 2011	Examiner Morris, David
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

1
EPO FORM 1503 03.82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 10 01 0671

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

09-03-2011

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5909262 A	01-06-1999	JP 3224730 B2 JP 9211424 A	05-11-2001 15-08-1997
US 2008100560 A1	01-05-2008	CN 101174070 A EP 1918938 A2 KR 20080039026 A	07-05-2008 07-05-2008 07-05-2008
US 2003169242 A1	11-09-2003	CN 1434667 A JP 3818261 B2 JP 2003288986 A TW 587400 B	06-08-2003 06-09-2006 10-10-2003 11-05-2004
US 2006104152 A1	18-05-2006	NONE	
US 2008136756 A1	12-06-2008	CN 101202024 A JP 2008165223 A KR 20080053598 A	18-06-2008 17-07-2008 16-06-2008
GB 2341714 A	22-03-2000	DE 19944724 A1 FR 2783629 A1 JP 4259691 B2 JP 2000137247 A JP 2007304613 A KR 20000022668 A	03-08-2000 24-03-2000 30-04-2009 16-05-2000 22-11-2007 25-04-2000
US 2004119675 A1	24-06-2004	CN 1506926 A JP 3666662 B2 JP 2004191888 A KR 20040052194 A TW 256030 B	23-06-2004 29-06-2005 08-07-2004 22-06-2004 01-06-2006

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	用于有源矩阵液晶显示器的扫描电路		
公开(公告)号	EP2355083A1	公开(公告)日	2011-08-10
申请号	EP2010010671	申请日	2010-09-25
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	三星电子有限公司		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	KOO BON YONG		
发明人	KOO, BON-YONG		
IPC分类号	G09G3/36		
CPC分类号	G09G3/3677 G09G3/3648 G09G2300/0408 G09G2300/0417 G09G2300/0426 G09G2300/043 G09G2320/0223 G09G2320/041		
代理机构(译)	韦策尔, WOLFGANG		
优先权	1020090124219 2009-12-14 KR		
其他公开文献	EP2355083B1 EP2355083B8		
外部链接	Espacenet		

摘要(译)

显示面板具有非晶硅栅极驱动器。在显示面板一侧的扫描电路 (500) 在每级 ($SR1-SR_{n+1}$) 的输出端连接有栅极线 ($G1-G_{n+1}$) 。在栅极线的另一端形成可变电容器 (V_{sc}) , 以防止由于高温噪声导致的显示质量的劣化。向可变电容器提供预定水平的电容, 以减小栅极电压的纹波并消除高温噪声。在每条栅极线的末端还包括用于将电荷放电到低电平的电路, 该放电由施加到下一栅极线的电压控制。

FIG. 2

