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(54) **Method and apparatus for driving a liquid crystal display device**

Verfahren und Vorrichtung zur Ansteuerung einer Flüssigkristallanzeige

Procédé et appareil de contrôle d'un dispositif d'affichage à cristaux liquides

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Description**FIELD OF THE INVENTION**

5 [0001] The present invention relates generally to a liquid crystal display (LCD), and more particularly, to a low-power-consumption source driver for an LCD and methods of driving the same.

BACKGROUND OF THE INVENTION

10 [0002] Liquid crystal display (LCD) is commonly used as a display device because of its capability of displaying images with good quality while using little power. An LCD apparatus includes an LCD panel formed with liquid crystal cells and pixel elements with each associating with a corresponding liquid crystal cell and having a liquid crystal capacitor and a storage capacitor, a thin film transistor (TFT) electrically coupled with the liquid crystal capacitor and the storage capacitor. These pixel elements are substantially arranged in the form of a matrix having a number of pixel rows and a number of pixel columns. Typically, scanning signals, generated from a gate driver, are sequentially applied to the number of pixel rows, through a plurality of scanning lines along the row direction, for sequentially turning on the pixel elements row-by-row. When a scanning signal is applied to a pixel row to turn on corresponding TFTs of the pixel elements of a pixel row, source signals of an image to be displayed, generated from a source driver, for the pixel row are simultaneously applied to the number of pixel columns, through a plurality of data lines arranged crossing over the plurality of scanning lines along the column direction, so as to charge the corresponding liquid crystal capacitor and storage capacitor of the pixel row for aligning orientations of the corresponding liquid crystal cells associated with the pixel row to control light transmittance therethrough. By repeating the procedure for all pixel rows, all pixel elements are supplied with corresponding source signals of the image signal, thereby displaying the image signal thereon.

15 [0003] Liquid crystal molecules have a definite orientational alignment as a result of their long, thin shapes. The orientations of liquid crystal molecules in liquid crystal cells of an LCD panel play a crucial role in the transmittance of light therethrough. It is known if a substantially high voltage is applied between the liquid crystal layer for a long period of time, the optical transmission characteristics of the liquid crystal molecules may change. This change may be permanent, causing an irreversible degradation in the display quality of the LCD panel. To prevent the LC molecules from being deteriorated, the polarity of the voltage signals applied on the LC cell has to be changed continuously. Usually, a source driver is configured to generate such voltage signals having their polarity alternated according to an inversion scheme such as frame inversion, row inversion, column inversion, or dot inversion. Typically, one or more portions of the source driver are classified into the positive and negative types. The driving voltages for the positive and negative driver circuits are the same. However, the range of operational voltage is twice larger than that of the driver circuit with the single polarity. As a consequence, the power consumption of the source driver increases substantially. Additionally, notwithstanding the inversion schemes, a higher image quality requires higher power consumption because of frequent polarity conversions. Such LCD devices, in particular thin film transistor (TFT) LCD devices, may consume significant amounts of power, which may in turn generate excessive heat. The characteristics of the LCD devices will be significantly deteriorated due to the heat generated.

25 [0004] Therefore, a heretofore unaddressed need exists in the art to address the aforementioned deficiencies and inadequacies.

30 [0005] US 2008/0211703 A1 discloses a liquid crystal display having a data driver that performs dot inversion driving. The data driver comprises a positive polarity path and a negative polarity path each comprising a reference voltage generation circuit, a polarity decoder and a polarity amplifier and both path are connected to an output switch circuit.

SUMMARY OF THE INVENTION

35 [0006] The present invention provides a source driver with the features of claim 1. Further embodiments are subject-matter of the dependent claims.

40 [0007] These and other aspects of the present invention will become apparent from the following description of the preferred embodiment taken in conjunction with the following drawings, although variations and modifications therein may be affected without departing from the scope of the novel concepts of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

45 [0008] The accompanying drawings illustrate one or more embodiments of the invention and, together with the written description, serve to explain the principles of the invention. Wherever possible, the same reference numbers are used throughout the drawings to refer to the same or like elements of an embodiment, and wherein:

Fig. 1 shows schematically a block diagram of a source driver according to one embodiment of the present invention; Fig. 2 shows schematically a block diagram of a source driver according to another embodiment of the present invention, where $POL = 0$;

Fig. 3 shows schematically the block diagram of the source driver as shown in Fig. 2, where $POL = 1$;

Fig. 4 shows schematically configurations of a source driver: (a) a conventionally full voltage driving configuration, (b) an half voltage driving configuration with the first middle voltage $VM1 = (VDD/2 - \Delta V)$ and the second middle voltage $VM2 = (VDD/2 + \Delta V)$ according to one embodiment of the present invention, and (c) an half voltage driving configuration with the first middle voltage $VM1 = VDD/2$, and the second middle voltage $VM2 = VDD/2$ according to another embodiment of the present invention;

Fig. 5 shows exemplary results of the power consumptions and operation temperatures of an LCD module under a conventionally full voltage driving configuration and the half voltage driving configuration according to embodiment of the present invention;

Fig. 6 shows deviations of the operation voltages of a conventional source driver (a) and (b), and of the source driver according to one embodiment of the present invention (c) and (d); and

Fig. 7 shows experimental results of the RMS deviations of a conventional source driver (a) and of the source driver according to one embodiment of the present invention (b).

DETAILED DESCRIPTION OF THE INVENTION

[0009] The present invention is more particularly described in the following examples that are intended as illustrative only since numerous modifications and variations therein will be apparent to those skilled in the art. Various embodiments of the invention are now described in detail. Referring to the drawings, like numbers indicate like components throughout the views. As used in the description herein and throughout the claims that follow, the meaning of "a", "an", and "the" includes plural reference unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

[0010] The terms used in this specification generally have their ordinary meanings in the art, within the context of the invention, and in the specific context where each term is used. Certain terms that are used to describe the invention are discussed below, or elsewhere in the specification, to provide additional guidance to the practitioner regarding the description of the invention. The use of examples anywhere in this specification, including examples of any terms discussed herein, is illustrative only, and in no way limits the scope and meaning of the invention or of any exemplified term. Likewise, the invention is not limited to various embodiments given in this specification.

[0011] As used herein, the terms "comprising," "including," "having," "containing," "involving," and the like are to be understood to be open-ended, i.e., to mean including but not limited to.

[0012] The description will be made as to the embodiments of the present invention in conjunction with the accompanying drawings of Figs. 1-7. In accordance with the purposes of this invention, as embodied and broadly described herein, this invention, in one aspect, relates to a source driver for driving a display having a plurality of pixels spatially arranged in a matrix form, and a plurality of data lines, where each data line is associated with pixels of a corresponding pixel column.

[0013] Referring to Fig. 1, a source driver 100 is shown according to one embodiment of the present invention. The source driver 100 includes a first level shifter 110 and a second level shifter 115 for receiving digital image data and shifting a voltage level of the digital image data, a first digital-to-analog converter with a positive polarity (PDAC) 120 and a second first digital-to-analog converter with a negative polarity (NDAC) 125 for converting the level-shifted digital image data into analog signals, a first analog circuit 130 and a second analog circuit 135 for comparing and amplifying the analog signals, and a first output stage 140 with a positive polarity and a second output stage 145 with a negative polarity for outputting the amplified analog signals with desired polarities to the plurality of data lines so as to drive the plurality of pixels.

[0014] According to the present invention, the PDAC 120 and the NDAC 125 electrically coupled to the first analog circuit 130 and the second analog circuit 135 through a first pair of switches, S11 and S12; the first analog circuit 130 and the second analog circuit 135 electrically coupled to the first output stage 140 and the second output stage 145 through a second pair of switches, S21 and S22; and the first output stage 140 and the second output stage 145 electrically coupled to odd data lines and even data lines through a third pair of switches, S31 and S32, respectively. The first pair of switches, S11 and S12, the second pair of switches, S21 and S22, and the third pair of switches, S31 and S32, are controlled by a control signal, POL, having a low state (e.g., $POL = 0$) and a high state (e.g., $POL = 1$).

[0015] As shown in Fig. 1, the first level shifter 110 has a first input for receiving a digital input data of an image to be displayed, a second input for receiving a power supply voltage, VDD, a third input for receiving a first middle voltage, VM1, and an output for outputting a first level-shifted signal of the input data to the PDAC 120. Similarly, the second level shifter 115 has a first input for receiving the input data, a second input for receiving a second middle voltage, VM2, a third input for receiving a ground voltage, GND, and an output for outputting a second level-shifted signal of the input

data to the NDAC 125.

[0016] Each of the first middle voltage VM1 and the second middle voltage VM2 is less than the power supply voltage VDD and greater than the ground voltage GND, where GND is usually set to 0V. The first middle voltage VM1 and the second middle voltage VM2 are identical to or different from each other. Further, each of the first middle voltage VM1 and the second middle voltage VM2 is equal to or less than a half of the power supply voltage VDD. The power supply voltage, VDD, the first middle voltage VM1 and the second middle voltage VM2 are provided by one or more power supplies. According to one embodiment of the present invention, the middle voltages are set as follows: If the middle voltages are supplied from a single power source, i.e., if the first middle voltage VM1 and the second middle voltage VM2 are the same, the first middle voltage and the second middle voltage VM1 = VM2 can be set as VDD/2. When there are two or more power sources, i.e., when VM1 ≠ VM2, the first middle voltage level VM1 is set to larger than the ground voltage GND and smaller than or equal to VDD/2, and the second middle voltage VM2 is larger than or equal to VDD/2 and is smaller than the power supply voltage VDD.

[0017] The PDAC 120 has a first input electrically coupled to the output of the first level shifter 110 for receiving the first level-shifted signal therefrom, a second input for receiving the power supply voltage VDD, a third input for receiving the first middle voltage VM1, a fourth input for receiving a Gamma voltage, and an output for outputting a first converted signal having a positive polarity. The NDAC 125 has a first input electrically coupled to the output of the second level shifter 115 for receiving the second level-shifted signal therefrom, a second input for receiving the second middle voltage VM2, a third input for receiving the ground voltage GND, a fourth input for receiving the Gamma voltage, and an output for outputting a second converted signal having a negative polarity. The Gamma voltage is adapted for Gamma correction of the display, and provided by a Gamma voltage generator or the like. The first converted signal output from the PDAC 120 and the second converted signal output from the NDAC 125 are analog data corresponding to the digital input data of the image to be displayed. Each of the first and second converted signals is output to the first analog circuit 130 or the second analog circuit 135, depending upon the control signal POL. For example, if POL = 0, the first converted signal is provided to the first analog circuit 130, and the second converted signal is provided to the second analog circuit 135. However, if POL = 1, the first converted signal is provided to the second analog circuit 135, while the second converted signal is provided to the first analog circuit 130.

[0018] The first analog circuit 130 has a first input electrically coupled to the output of the PDAC 120 and the output of the NDAC 125 through a switch S11 of the first pair of switches S11 and S12 for receiving the first converted signal from the PDAC 120 or the second converted signal from the NDAC 125, a second input for receiving the power supply voltage VDD, a third input for receiving the ground voltage GND, and an output for outputting a first amplified signal. The second analog circuit 135 has a first input electrically coupled to the output of the PDAC 120 and the output of the NDAC 125 through a switch S12 of the first pair of switches S11 and S12 for receiving the first converted signal from the PDAC 120 or the second converted signal from the NDAC 125, a second input for receiving the power supply voltage VDD, a third input for receiving the ground voltage GND, and an output for outputting a second amplified signal. Each of the first and second amplified signals is provided to the first output stage 140 or the second output stage 145, depending upon the control signal POL. For example, if POL = 0, the first amplified signal is provided to the first output stage 140, and the second amplified signal is provided to the second output stage 145. However, if POL = 1, the first amplified signal is provided to the second output stage 145, and the second amplified signal is provided to the first output stage 140.

[0019] The first analog circuit and the second analog circuit are identical to or different from each other. Preferably, the first analog circuit and the second analog circuit are identical.

[0020] The first output stage 140 with a positive polarity has a first input electrically coupled to the output of the first analog circuit 130 and the output of the second analog circuit 135 through a switch S21 of the second pair of switches S21 and S22 for receiving the first amplified signal from the first analog circuit 130 or the second amplified signal from the second analog circuit 135, a second input for receiving the power supply voltage VDD, a third input for receiving the first middle voltage VM1, and an output for outputting a first data signal. The second output stage 145 with a negative polarity having a first input electrically coupled to the output of the first analog circuit 130 and the output of the second analog circuit 135 through a switch S22 of the second pair of switches S21 and S22 for receiving the first amplified signal from the first analog circuit 130 or the second amplified signal from the second analog circuit 135, a second input for receiving the second middle voltage VM2, a third input for receiving the ground voltage GND, and an output for outputting a second data signal. The first and second data signals have positive and negative polarities, respectively.

[0021] Additionally, the output of the first output stage 140 and the output of the second output stage 145 are electrically coupled to odd data lines and even data lines through a switch S31 of the third pair of switches S31 and S32 that is controlled by the control signal POL. If POL = 0, the first data signal is provided to the odd data lines, while the second data signal is provided to the even data lines. If POL = 1, the first data signal is provided to the even data lines, while the second data signal is provided to the odd data lines. In other words, when the control signal POL is in the low state, each odd data line of the plurality of data line receives the first data signal having the positive polarity, while each even data line of the plurality of data line receives the second data signal having the negative polarity. When the control signal POL is in the high state, each odd data line of the plurality of data line receives the second data signal having the negative

polarity, while each even data line of the plurality of data line receives the first data signal having the positive polarity.

[0022] According to the present invention, as described above, the power source for all the first level shifter 110, the PDAC 120, and the first output stage 140 is between the power supply voltage level VDD and the first middle voltage level VM1, and the power source for all the second level shifter 115, the NDAC 125 and the second output stage 145 between the second middle voltage level VM2 and the ground voltage GND. That is, the amplitude variations of the operational voltages for the first level shifter 110, the PDAC 120, and the first output stage 140 is about (VDD - VM1), and for the second level shifter 115, the NDAC 125 and the second output stage 145 is about (VM2 - GND), which are much less than the amplitude variations of the conventionally operational voltages, (VDD - GND). As discussed below, for a driving configuration, the power consumption of the display and the temperature of the display panel could be reduced substantially.

[0023] Figs. 2 and 3 show a source driver 200 according to another embodiment of the present invention. The source driver 200 includes a first digital-to-analog converter with a positive polarity (PDAC) 220 having an output for outputting a first converted signal having a positive polarity, a second digital-to-analog converter with a negative polarity (NDAC) 225 having an output for outputting a second converted signal having a negative polarity, a first amplifying circuit 230, a first output stage 240, a second amplifying circuit 235 and a second output stage 245.

[0024] The first amplifying circuit 230 has a first input electrically coupled to the output of the PDAC 220 and the output of the NDAC 225 through a switch S11 of the first pair of switches S11 and S12 for receiving the first converted signal from the PDAC 220 or the second converted signal from the NDAC 225, a second input for receiving the power supply voltage VDD, a third input for receiving the ground voltage GND, and an output for outputting a first amplified signal. The first output stage 240 has a first input, a second input for receiving the power supply voltage VDD, a third input for receiving the first middle voltage VM1, and an output for outputting a first data signal having a positive polarity.

[0025] The second amplifying circuit 235 has a first input electrically coupled to the output of the PDAC 220 and the output of the NDAC 225 through a switch S12 of the first pair of switches S11 and S12 for receiving the first converted signal from the PDAC 220 or the second converted signal from the NDAC 225, a second input for receiving the power supply voltage VDD, a third input for receiving the ground voltage GND, and an output for outputting a second amplified signal. The second output stage 245 has a first input, a second input for receiving the power supply voltage VM2, a third input for receiving the ground voltage GND, and an output for outputting a second data signal having a negative polarity.

[0026] The first input of the first output stage 240 is electrically coupled to the output of the first amplifying circuit 230 and the output of the second amplifying circuit 235 through a switch S21 of the second pair of switches S21 and S22 for receiving the first amplified signal from the first amplifying circuit 230 or the second amplified signal from the second amplifying circuit 235

The first input of the second output stage 245 is electrically coupled to the output of the first amplifying circuit 230 and the output of the second amplifying circuit 235 through a switch S22 of the second pair of switches S21 and S22 for receiving the first amplified signal from the first amplifying circuit 230 or the second amplified signal from the second amplifying circuit 235 .

[0027] Additionally, each odd data line of the plurality of data line are electrically coupled to the output of the first output stage 240 and the output of the second output stage 245 through a switch S31 of the third pair of switches S31 and S32 for receiving the first data signal from the first output stage 240 or the second data signal from the second output stage 245. Each even data line of the plurality of data line are electrically coupled to the output of the first output stage 240 and the output of the second output stage 245 through a switch S32 of the third pair of switches S31 and S32 for receiving the first data signal from the first output stage 240 or the second data signal from the second output stage 245. The third pair of switches S31 and S32 is configured such that each odd data line of the plurality of data line receives one of the first and second data signals, while each even data line of the plurality of data line receives the other of the first and second data signals, and vice versa.

[0028] Furthermore, the source driver 200 may have a first level shifter coupled to the power supply voltage VDD and the first middle voltage VM1 for receiving digital input data of an image to be displayed, converting a voltage level of the digital image data, and outputting the first level-shifted signal to the PDAC 220. The source driver 200 may also have a second level shifter coupled to the ground voltage GND and the second middle voltage VM2, for receiving the digital input data of an image to be displayed, converting a voltage level of digital image data, and outputting the second level-shifted signal to the NDAC 225.

[0029] Additionally, the PDAC 220 may include a first input electrically coupled to the output of the first level shifter for receiving the first level-shifted signal therefrom, a second input for receiving the power supply voltage VDD, a third input for receiving the first middle voltage VM1, a fourth input for receiving a Gamma voltage, and an output for outputting a first converted signal having a positive polarity. The NDAC 225 may also includes a first input electrically coupled to the output of the second level shifter for receiving the second level-shifted signal therefrom, a second input for receiving the second middle voltage VM2, a third input for receiving the ground voltage GND, a fourth input for receiving the Gamma voltage, and an output for outputting a second converted signal having a negative polarity.

[0030] In operation, the first pair of switches S11, and S12, the second pair of switches S21 and S22, and a third pair

of switches S31 and S32 are controlled by the control signal POL having a low state (POL = 0) and a high state (POL = 1).

[0031] When the control signal POL is in the low state, as shown in Fig. 2, the first converted signal is output from the PDAC 220 to the first amplifying circuit 230 ; the first amplified signal is output from the first amplifying circuit 230 to the first output stage 240; the first data signal is output from the first output stage 240 to the odd data lines of the plurality of data lines. The signals are transmitted from the PDAC 220 to the odd data lines along a path 260. Further, the second converted signal is output from the NDAC 225 to the second amplifying circuit 235; the second amplified signal is output from the second amplifying circuit 235 to the second output stage 245; the second data signal is output from the second output stage 245 to the even data lines of the plurality of data lines. The signals are transmitted from the NDAC 225 to the even data lines along a path 265.

[0032] When the control signal POL is in the high state, as shown in Fig. 3, the first converted signal is output from the PDAC 220 to the second amplifying circuit 235; the second amplified signal is output from the second amplifying circuit 235 to the first output stage 240; the first data signal is output from the first output stage 240 to the even data lines of the plurality of data lines. The signals are transmitted from the PDAC 220 to the even data lines along a path 270. Further, the second converted signal is output from the NDAC 225 to the first amplifying circuit 230; the first amplified signal is output from the first amplifying circuit 230 to the second output stage 245; the second data signal is output from the second output stage 245 to the odd data lines of the plurality of data lines. The signals are transmitted from the NDAC 225 to the odd data lines along a path 275

[0033] Fig. 4 shows various configurations of a source driver: (a) a conventionally full voltage driving configuration, (b) an half voltage driving configuration with the first middle voltage VM1 = (VDD/2 - ΔV) and the second middle voltage VM2 = (VDD/2 + ΔV) according to one embodiment of the present invention, and (c) an half voltage driving configuration with the first middle voltage VM1= VDD/2, and the second middle voltage VM2 = VDD/2 according to another embodiment of the present invention. VDD and GND are the power supply voltage and the ground voltage, respectively. I₁ and I₂ are respectively the current flow through the power supply to the first amplifying circuit 230 and the first output stage 240 and through the second middle voltage supply to the second output stage 245.

[0034] Accordingly, the power consumption of the source driver shown in Fig. 4(a) is about

$$P_{IC-1} = VDD \times (I_1 + I_2),$$

And its system power consumption is in the form of

$$P_{SYS-1} = VDD \times (I_1 + I_2),$$

which is same as the power consumption of the source driver.

[0035] The power consumption of the source driver shown in Fig. 4(b) is about

$$\begin{aligned} P_{IC-2} &= (VDD/2 - \Delta V) \times I_1 + (VDD/2 + \Delta V) \times I_2 = VDD/2 \times (I_1 + I_2) + \Delta V \times (I_1 + I_2) = \\ &= VDD/2 \times (I_1 + I_2) \times (1 + 2 \times \Delta V/VDD) \\ &= P_{IC-1}/2 \text{ (assuming that } \Delta V \text{ is very small)}. \end{aligned}$$

The power consumption of the source driver shown in Fig. 4(b) is approximately an half of that of the conventional source driver shown in Fig. 4(a).

[0036] For the source driver shown in Fig. 4(c), the power consumption is obtained by

$$\begin{aligned} P_{IC-3} &= (VDD/2) \times I_1 + (VDD/2) \times I_2 \\ &\approx P_{IC-1}/2. \end{aligned}$$

The power consumption of the source driver shown in Fig. 4(c) is approximately an half of that of the conventional source driver shown in Fig. 4(a).

[0037] Accordingly, the operation temperature can also be reduced significantly for the half voltage driving configuration of the source driver of the present invention. Fig. 5 lists exemplary results of the power consumptions and operation temperatures of an LCD module under a conventionally full voltage driving configuration (Full-AVDD) and the half voltage

driving configuration (Half-AVDD) according to embodiment of the present invention for various power consumption check patterns, such as white, black, sub-V-stripe, H-stripe and sub-checker, and different frame rates, such as 60 Hz, as shown in Fig. 5(a), and 120 Hz, as shown in Fig. 5(b). It is clearly shown that for all these power consumption check patterns with different frame rates, the power consumptions and operation temperatures of the LCD panel under the half voltage driving configuration (Half-AVDD) of the present invention are reduced substantially, comparing those under the conventionally full voltage driving configuration (Full-AVDD). Further, the reductions of the power consumptions and operation temperatures are the most significant for the H-stripe pattern with a higher frame rate. For example, according to the present invention, 31.38 % of the power consumption and 37.39 °C of the operation temperature are reduced for the frame rate of 60 Hz, while 33.66 % of the power consumption and 70.33 °C of the operation temperature are reduced for the frame rate of 120 Hz.

[0038] Additionally, according to the half voltage driving configuration of the present invention, the deviation of the pixel driving voltages is also minimized, so that no V-line mura and/or flickers occur when an image is displayed in the display. Furthermore, no chopper and YDIO signals are needed in driving the display.

[0039] For example, for a conventional source driver, a source data signal with a positive polarity applied to a channel (data line) is output from a first amplifier (OP1) with a positive polarity, while the source data signal with a negative polarity for the channel is output from a second amplifier (OP2) with a negative polarity. If the target driving voltages of a pixel, e.g., Pexil1, are about ± 5 V, as shown in Fig. 6(a), ideally, the RMS (root-mean-square) brightness is averaged with the positive and negative polarities, which is:

$$\text{Brightness} = \text{RMS}(5\text{V}, -5\text{V}).$$

[0040] In fact, due to the manufacturing process, the outputs of the amplifiers may have voltage deviations from the input voltages. Provided that the output of the first amplifier (OP1) with the positive polarity has a voltage deviation of about +12 mV from the input target voltage, +5 V, and the output of the second amplifier (OP2) with the negative polarity has a voltage deviation of about -5 mV from the input target voltage, -5 V, as shown in Fig. 6(b), the actual RMS brightness in the channels is about

$$\text{Brightness} = \text{RMS}(5.012\text{V}, -5.005\text{V}) = 5\text{V} + 8\text{mV}.$$

[0041] However, according to the present invention, the source data signal with the positive and negative polarities for the channel are always output from the first amplifier (OP1), as shown in Fig. 6(d). Accordingly, the RMS brightness in the channels is about

$$\text{Brightness} = \text{RMS}(5.012\text{V}, -4.988\text{V}) = 5\text{V} + 0.014\text{mV}.$$

[0042] Therefore, there are no bright and dark lines in the display according to the present invention.

[0043] Fig. 7 shows experimental results of the RMS deviations from a conventional source driver (a) and from the source driver of the present invention (b). The maximal deviation from the conventional source driver is about ± 28 mV. However, it is about ± 19 mV for the source driver of the present invention, which is significantly reduced, compared to the deviation of the conventional source driver.

[0044] The present invention, among other things, discloses a source driver that comprises a first digital-to-analog converter with a positive polarity (PDAC), a second digital-to-analog converter with a negative polarity (NDAC), a first amplifying circuit, a first output stage, a second amplifying circuit and a second output stage. Both the PDAC and NDAC are coupled to the first and second amplifying circuits through a first pair of switches. The first amplifying circuit and the first output stage are coupled to the second amplifying circuit and the second output stage through a second pair of switches. The first and second output stages are coupled to odd data lines and even data line through a third pair of switches. Further, the amplitudes of the operational voltages for the PDAC, the NDAC and the first and second output stages are set to be between the supply voltage and the ground voltage. Accordingly, the power consumption and the operational temperature are substantially reduced.

Claims

1. A source driver (100, 200) for driving a display having a plurality of pixels spatially arranged in a matrix form, and

a plurality of data lines, each data line being associated with pixels of a corresponding pixel column, comprising:

- (a) a first pair of switches (S11, S12), a second pair of switches (S21, S22), and a third pair of switches (S31, S32), controlled by a control signal (POL);
- (b) a first digital-to-analog converter (120, 220) with a positive polarity (PDAC) configured to output a first converted signal having a positive polarity;
- (c) a second digital-to-analog converter (125, 225) with a negative polarity (NDAC) configured to output a second converted signal having a negative polarity;
- (d) a first amplifying circuit (130, 230) having a first input electrically coupled to the output of the PDAC and the output of the NDAC through one (S11) of the first pair of switches (S11, S12) and configured to receive the first converted signal from the PDAC or the second converted signal from the NDAC, a second input configured to receive a power supply voltage (VDD), a third input configured to receive a ground voltage (GND), and an output configured to output a first amplified signal;
- (e) a first output stage (140, 240) having a first input, a second input configured to receive the power supply voltage (VDD), a third input configured to receive a first middle voltage (VM1), and an output configured to output a first data signal;
- (f) a second amplifying circuit (135, 235) having a first input electrically coupled to the output of the PDAC and the output of the NDAC through the other (S12) of the first pair of switches (S11, S12) and configured to receive the first converted signal from the PDAC or the second converted signal from the NDAC, a second input configured to receive the power supply voltage (VDD), a third input configured to receive the ground voltage (GND), and an output configured to output a second amplified signal; and
- (g) a second output stage (145, 245) having a first input, a second input configured to receive a second middle voltage (VM2), a third input configured to receive the ground voltage (GND), and an output configured to output a second data signal;

wherein the first input of the first output stage (140, 240) is electrically coupled to the output of the first amplifying circuit (130, 230) and the output of the second amplifying circuit (135, 235) through one (S21) of the second pair of switches (S21, S22) and is configured to receive the first amplified signal from the first amplifying circuit (230) or the second amplified signal from the second amplifying circuit (235); wherein the first input of the second output stage (145, 245) is electrically coupled to the output of the first amplifying circuit (130, 230) and the output of the second amplifying circuit (135, 235) through the other (S22) of the second pair of switches (S21, S22) and is configured to receive the first amplified signal from the first amplifying circuit (130, 230) or the second amplified signal from the second amplifying circuit (135, 235); wherein an odd data line of the plurality of data lines is electrically coupled to the output of the first output stage (140, 240) and the output of the second output stage (145, 245) through one (S31) of the third pair of switches (S31, S32) and is configured to receive the first data signal from the first output stage (140, 240) or the second data signal from the second output stage (145, 245); wherein an even data line of the plurality of data lines is electrically coupled to the output of the first output stage (140, 240) and the output of the second output stage (145, 245) through the other (S32) of the third pair of switches (S31, S32) and is configured to receive the first data signal from the first output stage (240) or the second data signal from the second output stage (245); wherein the third pair of switches (S31, S32) is configured such that the odd data line of the plurality of data lines receives one of the first and second data signals, while the even data line of the plurality of data lines receives the other of the first and second data signals, and vice versa; and wherein the first and second data signals have positive and negative polarities, respectively, and the control signal (POL) has a low state and a high state, wherein when the control signal (POL) is in the high state, the odd data line of the plurality of data lines receives the first data signal, while the even data line of the plurality of data lines receives the second data signal, and when the control signal (POL) is in the low state, the odd data line of the plurality of data lines receives the second data signal, while the even data line of the plurality of data lines receives the first data signal.

2. The source driver (100) of claim 1, further comprising:

- (a) a first level shifter (110) having a first input configured to receive input data, a second input configured to receive the power supply voltage (VDD), a third input configured to receive the first middle voltage (VM1), and an output configured to output a first level-shifted signal of the input data to the first digital-to-analog converter (120); and
- (b) a second level shifter (115) having a first input configured to receive the input data, a second input configured to receive the second middle voltage (VM2), a third input configured to receive the ground voltage (GND), and an output configured to output a second level-shifted signal of the input data to the second digital-to-analog

converter (125).

3. The source driver (100) of claim 2, wherein the PDAC further comprises a first input electrically coupled to the output of the first level shifter (110) and configured to receive the first level-shifted signal therefrom, a second input configured to receive the power supply voltage (VDD), a third input configured to receive the first middle voltage (VM1), a fourth input configured to receive a Gamma voltage, and an output configured to output a first converted signal having a positive polarity; and wherein the NDAC further comprises a first input electrically coupled to the output of the second level shifter (115) and configured to receive the second level-shifted signal therefrom, a second input configured to receive the second middle voltage (VM2), a third input configured to receive the ground voltage (GND), a fourth input configured to receive the Gamma voltage, and an output configured to output a second converted signal having a negative polarity.
4. The source driver (100, 200) of claim 1, wherein each of the first middle voltage (VM1) and the second middle voltage (VM2) is less than the power supply voltage (VDD) and greater than the ground voltage (GND) and the first middle voltage (VM1) and the second middle voltage (VM2) are identical to or different from each other.

Patentansprüche

1. Quelltreiber (100, 200) zur Ansteuerung einer Anzeige mit einer Mehrzahl von Bildpunkten, die räumlich in einer Matrixform angeordnet sind, und einer Mehrzahl von Datenleitungen, wobei jede Datenleitung mit den Bildpunkten einer korrespondierenden Pixelspalte verbunden ist, umfassend:

(a) ein erstes Paar von Schaltern (S11, S12), ein zweites Paar von Schaltern (S21, S22) und ein drittes Paar von Schaltern (S31, S32), welche durch ein Steuersignal (POL) angesteuert werden;

(b) einen ersten Digital-zu-Analog-Wandler (120, 220) mit einer positiven Polarität (PDAC), der zur Ausgabe eines ersten konvertierten Signals konfiguriert ist, das eine positive Polarität aufweist;

(c) einen zweiten Digital-zu-Analog-Wandler (125, 225) mit einer negativen Polarität (NDAC), der zur Ausgabe eines zweiten konvertierten Signals konfiguriert ist, das eine negative Polarität aufweist;

(d) eine erste Verstärkerschaltung (130, 230), die einen ersten Eingang, der elektrisch mit dem PDAC-Ausgang und dem NDAC-Ausgang durch einen (S11) von dem ersten Paar von Schaltern (S11, S12) gekoppelt ist und konfiguriert ist, um das erste konvertierte Signal vom PDAC oder das zweite konvertierte Signal vom NDAC zu empfangen, einen zweiten Eingang, der zum Empfang einer Stromversorgungsspannung (VDD) konfiguriert ist, einen dritten Eingang, der zum Empfang einer Erdungsspannung (GND) konfiguriert ist, und einen Ausgang aufweist, der zur Ausgabe eines ersten verstärkten Signals konfiguriert ist;

(e) eine erste Ausgangsstufe (140, 240), die einen ersten Eingang, einen zweiten Eingang, der zum Empfang der Stromversorgungsspannung (VDD) konfiguriert ist, einen dritten Eingang, der zum Empfang einer ersten Mittelspannung (VM1) konfiguriert ist, und einen Ausgang aufweist, der zur Ausgabe eines ersten Datensignals konfiguriert ist;

(f) eine zweite Verstärkerschaltung (135, 235), die einen ersten Eingang, der elektrisch mit dem PDAC-Ausgang und dem NDAC-Ausgang durch den anderen (S12) von dem ersten Paar von Schaltern (S11, S12) gekoppelt ist und konfiguriert ist, um das erste konvertierte Signal vom PDAC oder das zweite konvertierte Signal vom NDAC zu empfangen, einen zweiten Eingang, der zum Empfang der Stromversorgungsspannung (VDD) konfiguriert ist, einen dritten Eingang, der zum Empfang der Erdungsspannung (GND) konfiguriert ist, und einen Ausgang aufweist, der zur Ausgabe eines zweiten verstärkten Signals konfiguriert ist; und

(g) eine zweite Ausgangsstufe (145, 245), die einen ersten Eingang, einen zweiten Eingang, der zum Empfang einer zweiten Mittelspannung (VM2) konfiguriert ist, einen dritten Eingang, der zum Empfang der Erdungsspannung (GND) konfiguriert ist, und einen Ausgang aufweist, der zur Ausgabe eines zweiten Datensignals konfiguriert ist;

wobei der erste Eingang der ersten Ausgangsstufe (140, 240) elektrisch mit dem Ausgang der ersten Verstärkerschaltung (130, 230) und dem Ausgang der zweiten Verstärkerschaltung (135, 235) durch einen (S21) von dem zweiten Paar von Schaltern (S21, S22) gekoppelt ist und konfiguriert ist, um das erste verstärkte Signal von der ersten Verstärkerschaltung (230) oder das zweite verstärkte Signal von der zweiten Verstärkerschaltung (235) zu empfangen,

wobei der erste Eingang der zweiten Ausgangsstufe (145, 245) elektrisch mit dem Ausgang der ersten Verstärkerschaltung (130, 230) und dem Ausgang der zweiten Verstärkerschaltung (135, 235) durch den anderen (S22) von dem zweiten Paar von Schaltern (S21, S22) gekoppelt ist und konfiguriert ist, um das erste verstärkte Signal von

der ersten Verstärkerschaltung (130, 230) oder das zweite verstärkte Signal von der zweiten Verstärkerschaltung (135, 235) zu empfangen,

wobei eine ungerade Datenleitung der Mehrzahl von Datenleitungen elektrisch mit dem Ausgang der ersten Ausgangsstufe (140, 240) und dem Ausgang der zweiten Ausgangsstufe (145, 245) durch einen (S31) von dem dritten Paar von Schaltern (S31, S32) gekoppelt ist und konfiguriert ist, um das erste Datensignal von der ersten Ausgangsstufe (140, 240) oder das zweite Datensignal von der zweiten Ausgangsstufe (145, 245) zu empfangen, wobei eine gerade Datenleitung der Mehrzahl von Datenleitungen elektrisch mit dem Ausgang der ersten Ausgangsstufe (140, 240) und dem Ausgang der zweiten Ausgangsstufe (145, 245) durch den anderen (S32) von dem dritten Paar von Schaltern (S31, S32) gekoppelt ist und konfiguriert ist, um das erste Datensignal von der ersten Ausgangsstufe (240) oder das zweite Datensignal von der zweiten Ausgangsstufe (245) zu empfangen, wobei das dritte Paar von Schaltern (S31, S32) so konfiguriert ist, dass die ungerade Datenleitung der Mehrzahl von Datenleitungen entweder das erste oder das zweite Datensignal empfängt, während die gerade Datenleitung der Mehrzahl von Datenleitungen das andere von dem ersten und zweiten Datensignalen empfängt, und umgekehrt und

wobei die ersten und zweiten Datensignale entsprechend positive und negative Polaritäten haben, und wobei das Steuersignal (POL) einen Tiefstand und einen Hochstand hat, wobei, wenn das Steuersignal (POL) in dem Hochstand ist, die ungerade Datenleitung der Mehrzahl von Datenleitungen das erste Datensignal empfängt, während die gerade Datenleitung der Mehrzahl von Datenleitungen das zweite Datensignal empfängt, und wobei, wenn das Steuersignal (POL) in dem Tiefstand ist, die ungerade Datenleitung der Mehrzahl von Datenleitungen das zweite Datensignal empfängt, während die gerade Datenleitung der Mehrzahl von Datenleitungen das erste Datensignal empfängt.

2. Quelltreiber (100) nach Anspruch 1, ferner umfassend:

(a) einen ersten Pegelwandler (110), der einen ersten Eingang, der zum Empfang von Eingangsdaten konfiguriert ist, einen zweiten Eingang, der zum Empfang der Stromversorgungsspannung (VDD) konfiguriert ist, einen dritten Eingang, der zum Empfang der ersten Mittelspannung (VM1) konfiguriert ist, und einen Ausgang aufweist, der zur Ausgabe eines ersten pegelverschobenen Signals der Eingangsdaten an den ersten Digital-zu-Analog-Wandler (120) konfiguriert ist; und

(b) einen zweiten Pegelwandler (115), der einen ersten Eingang, der zum Empfang der Eingangsdaten konfiguriert ist, einen zweiten Eingang, der zum Empfang der zweiten Mittelspannung (VM2) konfiguriert ist, einen dritten Eingang, der zum Empfang der Erdungsspannung (GND) konfiguriert ist, und einen Ausgang aufweist, der zur Ausgabe eines zweiten pegelverschobenen Signals der Eingangsdaten an den zweiten Digital-zu-Analog-Wandler (125) konfiguriert ist.

3. Quelltreiber (100) nach Anspruch 2, bei welchem der PDAC ferner einen ersten Eingang, der elektrisch mit dem Ausgang des ersten Pegelwandlers (110) gekoppelt ist und konfiguriert ist, um das erste pegelverschobene Signal davon zu empfangen, einen zweiten Eingang, der zum Empfang der Stromversorgungsspannung (VDD) konfiguriert ist, einen dritten Eingang, der zum Empfang der ersten Mittelspannung (VM1) konfiguriert ist, einen vierten Eingang, der zum Empfang einer Gammaspannung konfiguriert ist, und einen Ausgang umfasst, der zur Ausgabe eines ersten konvertierten Signals mit einer positiven Polarität konfiguriert ist; und wobei der NDAC ferner einen ersten Eingang, der elektrisch mit dem Ausgang des zweiten Pegelwandlers (115) gekoppelt ist und konfiguriert ist, um das zweite pegelverschobene Signal davon zu empfangen, einen zweiten Eingang, der zum Empfang der zweiten Mittelspannung (VM2) konfiguriert ist, einen dritten Eingang, der zum Empfang der Erdungsspannung (GND) konfiguriert ist, einen vierten Eingang, der zum Empfang der Gammaspannung konfiguriert ist, und einen Ausgang umfasst, der zur Ausgabe eines zweiten konvertierten Signals mit einer negativen Polarität konfiguriert ist.

4. Quelltreiber (100, 200) nach Anspruch 1, bei welchem die erste Mittelspannung (VM1) und die zweite Mittelspannung (VM2) jeweils geringer sind als die Stromversorgungsspannung (VDD) und größer sind als die Erdungsspannung (GND) und die erste Mittelspannung (VM1) und die zweite Mittelspannung (VM2) gleichgroß oder voneinander verschieden sind.

Revendications

1. Dispositif de contrôle d'une source (100, 200) pour contrôler un dispositif d'affichage ayant une pluralité de pixels agencés spatialement sous une forme de matrice, et une pluralité de lignes de données, chaque ligne de données étant associée à des pixels d'une colonne de pixels correspondante, comprenant:

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(a) une première paire de commutateurs (S11, S12), une deuxième paire de commutateurs (S21, S22), et une troisième paire de commutateurs (S31, S32), commandées par un signal de commande (POL);
(b) un premier convertisseur numérique-analogique (120, 220) ayant une polarité positive (PDAC) configuré pour délivrer en sortie un premier signal converti ayant une polarité positive;
5 (c) un second convertisseur numérique-analogique (125, 225) ayant une polarité négative (NDAC) configuré pour délivrer en sortie un second signal converti ayant une polarité négative;
(d) un premier circuit amplificateur (130, 230) ayant une première entrée électriquement couplée à la sortie du PDAC et à la sortie du NDAC à travers l'un (S11) de la première paire de commutateurs (S11, S12) et configurée pour recevoir le premier signal converti à partir du PDAC ou le second signal converti à partir du NDAC, une
10 deuxième entrée configurée pour recevoir une tension d'alimentation électrique (VDD), une troisième entrée configurée pour recevoir une tension de masse (GND), et une sortie configurée pour délivrer en sortie un premier signal amplifié;
(e) un premier étage de sortie (140, 240) ayant une première entrée, une deuxième entrée configurée pour recevoir la tension d'alimentation électrique (VDD), une troisième entrée configurée pour recevoir une première
15 tension intermédiaire (VM1), et une sortie configurée pour délivrer en sortie un premier signal de données;
(f) un second circuit amplificateur (135, 235) ayant une première entrée électriquement couplée à la sortie du PDAC et à la sortie du NDAC à travers l'autre (S12) de la première paire de commutateurs (S11, S12) et configurée pour recevoir le premier signal converti à partir du PDAC ou le second signal converti à partir du
20 NDAC, une deuxième entrée configurée pour recevoir la tension d'alimentation électrique (VDD), une troisième entrée configurée pour recevoir la tension de masse (GND), et une sortie configurée pour délivrer en sortie un second signal amplifié; et
(g) un second étage de sortie (145, 245) ayant une première entrée, une deuxième entrée configurée pour recevoir une seconde tension intermédiaire (VM2), une troisième entrée configurée pour recevoir la tension de
25 masse (GND), et une sortie configurée pour délivrer en sortie un second signal de données;

dans lequel la première entrée du premier étage de sortie (140, 240) est électriquement couplée à la sortie du premier circuit amplificateur (130, 230) et à la sortie du second circuit amplificateur (135, 235) à travers l'un (S21) de la deuxième paire de commutateurs (S21, S22) et est configurée pour recevoir le premier signal amplifié à partir
30 du premier circuit amplificateur (230) ou le second signal amplifié à partir du second circuit amplificateur (235);

dans lequel la première entrée du second étage de sortie (145, 245) est électriquement couplée à la sortie du premier circuit amplificateur (130, 230) et à la sortie du second circuit amplificateur (135, 235) à travers l'autre (S22) de la deuxième paire de commutateurs (S21, S22) et est configurée pour recevoir le premier signal amplifié à partir
35 du premier circuit amplificateur (130, 230) ou le second signal amplifié à partir du second circuit amplificateur (135, 235);

dans lequel une ligne de données impaire de la pluralité de lignes de données est électriquement couplée à la sortie du premier étage de sortie (140, 240) et à la sortie du second étage de sortie (145, 245) à travers l'un (S31) de la troisième paire de commutateurs (S31, S32) et est configurée pour recevoir le premier signal de données à partir
40 du premier étage de sortie (140, 240) ou le second signal de données à partir du second étage de sortie (145, 245);
dans lequel une ligne de données paire de la pluralité de lignes de données est électriquement couplée à la sortie du premier étage de sortie (140, 240) et à la sortie du second étage de sortie (145, 245) à travers l'autre (S32) de la troisième paire de commutateurs (S31, S32) et est configurée pour recevoir le premier signal de données à partir
45 du premier étage de sortie (240) ou le second signal de données à partir du second étage de sortie (245);

dans lequel la troisième paire de commutateurs (S31, S32) est configurée de telle manière que la ligne de données impaire de la pluralité de lignes de données reçoit l'un des premier et second signaux de données, tandis que la
50 ligne de données paire de la pluralité de lignes de données reçoit l'autre des premier et second signaux de données, et vice versa; et

dans lequel les premier et second signaux de données ont des polarités positive et négative, respectivement, et le signal de commande (POL) a un état bas et un état haut, dans lequel lorsque le signal de commande (POL) est dans l'état haut, la ligne de données impaire de la pluralité de lignes de données reçoit le premier signal de données,
55 tandis que la ligne de données paire de la pluralité de lignes de données reçoit le second signal de données, et lorsque le signal de commande (POL) est dans l'état bas, la ligne de données impaire de la pluralité de lignes de données reçoit le second signal de données, tandis que la ligne de données paire de la pluralité de lignes de données reçoit le premier signal de données.

2. Dispositif de contrôle d'une source (100) selon la revendication 1, comprenant en outre:

(a) un premier dispositif de décalage de niveau (110) ayant une première entrée configurée pour recevoir des données d'entrée, une deuxième entrée configurée pour recevoir la tension d'alimentation électrique (VDD),

une troisième entrée configurée pour recevoir la première tension intermédiaire (VM1), et une sortie configurée pour délivrer en sortie un premier signal à niveau décalé des données d'entrée au premier convertisseur numérique-analogique (120);

et

(b) un second dispositif de décalage de niveau (115) ayant une première entrée configurée pour recevoir les données d'entrée, une deuxième entrée configurée pour recevoir la seconde tension intermédiaire (VM2), une troisième entrée configurée pour recevoir la tension de masse (GND), et une sortie configurée pour délivrer en sortie un second signal à niveau décalé des données d'entrée au second convertisseur numérique-analogique (125).

3. Dispositif de contrôle d'une source (100) selon la revendication 2, dans lequel le PDAC comprend en outre une première entrée électriquement couplée à la sortie du premier dispositif de décalage de niveau (110) et configurée pour recevoir le premier signal à niveau décalé à partir de celle-ci, une deuxième entrée configurée pour recevoir la tension d'alimentation électrique (VDD), une troisième entrée configurée pour recevoir la première tension intermédiaire (VM1), une quatrième entrée configurée pour recevoir une tension Gamma, et une sortie configurée pour délivrer en sortie un premier signal converti ayant une polarité positive;

et dans lequel le NDAC comprend en outre une première entrée électriquement couplée à la sortie du second dispositif de décalage de niveau (115) et configurée pour recevoir le second signal à niveau décalé à partir de celle-ci, une deuxième entrée configurée pour recevoir la seconde tension intermédiaire (VM2), une troisième entrée configurée pour recevoir la tension de masse (GND), une quatrième entrée configurée pour recevoir la tension Gamma, et une sortie configurée pour délivrer en sortie un second signal converti ayant une polarité négative.

4. Dispositif de contrôle d'une source (100, 200) selon la revendication 1, dans lequel chacune de la première tension intermédiaire (VM1) et de la seconde tension intermédiaire (VM2) est inférieure à la tension d'alimentation électrique (VDD) et supérieure à la tension de masse (GND) et la première tension intermédiaire (VM1) et la seconde tension intermédiaire (VM2) sont identiques l'une à l'autre ou différentes l'une de l'autre.

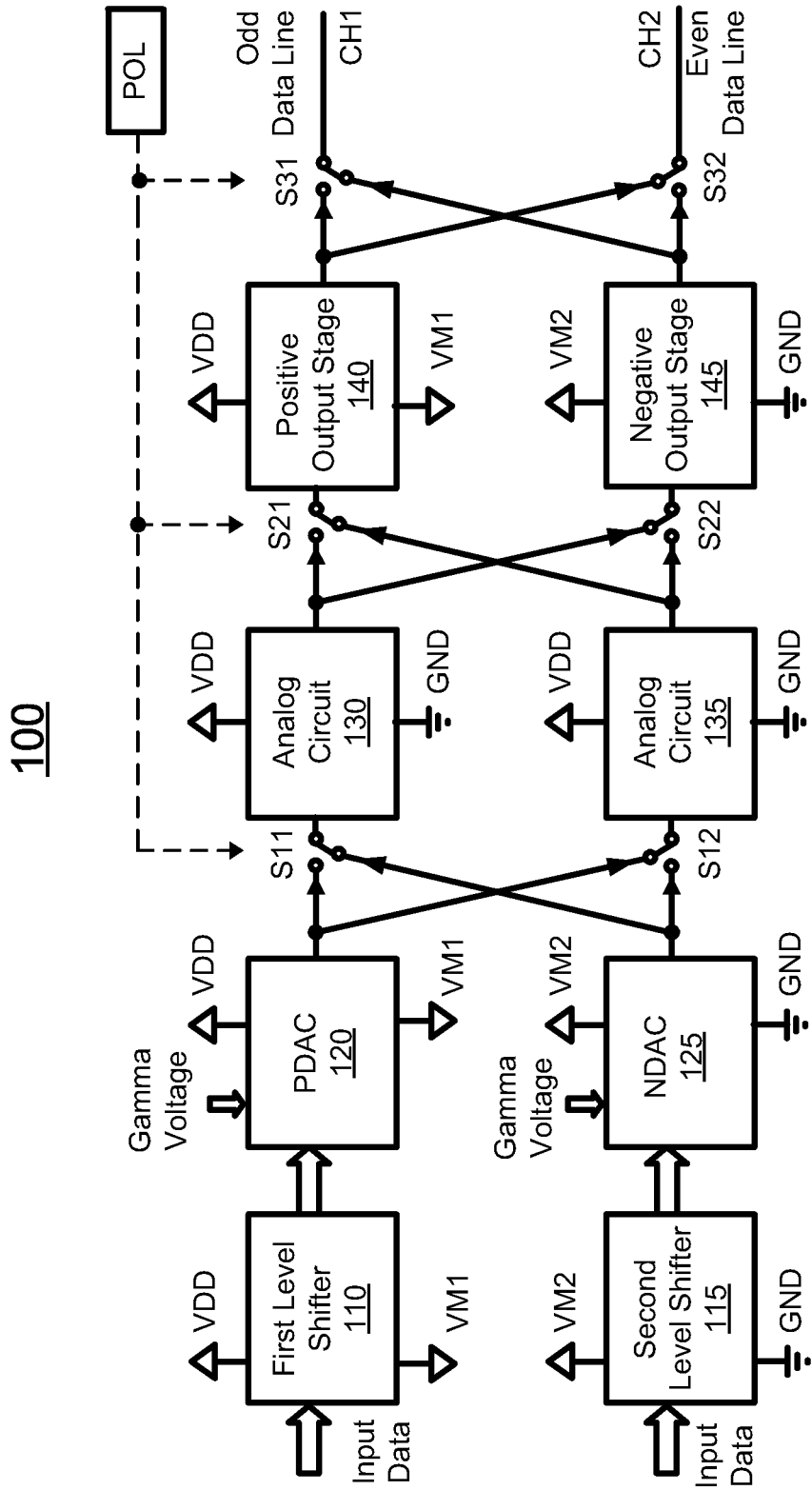


Fig. 1

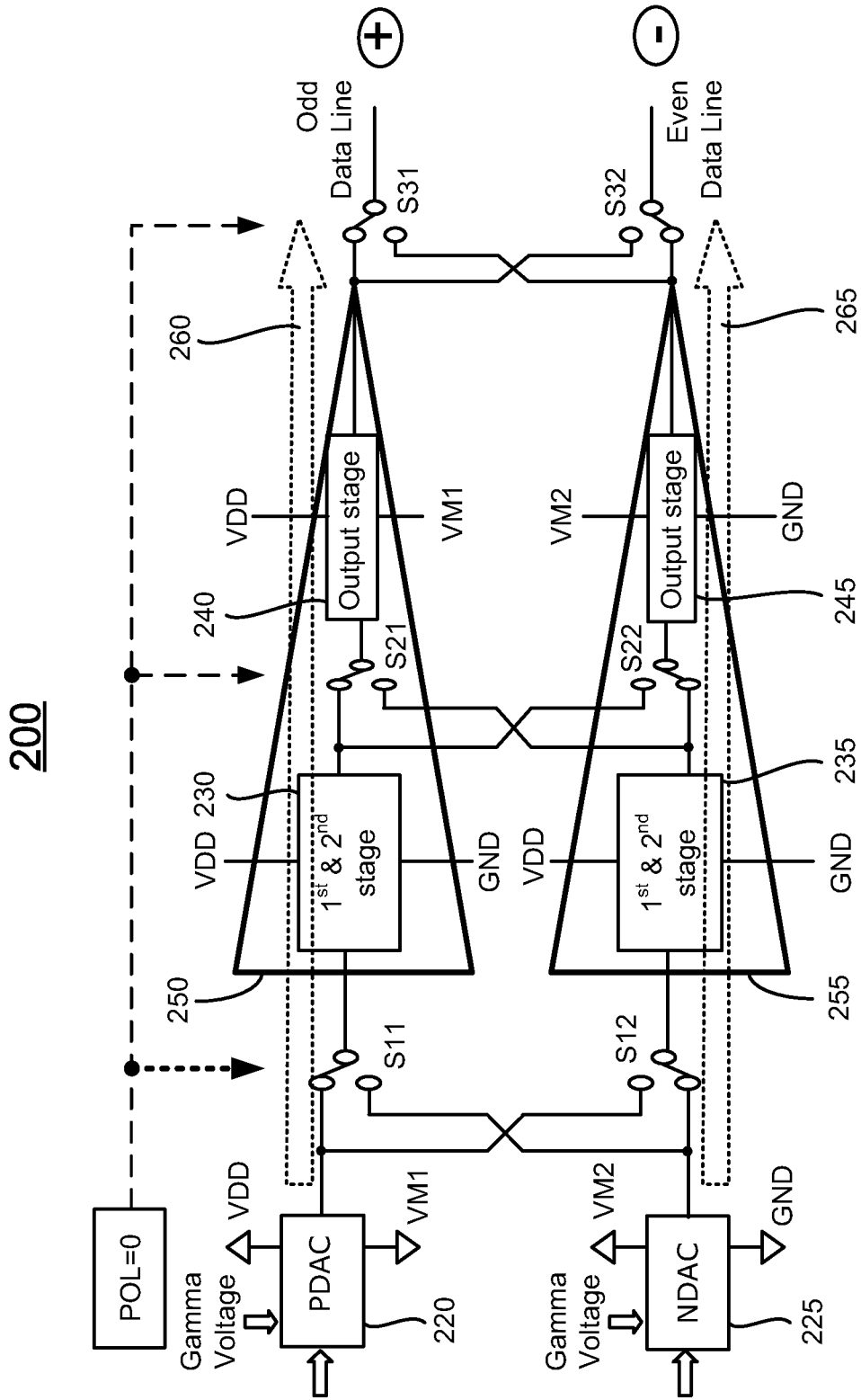


Fig. 2

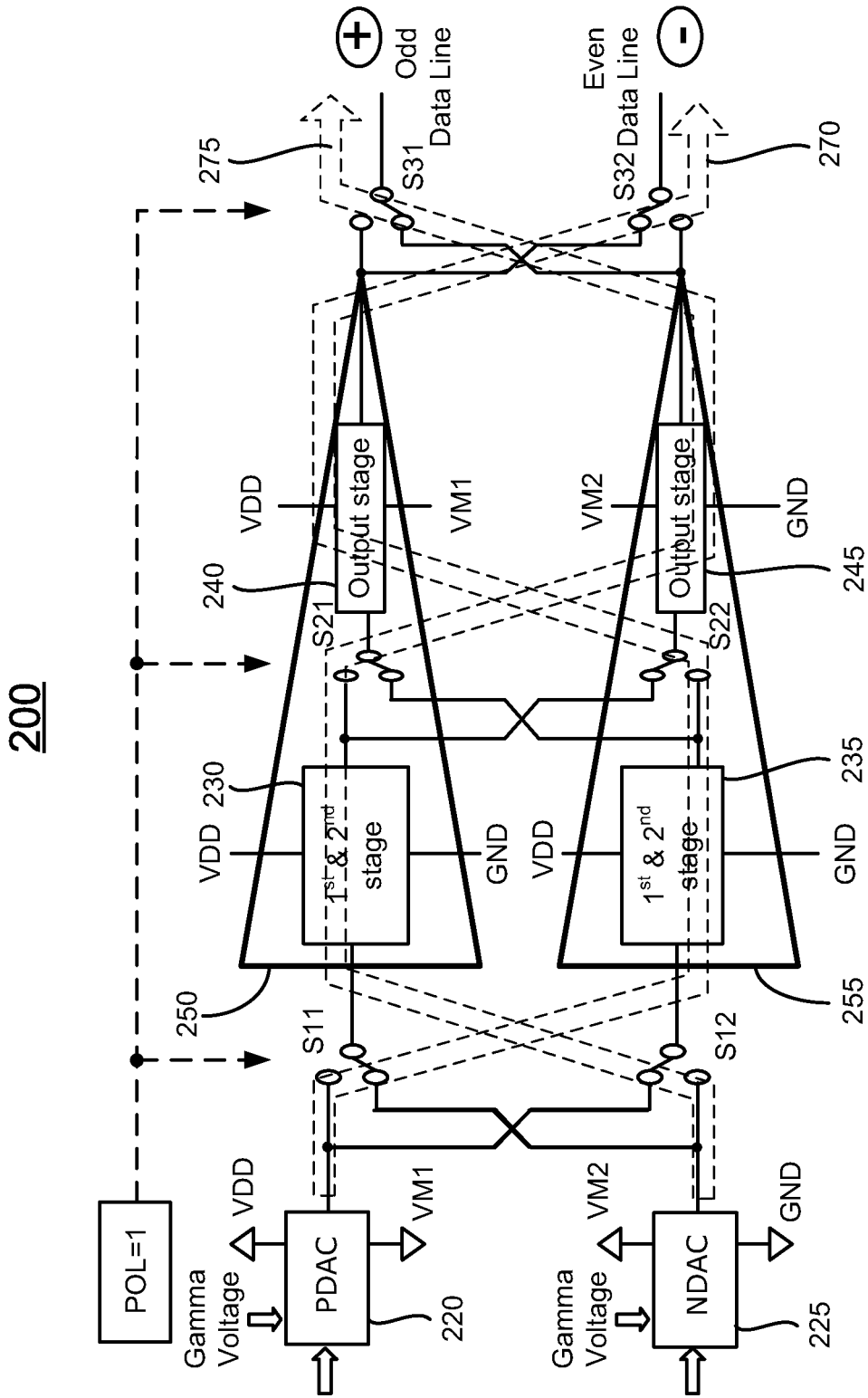


Fig. 3

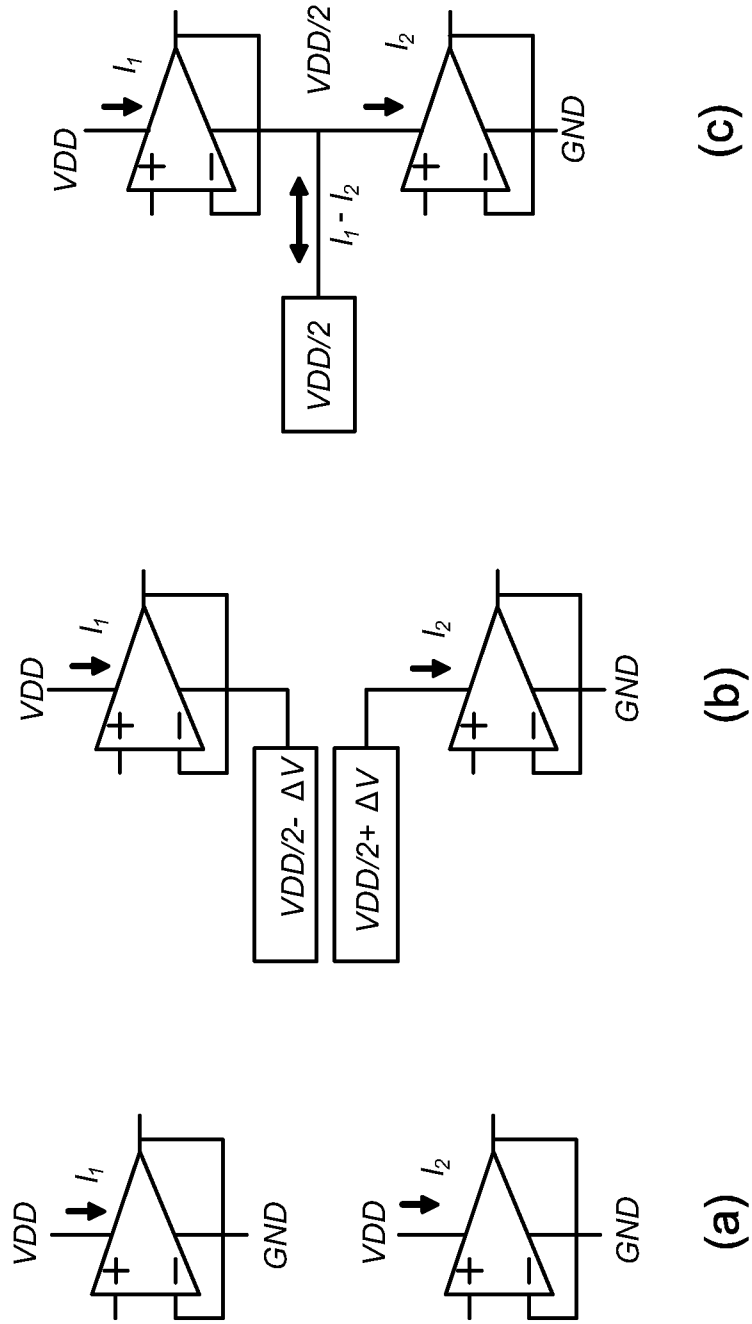


Fig. 4

□ 60Hz, 2-Line dot Inversion, PWRC=H, CS enable (L,H), ODLY disable

	Full-AVDD		Half-AVDD		$\Delta T(^{\circ}C)$	$\Delta P(w)$	Saving Ratio $\Delta P/P2 \times 100\%$
	P2(w)	T(C)	P1(w)	T(C)			
White	9.756	80	9.06	72.7	7.3	0.696	7.13%
Black	5.58	68.75	4.68	60.73	8.02	0.9	16.12%
Sub-v-stripe	9.576	81.27	8.328	69.56	11.71	1.248	13.0%
H-stripe	11.316	112.02	7.764	74.63	37.39	3.552	31.38%
Sub-checker	10.56	93.4	8.676	77.26	16.14	1.884	17.84%

(a)

□ 120Hz, Column Inversion, PWRC=H, CS disable, ODLY disable

	Full-AVDD		Half-AVDD		$\Delta T(^{\circ}C)$	$\Delta P(w)$	Saving Ratio $\Delta P/P2 \times 100\%$
	P2(w)	T(C)	P1(w)	T(C)			
White	5.628	61.47	5.412	59.95	1.52	0.216	3.83%
Black	5.868	67.02	5.28	63.37	3.65	0.588	10.02%
Sub-v-stripe	5.832	64.8	5.496	62.00	2.8	0.336	5.76%
H-stripe	16.86	160.05	11.184	89.72	70.33	5.676	33.66%
Sub-checker	11.4	96.95	8.376	72.27	24.68	3.024	26.52%

(b)

Fig. 5

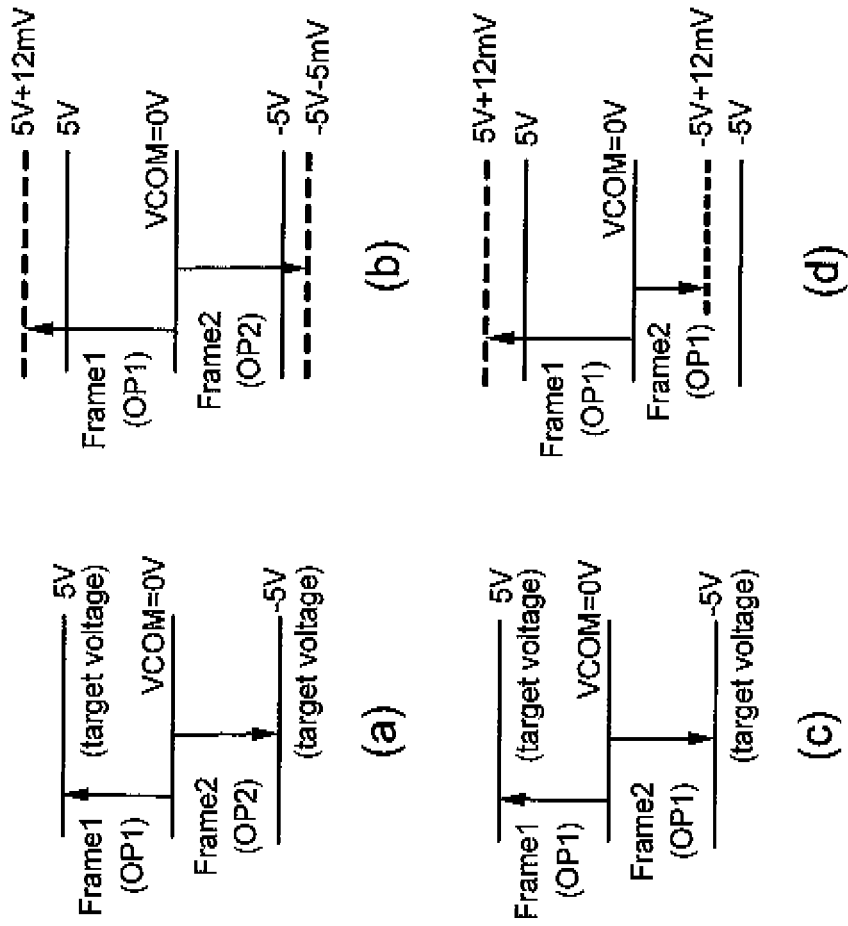


Fig. 6

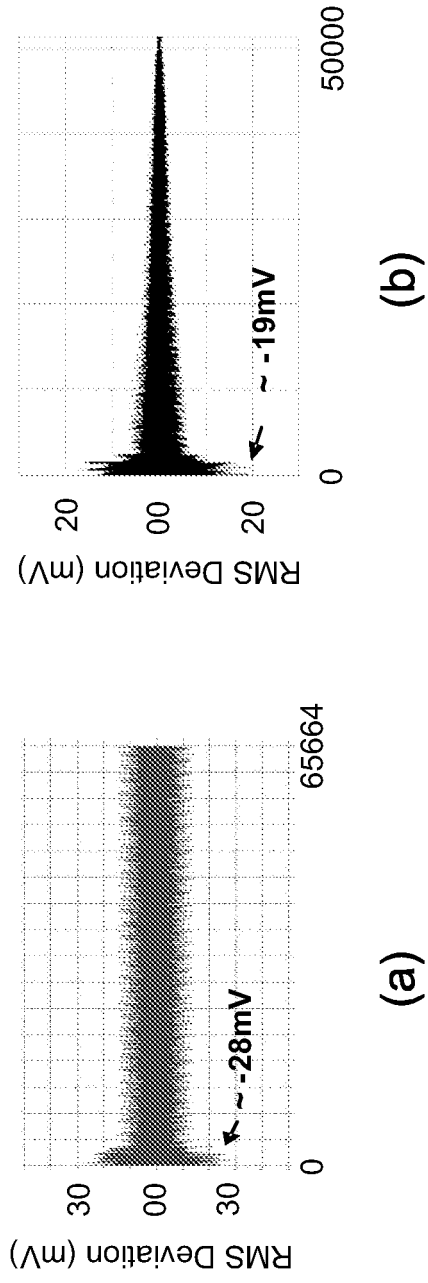


Fig. 7

REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	用于驱动液晶显示装置的方法和设备		
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外部链接	Espacenet		

摘要(译)

本发明的一个方面涉及一种源极驱动器，包括具有正极性 (PDAC) 的第一数模转换器，具有负极性的第二数模转换器 (NDAC)，第一运算放大器和第二运算放大器。每个运算放大器的特征在于第一级和第二级以及输出级。PDAC和NDAC都通过第一对开关耦合到第一和第二运算放大器。第一运算放大器的第一和第二和输出级通过第二对开关耦合到第二运算放大器的第一和第二和输出级。第一和第二运算放大器通过第三对开关耦合到奇数数据线和偶数数据线。此外，PDAC，NDAC和输出级第一和第二运算放大器的工作电压的幅度被设置在电源电压和地电压之间。因此，功耗和工作温度显著降低。

