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(54) **Method of manufacturing a high quality and ultra large screen liquid crystal display device.**

Methode zur Herstellung einer Flüssigkristallanzeige von hoher Qualität und mit ultragrossem Bildschirm

Procédé de fabrication d'un affichage à cristaux liquides de haute qualité à grand écran

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Description

FIELD OF THE INVENTION

[0001] This invention relates to a method of producing a liquid crystal display device using a transverse electric field system, and more particularly, an ultra large screen liquid crystal display device which is capable of dramatically improving an aperture ratio, a transmittance ratio, brightness, and contrast with low cost and high production yield.

BACKGROUND OF THE INVENTION

[0002] A liquid crystal display device utilizing a transverse electric fields system which applies an electric field to a liquid crystal in a parallel direction with a substrate has a wide viewing angle and is the standard for a large screen liquid crystal display. Such technologies have been proposed, for example, by Japanese patent laid-open publication Nos. 10-55000, 10-325961, 11-24104, 10-55001, 10-170939, and 11-52420, and have been improved to solve problems such as vertical crosstalk.

[0003] Numerous technologies have been proposed by liquid crystal makers including a technology in which a photolithography spacer is utilized to improve the contrast of a transverse electric field type liquid crystal display system. For example, such a technology has been proposed by Japanese patent laid-open publication Nos. 2000-199904 and 2000-19527. The majority of them utilize a photolithography technology to establish a spacer on a color filter substrate. The Japanese patent laid-open publication Nos. 2000-19527 and 2000-199904 show an idea of producing an electric field of a video signal line in a vertical direction of a substrate rather than a horizontal direction in order to suppress the vertical crosstalk. This requires the dielectric constant of the photolithography spacer to be larger than the dielectric constant of the liquid crystal. The Japanese patent laid-open publication No. 2000-19526 also proposed a photolithography spacer in which the dielectric constant is larger than that of the liquid crystal.

[0004] The Japanese patent laid-open publication No. 2001-209053 proposes a photolithography spacer in a vertical electric field system utilizing dielectric material with a smaller dielectric constant than that of the liquid crystal along a video signal line to cover the video signal line in order to lower the waveform distortion. According to this patent publication, the liquid crystal cell is constructed by creating a vacuum space inside the liquid crystal cell, then injecting the liquid crystal in the space through an injection opening using the atmospheric pressure. In this liquid crystal injection method, a batch process is used in which several hundred cells are processed at the same time to produce a large liquid crystal panel.

[0005] Japanese patent laid-open publication Nos. 2002-258321 and 2002-323706 teach a structure using a dielectric material of a smaller dielectric constant than that of the liquid crystal along the video signal line to cover the video signal line and placing a transparent conductive material along the video signal line to improve the pixel aperture ratio as well as to prevent signal delay.

[0006] Figure 3 is a flow chart showing a typical production process in the conventional technology for producing a TFT (thin film transistor) array substrate (active matrix substrate) of the transverse electric field type liquid crystal panel. This production process includes four-step photomasking processes using the conventional halftone exposure technology. Figures 36A-36F are cross sectional views showing the structural developments in accordance with the production flow of Figure 3 using the four-step photomasking technology.

[0007] In the conventional production process of Figure 3, gate electrodes of thin film transistors and common electrodes are formed at the same time in step S11. Then, at step S12, thin film transistors are separated from a semiconductor layer and source electrodes and drain electrodes of the thin film transistors are formed using the halftone photomask exposure. In step S13, contact holes for gate terminals, data terminals, pixel drain portions, and transistor circuits for electrostatic protection are created. Then, at step S14, gate terminals, data terminals, transparent conductive pixel electrodes are formed.

[0008] In the cross sectional views of Figures 36A-36F, a numeral 6 denotes an area on a positive photoresist layer after development where UV exposure is blocked, a numeral 7 denotes an area on the positive photoresist layer after development where the UV exposure is made through the halftone (translucent) photomask, a numeral 9 denotes a gate insulation film, a numeral 10 denotes a thin film semiconductor layer (non-doped layer), a numeral 11 denotes a thin film semiconductor layer (doped layer, i.e., ohmic contact layer), a numeral 15 denotes a scanning line, a numeral 50 denotes a scanning line terminal, a numeral 51 denotes a video signal line, a numeral 54 denotes a scanning line drive circuit contact-electrode, a numeral 64 denotes a drain electrode of the thin film transistor, and a numeral 65 denotes a transparent pixel electrode.

[0009] Prior to the start of the processes of Figures 36A-36F, the scanning lines 15 and the scanning terminals 50 are formed on a glass substrate (not shown). In Figure 36A, the gate insulation film 9, the thin film semiconductor layer (non-doped layer) 10 and the thin film transistor ohmic contact layer 11 are respectively deposited by, for example, a CVD plasma device. The positive photoresist 6 is coated and the halftone exposure is conducted so that the thicker positive photoresist 6 and the thinner positive photoresist 7 are created. In Figures 36B and 36C, through a dry etching process, the thin film transistors are separated from the semiconductor layer. In Figure 36D, the drain electrode 64 of the thin film transistor and the video signal line 51 are formed by further conducting the etching process. In Figure 36E, through the dry etching, contact holes are created over the scan-

ning line terminals 50. In Figure 36F, the scanning line drive circuit electrodes 54 and the transparent pixel electrodes 65 are formed.

[0010] The conventional transverse electric field type liquid crystal panel utilizes common electrodes placed at both sides of the video signal line to shield the electric field caused by the signal video line. In order for this construction to completely solve the problem involved with the vertical crosstalk, it is necessary to design the width of the common electrodes to be at least 1.5 times larger than that of the video signal line, hence resulted in a reduction of the pixel aperture ratio.

[0011] It is possible to reduce the vertical crosstalk by collecting the electric force lines of the electric field produced by the video signal line to the photolithography spacer. This can be done by placing a black mask made of thin film conductive material (chromium oxide layer and chromium metal thin film layer) at the side of color filter and setting the electric potential of the black mask to that of the common electrodes, and creating a photolithography spacer that is placed in an elongated fashion at the same direction as the video signal line by an insulation material that has a dielectric constant larger than that of the liquid crystal. However, in this method, because the material of large dielectric constant is used, the capacitance between the black mask and the video signal line is increased, hence the video signal waveform is delayed and distorted, which is not appropriate for a large screen liquid crystal panel.

[0012] As disclosed in Japanese patent laid-open publication No. 11-24104, it is possible to almost completely shield the video signal line by constructing a passivation layer on the: video signal line and placing a shielding electrode thereon along the video signal line. However, because this construction utilizes a very thin passivation layer with a thickness in the range between 0.3 micrometer and 1 micrometer, and the passivation layer made of silicon oxide or silicon nitride has a relatively large dielectric constant of 4-6, the capacitance between the shielding electrode and the video signal line increases. This causes the signal waveform to be delayed and distorted and is not appropriate for a large screen liquid crystal display panel.

[0013] Japanese patent laid-open publication No. 2001-209053 discloses a photolithography spacer constructed in a very thin manner that surround the video signal line using a dielectric material of a small dielectric constant so that the capacitance between the common electrodes on the side of the color filter and the video signal line can be decreased. This technology, however, utilizes a conventional method of

[0014] injecting the liquid crystal through an injection opening. Thus, the thin and long photolithography spacers cause the liquid crystal to be injected at a very slow speed, which severely decreases the production efficiency.

[0015] Japanese patent laid-open publication Nos. 2002-258321 and 2002-323706 disclose a structure which utilizes a dielectric material that has a smaller dielectric constant than that of the liquid crystal to cover the video signal line and places a transparent conductive material along the video signal line so that the pixel aperture ratio can be improved and the video signal line delay can be prevented. However, with this construction, it is not possible to produce the liquid crystal cell and the spacer at the same time. Therefore, an additional photolithography process has to be performed to produce the photolithography spacers. This causes the production processes to be more complicated and costly.

[0016] The implementation of the technology disclosed in Japanese patent laid-open publication No. 2002-258321 is not enough to produce a transverse electric field type liquid crystal panel with high contrast and low light leakage. When an angle of the bumps of the dielectric material with a small dielectric constant that cover the video signal lines along the video signal lines is larger than 40 degrees, the conventional technology of rubbing treatment using rubbing cloth causes areas with alignment defects due to the sideways slip caused at the tapered portions of the bumps in the direction of the movement at the tips of hairs of the rubbing cloth or areas on the inclined surfaces of the bumps where the hair tips of the rubbing cloth cannot reach.

[0017] US 2002/0149729, on which the preamble of claim 1 is based, discloses a method of producing an active matrix substrate of a transverse electric field type active matrix liquid crystal display apparatus which has a large pixel aperture ratio, a high luminance and good yield without causing any signal delay on wiring or increasing any driving voltage. In a structure in which a capacity is formed on a superimposed part of a common signal electrode and at least one of a data signal wiring and a scanning signal wiring via an interlayer insulating film, of insulating films included in the interlayer insulating film, at least a layer is selectively formed at least on a part of a region on a pixel electrode.

SUMMARY OF THE INVENTION

[0018] The present invention has been made to solve the above mentioned problems involved in the conventional technology, and it is an object of the present invention to provide a large screen color liquid crystal display device which is capable of achieving an improved aperture ratio, a transmittance ratio, high brightness and high contrast while promoting low cost and high production yield.

[0019] The object is attained by a method of producing an active matrix substrate of a transverse electric field type active matrix liquid crystal display device according to claim 1.

[0020] According to the claimed method, since it is possible to produce the insulation bump covering the video signal lines or to produce both the bumps covering the video signal lines and the spacer at the same time with use of the halftone exposure technique, thus it is possible

to reduce the production steps and cost. According to the conventional technologies shown in Japanese patent laid-open publication Nos. 2002-258321 and 2002-323706, a separate process is required for producing the photolithography spacers, which inevitably increases the production cost.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021]

Figures 1A-1B are cross sectional views showing the halftone exposure photomask and the positive photoresist after development on the active matrix substrate.

Figures 2A-2B are cross sectional views showing the halftone exposure photomask and the positive photoresist after development on the active matrix substrate.

Figure 3 is a flow chart showing the four operational steps involved in the photomasking process in the conventional technology.

Figure 4 is a flow chart showing the four operational steps involved in the photomasking processes.

Figures 5A-5C are cross sectional views showing an example of the separate two-step exposure method and the structure of the positive photoresist after development.

Figures 6A-6C are cross sectional views showing another example of the separate two-step exposure method and the structure of the positive photoresist after development.

Figures 7A-7E are cross sectional views showing an example of production process for forming the video signal lines and the common electrodes.

Figures 8A-8E are cross sectional views showing another example of production process for forming the video signal lines and the common electrodes.

Figure 9 is a perspective view showing the structure of a laser optical system used in the laser alignment marking process.

Figure 10 is a schematic diagram showing the laser optical system employing a fθ lens used in the laser alignment marking process.

Figure 11 is a schematic diagram showing the positions of the laser alignment markers formed by the laser optical system.

Figure 12 is a schematic diagram showing the structure of the optical system used for the laser beam scanning exposure.

Figure 13 is a schematic diagram showing the structure of the titler optical system (inverted real image) for the ultraviolet ray exposure method using a micro mirror array.

Figure 14 is a schematic diagram showing the structure of the multi-lens optical system (noninverted real image) for the ultraviolet ray exposure method using a micro mirror array.

Figure 15 is a plan view showing an example of structure of the multi-lens scanning exposure system used.

Figure 16 is a timing chart for explaining the operation of the micro mirror array for the ultraviolet light transmission adjustment by controlling the time widths.

Figure 17 is a plan view showing an example of structure of the scanning exposure device used in the multi-lens scanning exposure system.

Figure 18 is a plan view showing an example of structure in scanning exposure device used in the direct halftone exposure method in which a photomask is not used.

Figure 19 is a cross sectional view showing the scanning exposure device used in the separate two-step exposure method.

Figures 20A-20B are schematic diagrams showing the principle of the exposure in the direct halftone exposure and a cross sectional structure of the photoresist after the development.

Figure 21 is a circuit diagram showing an example of configuration in the static electricity protection circuit formed by thin film transistors.

Figure 22 is a circuit diagram showing another example configuration in the static electricity protection circuit formed by thin film transistors.

Figure 23 is a plan view showing an example of the structure of the static electricity protection circuit formed by the thin film transistors.

Figure 24 is a plan view showing another example of the structure of the static electricity protection circuit formed by the thin film transistors.

Figure 25 is a plan view showing a further example of the structure of the static electricity protection circuit formed by the thin film transistors.

Figure 26 is a plan view showing a further example of the structure of the static electricity protection circuit formed by the thin film transistors.

Figures 27A-27F are cross sectional views showing an example of the active matrix substrate production flow involved in the four-step photomasking process.

Figures 28A-28F are cross sectional views showing an example of the active matrix substrate production flow involved in the three-step photomasking process.

Figure 29 is a plan view showing an example of structure in the scanning exposure device used in the mixed exposure method.

Figure 30 is a plan view showing another example of structure in the scanning exposure device used in the mixed exposure method.

Figure 31 is a plan view showing an example of structure of the transverse electric field type active matrix array substrate produced using the mixed exposure method.

Figures 32A-32E are schematic diagrams showing the principle of the halftone shift exposure method

and a cross sectional structure of the photoresist after the development.

Figures 33A-33B are schematic diagrams showing an example of principle of the halftone shift exposure method.

Figures 34A-34B are schematic diagrams showing another example of principle of the halftone shift exposure method.

Figures 35A-35E are schematic diagrams showing the principle of the halftone shift exposure method and a cross sectional structure of the photoresist after the development.

Figures 36A-36F are cross sectional views showing an example of the production flow involved in the four-step photomasking process in the conventional technology.

Figures 37A-37B are schematic diagrams showing a further example of principle of the halftone shift exposure method.

Figures 38A-38B are schematic diagrams showing an example of principle of the separate two-step exposure method.

Figures 39A-39B are schematic diagrams showing another example of principle of the separate two-step exposure method.

Figures 40A-40B are schematic diagrams showing a further example of principle of the separate two-step exposure method.

Figures 41A-41B are schematic diagrams showing a further example of principle of the separate two-step exposure method.

Figure 42 is a flow chart showing an example of the production flow involved in the four-step photomasking process.

Figures 43A-43B are schematic diagrams showing a further example of principle of the separate two-step exposure method.

Figures 44A-44B are schematic diagrams showing a further example of principle of the separate two-step exposure method.

Figure 45 is a cross sectional view showing an example of structure in the transverse electric field type liquid crystal panel including the spacers covering the video signal lines and the shielding electrodes formed on the spacers.

Figure 46 is a cross sectional view showing another example of structure in the transverse electric field type liquid crystal panel including the spacers covering the video signal lines, and the shielding electrodes formed on the spacers.

Figure 47 is a cross sectional view showing an example of structure in the transverse electric field type liquid crystal panel.

Figure 48 is a cross sectional view showing another example of structure in the transverse electric field type liquid crystal panel.

Figure 49 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 50 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 51 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 52 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 53 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 54 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 55 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 56 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 57 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 58 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 59 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 60 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 61 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 62 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 63 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 64 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 65 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 66 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 67 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 68 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 69 is a plan view showing an example of structure in the transverse electric field type liquid crystal display device.
Figure 70 is a plan view showing another example of structure in the transverse electric field type liquid crystal display device.
Figure 71 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 72 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 73 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 74 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 75 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 76 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 77 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 78 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 79 is a plan view showing' a further example of structure in the transverse electric field type liquid crystal display device.
Figure 80 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 81 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 82 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 83 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 84 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 85 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 86 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 87 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 88 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 89 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 90 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 91 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 92 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 93 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 94 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 95 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 96 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 97 is a plan view showing a further example of structure in the transverse electric field type liquid crystal display device.
Figure 98 is a graph showing the characteristics concerning the thickness of the negative photoresist after development used in the halftone process.
Figure 99 is a graph showing the characteristics concerning the line width of the negative photoresist after development used in the halftone process.
Figures 100A-100B are cross sectional views showing an example of cross sectional structures of the photomask used in the halftone exposure and the negative photoresist after the development.
Figures 101A-101B are cross sectional views showing another example of cross sectional structures of the photomask used in the halftone exposure and the negative photoresist after the development.
Figures 102A-102C are cross sectional views showing an example of separate two-step exposure method and the cross sectional structure of the negative photoresist after the development.
Figures 103A-103C are cross sectional views showing another example of separate two-step exposure method and the cross sectional structure of the negative photoresist after the development.
Figure 104 shows an enlarged cross sectional view of the bump covering the video signal line and the photolithography spacer constructed on the bump.
Figure 105 is a flow chart showing the production flow involved in the four-step photomasking process.
Figures 106A-106F are cross sectional views showing the active matrix substrate production flow in-

volved in the four-step photomasking process using the halftone shift exposure method.

Figures 107A-107D are cross sectional views showing the process involved in the transverse electric field type liquid crystal panel which is planarized with use of the back surface exposure method.

Figure 108 is a cross sectional view showing an example of structure in the transverse electric field type liquid crystal panel.

Figure 109 is a cross sectional view showing another example of structure in the transverse electric field type liquid crystal panel.

Figure 110 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 111 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 112 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figure 113 is a cross sectional view showing a further example of structure in the transverse electric field type liquid crystal panel.

Figures 114A-114C are cross sectional views showing the process for planarizing the active matrix substrate and forming the photolithography spacers at the same time with use of the halftone back surface exposure method.

Figure 115 is a plan view showing an example of structure in the transverse electric field type liquid crystal display device.

Figure 116 is a flow chart showing an example of production flow involved in the six-step photomasking process.

Figure 117 is a flow chart showing another example of production flow involved in the six-step photomasking process.

Figure 118 is a flow chart showing a further example of production flow involved in the six-step photomasking process.

Figure 119 includes a cross sectional view and a plan view showing the structure of the transverse electric field type liquid crystal panel in the vicinity of the main seal.

Figure 120 is a schematic diagram showing the relationship between the alignment direction and the rotation direction of the liquid crystal molecules of the positive anisotropic dielectric material used in the transverse electric field type liquid crystal panel.

Figure 121 is a schematic diagram showing the relationship between the alignment direction and the rotation direction of the liquid crystal molecules of the negative anisotropic dielectric material used in the transverse electric field type liquid crystal panel.

Figure 122 is a plan view showing an example of structure of the color filter used in the transverse electric field type liquid crystal display panel.

Figure 123 is a plan view showing another example of structure of the color filter used in the transverse electric field type liquid crystal display panel.

Figure 124 is a flow chart showing an example of production flow involved in the three-step photomasking process.

Figure 125 is a flow chart showing an example of production flow involved in the five-step photomasking process.

Figure 126 is a flow chart showing an example of production flow involved in the four-step photomasking process.

Figure 127 is a flow chart showing an example of production flow involved in the three-step photomasking process.

Figure 128 is a flow chart showing an example of production flow involved in the five-step photomasking process.

Figure 129 is a flow chart showing an example of production flow involved in the six-step photomasking process.

Figures 130A-130C are cross sectional views showing the process for planarizing the active matrix substrate and forming the photolithography spacers at the same time with use of the halftone back surface exposure method.

Figure 131 is a cross sectional view showing an example of structure of the halftone back surface exposure device.

Figure 132 is a plan view showing an example of structure of the halftone back surface exposure device.

Figure 133 is a cross sectional view showing another example of structure of the halftone back surface exposure device.

Figure 134 is a plan view showing another example of structure of the halftone back surface exposure device.

Figure 135 is a schematic diagram showing an overall system configuration of the halftone back surface exposure device.

Figure 136 is a flow chart showing an overall process of the halftone back surface exposure method.

Figure 137 is a cross sectional view showing an example of optical structure in the white light interferometer.

[0022] DETAILED DESCRIPTION OF THE INVENTION

[0023] Embodiments will now be described in more detail with reference to the accompanying drawings.

[0024] Of these embodiments, the embodiments 1 through 8 and 11 through 24 relate to the present invention. The embodiments 9, 10, and 25, even if not directly relating to the invention, still are useful for a better understanding of the invention as well as of its features and advantages.

[First embodiment]

[0025] Figures 45, 46, 47, 70, 72, 74, 76, 78 and 80 show the first embodiment of the present invention. Figures 45-47 are cross sectional views showing examples of structure in the transverse electric field type liquid crystal panel including spacers covering, the video signal lines and the shielding electrodes formed on the spacers according to the present invention. Figures 70, 72, 74, 76, 78 and 80 are plan views showing examples of structure in the transverse electric field type liquid crystal display device according to the present invention.

[0026] In Figures: 45-47, a numeral 9 denotes a gate insulation film, a numeral 51 denotes a video signal line, a numeral 53 denotes a liquid crystal drive electrode (pixel electrode), a numeral 55 denotes a passivation film, a numeral 66 denotes a glass substrate in the side of color filter, a numeral 67 denotes a black mask (light shielding film), a numeral 68 denotes a color filter layer, a numeral 69 denotes a levelling layer in the side of color filter, a numeral 70 denotes an alignment film in the side of color filter, a numeral 71 denotes an alignment film in the side of TFT (thin film transistor) array substrate, a numeral 72 denotes a common electrode (upper layer) for shielding the electric field produced by the video signal line, a numeral 73 denotes a spacer bump for covering the video signal line, a numeral 74 denotes a common electrode within the pixel (upper layer), a numeral 75 denotes a common electrode (lower layer) for shielding the electric field produced by the video signal line, and a numeral 76 denotes a glass substrate in the side of the TFT array.

[0027] Further in Figures 70, 72, 74, 76, 78 and 80, a numeral. 15 denotes a scanning line, a numeral 49 denotes a common electrode within the pixel (lower layer), a numeral 79 denotes a shielding electrode formed on both side walls of the spacer bump, a numeral 80 denotes a TFT (thin film transistor) element, a numeral 81 denotes a contact hole for connecting the shielding common electrode and the lower layer common electrode, and a numeral 82 denotes the lower layer electrode.

[0028] The lower layer common electrodes 75 for shielding the electric field of the video signal line is constructed at the same time as the scanning lines 51 on the same layer. The video signal line 51 and the liquid crystal drive electrodes 53 are constructed at the same time on the same layer. The upper layer shielding common electrodes 72 for shielding the electric field of the video signal line and the common electrodes 74 within the pixel are constructed at the same time on the same layer. In the example of Figure 46, as opposed to the example of Figure 45, the upper layer shielding common electrodes 72 have a wider electrode width than that of the lower layer shield common electrodes 75. The structure shown in Figure 46 is able to provide a larger aperture ratio than that of the structure shown in Figure 45.

[0029] The video signal line 51. and the liquid crystal drive electrodes 53 are covered by the passivation layer 55, and the spacer bumps 73 are constructed in a manner to cover (surround) the video signal lines 51. The upper layer shielding common electrodes 72 can cover the spacer bumps 73 completely as shown in Figures 70 and 72, or the upper layer wall shielding common electrodes 79 can be placed at both side walls of the spacer bumps 73 as shown in Figures 76 and 80. When the height of the spacer bumps 73 is less than 3.0 micrometers or when the size of the liquid crystal panel is larger than 30 inches, the construction of the active matrix substrate using the upper layer wall shielding common electrodes 79. shown in Figures 76 and 80 would be preferable to more effectively prevent distortions in the video signal waveform.

[0030] The spacer bumps 73 shown in the cross sectional views of Figures 45, 46 and 47 actually have a gentle taper angle θ as shown in the cross sectional view of Figure 104. A distance L1 from an edge of the spacer bump 73 to an edge of the video signal line 51 is preferably at least 3 micrometers.

[0031] The taper angle θ of the spacer bump 73 in Figure 104 is preferably 30 degrees or smaller so that the movement of the tips of rubbing cloth hairs can be performed smoothly during the rubbing alignment treatment, thereby avoiding occurrence of alignment defective areas. It is preferable to make the distance L2 between an edge of the spacer bump 77 and the upper layer shielding common electrodes 79 be larger than 0.5 micrometers. Basically, the larger the distance L2, the better shielding effects will be available. When the lower shielding common electrodes do not exist such as in the example of Figure 47, the distance L2 of about 16 micrometers is sufficient.

[0032] It is imperative for the present invention that the cross sectional shape of the spacer bump 73 has an upward projection such as an oval, half oval, hyperbolic, or parabolic shape. This upward projection allows the spacer bump 73 to easily deform when a pressure caused by an atmospheric pressure is applied during a liquid crystal drop vacuum attachment alignment process. Materials utilized for forming the spacer bump 73 should be a type that allows the height of the spacer bump 73 to uniformly deform in the range between 0.1 micrometers and 0.5 micrometers when the atmospheric pressure is applied thereto, otherwise, a problem of residual air bubble will arise.

[0033] As shown in Figures 70, 74, and 76, it is especially important that the spacer bump 73 does not reside around the area of the crossing point between the scanning line 15 and the video signal line 51 because the liquid crystal has to be diffused in this area where the spacer bump 73 does not exist. In the example of Figures 78 and 80, an area where the spacer bump 73 does not exist is created at around the center of the pixel. Although the dripped liquid crystal will be diffused in this area, this structure of Figures 78 and 80 may not be suitable for a large screen liquid crystal panel, since the capacitance between the upper layer shielding common electrode 72 and the video signal line 51 will increase.

[0034] The construction as shown in Figure 74 in which the spacer bumps are also constructed over the scanning lines 15 and the upper layer common electrodes 72 are connected together between the upper and lower pixels and right and left pixels is suitable for a large screen liquid crystal display device. Since the shielding common electrodes 72 are connected in a mesh like manner, in the liquid crystal display device using this method, even when there is a breakage in the line, the resultant line fault will be negligible in the practical use.

[0035] It is preferable that the dielectric constant of the spacer bumps 73 is as small as possible, however, 3.3 or less should be sufficient for an actual implementation. In the case where the monomer or oligomer used as a material for forming the spacer bump 73 includes at least one benzocyclobutene structure or its dielectric material, or at least one fluorene skeleton or its dielectric material, then it is possible to composite the dielectric material with the dielectric constant of less than 3.3.

[0036] Figures 86 and 87 are plan views showing further examples of structure in the transverse electric field type liquid crystal display device of the first embodiment of the present invention. In the example of Figures 86 and 87, the size of the spacer bump 73 is minimized. In the drawings, a numeral 83 denotes a common electrode (upper layer) for shielding the electrical field produced by the video signal lines 51. As noted above, the numeral 75 denotes a lower layer shield common electrode. Because the size of the spacer bump 73 is minimized, the dielectric material of large dielectric constant can be used.

[Second preferred embodiment]

[0037] Figures 48, 49, 50, 71 and 75 show the transverse electric field type liquid crystal panel of the second embodiment of the present invention. Figures 48-50 are cross sectional views thereof and Figures 71 and 75 are plan views thereof. In the second embodiment, the common electrode within the pixel is formed under the passivation layer and the gate insulation film. The lower layer common electrodes 75 for shielding the electric field of the video signal lines 51 and the common electrodes 49 within the pixel for driving the liquid crystal element are constructed at the same time on the same layer where the scanning lines are formed. The video signal lines 51 and the liquid crystal drive electrodes 53 are constructed at the same time on the same layer.

[0038] In the example of Figure 49, as opposed to the example of Figure 48, the upper layer shielding common electrodes 72 have a wider width than that of the lower layer shielding common electrodes 75. Therefore, the structure shown in Figure 49 is able to achieve a larger aperture ratio than the structure shown in Figure 48. As shown in Figures 48-50, in the second embodiment, since the common electrode 49 within the pixel is constructed on the layer lower than the passivation layer 55 and the gate insulation layer 9, a voltage required to drive the liquid crystal tends to become higher.

[0039] With the structure used in the second embodiment of the present invention, as shown in Figure 71 and 75, the liquid crystal drive electrode 53 is sandwiched by the lower layer common electrode 82 connected to the common electrode 49 within the pixel and the upper shielding layer common electrode 72 through the gate insulation layer and the passivation layer. With this structure, it is possible to have a large hold capacity in a small area, thereby enabling to achieve a large aperture ratio.

[Third preferred embodiment]

[0040] Figures 51, 52, 53, 69, 73, 77, 79 and 81 show the transverse electric field type liquid crystal panel in the third embodiment of the present invention, Figures 51-53 are cross sectional views thereof and Figures 69, 73, 77, 79 and 81 are plan views thereof. In the drawings, a numeral 77 denotes an insulation (dielectric) bump covering the video signal line 51, a numeral 78 denotes a spacer formed on the bump 77 covering the video signal line 51, and a numeral 79 denotes a shielding common electrode formed on the side walls of the bump 77. The structure in the third embodiment is basically the same as that of the first embodiment noted above except that the spacer bump 73 in the first embodiment is separated to two structures, one is the insulation bump 77 that covers the video signal line 51 and the other is the spacer 78 that determines the liquid crystal cell gap.

[0041] One of the: features of the present invention is that the insulation bump 77 that covers the video signal line 51 and the spacer 78 that determines the liquid crystal cell gap can be produced through the same photolithography process. By utilizing a light transmission adjustable photomask (halftone photomask) as shown in Figures 1A-1B and 2A-2B and positive photoresist, it is possible to produce the cross sectional shape of the bump 77 and spacer 78 such as the one shown in Figure 104. It is also possible to produce the cross sectional shape the bump 77 and spacer 78 shown in Figure 104 by incorporating a two-step exposure technique (half exposure and supplemental exposure) as shown in Figure 5A-5C and Figures 6A-6C with use of an ordinary photomask and the positive photoresist.

[0042] In Figures 1A-1B, Figures 2A-2B, a numeral 1 denotes a silica glass substrate forming the photomask, a numeral 2 denotes a metal layer (Cr or Mo) on the glass substrate for controlling the amount of light pass therethrough, a numeral 3 denotes a translucent (halftone or gray) area of the photomask formed by slit patterns, a numeral 4 denotes a translucent (halftone or gray) area of the photomask (a-Si, TiSix, MoSix or Ti), a numeral 5 denotes a transparent area of the photomask, a numeral 6 denotes an area on a positive photoresist layer after development where UV exposure is blocked, a numeral 7 denotes an area on the positive photoresist layer after development where the UV exposure is made through the halftone (translucent) area of the photomask and a

numeral 8 denotes an area where the positive photoresist is completely removed after development, a numeral 9 denotes a gate insulation film, a numeral 10 denotes a thin film semiconductor layer (non-doped layer), a numeral 11 denotes a thin film semiconductor layer (doped layer, i.e., ohmic contact layer), a numeral 12 denotes a barrier metal layer, and a numeral 13 denotes a low resistance metal layer.

[0043] As shown in Figures 1A and 1B, unlike the opaque metal area 2 which completely blocks the UV light transmission, the area 3 allows the UV light to pass by a small amount (halftone) depending on the density of the slits. Thus, it is possible to create the area 6 where the photoresist is intact after development as well as the area 7 where the photoresist is removed but still remained (halftone exposed area). As shown in Figures 2A and 2B, the photomask includes the opaque area 2 and the translucent layer 4, and the transparent area 5. Thus, the photoresist is completely removed at the area 8 corresponding to the transparent area 5, the photoresist is removed halfway at the area (halftone exposed area) 7 corresponding to the translucent area 4, and the photoresist is unaffected in the area 6 corresponding to the opaque area 2. With use of the light transmission adjustable photomask shows in Figures 1A-1B and 2A-2B, the spacer bump 73 having the cross sectional structure shown in Figure 104 can be created by one photolithography process.

[0044] As noted above, the spacer bump 73 having the cross sectional structure shown in Figure 104 can also be created with use of the normal photomask through the two-step exposure method shown in Figures 5A-5C and 6A-6C. The photomask in this example has no halftone area and is configured only by the glass substrate 1 and the opaque metal layer 2. In Figures 5A-5C and 6A-6C, a numeral 19 denotes a UV light, a numeral 20 denotes an area on the positive photoresist layer after development where the UV light exposure is completely blocked, a numeral 21 denotes an area where the photoresist is removed after being completely exposed by the UV light 19, a numeral 22 denotes an area on the positive photoresist layer after development where the UV light exposure is made incompletely (under exposure), and a numeral 23 denotes an area where the photoresist is partially exposed by the second step of UV exposure, a numeral 24 denotes an area where the photoresist is completely removed by the first and second steps of UV light exposure, and a numeral 25 denotes an fθ lens used in the second exposure step of Figure 6B.

[0045] In the example of Figures 5A-5C, in the first exposure step of Figure 5A, the photoresist area 20 is not exposed because of the photomask metal (opaque) 2 and the photoresist area 21 is exposed by the UV light 19 in the degree that the photoresist 21 will not be completely removed after exposure (under exposure). In the second exposure step shown in Figure 5B, the photoresist area 21 that has been exposed in the first step is further exposed at the portion 23 at the position corresponding to the transparent portion of the photomask. Thus, as shown in Figure 5C, the photoresist is completely removed at the area 24, thereby creating the spacer 78 and bump 77 having the cross sectional structure shown in Figure 104.

[0046] In the example of Figures 5A-6C. the first exposure step (under exposure) is the same as that of Figure 5A. In the second exposure step shown in Figure 6B, the photoresist area 21 that has been exposed in the first step is further exposed at the portion 23 with use of the fθ lens. It should be noted that the photomask is not used in the second exposure step of. Figure 6B. The fθ lens has a function of producing focus points on the same flat surface of a relatively large area on the substrate. Thus, the relatively large area of the photoresist can be exposed uniformly without using a photomask. Accordingly as shown in Figure 6C, the photoresist is completely removed at the area 24, thereby creating the spacer 78 and bump 77 having the cross sectional structure shown in Figure 104.

[0047] However, it is difficult, although not impossible, to produce the bump and spacer with sufficient flexibility when using the positive photoresist. Therefore, one of the features of the present invention is to provide a method to utilize negative photoresist that has a more flexible characteristic to produce the cross sectional shape shown in Figure 104 with a singe photolithography process. It should be noted that types of negative photoresist that are susceptible to oxygen fault can suffer, when a quantity of exposure light is small, from accelerated photopolymerization by a small amount of ultraviolet light at the areas contacting with the glass substrate while it can suffer from lack of reaction in the photopolymerization by the oxygen in the atmosphere at the areas exposed to the atmosphere.

[0048] Figures 98 and 99 show the characteristics for this type of negative photoresist in terms of film thickness and line width with respect to parameters of the amount of exposure light and the length of the development. Using this type of negative photoresist and a light transmission adjustment photomask (halftone photomask) as shown in Figures 100A-100B and 101A-101B, it is possible to achieve the shape of the spacer and bump shown in Figure 104. The example of Figures 100A-100B corresponds to the process shown in Figures 2A-2B where the photomask includes the transparent portion 5, translucent portion (halftone) 4, and the opaque portion 2. The example of Figures 101A-101B corresponds to the process shown in Figures 1A-1B where the photomask includes the slit pattern (halftone photomask) 3 for incompletely exposing the photoresist in addition to the transparent portion and the opaque portion.

[0049] Alternatively, it is also possible to utilize a two-step exposure technique using the partial area complete exposure step and the half exposure step as shown in Figures 102A-102C and 103A-103C. The example of Figures 102A-102c corresponds to the process shown in Figures 5A-5C where the two different photomasks are

used in the first and second exposure steps. The example of Figures 103A-103B corresponds to the process shown in Figures 6A-6C where the fθ lens 25 is used in the second exposure step. In Figures 102A-102C and 103A-103C, a numeral 85 denotes an area of the negative photoresist after development where the photoresist is intact by the complete exposure of UV light, a numeral 86 denotes an area on the negative photoresist where the photoresist is removed but still remains by the incomplete exposure of UV light, and a numeral 87 denotes an area on the negative photoresist which is not exposed because of: the opaque pattern 2 on the photomask. In this manner, since the expensive light transmission: adjustment photomask (halftone photomask) does not need to be used, but an inexpensive ordinary photomask can be used in this example to produce the spacer 78 and bump 77 having the shape of Figure 104.

[0050] Figures 116-118 show examples of production flow using the six-step photomasking process for implementing the third embodiment of the present invention. In the example of Figure 116 which incorporates the halftone exposure technique, at step S51, gate electrodes (scanning line patterns) and common electrodes are formed at the same time. At step S52, the silicon elements are separated from a semiconductor thin film layer for forming the thin film transistors. Then, in step S53, through the first and second halftone exposure processes, source and drain electrodes of the thin film-transistors and liquid crystal drive electrodes are formed at the same time.

[0051] In the next step S54, the bumps that cover the video signal lines for shielding the electric field and the photolithography spacers that define the liquid crystal cell gap are formed through the first and second halftone exposure processes. At step S55, contact holes for terminal portions and circuits for static electricity protection are formed through an etching process. In the last step S56, the common electrodes for shielding the video signal lines, the transparent common electrodes within the pixel, and the gate and data electrodes at the same time.

[0052] In the example of Figure 117 which incorporates the halftone exposure technique, at step S61, gate electrodes (scanning line patterns) and common electrodes are formed at the same time through the first and second halftone exposure processes. At step S62, the silicon elements are separated from the semiconductor thin film layer for forming the thin film transistors. Then, in step S63, through the first and second (halftone exposure processes, source electrodes and drain electrodes of the thin film transistors, and liquid crystal drive electrodes are formed at the same time.

[0053] In the next step S64, the bumps that cover the video signal lines for shielding the electrical field and the photolithography spacers are formed through the first and second halftone exposure processes. At step S65, contact holes for terminal portions and circuits for static electricity protection are formed through an etching process. In the last step S66, the common electrodes for shielding the video signal lines, gate electrodes and data electrodes are formed at the same time.

[0054] In the example of Figure 118, at step S71, gate electrodes (scanning line patterns) and common electrodes are formed at the same time. At step S72, the silicon elements are separated from the semiconductor thin film layer for forming the thin film transistors. Then, in step S73, source electrodes and drain electrodes are formed at the same time. In the next step S74, the bumps that cover the video signal lines and the photolithography spacers are formed. At step S75, contact holes for terminal portions and circuits for static electricity protection are formed. In the last step S76, the common electrodes for shielding the video signal lines, common electrodes within the pixels, gate electrodes and data electrodes are formed at the same time.

[0055] Still referring to Figure 104, preferably, the thickness h1 of the bump 77 that covers the video signal line 51 is preferably in the range between 1.5 micrometers and 3.5 micrometers, and the spacer 78 projecting from the bump 77 has a height h2 of about 0.2-2.0 micrometers. As to the density of the spacers 78, about one (1) to seventy five (75) of them will be formed in an area of one square millimeter. The size of the area for the spacer is within a range between 200 square micrometers and 2,000 square micrometers within one square millimeter. It is important the upper layer shielding common electrodes will not be positioned at the area where the spacer is projected. The height h2 of the spacers 78 constructed on the bump 77 must be able to deform in the range of 0,2-0.5 micrometers, when a pressure is applied from the atmosphere during a liquid crystal injection vacuum attachment alignment process. If the spacer 78 is: covered by the upper layer shielding common electrode 79, a problem may arise where the deformation of the spacer 78 by the atmospheric pressure causes the upper layer shielding common electrodes to peel off.

[0056] Examples of material used for forming the upper layer shielding common electrodes 79 include conductive material with visible light transmission of 20 percent or more such as titanium metal compound including titanium nitride (TiNx), titanium oxide nitride (TiOxNy), titanium silicide (TiSix), titanium silicide nitride (TiSixNy), or metal oxide transparent conductive material mainly composed of indium oxide (In_2O_3) or zinc oxide (ZnO).

[0057] As shown in Figure 104, similar to the first embodiment described above, it is important to have the taper angle θ at an edge portion of the bump 77 to be as small as possible. Ordinarily this taper angle θ should be set to less than 30 degrees. By keeping the taper angle small, movements of the tips of the rubbing cloth hair can be performed smoothly during the rubbing alignment treatment process, which eliminates alignment defects. When the taper angle θ is larger than 45 degrees, instances occur where the tips of rubbing cloth hairs cannot make contact with the surface around the tapered area and may result in areas of alignment defects. If such alignment defects occur, such an area causes light to

leak during the black display, which seriously lowers the contrast of the display. Structures disclosed by Japanese patent laid-open publication numbers 2002-258321 and 2002-323706 do not allow for smooth movements of the tips of the rubbing cloth hairs, therefore, instances occur where the tips of the rubbing cloth hairs cannot reach around the tapered area and cannot completely prevent the occurrence of alignment defects.

[0058] As shown in Figure 77 the shape of the spacer does not have to be circular but can be an oval shape. In the example of Figures 79 and 81, the shape of the spacer is circular. When the spacer 78 is provided over the bump 77 that covers the video signal line as in the present invention, it is possible to construct the bump 77 at the intersecting points of the scanning lines 15 and the video signal line 51 since there is nothing to obstruct the diffusion of the liquid crystal during the liquid crystal injection vacuum attachment and alignment process. It is also possible to construct the bumps 77 on top of the scanning lines as shown in Figures 79 and 81 so that the bumps are arranged in a mesh like fashion throughout the substrate. When the upper layer shielding common electrode 72 completely covers or overlaps the video signal line 51 and scanning line 15 through the bump 77, the light shielding film on the color filter substrate side becomes unnecessary, which can increase the aperture ratio to the maximum level.

[0059] As shown in the example of Figure 81, the structure in which the upper layer shielding common electrodes 79 are constructed on both side walls of the bump 77 that covers the scanning line 15 and on both side walls of the bump 77 that covers the video signal line 51 is best suited for an ultra large screen liquid crystal display device. This is because this structure can minimize the distortion in the video signal line waveforms and the scanning line waveforms.

[Preferred embodiment 4]

[0060] Figures 54, 55 and 56 are the cross sectional views showing the structures of the transverse electric field type liquid crystal panel in the fourth embodiment of the present invention. This structure is basically the same as that of the second embodiment described above except that the spacer bump 73 of the second embodiment is separated into an insulation bump 77 that covers the video signal line and a spacer 78 that determines the liquid crystal cell gap.

[0061] In the second embodiment noted above, the dielectric (insulation) bump 73 that covers the video signal line 51 also functions as a spacer to determine the cell gaps. In the fourth embodiment, however, as in the third embodiment, the functions of the dielectric (insulation) bump 77 that covers the video signal line and the spacer 78 that determines the liquid cell gap are completely separated. The dielectric bump 77 of the third embodiment and fourth embodiment can completely cover the scanning line 15 and the video signal line 51. Therefore, by constructing an upper layer shielding common electrode 79 on both side walls of the insulation bump 77, it is possible to keep the distortion of signal waveform by the video signal line 51 and the scanning lines to the minimum level, and thus, achieve the maximum aperture ratio.

[0062] The spacer 78 shown in Figures 54, 55, and 56 are not covered by the upper layer shielding common electrodes 79 so that the dielectric material is projected by itself. This structure is advantageous in that the common electrode layer does not peel off when the pressure from the atmosphere is applied during liquid crystal injection vacuum attachment alignment process.

[0063] As has been described in the foregoing, in the structures of the first through fourth embodiments, the video signal line 51 and the liquid crystal drive electrode 53 are completely covered by the gate insulation layer 9 and the passivation layer 55 in the up and down directions. Further, the video signal line and the liquid crystal drive electrode are provided on the layer different from that of the shielding common electrodes and the common electrodes within the pixel. Therefore, even when a pattern fault occurs, the possibility of shorting each other becomes unlikely, thereby minimizing the possibility of pixel defect.

[Preferred embodiment 5]

[0064] Figures 57, 58 and 59 are cross sectional views showing the structures of the transverse electric field type liquid crystal panel in the fifth embodiment of the present invention. In this embodiment, the video signal line 51 and the liquid crystal drive electrode 53 are not covered by the passivation layer 55 unlike the first to fourth embodiments. Only the video signal line 51 is covered by the dielectric spacer bump 73. According to the present invention, the video signal line 51 and the liquid crystal drive electrode 53 can be constructed at the same time. Alternatively, the drain electrode of the thin film transistor can be constructed with the video signal line 51 at the same time and then the liquid crystal drive electrode 53 can be constructed simultaneously with the upper layer shielding electrode 72 and the common electrode 74 within the pixel at the same time after the construction of the spacer bump 73. Either construction method is applicable to the fifth embodiment. With the structure of the present invention, there is no need for opening a contract hole to connect the drain electrode of the thin film transistor with the liquid crystal drive electrode.

[Preferred embodiment 6]

[0065] Figures 60, 61 and 62 are cross sectional views showing the structures of the transverse electric field type liquid crystal panel in the sixth embodiment of the present invention. As with the fifth embodiment, the video signal line 51 and the liquid crystal drive electrode 53 are not covered by the passivation layer 55 unlike the first to

fourth embodiments. Only the video signal line 51 is covered by the dielectric spacer bump 73. The sixth embodiment is different from the fifth embodiment only in that the common electrode 49 within the pixel is constructed simultaneously with the scanning line and the lower layer shielding common electrode 75 on the same layer.

[Preferred embodiment 7]

[0066] Figures 63, 64 and 65 are cross sectional views showing the structures of the transverse electric field type liquid crystal panel in the seventh embodiment of the present invention. This structure is basically the same as that of the fifth embodiment except that the spacer bump 73 is separated into the dielectric (insulation) bump 77 that covers the video signal line and the spacer 78 that determines the liquid crystal cell gap.

[Preferred embodiment 8]

[0067] Figures 66, 67 and 68 are cross sectional views showing the structures of the transverse electric field type liquid crystal panel in the eighth embodiment of the present invention. This structure is basically the same as that of the sixth embodiment except that the spacer bump 73 is separated into the dielectric (insulation) bump 77 that covers the video signal line and the spacer 78 that determines the liquid crystal cell gap.

[Preferred embodiment 9]

[0068] Figures 108, 109, 110 show the sectional view and plan view of the transverse electric field type liquid crystal panel of the ninth embodiment which is not a part of the present invention. In the example of Figures 108, 109 and 110, a numeral 90 denotes a liquid crystal drive electrode. As noted above with reference to Figures 45-47, a numeral 9 denotes a gate insulation film, a numeral 51 denotes a video signal line, a numeral 53 denotes a liquid crystal drive electrode, a numeral 55 denotes a passivation film, a numeral 66 denotes a glass substrate in the side of color filter, a numeral 67 denotes a black mask (light shielding film), a numeral 68 denotes a color filter layer, a numeral 69 denotes a leveling layer in the side of color filter, a numeral 70 denotes an alignment film in the side of color filter, a numeral 71 denotes an alignment film in the side of TFT array substrate, a numeral 72 denotes an upper layer common electrode, a numeral 73 denotes a spacer bump covering the video signal line, a numeral 74 denotes a common electrode within the pixel, a numeral 75 denotes a lower layer common electrode, and a numeral 76 denotes a glass substrate in the side of TFT array.

[0069] In the embodiment of Figures 108-110, the video signal line 51 and the liquid crystal drive electrodes 90 are constructed on a different layer relative to the passivation layer 55. The upper layer shielding common electrodes 72 and the common electrode 74 within the pixel and the liquid crystal drive electrode 90 are constructed on the same layer at the same time. The liquid crystal drive electrode 90 is connected to the drain electrode of the thin film transistor through the contact hole.

[0070] The ninth embodiment is most effective in leveling (flattening) the irregularity in the areas around the display pixels. By forming the upper layer shielding common electrodes 72, the common electrode 74 within the pixel, and the liquid crystal drive electrode 90 at the same time with use of the transparent electrode material (ITO or IZO) with a thickness of 300-500 angstroms, it is possible to dramatically increase the effective aperture ratio. In the transverse electric field mode, when the width of the electrode is small such as about 3-5 micrometers, it is possible for a majority of the liquid crystal molecules above the electrode to rotate because of a fringe field effect so that the light can transmit from the areas around the electrode. Because of this fringe field effect, the structure shown in Figure 109 is most effective in improving the aperture ratio, thereby achieving the display with high contrast.

[0071] With the structures shown in Figures 109 and 110, the fringe field effect is also effective around the edge areas of the upper layer shielding common electrode 72, which promotes the light transmission around the edge areas of the upper layer shielding common electrode 72, thereby improving the aperture ratio. The black mask 67 provided on the side of the color filter substrate is not essential to the structure of this embodiment. It is preferable that the width of the black mask 67 is the same as that of the dielectric spacer bump 73 or slightly smaller. It is important to keep the taper angle θ of the spacer bump 73 to be less than 30 degrees to prevent occurrences of alignment defects in the rubbing alignment treatment.

[0072] It is preferable that the spacer bump is not formed at the intersection area of the scanning line and the video signal line so that the liquid crystal can smoothly diffuse during the liquid crystal injection vacuum attachment alignment process. A problem of residual air bubble can occur if the spacer bump 73 is not fabricated by material that allows the spacer bump to deform 0.1-0.5 micrometers when a pressure from the atmosphere is applied thereto.

[Preferred embodiment 10]

[0073] Figures 111, 112 and 113 are cross sectional views and Figure 115 is a plan view, respectively, showing the structures of the transverse electric field type liquid crystal panel in the tenth embodiment which is not a part of the present invention. This structure is basically the same as that of the ninth embodiment except that the spacer bump 73 of the ninth embodiment is separated into an insulation (dielectric) bump 77 that covers the video signal line and a spacer 78 that determines the liquid crystal cell gap.

[0074] As shown in Figure 115, the upper layer shield-

ing common electrodes 72, the common electrode 74 within the pixel, and the liquid crystal drive electrode 90 are produced on the same layer at the same time. The liquid crystal drive electrode 90 is connected to the drain electrode of the thin film transistor though a contact hole 93. The upper layer shielding common electrode is not provided above the spacer 78. The upper layer shielding common electrodes 72 are connected to each other on the scanning lines in up/down and right/left directions in a mesh like fashion. In Figure 115, the upper layer shielding common electrode 72 covers the video signal line 51 almost completely. It is also possible to form the upper layer shielding common electrode on the side walls of the dielectric bump 77 such as the one shown in Figure 81. In an application of a large screen liquid crystal display panel of 30 inches or larger, the construction in which the upper layer shielding common electrodes are placed at the side walls are preferred because this structure is able to decrease the distortion in the video signal line waveforms.

[Preferred embodiment 11]

[0075] Figures 69-81 and Figure 115 are plan views showing the structure of the transverse electric field type liquid crystal display panel in the eleventh embodiment of the present invention. In this structure, the video signal line 51, the upper layer shielding common electrode 72, the common electrode 74 within the pixel and the liquid crystal drive electrode 90 are bent within a pixel at least once at an angle within 0-30 degrees except 0 degree with respect to the alignment direction of the liquid crystal molecules. In the eleventh embodiment, positive dielectric constant anisotropic liquid crystals are used in which the alignment direction of the liquid crystal molecules is almost perpendicular to the direction of the scanning lines.

[0076] Figure 120 is a schematic diagram showing the relationship between the alignment direction and the rotation direction of the liquid crystal molecules of positive anisotropic dielectric material used in the transverse electric field type liquid crystal panel of the present invention. In Figure 120, a numeral 97 denotes an alignment direction of the liquid crystal molecule, a numeral 98 denotes a positive dielectric constant anisotropic liquid crystal molecule, and a numeral 105 denotes an angle between the pixel electrode (liquid crystal drive electrode 53) and the alignment direction of the crystal molecule 98. As shown in Figure 120, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time.

[0077] Figure 121 is a schematic diagram showing the relationship between the alignment direction and the rotation direction of the liquid crystal molecules of negative anisotropic dielectric material used in the transverse electric field type liquid crystal panel of the present invention. In Figure 121, a numeral 97 denotes an alignment direction of the liquid crystal molecule, a numeral 99 denotes a negative dielectric constant anisotropic liquid crystal molecule, and a numeral 106 denotes an angle between the pixel electrode (liquid crystal drive electrode 53) and the alignment direction of the crystal molecule 99.

[0078] As shown in Figure 121, by using the negative dielectric constant anisotropic liquid crystal with the alignment direction of the liquid crystal molecules in parallel with the direction of the scanning lines, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time. In the arrangement of Figure 121, the video signal line, the liquid crystal drive electrode, the common electrodes within the pixel, and the upper layer common electrode are bent at least once at an angle between 60 degrees and 120 degrees except 90 degrees, with respect to the alignment direction of the liquid crystal molecule in a given pixel.

[preferred embodiment 12]

[0079] Figures 82, 84, 92, 93, 94 and 95 are plan views showing the structure of the transverse electric field type liquid crystal panel in the twelfth embodiment of the present invention. In this structure, the video signal line is straight while the upper layer shielding common electrode, common electrode within the pixel, and the liquid crystal drive electrode are bent within a pixel at least once at an angle within a range between 0-30 degrees except 0 degree with respect to the alignment direction of the liquid crystal molecules. In the twelfth embodiment, positive dielectric constant anisotropic liquid crystals are used in which the alignment direction of the liquid crystal molecules is substantially perpendicular to the direction of the scanning line. As shown in Figure 120, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time.

[0080] In the twelfth embodiment, as shown in Figure 121, by using the negative dielectric constant anisotropic liquid crystals with the alignment direction of the liquid crystal molecules in parallel with the direction of the scanning lines, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time. In the arrangement of this embodiment, the liquid crystal drive electrode, the common electrodes within the pixel, and the upper layer common electrode are bent at least once at an angle between 60 degrees and 120 degrees except 90 degrees, with respect to the alignment direction of the liquid crystal molecule in a given pixel.

[Preferred embodiment 13.]

[0081] Figures 83, 85, 88, 89, 90, 91, 96 and 97 are plan views showing, the structure of the transverse electric field type liquid crystal panel in the thirteenth embod-

iment of the present invention. In this structure, as to one pixel, the video signal line and the upper layer shielding common electrode are straight while the common electrode within the pixel and the liquid crystal drive electrode are bent at least once at an angle within a range between 0-30 degrees except 0 degree with respect to the alignment direction of the liquid crystal molecules. In the thirteenth embodiment, positive dielectric constant anisotropic liquid crystals are used in which the alignment direction of the liquid crystal molecules is substantially perpendicular to the direction of the scanning line. As shown in Figure 120, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time.

[0082] In the thirteenth embodiment, as shown in Figure 121, by using the negative dielectric constant anisotropic liquid crystal with the alignment direction of the liquid crystal molecules in parallel with the direction of the scanning lines, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time. In the arrangement of this embodiment, the liquid crystal drive electrode and the common electrode within the pixel are bent at least once at an angle between 60 degrees and 120 degrees except 90 degrees, with respect to the alignment direction of the liquid crystal molecule in a given pixel.

[Preferred embodiment 14]

[0083] It is also possible that the video signal line, the upper layer shielding common electrode, and the common electrode within the pixel are straight while only the liquid crystal drive electrode is bent at least once at an angle within a range 0-30 degrees except 0 degree with respect to the alignment direction of the liquid crystal molecule. In this arrangement, positive dielectric constant anisotropic liquid crystals, are used in which the alignment direction of the liquid crystal molecules is substantially perpendicular to the direction of the scanning line. As shown in Figure 120, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time.

[0084] In the fourteenth embodiment, as shown in Figure 121, by using the negative dielectric constant anisotropic liquid crystal with the alignment direction of the liquid crystal molecules in parallel with the directions of the scanning lines, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time. In this arrangement, only the liquid crystal drive electrode is bent at least once at an angle between 60 degrees and 120 degrees except 90 degrees, with respect to the alignment direction of the liquid crystal molecule in a given pixel.

[Preferred embodiment 15]

[0085] With respect to the structure described in the above regarding the eleventh embodiment, it is also possible that the common electrode within the pixel is obviated and only one line of liquid crystal drive electrode exists within a pixel, and further, the video signal line, the upper layer shielding common electrode, and the liquid crystal drive electrode are bent at least once at an angle within a range 0-30 degrees except 0 degree with respect to the alignment direction of the liquid crystal molecules. As shown in Figure 120, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time. In this arrangement, positive dielectric constant anisotropic liquid crystals, are used in which the alignment direction of the liquid crystal molecules is substantially perpendicular to the direction of the scanning line. The fifteenth embodiment is suited for the production of super high resolution display device with a pixel pitch of 50 micrometers or smaller.

[0086] In the fifteenth embodiment, as shown in Figure 121, by using the negative dielectric constant anisotropic liquid crystal with the alignment direction of the liquid crystal molecules in parallel with the direction of the scanning lines, the liquid crystal molecules are able to rotate in the right and left directions, which contributes to increase the viewing angle while decreases the color shift at the same time. In this arrangement, the video signal line, the upper layer shielding common electrode, and the single line of the liquid crystal drive electrode are bent at least once at an angle between 60 degrees and 120 degrees except 90 degrees, with respect to the alignment direction of the liquid crystal molecule in a given pixel.

[0087] In the structure of the color filter substrate used in the eleventh and fifteenth embodiments, as shown in Figures 122 and 123, the light shielding film (black mask) 101 and the color filter layer 68 are bent in a similar manner to the video signal line. More particularly, the black mask 100 that covers the scanning line is straight and the black mask 101 covers the video signal line is bent as noted above. According to the present invention, the spacer bump and the bump covering the video signal line are also bent similarly to the vide signal line. In the case where the upper layer shielding common electrode covers the video signal line completely, the light leakage will not occur even when the black mask corresponding to the video signal line is not used, thus it is possible to eliminate the black mask. When the upper layer shielding common electrodes covers both the video signal line and the scanning lines completely, the light leakage will not occur even when the black mask is not used, thus, it is sufficient that only the color filter is bent similarly to the video signal line.

[Preferred embodiment 16]

[0088] Figure 119 shows a cross sectional view and a

plan view of the transverse electric field type liquid crystal panel in the sixteenth embodiment of the present invention. In Figure 119, a numeral 66 denotes a glass substrate in the side of color filter, a numeral 67 denotes a black mask (light shield film), a numeral 68 denotes a color filter layer, a numeral 69 denotes a leveling layer in the side of the color filter, a numeral 70 denotes an alignment film in the side of the color filter, a numeral 71 denotes an alignment film in the side of TFT array substrate, a numeral 76 denotes a glass substrate in the side of TFT array, a numeral 78 denotes a spacer formed on the bump covering the video signal line, a numeral 94 denotes a photolithography spacer having a ring shape, a numeral 95 denotes a photolithography spacer having a circular shape, a numeral 96 denotes a main seal for forming the liquid crystal cell.

[0089] The spacer bump 94 having a closed loop shape is formed at the position that overlaps the boarder of the black mask (light shielding film) that surrounds the outer most display area. The width of 1000-500 micrometers will be sufficient for the spacer bump 94, although the width of the spacer bump should not be too small. Figure 119 only shows one closed looped spacer bump 94, however, two or more of them can also be incorporated. In the area of the main seal 96, many spacer bumps 95 having a circular shape are provided. By utilizing the structure of the present invention, glass fibers that determine the cell gap does not need to, be introduced. Because the glass fibers are not mixed therein, this structure can prevent; the occurrence of line breakage even when the video signal line and the scan lines are fabricated by soft material such as aluminum alloy. Further, by utilizing the structure of the present invention, the main seal does not invade the areas of the black mask, thus, the main seal can be completely hardened by ultraviolet rays. In this structure, since the spread of impurities from the main seal can be effectively suppressed, it is able to improve the reliability.

[Preferred embodiment 17]

[0090] Figures 32, 33, 34, 35 and 106 show the transverse electric field type liquid crystal panel in the seventeenth embodiment of the present invention. Figures 32A-32E and 35A-35E are plan views and cross sectional views showing the principle of the halftone shift exposure method of the present invention and the structure of the photoresist after the development. Figures 33A-33B and 34A-34B are plan views showing other examples of the halftone shift exposure method of the present invention. Figures 106A-106F are cross sectional views showing the production flow involved in the four-step photomasking process using the halftone shift exposure method of the present invention.

[0091] In Figures 32A-32E and 35A-35E, a numeral 1 denotes a silica glass substrate forming a photomask, a numeral 2 denotes a metal layer (opaque mask pattern) on the glass substrate 1, a numeral 19 denotes a UV light, a numeral 20 denotes an area on the positive photoresist layer after development where the UV light exposure is completely blocked, a numeral 21 denotes an area where the photoresist is completely removed, a numeral 22 denotes an area on the positive photoresist layer after development where the UV light exposure is made through the under exposure (incomplete exposure) step, and a numeral 62 denotes an area on the photoresist which has been exposed in the first under exposure step, and a numeral 63 denotes an area on the photoresist which has been completely exposed through both the first and second under exposure steps.

[0092] In the present invention, as shown in Figure 32A, the mask pattern 2 is designed to have a gap 1 between a source electrode and a drain electrode where a gap distance 1 is equal to a half of the channel length of the thin film transistor. That is, if the channel length of the thin film transistor is desired to be 6 micrometers, the gap distance 1 of 3-micrometers is used to create the source electrode and the drain electrode. By using an ordinary photomask, a first exposure step is conducted for the positive resist by an under exposure (incomplete exposure) process as shown in Figure 32B. Then, in Figure 32C, either the photomask or the glass substrate is shifted horizontally (X direction) by a distance equal to or slightly larger than the gap distance 1 between the source electrode and the drain electrode. Then, a second exposure step is conducted as shown in Figure 32D by the same degree of under exposure as that of the first exposure step.

[0093] Because the positive photoresist is not completely exposed by the UV light in the first exposure since it is the under exposure process, the photoresist layer underneath the area 62 shown in Figure 32B remains after the development. Further, because the under exposure step is repeated two times as noted above, the area 63 of the photoresist shown in Figure 32D which has experienced the under exposure by two times is completely exposed and removed after the development. Thus, when the development is done, the positive photoresist with the cross sectional shape shown in Figure 32E can be achieved.

[0094] Figures 33A-33B and Figures 34A-34B show similar concepts. In the example of Figures 33A-33B, either the photomask or the glass substrate is' shifted horizontally (Y direction) by a distance equal to the gap distance 1 between the source electrode and the drain electrode. In the example of Figures 34A-34B, either the photomask or the glass substrate is shifted in two horizontal directions (both X and Y directions) by a distance Δx and Δy, each being equal to the gap distance 1 or slightly larger than the gap distance 1 between the source electrode and the drain electrode.

[0095] In the example of Figures 35A-35E, a thin pattern is provided in the gap between the source electrode and the drain electrode of the photomask. The pattern width L of the thin pattern and a gap distance 1 between the thin pattern and either the source electrode or drain

electrode have a relationship of L<1. It is preferable that the gap distance l is slightly larger than the pattern width L for the under exposure process. Similar to the example of Figures 32A-32E, after the first under exposure process, either the photomask or the glass substrate is shifted by a distance equal to or slightly larger than the gap distance l, the second under exposure process is conducted.

[0096] When the development is done, the positive photoresist with the cross sectional shape shown in Figure 35E can be achieved. Preferably, the amount of shift distance and the amount of exposure are adjusted so that the channel area of the thin film transistor becomes as flat as possible. Further, it is preferable that the shift distance and the exposure amount are adjusted so that, in Figures 32E and 35E, the thickness of the area 20 of the positive photoresist that has not been exposed is 1.5-2.5 micrometers and the thickness of the half exposed area (under exposed area) 22 on the positive photoresist is 0.2-0.5 micrometers.

[0097] Figures 106A-106F are cross sectional- views showing the process for.*producing.the thin film transistors elements using the halftone shift exposure method of the present invention. In Figures 106A-106F, a numeral 6 denotes an area -on a positive photoresist layer after development where UV exposure is blocked, a, numeral 7 denotes an area on the positive photoresist layer after development where the W exposure is made through the halftone shift exposure (under exposure), i a. numeral 9 denotes a gate insulation film, a. numeral 10 denotes a thin film semiconductor layer (non-doped layer), a numeral 11 denotes a thin film semiconductor layer . (doped layer, i.e., ohmic contact layer), a numeral 15 denotes a scanning line, a numeral 50 denotes a scanning line terminal, a numeral 51 denotes a video signal line, a numeral 54 denotes a scanning line terminal drive circuit contact electrode, a numeral 64 denotes a drain electrode, and a numeral 65 denotes a transparent pixel electrode.

[0098] In this example, the production process utilizes four photomasking steps. The processes for producing a thin film resistor using the light transmission adjustment photomask with the halftone exposure is shown in Figures. 36A-36F. The process of Figures 106A-106F involves a process of shifting the exposure position by moving either the photomask or glass substrate. Although the overall process is similar to that of Figures. 36A-36F, the process of Figures 106A 106F achieve the halftone exposure without using the light transmission adjustment photomask (halftone photomask).

[0099] Prior to the start of the process of Figures 106A-106F, the scanning lines 15 and the scanning terminals 50 are formed on a TFT array glass substrate (not shown), which can be done by a process shown in Figures 7A-7E or Figures 8A-8E as will be explained later. In Figure 106A, the gate insulation film 9, the thin film semiconductor layer (non-doped layer) 10 and the thin film semiconductor layer (ohmic contact layer) 11 are respectively deposited by, for example, a CVD plasma device. The positive photoresist 6 is coated and the halftone shift exposure (under' exposure) using the ordinary photomask is conducted in the manner described with reference to Figures 32A-32E, 33A-33B, 34A-34B and 35A-35E so that the thicker positive photoresist 6 and the thinner positive photoresist 7 are created.

[0100] In Figures 106B and 106C, through a dry etching process and plasma ashing process, the silicon elements for the thin film transistors are separated from the semiconductor layer.

[0101] In Figure 106D, the drain electrode 64 of the thin film transistor and the video signal line 51 are formed by further conducting the etching process. In Figure 106E, through the dry etching, contact holes are created over the scanning line terminals 50. In Figure 106F, the scanning line drive circuit electrodes 54 and the transparent pixel electrodes 65 are formed.

[0102] In this embodiment, the passivation coverage is improved because the edge portions of the thin film semiconductor layer are formed in a step like shape. The conventional light transmission adjustment photomask is expensive, and is not practical for an ultra large screen liquid crystal television. However, as noted above, the halftone shift exposure method of the present invention can be conducted with use of inexpensive ordinary photomasks.

[0103] The seventeenth embodiment of the present invention noted above can be applied not: only to the liquid crystal display device. For example, the present invention is also applicable to the production processes of organic EL (electro-luminescence) display devices or active matrix substrates for X ray detectors, which can dramatically the production cost.

[0104] Figures 17 and 19 show an example of a scan exposure device that can be used in the halftone shift exposure process of the seventeenth embodiment. Figure 17 is a plan view showing the structure of the scanning exposure device used in the multi-lens scanning exposure system for implementing the seventeenth embodiment of the present invention, and Figure 19 is a cross sectional view showing the scanning exposure.device of Figure 17. In Figures 17 and 19, a numeral 19 denotes a UV light, a numeral 44 denotes a multi-lens exposure module, a numeral 45 denotes an ordinary photomask, a numeral 46 denotes an X-Y stage, and a numeral 48 denotes an optical fiber cable.

[0105] When the glass substrate is large, if the photomask of the same size as that of glass substrate is used, the overall cost becomes too high. Thus, in such a case, the photomask 45 which is smaller than the glass plate is used which is shifted in X and Y directions by driving the X-Y stage 46. Since the scanning exposure device of Figures 17 and 19 has a plurality of exposure lens arranged in a row, by scanning the exposure lens, it is possible to expose the glass substrate of any size.

[0106] The ordinary photomask 45 is a photomask which has no function of adjusting the light transmission

unlike the photomask (halftone photomask) 1 of Figures 1A and 2A. In the halftone shift exposure method of the present invention, the photomask 45 can be shifted or the substrate on the X-Y stage: 46 can be shifted. - The halftone shift exposure method can also be implemented by using a mirror projection scan exposure device. The multi-lens scan exposure device shown in Figures 17 and 19 is suitable for the halftone shift exposure method of the present invention because the resolution of the positive photoresist can be improved. With the conventional technology using the light transmission adjustment photomask; the halftone exposure method using the mirror projection scan exposure device with lower resolution is more suited.

[Preferred embodiment 18]

[0107] Figures 13-16, 18 and 20 show examples of scanning exposure device without using a photomask in accordance with the eighteenth embodiment of the present invention. Figure 13 shows a structure of the titler optical system (inverted real image) for the ultraviolet ray exposure method using a micro mirror array; Figure 14 shows a structure of the multi-lens optical system (non-inverted real image) for the ultraviolet ray exposure method using a micro mirror array, Figure 15 is a plan view showing the structure of the multi-lens scanning exposure system, Figure 16 is a timing chart for explaining the operation of the micro mirror array for the ultraviolet light transmission adjustment by time width control, Figure 18 is a plan view showing the scanning exposure device used in the direct halftone exposure method without using a photomask, and Figures 20A and 20B show the principle of the direct halftone exposure of the present invention using the exposure device of Figure 18

[0108] In Figures 13-16, 18 and 20, a numeral 19 denotes a UV light, a numeral 20 denotes an area on the positive photoresist layer after development where the UV light exposure is completely blocked, a numeral 21 denotes an area where the photoresist is completely exposed, a numeral 22 denotes an area on the positive photoresist layer after development where the UV light exposure is made through the halftone exposure process, a numeral 37 denotes a projection lens, a numeral 38 denotes a glass substrate for TFT array, a numeral 39 denotes a positive photoresist layer, a numeral 40 denotes a micro mirror array device (DMD module), a numeral 41 denotes a micro mirror, a numeral 42 denotes a time length during which the micro mirror 41 is in operation, a numeral 43 denotes a time length for rewriting the data during which the micro mirror 41 is not in operation, a numeral 44 denotes a multi-lens projection exposure module (non-inverted real image), a numeral 46 denotes an X-Y stage, and a numeral 47 denotes a UV light source.

[0109] In the eighteenth embodiment, the scanning exposure device includes a plurality of reflective mirror devices 40 which are arranged in a checker board manner where each mirror device has micro-mirrors formed in a two dimensional manner. As noted above, the scanning exposure device of the present invention does not require the photomask for producing the pattern on the glass substrate. The UV light 19 from the light source 47 is reflected by the micro-mirrors 41 on the micro-mirror array device 40 in the exposure system of Figure 14. In the exposure system of Figure 15, the UV light 19 passes through the multi-lens projection exposure module 44 which produces a non-inverted real image and projects the image on the positive photoresist 39 on the glass substrate 38. Thus, the photoresist 39 is exposed by the UV light 19 for the image produced by the projection exposure module 44. In the exposure systems of Figures 14, 15 and 18, the degree of UV light applied to the photoresist 39 is regulated by the time lengths as shown by the timing chart of Figure 16.

[0110] AS shown in the time chart of Figure 16, the movement of the micro mirrors 41 can be controlled one by one. By using this reflective mirror device to alter the exposure timing of the UV ray to the positive photoresist, a multi-level halftone exposure method such as shown in Figures 20A-20B can be performed. As described above, in the eighteenth embodiment, it is possible to easily conduct the multi-level halftone exposure method for a large area without using the expensive light transmission adjustment (halftone) photomask.

[0111] The major difference between the optical system of Figure 13 and the optical system of Figure 14 resides in that the optical system of Figure 13 involves the inverted real image while the optical system of Figure 14 involves the non-inverted real image. The optical system of Figure 13 may be sufficient for use as a titler for locally exposing a simple image such as text data. However, for a scanning exposure system to expose the complicated patterns on the substrate, the optical system of non-inverted real image such as the one shown in Figure 14 must be used for producing fine and accurate patterns on the substrate.

[Preferred embodiment 19]

[0112] Figures 37A-37B and Figures 43A-43B show nineteenth embodiment of the present invention. Figures 37A-37B are plan views showing an example of principle of the halftone shift exposure method of the present invention. Figures 43A-43B are plan view showing a further example of principle of the two-step exposure method of the present invention. More particularly, Figures 37A-37B and Figures 43A-43B show the structure of an ordinary photomask for producing the scanning line, the lower layer shielding common electrode and the common electrode within the pixel by the halftone shift exposure method in the seventeenth embodiment described above. Figures 37A-37B and Figures 43A-43B also show the distribution of the amount of light exposed during the half shift exposure process.

[0113] In this exposure process, a first under exposure

step is conducted with use of an ordinary photomask. After the first under exposure, the photomask is shifted in parallel with the scanning line by the distance equal to the width of the common electrode. Then, the second under exposure step is conducted preferably with the same amount of light as that of the first exposure step. After the development, there remains an area having a thick positive photoresist, an area having a thin positive photoresist, and an area having no positive photoresist.

[0114] Figures 7A-7E and Figures 8A-8E are cross section views showing the processes to create electrodes of two different thicknesses using the halftone shift exposure method. Metals or alloys that can be selectively etched are constructed in two or three layers and two different thickness of positive photoresist are constructed using the halftone shift exposure of the present invention to construct a non-exposed area 20 and an incompletely exposed area 22 (Figures 32E and 35E) . With use of the etching and ashing process for the positive photoresist and selective etching technology, the electrodes having two different thickness are produced.

[0115] The process shown in Figures 7A-7E and 8A-8E will be repeated for forming electrodes, on different layers on the TFT array glass substrate. For example, the process of Figures 7A-7E and 8A-8E precedes the process of Figures 106A-106F described above so that the process of Figures 106A-106F starts after creating the scanning line 15 and scanning line terminal 50. In Figures 7A-7E and Figures 8A-8E, a numeral 26 denotes lower electrode material, a numeral 27 denotes low resistance electrode material, a numeral 28 denotes an upper electrode material. As noted above, a numeral 20 denotes an area of the photoresist which is not exposed by the UV light, and a numeral 22 denotes an area of the photoresist which is incompletely exposed (halftone exposure).

[0116] In the process of Figures 7A-7E and Figures 8A-8E, the lower electrode material (barrier metal) 26 is incorporated because it is not possible to directly connect the doped semiconductor n+a-Si layer to pure aluminum or aluminum alloy. An example of material for the barrier metal is titanium (Ti). An alloy of titanium and molybdenum or an alloy of molybdenum and tungsten is also possible for the barrier metal. In the case of using an aluminum alloy for the electrode material 27, the structure of Figure 7A will be sufficient since there arise no problem in direct connection with ITO (indium tin oxide).

[0117] However, when the low resistance electrode material 27 is configured by pure aluminum, there arises a problem of contact defect because aluminum oxide is formed at the contact surface. To overcome this problem, the upper electrode material 28 is formed as shown in Figure 8A. An example of material for the upper electrode 28 is molybdenum. Therefore, the basic difference between the examples of Figures 7A-7E and Figures 8A-8E is that the example of Figures 8A-8E includes the upper electrode material 28 additionally, although the remaining production process is the same.

[0118] In the example of Figures 7A-7E, two metal layers are formed on the substrate, one is the lower electrode layer 26 and the other is the low resistance electrode layer 27. For example, the lower electrode layer 26 is made of titanium (Ti) and the low resistance electrode layer 27 is made of aluminum neodymium nickel (Al-Nd-Ni) or aluminum carbon nickel (Al-C-Ni). In Figure 7A, through the (halftone shift exposure method, for example, the positive photoresist of two different thickness areas 20 and 22 are created.

[0119] Then, as shown in Figure 7B, the low resistance electrode layer 27 is etched through a wet etching process and the lower electrode layer 26 is etched through a dry etching process. Then, in Figure 7C, the thinner photoresist area 22 is removed through, for example, a dioxide plasma ashing process while leaving the thicker photoresist area 20. The wet etching process is performed again for the low resistance electrode layer 27 as shown in Figure 7D. Lastly, the positive photoresist is completely removed through the ashing process as shown in Figure 7E.

[0120] In the example of Figures 8A-8E, three metal layers are formed on the substrate; the first one is the lower electrode layer 26, the second one is the low resistance electrode layer 27, and the third one is the upper electrode layer 28. For example, the lower electrode layer 26 is made of titanium (Ti), the low resistance electrode layer 27 is made of pure aluminum (A1), and the upper electrode layer 28 is made of molybdenum (Mo) In Figure 8A, through for example, the halftone shift exposure method, the positive photoresist of two different thickness areas 20 and 22 are created. The process of Figures 8A-8E are the same as that of Figures 7B-7E, thus the explanation thereof is omitted here.

[0121] In performing the halftone shift exposure method of the present invention, the first exposure and the second exposure use the same photomask for producing the scanning: line, shielding common electrode, and common electrode within the pixel. Thus, in determining the positions of the first exposure and the second exposure, it is only necessary to: shift the photomask by a small horizontal movement in one direction. In other words, there is no need to construct an alignment mark on the glass substrate for positioning two different photomasks since only one photomask has to be used. Therefore, it is possible to reduce the time and cost in the production process.

[Preferred embodiment 20]

[0122] Figures 38A-38B, 39A-39B, 40A-40B, 41A-41B and 44A-44B show example of distribution of light exposure when the halftone shift exposure method in the twentieth embodiment of the present invention is conducted with use of two or more ordinary photomasks, i.e, without using the light transmission adjustable photomask (halftone photomask) such as shown in Figures 1A and 2A. This example shows the case where the halftone shift

exposure method of the present invention is applied to the production process of the scanning lines and the shielding common electrodes. In implementing this method, one or more alignment marks need to be provided inside the glass substrate since the first exposure and the second exposure use photomasks different from one another.

[0123] Figure 9 shows a device that directly writes alignment marks in the glass substrate. Figure 10 shows the principle underlining the device of Figure 9 for writing the alignment marks inside the: glass substrate. In Figure 11, the alignment marks are formed on the areas outside the metal deposition for construction of the scanning lines and the shielding common electrodes. In Figures 9, 10 and 11, a numeral 25 denotes an fθ lens, a numeral 29 denotes a laser light source, a numeral 30 denotes a beam formatter, a numeral 31 denotes a galvanomirror, a numeral 32 denotes a laser beam, a numeral 33 denotes a mark pattern formed within the glass substrate, and a numeral 38 denotes the glass substrate for TFT array. The laser marking utilized in the present invention is disclosed in more detail in Japanese patent laid-open publication No. 11-267861. It is important to form the alignment marks inside the glass substrate rather than the surface of the glass substrate for improving the production efficiency.

[0124] In this embodiment, with use of the different photomasks for the first and second under exposure steps, the positive photoresist pattern of two different thickness will be created after the development. Through the processes shown in Figures 7A-7E and Figures 8A-8E as noted above, the metal electrodes with two levels of thickness will be produced by etching, ashing and selective etching of the positive photoresist.

[Preferred embodiment 21]

[0125] Figures 27A-27F and Figures 28A-28F show examples of process for constructing thin film transistors on the glass substrate with use of the two step halftone exposure method in the twenty first embodiment of the present invention. In this example, the two step halftone exposure method of the present invention is used in constructing the scanning line 15 and the common electrodes 49 within the pixel 49 at the same time, and the video signal line 51 and the liquid crystal drive electrode 53 at the same time.

[0126] In the example of Figures 27A-27F, a three-layer metal structure is utilized for the scanning line 15 which is created through the process of Figures 8A-8E. In the example of Figures 28A-28F; a two-layer metal structure is utilized for the scanning line 15 which is created through the process of Figures 7A-7E. Both examples of Figures 27A-27F utilize the two-step halftone exposure method in which the common electrode 49 within the pixel is structured with a single-layer of thin film.

[0127] When using the two-step halftone exposure method for forming the scanning line, alignment marks must be formed in the glass substrate in advance as shown in Figure 11 by the laser beam device such as shown in Figures 9 and 10. Both examples of Figures 27A-27F and 28A-28F utilize the halftone exposure to perform the processes of separating the silicon elements (silicon island forming process) from the semiconductor layer and constructing the terminal portion of contact holes at the same time.

[0128] In Figures 27A-27F and 28A-28F, a numeral 8 denotes an area where the photoresist is completely removed after development, a numeral 9 denotes a gate insulation film, a numeral 10 denotes a thin film semiconductor layer (non-doped layer), a numeral 11 denotes a thin film semiconductor layer (doped layer, i.e., ohmic contact layer), a numeral 15 denotes a scanning line, a numeral 20 denotes an area of the photoresist which is not exposed by the UV light, and a numeral 22 denotes an area of the photoresist which is incompletely exposed (halftone exposure), a numeral 49 denotes a common electrode within the pixel, a numeral 50 denotes a scanning line terminal, a numeral 51 denotes a video signal line, a numeral 52 denotes a barrier metal, a numeral 53 denotes a liquid crystal drive electrode, a numeral 54 denotes a scanning line terminal drive circuit contact electrode, and a numeral 55 denotes a passivation film.

[0129] In the example of Figures 27A-27F, the scanning line 15, scanning line terminal 50 and the common electrode 49 within the pixel have been formed through the process shown in Figures 8A-8E. In the example of Figures 28A-28F, the scanning line 15, the scanning line terminal 50 and the common electrode 49 within the pixel have been formed through the process shown in Figures 28A-28F. Then, in the both examples of Figures 27A-27F and 28A-28F, by the same procedures, the silicon elements are separated and the contact holes are created as follows:

[0130] First, as shown in Figures 27A and 28A, the gate insulation film 9, the thin film semiconductor layer (non-doped layer) 10, and thin film semiconductor layer (ohmic contact layer) 11 are consecutively deposited with use of a plasma CVD device. After coating the positive photoresist with a thickness of 2-3 micrometers, the halftone exposure process is conducted on the positive photoresist. Thus, the thicker area 20 and the thinner area 22 of the positive photoresist are created, while the photoresist is removed at an area over the scanning line terminal 50.

[0131] In Figures 27B and 28B, contact holes for the scanning line terminals 50 are created through, for example, a dry etching process. Then, the thinner area 22 of the photoresist formed through the halftone exposure is removed by the ashing process so that the positive photoresist remains at an area where the thin film transistor will be formed. In Figures 27C and 28C, through the dry etching process, the semiconductor layers are removed except for the areas where the thin film transistors will be formed. In Figures 27D-27F and 28D-28F, the video signal lines 51, the scanning line drive circuit

connection electrode 54 and the liquid, crystal drive electrode 53 are created, by using the process shown in Figures 7A-7E or Figures 8A-8E.

[0132] As has been describe above, in the process shown in Figures 27A-27F and 28A-28F, with use of the two-step exposure method of the present invention, the liquid crystal drive electrode 53 is made of a single layer of thin film. As in the present invention, since each of the common electrode 49 within the pixel and the liquid crystal drive electrode 53 is made of a thin film using the two-step halftone exposure method in the production process of the scanning line and the video signal line, smooth movements of the tips of the hairs of the rubbing cloth can be achieved in the alignment treatment, which is able to prevent occurrence of alignment defects.

[0133] When the separation of the silicon elements of the thin film transistors and the construction of the terminal portion of the contact holes are performed using the halftone exposure method as noted above, electrostatic protection circuits such as shown in Figures 21-26 must be created at the same time. Figures 21 and 22 show examples of circuit structure in the static electricity protection circuit, and Figures 23-26 show examples of pattern structure for establishing the static electricity protection circuits of Figures 21 and 22 on the substrate. In Figures 21-26, a numeral 14 denotes a video signal line, a numeral 15 denotes a scanning line, a numeral 16 denotes a common electrode for electrostatic protection, a numeral 17 denotes a thin film semiconductor layer; a numeral 18 denotes a contact hole for creating a thin film transistor circuit static electricity protection.

[0134] As shown in Figure 23, 24, 25 and 26, it is possible to maximize the size of the contact holes 18 by positioning them together. In this case, a local exposure device such as shown in Figures 12 and 13 using either an ultraviolet laser beam or an ultraviolet. LED can be used to locally expose the portions of the contact holes. In Figure 12, a numeral 25 denotes an fθ lens, a numeral 29 denotes a laser light source, a numeral 30 denotes a beam formatter, a numeral 31 denotes a galvanomirror, a numeral 32 denotes a laser- beam, a numeral 33 denotes a mark pattern formed within the glass substrate, a numeral 34 denotes an ultrasonic polarizer, a numeral 35 denotes a UV laser source, a numeral 36 denotes a UV laser light, a numeral 38 denotes the glass substrate for TFT array, and a numeral 39 denotes a positive photoresist layer.

[0135] Figures 6A-6C show the first and second exposure steps using the local exposure device. In the example of Figures 6A-6C, the second exposure step is performed without using a photomask but using the fθ lens for locally exposing a part of the glass substrate. As noted above, the fθ lens is able to focus on a relatively large area on the same flat surface of the substrate.

[0136] Figures 29 and 30 show the plan views of the halftone scan exposure device having a built-in local exposure device of the present invention. In Figures 29 and 30, a numeral 40 denotes a micro-mirror array device, a numeral 44 denotes a multi-lens projection module, a numeral 45 denotes a photomask, a numeral 46 denotes an X-Y stage, a numeral 47 denotes a UV source, and a numeral 56 denotes an ultraviolet laser scan exposure device. The halftone exposure process and the local exposure process can be conducted at the same time with use of only one device of either Figure 29 or Figure 30 and the ordinary photomask. Thus, the production efficiency can be improved significantly.

[0137] Figure 31 shows the plan view of the transverse electric field type active matrix substrate created with use of the halftone exposure method of the present invention In Figure 31, a numeral 57 denotes a terminals of the video signal line, a numeral 58 denotes a terminal of the common electrode surrounding the pixel, a numeral 59 denotes a static electricity protection circuit, a numeral 60 denotes a passivation film, and a numeral 61 denotes a contact hole created through the local UV exposure noted above. The contact holes 61 constructed through the local ultraviolet ray exposure are positioned together in a line.

[0138] Figure 4 is a flow chart summarizing the process for producing the TFT array on the substrate using the ordinary photomasks through the two-step halftone exposure method of the present invention. The basic process of the two-step halftone exposure is shown in Figures 5 and 6, which uses two or more ordinary photomasks. In the process of Figure 4, the photomasking process is repeated four times each including the first and second halftone exposure. First, alignment marks are formed in the glass substrate by a laser beam at step S21. In the first and second halftone exposure in step S22, the gate electrodes for thin film transistors and the common electrodes are formed at the same time. Then, at step S23, through the first and second halftone exposure, the thin film transistors are separated from the semiconductor layer and the contact holes are created. In step S24, the source and drain electrodes and the liquid crystal drive electrodes are formed at the same time through the first and second halftone exposure. Lastly, at step S25, gate terminals and data terminals are formed.

[0139] Figure 124 is a flow chart summarizing the process for producing the TFT array on the substrate using the ordinary photomasks through the two-step halftone exposure method of the present invention. The basic process of the two-step halftone exposure is shown in Figures 5 and 6 which uses two or more ordinary photomasks . In the process of Figure 124, the photomasking process is repeated three times each including the first and second halftone exposure. First, alignment marks are formed in the glass substrate by a laser beam at step S81. Through the first and second halftone exposure, in step S82, the gate electrodes for thin film transistors and the common electrodes are formed at the same time. Then, at step 583, through the first and second halftone exposure, the thin film transistors are separated from the semiconductor layer and the contact holes are created. In step S84, the source and drain elec-

trodes of the thin film transistors and the liquid crystal drive electrodes are formed at the same time through the first and second halftone exposure. During this process, a leveling film is applied to the surface of the substrate for flattening the surface. For example, after a back channel B2H6 plasma doping treatment, the leveling film is formed by an ink jet printing method or a partial P-SiNx protection film is formed through a masking method using a shadow frame.

[Preferred embodiment.22]

[0140] Figures 114A-114C and Figures 130A-130C are cross sectional views showing examples of processes in which the steps of flattening (leveling or planarizing) the substrate and forming the photolithography spacers are conducted with use of both the ordinary photomask exposure and the halftone back surface exposure in the twenty second embodiment of the present invention. In this example, negative photoresist is used. In the example of Figures 114A-114C and Figures 130A-130C, a numeral 55 denotes a passivation film, a numeral 71 denotes a TFT array alignment film, a numeral 87 denotes a negative photoresist layer for halftone exposure, a numeral 89 denotes a photolithography spacer, a numeral . 91 denotes a UV light from the back surface of the substrate, a numeral 92 denotes the negative photoresist remained after the back surface exposure and the development.

[0141] First, the negative photoresist 87 is applied on the passivation film 55 for the thickness oaf the liquid crystal cell gap as shown in Figures 114A and 130A. Next, as shown in the upper part of Figures 114B and 130B, the complete exposure is done with an ordinary photomask at the areas where the photolithography spacers are to be constructed. Then, as shown in the lower part of Figures 114B and 130B, with use of the scanning type back surface exposure device such as shown in Figures 131, 132, 133 and 134, the negative photoresist 87 is exposed by the ultraviolet rays 91 from the back surface of the active matrix substrate to expose enough light for a thickness sufficient to flatten the irregularity of the substrate. After the back surface exposure, flattening of the substrate (TFT alignment film 71) and construction of the photo spacer 89 are effectively done at the same time as shown in Figures, 114C and 130C.

[0142] Figure 129 is a flow chart summarizing, the process of producing the active matrix substrate including the steps for flattening (leveling) the substrate and forming the photolithography spacers by using the ordinary photomask exposure and the halftone back surface exposure in the twenty second embodiment. In step S131, the gate electrodes for thin film transistors and the common electrodes are formed at the same time. Then, at step S132, silicon element for the thin film transistors are separated from the semiconductor layer. At step S133, the source and drain electrodes of the thin film transistors and the liquid crystal drive electrodes are formed at the same time. Then, the contact holes are formed at step S134. Next, the static electricity protection circuit, gate terminal and data terminal are formed in step S135. Lastly, at step S136, the creation of photolithography spacers and the leveling of the substrate surface are conducted by first conducting the halftone back exposure for flattening the substrate surface and then conducting the complete exposure for forming the photolithography spacers.

[0143] Figures 131 and 132 shows a scanning type bask surface exposure device utilized in the twenty second embodiment of the present invention. In the example of Figures 131 and 132, a numeral 19 denotes a UV light, a numeral. 76 denotes a glass substrate for the TFT array, a numeral 87 denotes a negative photoresist for halftone exposure, a numeral 102 denotes a conveyer roller, a numeral 103 denotes a UV cut cover, and a numeral 104 a silica glass fiber. The glass substrate 76 is moved horizontally on the roller 102 so that the large substrate can be exposed by a relatively small exposure device. The silica glass fibers 104 are bundled together and positioned next to each other to produce a constant strength of ultraviolet ray. In the example of Figures 133 and 134, the back surface exposure device includes a plurality of ultraviolet ray LEDs. 107 positioned next to each other to produce a uniform power level of the ultraviolet rays 19.

[0144] Figures 135-137 show examples of optical system including a white light interferometer and a process using the optical system for precisely measuring the height of the photolithography spacers constructed on the active matrix substrate. Figure 135 shows an overall system configuration for producing the active matrix substrate including the halftone back surface exposure device of the present invention, Figure 136 is a flow chart showing an overall process, of the halftone back surface exposure method of the present invention, and Figure 137 shows an example of optical system structure in the white light interferometer used in the present invention.

[0145] In the flow chart of Figure 136, at step 141, the negative photoresist is coated on the glass substrate where the thickness of the negative photoresist is adjusted bases on the measured data regarding the height of the photolithography spacer and photoresist on the substrate. At step 142, the halftone back surface exposure is performed in which the amount of light exposure is adjusted based on the measured data. After the halftone back surface exposure, the negative photoresist for the photolithography spacers is completely exposed in step 143. After the development in step S144, the height of the photolithography spaces are measured by, for example, the white light interferometer, the result of which is feedbacked to the photoresist coating and the halftone back surface exposure through a step S146 for adjusting the photoresist coating thickness and amount of light for exposure. The above process may repeated two or more times. The resultant substrate is evaluated at step 147, and if the result is acceptable, the process moves to a post bake process in step S148.

[0146] In the example of Figure 137, the white light interferometer includes a CCD camera, a white light source, a mirror, and an interferometric objective lens. The vertical position of the interferometric objective lens is controlled by a mechanism using, for example, a piezo-electric device (PZT), for focusing the white light on the top and bottom of the photolithography spacer and/or negative photoresist. The voltage used for driving the piezo-electric device can be used as the measured data indicating the height of the photolithography spacer.

[0147] As shown in Figures 135, 136 and 137, the white light interferometer accurately measures the thickness of the negative resist layer and the height of the spacer on the glass substrate. This measurement data from the white light interferometer is feedbacked to the coater (slit, coaster and spin and the halftone back exposure system to adjust the coating thickness of the negative photoresist and the amount of light for the halftone back surface exposure. Accordingly, the surface irregularity of the substrate and the height irregularity of the photolithography spacers can be minimized.

[0148] Figures 107A-107D show the processes for performing the flattening (leveling) the substrate surface first then constructing the photolithography spacers using the scanning type back surface exposure device of the present invention. In the example of Figures 107A-107D, a numeral 9 denotes a gate insulation film, a numeral 49 denotes a common electrode within the pixel, a numeral 51 denotes a video signal line, a numeral 53 denotes a liquid crystal drive electrode, a numeral 55 denotes a passivation film, a numeral 71 denotes a TFT array alignment film, a numeral 75 denotes a common electrode for shielding the video signal line, a numeral 76 denotes a glass substrate for TFT array, a numeral 88 denotes a negative photoresist layer for leveling (flattening) the substrate surface, a numeral 89 denotes a photolithography spacer, a numeral 91 denotes a UV light, and a numeral 92 denotes negative photoresist remained after back surface exposure.

[0149] In the example of Figures 107A-107D, the negative photoresist 88 is applied on the passivation film 55 for the thickness of the liquid crystal cell gap as shown in Figure 107A. The UV light 91 is applied from the back surface of the glass substrate 76 to expose the negative photoresist 88 by an enough light for a thickness sufficient to flatten the irregularity of the substrate. After the development, the negative photoresist 92 is remained on the glass substrate in a flat manner to form a flat surface as shown in Figure 107B. Then, the negative photoresist is coated again and the complete exposure is performed with an ordinary photomask at the areas where the photolithography spacers are to be constructed. Thus, the photolithography spacers 89 are created after development as shown in Figure 107C. Lastly, the alignment film 71 is formed on the surface of the substrate as shown in Figure 107D.

[0150] Although the photolithography spacers are utilized in the example of Figures 107A-107D, 114A-114C and 130A-130C, the spacer bumps 73 described above with respect to the first, second, fifth, sixth and ninth embodiments can also be utilized. When the scanning type back surface exposure method is used to perform the flattening process, metal electrodes that do not allow the light to transmit therethrough must be used for the common electrodes 49 within the pixel and the liquid crystal drive electrodes 53.

[0151] Figure 105 is a flow chart summarizing the process of producing the active matrix substrate including the steps for flattening (leveling) the substrate and forming the photolithography spacers using the ordinary photomask exposure method arid the halftone back surface exposure in the twenty second embodiment. In step 541, the gate electrodes of the thin film transistors and the common electrodes are formed at the same time. Then, at step S42, the silicon elements far the thin film transistors are separated from the semiconductor layer, and the contact holes are formed welt the same time using the first and second halftone exposure. Then in step S43, the source and drain electrodes of the thin film transistors and the liquid crystal drive electrodes are formed at the same time. During this step, after creating the source and drain electrodes and the liquid crystal drive electrodes, a leveling film is applied on the substrate and the surface flattening (leveling) is performed by the halftone back surface exposure. Lastly, at step S44, the photolithography spacers are created through the complete exposure.

[Preferred embodiment 23]

[0152] Figure 125 is a flow chart showing an example of production processes involved in the transverse electric field type active matrix substrate according to the twenty third embodiment of the present invention. There are five photolithography processes. In step S91, the gate electrodes of the for thin film transistors and the common electrodes are formed at the same time. Then, at step S92, silicon elements for the thin film transistors are separated from the semiconductor layer, and the contact holes are formed at the same time through the first and second halftone exposure. In step S93, the source and drain electrodes of the thin film transistors and the liquid crystal drive electrodes are formed at the same. Then, at step 594, the photolithography spacer is formed through the complete exposure after the surface flattening (leveling) is conducted through the halftone back surface exposure method. Lastly, at step S95, contact holes for the gate terminals and data terminals are formed.

[0153] In the twenty third embodiment described above, the production process is already significantly shortened by utilizing the processes implemented in the twenty first embodiment and the twenty second embodiment. The flattening (levelling) process is performed on the surface of the substrate, thus, alignment defects will not arise during the rubbing alignment treatment. As a result, light leakage during the black display is minimized, thereby achieving a display with high contrast.

[0154] Figure 128 is a flow chart summarizing a further example of process for producing the active matrix substrate including the steps for flattening (leveling) the substrate, and forming the photolithography spacers using the ordinary photomask exposure and the halftone back surface exposure in the twenty third embodiment. In step S121, the gate electrodes of the thin film transistors and the common electrodes are formed at the same time. Then, at step S122, silicon elements for the thin film transistors are separated from the semiconductor layer. At step S123, the contact holes are formed. In step S124, the source and drain electrodes of the thin film transistors and the liquid crystal drive electrodes are formed at the same time. During this process, a leveling film is applied to the surface of the substrate. For example, after a back channel B2H6 plasma doping treatment, the leveling film is formed by an ink jet printing method or a partial P-SiNx protection film is formed through a masking method using a shadow frame. Lastly, at step S125, the leveling of the substrate surface are conducted through the halftone back surface exposure, and then, the photolithography spacers are formed through the complete exposure.

[Preferred embodiment 24]

[0155] Figure 126, is a flow chart showing an example of process involved in the production of the transverse electric field type active matrix substrate according to the twenty fourth embodiment of the present invention. There are four photolithography steps in this process. In step S101, the gate electrodes of the thin film transistors and the common electrodes are formed at the same time. Then, at step S102, the silicon elements for the thin film transistors are separated from the semiconductor layer and the contact holes are formed at the same time through the first and second halftone exposure. In step S103, the source and drain electrodes and liquid crystal drive electrodes are formed as the same time. During this process, a leveling film is applied to the surface of the substrate. For example, after a. back channel B2H6 plasma doping treatment, the leveling film is formed by an ink jet printing method or a partial P-SiNx protection film is formed through a masking method using a shadow frame. Lastly, at step S104, the flattening process for the substrate surface are conducted through the: halftone back surface exposure, and then, the photolithography spacers are formed through the complete exposure. The overall production process is significantly shortened by utilizing the processes in the twenty first embodiment and the twenty second embodiment described above.

[0156] In the twenty fourth embodiment, although the P-SiNx passivation layer is applied using the P-CVD device on the entire surface of the substrate in the twenty third embodiment, the process for opening the contact holes for terminals of the scanning lines (gate electrodes) and the video signal line (data electrodes) is eliminated by partially applying the P-SiNx passivation layer using a partial layer construction method using a shadow frame or by partially applying an organic passivation layer (BCB for example) using an application device such as an ink jet printer. Similar to the foregoing embodiments, since the substrate surface undergoes a leveling process, alignment defects will not occur during the rubbing treatment.

[Preferred embodiment 25]

[0157] Figure 127 is a flow chart showing an example of process involved in the production of transverse electric field type active matrix substrate according to the twenty fifth embodiment which is not a part of the present invention. There are three photolithography processes. In step 5111, the gate electrodes of the thin film transistors and the common electrodes are formed at the same time through, for example, a masking deposition process using a shadow frame for a structure of P-SiNx\a-Si i\n+a-Si. Then, at step S112, the silicon elements for the thin film transistors are separated from the semiconductor layer and the source and drain electrodes of the thin film transistors are formed at the same time through the first and second halftone exposure. During this process, a leveling film is applied to the surface of the substrate. For example, after a back channel B2H6 plasma doping treatment, the leveling film is formed by an ink jet printing method or a partial P-SiNx protection film is formed through a masking method using a shadow frame. Lastly, at step S113, the leveling of the substrate surface are conducted through the halftone back surface exposure, and then, the photolithography spacers are formed through the complete exposure.

[0158] By utilizing the processes in the seventeenth embodiment and the twenty second embodiment, the time required for the overall production process is significantly shortened. This embodiment can eliminate the process for opening the contact holes for terminals of the scanning lines (gate electrodes) and the video signal line (data electrodes) by partially applying the P-SiNx passivation layer using a partial layer construction method utilizing a shadow frame or by partially applying an organic passivation layer (BCB for example) using an application device such as an ink jet printer. Similar to the foregoing embodiments, since the substrate surface undergoes a flattening process, alignment defects will not occur during the rubbing treatment.

[Effect]

[0159] As has been described above, by utilizing the halftone shift exposure method using an ordinary photomask, or by utilizing the halftone mixed exposure method which is a combination of the halftone exposure using the ordinary photomask and the local additional exposure, the transverse electric field type liquid crystal display device can be produced with low cost and high production yield.

[0160] By utilizing the halftone back surface scanning

exposure method and by constructing the photolithography spacers in one negative photoresist process, low production cost, high display quality without alignment defects, and high contrast can be achieved.

[0161] By adapting the spacer bump structure, the transverse electric field type liquid crystal display system with high aperture ratio and low production cost can be realized. By constructing the upper layer shielding common electrodes, the common electrodes within the pixel, and the liquid crystal drive electrodes by the same conductive material on the same layer, it is possible to produce a high quality display device with minimized residual image, high aperture ratio, and with uniform and deep black level display. Thus, an ultra large screen transverse electric field type liquid crystal display television with low cost and high contrast can be realized.

Claims

1. A method of producing an active matrix substrate of a transverse electric field type active matrix liquid crystal display device, comprising the following steps of:

   (1) forming patterns for scanning lines (15) in a scanning line patterning step;
   (2) separating silicon elements for thin film transistors from a semiconductor layer in a silicon island forming step;
   (3) forming video signal lines (51) and liquid crystal drive electrodes (53) at the same time;
   (4) forming spacer bumps (73) that cover the video signal lines (51), or forming spacers and insulation bumps that cover the video signal lines;
   (5) forming contact holes for terminal portions and for static electricity protection circuits; and
   (6) forming transparent common electrodes for shielding the video signal line and transparent common electrodes within pixels at the same time;

   characterized in that
   a taper angle (θ) of the bumps being an angle between the bottom face and the side faces of the bump at the edges of the bump on the active matrix substrate is 30 degrees or less, and
   in the case of forming spacers and insulation bumps that cover the video signal lines, the spacers and the insulation bumps are formed at the same time in a halftone exposure process.

Patentansprüche

1. Verfahren zum Herstellen eines Aktivmatrixsubstrats einer Aktivmatrixflüssigkristallanzeigevorrichtung vom elektrischen Transversalfeldtyp, das die folgenden Schritte enthält:

   (1) Bilden von Strukturen für Abtastleitungen (15) in einem Abtastleitungsstrukturierungsschritt,
   (2) Trennen von Siliziumelementen für Dünnfilmtransistoren aus einer Halbleiterschicht in einem Siliziuminselbildungsschritt,
   (3) gleichzeitiges Bilden von Videosignalleitungen (51) und Flüssigkristallansteuerelektroden (53),
   (4) Bilden von Abstandshalterhöckern (73), die die Videosignalleitungen (51) bedecken, oder von Abstandshaltern und Isolationshöckern, die die Videosignalleitungen bedecken,
   (5) Bilden von Kontaktlöchern für Anschlussabschnitte und für Schutzschaltungen gegen statische Elektrizität, und
   (6) gleichzeitiges Bilden von transparenten gemeinsamen Elektroden zum Abschirmen der Videosignalleitung und von transparenten gemeinsamen Elektroden innerhalb von Pixeln,

   dadurch gekennzeichnet, dass
   ein Neigungswinkel (θ) der Höcker, der ein Winkel zwischen der Grundfläche und den Seitenflächen des Hökkers an den Rändern des Höckers auf dem Aktivmatrixsubstrat ist, 30 Grad oder weniger ist, und im Fall des Bildens von Abstandshaltern und Isolationshöckern, die die Videosignalleitung bedecken, die Abstandshalter und Isolationshöcker gleichzeitig in einem Halbtonbelichtungsverfahren gebildet werden.

Revendications

1. Procédé de production d'un substrat de matrice active d'un dispositif d'affichage à cristaux liquides à matrice active du type à champ électrique transversal, comprenant les étapes suivantes qui consistent :

   (1) à former des motifs pour des lignes de balayage (15) dans une étape de formation de motifs de lignes de balayage ;
   (2) à séparer des éléments de silicium pour des transistors à couches minces depuis une couche de semiconducteur dans une étape de formation d'îlot de silicium ;
   (3) à former des lignes de signal vidéo (51) et des électrodes d'entraînement de cristaux liquides (53), en même temps ;
   (4) à former des bosses (73) d'espaceur qui couvrent les lignes de signal vidéo (51), ou à former des espaceurs et des bosses d'isolation qui couvrent les lignes de signal vidéo ;

(5) à former des trous de contact pour des parties terminales et pour des circuits de protection d'électricité statique ; et
(6) à former des électrodes de référence transparentes pour protéger la ligne de signal vidéo et des électrodes de référence transparentes dans des pixels, en même temps ;

caractérisé en ce que
un angle de conicité (θ) des bosses qui est un angle entre la face inférieure et les faces latérales de la bosse au niveau des bords de la bosse sur le substrat de matrice active est de 30 degrés ou moins, et
dans le cas de formation d'espaceurs et de bosses d'isolation qui couvrent les lignes de signal vidéo, les espaceurs et les bosses d'isolation sont formés en même temps dans un processus d'exposition à demi-ton.

FIG. 1 (A)

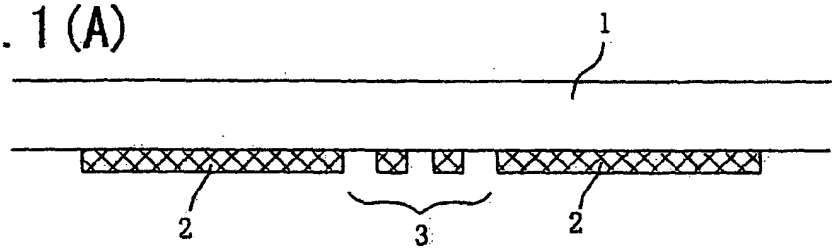


FIG. 1 (B)

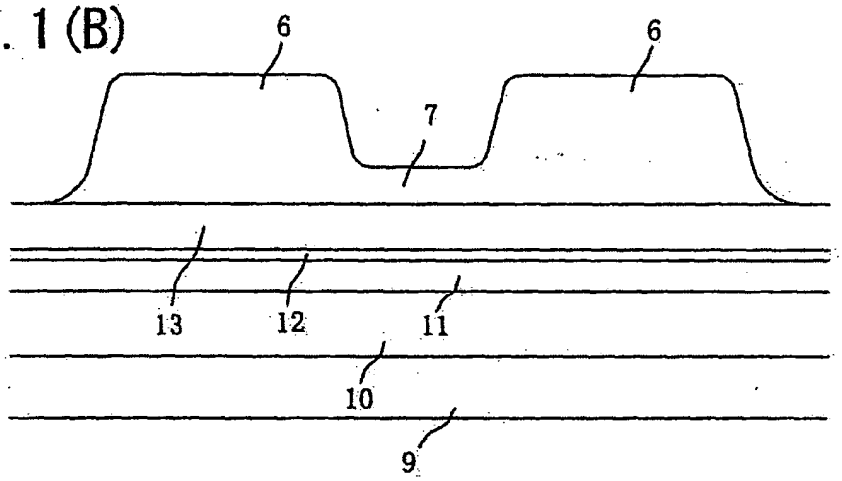


FIG. 2 (A)

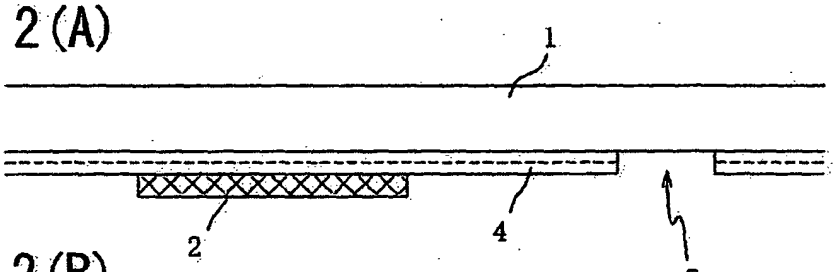


FIG. 2 (B)

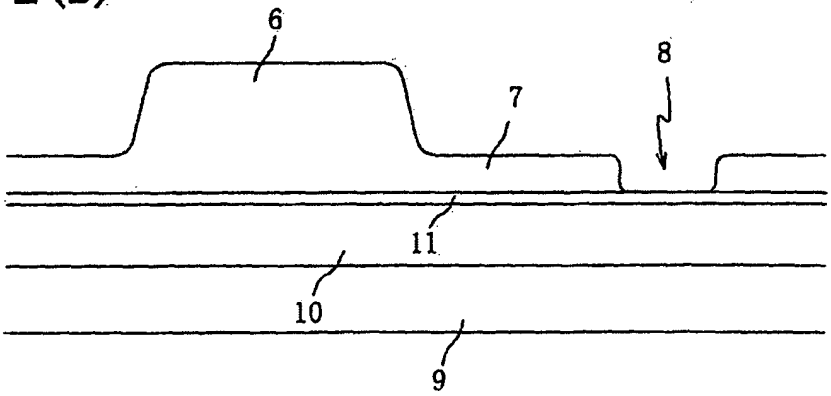


FIG. 3

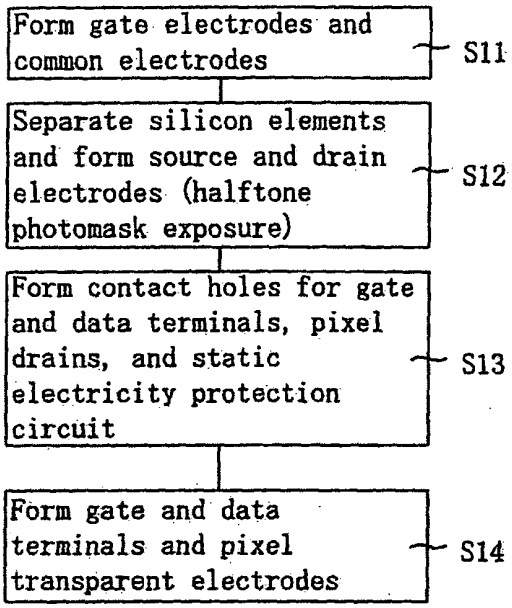

Form gate electrodes and common electrodes
S11
Separate silicon elements and form source and drain electrodes (halftone photomask exposure)
S12
Form contact holes for gate and data terminals, pixel drains, and static electricity protection circuit
S13
Form gate and data terminals and pixel transparent electrodes
S14

FIG. 4

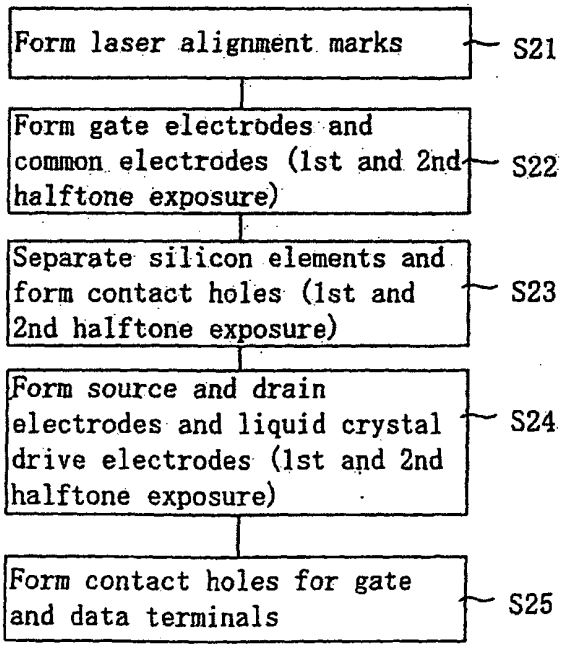

Form laser alignment marks
S21
Form gate electrodes and common electrodes (1st and 2nd halftone exposure)
S22
Separate silicon elements and form contact holes (1st and 2nd halftone exposure)
S23
Form source and drain electrodes and liquid crystal drive electrodes (1st and 2nd halftone exposure)
S24
Form contact holes for gate and data terminals
S25

FIG. 5(A) 1st Exposure

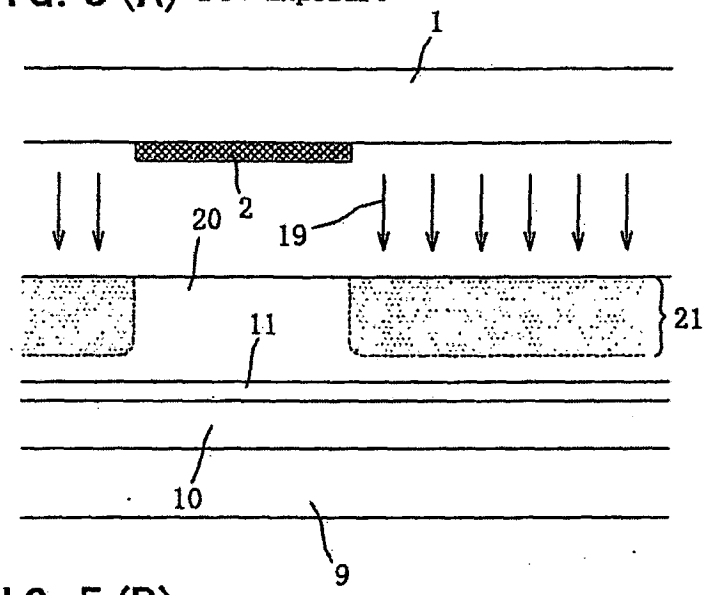


FIG. 5(B) 2nd Exposure

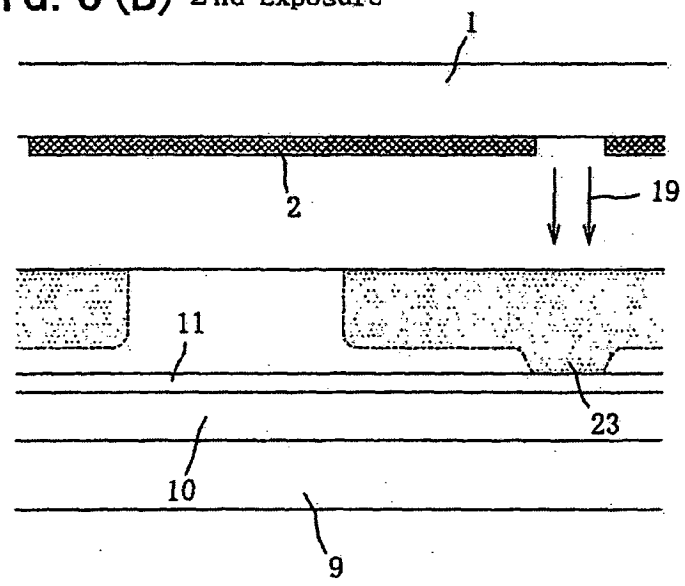


FIG. 5(C)

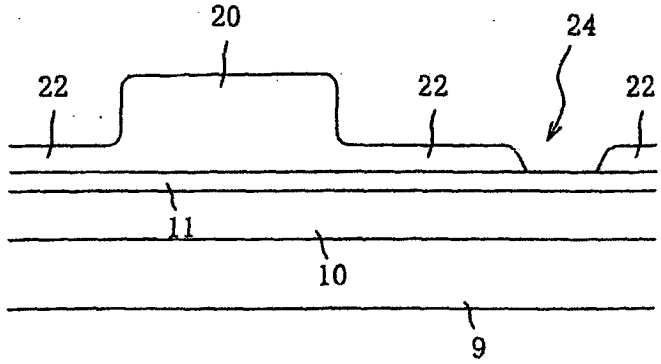


FIG. 6(A) 1st Exposure

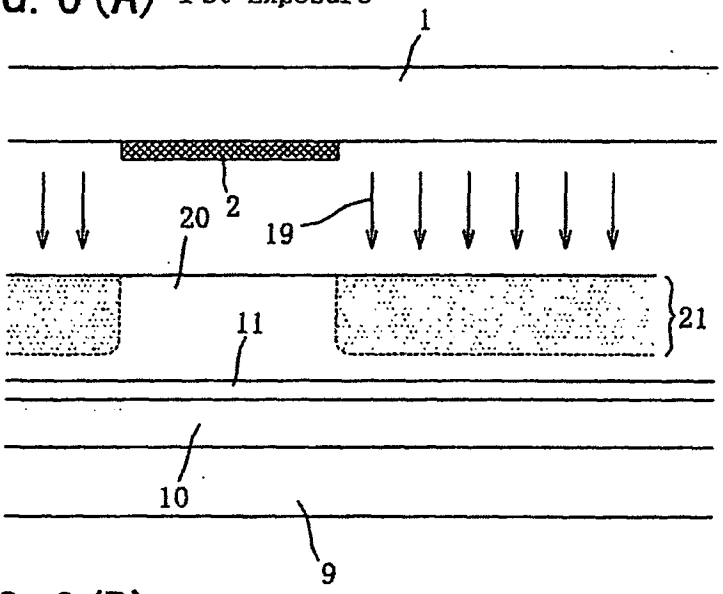


FIG. 6(B) 2nd Exposure

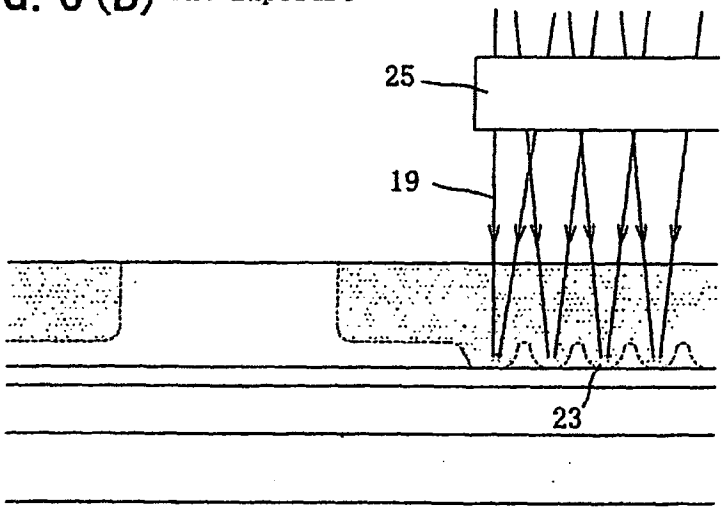


FIG. 6(C)

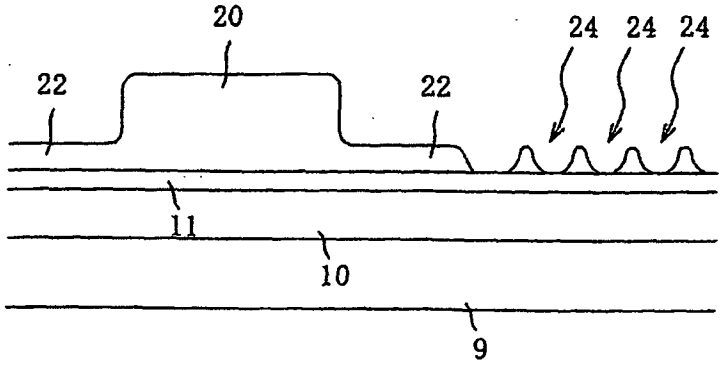


FIG. 7(A)

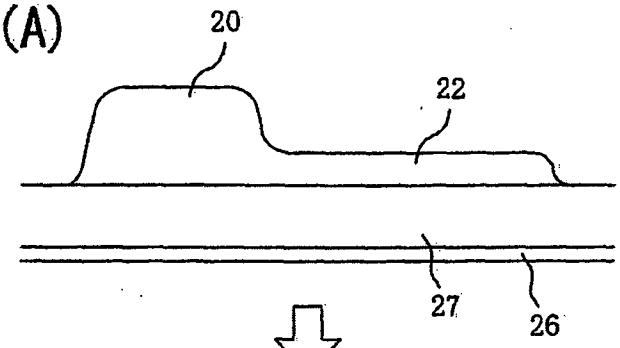


FIG. 7(B)

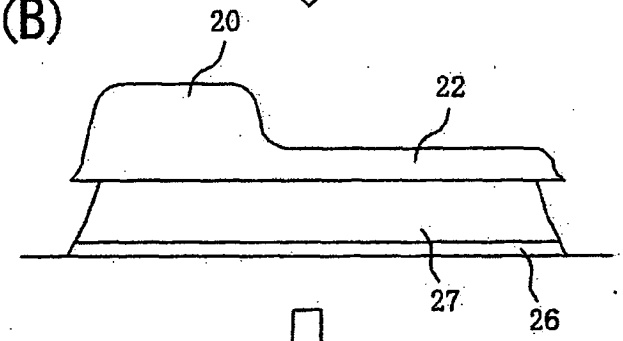


FIG. 7(C)

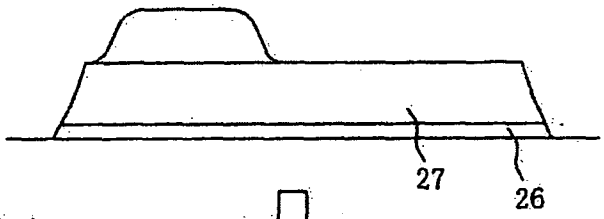


FIG. 7(D)

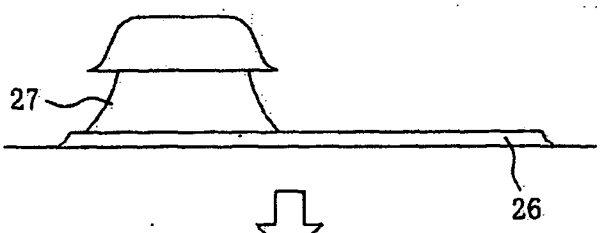


FIG. 7(E)

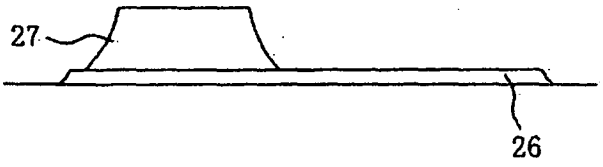


FIG. 8(A)

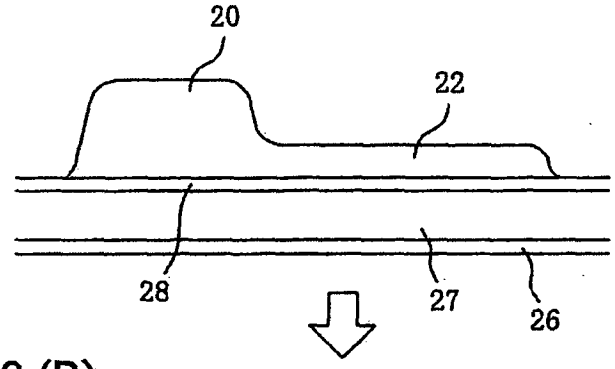


FIG. 8(B)

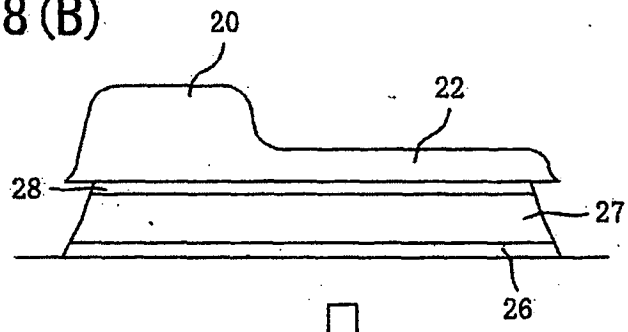


FIG. 8(C)

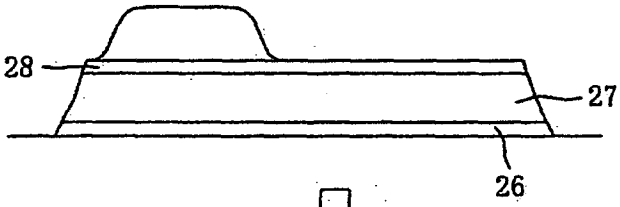


FIG. 8(D)

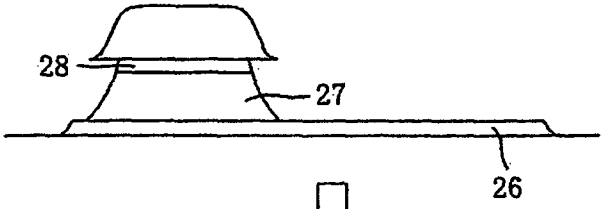


FIG. 8(E)

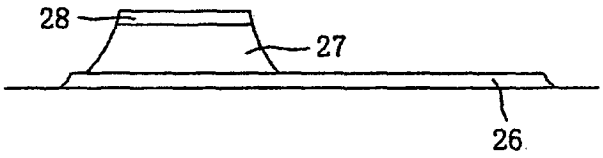


FIG. 9

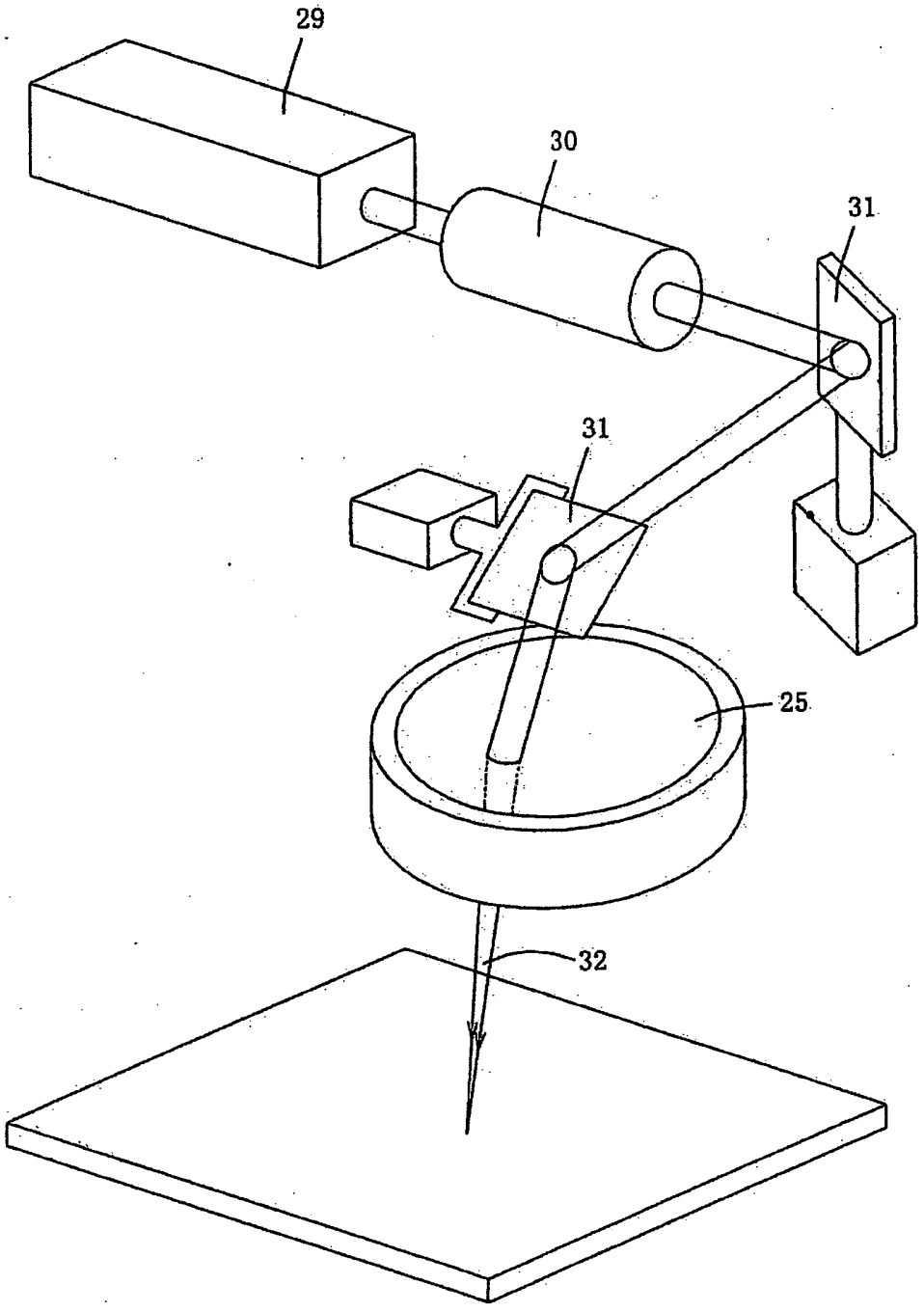


FIG. 10

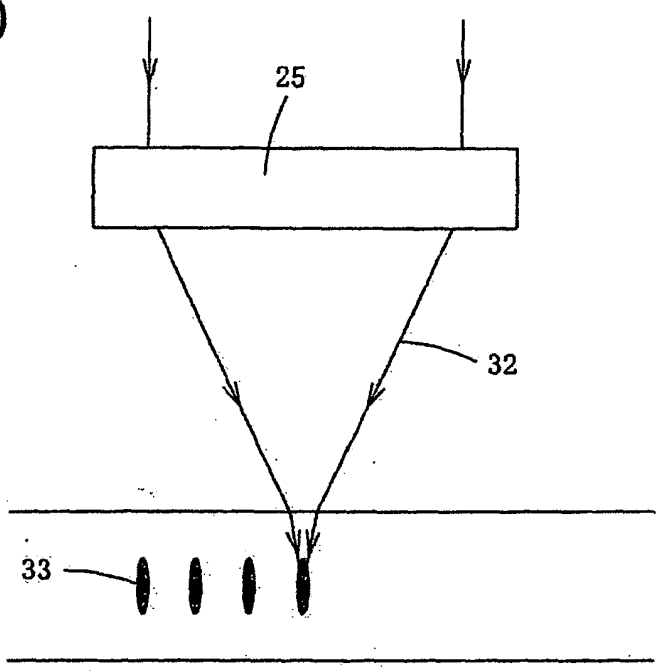


FIG. 11

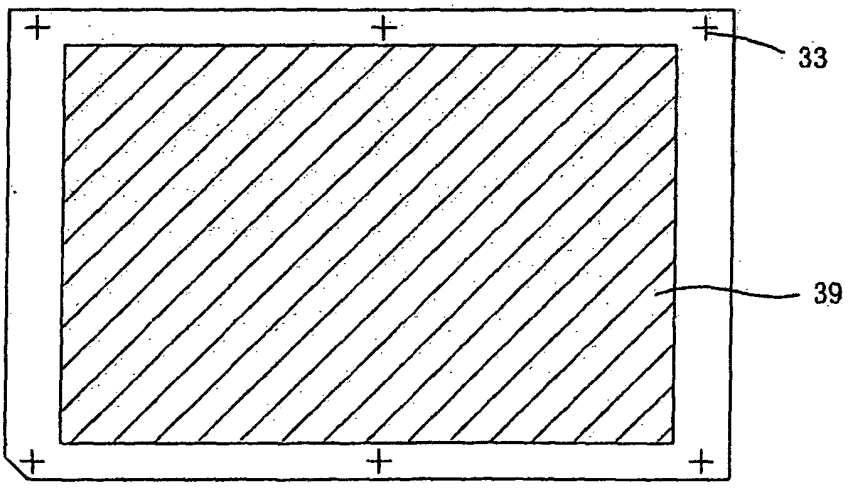


FIG. 12

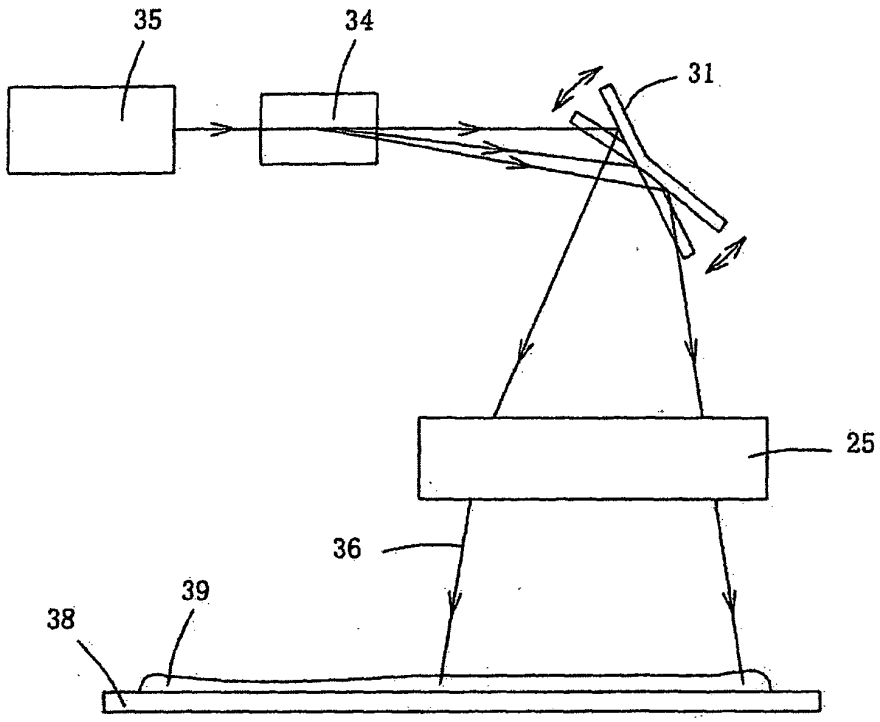


FIG. 13

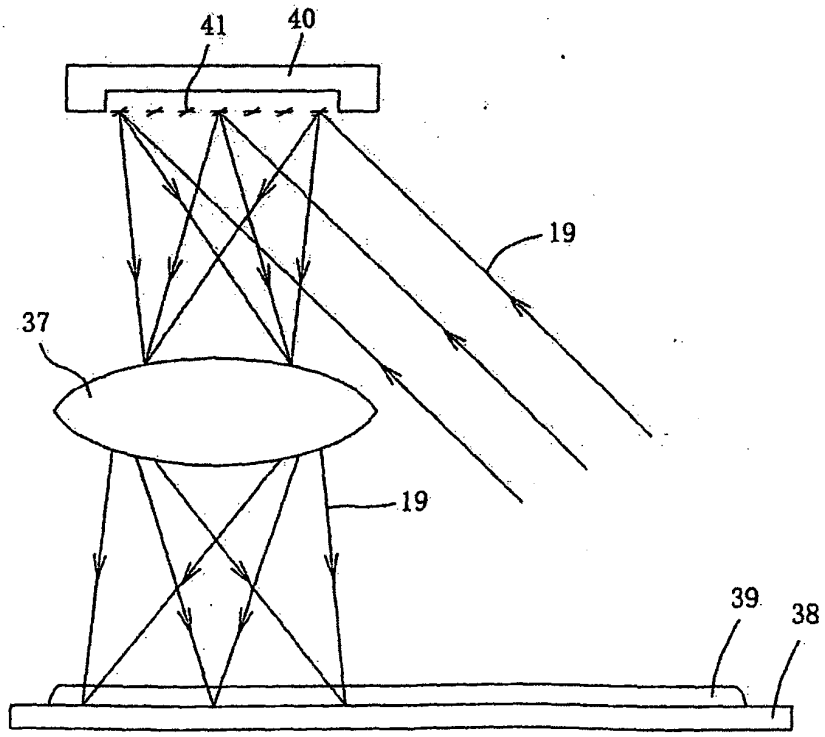


FIG. 14

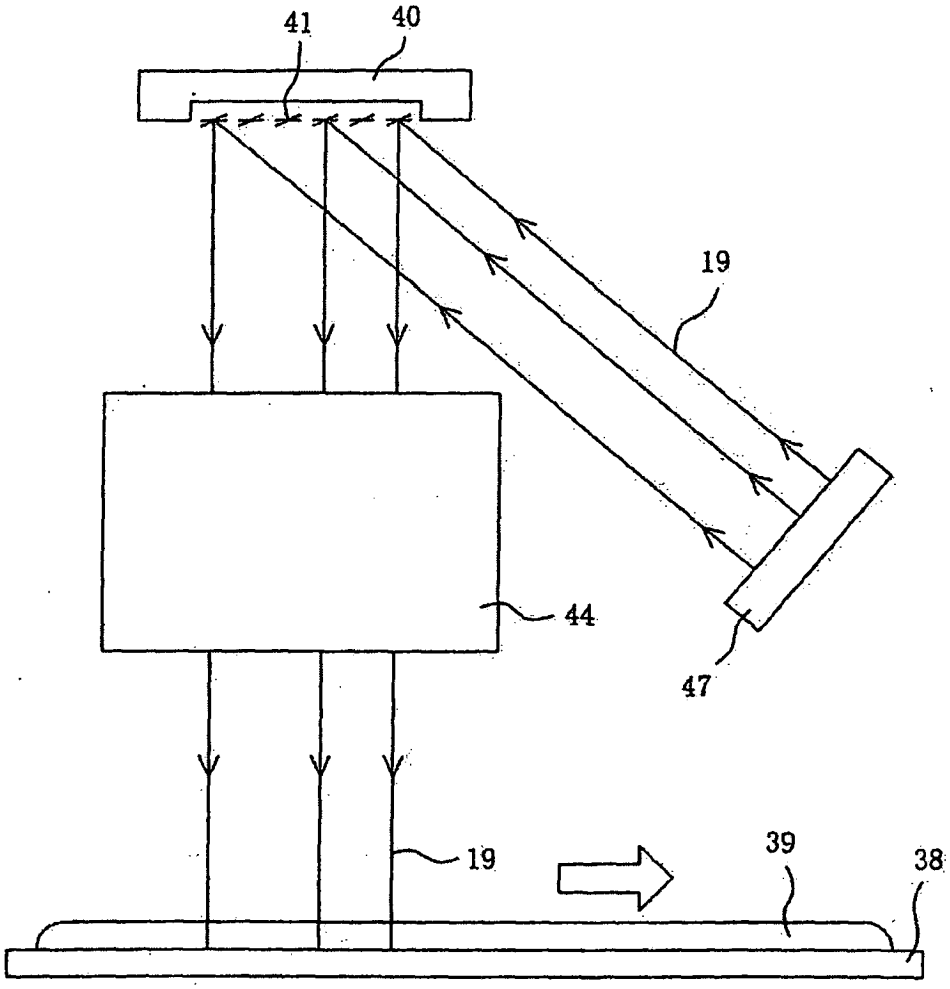


FIG. 15

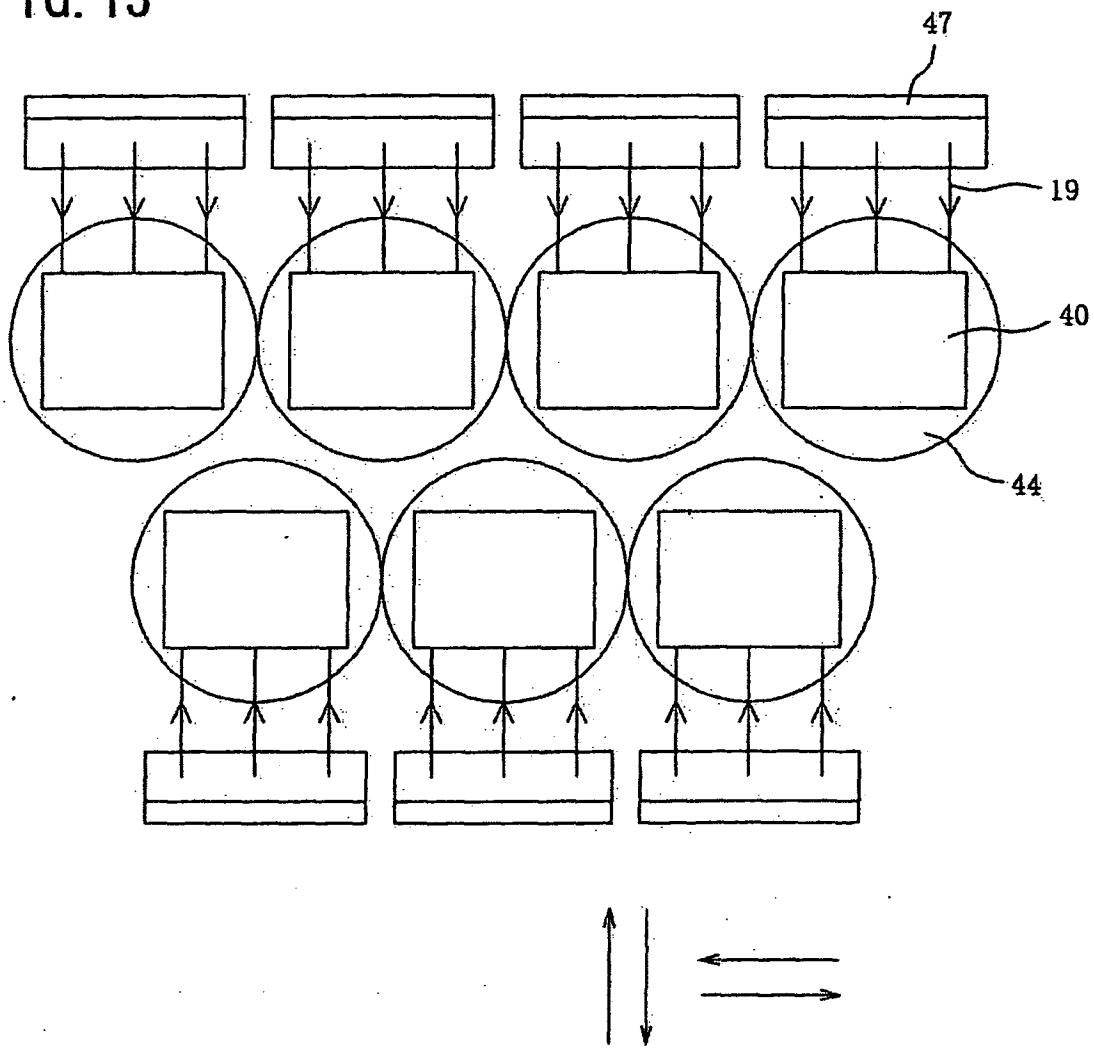


FIG. 16

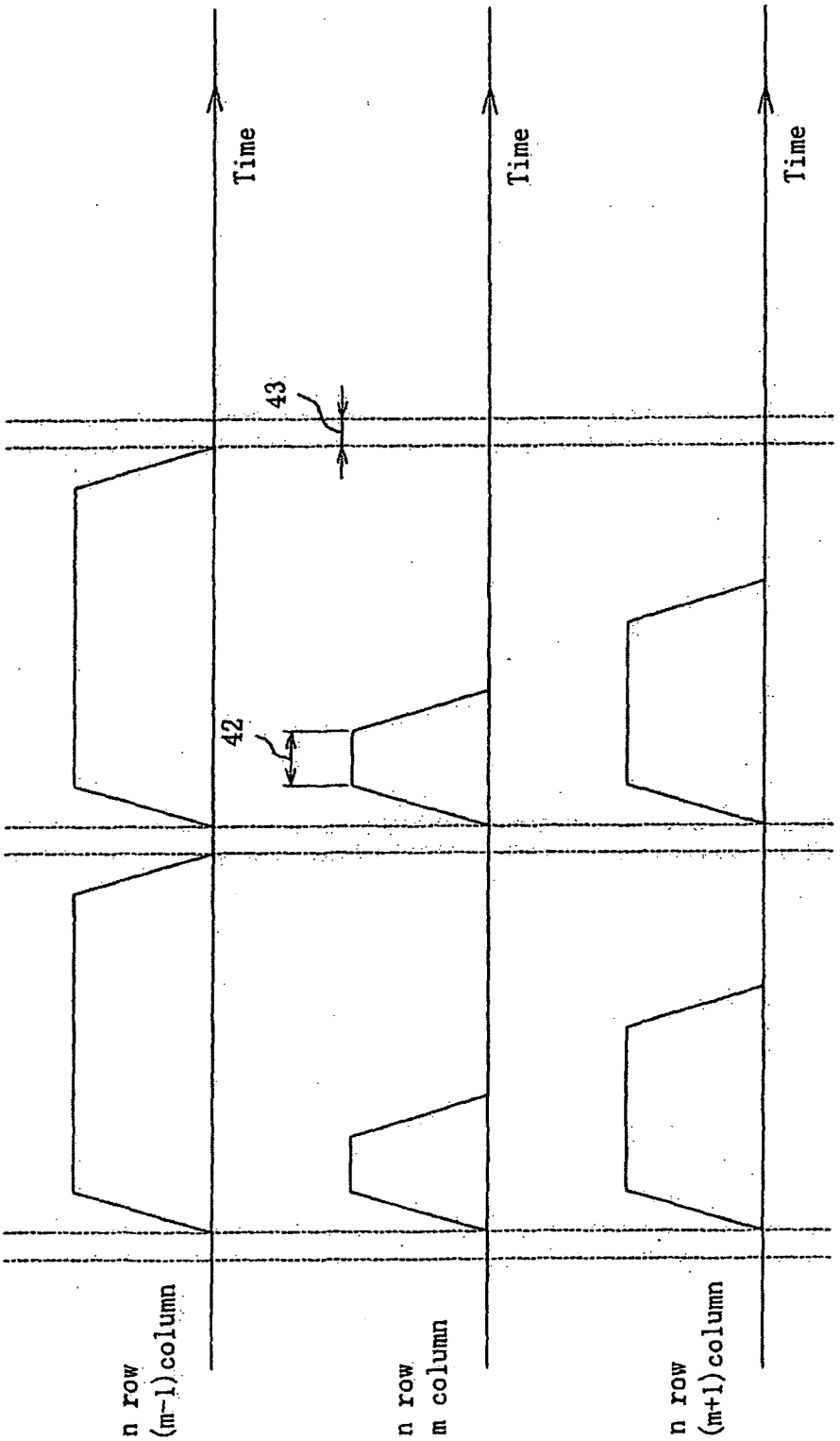

Time
Time
Time
43
42
n row
(m-1) column
n row
m column
n row
(m+1) column

FIG. 17

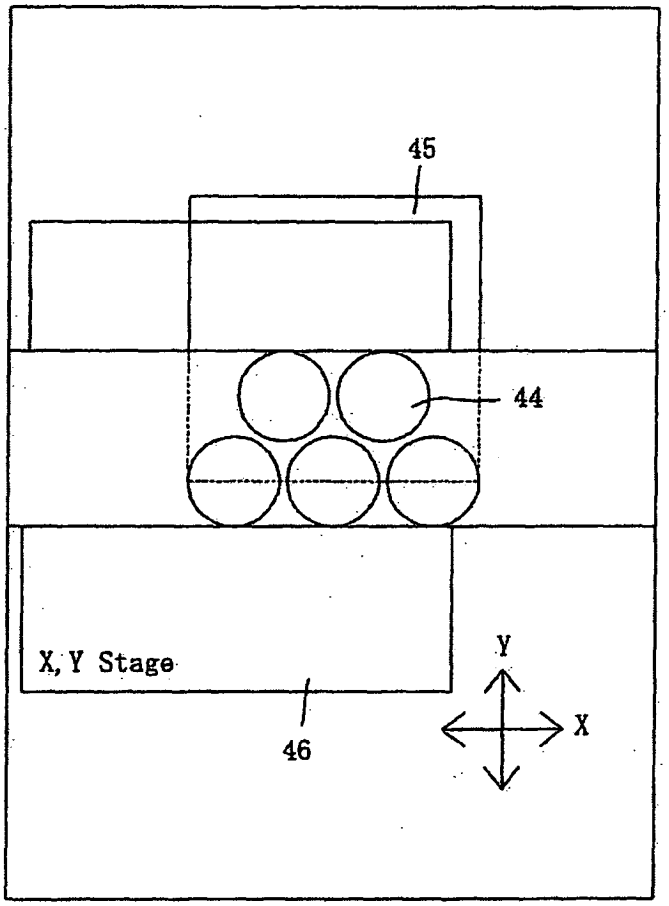


FIG. 18

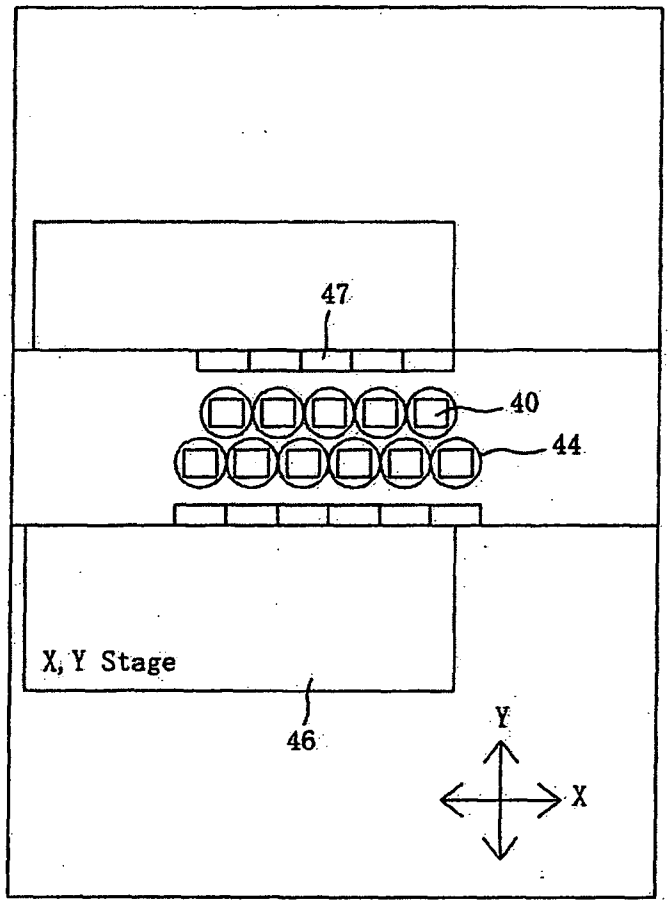


FIG. 19

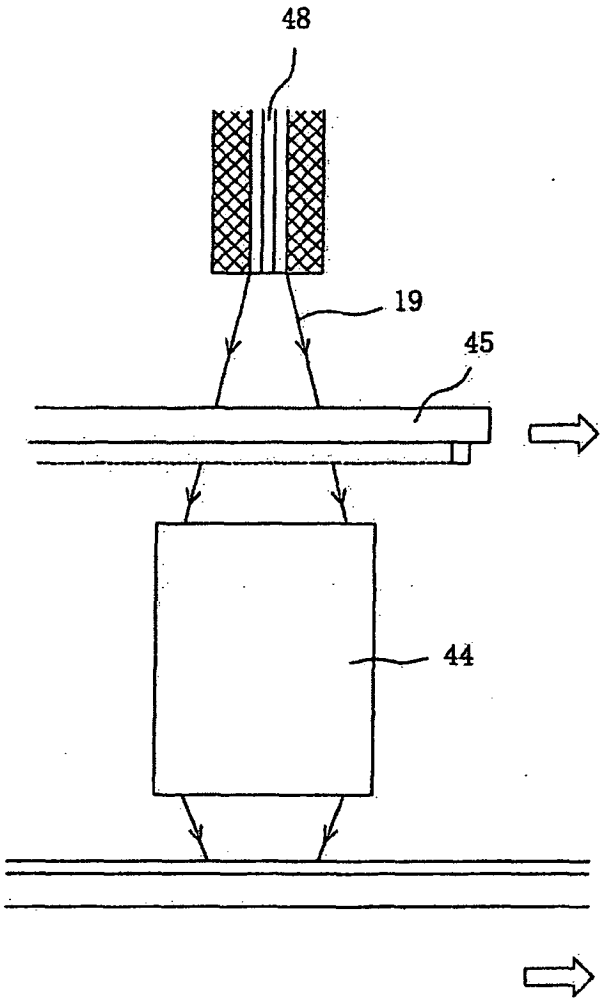


FIG. 20(A)

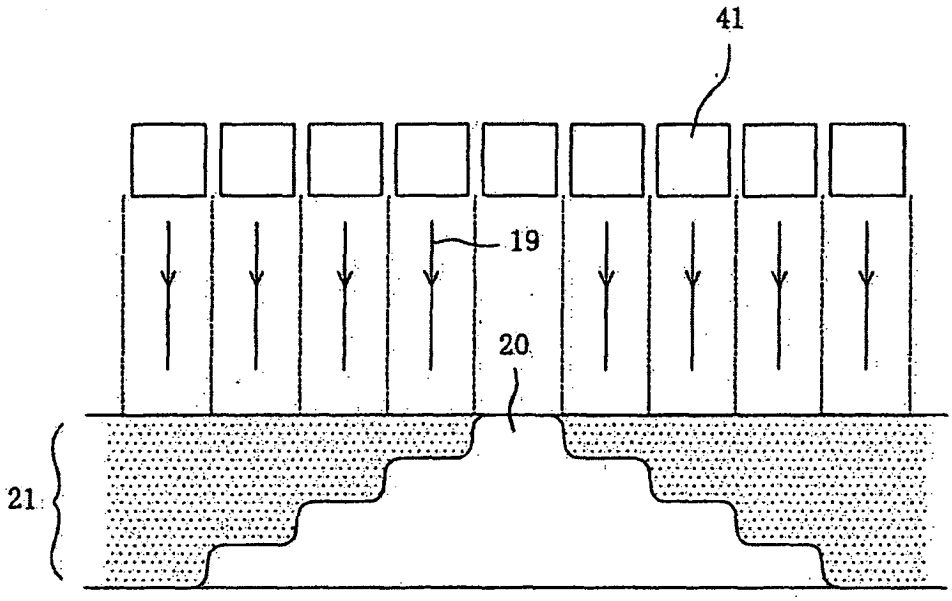


FIG. 20(B)

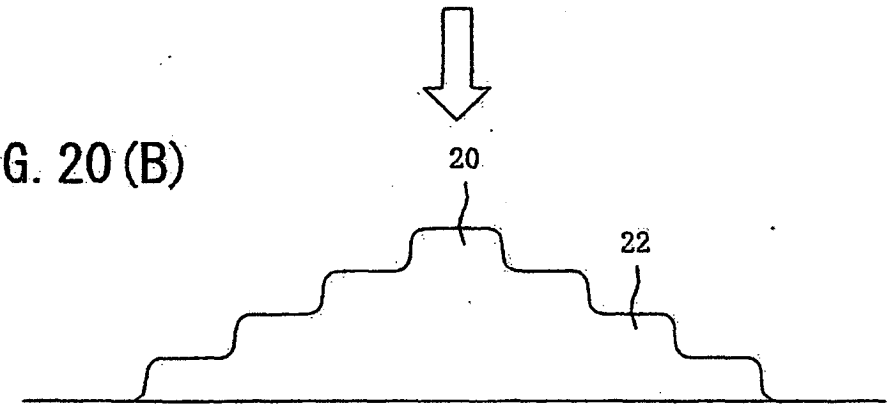


FIG. 21

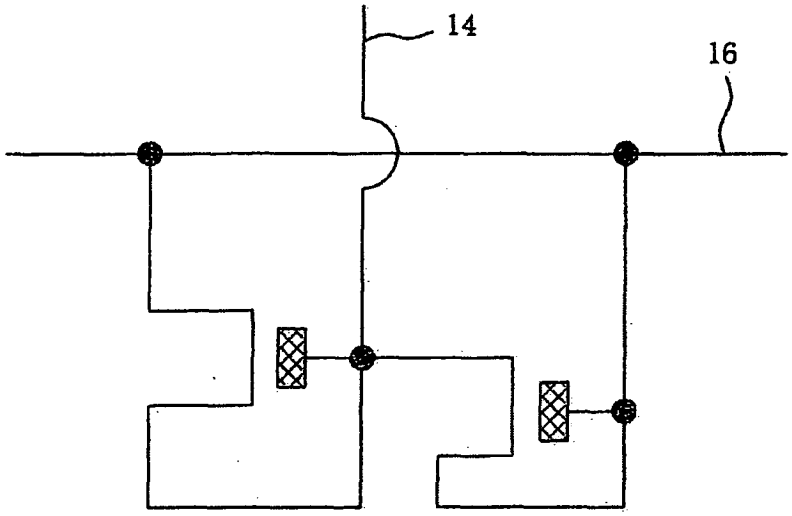


FIG. 22

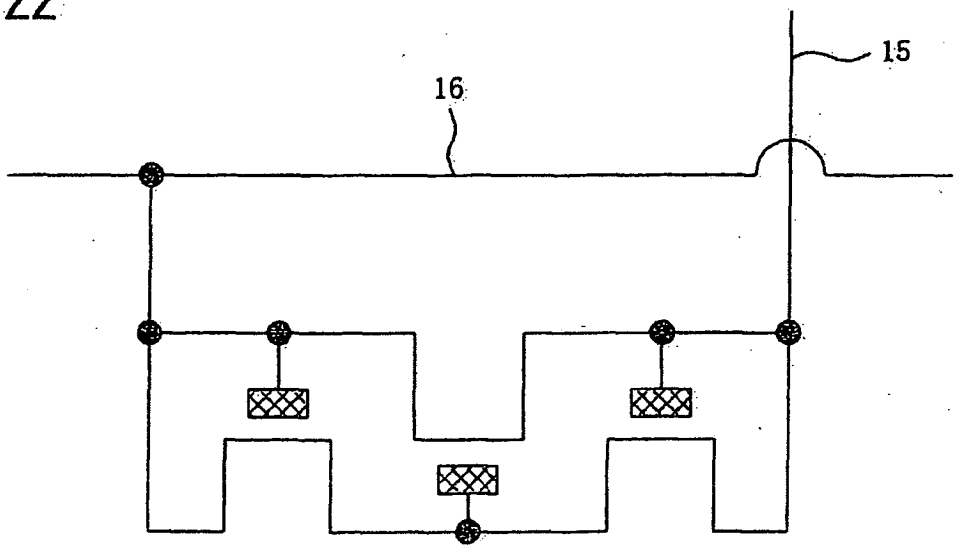


FIG. 23

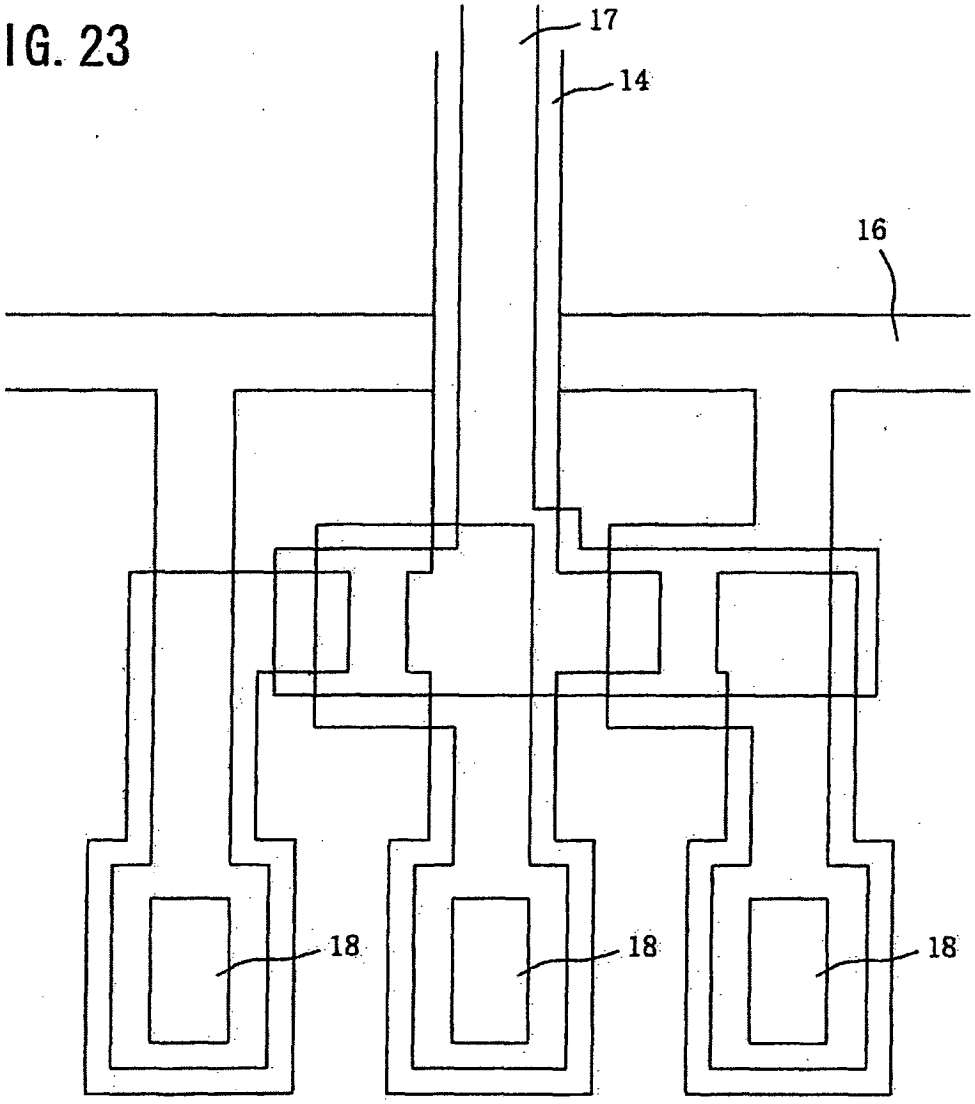


FIG. 24

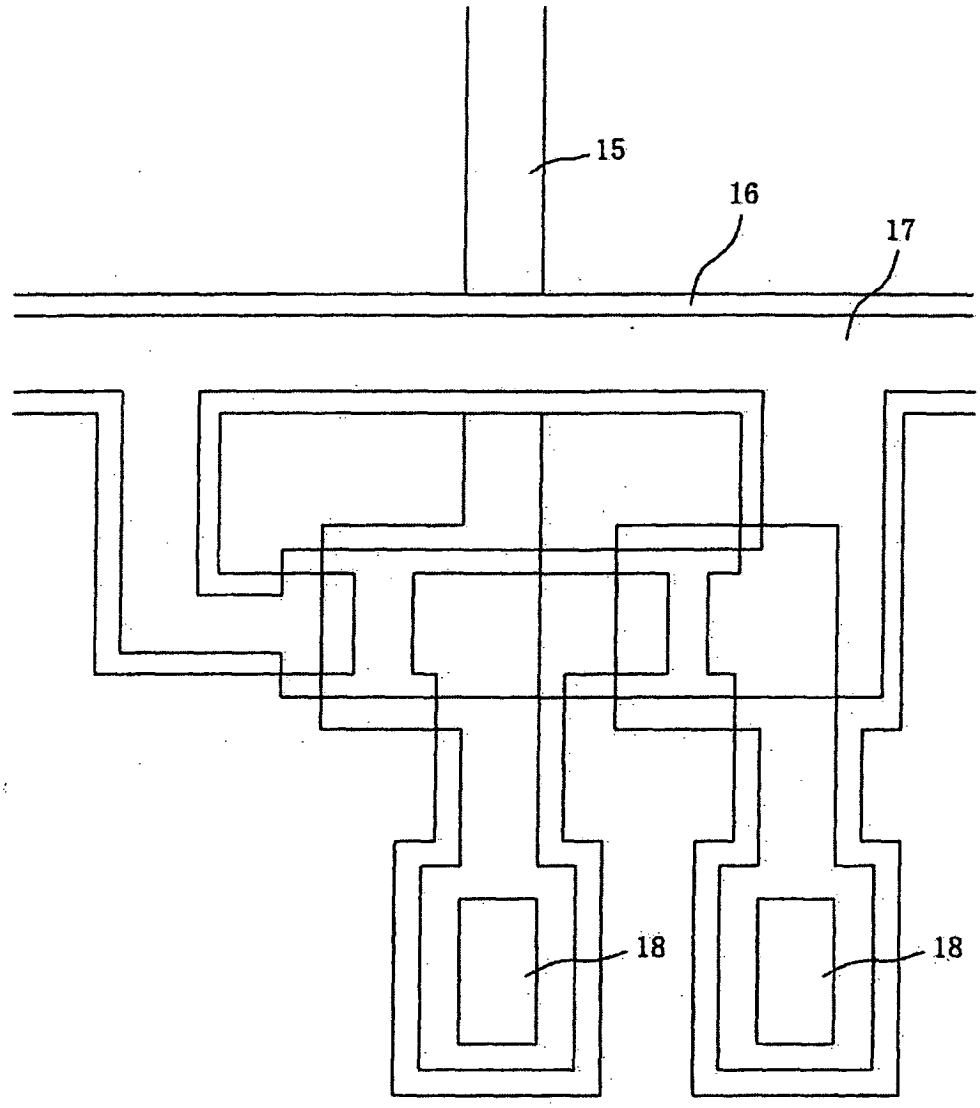


FIG. 25

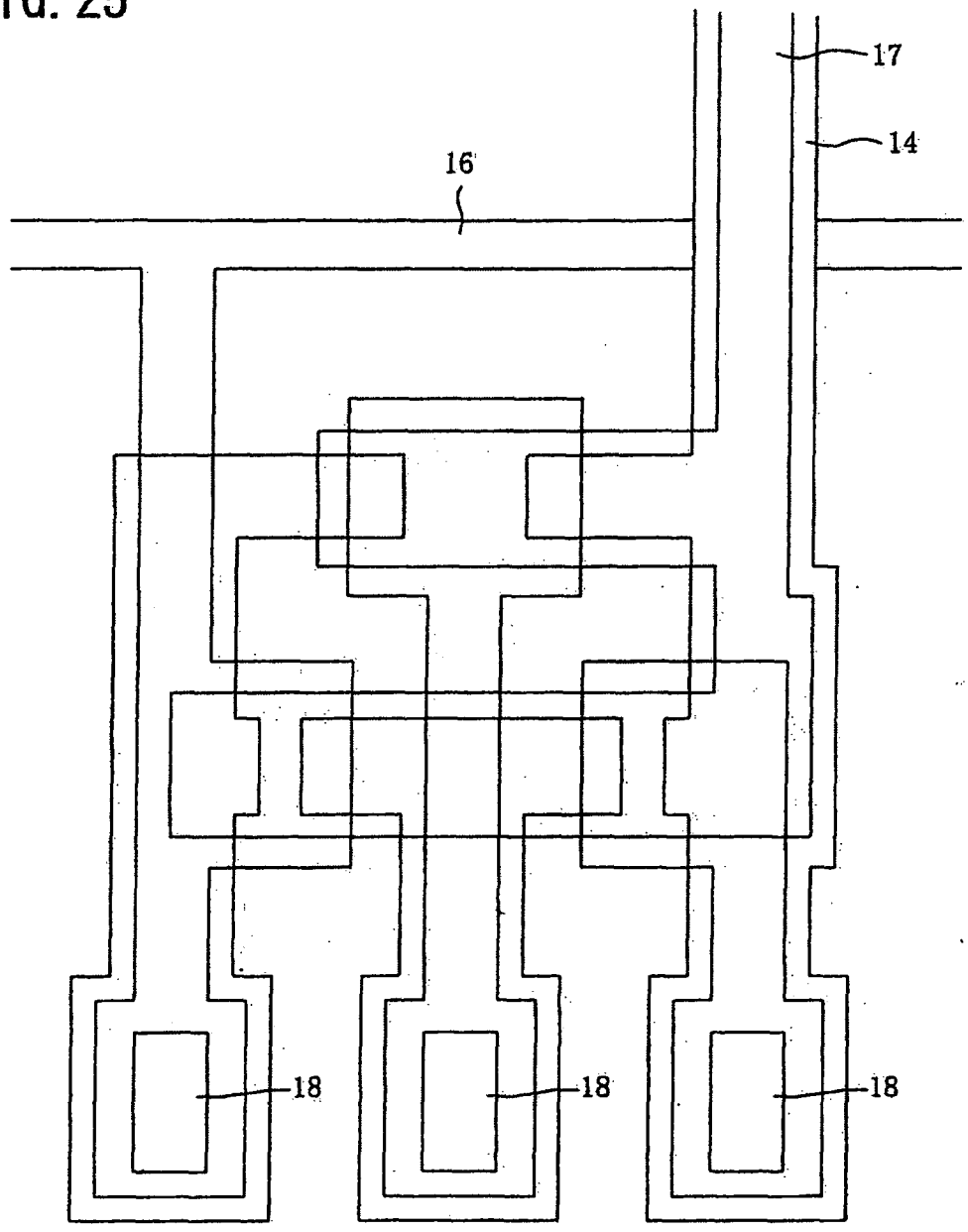


FIG. 26

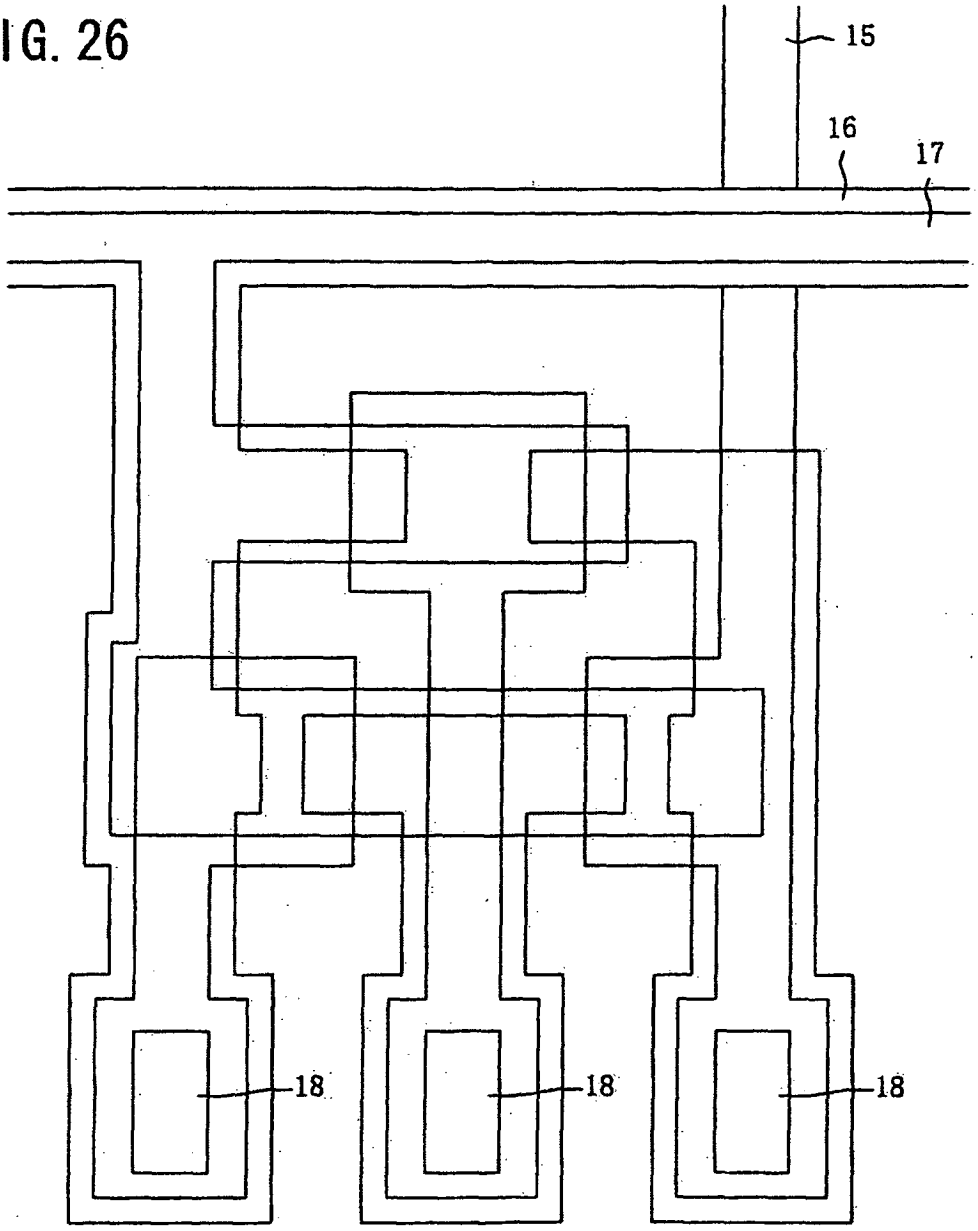


FIG. 27 (A)

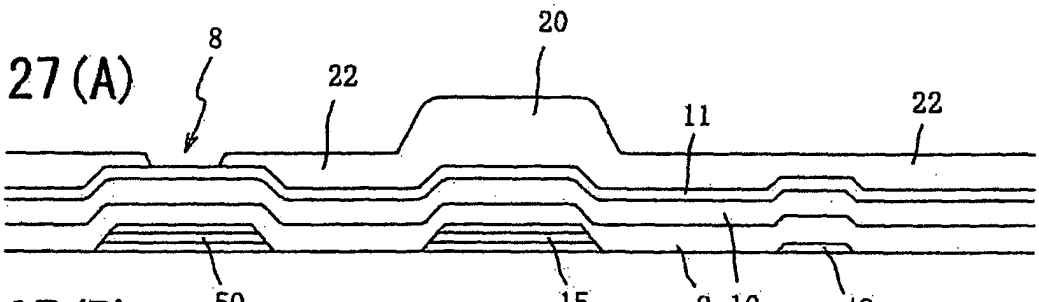


FIG. 27 (B)

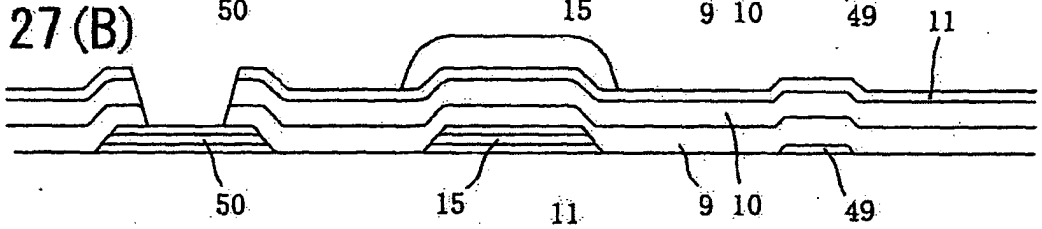


FIG. 27 (C)

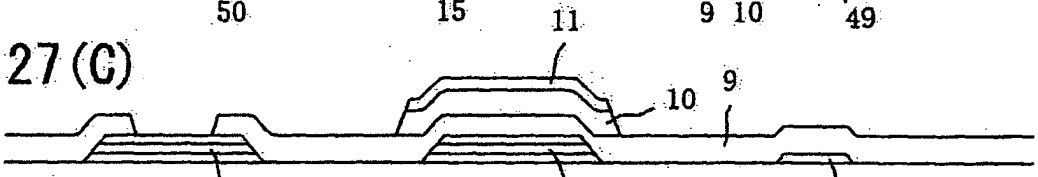


FIG. 27 (D)

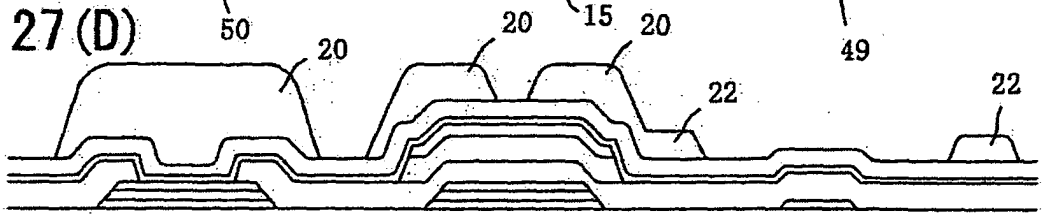


FIG. 27 (E)

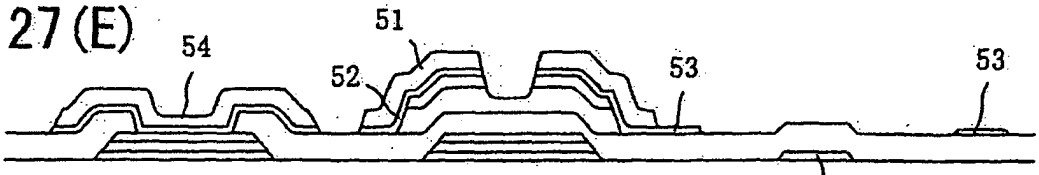


FIG. 27 (F)

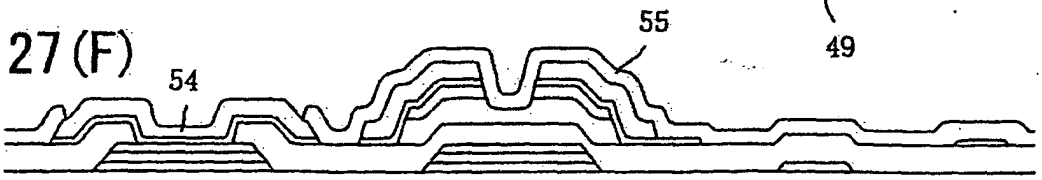


FIG. 28 (A)

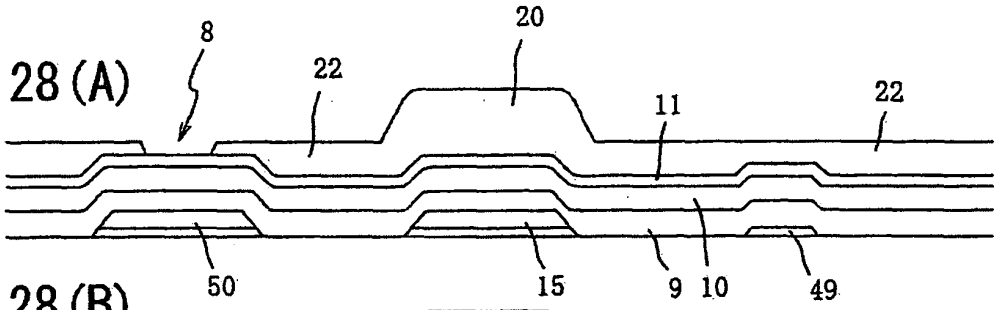


FIG. 28 (B)

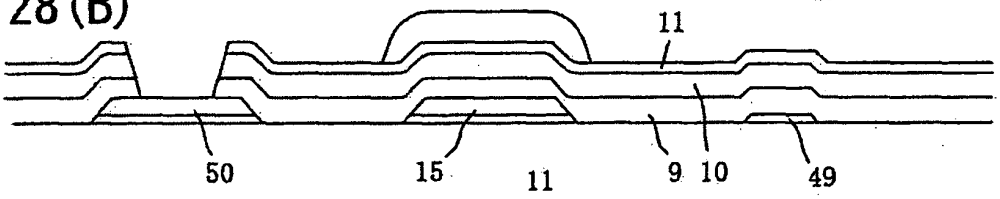


FIG. 28 (C)

FIG. 28 (D)

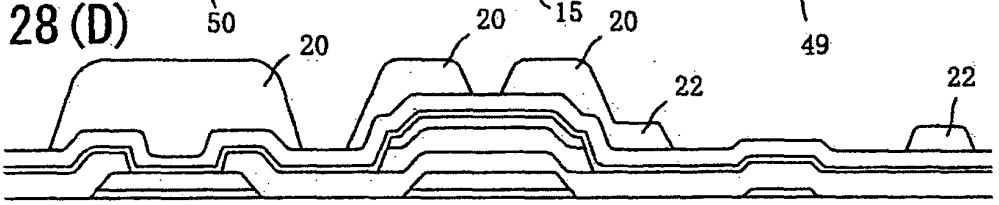


FIG. 28 (E)

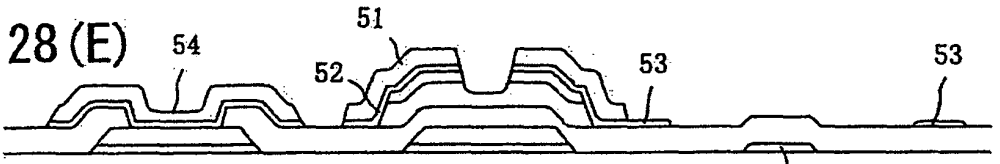


FIG. 28 (F)

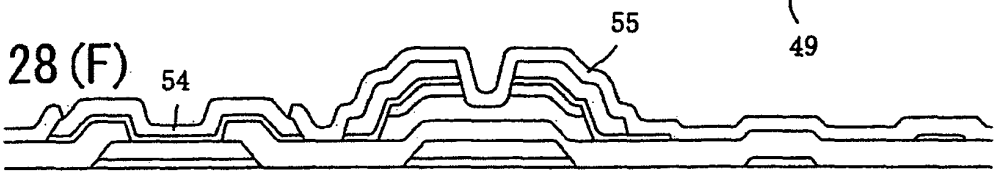


FIG. 29

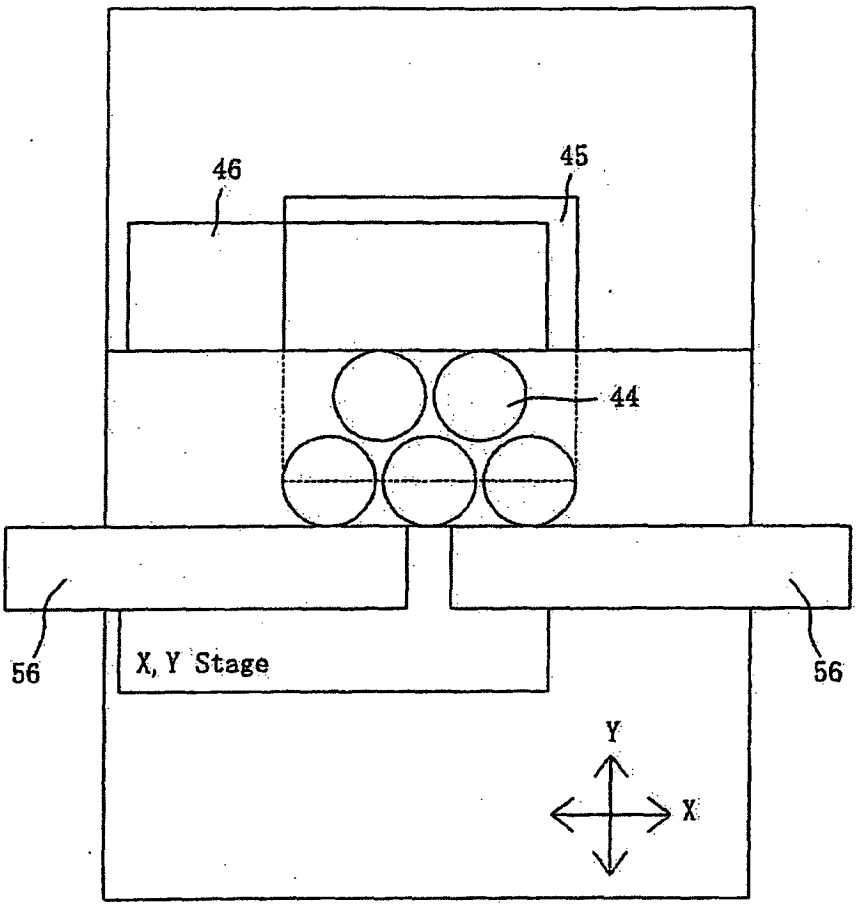


FIG. 30

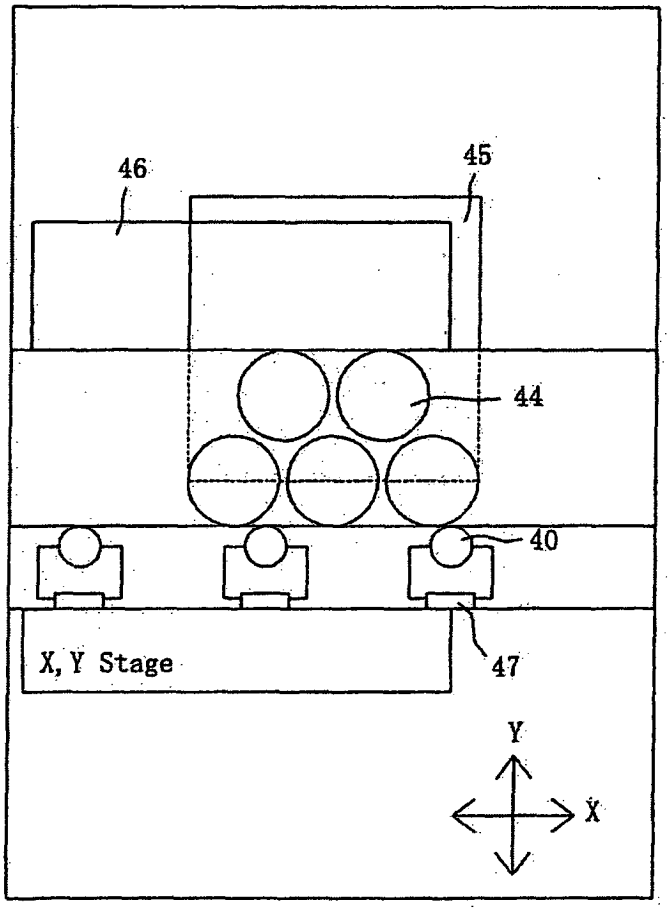


FIG. 31

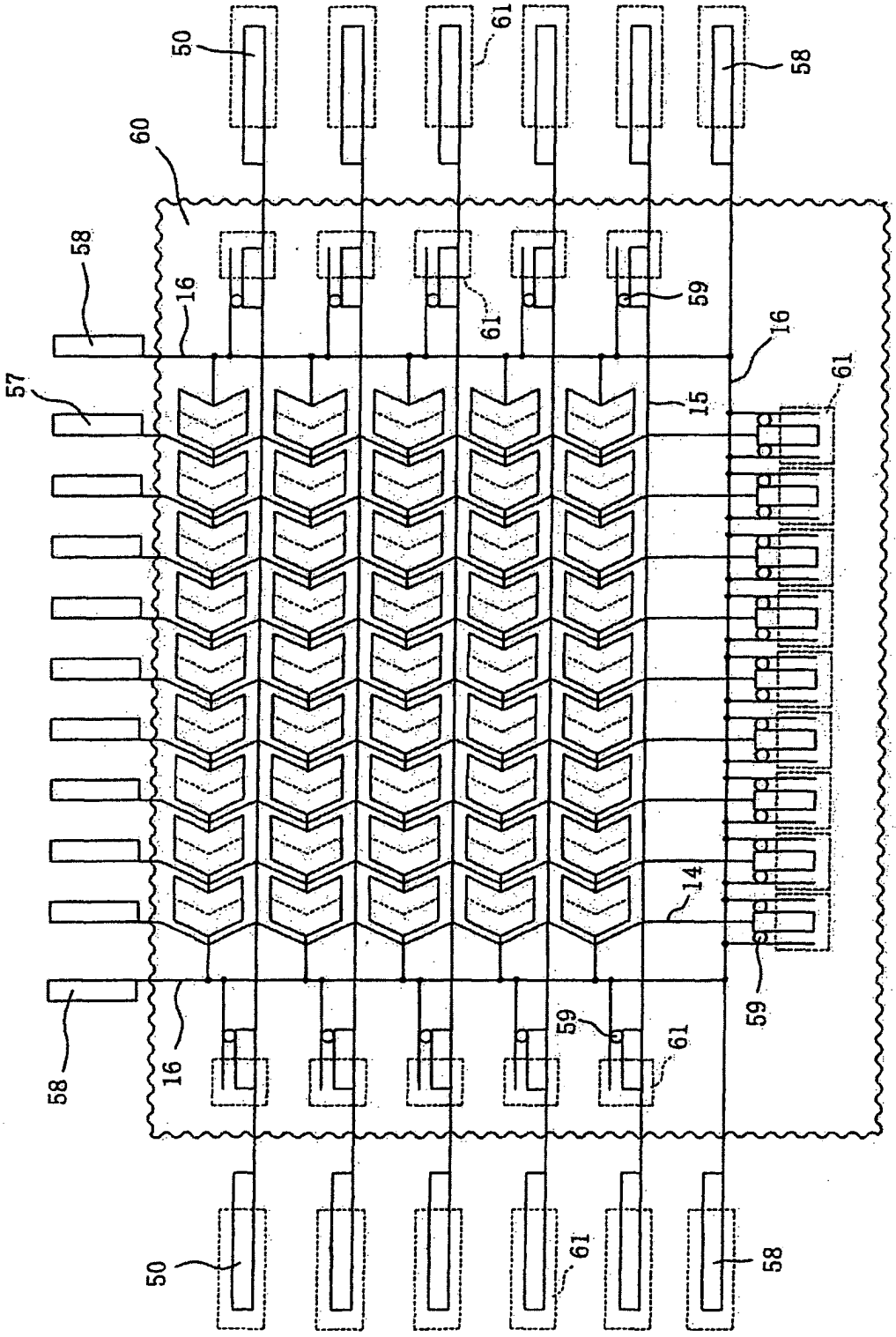


FIG. 32(A)

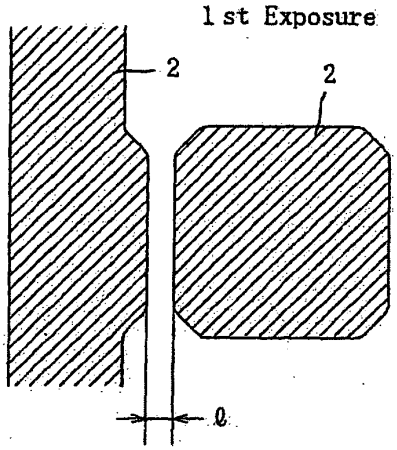


FIG. 32(C)

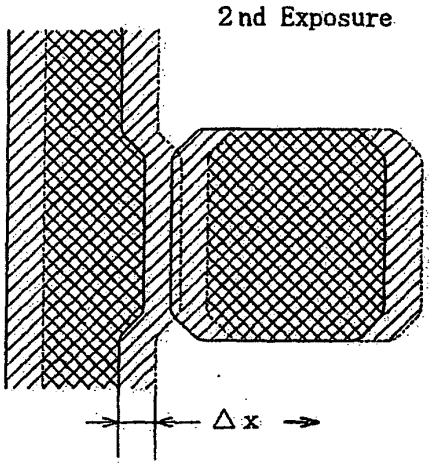


FIG. 32(B)

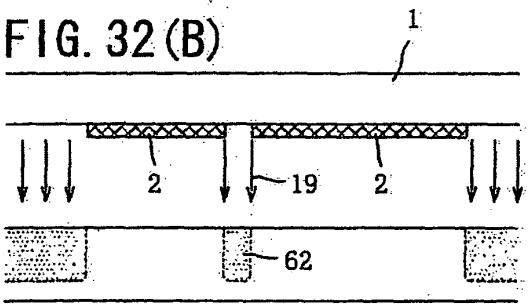


FIG. 32(D)

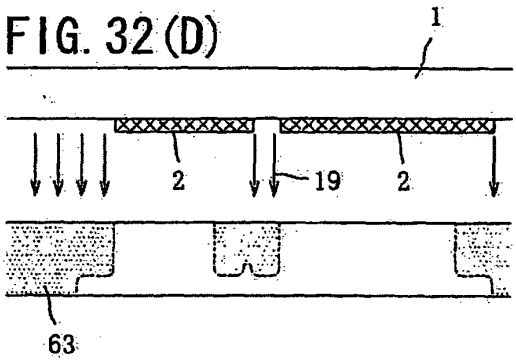


FIG. 32(E)

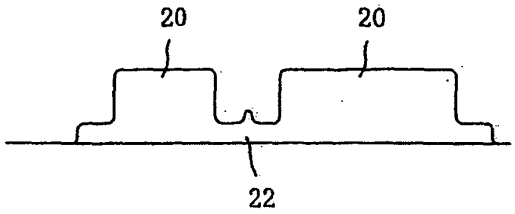


FIG. 33 (B)

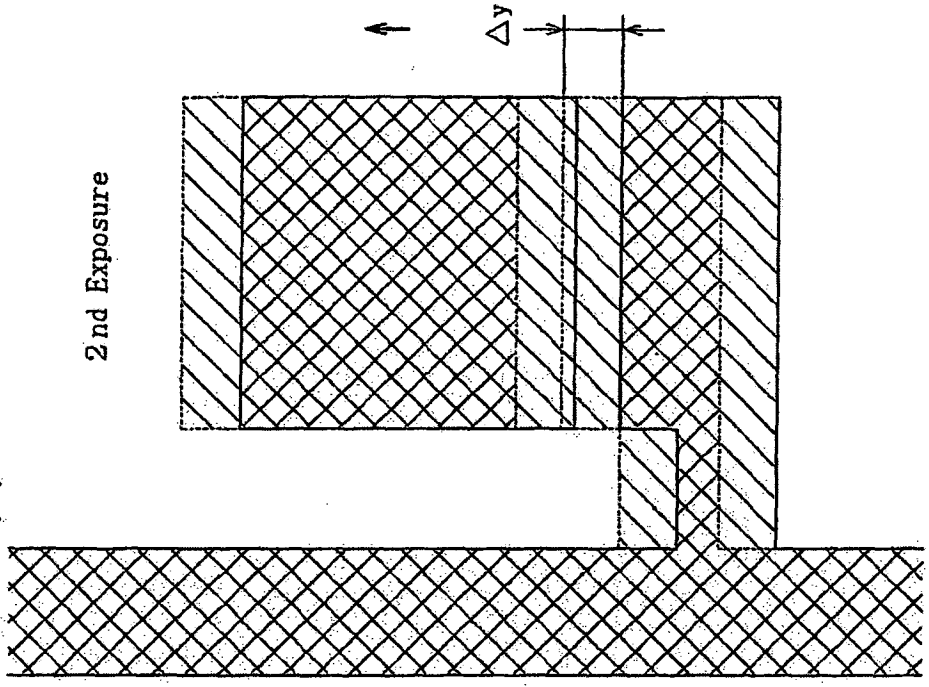


FIG. 33 (A)

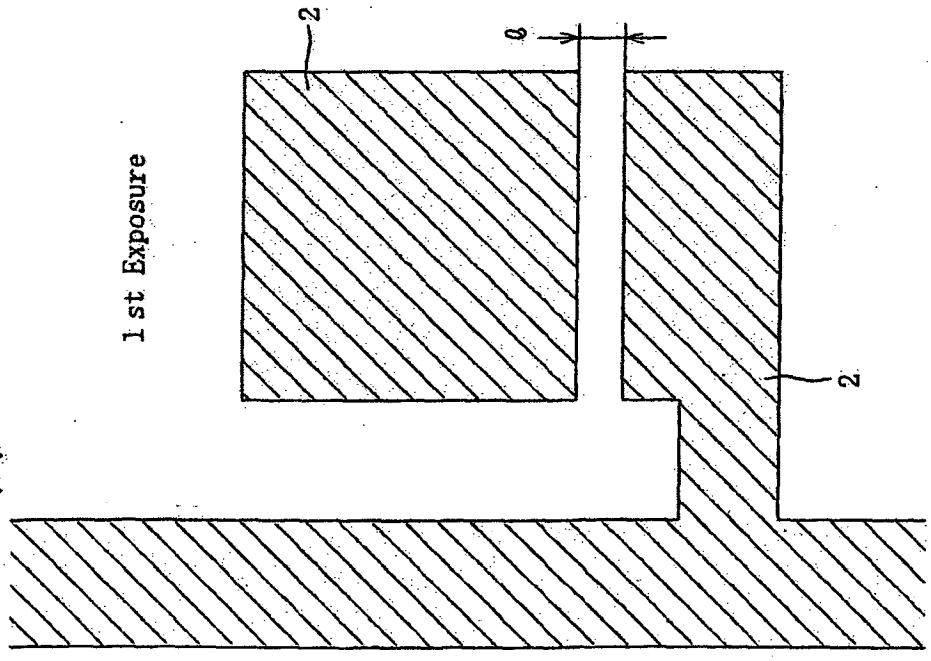


FIG. 34 (A) 1 st Exposure

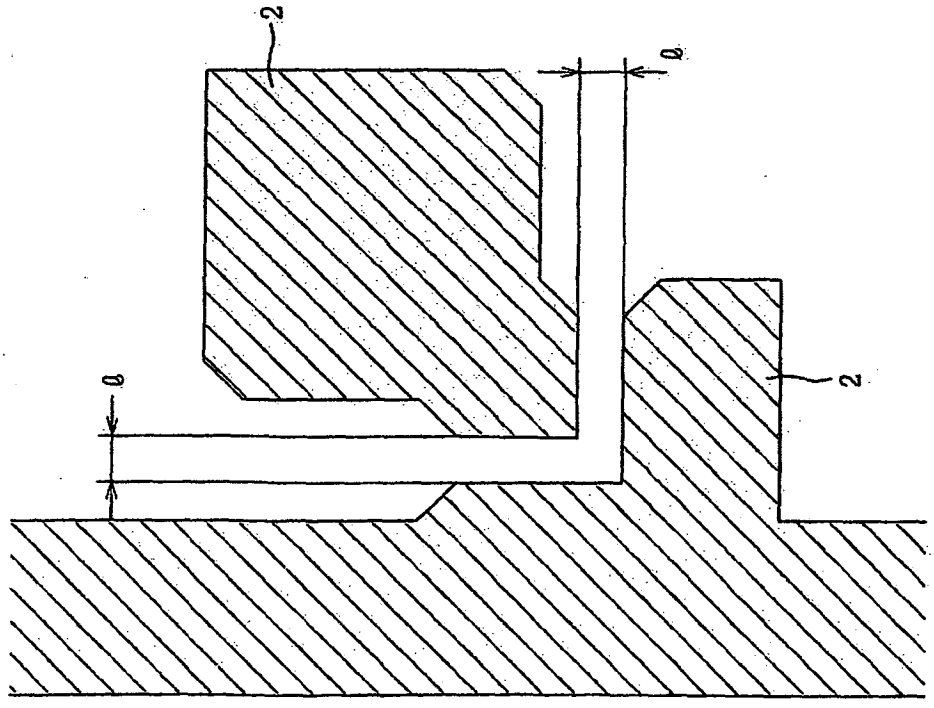


FIG. 34 (B) 2nd Exposure

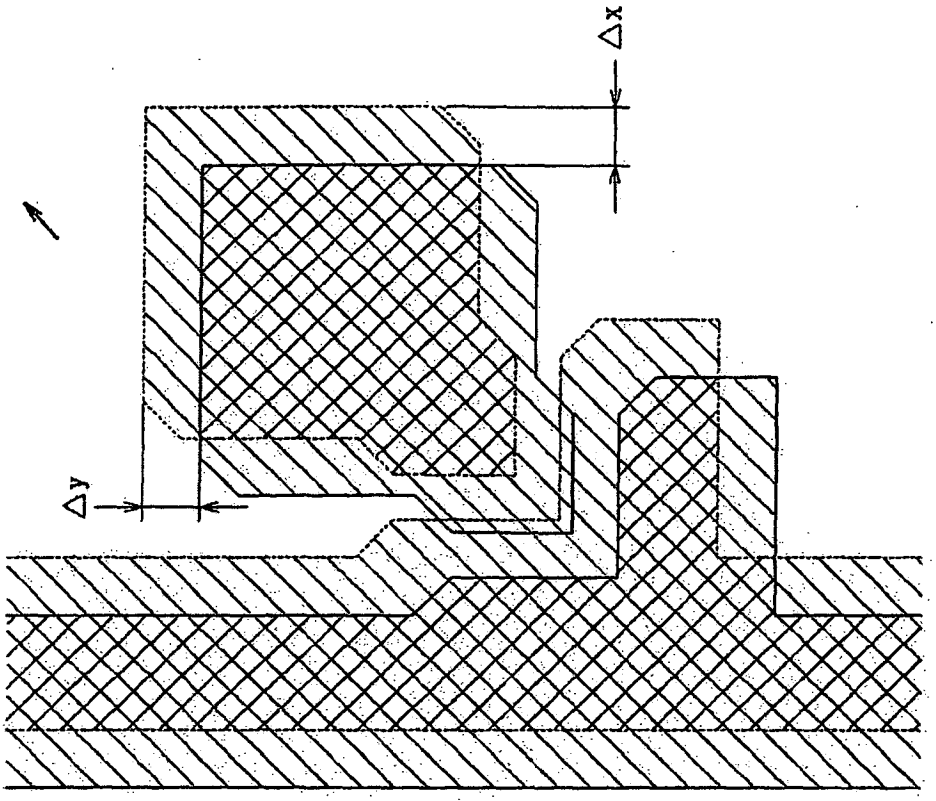


FIG. 35 (A)

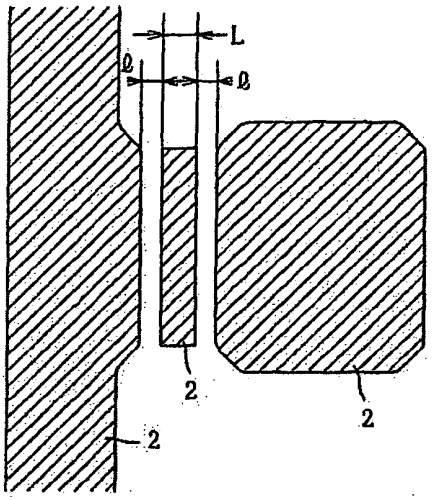


FIG. 35 (C)

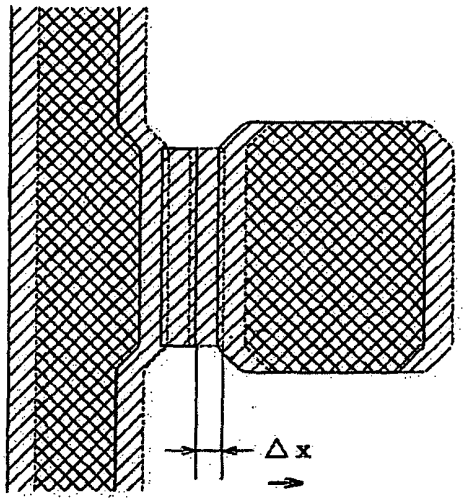


FIG. 35 (B)

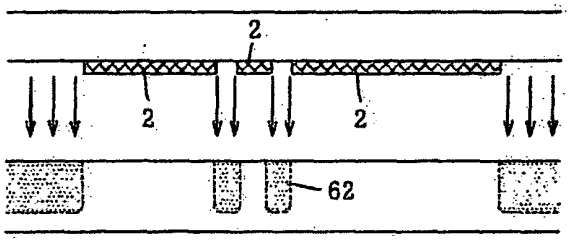


FIG. 35 (D)

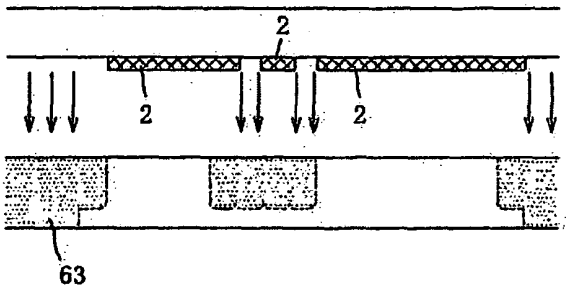


FIG. 35 (E)

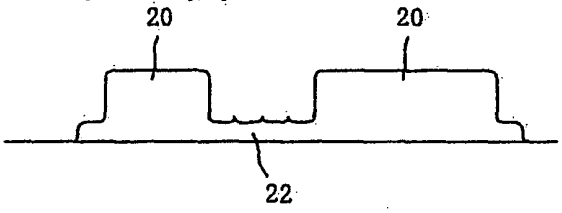


FIG. 36 (A)

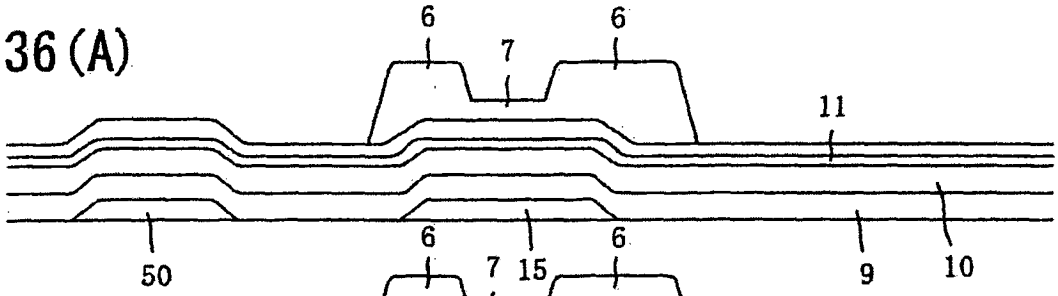


FIG. 36 (B)

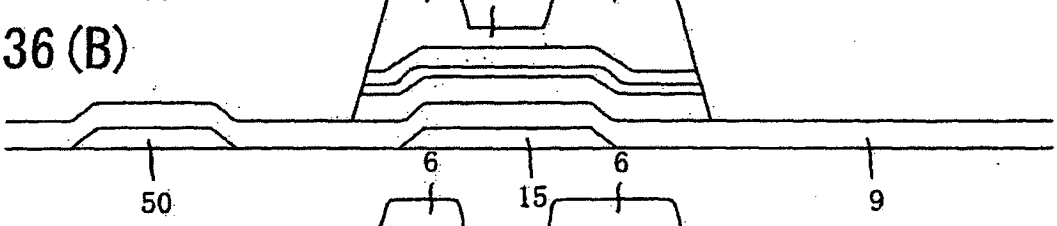


FIG. 36 (C)

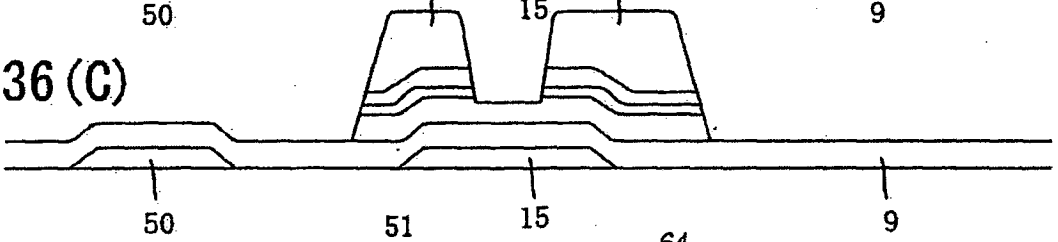


FIG. 36 (D)

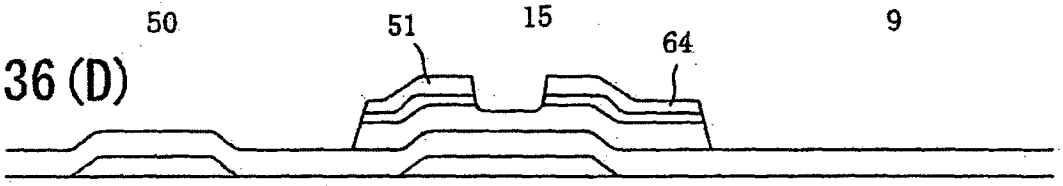


FIG. 36 (E)

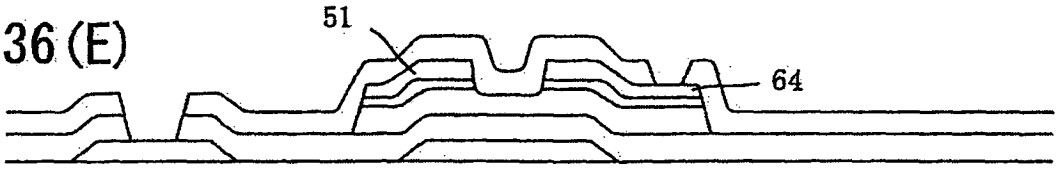


FIG. 36 (F)

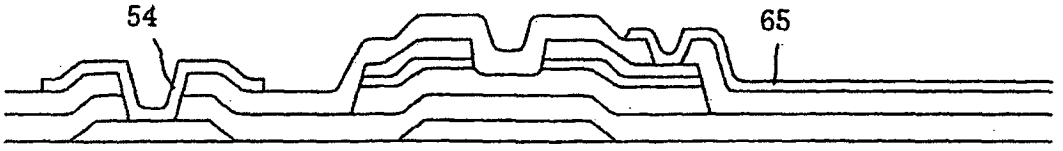


FIG. 37(A) 1st Exposure

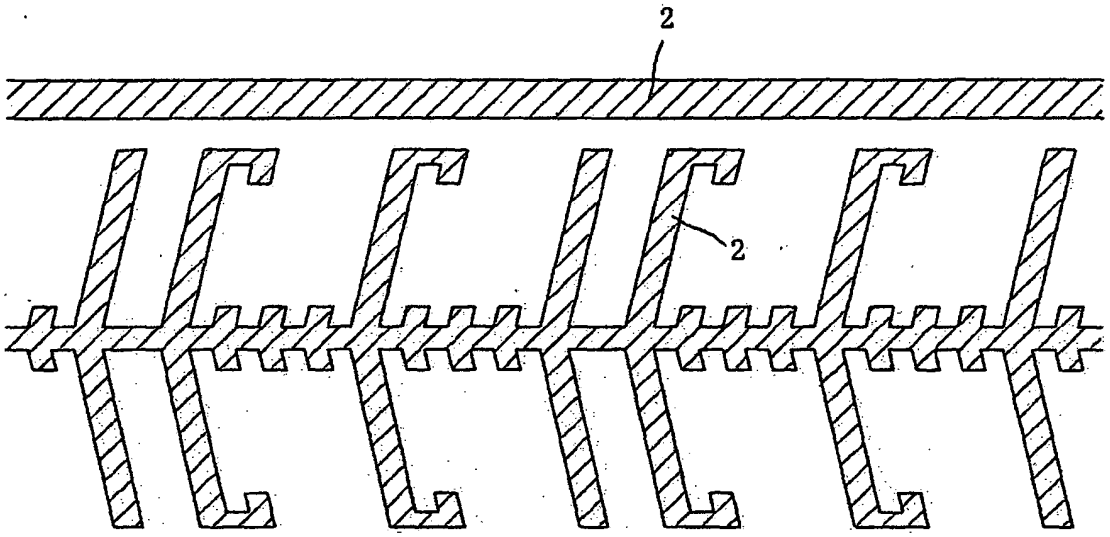


FIG. 37(B) 2nd Exposure

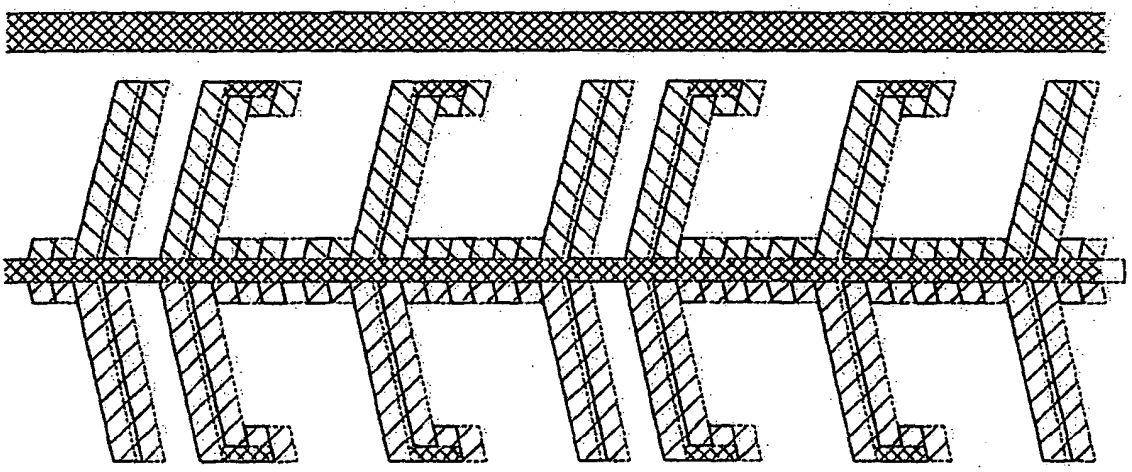


FIG. 38 (A) 1 st Exposure

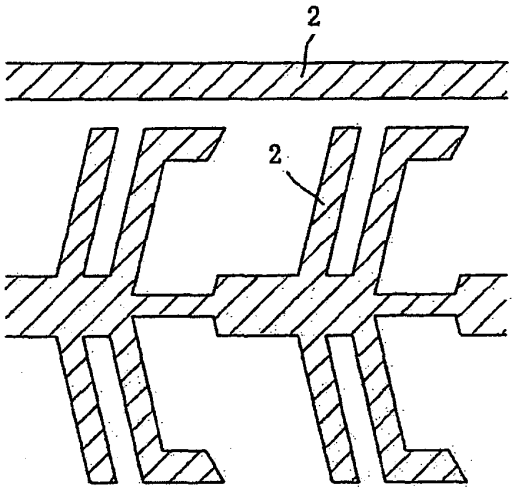


FIG. 38 (B) 2nd Exposure

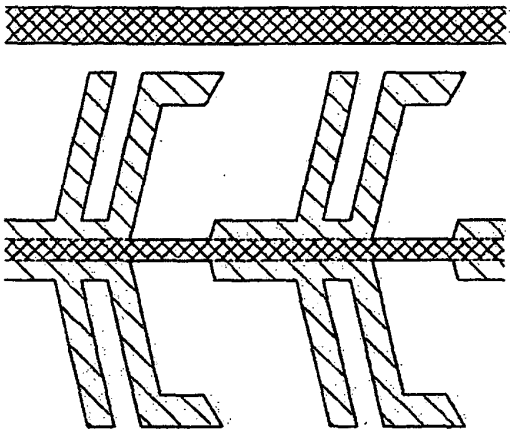


FIG. 39 (A) 1 st Exposure

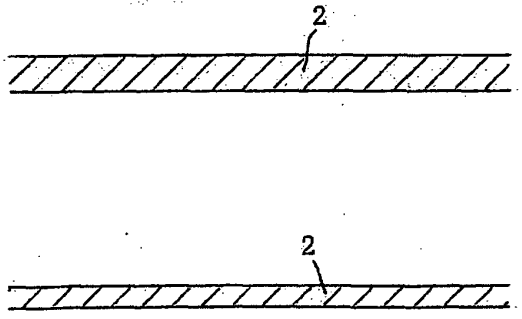


FIG. 39 (B) 2nd Exposure

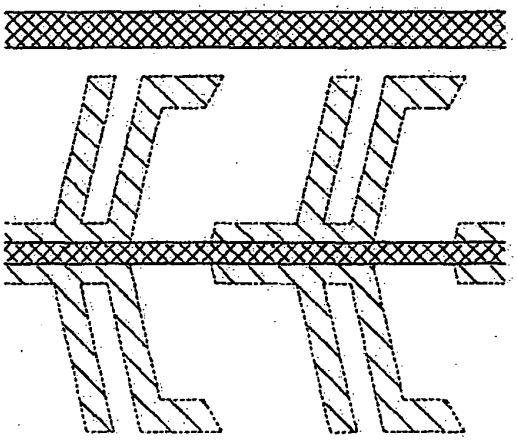


FIG. 40 (A) 1st Exposure

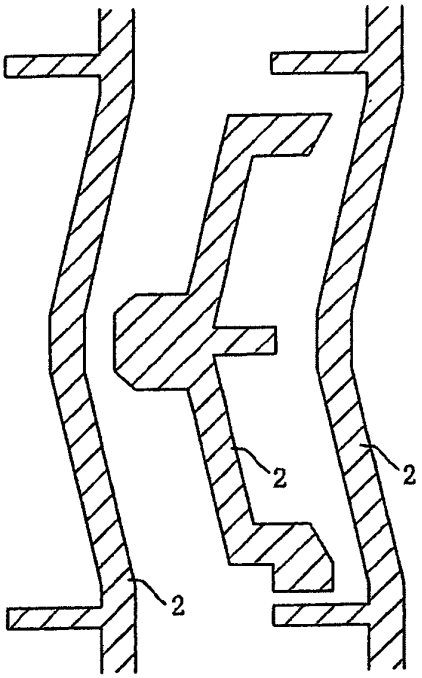


FIG. 40 (B) 2nd Exposure

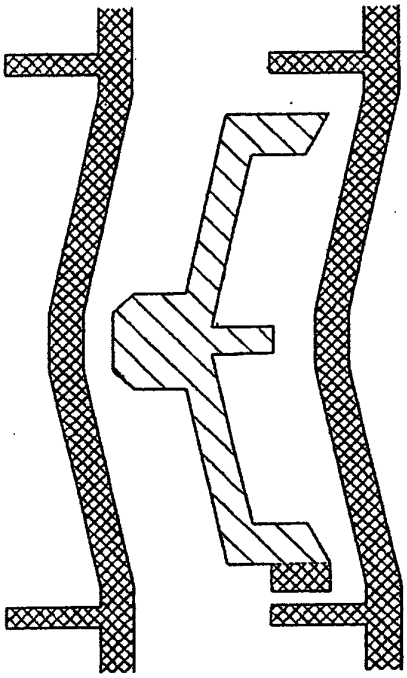


FIG. 41 (A) 1st Exposure

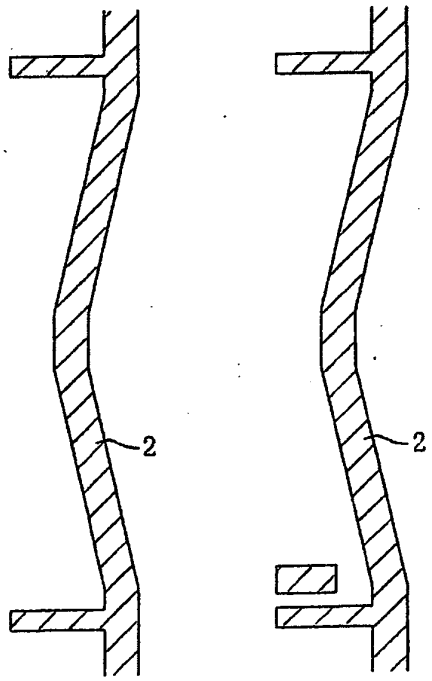


FIG. 41 (B) 2nd Exposure

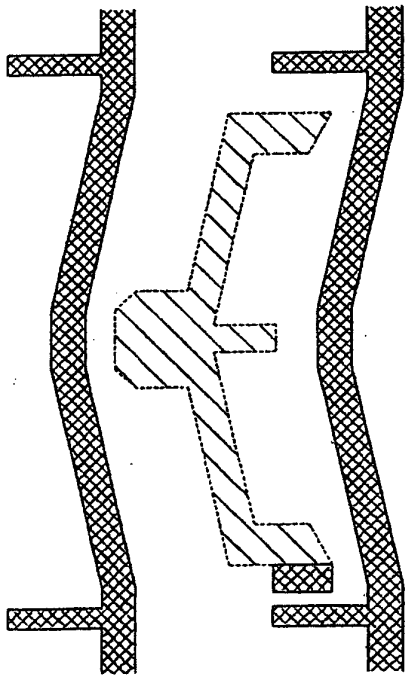


FIG. 42

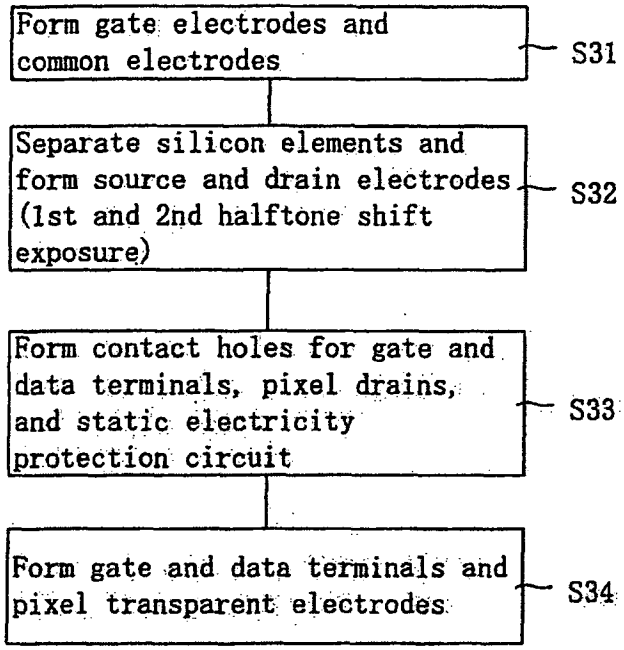

Form gate electrodes and common electrodes
S31
Separate silicon elements and form source and drain electrodes (1st and 2nd halftone shift exposure)
S32
Form contact holes for gate and data terminals, pixel drains, and static electricity protection circuit
S33
Form gate and data terminals and pixel transparent electrodes
S34

FIG. 43 (A) 1st Exposure

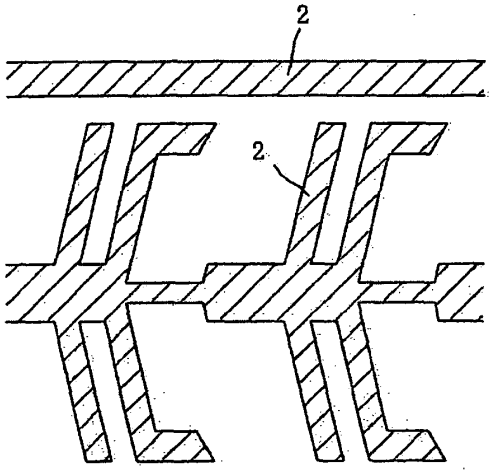


FIG. 43 (B) 2nd Exposure

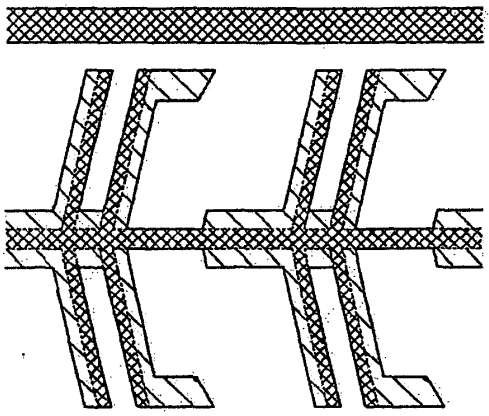


FIG. 44 (A) 1st Exposure

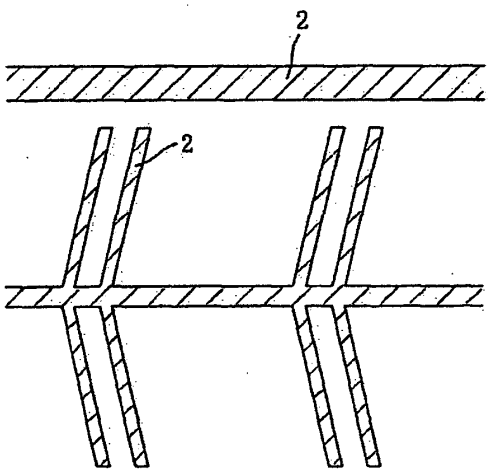


FIG. 44 (B) 2nd Exposure

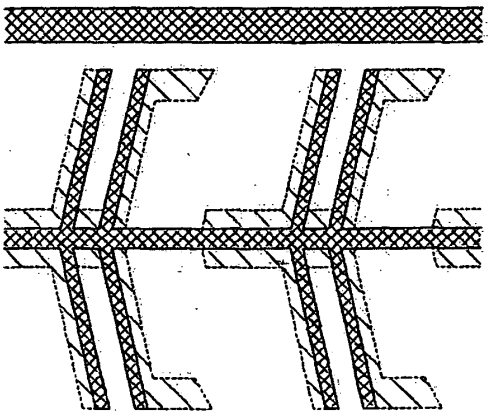


FIG. 45

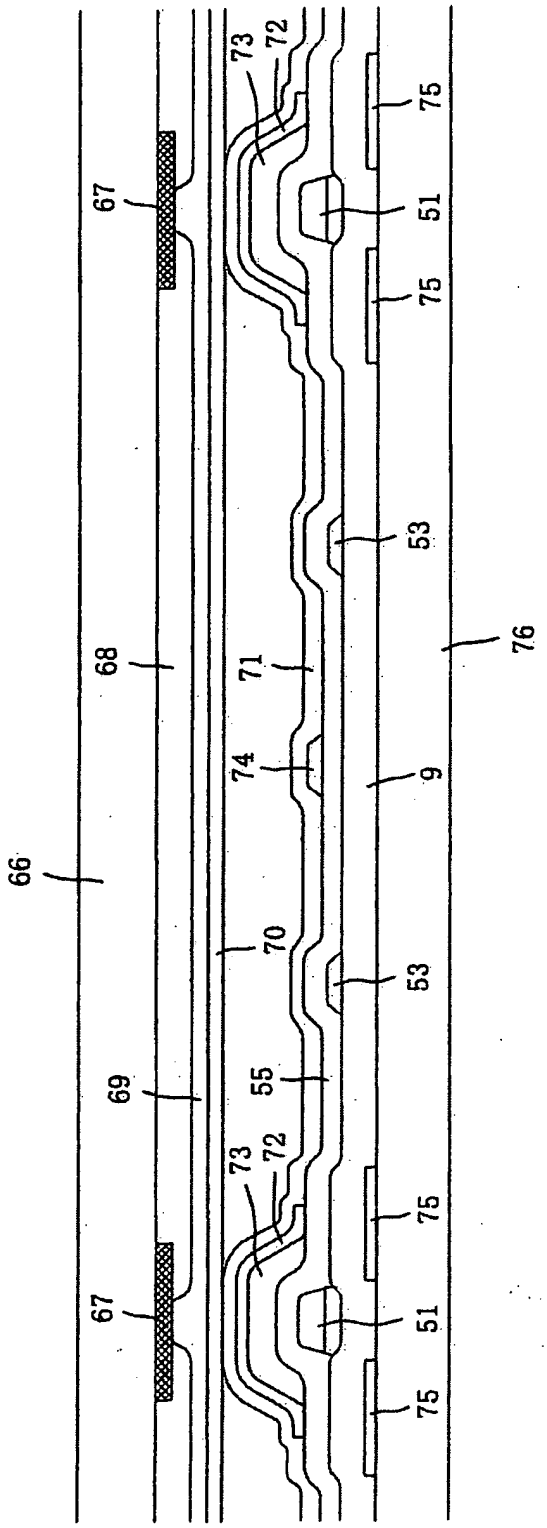


FIG. 46

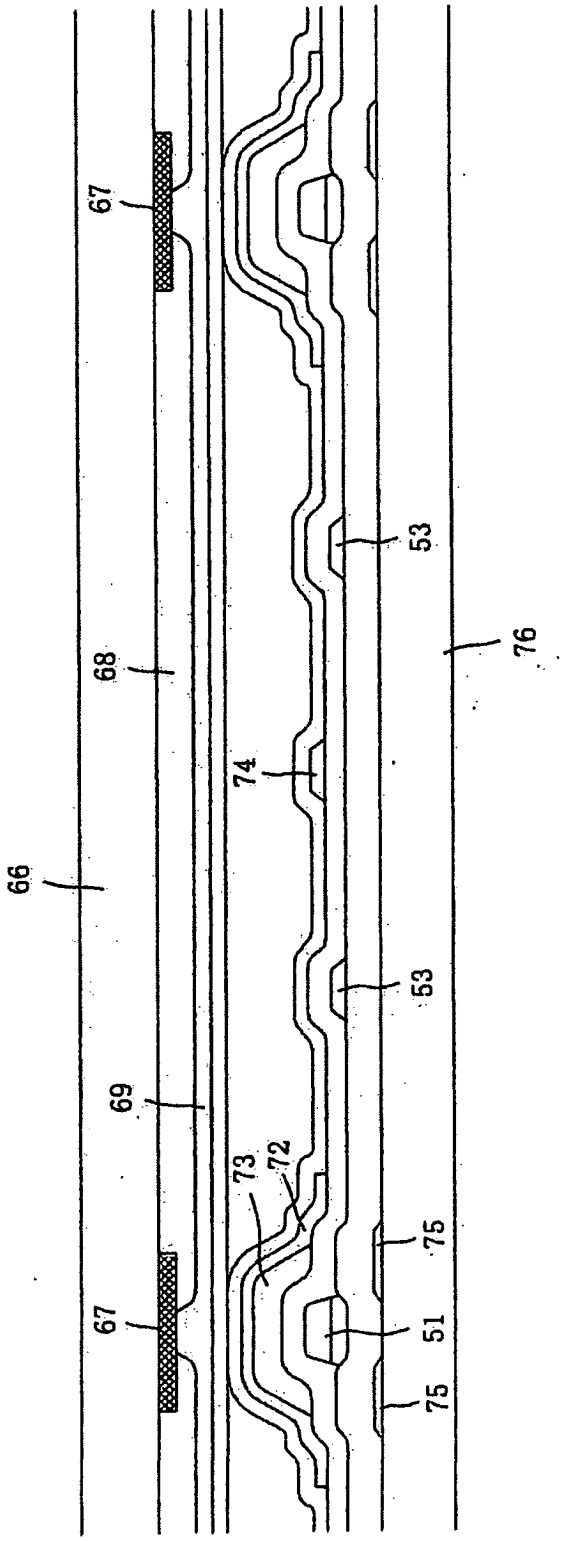


FIG. 47

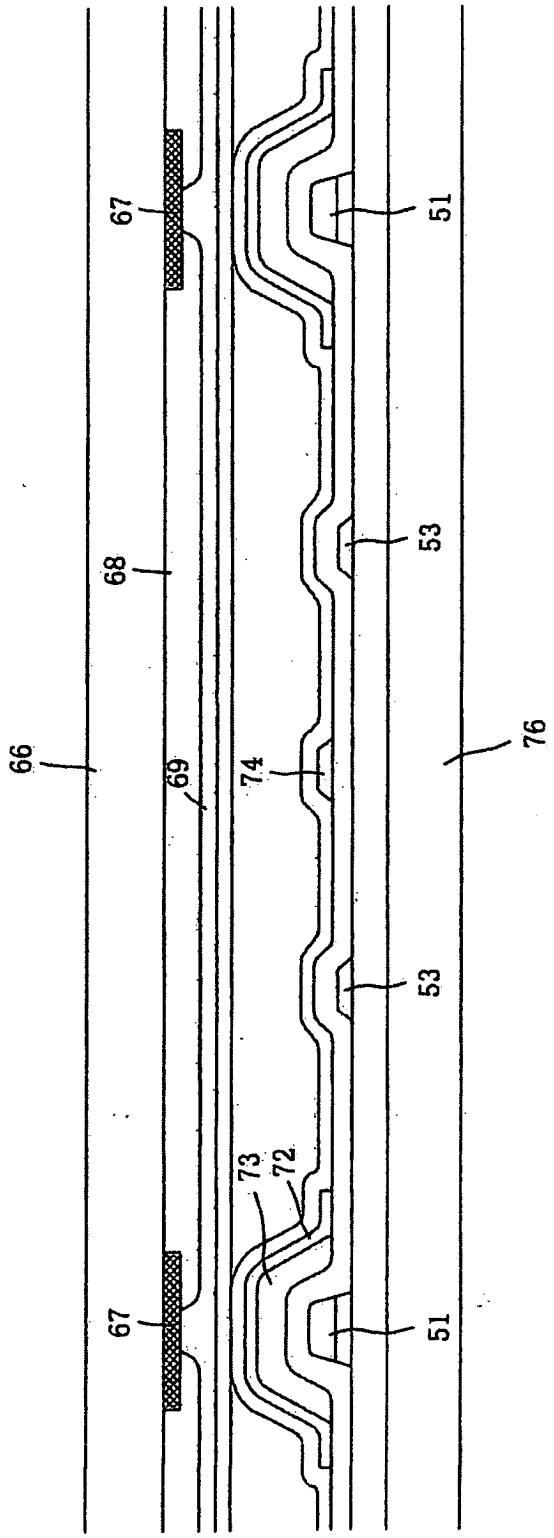


FIG. 48

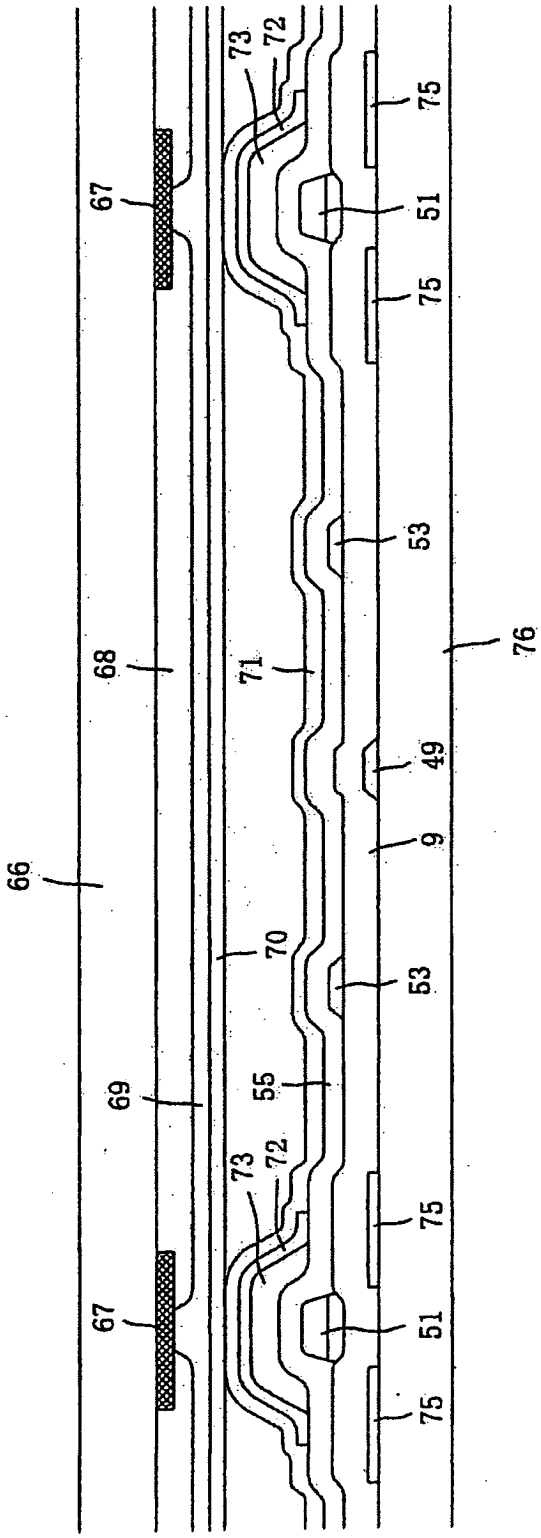
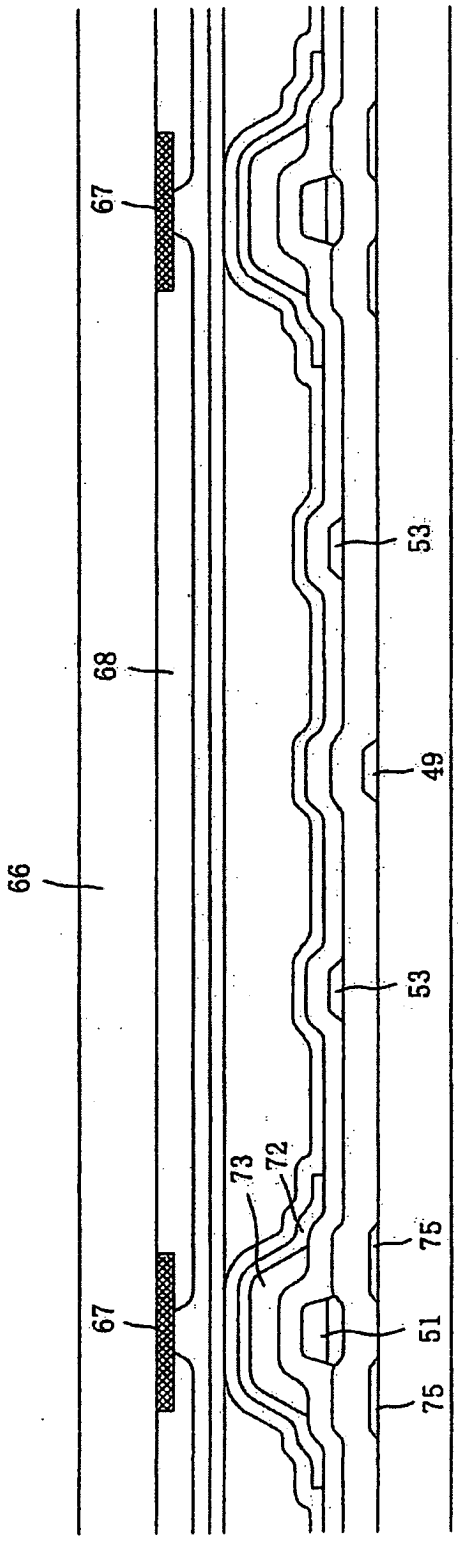


FIG. 49



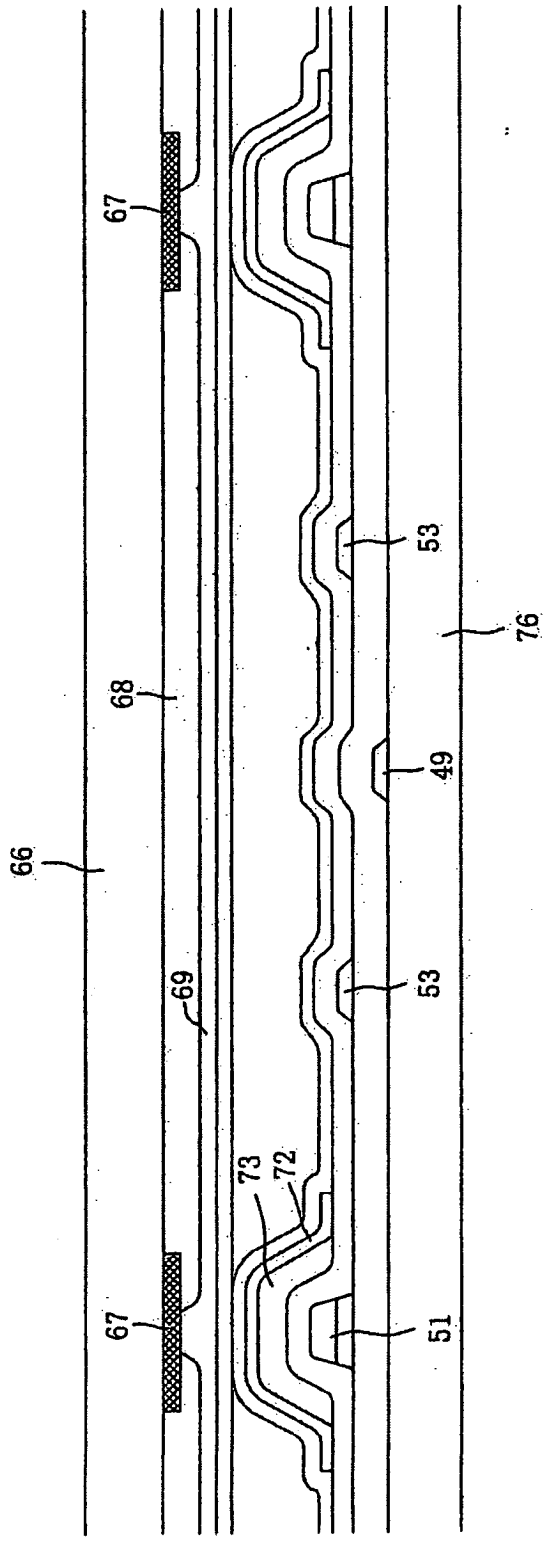


FIG. 50

FIG. 51

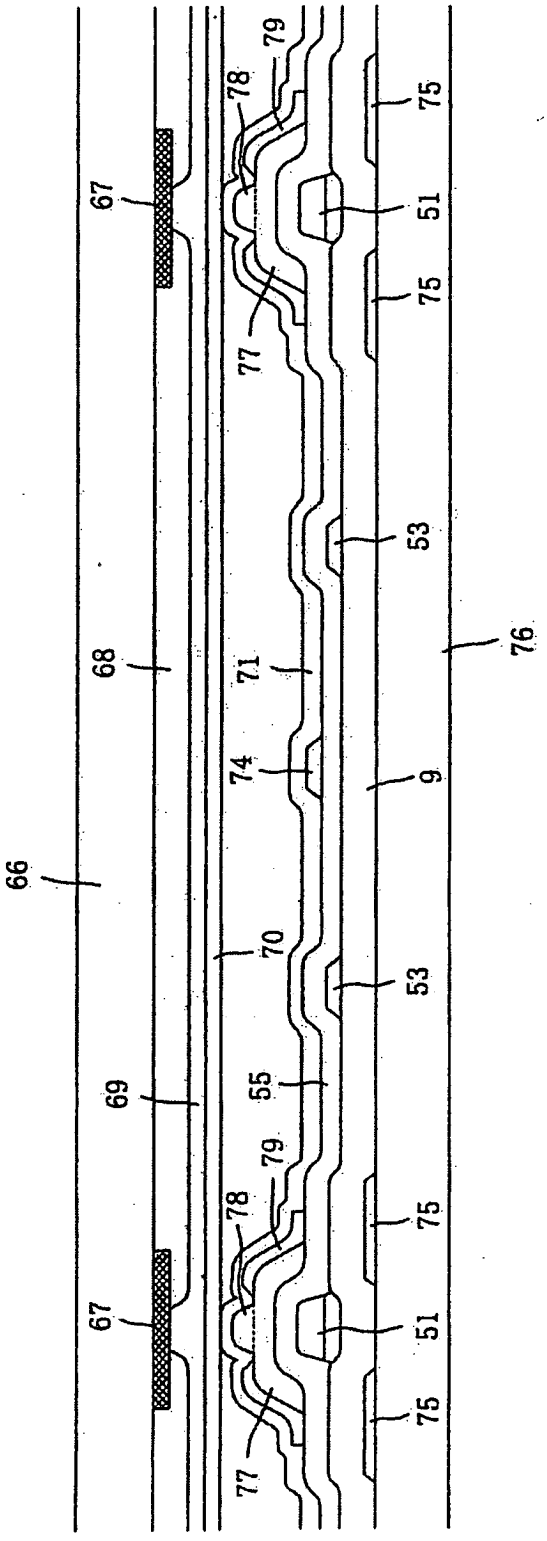


FIG. 52

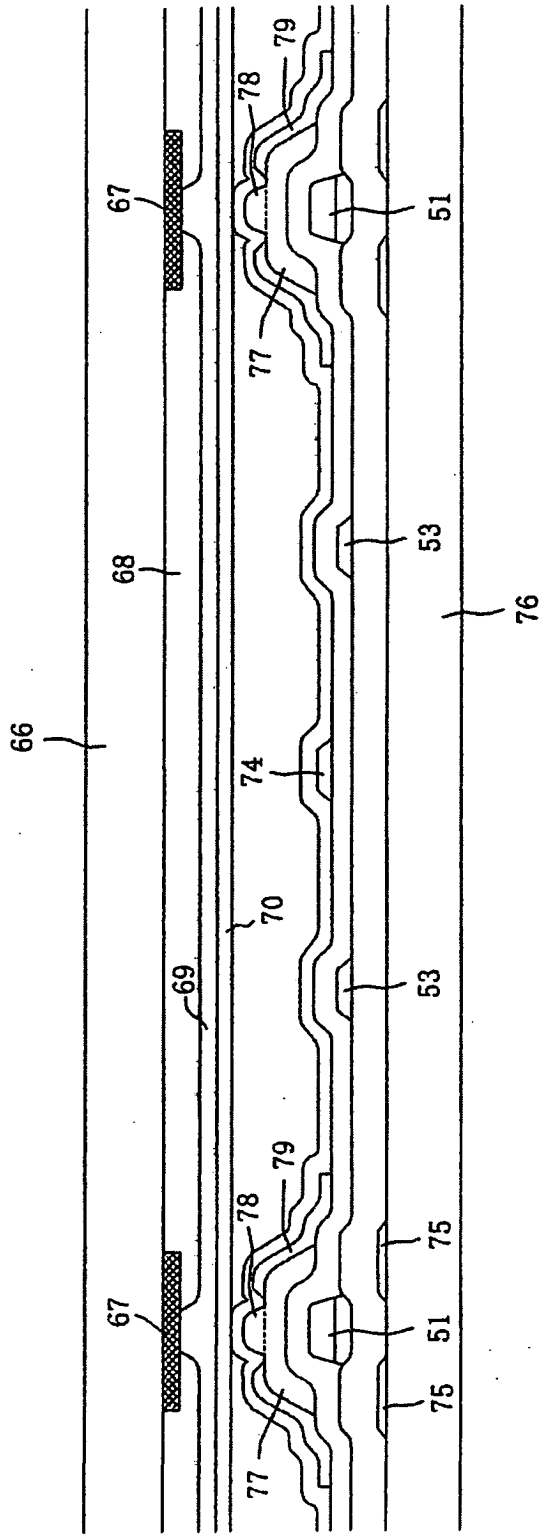

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FIG. 53

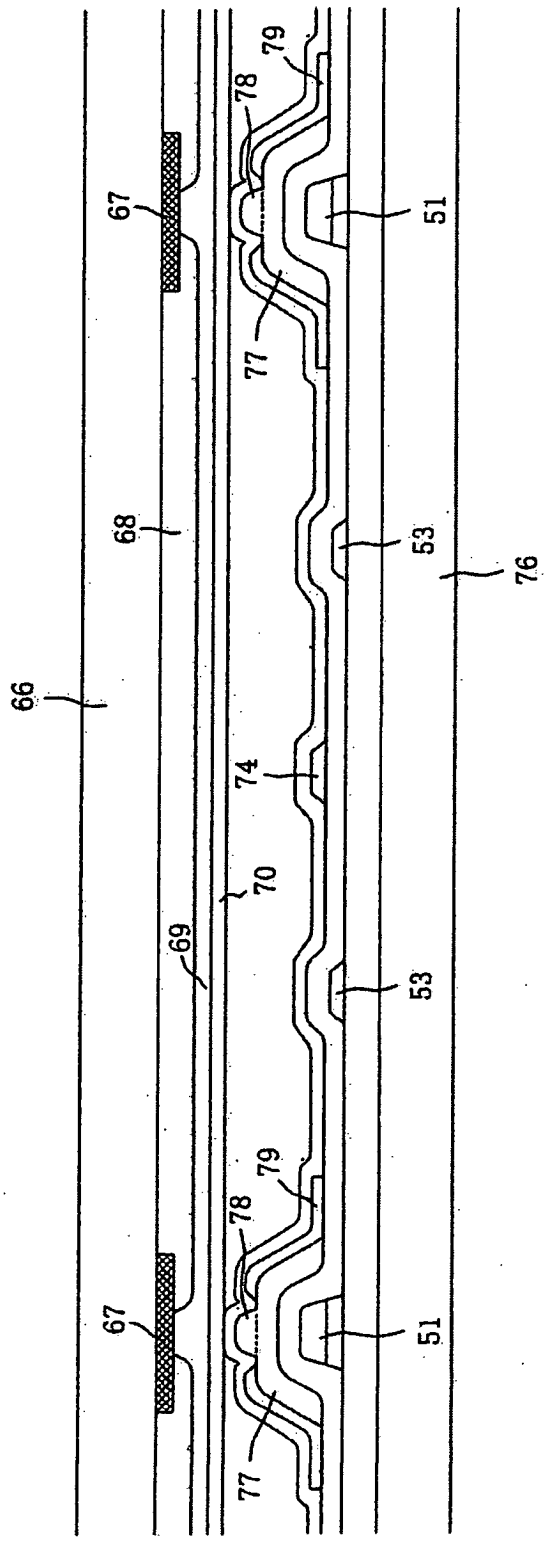


FIG. 54

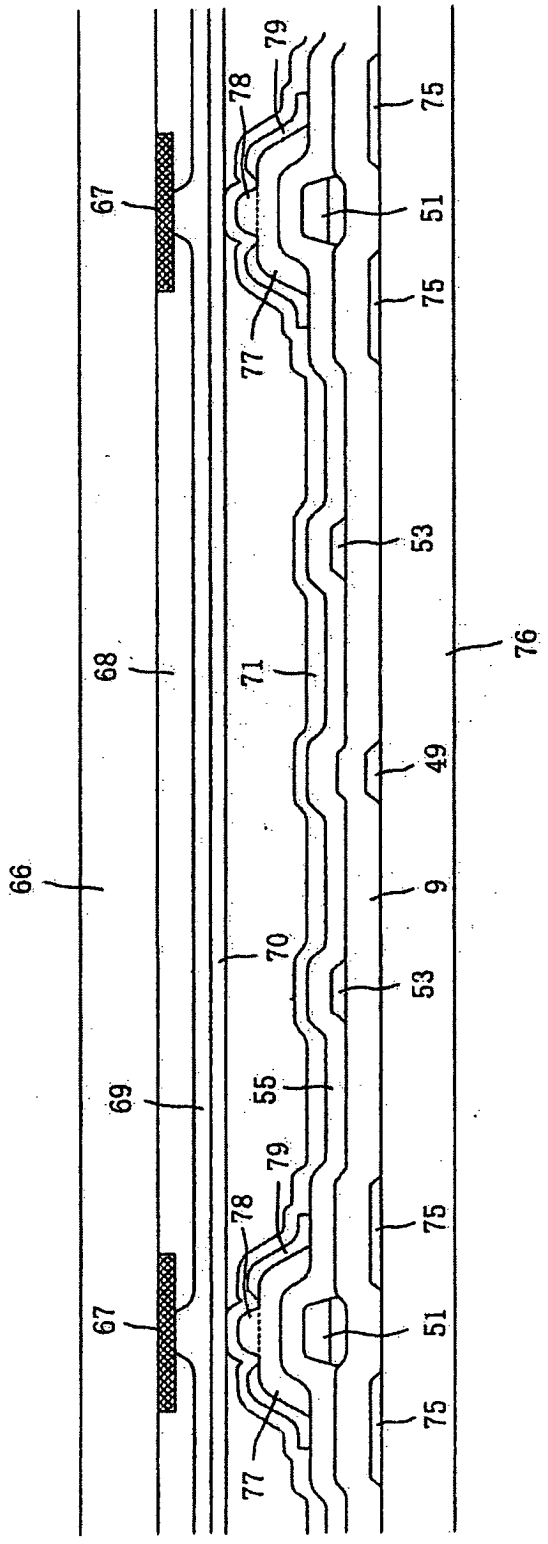


FIG. 55

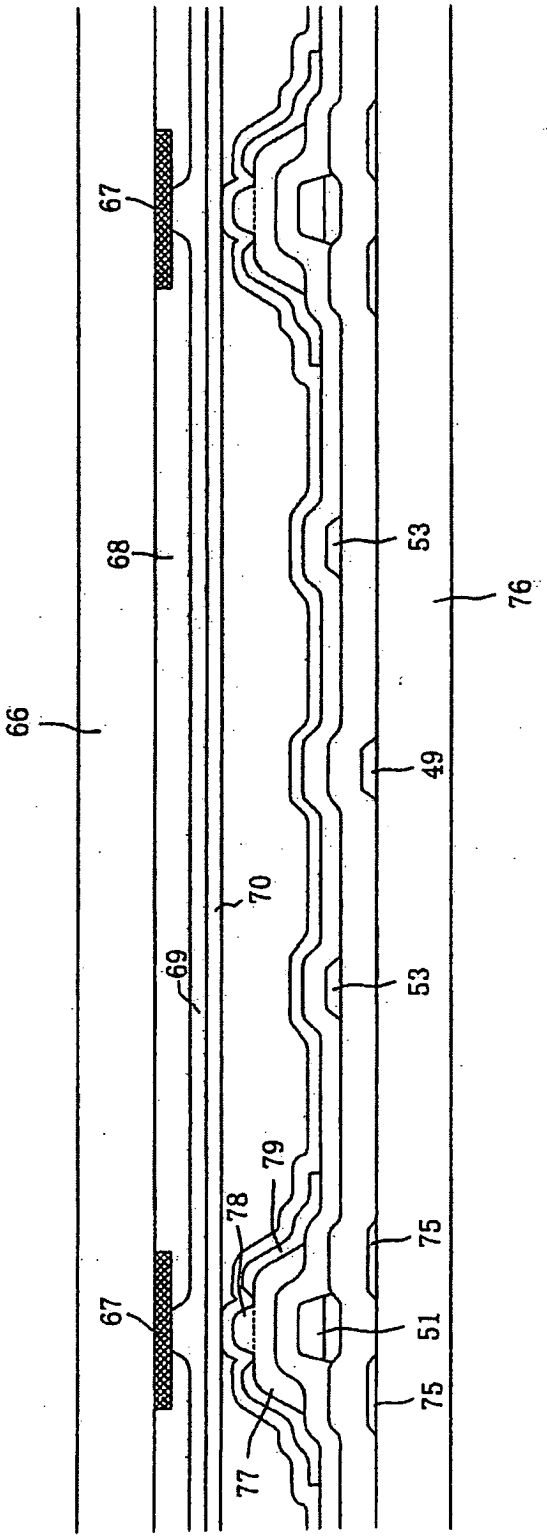


FIG. 56

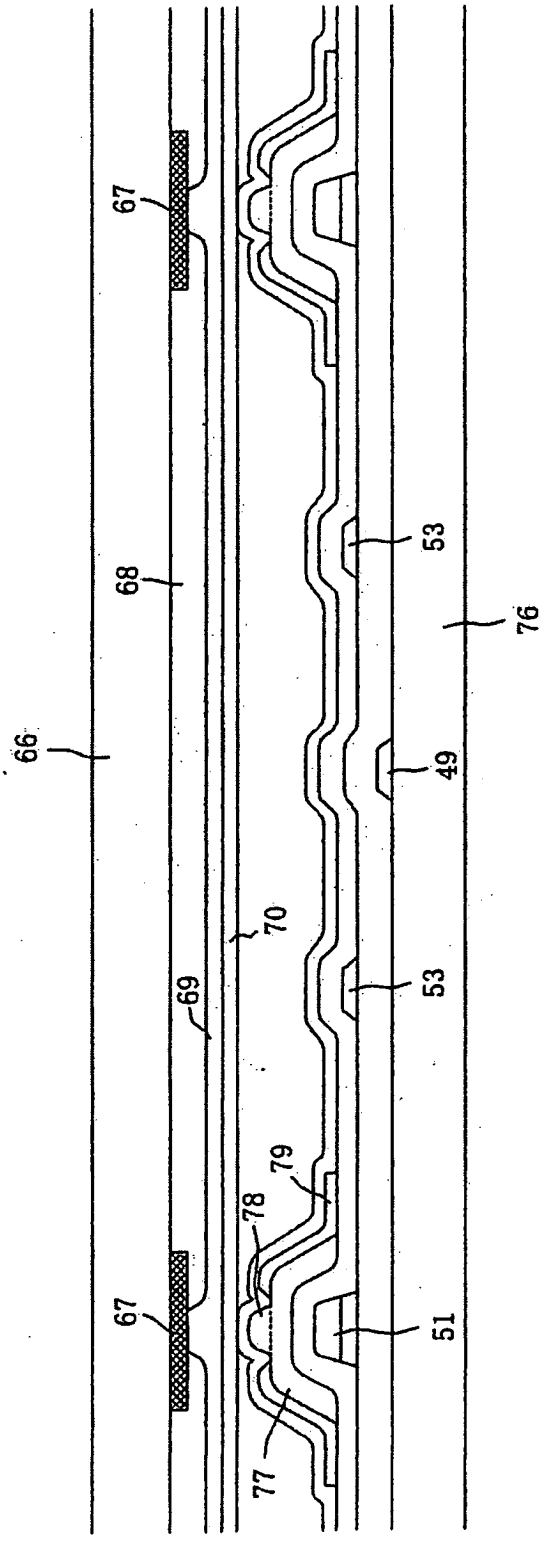


FIG. 57

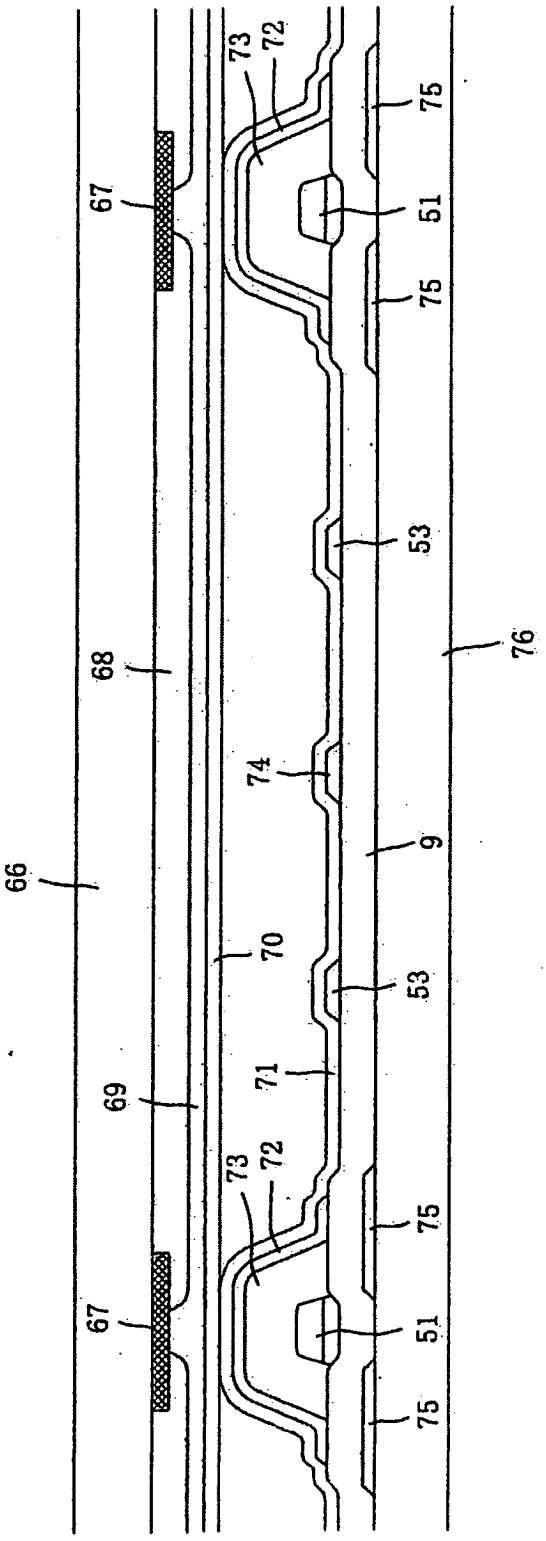


FIG. 58

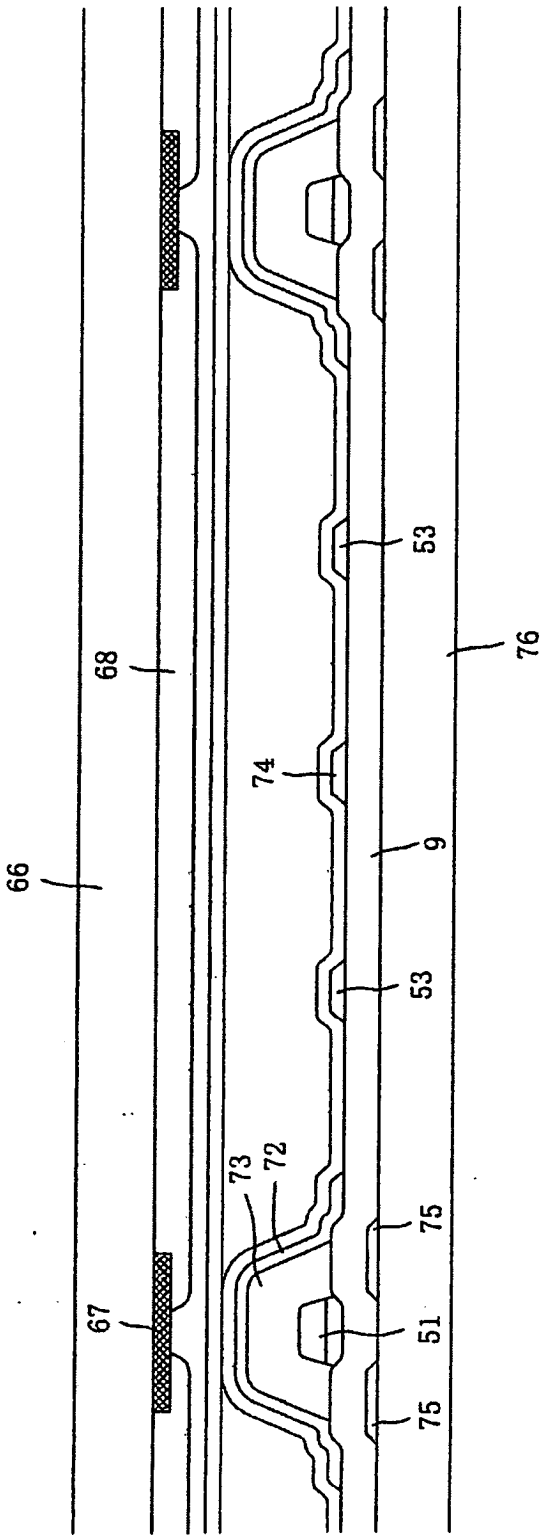


FIG. 59

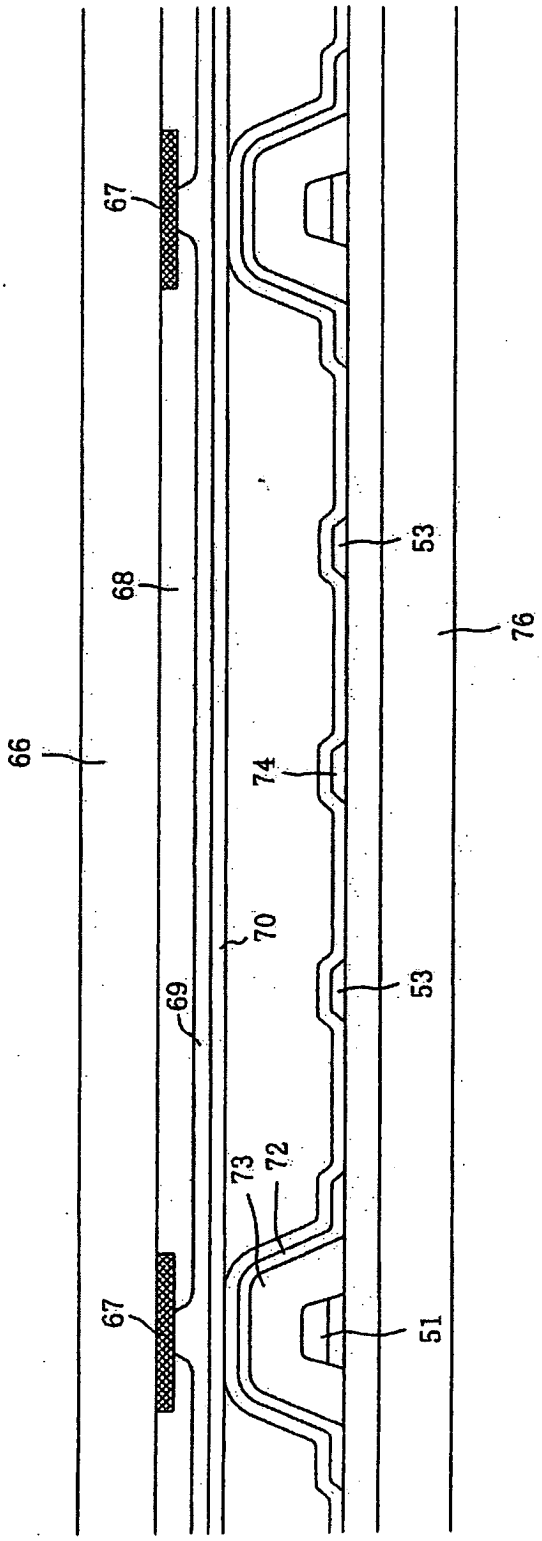


FIG. 60

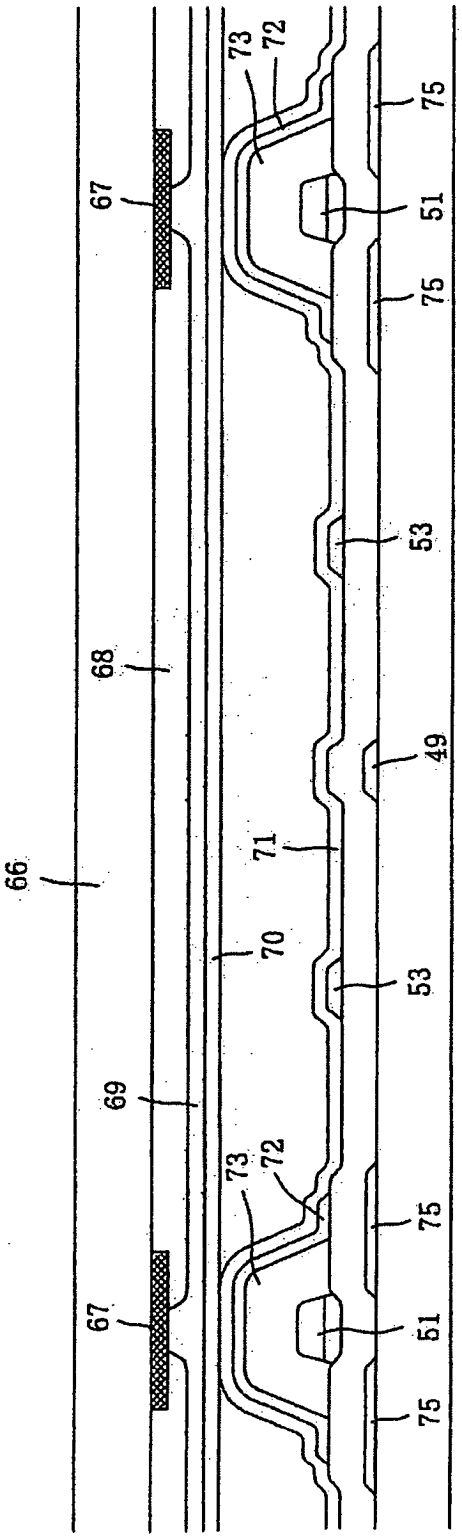


FIG. 61

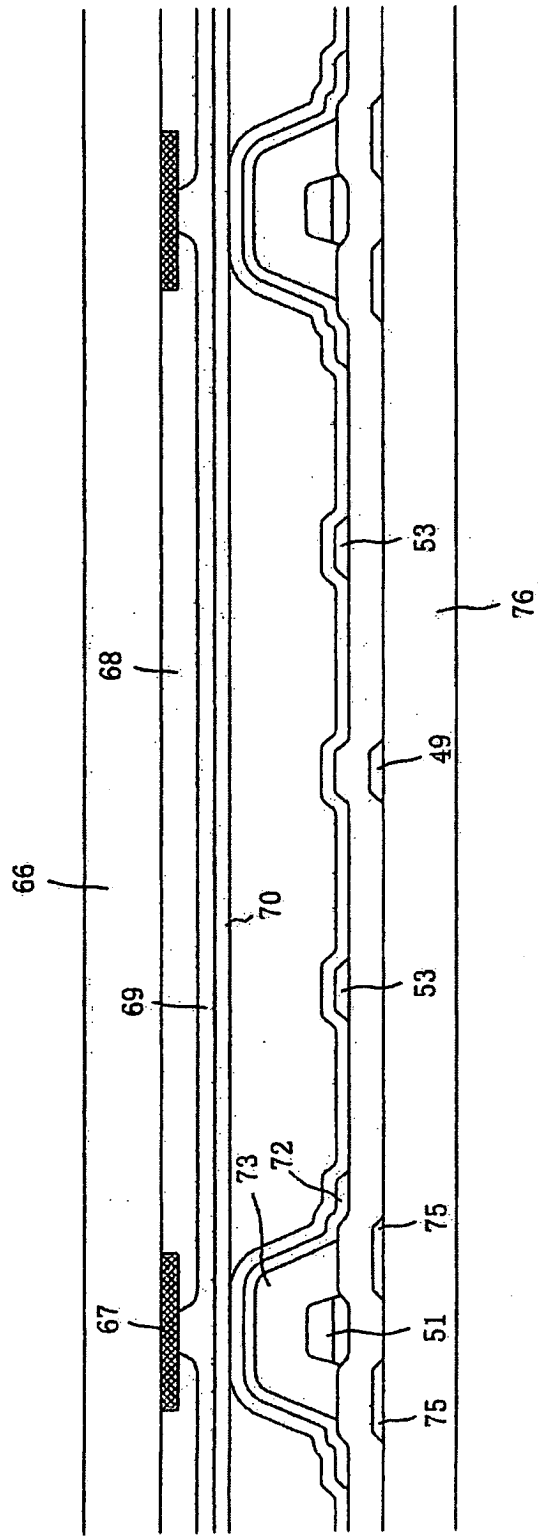


FIG. 62

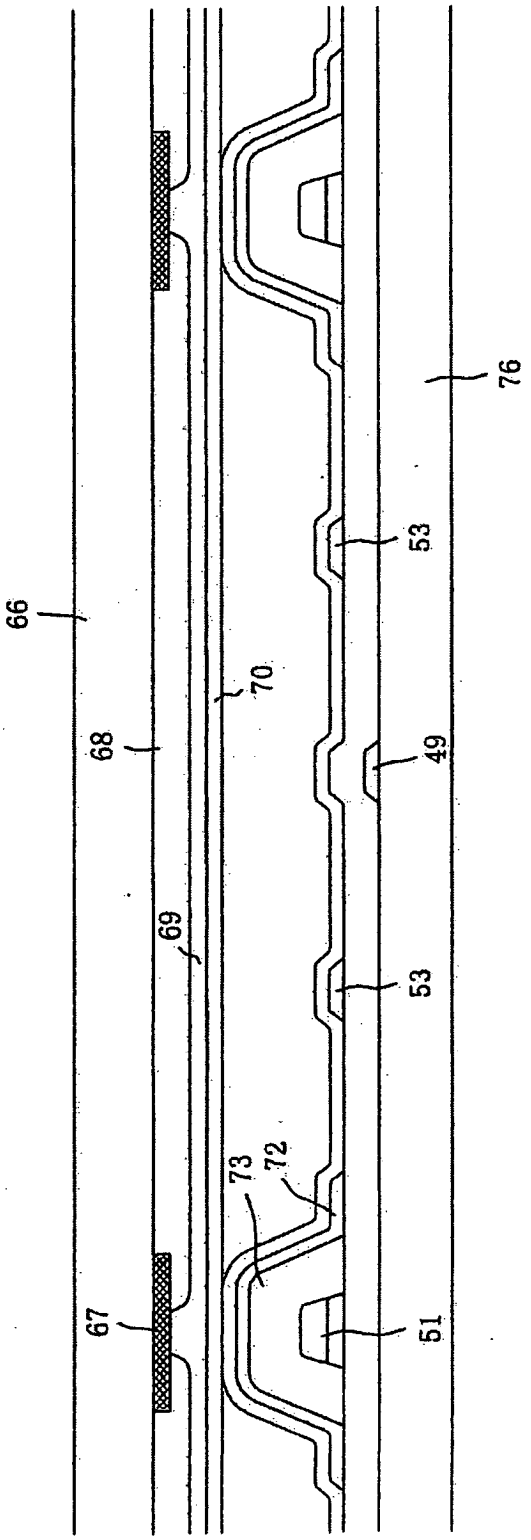


FIG. 63

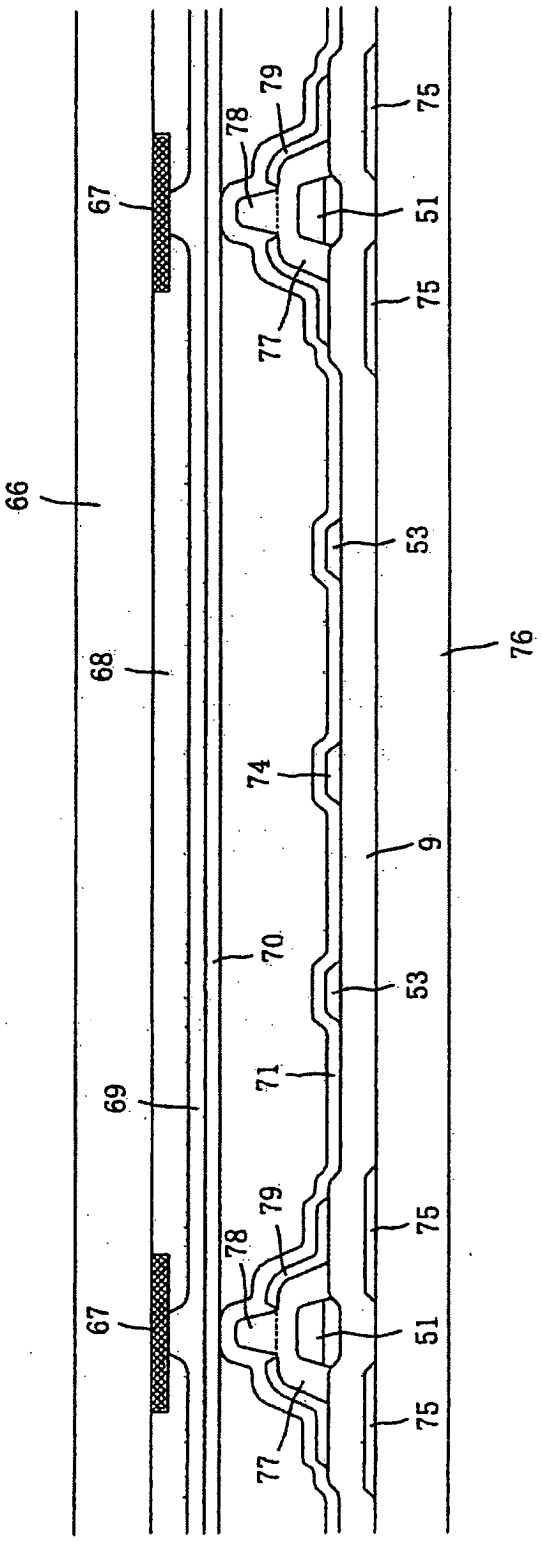
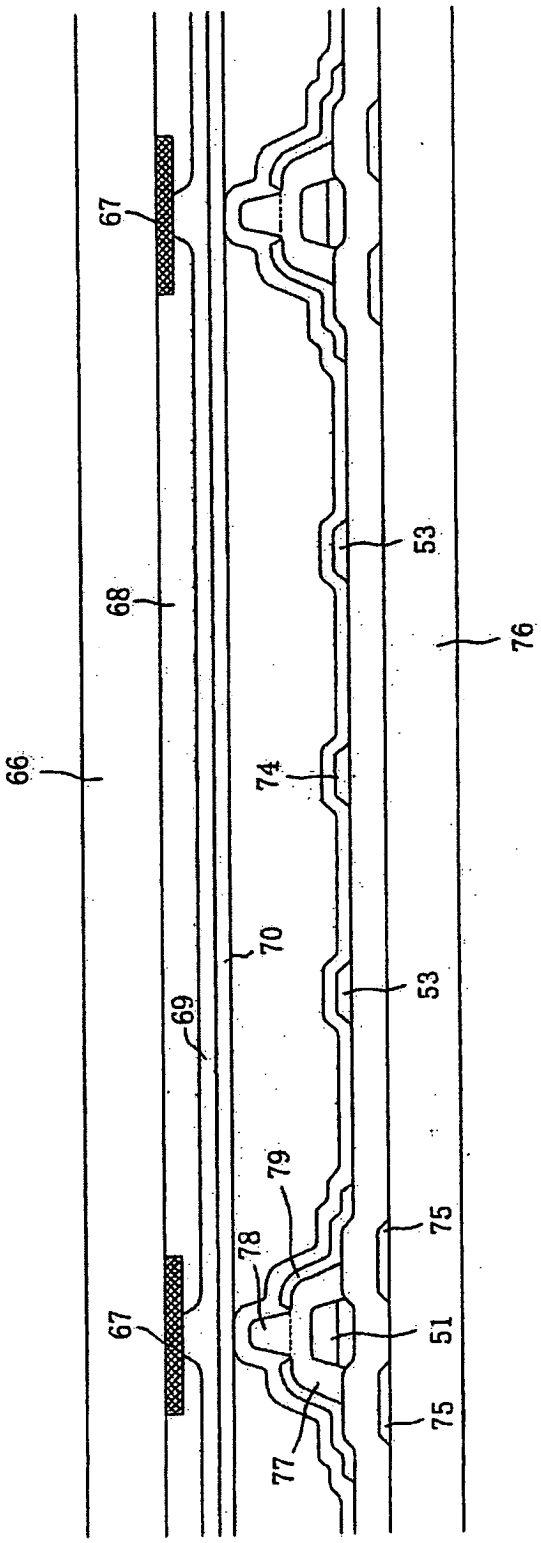


FIG. 64



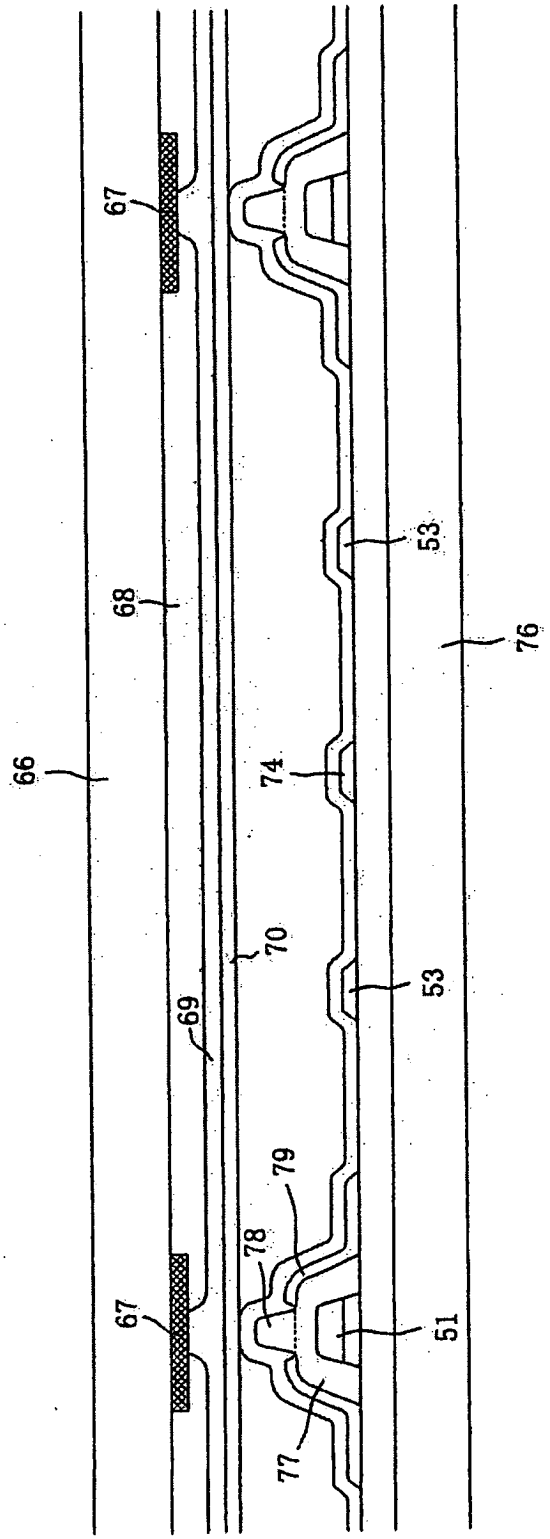


FIG. 65

FIG. 66

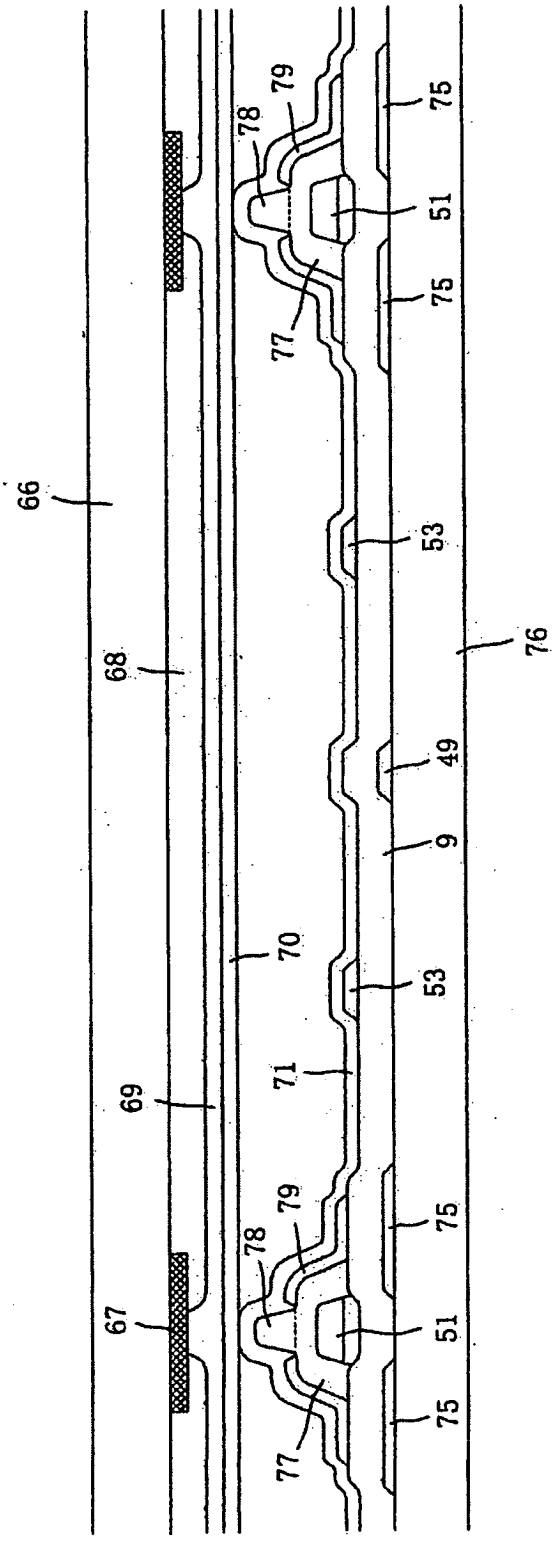


FIG. 67

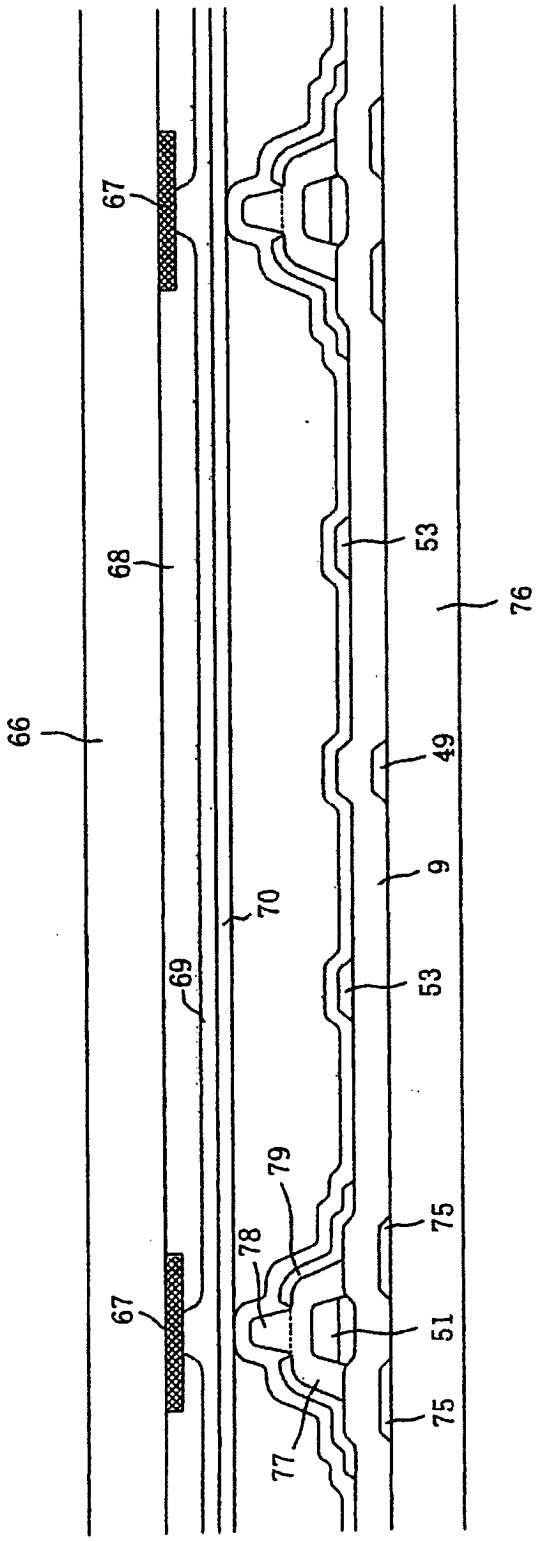


FIG. 68

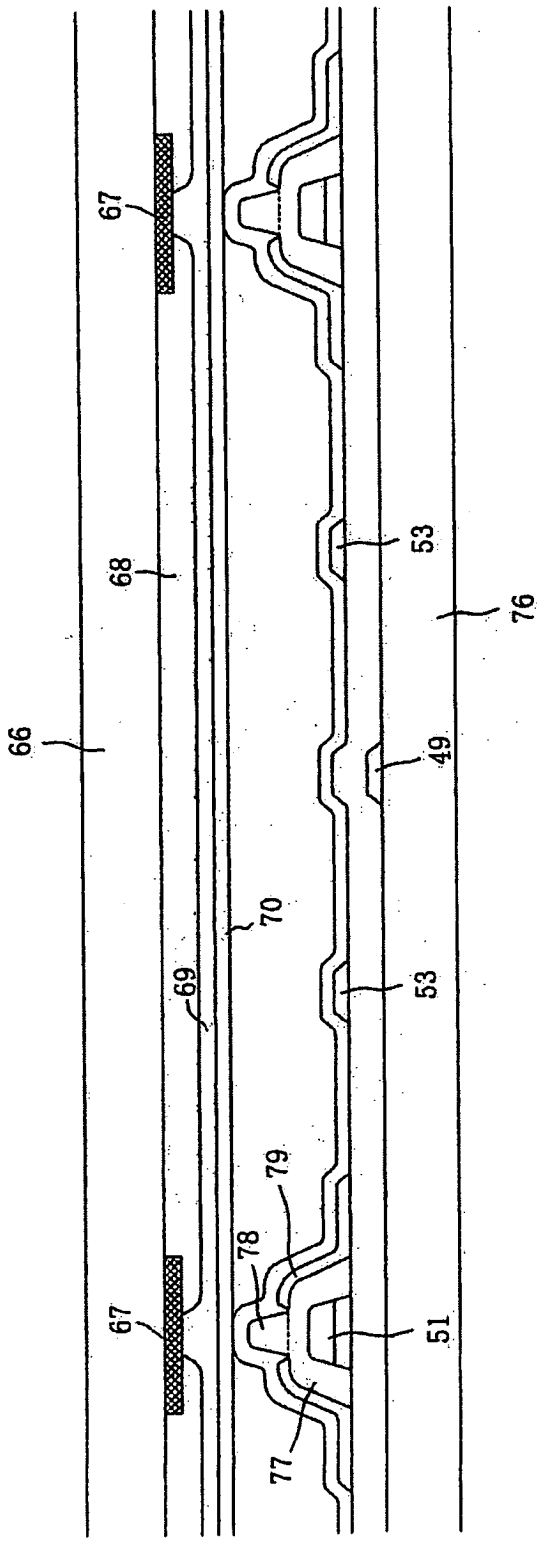


FIG. 69

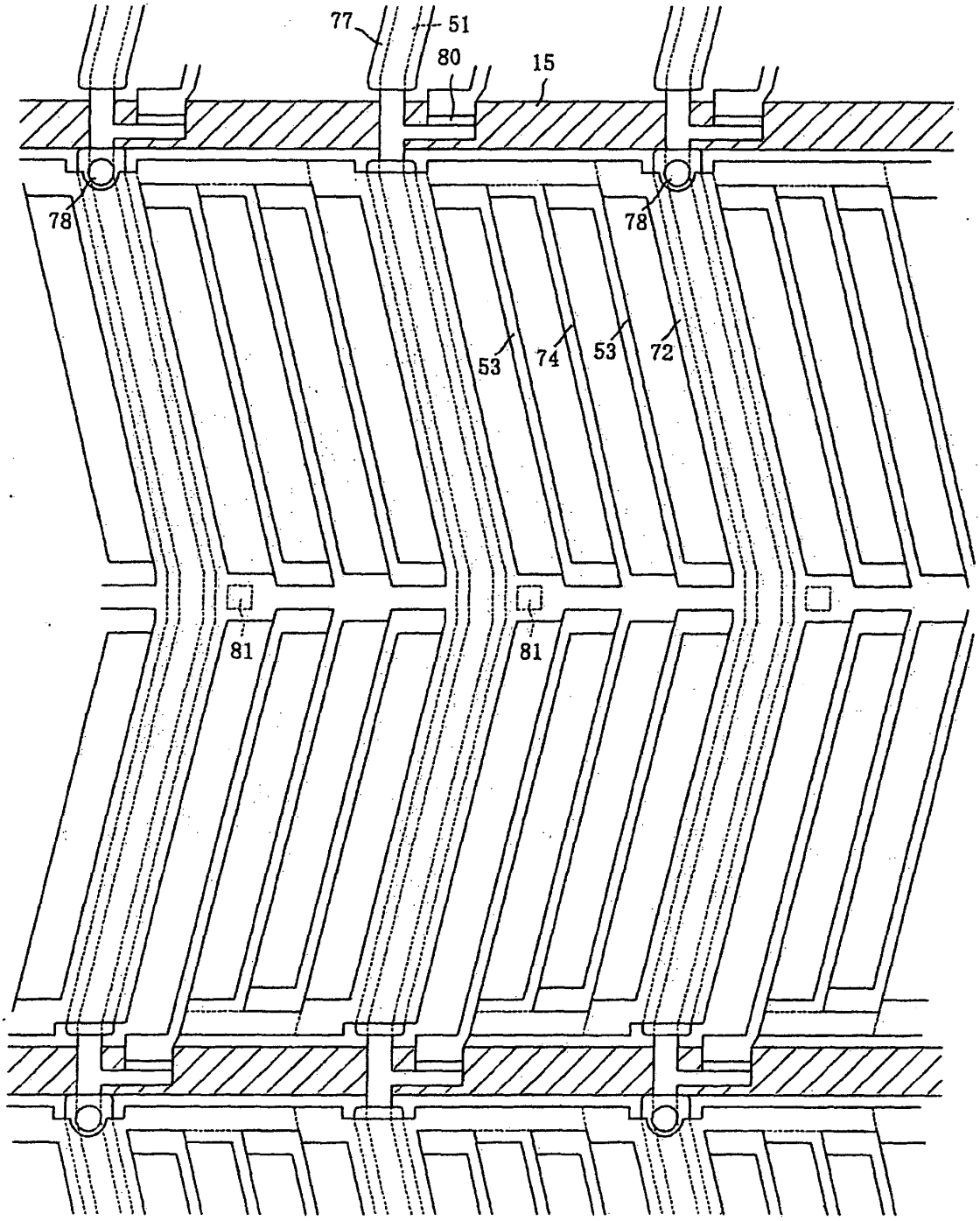


FIG. 70

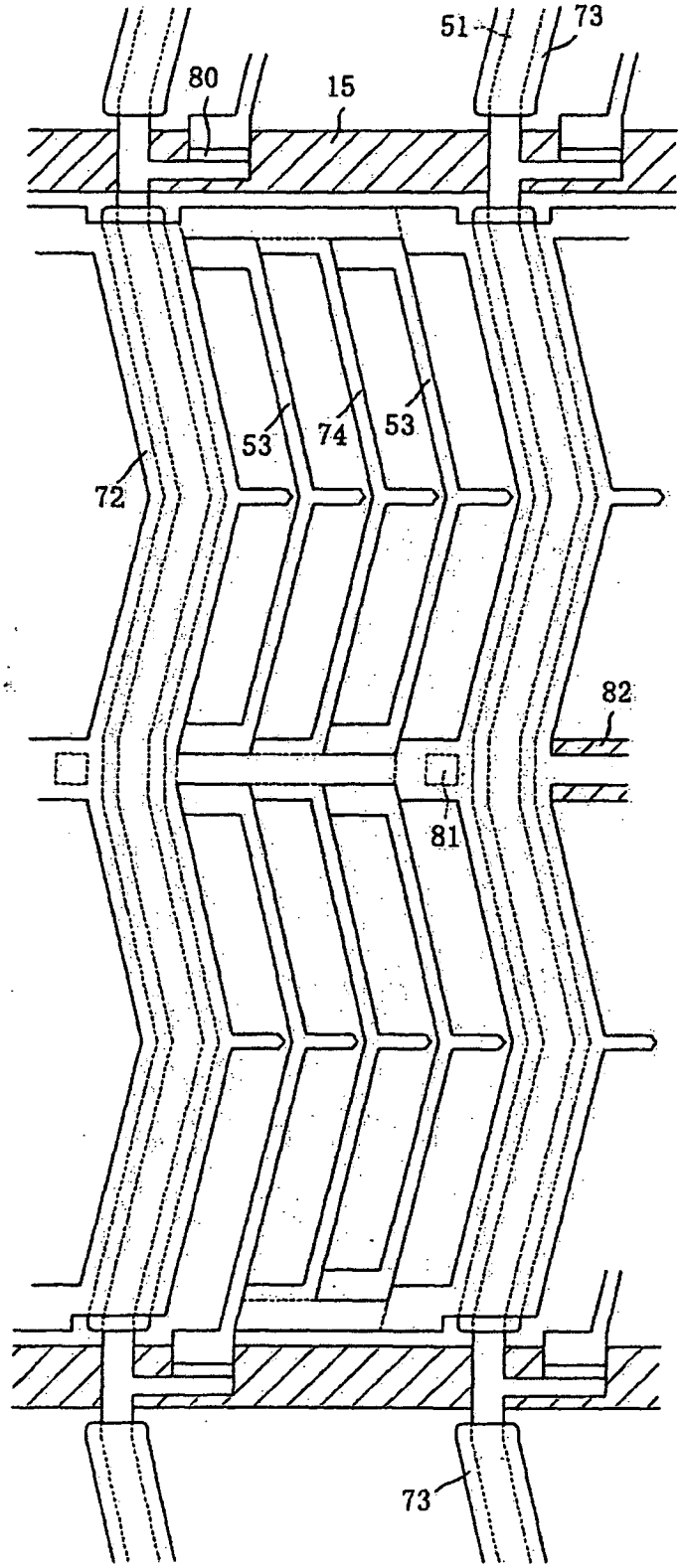


FIG. 71

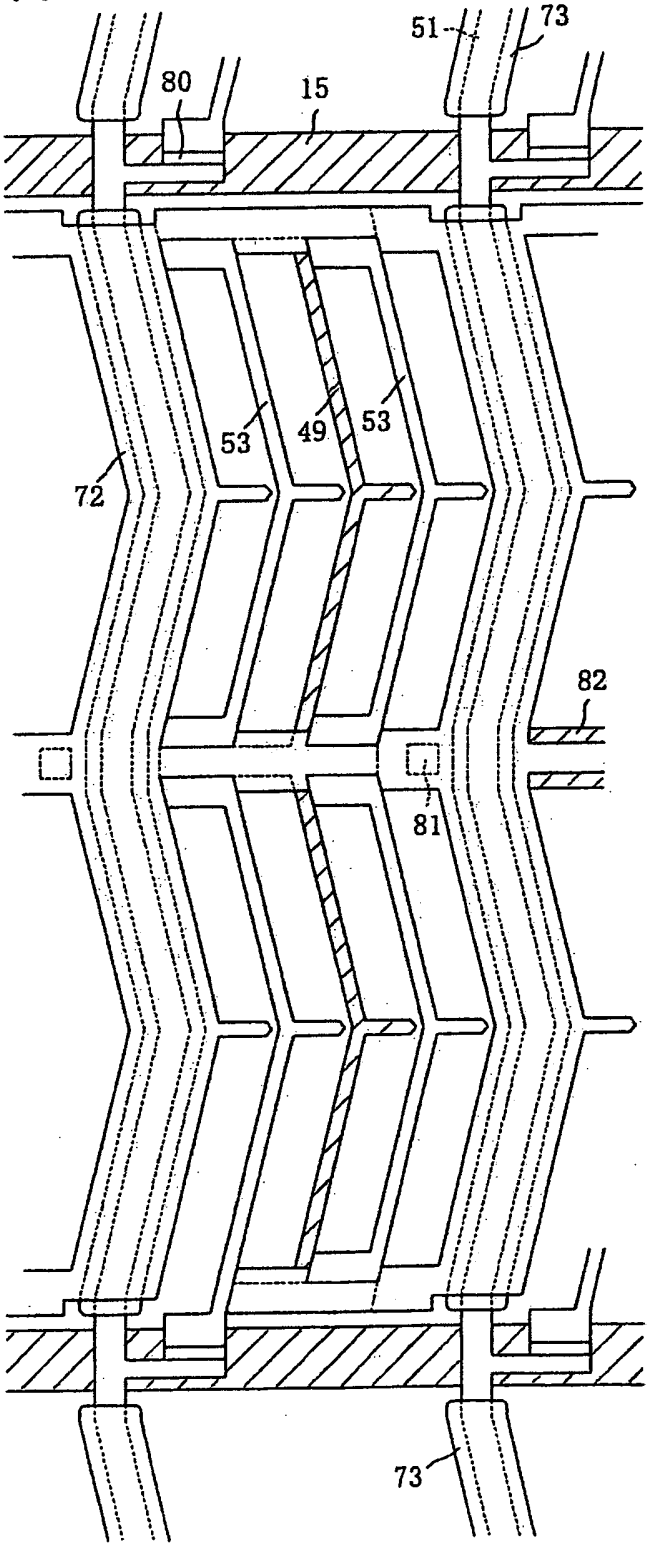


FIG. 72

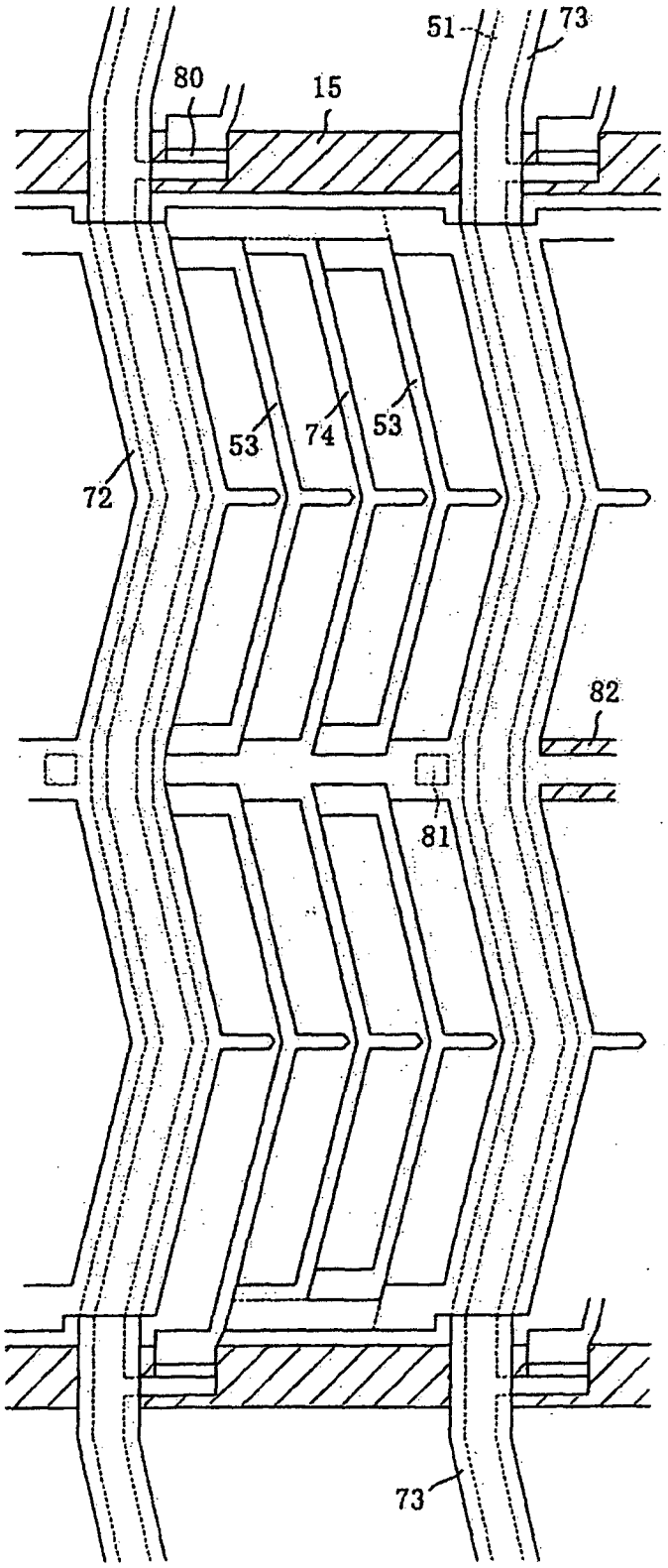


FIG. 73

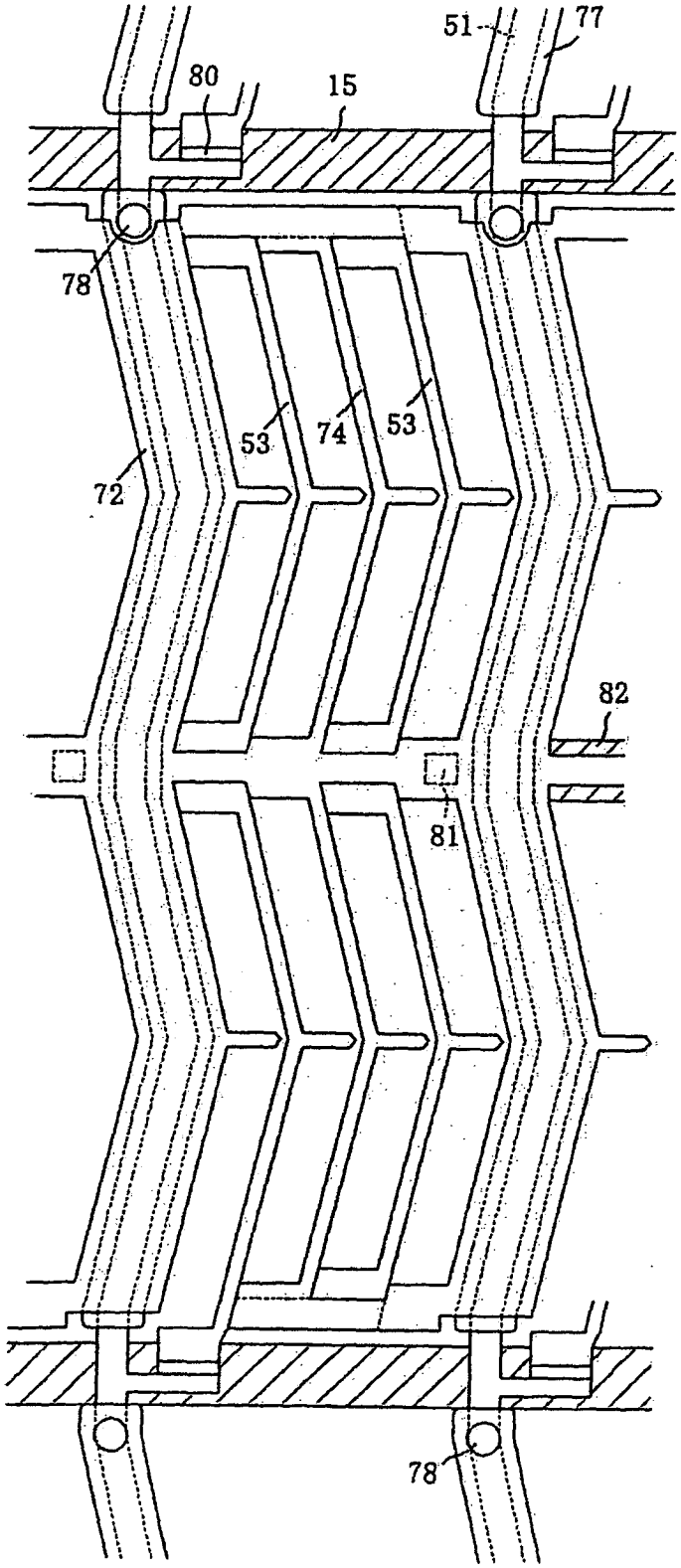


FIG. 74

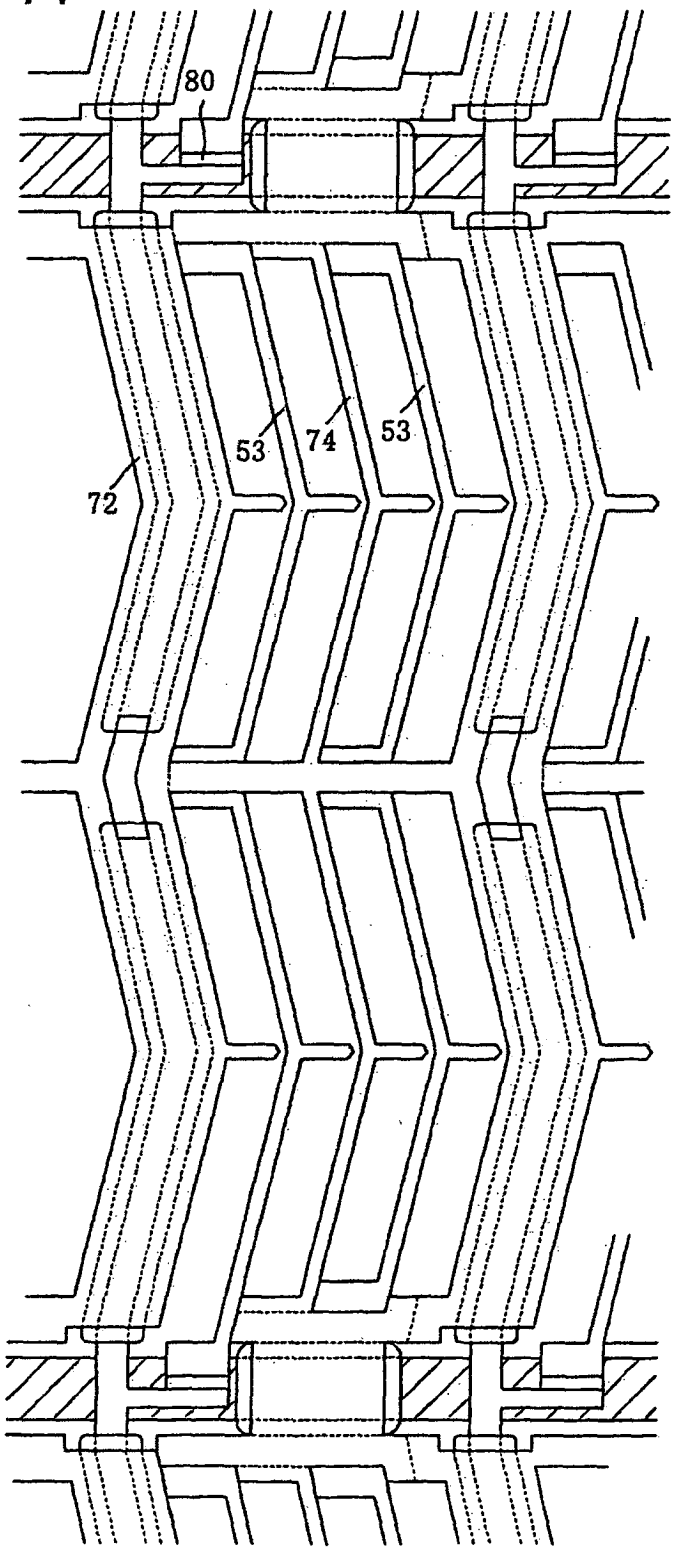


FIG. 75

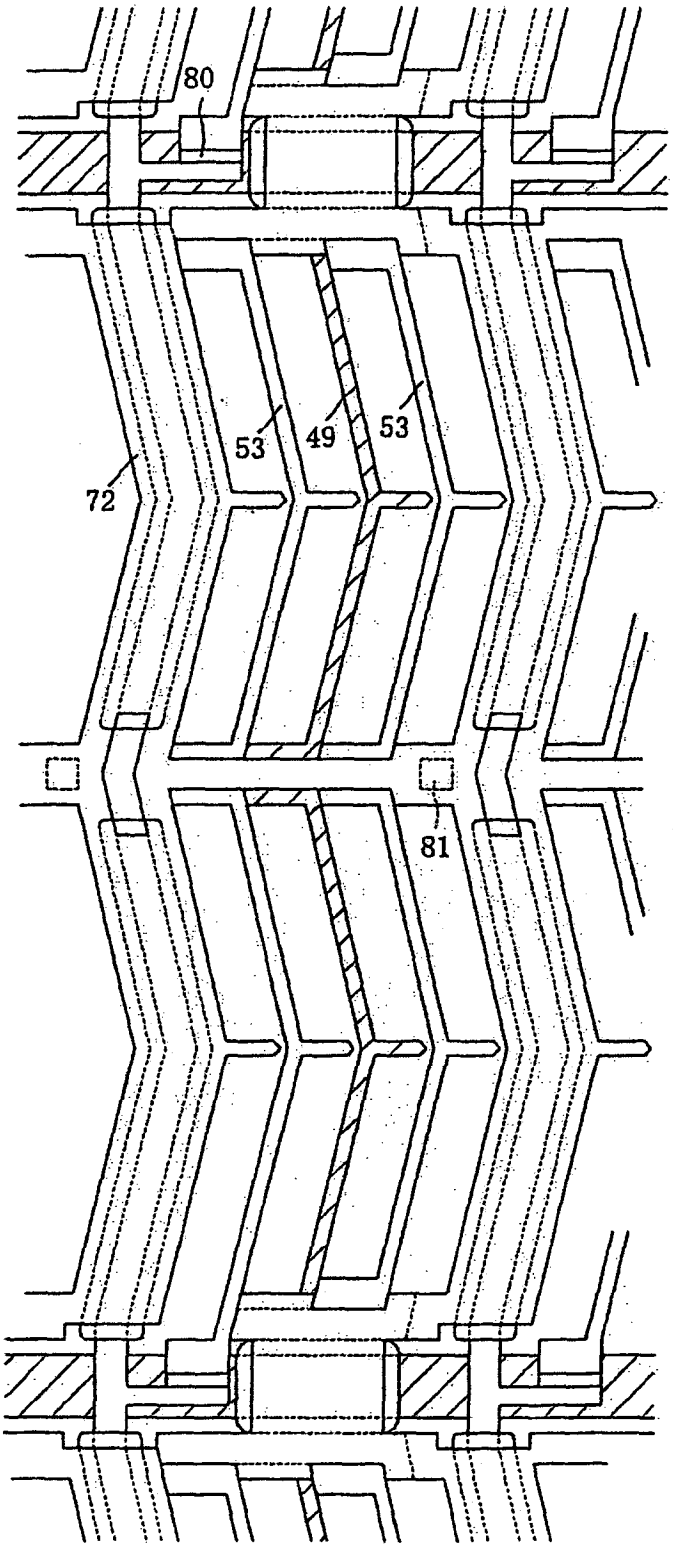


FIG. 76

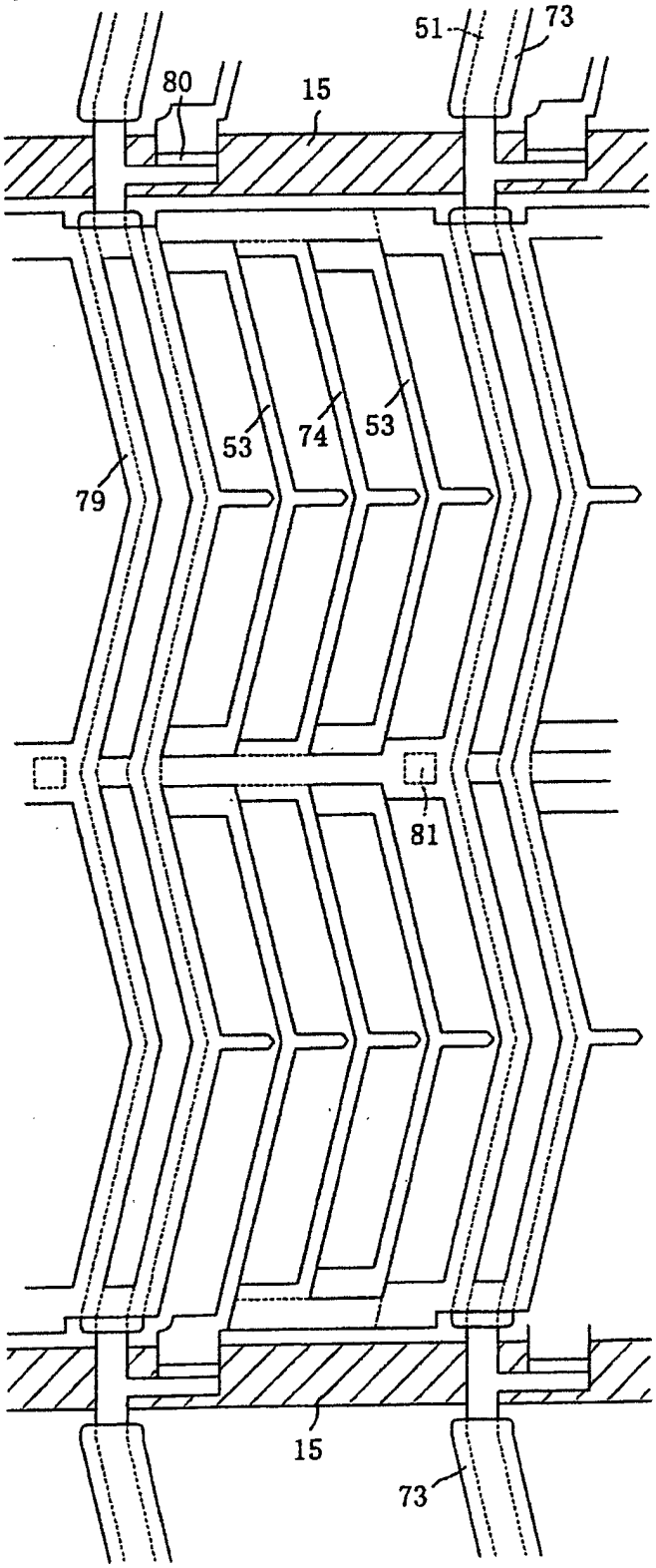


FIG. 77

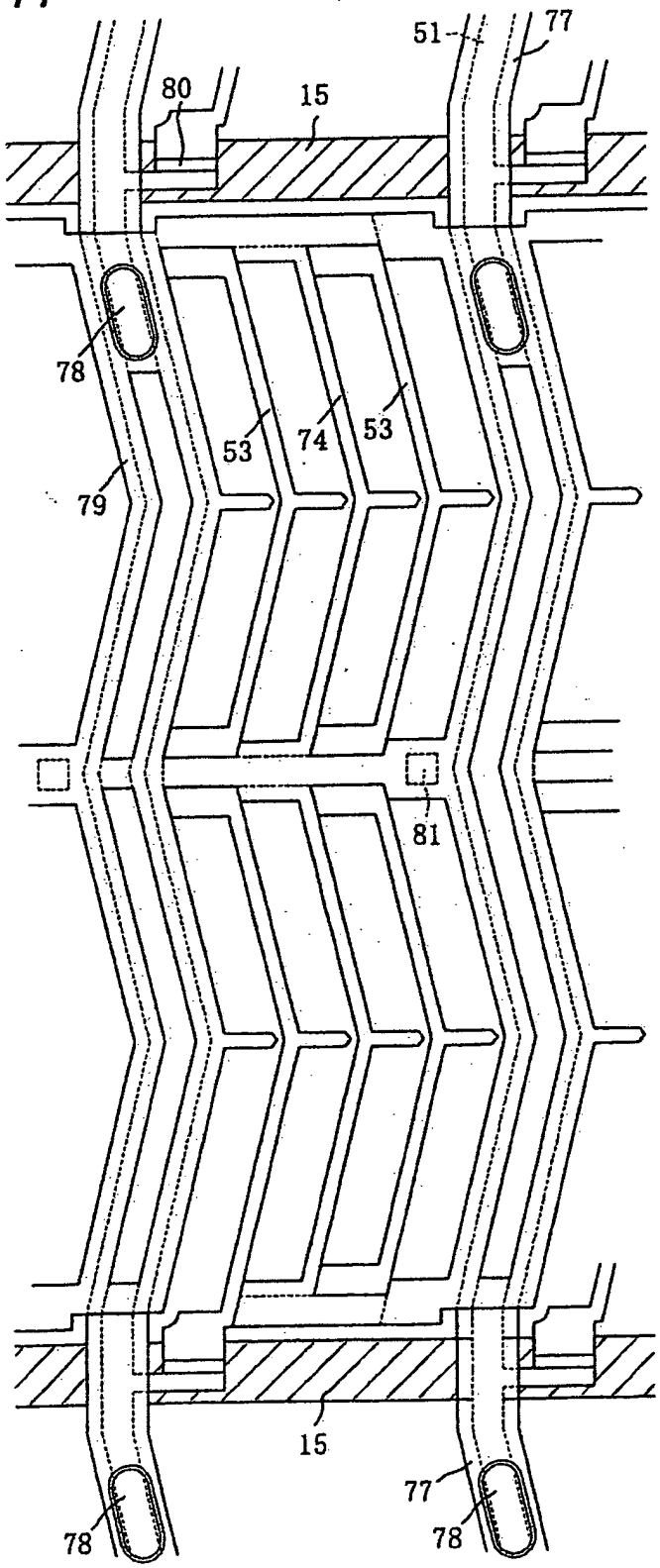


FIG. 78

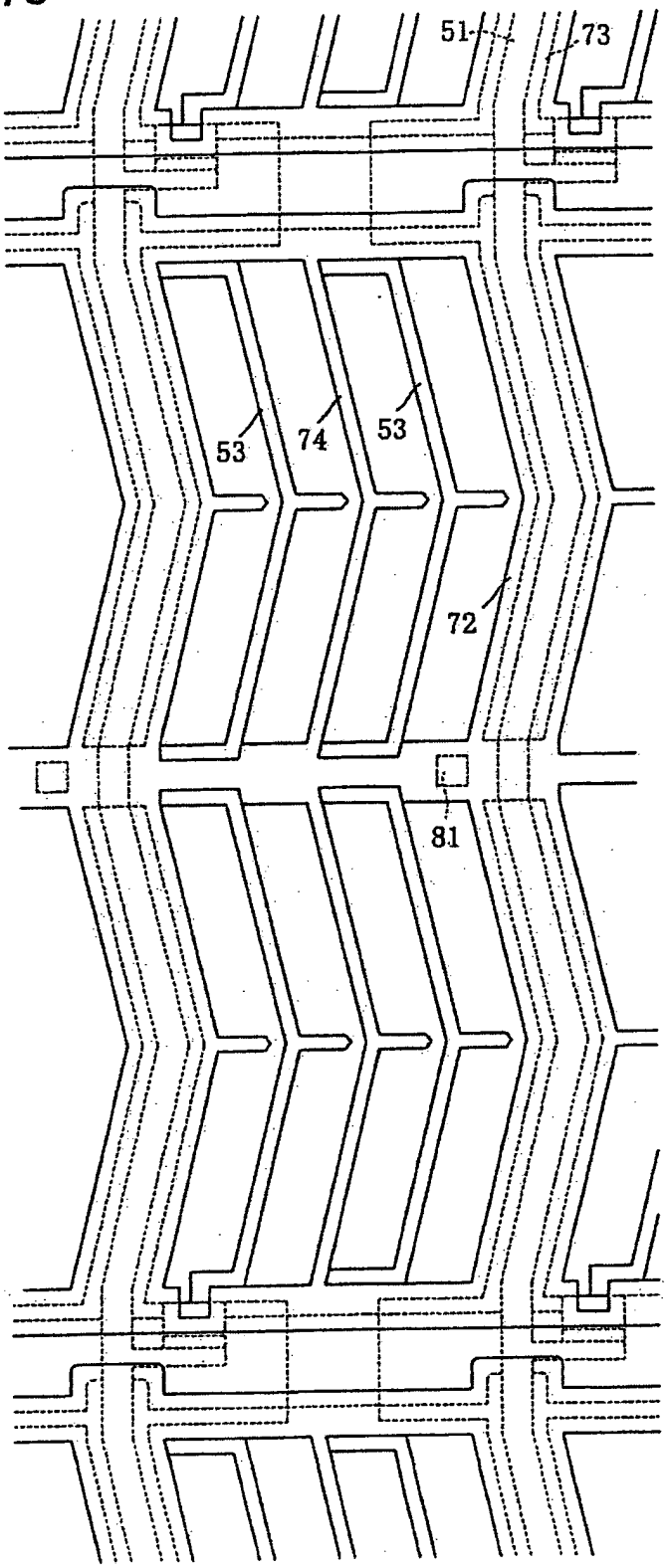


FIG. 79

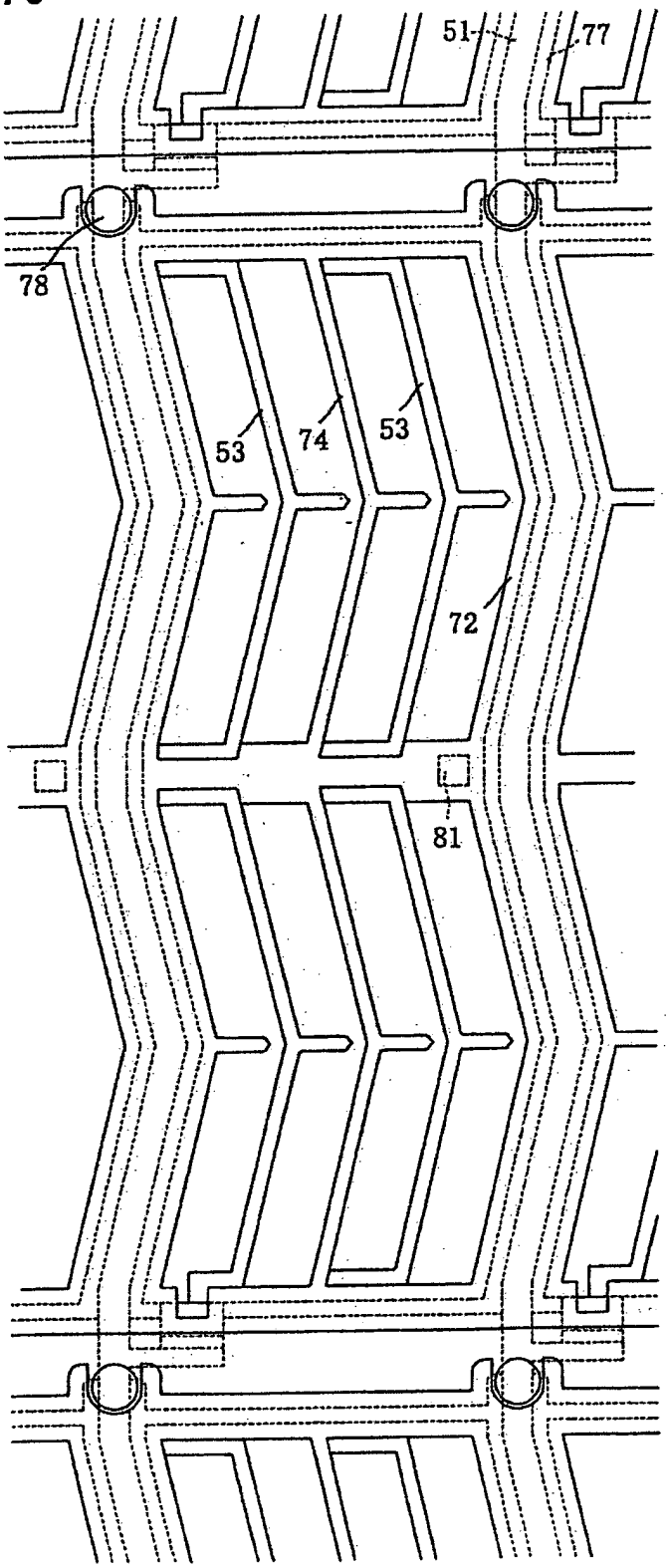


FIG. 80

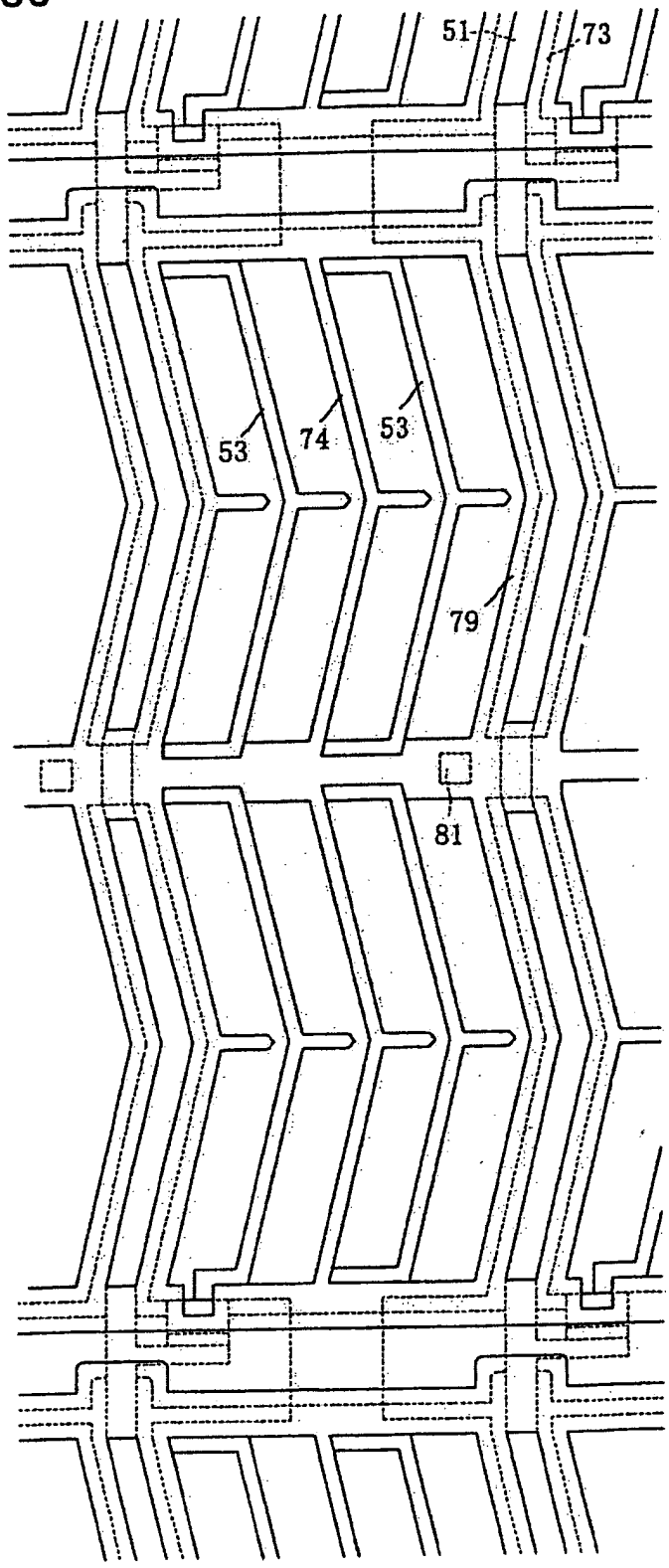


FIG. 81

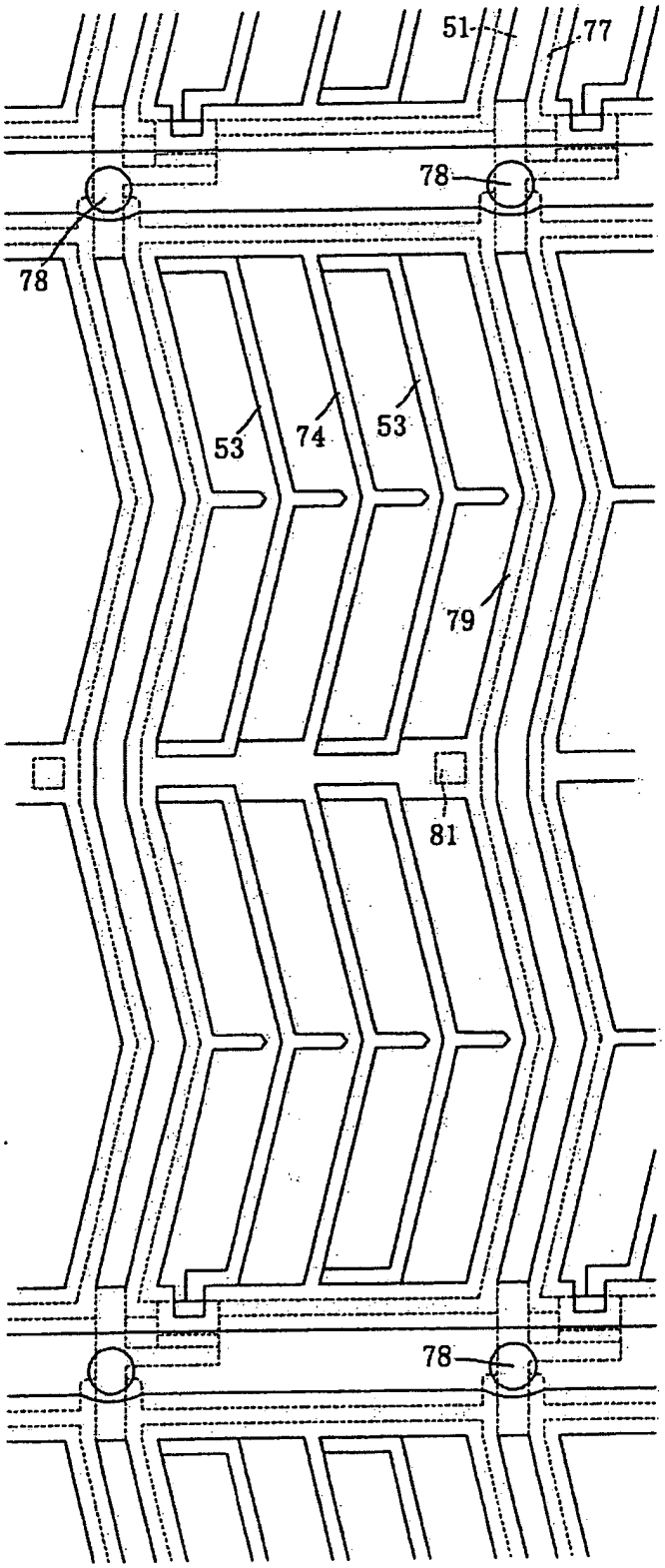


FIG. 82

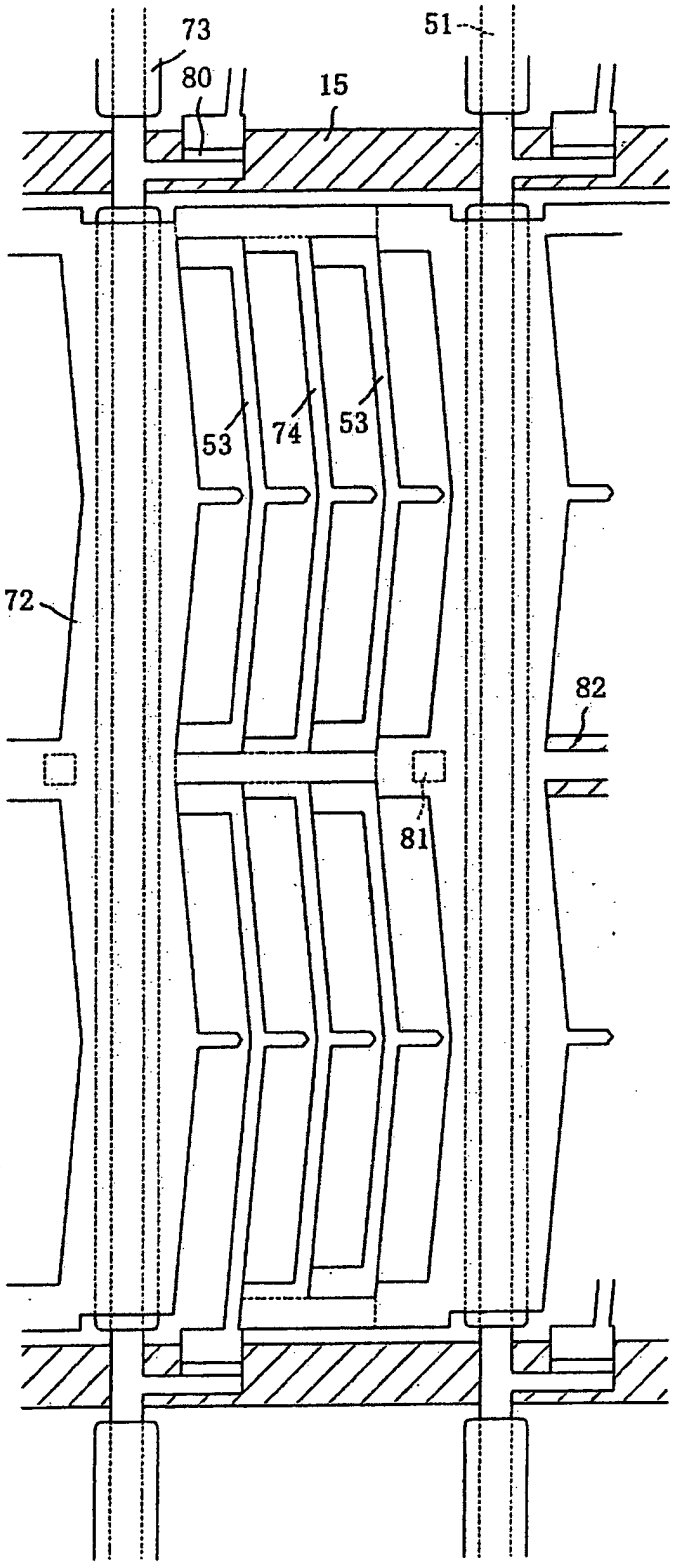


FIG. 83

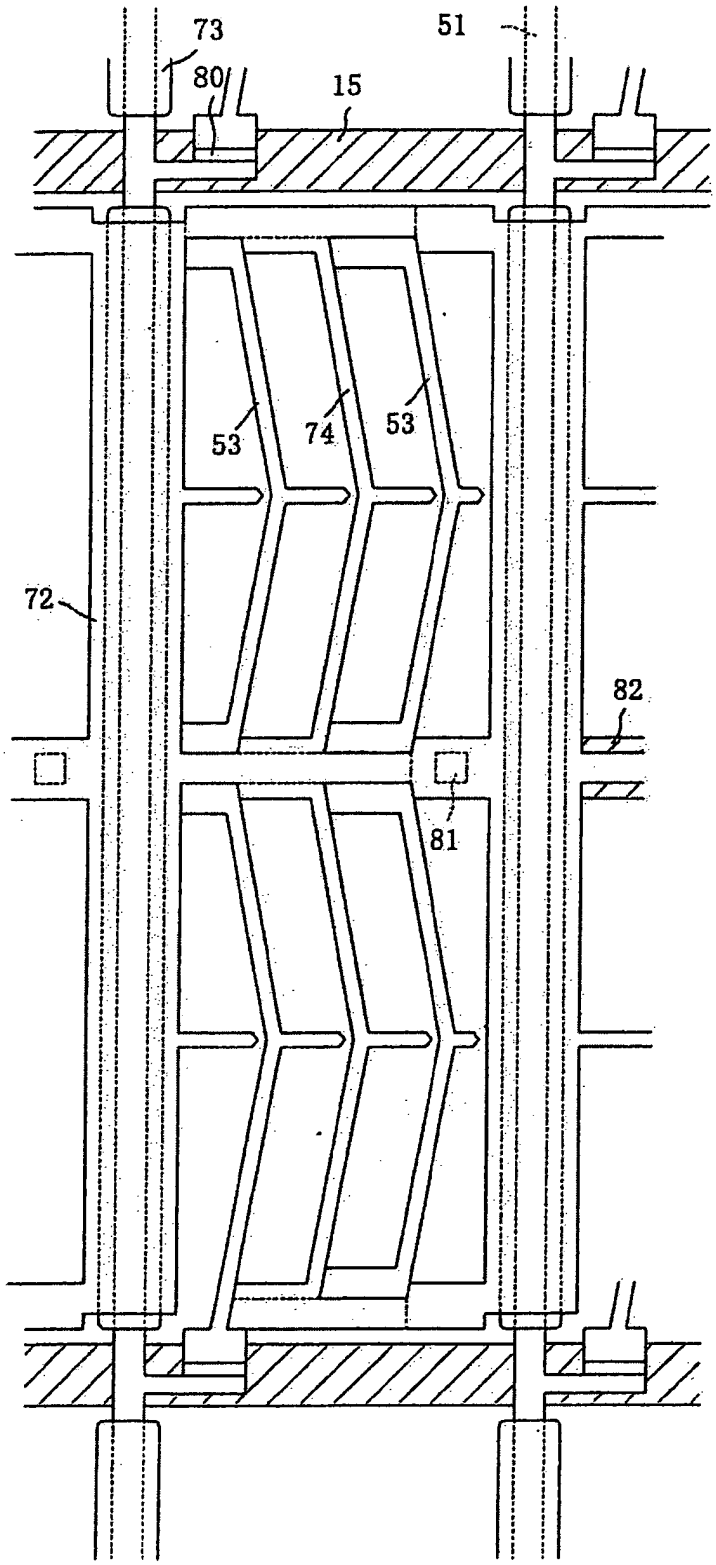


FIG. 84

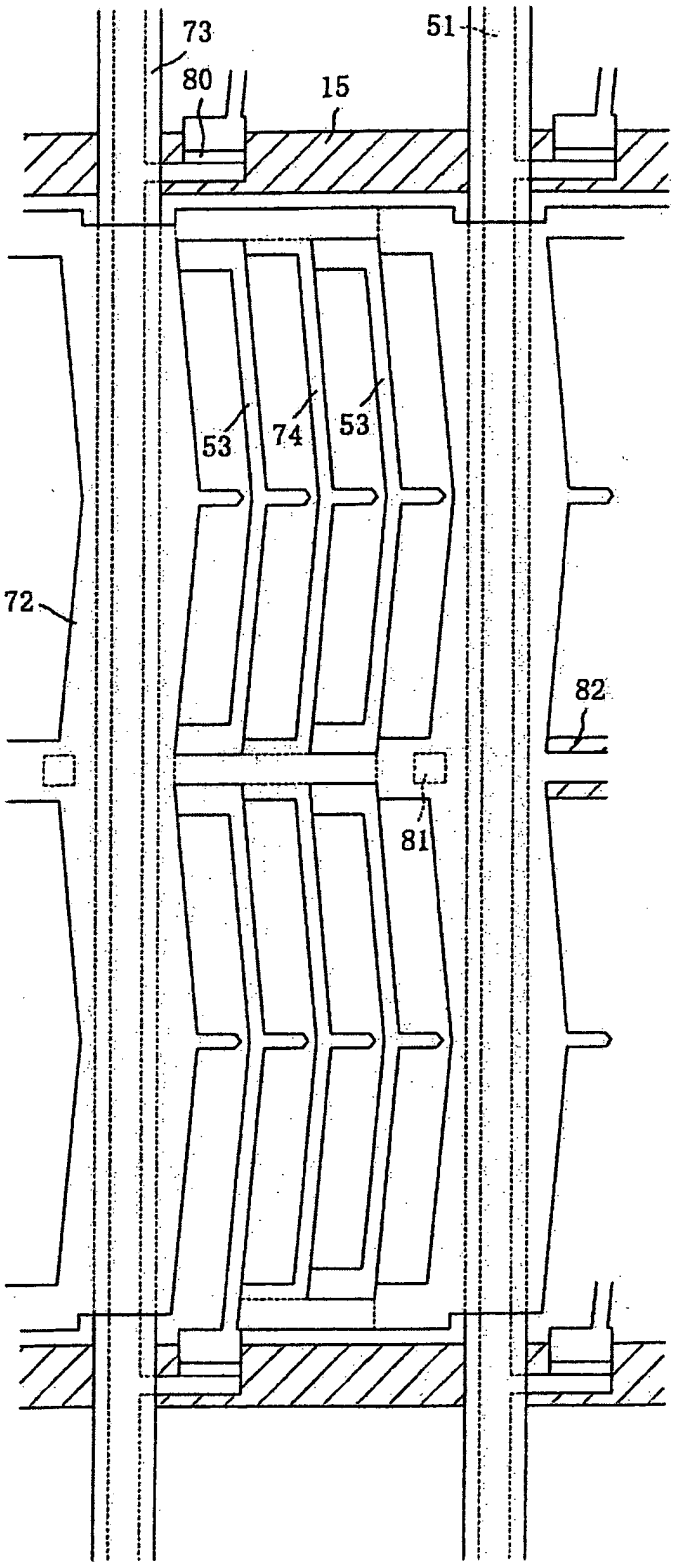


FIG. 85

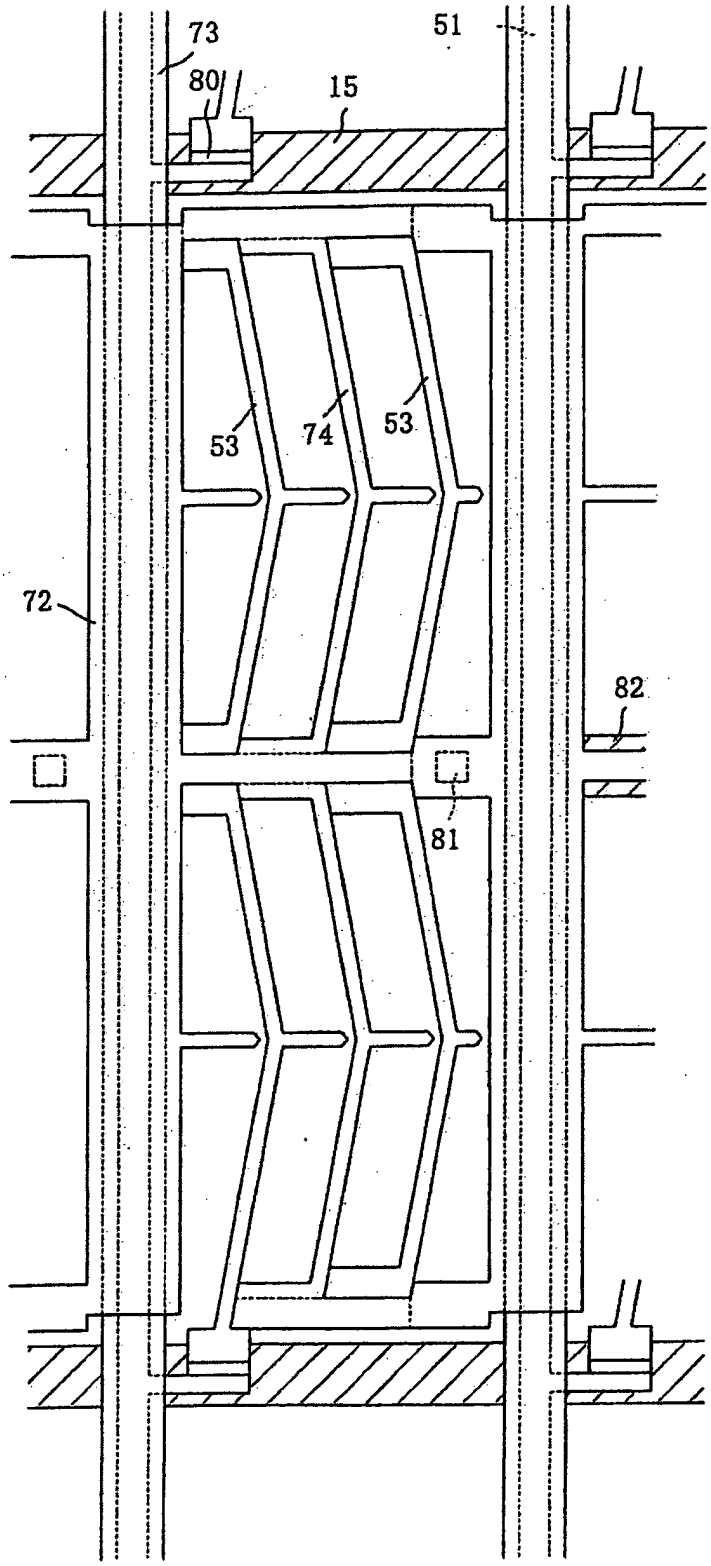


FIG. 86

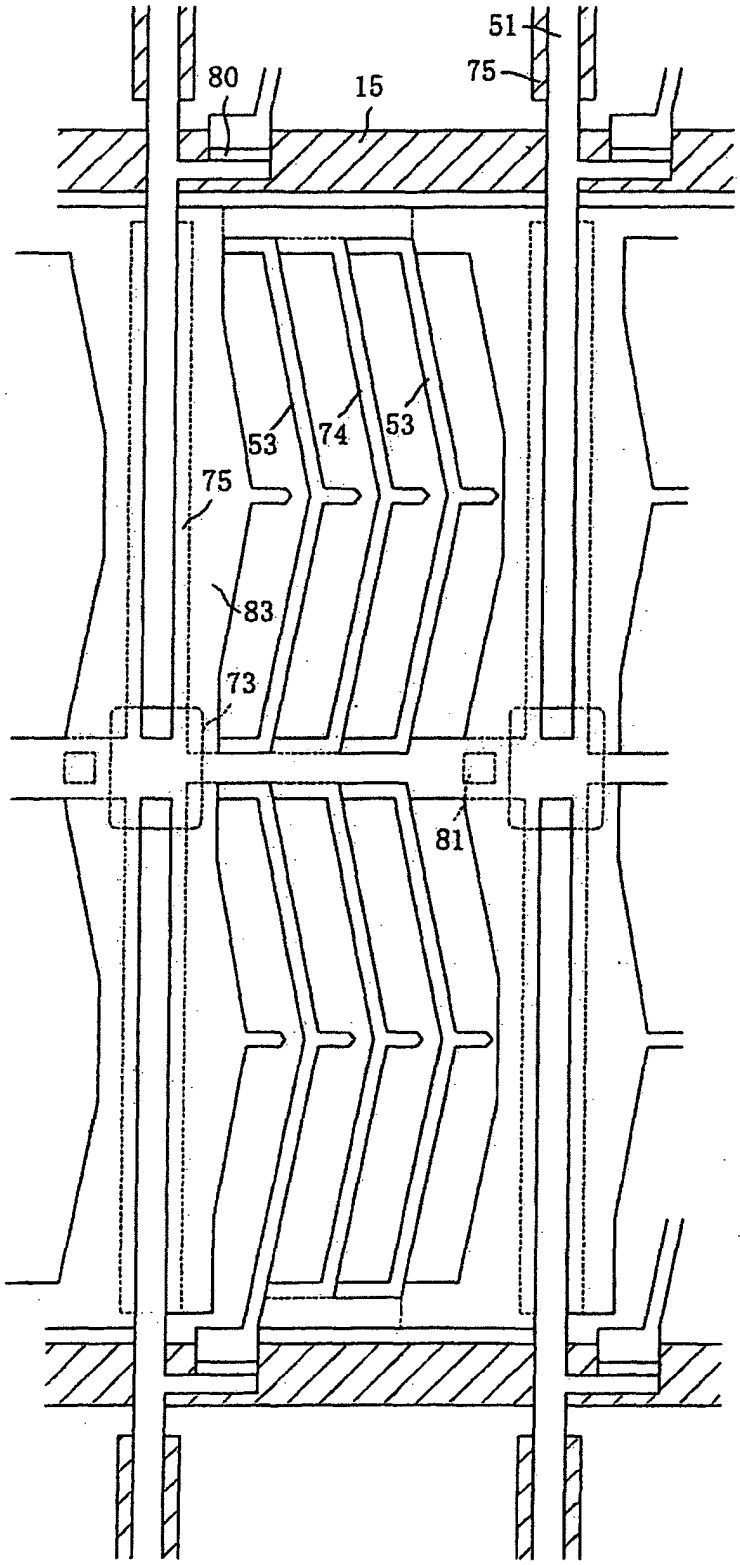


FIG. 87

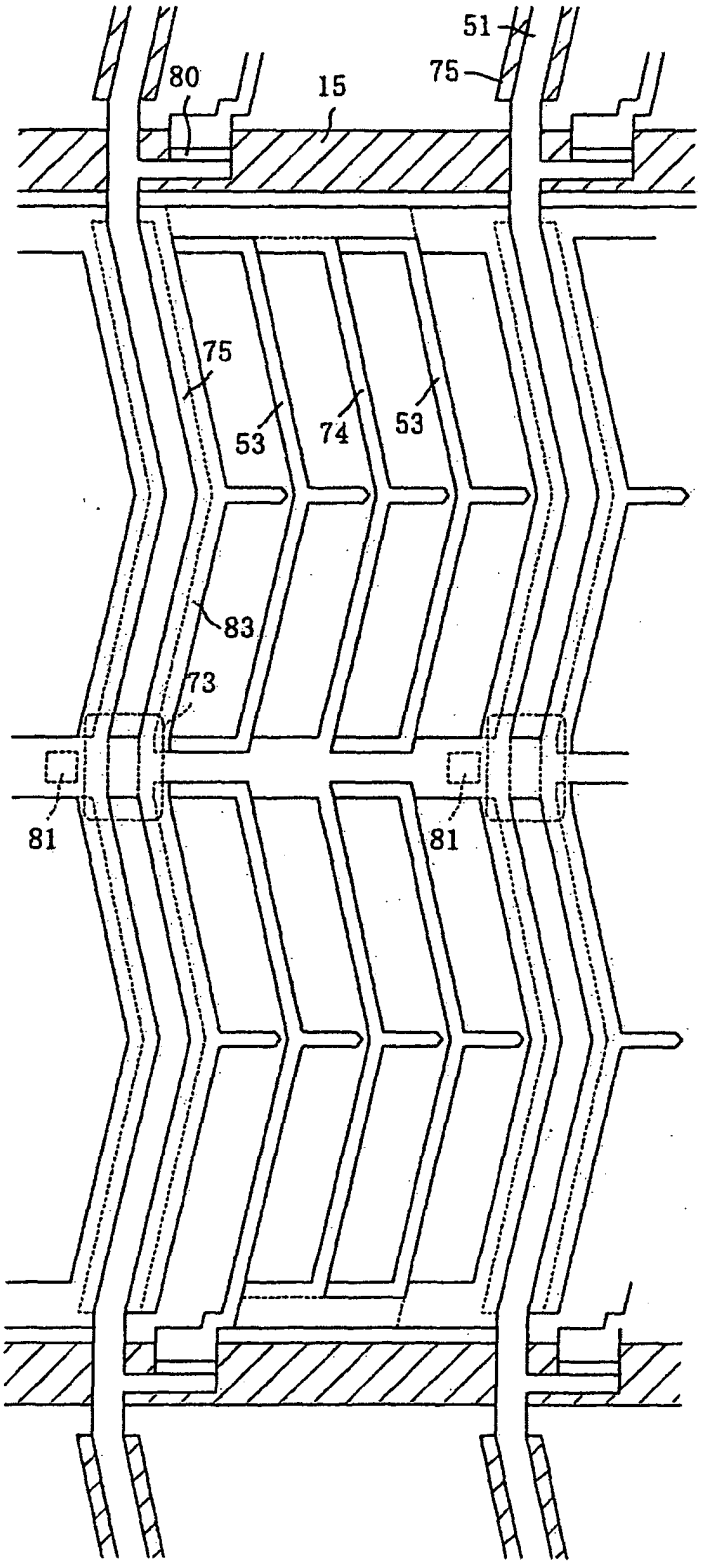


FIG. 88

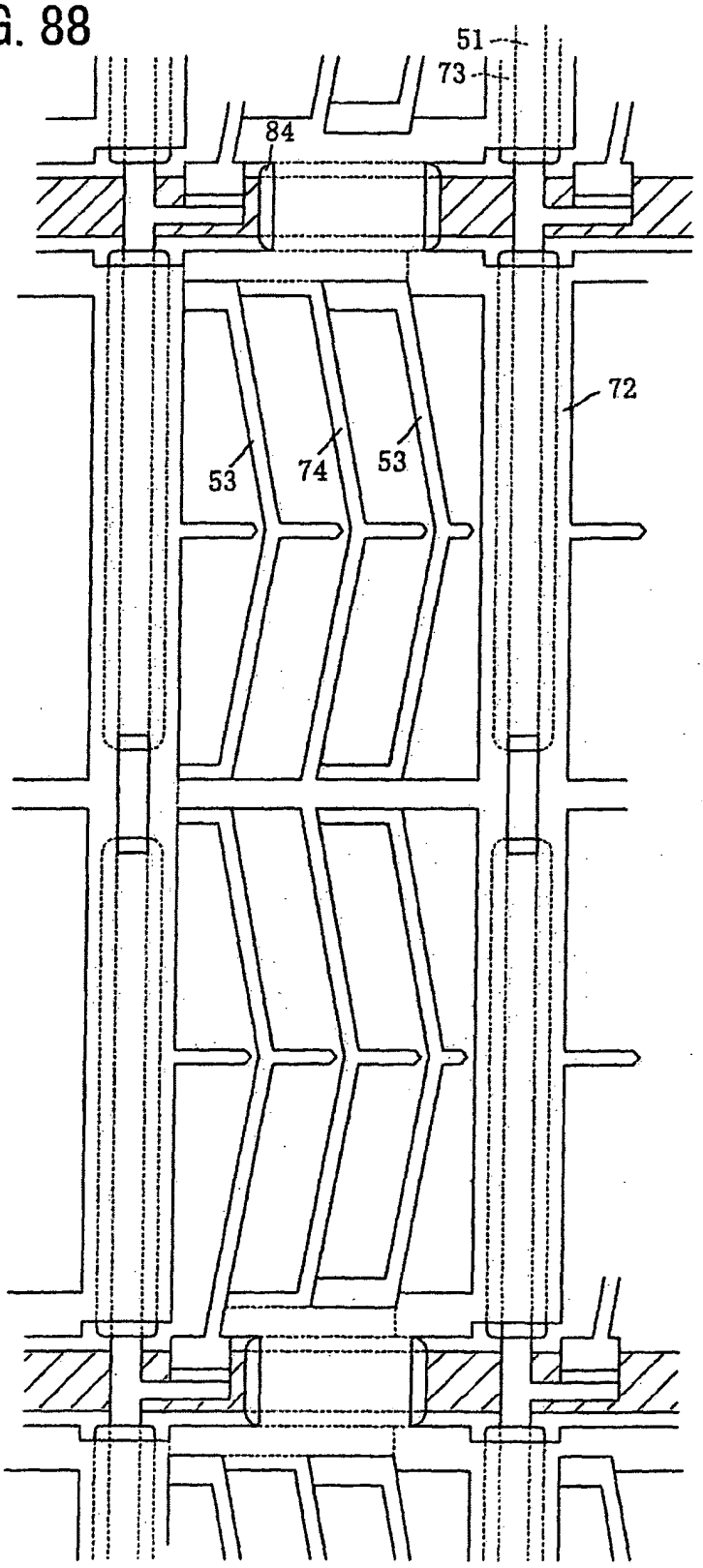


FIG. 89

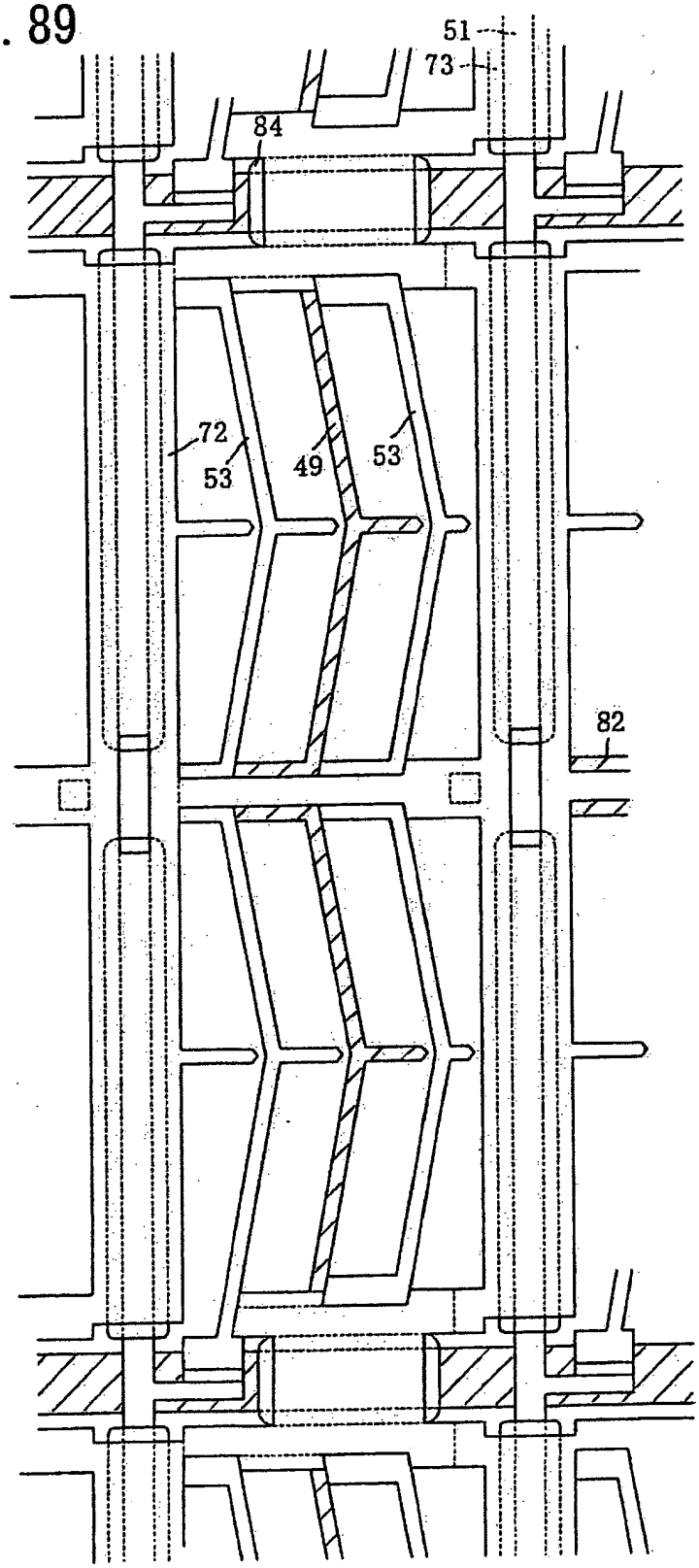


FIG. 90

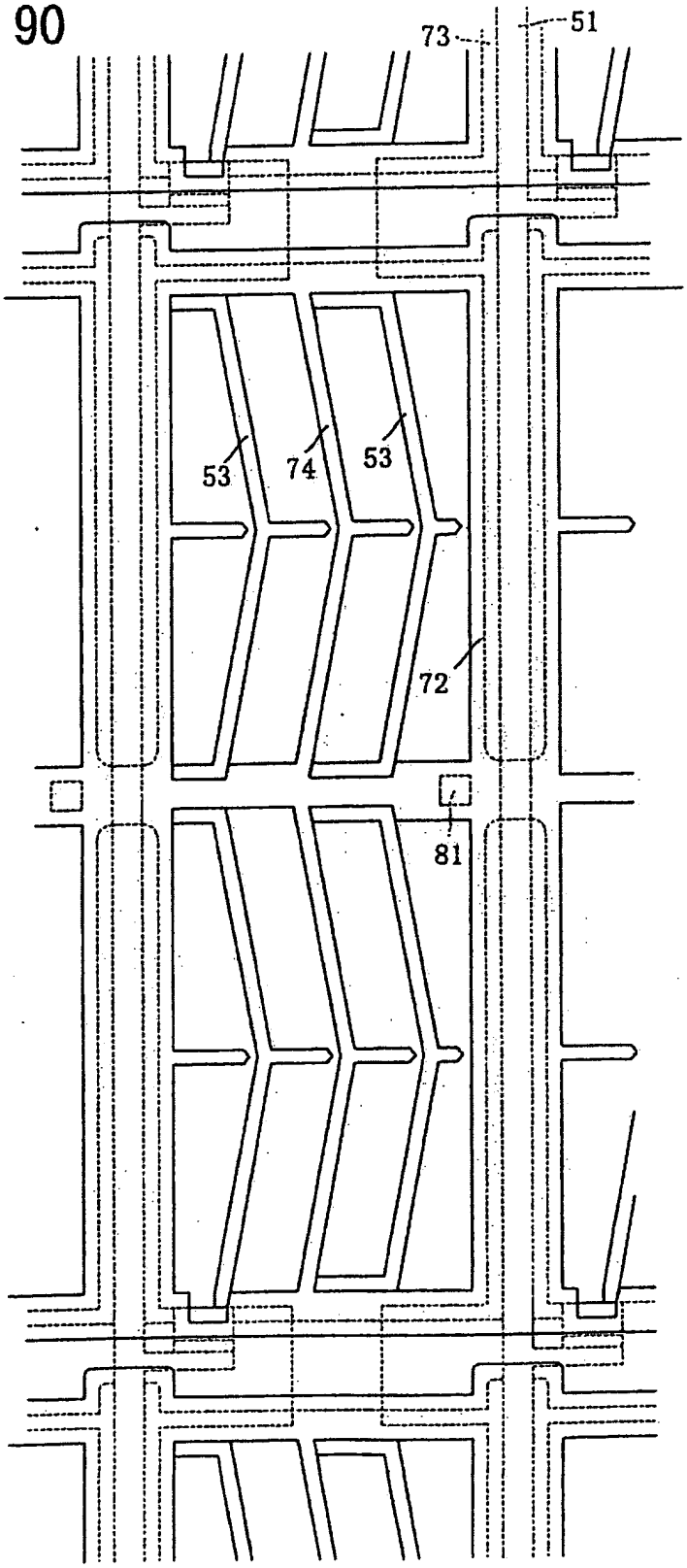


FIG. 91

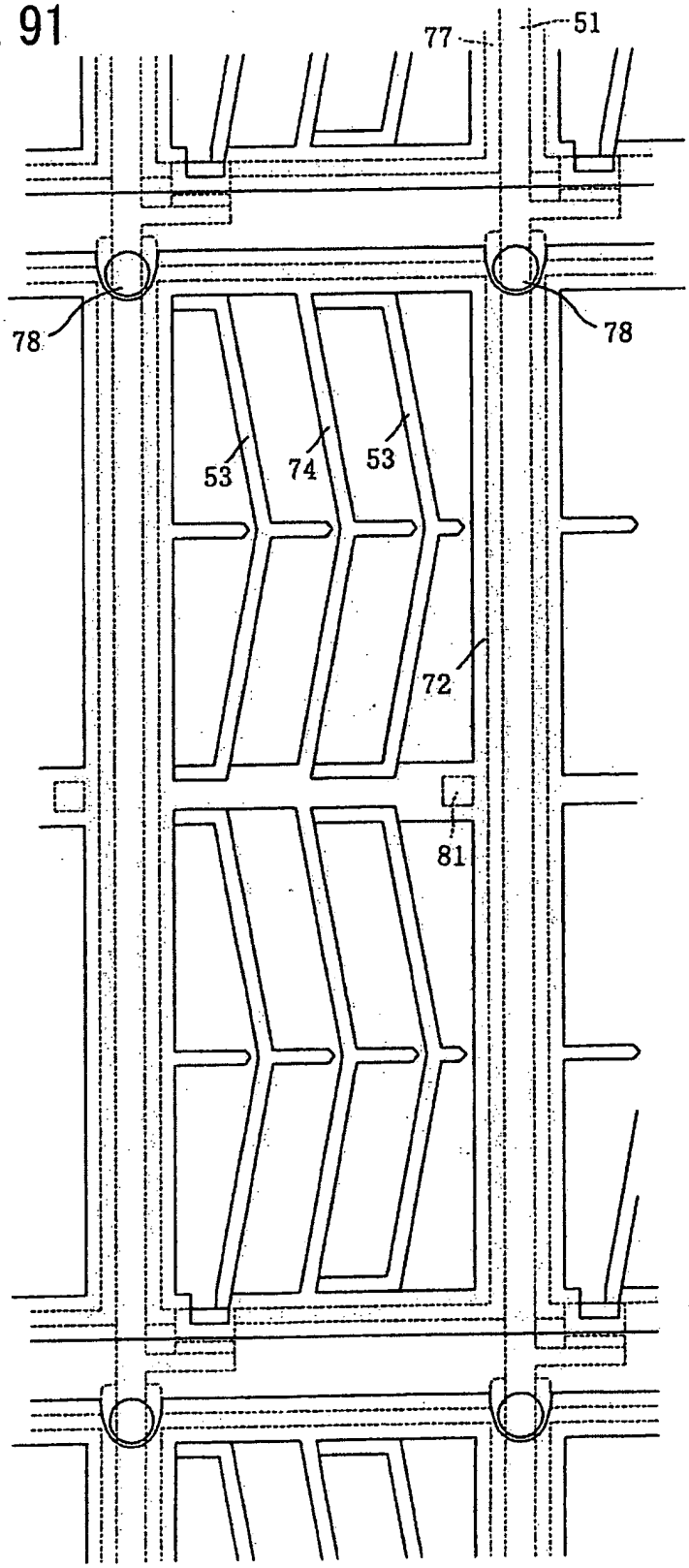


FIG. 92

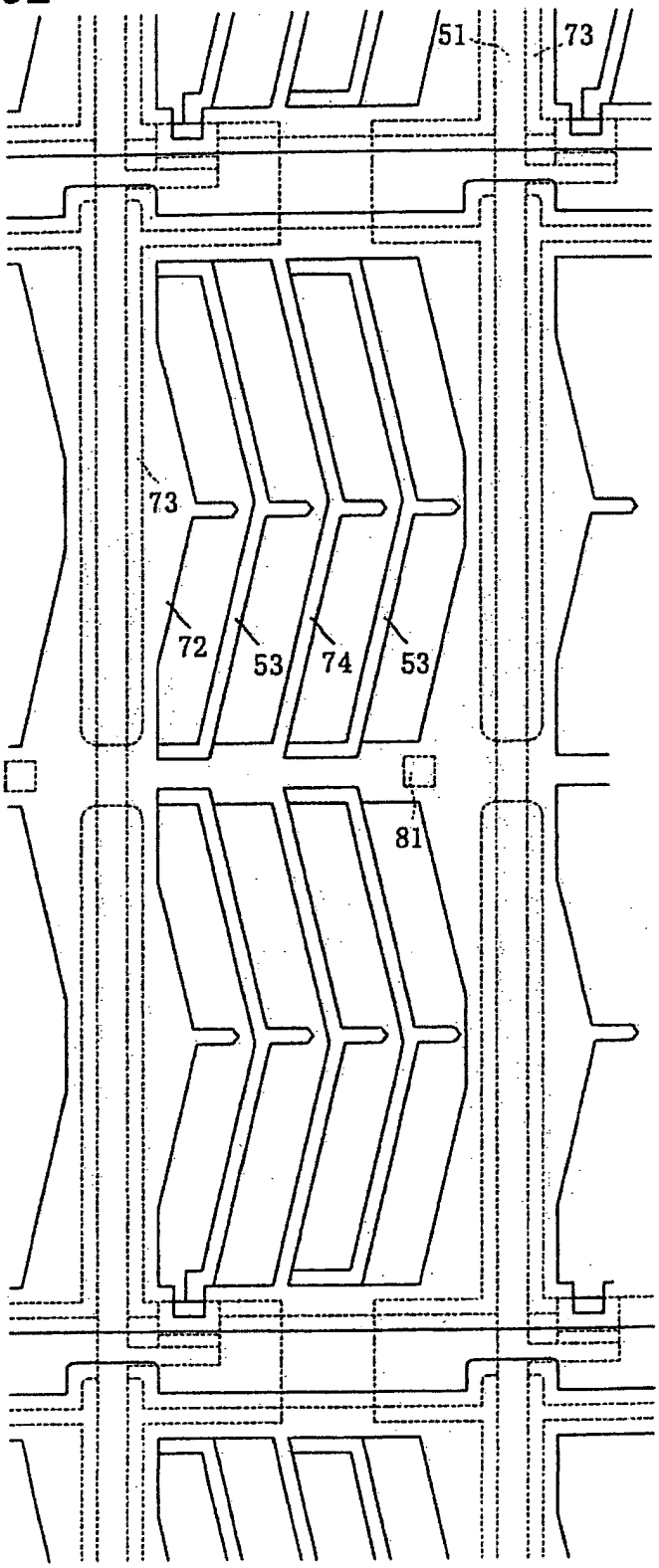


FIG. 93

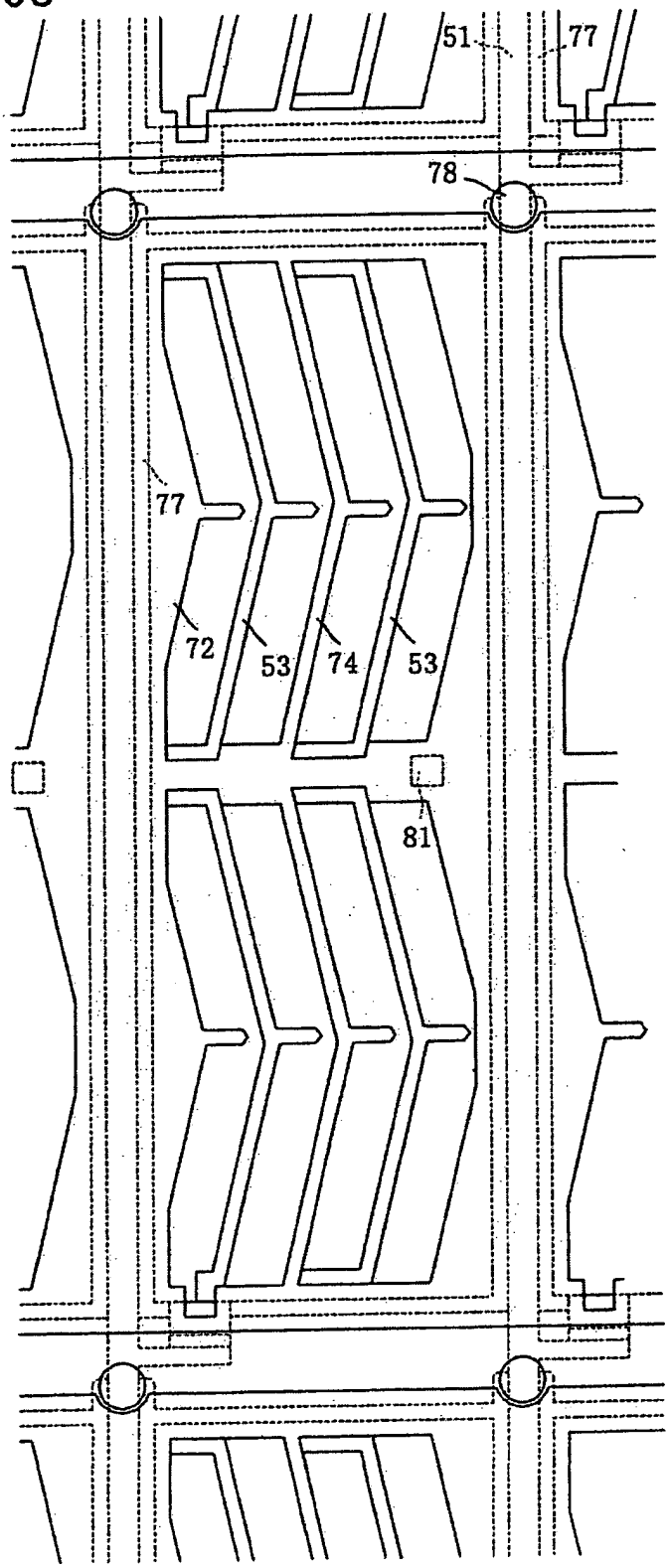


FIG. 94

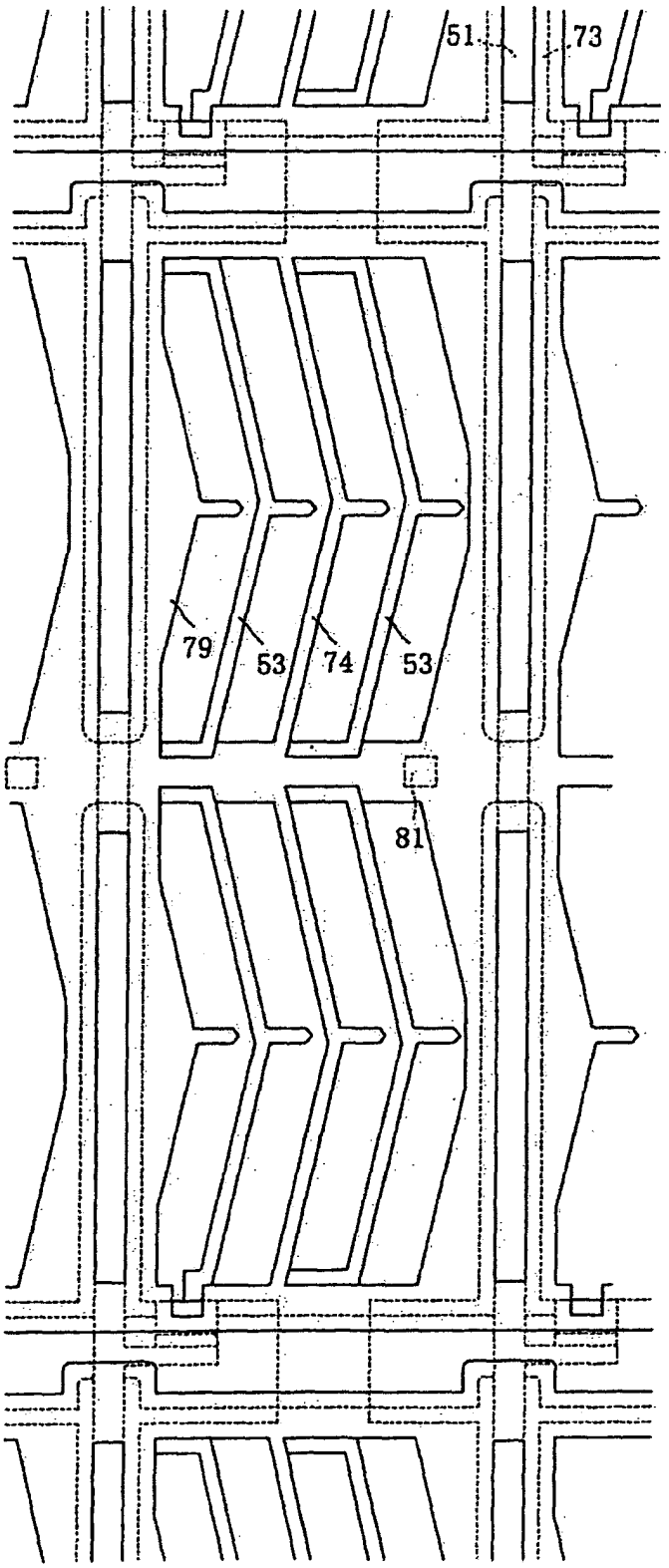


FIG. 95

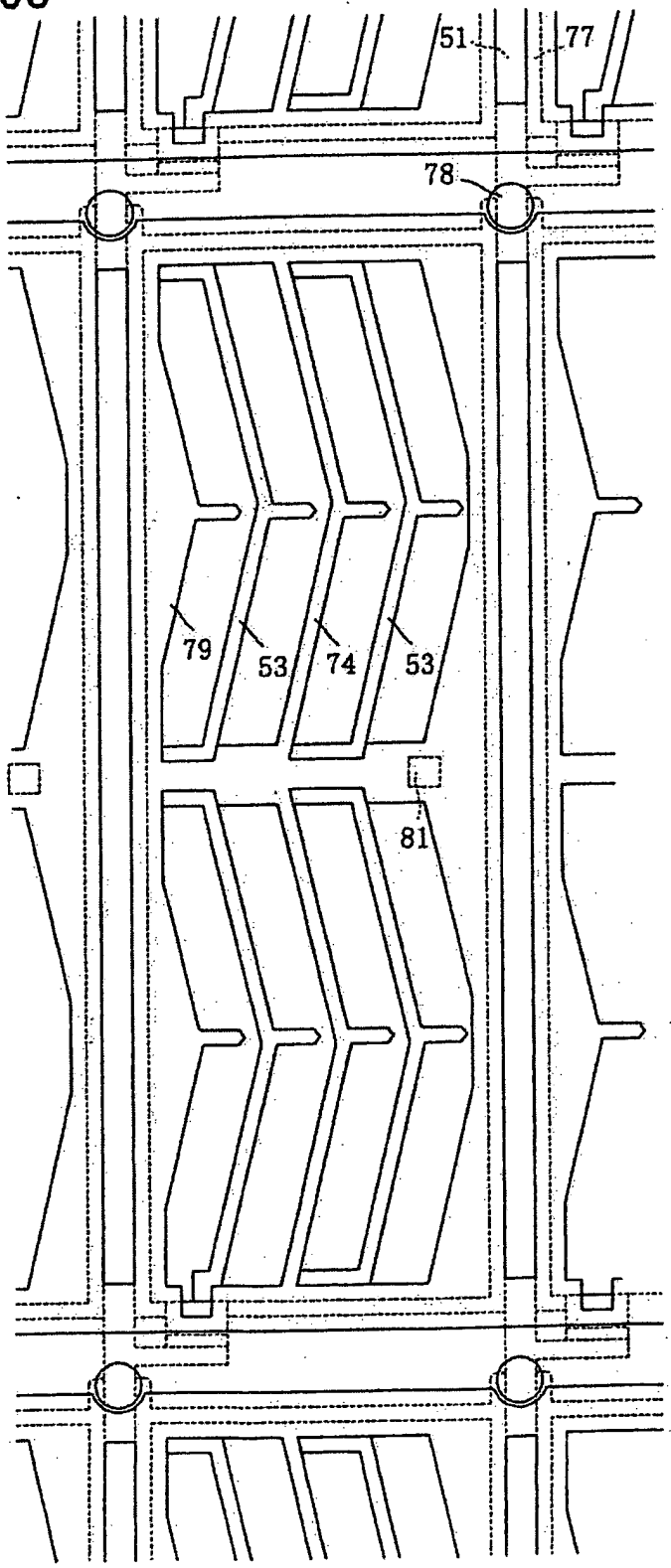


FIG. 96

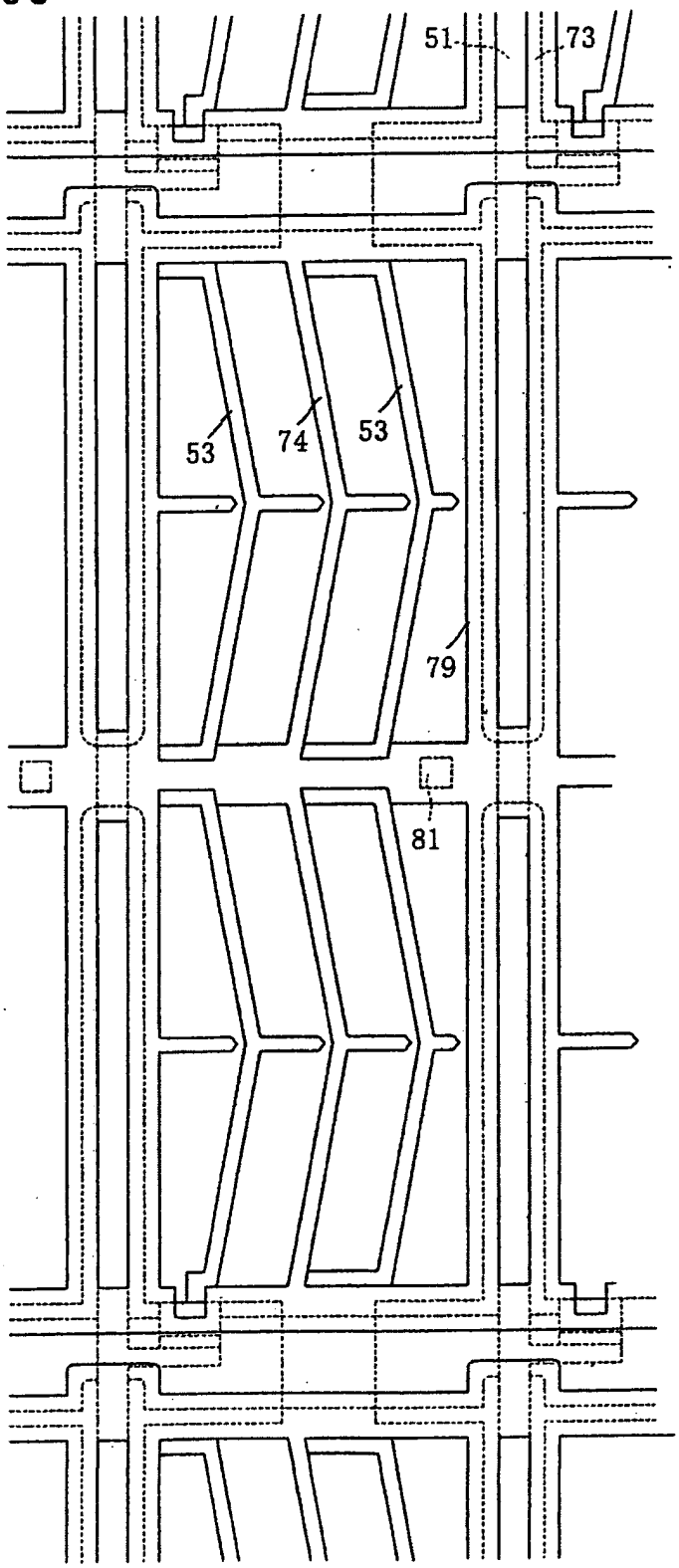


FIG. 97

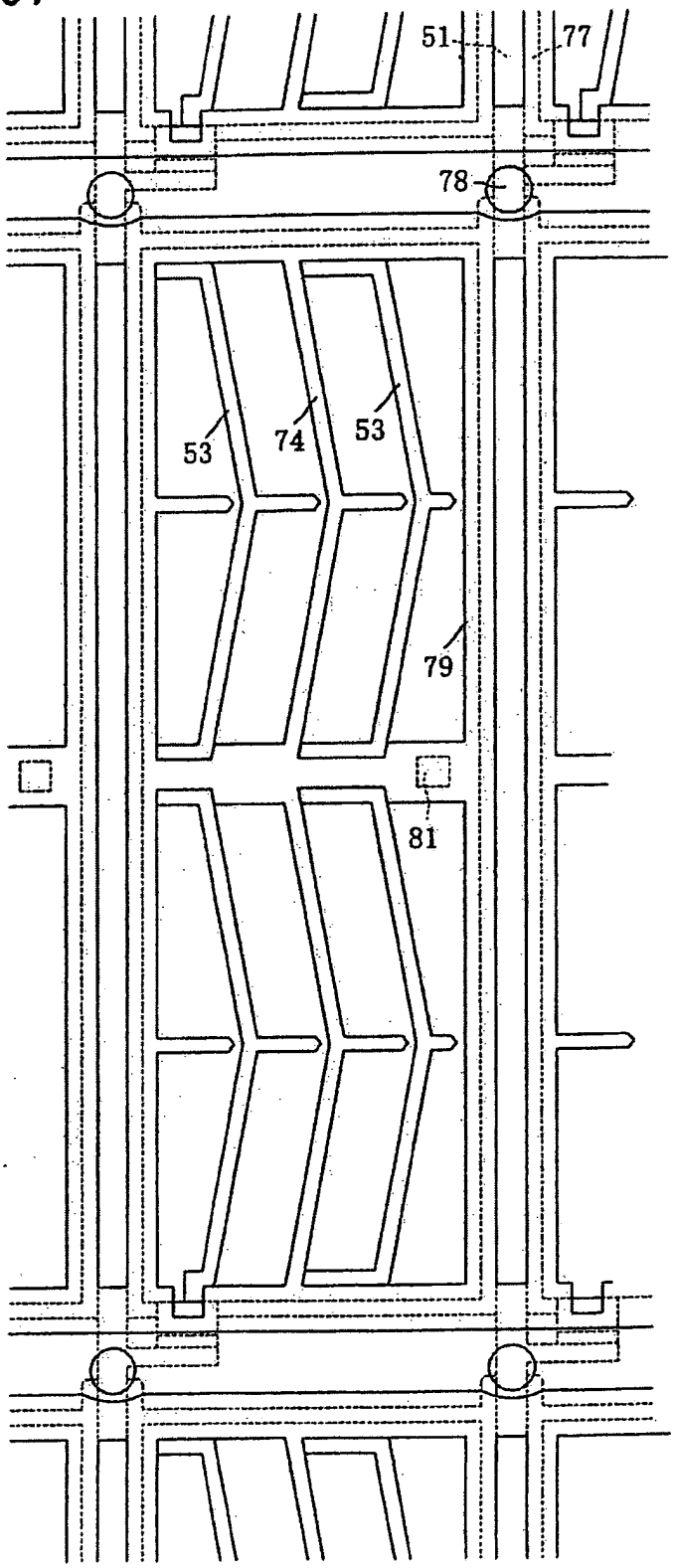


FIG. 98

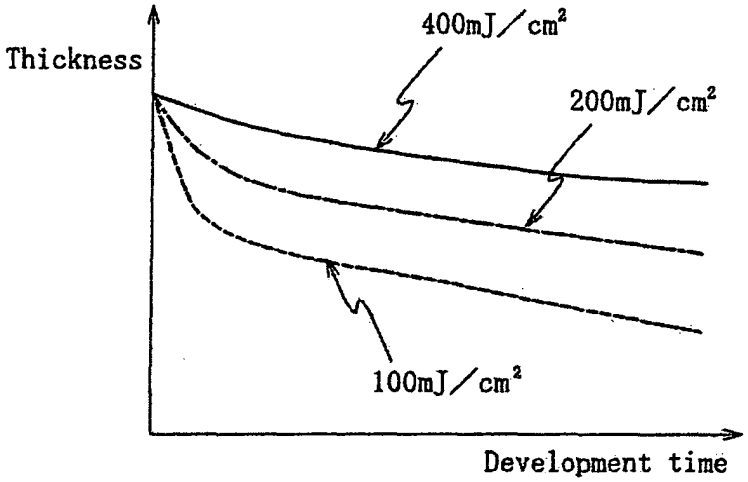

Thickness
400mJ/cm²
200mJ/cm²
100mJ/cm²
Development time

FIG. 99

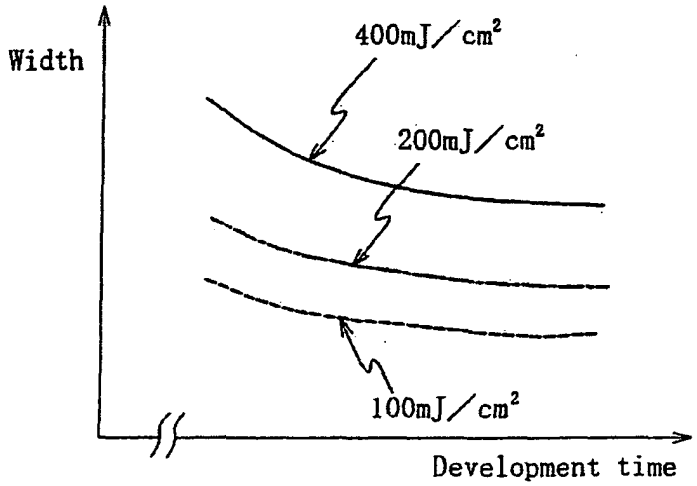

Width
400mJ/cm²
200mJ/cm²
100mJ/cm²
Development time

FIG. 100(A)

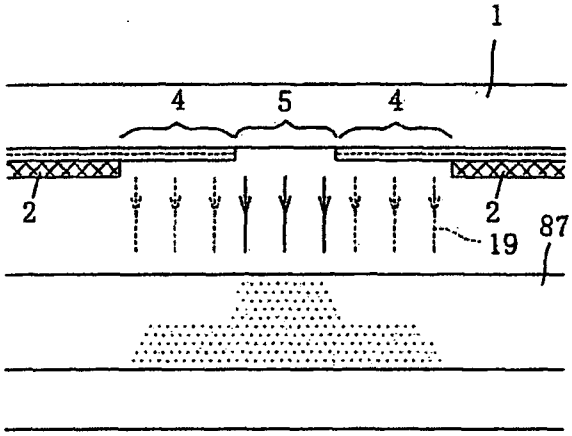


FIG. 100(B)

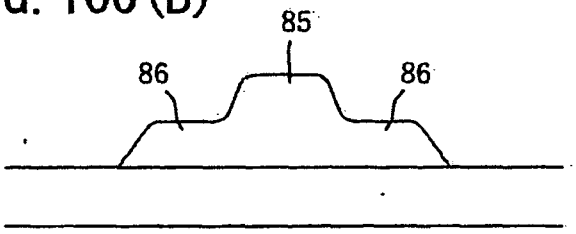


FIG. 101 (A)

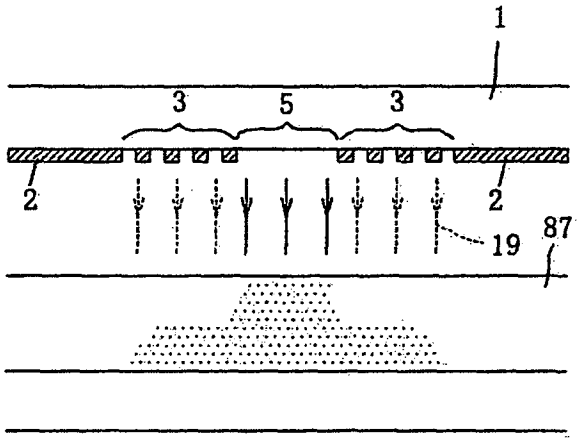


FIG. 101 (B)

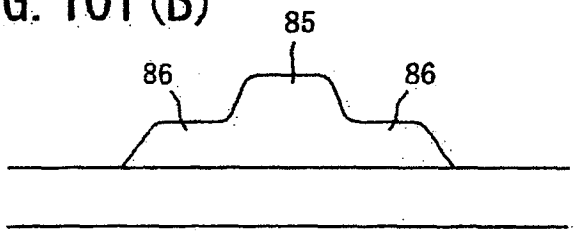


FIG. 102 (A) 1 st Exposure

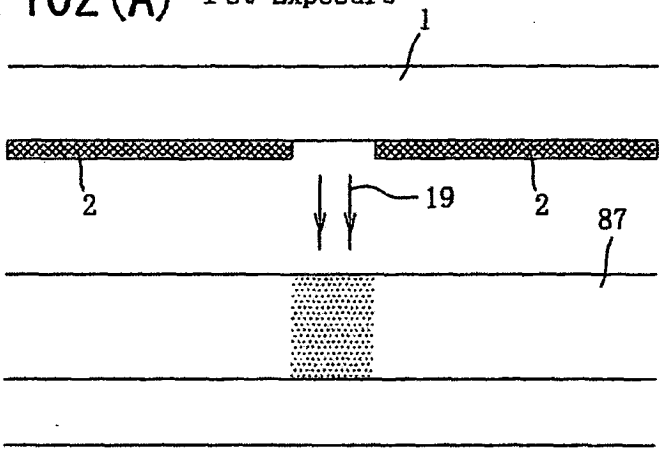


FIG. 102 (B) 2nd Exposure

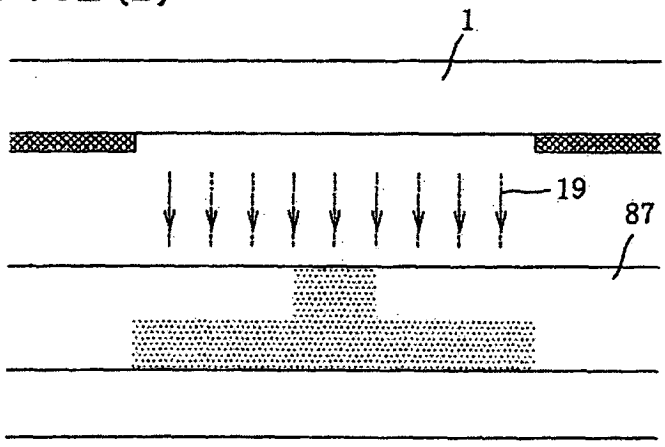


FIG. 102 (C)

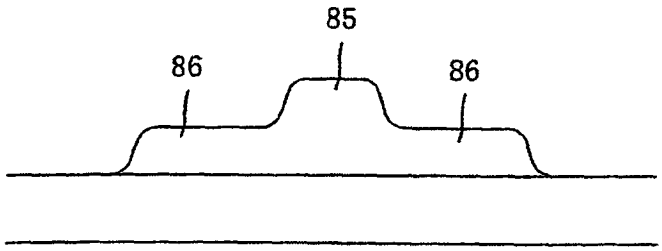


FIG. 103 (A) 1 st Exposure

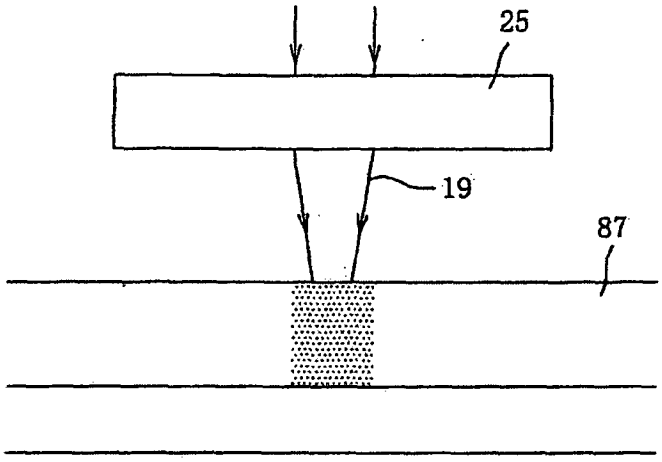


FIG. 103 (B) 2nd Exposure

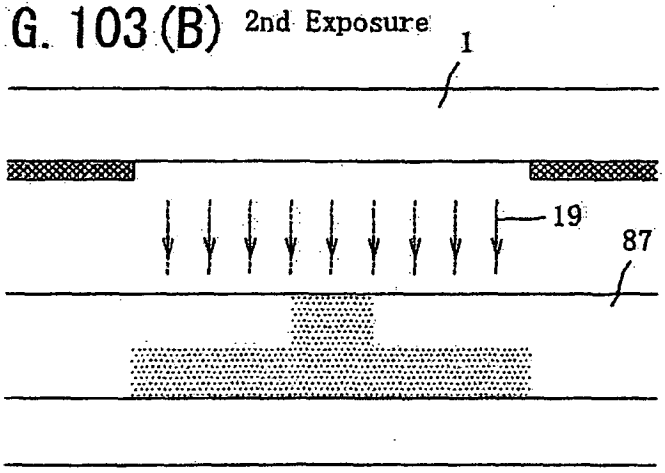
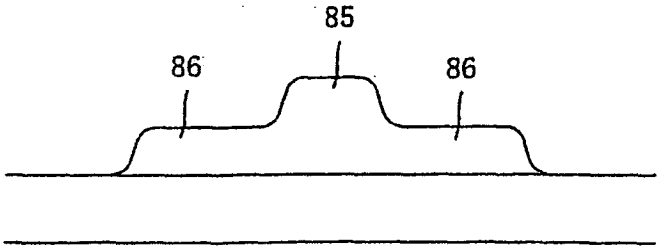


FIG. 103 (C)



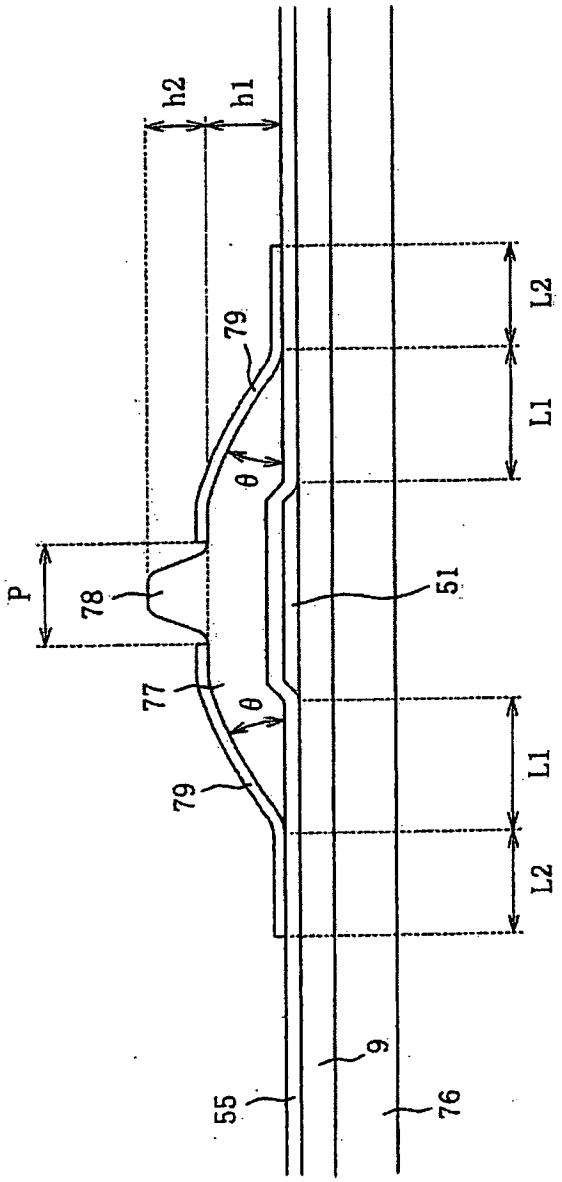


FIG. 104

FIG. 105

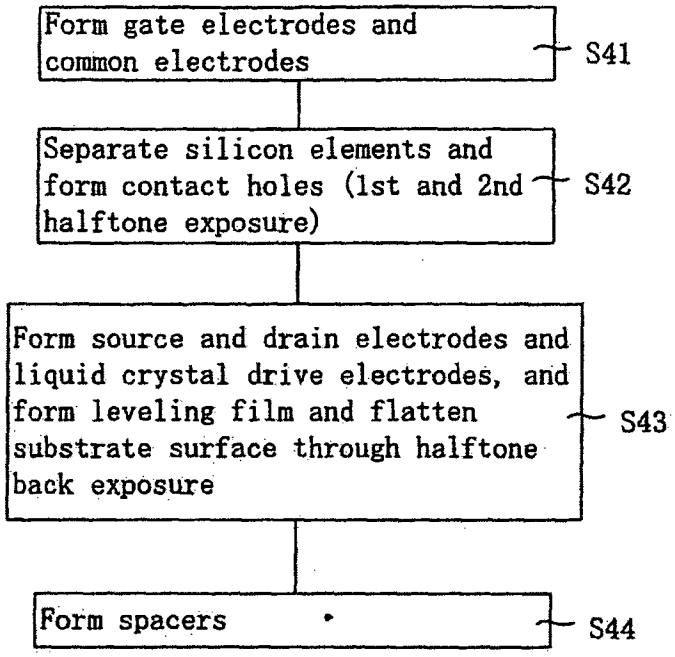

Form gate electrodes and common electrodes
S41
Separate silicon elements and form contact holes (1st and 2nd halftone exposure)
S42
Form source and drain electrodes and liquid crystal drive electrodes, and form leveling film and flatten substrate surface through halftone back exposure
S43
Form spacers
S44

FIG. 106 (A)

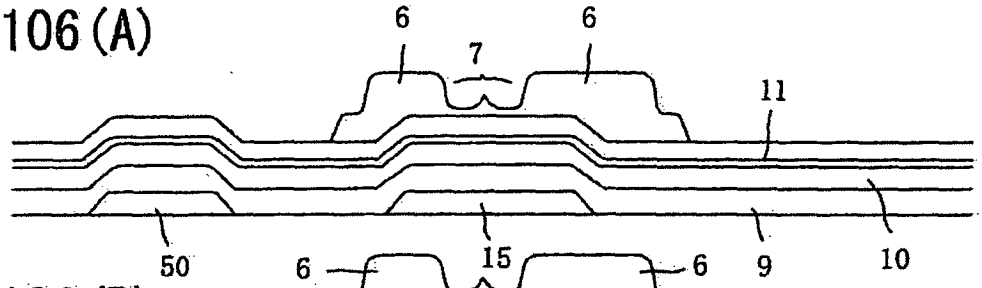


FIG. 106 (B)

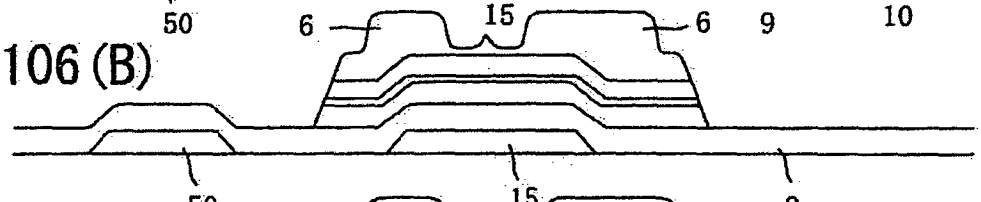


FIG. 106 (C)

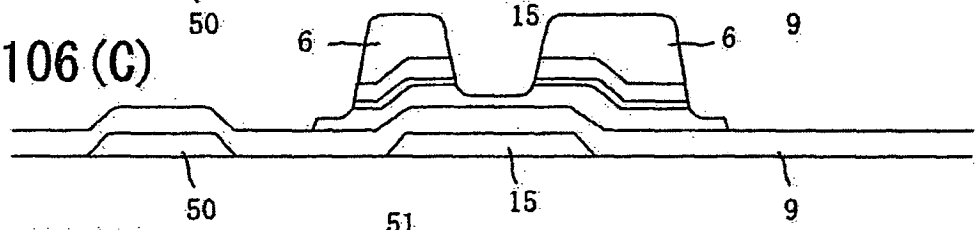


FIG. 106 (D)

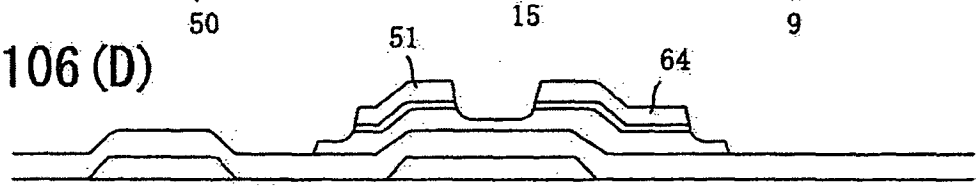


FIG. 106 (E)

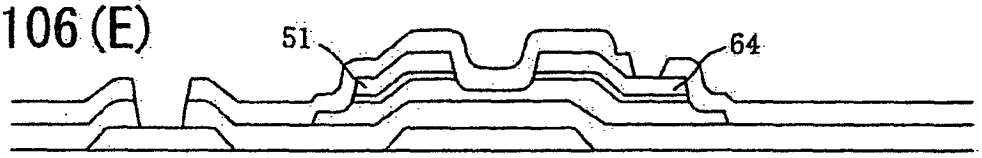


FIG. 106 (F)

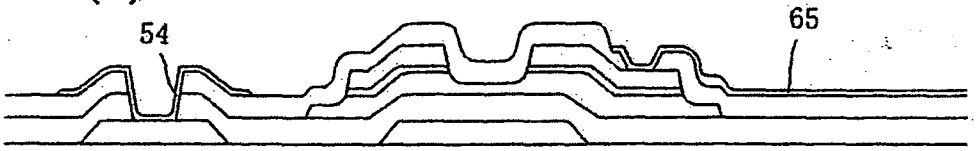


FIG. 107 (A)

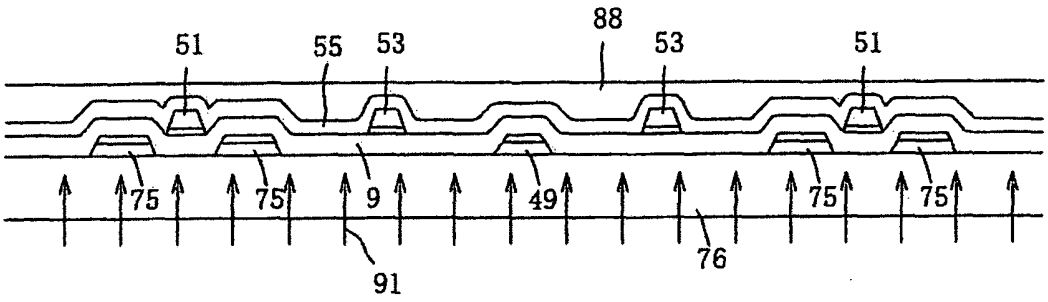


FIG. 107 (B)

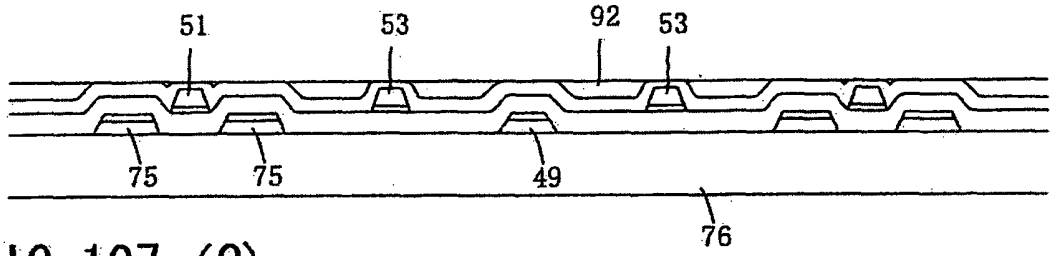


FIG. 107 (C)

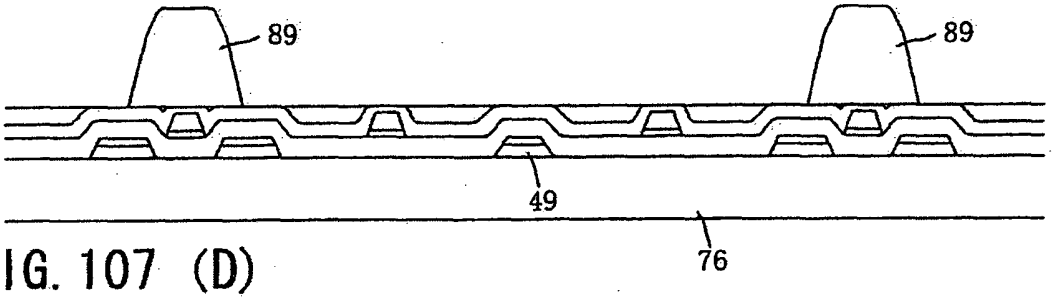


FIG. 107 (D)

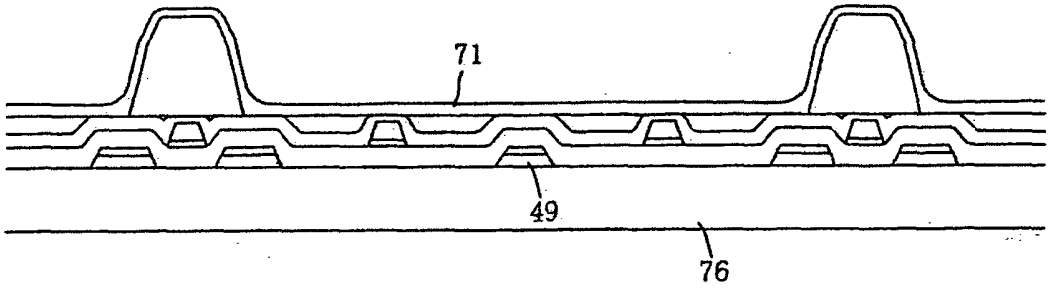


FIG. 108

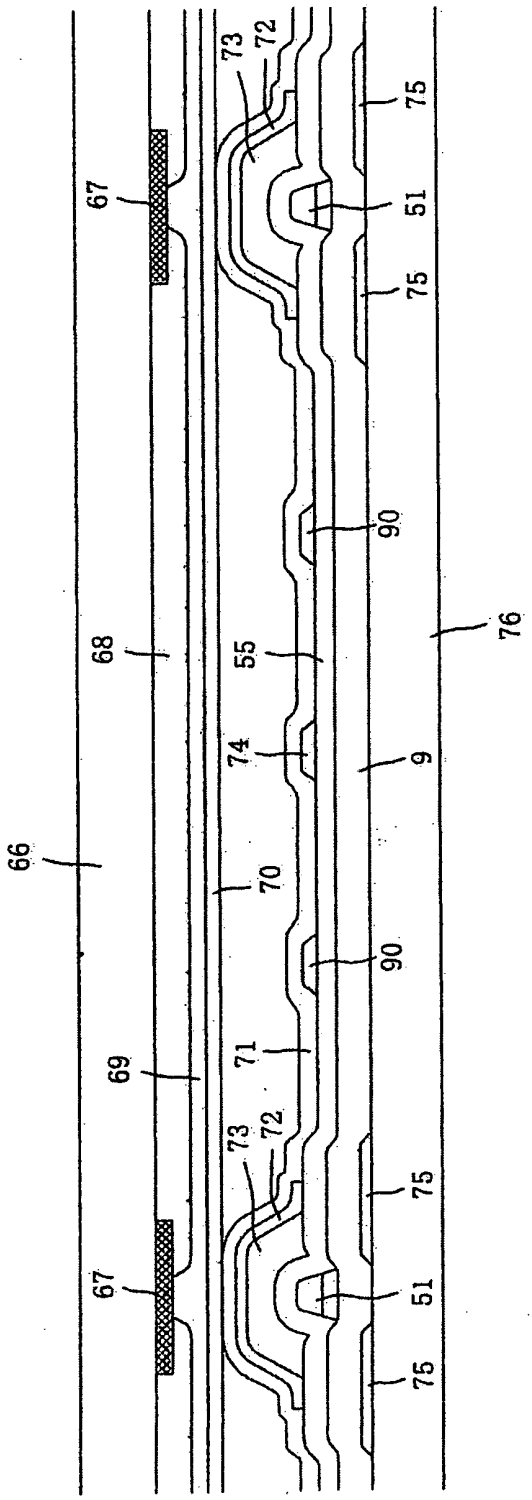


FIG. 109

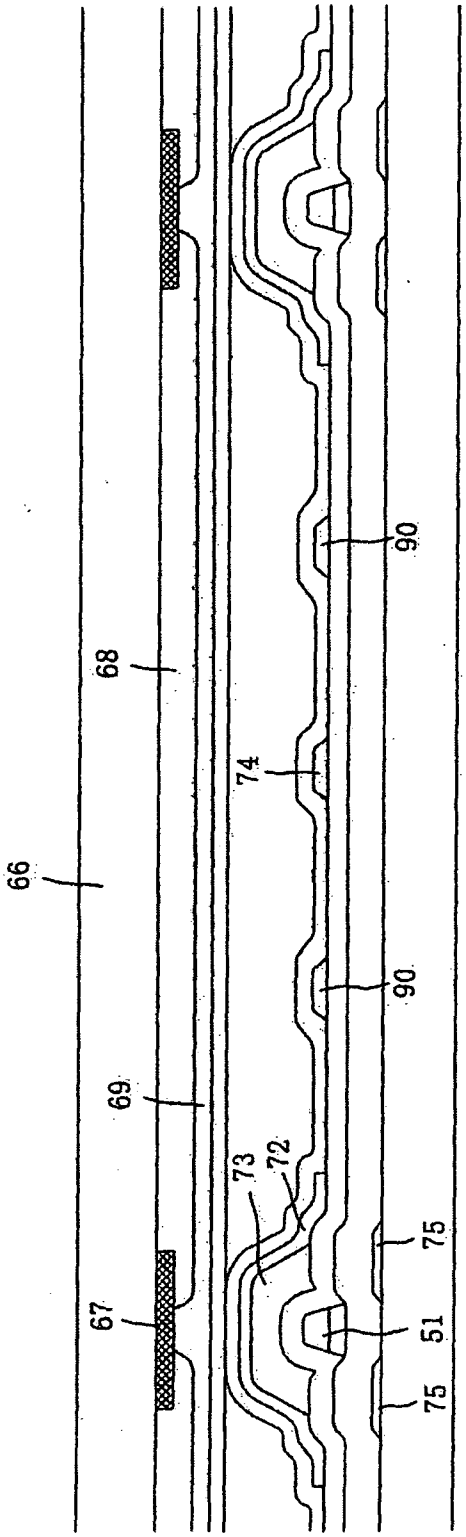


FIG. 110

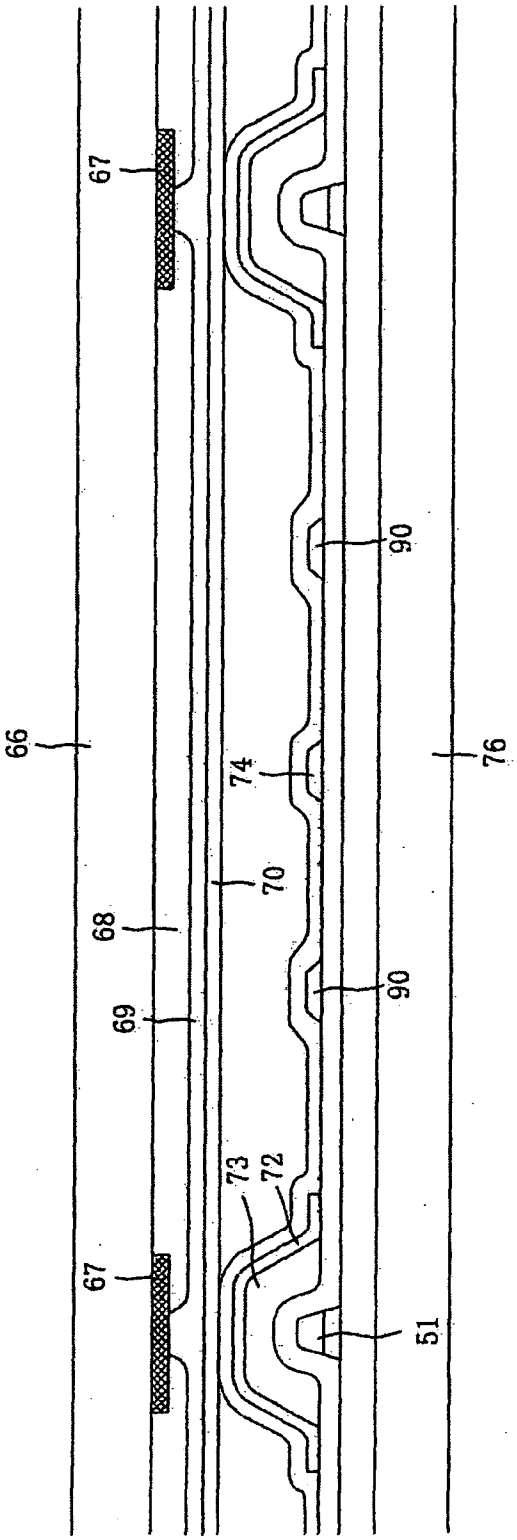


FIG. 111

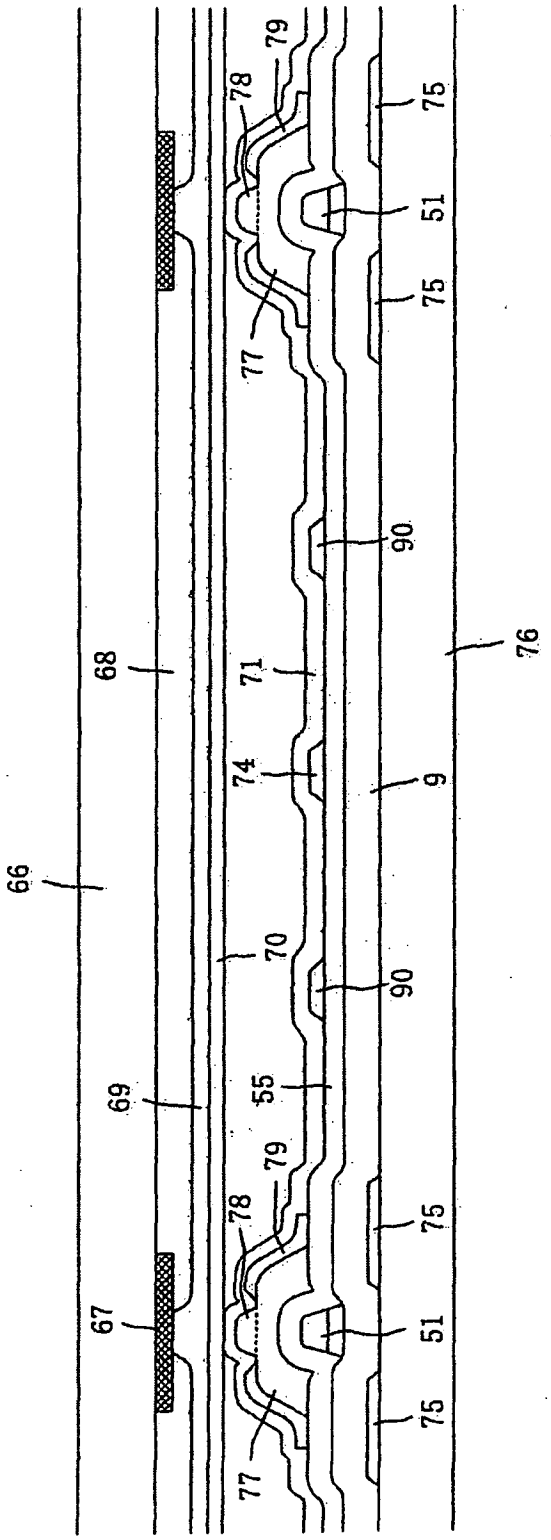


FIG. 112

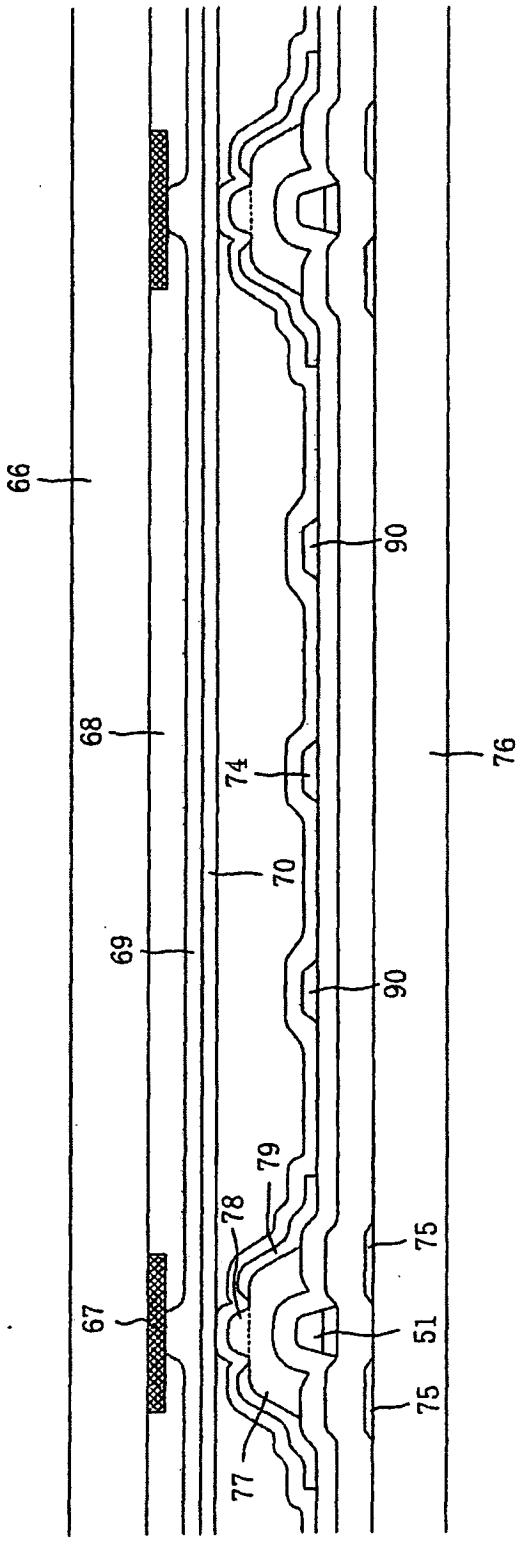


FIG. 113

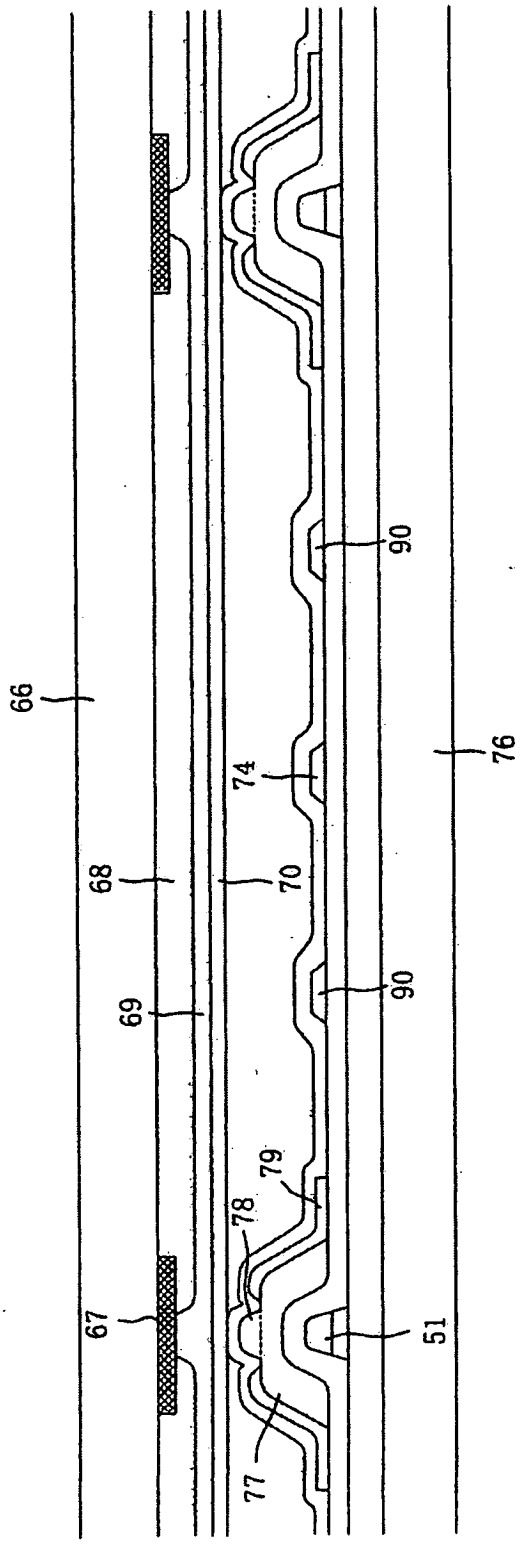


FIG. 114 (A)

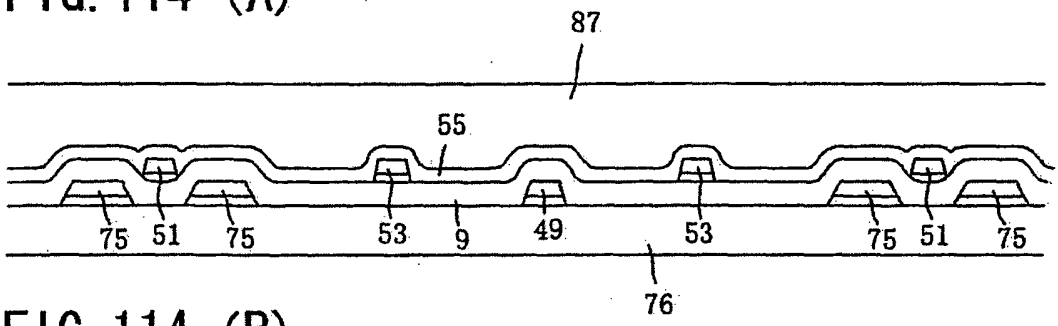


FIG. 114 (B)

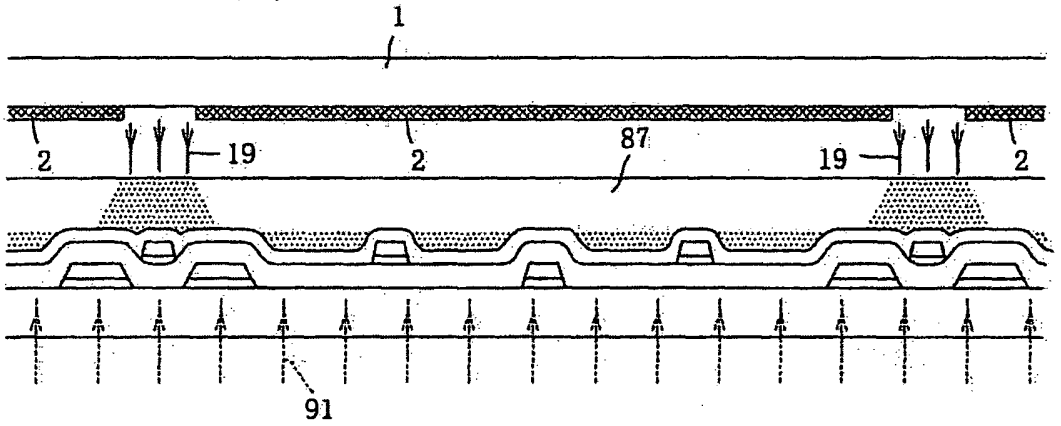


FIG. 114 (C)

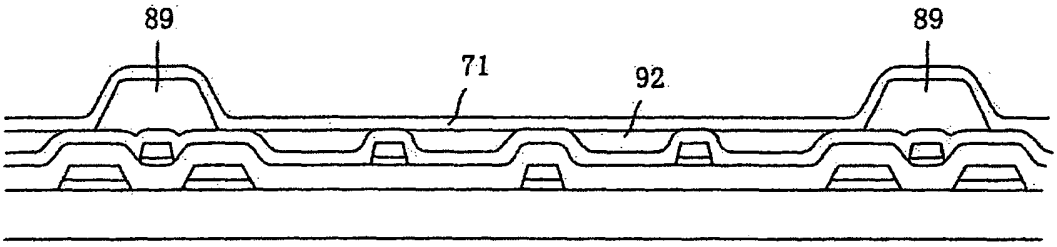


FIG. 115

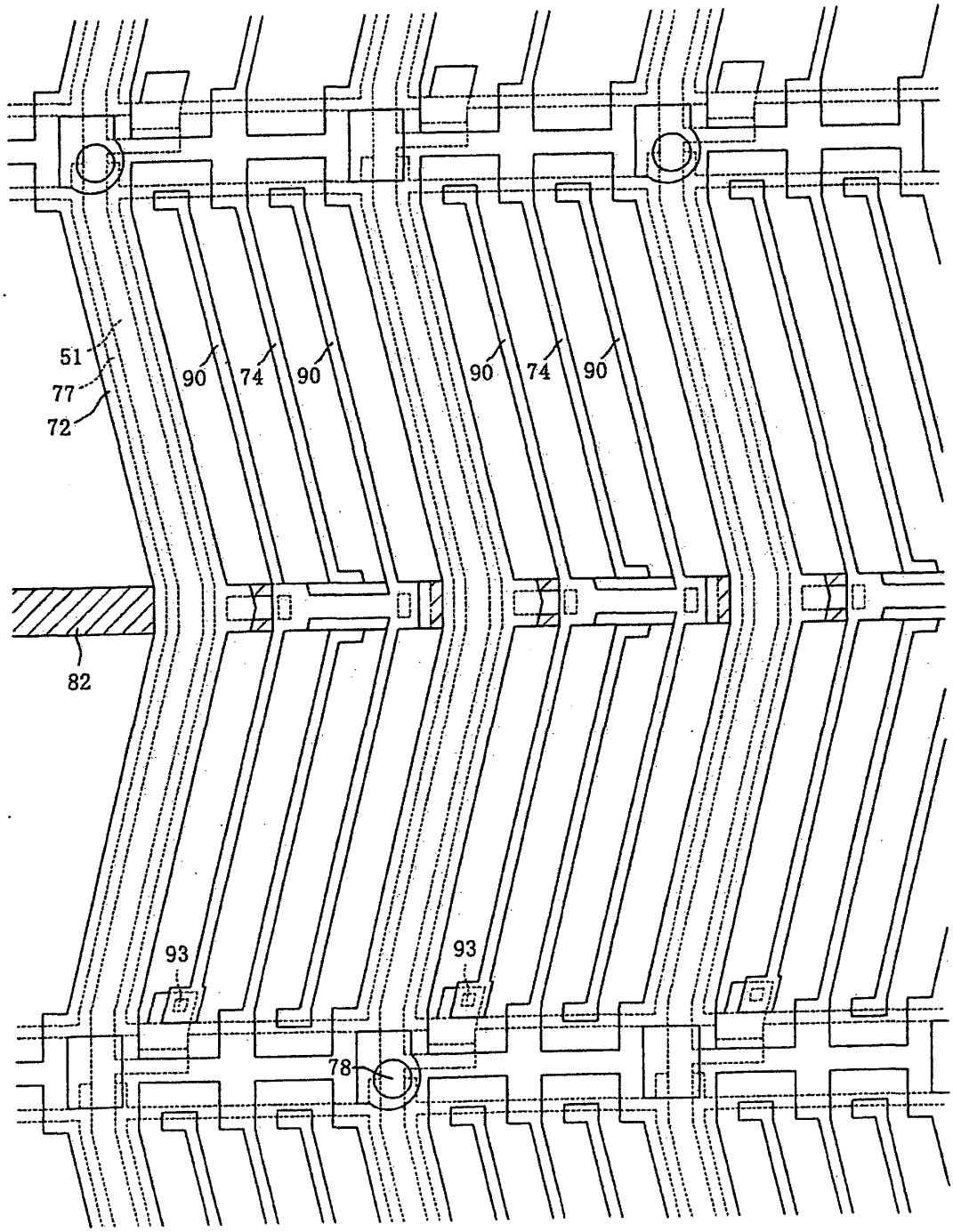


FIG. 116

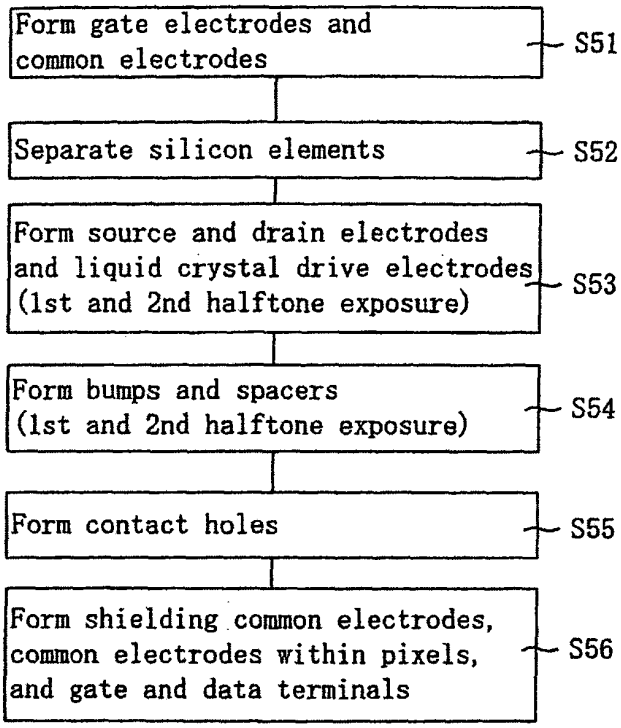


FIG. 117

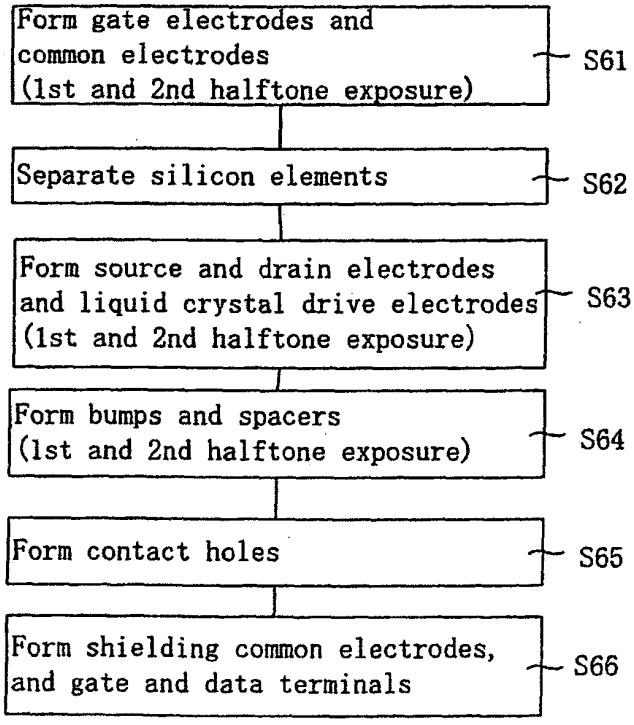


FIG. 118

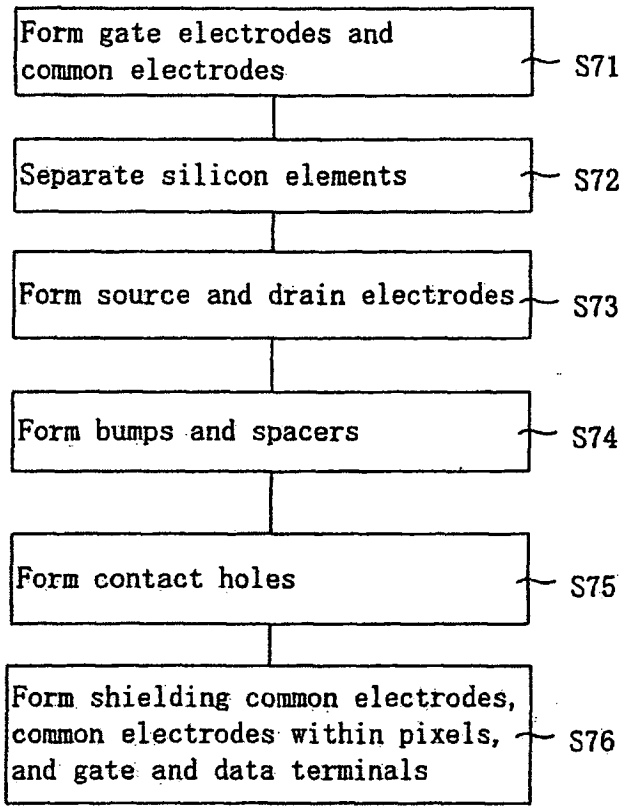

Form gate electrodes and common electrodes
S71
Separate silicon elements
S72
Form source and drain electrodes
S73
Form bumps and spacers
S74
Form contact holes
S75
Form shielding common electrodes, common electrodes within pixels, and gate and data terminals
S76

FIG. 119

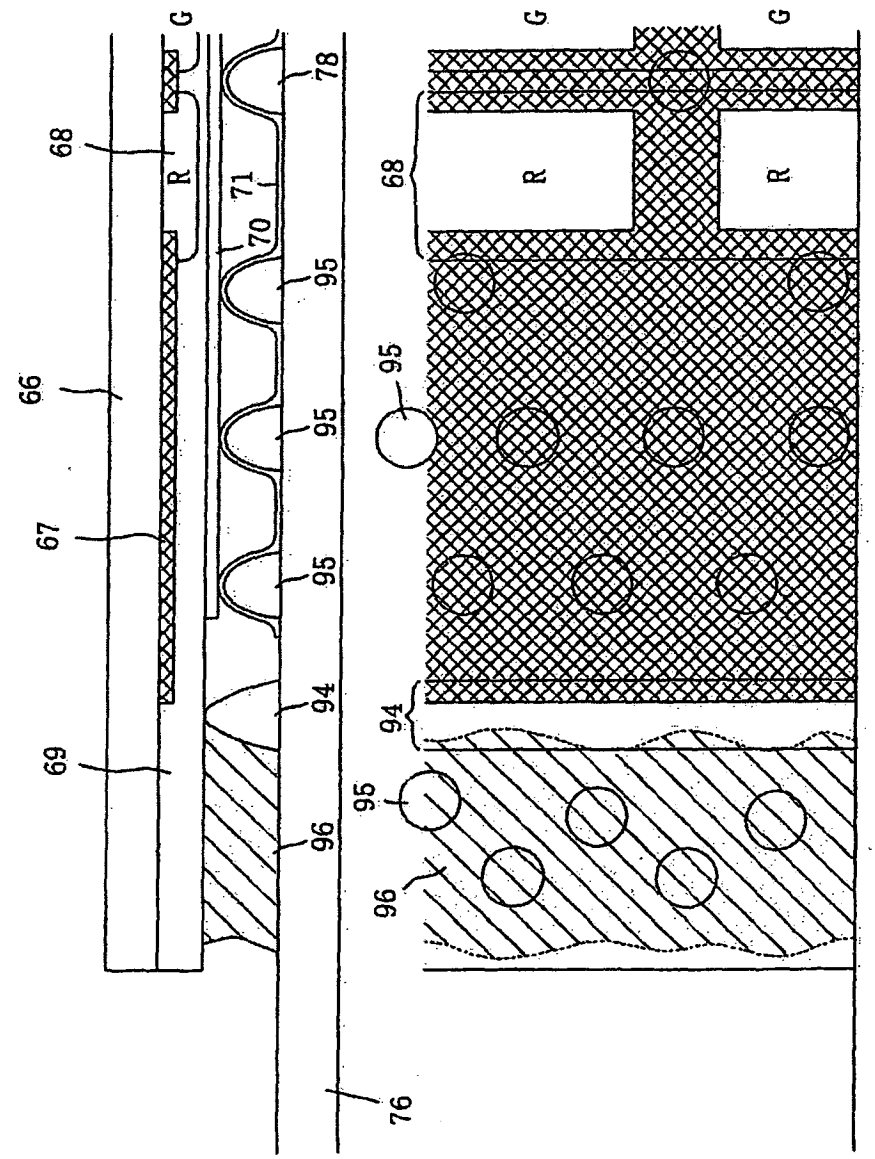


FIG. 120

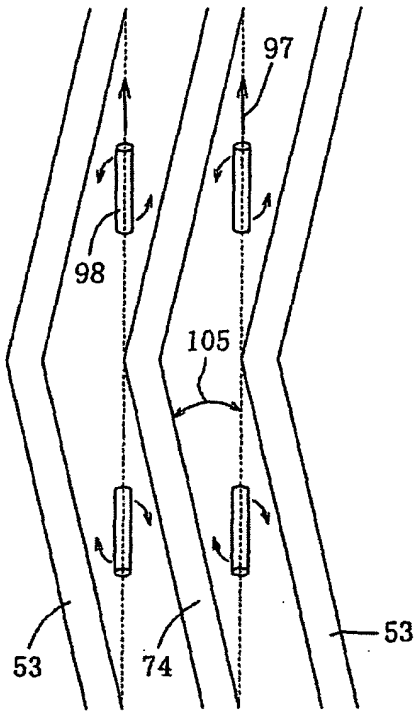


FIG. 121

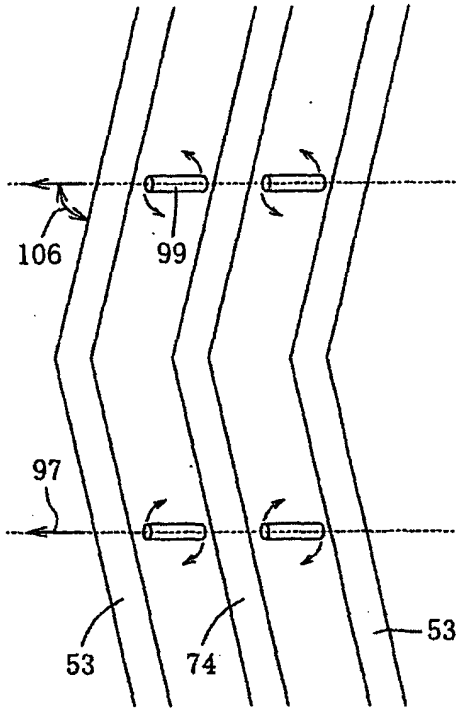


FIG. 122

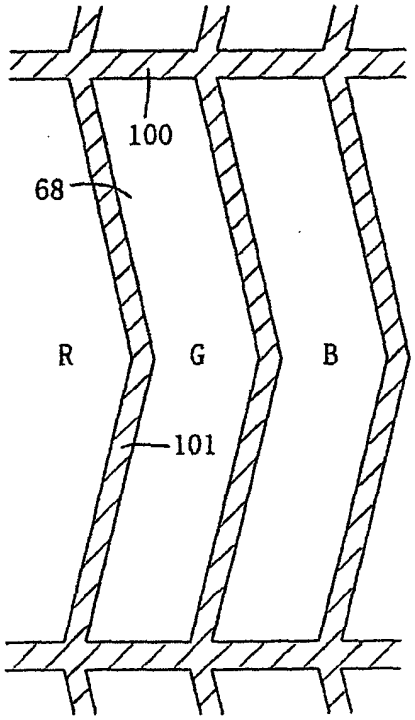


FIG. 123

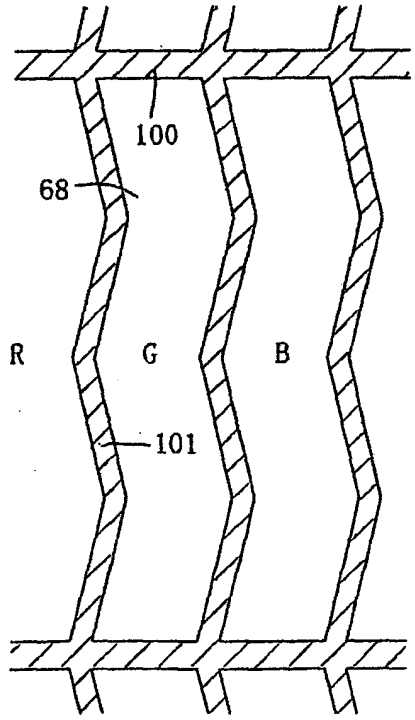


FIG. 124

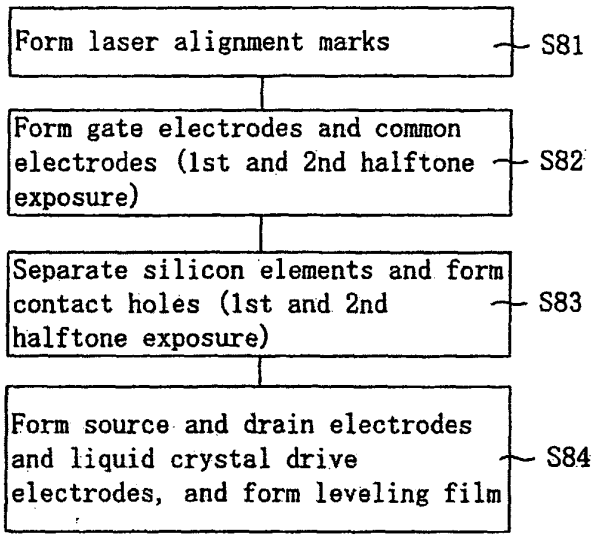


FIG. 125

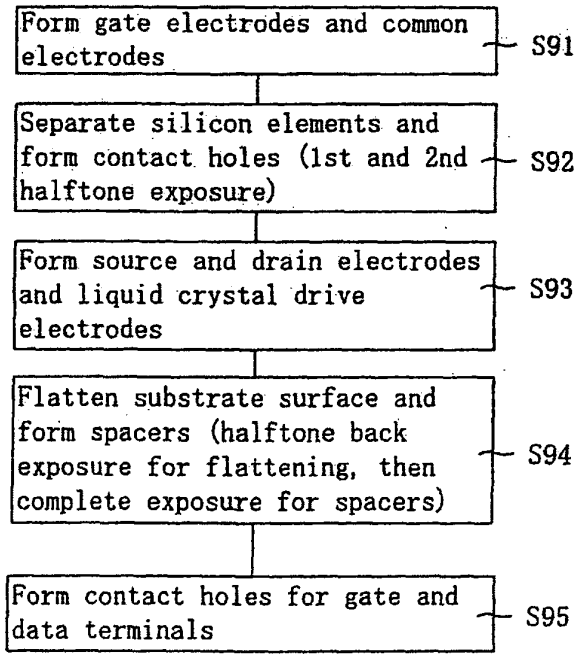


FIG. 126

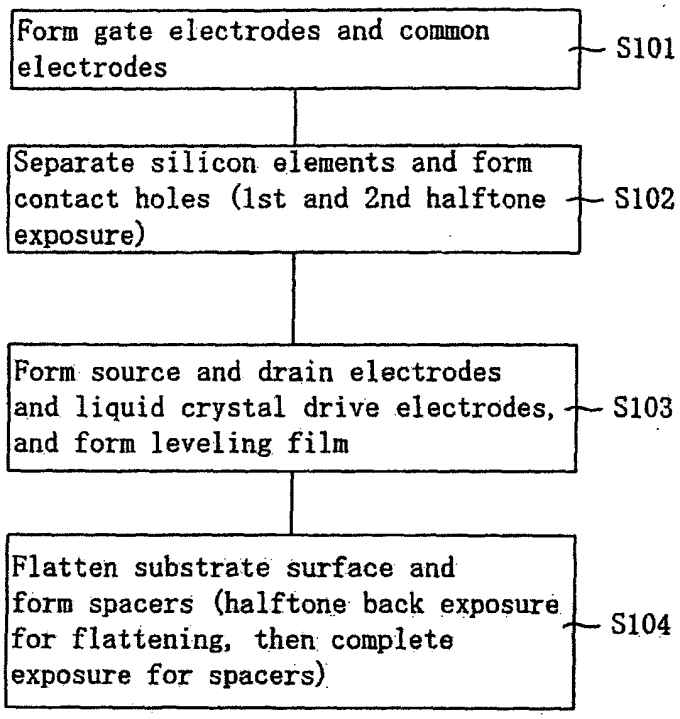


FIG. 127

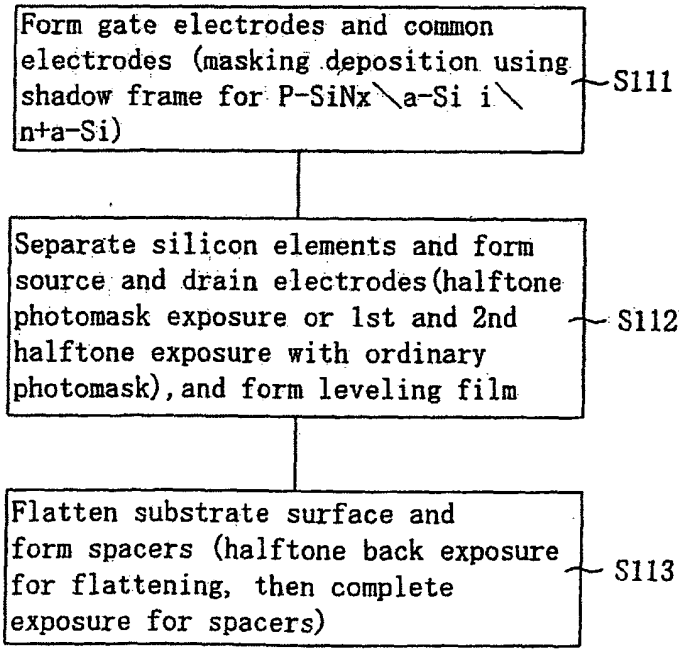


FIG. 128

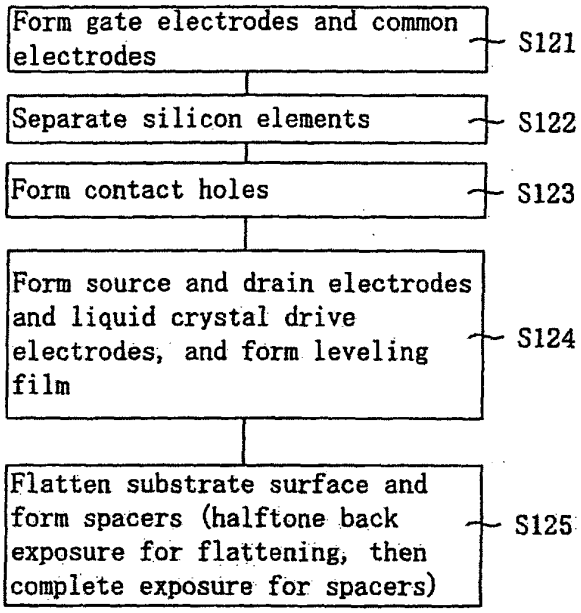


FIG. 129

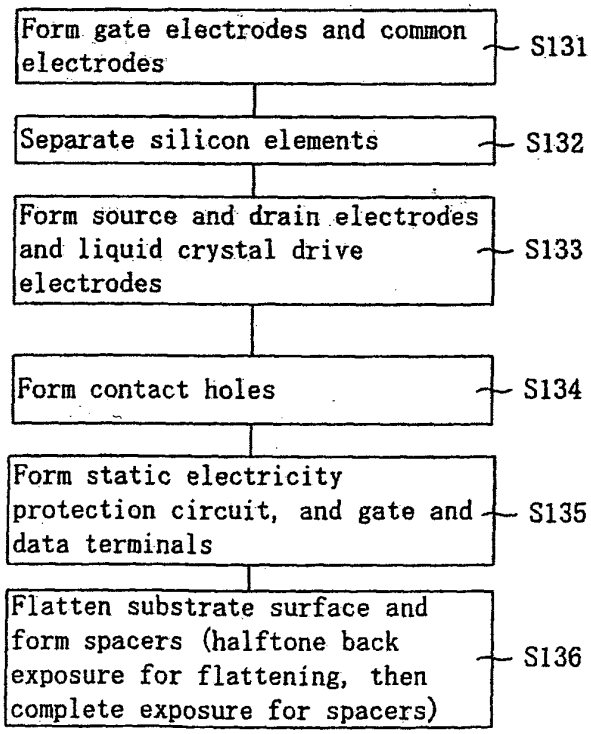


FIG. 130 (A)

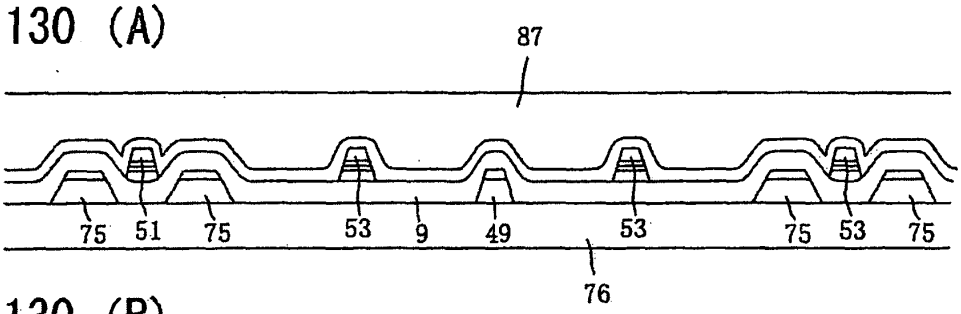


FIG. 130 (B)

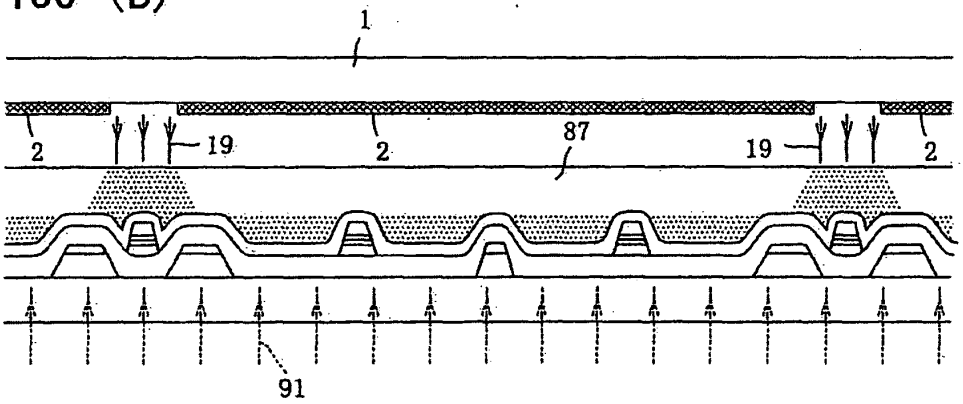


FIG. 130 (C)

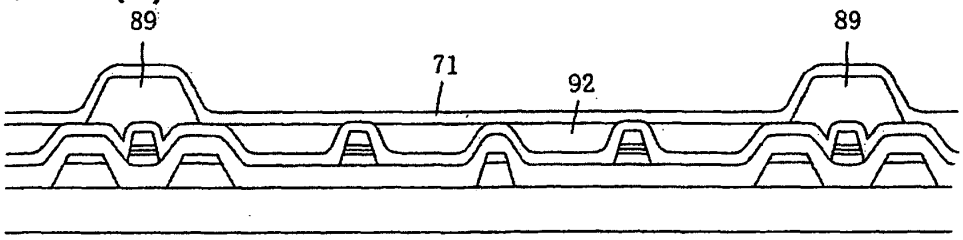


FIG. 131

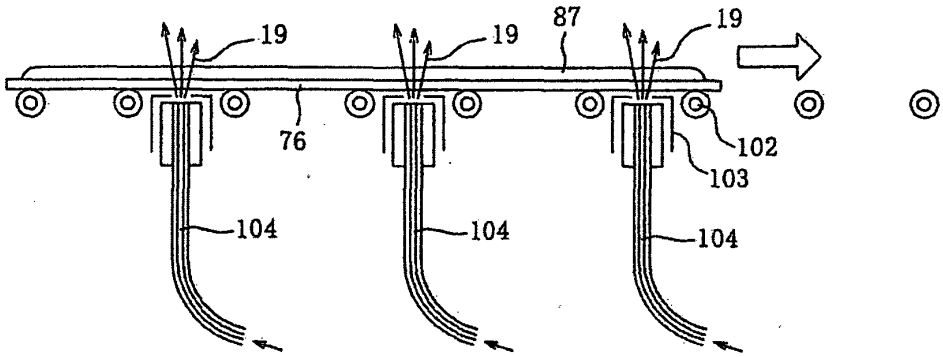


FIG. 132

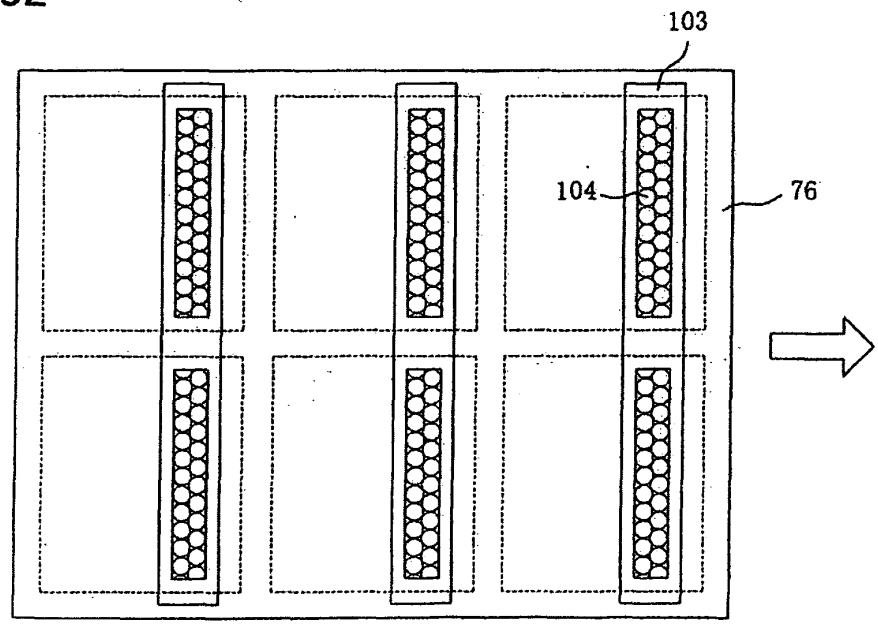


FIG. 133

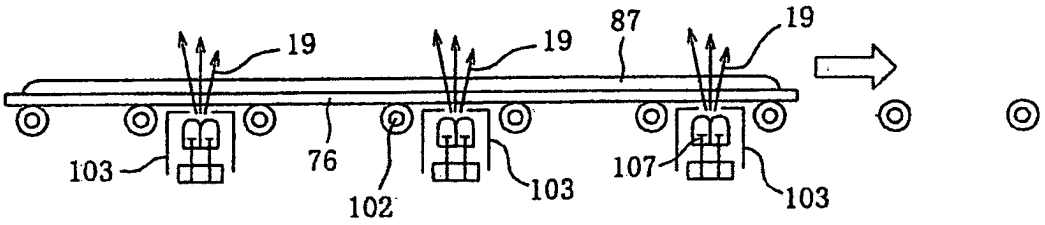


FIG. 134

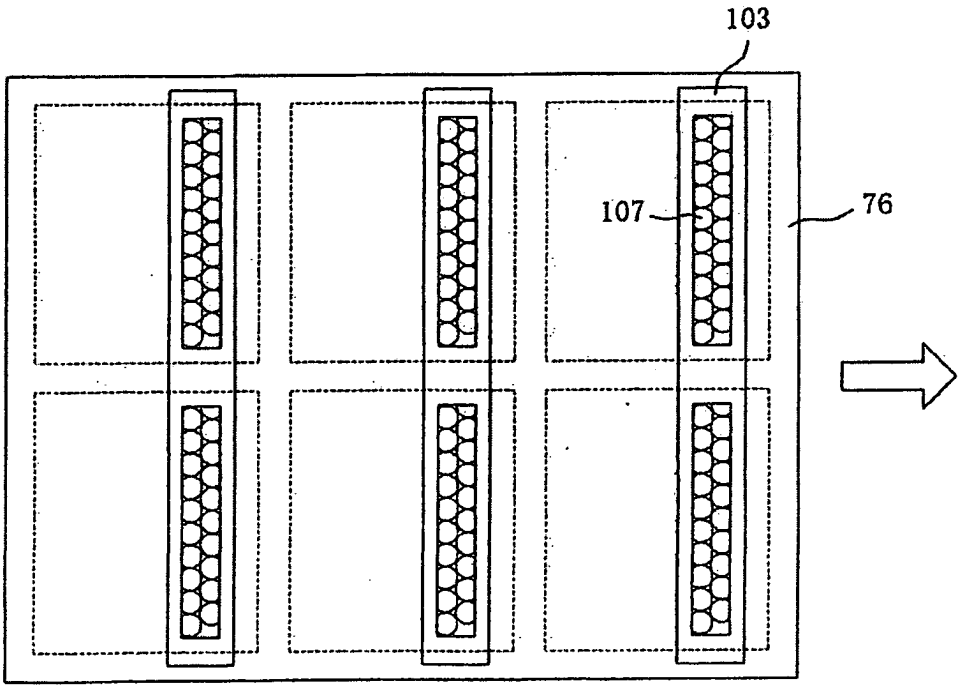


FIG. 135

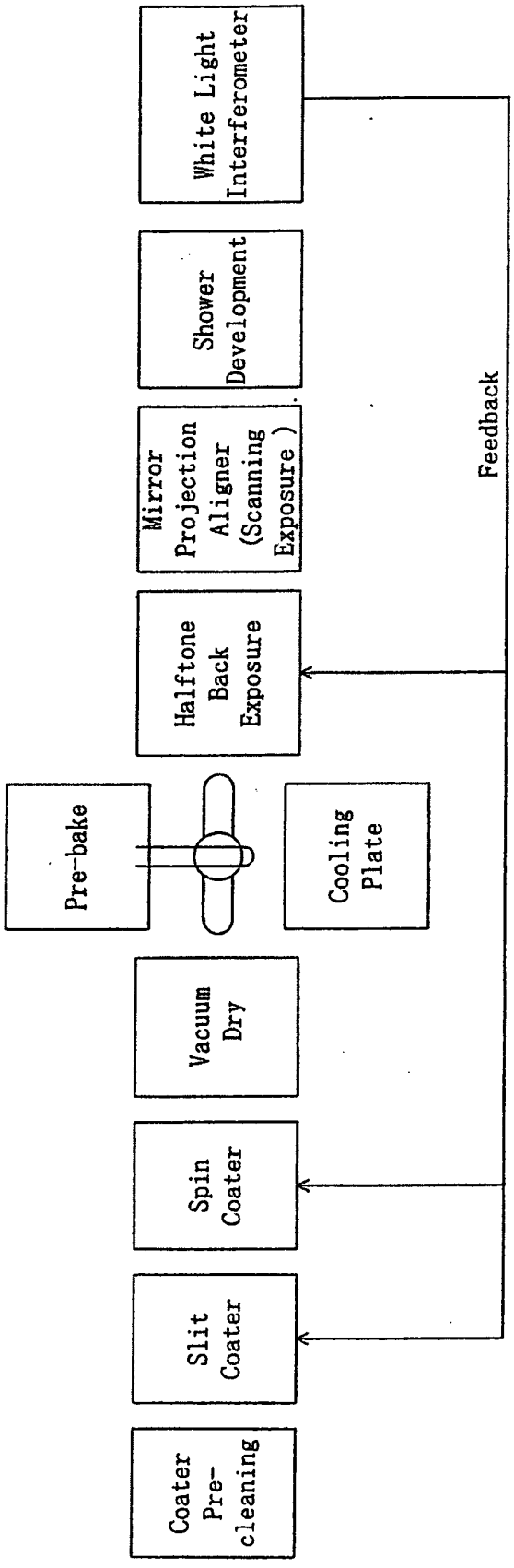

White Light Interferometer
Shower Development
Mirror Projection Aligner (Scanning Exposure)
Halftone Back Exposure
Pre-bake
Cooling Plate
Vacuum Dry
Spin Coater
Slit Coater
Coater Pre-cleaning
Feedback

FIG. 136

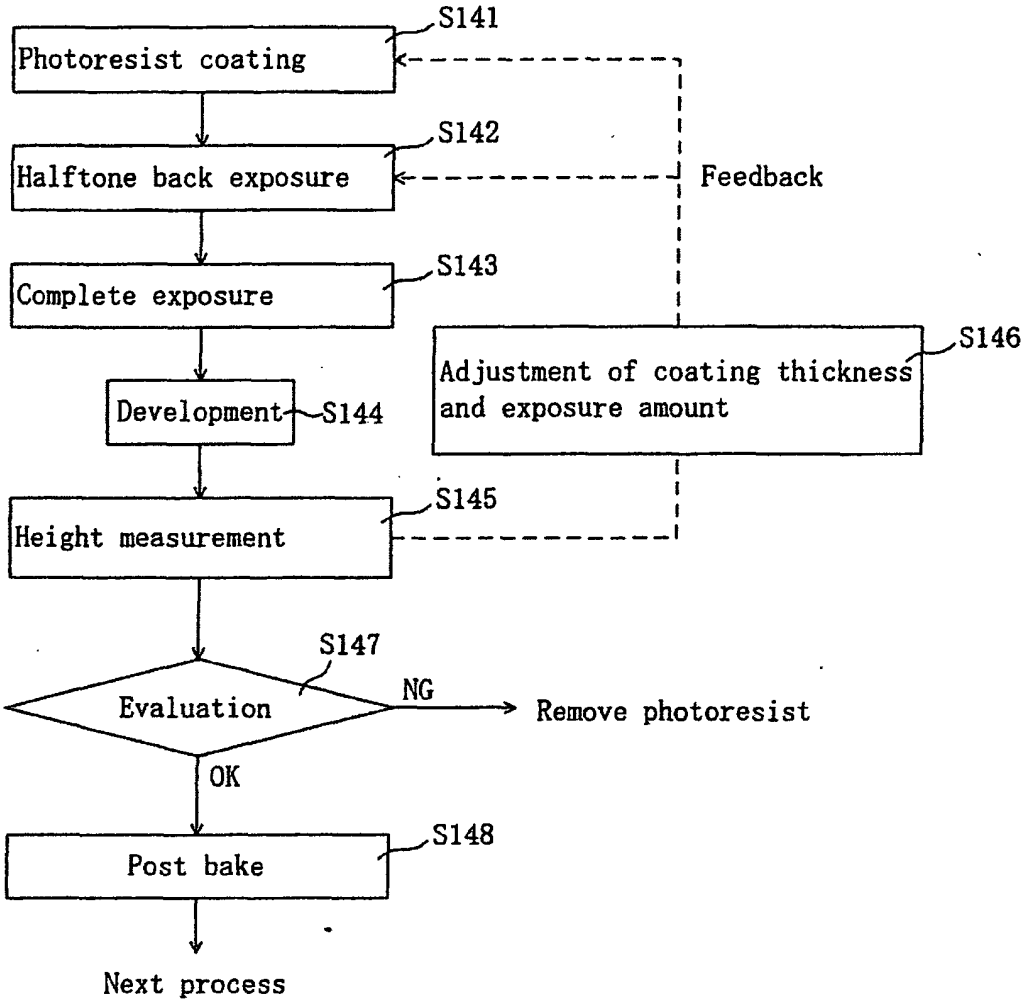
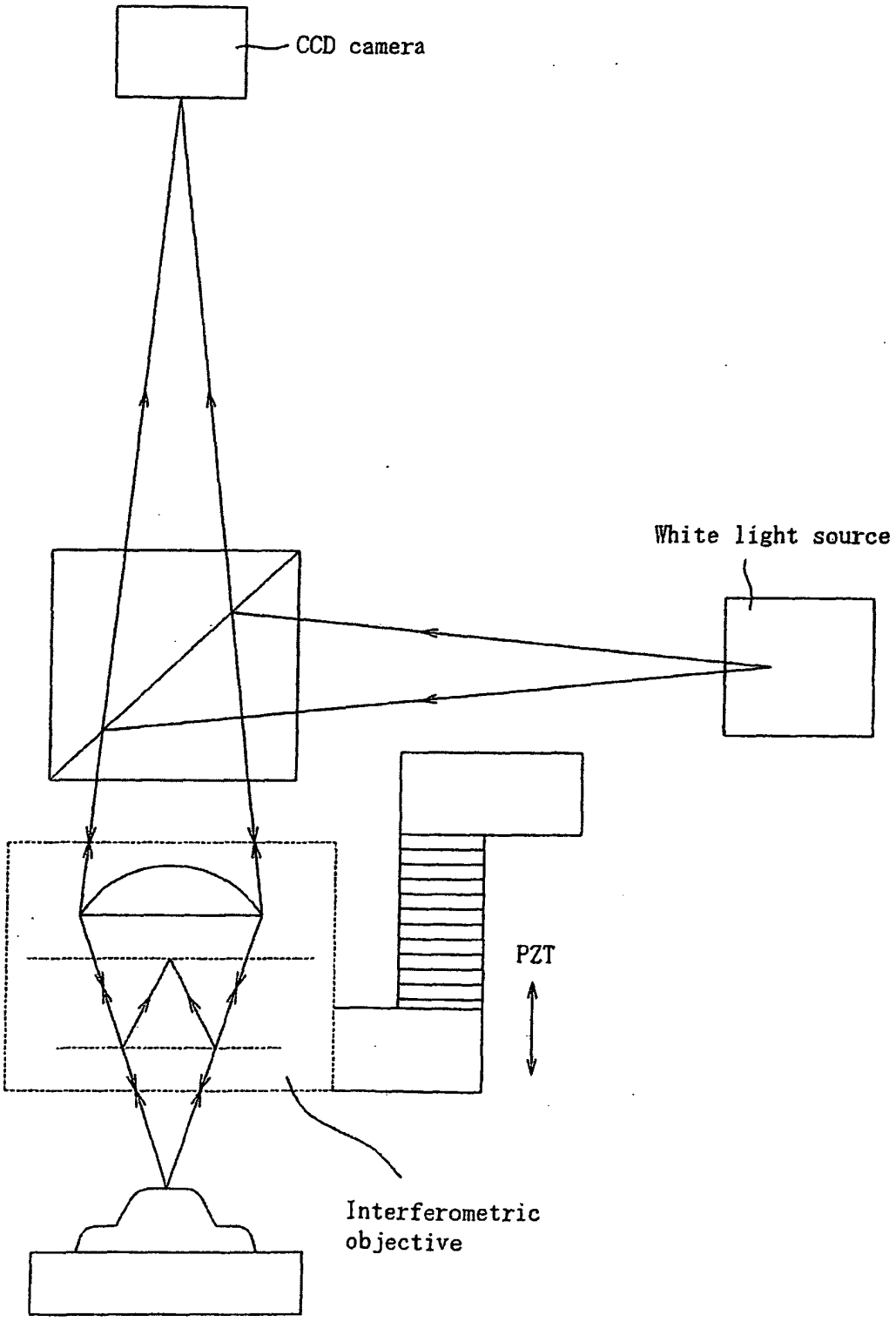

S141
Photoresist coating
S142
Halftone back exposure
Feedback
S143
Complete exposure
S146
Adjustment of coating thickness and exposure amount
Development
S144
S145
Height measurement
S147
Evaluation
NG
Remove photoresist
OK
S148
Post bake
Next process

FIG. 137


CCD camera
White light source
PZT
Interferometric objective

REFERENCES CITED IN THE DESCRIPTION

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- JP 10325961 A **[0002]**
- JP 11024104 A **[0002] [0012]**
- JP 10055001 A **[0002]**
- JP 10170939 A **[0002]**
- JP 11052420 A **[0002]**
- JP 2000199904 A **[0003]**
- JP 2000019527 A **[0003]**
- JP 2000019526 A **[0003]**
- JP 2001209053 A **[0004] [0013]**
- JP 2002258321 A **[0005] [0015] [0016] [0020] [0057]**
- JP 2002323706 A **[0005] [0015] [0020] [0057]**
- US 20020149729 A **[0017]**
- JP 11267861 A **[0123]**

专利名称(译)	制造高质量和超大屏幕液晶显示装置的方法。		
公开(公告)号	EP2293141B1	公开(公告)日	2012-06-06
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[标]申请(专利权)人(译)	大林精工株式会社		
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当前申请(专利权)人(译)	OBAYASHISEIKOU CO.，LTD.		
[标]发明人	HIROTA NAOTO		
发明人	HIROTA, NAOTO		
IPC分类号	G02F1/1343 G02F1/1339 G02F1/1362 G03F7/20 G02F1/1333 G02F1/1345 G02F1/1368 H01L21/3205 H01L21/336 H01L29/786		
CPC分类号	G02F1/133707 G02F1/133753 G02F1/13394 G02F1/134309 G02F1/134363 G02F1/1362 G02F1/136204 G02F2001/136218 G02F2001/136231 G02F2001/136236 G02F2001/13629 G02F2201/48 A61B5/0537 A61B5/4519 A61B5/4872 A61B5/4875 A61B5/7425 B42D15/00		
优先权	2003185823 2003-05-14 JP		
其他公开文献	EP2293141A1		
外部链接	Espacenet		

摘要(译)

一种使用横向电场系统的大屏幕液晶显示装置，其能够以低成本和高产量显着地改善孔径比，透射比，亮度和对比度。例如，可以显着减小屏蔽视频信号线的电场的公共电极的宽度，并且可以显着提高孔径比。特别是，覆盖视频信号线的凸块可以与间隔物一起使用，并且通过使用半色调曝光方法，可以同时构造覆盖视频信号线和间隔物的凸块，这大大缩短了所需的时间。用于生产过程。