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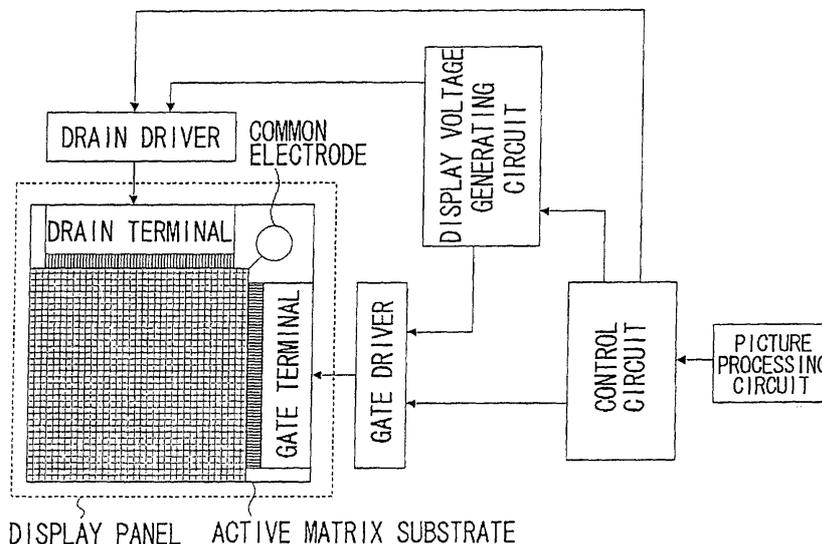
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AL LT LV MK RO SI</p> <p>(30) Priority: 03.07.2001 JP 2001201850</p> <p>(71) Applicant: NEC LCD Technologies, Ltd. Kawasaki, Kanagawa 211-8666 (JP)</p> | <p>(72) Inventor: Yamaguchi, Hirota, c/o Nec Corporation Minato-ku, Tokyo (JP)</p> <p>(74) Representative: Patentanwälte Wenzel & Kalkoff Grubessallee 26 22143 Hamburg (DE)</p> |
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(54) **Method for producing a liquid-crystal display apparatus**

(57) To provide a liquid crystal display apparatus exhibiting optimum display performance despite reduction in the number of (photolithography) processes, and a method for producing the apparatus. A method for producing a liquid crystal display apparatus having a first substrate including a thin film transistor and a reflector on an insulating substrate. An etching mask(24) is formed on a metal layer(3a, 25, and 26) formed on the insulating substrate(1) and, using this etching mask, the

metal layer is etched to form a constituent portion(3a) of the thin film transistor and protrusions. Only the etching mask is caused to reflow to cover exposed surface portions of the constituent portion(3a) of the thin film transistor and protrusions(26) and near-by surface portions of the insulating substrate with the etching mask as the insulating substrate is partially exposed. Using the etching mask, recesses are formed in an exposed area of the insulating substrate. A reflector(4a ,4b) is formed on the protrusions and recesses.

FIG . 1





European Patent
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EUROPEAN SEARCH REPORT

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
D,A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 03, 31 March 1999 (1999-03-31) -& JP 10 319422 A (SHARP CORP), 4 December 1998 (1998-12-04) * abstract * * figures *	1-13	G02F1/1335 G02F1/1362
A	--- PATENT ABSTRACTS OF JAPAN vol. 1996, no. 10, 31 October 1996 (1996-10-31) & JP 08 160462 A (SANYO ELECTRIC CO LTD), 21 June 1996 (1996-06-21) * abstract *	1-13	
A	--- US 4 519 678 A (MUNAKATA EIKO ET AL) 28 May 1985 (1985-05-28) * figure 8 * -----	1-13	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G02F
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	1 December 2003	Gill, R	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 02 09 0225

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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01-12-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 10319422 A	04-12-1998	JP 3012596 B2	21-02-2000
		DE 69220643 D1	07-08-1997
		DE 69220643 T2	22-01-1998
		EP 0536898 A1	14-04-1993
		JP 2825713 B2	18-11-1998
		JP 6075238 A	18-03-1994
		US 5408345 A	18-04-1995

JP 08160462 A	21-06-1996	NONE	

US 4519678 A	28-05-1985	JP 58125084 A	25-07-1983
		CA 1191588 A1	06-08-1985
		DE 3363206 D1	05-06-1986
		EP 0084930 A1	03-08-1983

专利名称(译)	制造液晶显示装置的方法		
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优先权	2001201850 2001-07-03 JP		
其他公开文献	EP1273961A2		
外部链接	Espacenet		

摘要(译)

提供尽管(光刻)工艺数量减少而显示出最佳显示性能的液晶显示装置,以及制造该装置的方法。一种制造液晶显示装置的方法,该液晶显示装置具有在绝缘基板上包括薄膜晶体管和反射器的第一基板。在形成在绝缘基板(1)上的金属层(3a,25和26)上形成蚀刻掩模(24),并且使用该蚀刻掩模蚀刻金属层以形成金属层的构成部分(3a)。薄膜晶体管和突起。仅使蚀刻掩模回流以覆盖薄膜晶体管的构成部分(3a)的暴露表面部分和突起(26)以及绝缘基板的附近表面部分,其中蚀刻掩模作为绝缘基板是部分的裸露。使用蚀刻掩模,在绝缘基板的暴露区域中形成凹槽。反射器(4a,4b)形成在突起和凹槽上。

FIG . 1

